High Dynamic Range Power Amplifiers to Support Modern Communication Standards

by

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ABSTRACT

Recent advancements in communication standards, such as 5G demand transmitter hardware to support high data rates with high energy efficiency. With the revolution of communication standards, modulation schemes have become more complex and require high peak-to-average (PAPR) signals. In wireless transceiver hardware, the power amplifier (PA) consumes most of the transceiver's DC power and is typically the bottleneck for transmitter linearity. Therefore, the transmitter's performance directly depends on the PA. To support high PAPR signals, the PA must operate efficiently at its saturated and backoff output power. Maintaining high efficiency at both peak and backoff output power is challenging. One effective technique for addressing this problem is load modulation. Some of the prominent load-modulated PA architectures are outphasing PAs, load-modulated balanced amplifiers (LMBA), envelope elimination and restoration (EER), envelope tracking (ET), Doherty power amplifiers (DPA), and polar transmitters. Amongst them, the DPA is the most popular for infrastructure applications due to its simpler architecture compared to other techniques and linearizability with digital pre-distortion (DPD).

Another crucial characteristic of progressing communication standards is wide signal bandwidths. High-efficiency power amplifiers like class J/F/F^1 and load-modulated PAs like the DPA exhibit narrowband performance because the amplifiers require precise output impedance terminations. Therefore, it is equally essential to develop adaptable PA solutions to process radio frequency (RF) signals with wide bandwidths.

To support modern and future cellular infrastructure, RF PAs need to be innovated to increase the backoff power efficiency by two times or more and support ten times or more wider bandwidths than current state-of-the-art PAs. This work presents five RF PA analyses and implementations to support future wireless commu-

nications transmitter hardware. Chapter 2 presents an optimized output-matching network analysis and design to achieve extended output power backoff of the DPA. Chapters 3 and 4 unveil two bandwidth enhancement techniques for the DPA while maintaining extended output power backoff. Chapter 5 exhibits a dual-band hybrid mode PA design targeted for wideband applications. Chapter 6 presents a built-in self-test circuit integrated into a PA for output impedance monitoring. This can alleviate the PA performance degradation due to the variation in the PA's output load over frequency, process, and aging. All RF PAs in this dissertation are implemented using Gallium Nitride (GaN)-based high electron mobility transistors (HEMT), and the realized designs validate the proposed PAs' theories/architectures.

DEDICATION

To my husband, Parijat

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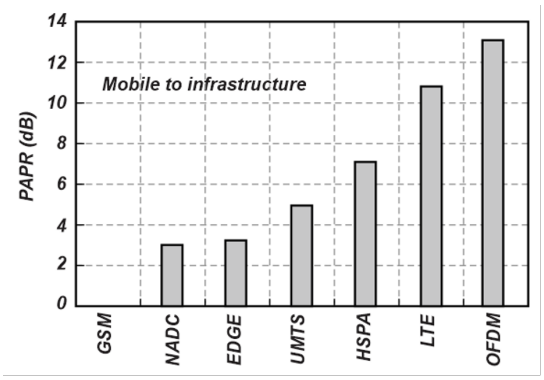
INTRODUCTION

With the fast growth of communication standards, modulation schemes have become increasingly complex to accommodate a large number of users within a fixed bandwidth. Figure 1.1a shows the increasing peak-to-average power ratio (PAPR) requirements with the advancement of modulation standards. As the wireless industry moves towards 5G, the transceiver hardware must process modulation schemes like Orthogonal Frequency Division Multiplexing (OFDM), which exhibits more than 10 dB PAPR. The efficiency of the transceiver is directly related to the PAPR. As shown in Figure 1.1b, for a 6 dB PAPR signal, most of its signal density lies at the backoff power and not at peak power. Therefore, the wireless industry demands high-efficiency transceivers at peak and backoff power levels to process these high PAPR signals.

Another crucial characteristic of progressing communication standards is wide signal bandwidths. Figure 1.1c illustrates the growing bandwidth requirement with evolving communication standards. Wideband or multi-band transceivers have become necessary to eliminate hardware redundancy while at the same time maintaining competitive output power and efficiency. In the transceiver, the power amplifier (PA) is the most power-hungry component, and the transceiver's overall efficiency depends directly on the PA efficiency. To support the high PAPR and wideband operation requirements, the wireless industry demands high saturated power, high optimized backoff power, and high-efficiency PAs [3],[4].



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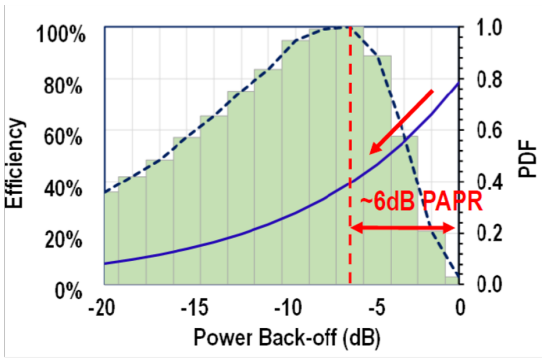

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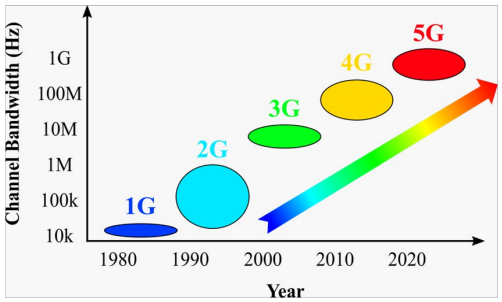


(c)

Figure 1.1: (a) PAPR Requirement of Different Modulation Standards [2], (b) Efficiency and Probability Density Function of a Modulated Signal Versus Power Backoff [5], and (c) Trend of Bandwidth Requirement for Modern Communication Standards [6].

1.1 Different Classes of PAs

Based on the PA's bias conditions, PAs are classified into four types: class A, class B, class AB, and class C [7]. The PA's drain efficiency depends on the conduction angle. Drain efficiency increases as the conduction angle decreases from class A to C. However, linearity decreases when moving from class A to class C. Class A is the most linear PA with the lowest drain efficiency, whereas class C has theoretically 100% drain efficiency with high nonlinearity. A PA architecture is selected based on the target application and specifications for the hardware. The conduction angles for different modes are summarized in Table 1.1 [8]. Class AB PAs are the basic building

Table 1.1

Basic PA Types

Class	I_{DQ}	Conduction Angle	Efficiency %
A	$\frac{I_{max}}{2}$	2π	50
AB	0 to $\frac{I_{max}}{2}$	π to 2π	50 to 78.54
B	0	π	78.54
C	0	0 to π	78.54 to 100

block of most load-modulated power amplifier architectures (for example, Doherty, Load Modulated Balanced Power Amplifier (LMBA), and Envelope tracking).

1.2 Waveform Engineered PAs

Compared to class AB/B amplifiers, waveform-engineered or harmonic-tuned PAs [7], [10] offer better performance (e.g., higher efficiency, power, and gain). A conceptual model demonstrating the operation of a waveform-engineered PA is shown in Figure 1.2. Waveshaping is achieved by providing specific impedance terminations for the fundamental and higher-order harmonics. In Figure 1.2, the fundamental impedance component is terminated by R_{Opt}. The active device is biased at class AB/B mode. The purpose is to control the drain-source voltage and current waveforms. Theoretically, an infinite number of harmonic terminations are required. In practice, only a finite number of harmonic controls is possible. The following subsections summarize the most prominent types of waveform-engineered PAs: the class F, F^{-1}, and J.

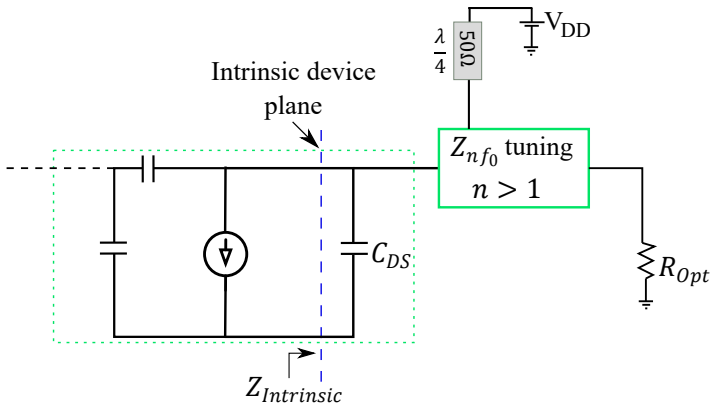


Figure 1.2: A Simple Model for Waveform Engineered PA.

Class F and F^{-1} PA

Class-F and F^{-1} [9], [11], [12], [13] power amplifiers employ harmonic frequency resonators to shape their drain (or collector) waveforms to improve efficiency. Class F^{-1} is the dual of Class F and has been mostly used in low-voltage PAs for monolithic applications. For PAs operating close to their active device's f_{max}, Class F^{-1} is easier to implement. The voltage and current waveform relationships for the class F amplifier are shown in equations 1.1-1.2, and the voltage and current waveforms are interchanged in the case of class F^{-1}.

$$V_{DS,ClassF} = V_{DD} + V_1 \sin(\theta) + V_3 \sin(3\theta) \tag{1.1}$$

$$I_{DS,ClassF} = I_{DC} - I_1 \sin(\theta) + I_2 \cos(2\theta) \tag{1.2}$$

The 2nd and 3rd harmonics are short and open for class F PA operation. These harmonic terminations are reversed in a class F^{-1} PA.

$$ClassF \begin{cases} Z_{f0} = R_{f0} \\ Z_{nf0} = 0, & \text{for even n} \\ Z_{nf0} = \infty, & \text{for odd n} \end{cases} \tag{1.3}$$

$$ClassF^{-1} \begin{cases} Z_{f0} = R_{f0} \\ Z_{nf0} = \infty, & \text{for even n} \\ Z_{nf0} = 0, & \text{for odd n} \end{cases} \tag{1.4}$$

The voltage-current relationships are shown in Figure 1.3

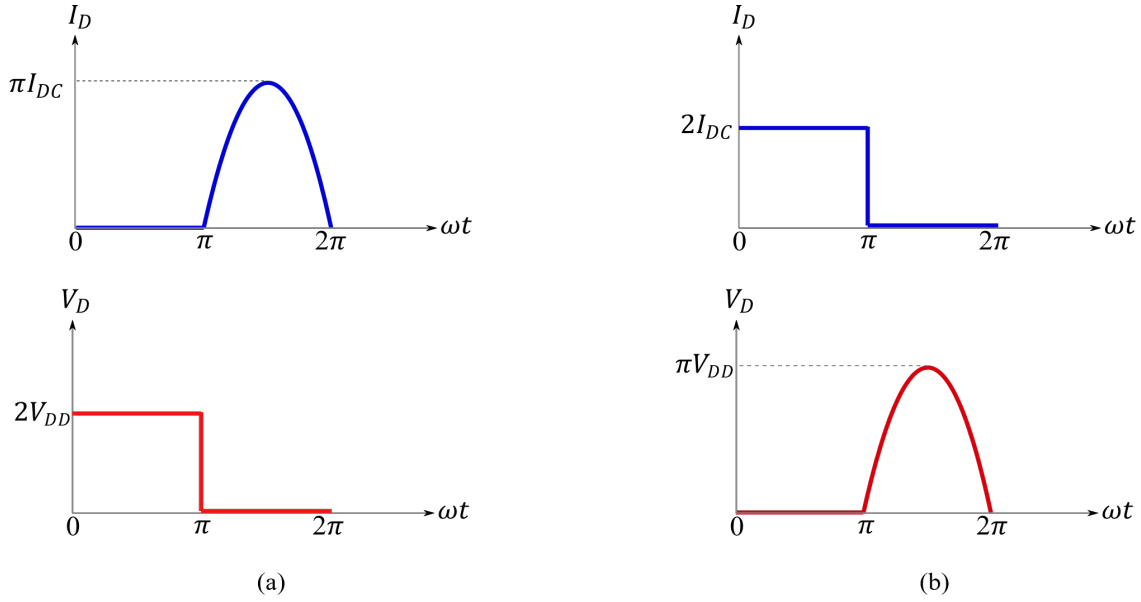


Figure 1.3: Voltage and Current Waveforms of (a) Class F and (b) Class F^{-1} PA.

Class J PA

The class J PA [17], [18], [19], [20] was first introduced by S.C. Cripps, and exhibits the same performance as a class B PA with different load terminations to allow for

easier realization of PAs. Instead of short-circuiting the 2nd harmonic as in a class B PA, the 2nd harmonic is terminated by reactive impedance (-jX_2 or +jX_2). Also, at the fundamental frequency, the impedance is complex (R_1+jX_1, or R_1-jX_1), unlike a class B PA where the impedance is typically real. As a result of these impedance terminations, the maximum voltage increases from class B, and class J has a partial overlap between the current and voltage waveforms. However, the theoretical drain efficiency of a class J PA is the same as a class B PA, 78.5%.The voltage and current waveforms are shown in Figure 1.4, and the mathematical relation is described in equations 1.5 and 1.6.

$$V_{DS,ClassJ} = V_{DD}(1 - cos(\theta))(1 - sin(\theta)) \tag{1.5}$$

$$I_{DS,ClassJ} = I_{max}(\frac{1}{\pi} + \frac{1}{2}\cos(\theta) + \frac{2}{3\pi}\cos(2\theta)) \tag{1.6}$$

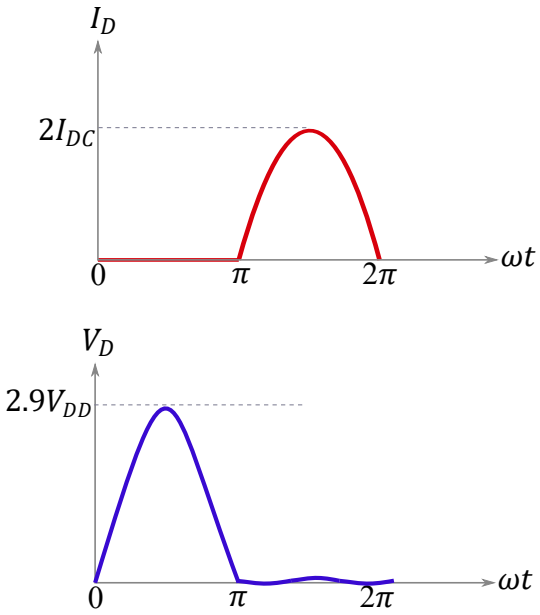


Figure 1.4: Typical Voltage and Current Waveform of Class J PA.

The impedance relationships are shown in equation 1.7.

$$ClassJ \begin{cases} Z_{f0} = R_1 + jX_1 \\ Z_{2f0} = -jX_2 \\ Z_{3f0} = 0 \end{cases} \tag{1.7}$$

Unlike class, F/F^{-1} PAs, class J PAs do not need harmonics to be strictly terminated by open/short circuits. This gives design flexibility to maximize the PA performance and ensure broadband performance, even in the presence of parasitics when realizing the design. This idea has been further expanded by other researchers to continuous mode PAs [13], [14], [15], [16], [19], where the PA holds good performance (e.g. high PAE, gain) for different load conditions. Therefore, continuous-mode PAs have become a promising architecture for broadband PA applications.

1.3 Doherty Power Amplifier (DPA)

The Doherty power amplifier [21], [22] was invented and published by W.H. Doherty in the year 1936. The DPA was first introduced for AM transmitters; however, in the mid-2000s, the DPA became famous for cellular infrastructure. The DPA gained popularity with the advent of high dynamic range applications, as the DPA can support 8-10 dB PAPR signals. With digital pre-distortion techniques, DPAs can be easily linearized to meet the requirements of these present-day communication standards. The architecture of a DPA is shown in Figure 1.5. The DPA consists of two amplifiers: the carrier amplifier and the peaking amplifier. The peaking amplifier modulates the output impedance of the carrier amplifier. The carrier amplifier is generally biased in class B/AB mode, and the peaking amplifier is biased in class C mode. The RF input signal is equally divided between the two amplifiers using a splitter. Generally, a hybrid branch line coupler or a Wilkinson power divider is used.

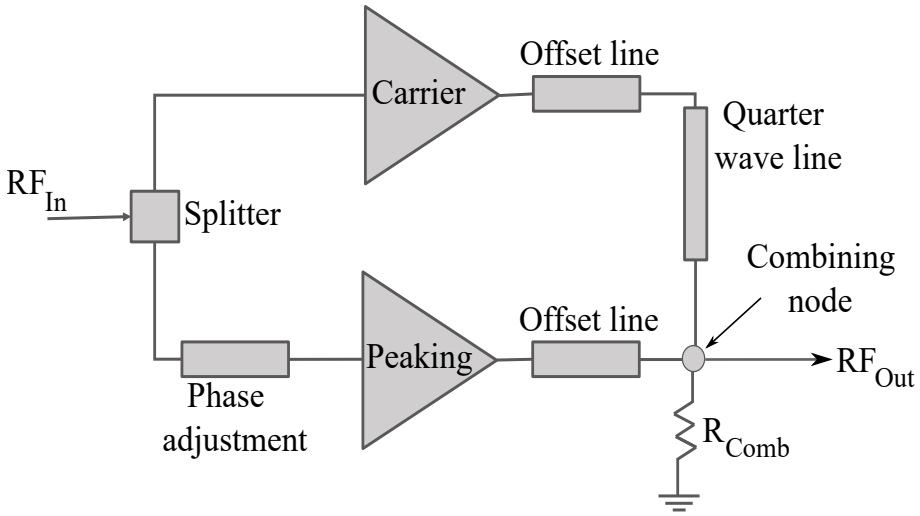
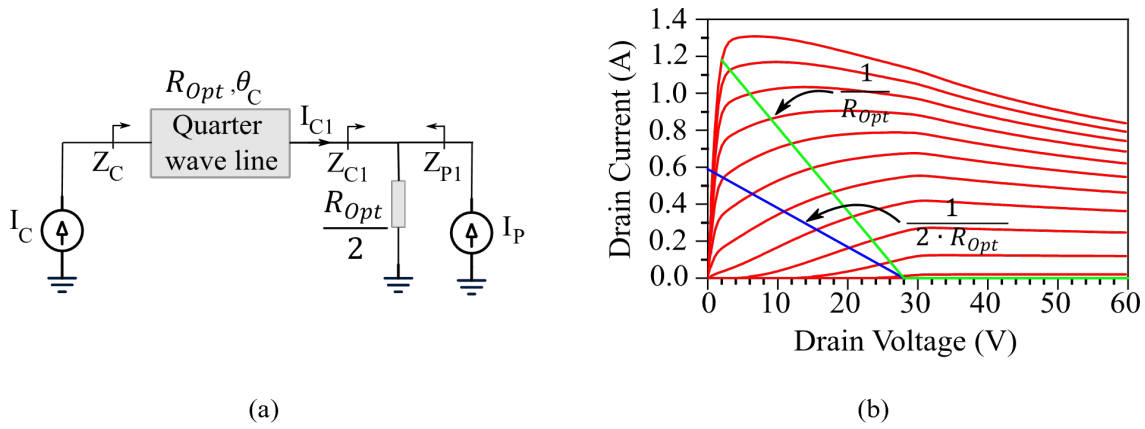


Figure 1.5: Basic Architecture of a DPA.

The most important part of the DPA is the quarter wave transmission line (QWTL) at the PA's output. Load modulation is mainly achieved by using the QWTL. The offset lines at the output and the phase adjustment transmission lines at the input ensure accurate phase alignment between the carrier and peaking paths. Finally, the output is measured across the combining node resistor R_{Comb}. The carrier and peaking amplifiers are replaced by ideal current sources to analyze the DPA operation, as shown in Figure 1.6a. The offset and phase adjustment lines are removed from the diagram for simplification. In Figure 1.6a, I_C and I_P are currents at the carrier and peaking PA's intrinsic device plane, and I_{C1} is the carrier current at the combining node. The carrier and peaking PAs' impedances at the combining node are expressed as Z_{C1} and Z_{P1}, respectively. The impedance is denoted Z_C at the carrier PA's intrinsic device plane. The impedances can be expressed in terms of currents at the



(a) (b)

Figure 1.6: (a) Conceptual Diagram of a DPA, and (b) Load Line of the Carrier Amplifier at Low and High-power DPA Operation.

combining node.

$$Z_{C1} = \frac{R_{Opt}}{2}(1 + \frac{I_P}{I_{C1}}) \tag{1.8}$$

$$Z_{P1} = \frac{R_{Opt}}{2}(1 + \frac{I_{C1}}{I_P}) \tag{1.9}$$

$$Z_C = \frac{R_{Opt}^2}{Z_{C1}} \tag{1.10}$$

R_{Opt} is the optimum impedance of the PA for generating maximum output power. The DPA has two operational modes: low-power and high-power operation. At low-power operation, the peaking PA is off as the input drive is too low to turn on the class C biased PA. Therefore, at low-power operation, only the carrier PA conducts current. Z_{C1-BO} becomes $\frac{R_{Opt}}{2}$ and $Z_{P1-BO} = \infty$. At the carrier PA's intrinsic device plane, $Z_C = 2 \cdot R_{Opt}$. Figure 1.6b shows the load line of the DPA. For low-power operation, the blue line shows the approximate load line of the DPA with a slope of $\frac{1}{2 \cdot R_{Opt}}$. In high-power operation, carrier and peaking PAs conduct current, and at maximum input drive, $I_{C1} = I_P$. In this mode of operation, current from the peaking PA modulates the carrier's load impedance. At high power, $Z_{C1-SAT} = R_{Opt}$ and $Z_C = R_{Opt}$. In Figure 1.6b, the green line represents the load line of the carrier

PA for high-power operation. The slope of the line is $\frac{1}{R_{Opt}}$. Therefore, the load of the carrier PA is modulated by the peaking PA from $2 \cdot R_{Opt}$ to R_{Opt}. From the knowledge of impedance (Z_C) and current (I_C) at the device intrinsic plane, the drain efficiency of the DPA is plotted in Figure 1.7. The DPA exhibits two peaks in drain efficiency, reaching 78.5% when operating at both saturated and backoff power levels. The plot also compares the DPA efficiency with a standard class B PA. It is evident that at power backoff, the DPA achieves significantly better efficiency compared to a class B PA. Figure 1.7 shows DPA drain efficiency characteristics at different output

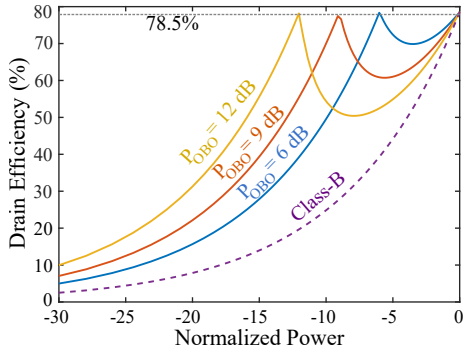


Figure 1.7: Typical Drain Efficiency Characteristics of a DPA and a Class B PA.

power backoff (P_{OBO}) levels. The P_{OBO} defines the peaking amplifier turn-on point. Different P_{OBO} levels are achieved by varying $\alpha = I_P/I_{C1}$ ratio.

$$P_{OBO} = 20 \cdot \log(1 + \alpha) \tag{1.11}$$

For the conventional DPA case explained above, $I_{C1} = I_P$, $P_{OBO} = 6$ dB. The DPA can also operate in an asymmetrical mode where $I_{C1} \neq I_P$, typically $I_P > I_{C1}$ to achieve a higher P_{OBO} than 6 dB. If the DPA is operated in asymmetrical mode, $R_{Comb} = \frac{R_{Opt}}{(1+\alpha)}$. High P_{OBO} can be achieved by using an asymmetrical DPA configuration, however as the P_{OBO} increases, the drain efficiency between the backoff and saturated power drops. The same situation is observed in Figure 1.7. For example, the drain efficiency between 12 dB P_{OBO} and saturated power dips much lower than a 9 dB P_{OBO} DPA.

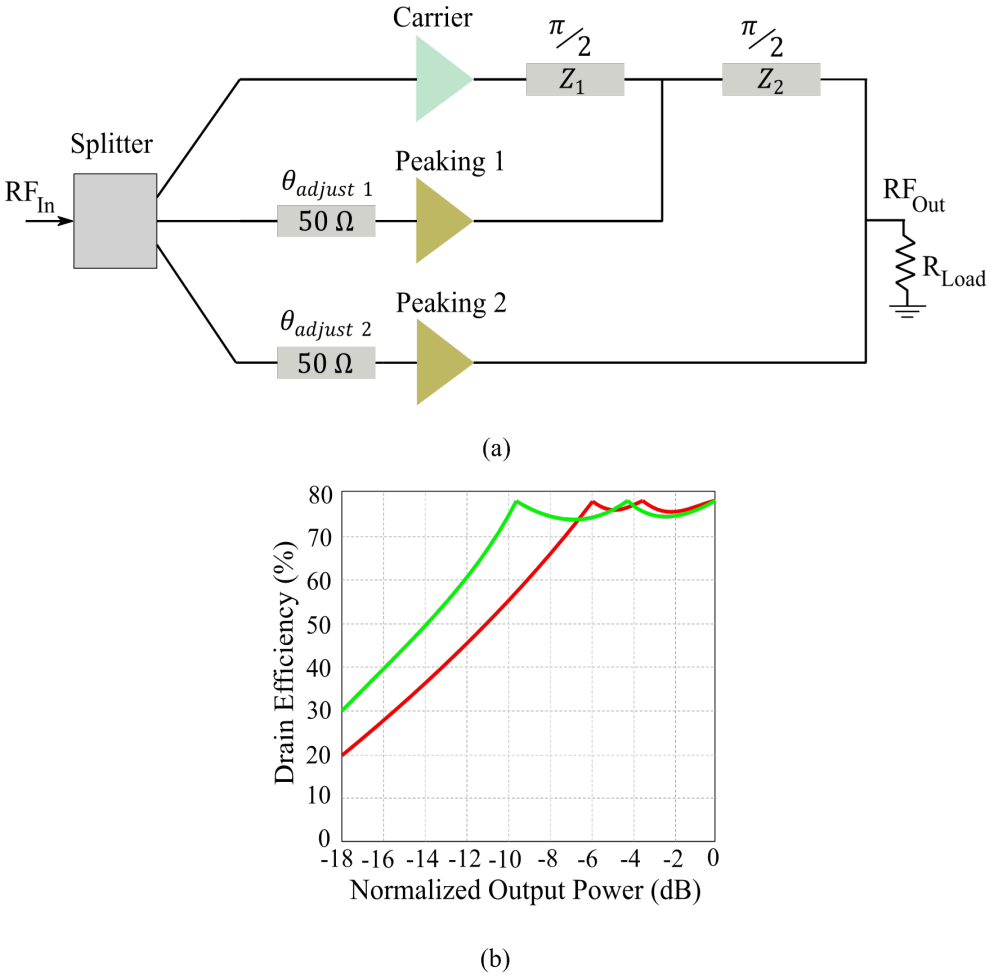


Figure 1.8: (a) 3-way DPA, (b) Drain Efficiency Characteristics.

To address this issue, multi-stage or multi-way DPAs can be realized. Instead of one peaking amplifier, as shown in Figure 1.5 and known as a 2-way/stage DPA, multiple peaking amplifiers are used in parallel to introduce multiple peaks at backoff power. The carrier and peaking amplifier PAs' sizing depends on the target backoff efficiency peaks. For example, a 3-way/stage DPA is shown in Figure 1.8a. Different backoff combinations can be achieved by varying the carrier and peaking amplifiers' sizes. To achieve 6 dB P_{OBO}, symmetrical carrier and peaking devices are used, and the drain efficiency response will look like the red curve in Figure 1.8b. It should be noted that

the efficiency between 6 dB backoff and saturated power is much higher compared to the conventional case shown by the blue curve in Figure 1.7. Another example is shown by the green curve (Figure 1.8b) for 9.5 dB P_{OBO}, where the carrier, peaking PA 1, and peaking PA 2 sizing ratio is 1:2:2. By controlling the transistors' sizing, different backoff combinations can be achieved. Although multi-stage DPAs (also known as N-Way Doherty) can offer efficiency advantages, they are more complex and challenging to implement than the conventional 2-way DPA. The overall gain is also decreased due to the multi-way input division.

Drawbacks in DPAs

DPAs are popular for effectively processing high PAPR signals. Unfortunately, these DPAs, in general, suffer from bandwidth limitations [31] due to the presence of a quarter wave transmission line (QWTL), offset lines for phase adjustment, the limited bandwidths of output and input matching networks, and device parasitics.

Several methods have been proposed to overcome this frequency limitation in DPAs. The state-of-the-art techniques are broadly classified into four categories.

1. Modifying the output combing network, this is implemented by:
    - Changing the combining load impedance from $\frac{R_{Opt}}{2}$
    - Parallel combining
    - Modified output combiner architecture
2. Parasitic compensation
    - Absorbing drain-to-source capacitance of the active device (C_{Out}) into the output matching network.
3. Post matching DPAs

- The carrier and peaking PAs' impedance matching networks are realized by simple low-pass networks to extend the bandwidth.
- A broadband impedance matching network is used at the output of the DPA to transform the load resistance into the optimum resistance for broadband operation.

4. Continuous-mode DPAs

   - Using non-infinite peaking impedance, the DPA achieves continuous class J mode at power backoff. Due to the class J characteristics, the DPA can achieve wide bandwidth at power backoff.
   - At saturated power, the DPA behaves like a conventional DPA.

The design implementations of parallel combining (category 1) and continuous-mode DPA (category 4) techniques are discussed in later chapters.

1.4 Broadband PAs

Broadband PA architectures can be generally categorized into the following types:

- Distributed PAs
- Non-uniform distributed PAs
- Dual band/Multi-band PAs
- Hybrid mode PAs

The different architectures are briefly described in the following subsections.

Distributed PA

The distributed amplifier [42]-[45] is a unique circuit in the field of high-frequency microwave engineering for broadband applications. The basic configuration of the distributed PA using N identical FETs is shown in Figure 1.9. The gates of all FETs are connected to a transmission line having a characteristic impedance Z_g and length l_g. Similarly, the drains are connected to a transmission line of characteristic impedance Z_d, with a spacing l_d. The input and output capacitance of the transistors are absorbed in the gate and drain transmission lines. To ensure good matching, the gate and drain ports are terminated using resistors Z_g and Z_d. As the input signal propagates, the gate terminal of each FET taps, therefore of the input power, and the amplified signal travels down the drain line. Finally, the output signal from each FET is constructively added at the output terminal.

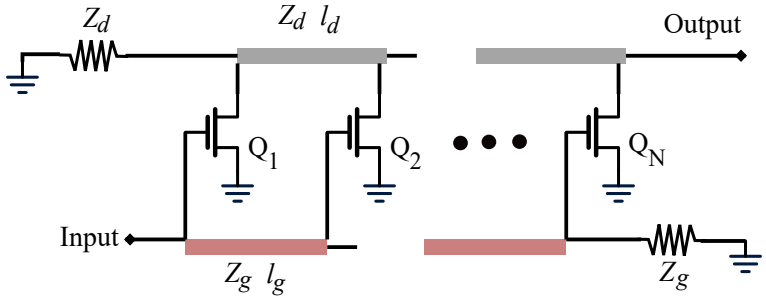


Figure 1.9: Configuration of Distributed Amplifier.

Although the distributed amplifier is a popular choice for broadband applications, the distributed amplifier has some drawbacks. The output signal travels in the reverse direction and dissipates in Z_d, which affects the output power and power-added efficiency (PAE). The transistors do not tap the input uniformly, therefore, the contributions from all of the FETs at the output are not uniform. In most cases, PAE $<$ 20% at saturated power and even lower at 3-6 dB power backoff. This topology may not be the optimum choice when high PAE is required.

Non-Uniform Distributed PA

A Non-Uniform Distributed Power Amplifier (NDPA) [46]-[50] topology incorporating N non-identical transistors is typically used to improve output power and PAE of a distributed PA. A typical NDPA architecture is shown in Figure 1.10. Unlike the

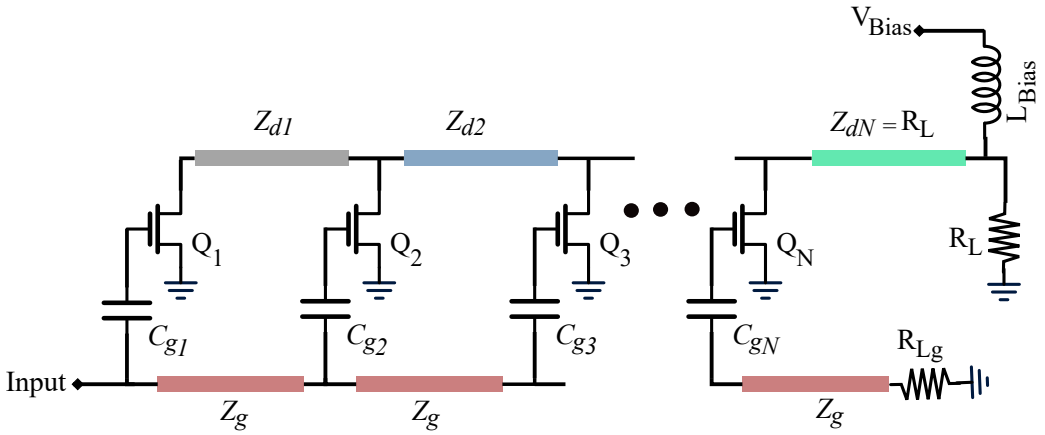


Figure 1.10: Architecture of Non-Uniform Distributed Power Amplifier.

distributed amplifier, the NDPA drain termination resistor Z_d is removed to reduce the reverse traveling signal. The left side is terminated by an output impedance of Q_1. To ensure proper loading of the transistors, the drain transmission line is tapered, while the highest impedance line is connected to Q_1, and the last stage has the characteristic impedance of R_L.

The drawback of this architecture is its realizability. For a large number of gain stages N, lines with high characteristic impedance might be too narrow for implementation.

Dual-Band and Multi-Band PAs

Dual-band or multi-band PAs [51]-[53] have more than one operational frequency. This class of PAs can provide good performance at the frequency band of interest

compared to a PA covering the whole contiguous band of operation. Depending on the architecture, multi-band PAs are broadly classified as employing 3 techniques:

- Reconfigurable components like varactors or RF switches are used to select the required RF path. However, a low-quality factor of the varactor(s) or high on-resistance of the switch(es) causes high loss.
- It has a shared input matching network (IMN) branch and two separate output matching network (OMN) branches connected via a T-type network.
- Two separate IMN and OMN, connected via a diplexer.

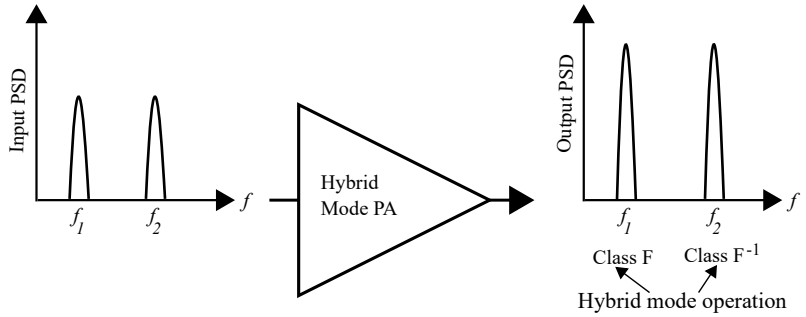


Figure 1.11: Conceptual Diagram of Hybrid Mode PA.

Hybrid Mode PAs

Waveform-engineered PAs (e.g., class J/F/F^{-1}) demonstrate state-of-the-art performance (higher drain efficiency and output power compared to class B/AB) at a specific design frequency. Still, they are narrowband due to their specific harmonic terminations. Dual-band or multiband PAs can be designed using the hybrid PA building block [28], [54]-[55]. Figure 1.11 illustrates the concept of a hybrid mode PA. For example if at frequency f_1, the PA functions as class F, then at f_2 the PA will operate as class F^{-1}. The narrowband nature of the specific class of PA would not limit it. At

both f_1 and f_2, the PA will achieve target performances from class F and class F^{-1} modes, respectively. Similar works have been realized previously in SiGe BiCMOS [54] and 45nm CMOS SOI, reporting output power less than 20 dBm. For hybrid mode dual-band PA implementation, f_1 and f_2 should be lower than each frequency's odd and even harmonics.

$$f_1 \text{ and } f_2 \ll 2f_1, 2f_2, 3f_1, 3f_2$$

Otherwise, the fundamental signal will superimpose with the harmonics, and specific harmonic terminations would be challenging to achieve without filtering the fundamental. Due to this limitation, hybrid mode class F and F^{-1} implementations are challenging in the sub-6GHz frequency band.

1.5 Organization of the Work

The objective of this research is to innovate and develop GaN-based RF power amplifiers to support extended output power backoff and wide bandwidth requirements of modern wireless communications infrastructure. The organization of the chapters is as follows.

In Chapter 2, an optimized load network for a phase-exploited symmetrical DPA (PE-DPA) is presented to achieve higher output power backoff (OBO) using symmetrical carrier and peaking PA devices. The presented work explores the effect of non-linear phase distortion (NPD) on the output network and resulting drain efficiency. The work compares PE-DPA behavior from two different output networks and selects the one with superior performance for hardware implementation. The resulting PE-DPA is implemented at 3 GHz using Cree's GaN HEMT. The DPA delivers 44.3 dBm power at 3-dB compression (P3 dB), with a drain efficiency of 73% at P3 dB and 44% at 8 dB OBO under continuous wave excitation. The power spectral

density with a 20 MHz LTE signal is also reported.

Chapter 3 presents a PE-DPA with a Parallel Load Combining Network operating from 3.3-3.6 GHz. The presented DPA uses parallel combining to increase the bandwidth over a conventional DPA and phase exploitation to extend the high-efficiency backoff point beyond 6 dB. Detailed performance analysis with respect to frequency is presented for the phase exploited symmetric DPA with parallel load combining (PE-PDPA). To validate the presented technique, a prototype is designed using GaN HEMT devices, and simulation results demonstrate that the PE-PDPA achieves 60% − 77% efficiency at saturation and 43% − 54% efficiency at 8 dB backoff over the 3.3-3.6 GHz operating band. The PA maintains a 10 dB gain and an average of 43 dBm saturated power over the entire frequency range.

Chapter 4 presents a broadband asymmetrical continuous-mode class J Doherty power amplifier (PA) using complex combining load. The DPA functions as a class J PA when operating in the low-power region. The proposed Doherty PA (DPA) achieves continuous mode class J characteristics by varying the reactive part of the complex load. A novel post-matching network (PMN) has realized this variable complex combing load. A detailed theoretical analysis shows the impedance transformation procedure from the asymmetrical DPA impedance trajectory to a class J. To validate the proposed technique, a prototype PA has been designed with Cree GaN devices for 9 dB output power backoff (OBO) operating from 1.8 GHz to 2.6 GHz. In the aforementioned frequency band, the PA achieves 61% − 76% efficiency at saturation and 43% − 60% efficiency at OBO. The PA maintains a 10 dB gain and an average of 43 dBm power over the entire frequency range.

Chapter 5 presents an X-Ku hybrid-mode dual-band PA realized in a 40 nm GaN-on-SiC process. The PA operates in class F for the X band and F^{-1} for the Ku band. The detailed design procedure is explained in Chapter 5. The PA has above 45%

PAE and 30 dBm output power in both operating bands.

Chapter 6 reports a periodic structure-based built-in self-test (BIST) technique integrated into an RF PA to monitor impedance variation at the PA's output. The proposed circuit prototype is designed to withstand the high output power of the PA without saturating the power detectors used in the BIST circuit. Experimental results from 1.5-2.5 GHz with a commercially available power amplifier are presented. The test results show considerable convergence between the measured and test loads.

Chapter 2

OPTIMIZED LOAD NETWORK FOR PHASE EXPLOITED SYMMETRICAL DOHERTY POWER AMPLIFIERS

2.1 Introduction

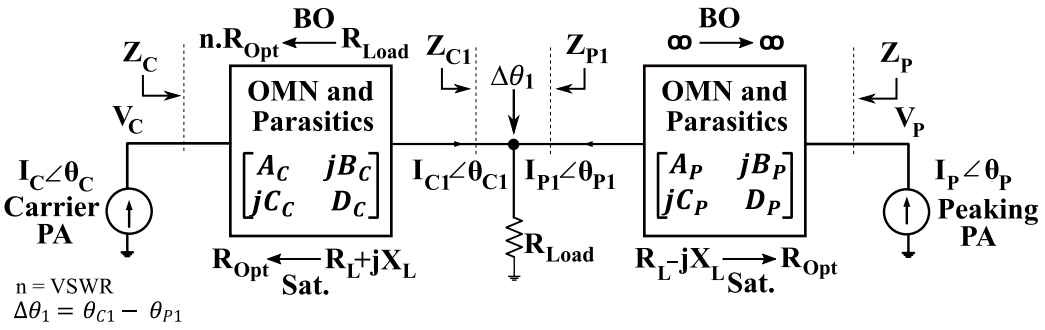


Figure 2.1: Conceptual Diagram of PE-DPA.

The chapter presents the design and analysis of a DPA to support signals with more than 6 dB PAPR. Several works have been done [23]-[29] that report extended output backoff (P_{OBO}) range than the conventional DPA (6 dB). One of the exciting techniques to extend the output backoff of the DPA is phase-exploited DPA (PE-DPA) [23]. It intentionally mismatches the phase of the carrier and peaking amplifier at the combining node to extend the output power backoff (P_{OBO}). The non-linear phase distortion (NPD) [30] in the DPA, mainly caused by the variation of the peaking PA's parasitic input capacitance with its input drive level, is a significant factor leading to drain efficiency degradation. It is crucial to address this issue to improve the system's overall performance. The prior work explored PE-DPA in detail and presented a closed form of output matching network (OMN) ABCD parameters. The ABCD parameters of the carrier and peaking amplifier have two distinct solutions for

OMNs. However, it did not consider the effect of NPD while choosing the solution for the matching networks of PE-DPA.

In this work, two PE-DPA designs based on two different ABCD parameters solutions are individually designed and optimized at 3 GHz using Cree's CG2H40010F GaN HEMT device. This letter explores both design solutions of PE-DPA and selects one for fabrication with better performance in the presence of NPD.

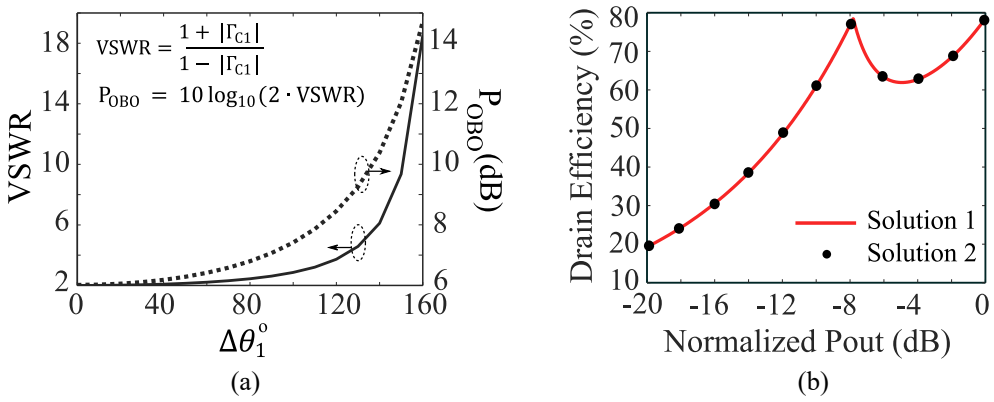


Figure 2.2: (a) VSWR and P_{OBO} Vs $\Delta\theta_1$, (b) Drain Efficiency Profile of Solution 1 and Solution 2 at $\Delta\theta_1 = 105°$.

2.2 Investigation of PE-DPA's output network

Figure 2.1 depicts the architecture of PE-DPA, where ideal current sources represent the carrier and peaking amplifiers. At power backoff, $Z_{C1,BO} = 0.5 \cdot R_{Opt}$, which transformed to $Z_{C,BO} = VSWR \cdot R_{Opt}$ by the carrier OMN, while maintaining $Z_{P1,BO} = \infty$. At saturation, it intentionally mismatches the phase ($\Delta\theta = \theta_{C1} - \theta_{P1}$) of the carrier and peaking amplifier, keeping their magnitude ($|I_{C1}| = |I_{P1}|$) the same at the combining node of the DPA. The impedance relations at saturation are shown

in equations 2.1-2.2.

$$Z_{C1,SAT} = R_{Load} \cdot (1 + \cos\theta_1 + j\sin\theta_1) \tag{2.1}$$

$$Z_{P1,SAT} = R_{Load} \cdot (1 + \cos\theta_1 - j\sin\theta_1) \tag{2.2}$$

For the conventional DPA, $\Delta\theta_1 = 0$ gives 6 dB OBO. As $\Delta\theta_1$ (> 0) further increases, higher OBO is achieved, shown in Figure 2.2a. For example, $\Delta\theta_1 = 105°$ can extend the OBO to 8 dB. To satisfy the load conditions mentioned above at saturation and backoff, the carrier and peaking amplifier OMNs should be designed accordingly. The OMSs' equivalent ABCD parameters were derived in detail in prior work and tabulated in table 2.1. It shows that the carrier and peaking OMNs have two possible solutions – *Solution 1*: all negative peaking ABCD parameters and positive root for CC and *Solution 2*: all positive peaking ABCD parameters and negative root for CC. The prior work opted for solution 1 and reported measured results at 2.2 GHz.

Table 2.1

ABCD Parameters of the Carrier and Peaking Amplifier of PE-DPA

Carrier ABCD parameters	Peaking ABCD parameters
$A_C = Q \cdot VSWR \cdot R_{Opt} \cdot R_{Load} \cdot C_C$	$A_P = \pm\sqrt{R_{Opt}/R_{Load}}$
$B_C = VSWR \cdot R_{Opt} \cdot R_{Load} \cdot C_C$	$B_P = \pm\sqrt{R_{Opt}/R_{Load}} \cdot X_L$
$C_C =$ $\pm 1/\sqrt{VSWR \cdot R_{Opt} \cdot R_{Load} \cdot ((Q \cdot R_{Load}) + 1)}$	$C_P = 0$
$D_C = Q \cdot R_{Load}^2 \cdot C_C$	$D_P = \pm\sqrt{R_L/R_{Opt}}$

Q = -((1- $\frac{R_L^2+X_L^2}{R_{Load}^2}$) $\pm\sqrt{(1 - \frac{R_L^2+X_L^2}{R_{Load}^2} + 4 \cdot \frac{X_L^2}{R_{Load}^2})}/(2 \cdot X_L)$

Theoretically, both solutions will generate a similar drain efficiency profile without any device non-linearity. An example plot is shown in Figure 2.2b, where drain

efficiencies for 8 dB OBO ($\Delta\theta_1 = 105°$) are plotted using the ABCD parameter from table 2.1.

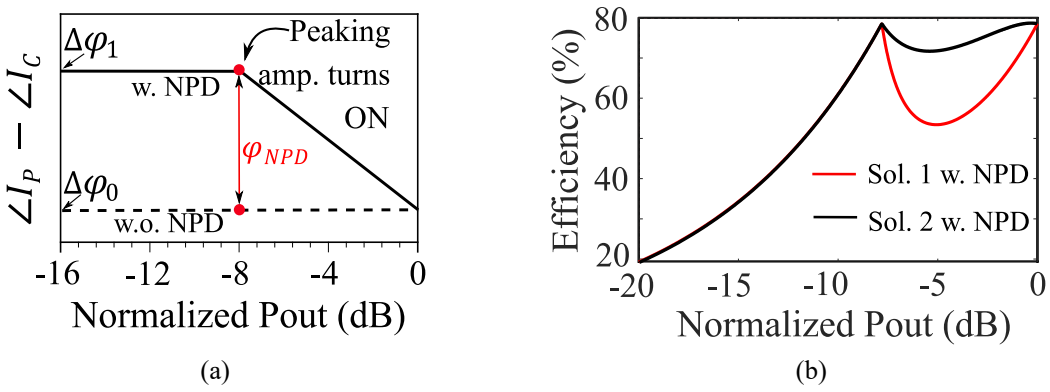


Figure 2.3: (a) Standard NPD Profile for the DPA, (B) Drain Efficiency Profile for Both Solutions with NPD Effect.

The prior work's analysis did not incorporate NPD's effect on the two solutions. The class C biased peaking amplifier experiences a significant variation of the input capacitance with the increasing input power drive, which causes deviation in the dynamic load trajectories of both the carrier and peaking PA, thus resulting in efficiency degradation. The NPD is calculated by comparing the phase difference at the second efficiency peak to that at P3 dB. An 8-dB OBO DPA design is used to explore NPD's effect, and the NPD value (45°) is extracted for the CG2H40010F device. The standard NPD profile will look like Figure 2.3a, where the peaking PA turns on at 8 dB OBO. Without the NPD, $\angle I_P - \angle I_C$ will have a constant value ($\Delta\phi_0 = 0$) throughout the input drive. However, when the peaking amplifier turns on, with NPD $\angle I_P - \angle I_C$ will be $\Delta\phi_1 = \Delta\phi_0 + \phi_{NPD}$, and this will gradually decrease with input drive and become $\Delta\phi_0$ at P3 dB. To get an idea of how the solutions will react with the NPD effect, the extracted PD (45°) is added to both the solutions, and drain efficiency (for $\Delta\theta_1 = 105°$) is plotted and shown in Figure 2.3b. It is evident that without the effect of NPD, both solutions can generate identical drain efficiency profiles (Figure 2.2b)

whereas with the presence of NPD solution 2 has improved drain efficiency compared to solution 1.

2.3 Experimental validation of proposed theory

To validate the proposed NPD theory, two PE-DPAs based on solution 1 and solution 2 are individually designed and optimized at 3 GHz in the Advanced Design System. Cree's newly introduced GaN-on-SiC HEMT packaged device, CG2H40010F, is the carrier and peaking amplifier. Based on the load-pull simulation at 3 GHz, R_{Opt} is selected as 30 Ω to achieve maximum efficiency at saturated power. $R_{Load} = 0.5 \cdot R_{Opt} = 15\Omega$ is used for both solutions. The carrier amplifier is biased in class AB (Vgs = -2.9 V), and the peaking amplifier operates in class C (Vgs = -5.3V). Drain voltages for the carrier and peaking amplifiers are 28 V. Both designs are implemented to achieve 8 dB output power backoff (OBO); therefore, $\Delta\theta_1$ is selected 105° from Figure 2.2. The equivalent two port output matching circuits are derived from the OMN's ABCD parameters in table 2.1 for solutions 1 and 2 [1]. Later, lumped components are converted to microstrip line circuits in Rogers 04350B (ε_r = 3.66) substrate material.

The EM simulated results of both solutions are shown in Figures 2.4-2.5. It is evident from the drain efficiency results shown in Figure 2.4a that solution 2 has significantly better efficiency compared to solution 1 in between 8-dB OBO and P3 dB. Both solutions have identical efficiency below OBO and at P3 dB. The effect of NPD becomes apparent once the peaking amplifier turns on. Therefore, the NPD would not have any significant impact before OBO. Similarly, at P3 dB $\angle I_P - \angle I_C$ becomes equal for both with and without NPD cases (Figure 2.3a); as a result, both solutions have identical efficiency. To understand the effect of the NPD more clearly, the load trajectories of peaking PA for both solutions are shown in Figure 2.4b.

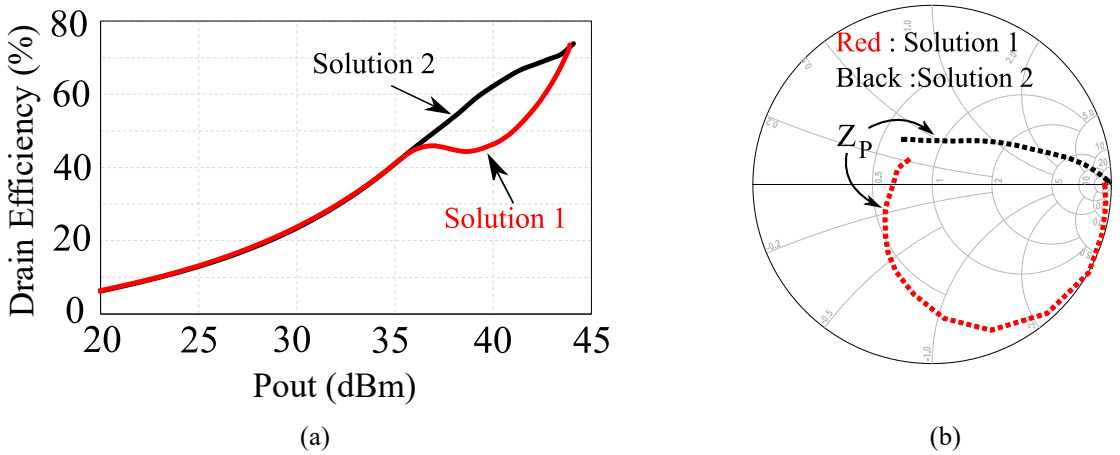


Figure 2.4: (a) EM Simulated Drain Efficiency of Solution 1 and 2. (b) Impedances at the Device's Intrinsic Plane of Peaking PA.

Solution 1 experiences higher capacitive impedance due to the presence of NPD and generates more reactive power, which causes efficiency degradation. Conversely, NPD brings the peaking load trajectory of solution 2 closer to the real axis in the Smith chart, hence generating less reactive power. The simulated gain, power, and $\Delta\theta_1$ for both solutions are shown in Figure 2.5. Both solutions have almost the same gain and output power profile and $\Delta\theta_1$. Therefore, PE-DPA design with solution 2 provides better performance for a given frequency than solution 1.

2.4 Measured Results

Based on the presented NPD theory and simulated performance comparison in section 2.3, solution 2 PE-DPA design is selected for fabrication on Rogers 04350B board material.

The circuit schematic at 3 GHz design frequency is shown in Figure 2.6. At the input side, a hybrid branch line coupler is used to split the signal into two amplifier paths equally. RC stabilization circuit is used to ensure the unconditional stability of the HEMT devices. An offset line is used at the input to adjust the desired

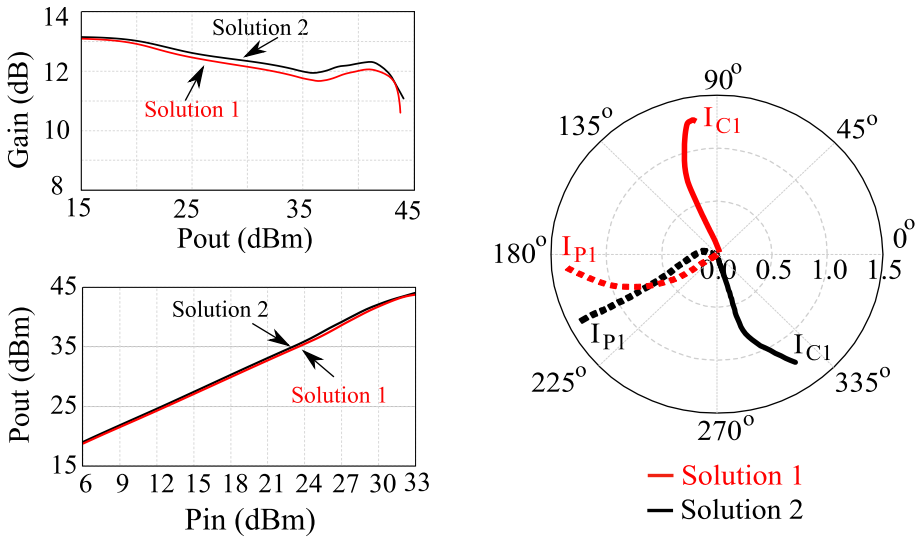
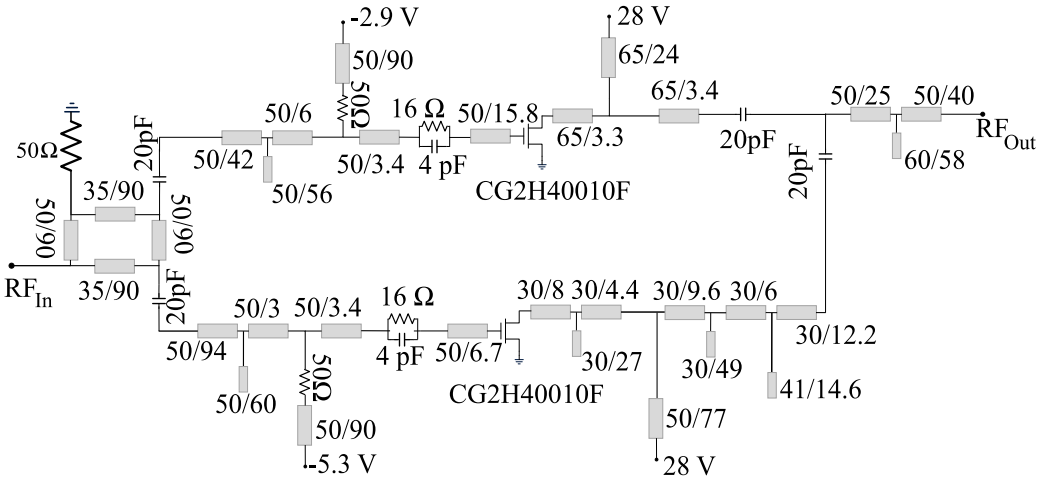


Figure 2.5: Simulated Performance of Solution 1 and 2.

phase between the carrier and peaking amplifier paths. A single L section matching network matches $R_{Load} = 15\Omega$ to 50 Ω. The OMN for carrier and peaking PAs are implemented from the ABCD parameters for solution 2. The fabricated PE-DPA is shown in Figure 2.7.



Transmission lines expressed as: Characteristic impedance/Electrical length in degrees

Figure 2.6: Circuit Schematic of PE-DPA.

The measured results at 3 GHz under continuous wave excitation are plotted in

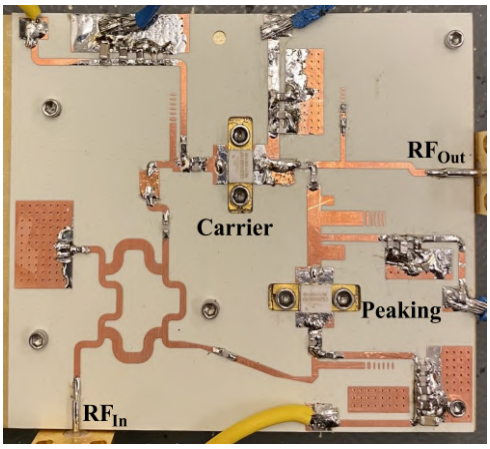


Figure 2.7: Fabricated PE-DPA.

Figure 2.8. The PE-DPA measured results closely follow the simulated results. The measured DPA exhibits 73% and 44% drain efficiency at P3 dB and 8 dB OBO. The output power at P3 dB is 44.3 dBm. The transducer gain is 13 dB and 9.9 dB at low power and P3 dB, respectively.

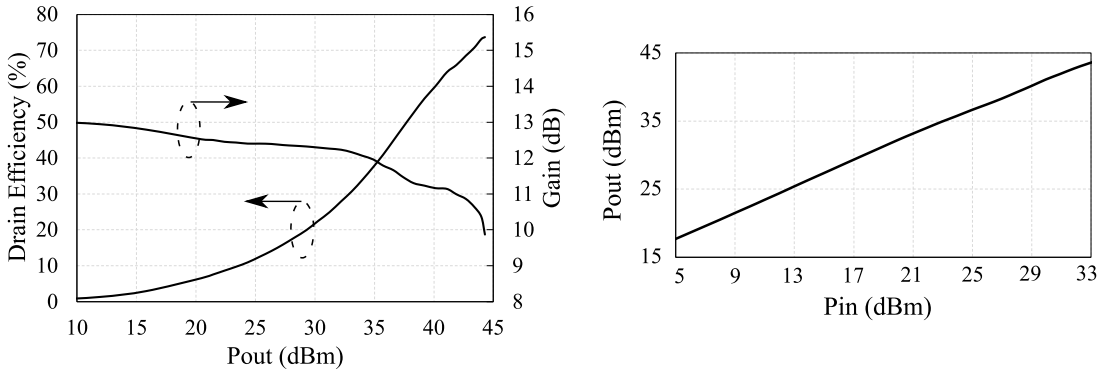


Figure 2.8: Measured Results of PE-DPA.

The designed PE-DPA's performance has been measured across the 2.85 - 3.2 GHz frequency band, and the results are shown in Figure 2.9. The drain efficiency varies 52-73% 38-52% and 35-44% at P3 dB, 6dB OBO and 8 dB OBO respectively. The output power and gain at low power vary between 42.7-44.3 dBm and 9.6-13 dB, respectively.

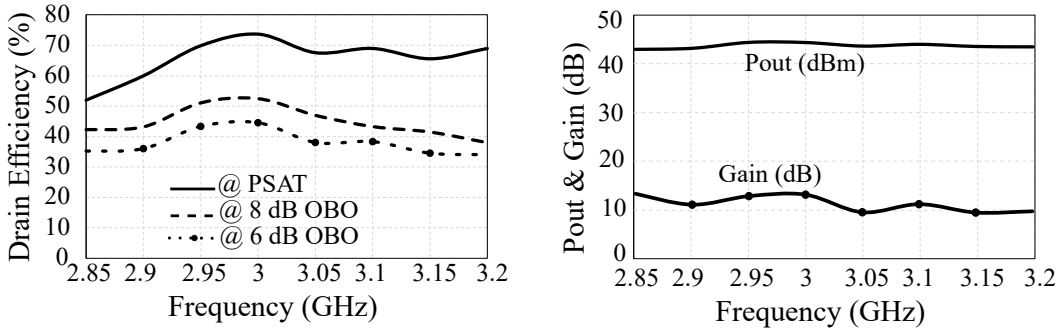


Figure 2.9: Measured DPA Performance Across Frequency.

The measurement with a single carrier 20 MHz LTE signal with peak to average (PAPR) of 7.5 dB is also performed and shown in Figure 2.10. A generalized memory polynomial-based digital pre-distortion (DPD) is used to linearize the PE-DPA, and the power spectral density (PSD) after DPD correction is shown in Figure 2.10. At 3 GHz, the PE-DPA achieves 37% drain efficiency and 11.9 dB gain at 34.6 dBm average power.

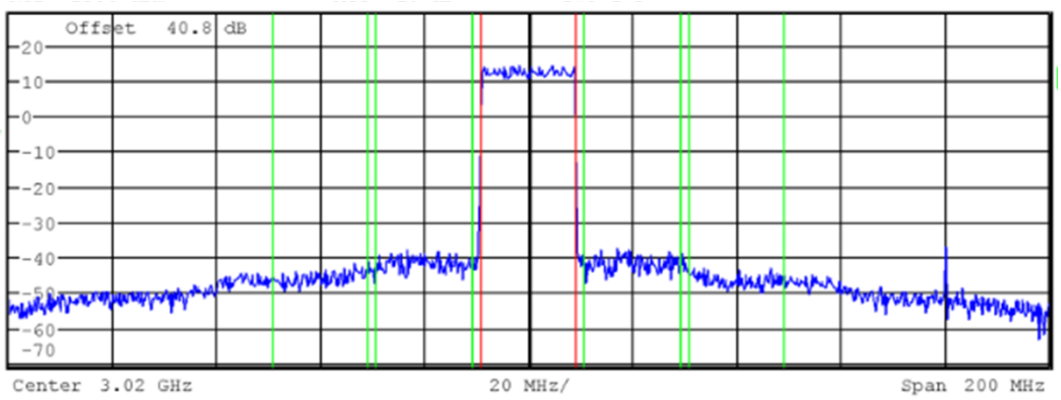


Figure 2.10: PSD of the DPA with 20 MHz LTE Signal.

2.5 Summary

This work presents the effect of NPD on PE-DPA's output network selection. It compares the performance of two possible output networks and selects the one

with superior performance for hardware implementation. Table 2.2 summarizes the performance of the designed PE-DPA and compares it with other state-of-the-art architectures. The implemented PE-DPA shows competitive performance compared to prior DPAs.

Table 2.2

Performance Summary

Ref.	Freq. (GHz)	OBO (dB)	Pout (dBm)	Gain (dB)	DE,SAT (%)	DE,BO (%)
[23]	2.1-2.3	9	42-43	>9	63-72	40-55
[25]*	3.3-3.6	8	43.6-45	>9	67-73	46-54
[26]	3.3-3.4	6	44-44.5	6-7	70.7-73.2	39-42.4
[27]	3.5	9	42.5	12	70	55.1
[28]	3.3-3.8	6	42.6	12	56-64	42-51
This work	2.85-3.2	8	42.7-44.3	9.6-13	52-73	35-45

* : Simulated result

Chapter 3

3.3-3.6 GHZ PHASE EXPLOITED DOHERTY POWER AMPLIFIER WITH PARALLEL LOAD COMBINING NETWORK

3.1 Introduction

Doherty PAs are preferred for handling high PAPR signals but suffer from narrow bandwidth. An interesting technique is presented in [23] to extend the DPA output power back to more than 6 dB. The authors reported results for 8-dB OBO with high efficiency at saturation and backoff. But their results hold for a narrow frequency band (200 MHz, center at 2.2 GHz). The main bandwidth limiting factor of the DPA is the impedance inversion network (IIN). The simplest solution to overcome this limitation is to use a parallel combining technique. The parallel combining technique reduces the impedance transformation ratio (ITR) of the IIN [25], [32], [33]. This work analyses the limitation of [23] with respect to frequency and proposes a parallel load-combining network to overcome the frequency limitations while maintaining high OBO. A detailed mathematical investigation is presented, and a simulation model is developed using GaN Cree bare die models. The PEDPA with parallel combiner is designed for 8-dB OBO and a bandwidth of 300 MHz from 3.3-3.6 GHz.

3.2 Analysis of PE-DPA and bandwidth extension

3.2.1 Analysis of PE-DPA with respect to frequency

Figure 3.1 shows the conceptual diagram of PE-DPA (explained in detail in Chapter 2), where the ideal current sources replace the carrier and peaking amplifiers. At saturation, it intentionally mismatches the phase ($\Delta\theta_1 = \theta_{C1} - \theta_{P1}$) of the carrier

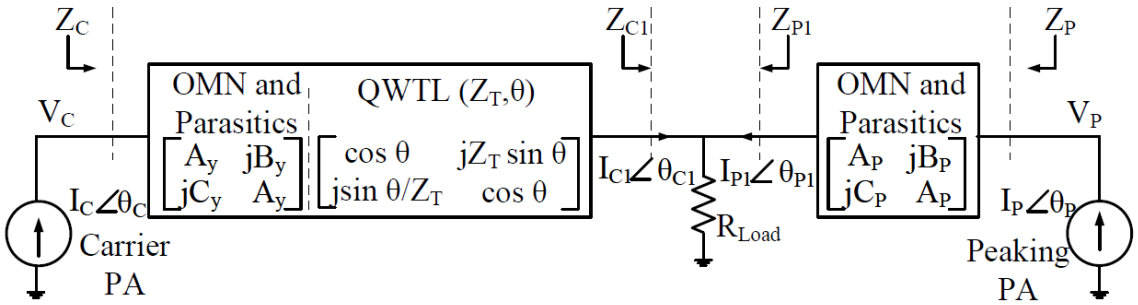


Figure 3.1: Conceptual Diagram of PE-DPA.

and peaking amplifier keeping their magnitude ($|I_{C1}| = |I_{P1}|$) the same at combining node of the DPA.

Since the major frequency limitation in a DPA comes from the quarter wave transmission line (QWTL), this work separately analyses its effect while calculating the carrier output network transmission matrix. The modified representation of the carrier ABCD matrix will be:

$$\begin{bmatrix} A_C & jB_C \\ jC_C & D_C \end{bmatrix} = \begin{bmatrix} A_y & jB_y \\ jC_y & D_y \end{bmatrix} \cdot \begin{bmatrix} \cos\theta & jZ_T \sin\theta \\ j\sin\theta/Z_T & \cos\theta \end{bmatrix} \tag{3.1}$$

In equation 3.1, the first part accounts for the parasitics and OMN, and the second part is for QWTL. A_C, B_C, C_C, D_C and peaking amplifier network parameters (A_P, B_P, C_P, D_P) will be same as reported in [23]. From the equation 3.1, A_y, B_y, C_y, D_y can be expressed in terms of A_C, B_C, C_C, D_C , θ and Z_T .

$$A_y = A_C \cos\theta + \frac{B_C}{Z_T} \sin\theta \tag{3.2}$$

$$B_y = B_C \cos\theta - Z_T A_C \sin\theta \tag{3.3}$$

$$C_y = C_C \cos\theta - \frac{D_C}{Z_T} \sin\theta \tag{3.4}$$

$$D_y = Z_T C_C \sin\theta + D_C \cos\theta \tag{3.5}$$

$Z_T = R_{Opt}$ and θ are the characteristics impedance and phase delay of the QWTL. At normalized frequency, f, $\theta = (\pi/2) \cdot f$. Impedances at the intrinsic plane (Z_C and Z_P) are calculated using equations 3.6 - 3.10, and the ABCD network parameters of the carrier and peaking network parameters.

$$Z_x = \frac{Z_{x1} A_x + B_x}{Z_{x1} C_x + D_x} \tag{3.6}$$

$$Z_{C,BO} = VSWR \cdot R_{Opt} \tag{3.7}$$

$$Z_{P1,BO} = \infty \tag{3.8}$$

$$Z_{C1,SAT} = R_{Load} \cdot (1 + \cos\theta_1 + j \sin\theta_1) \tag{3.9}$$

$$Z_{P1,SAT} = R_{Load} \cdot (1 + \cos\theta_1 - j \sin\theta_1) \tag{3.10}$$

In the above equations, x is C or P for the carrier and peaking amplifier. Using the equation 3.6, the voltage at the intrinsic plane of the amplifiers can be easily calculated ($V_x = I_x \cdot Z_x$). Output power and efficiency are estimated from the knowledge of V_x and I_x.

The theoretical simulated efficiency over normalized frequency at saturated power and various OBO levels is plotted in Figure 3.2. In the PE-DPA, extended backoff is achieved by varying $\Delta\theta_1$. $\Delta\theta_1 = 0°, 86°, 105°, 124°$ represents OBO of 6dB, 7dB, 8dB, and 9dB, respectively. At $f = 1$, efficiency is maximum for both backoff and saturated power levels. For $\Delta\theta_1 = 0$, the efficiency at saturation remains maximum across the

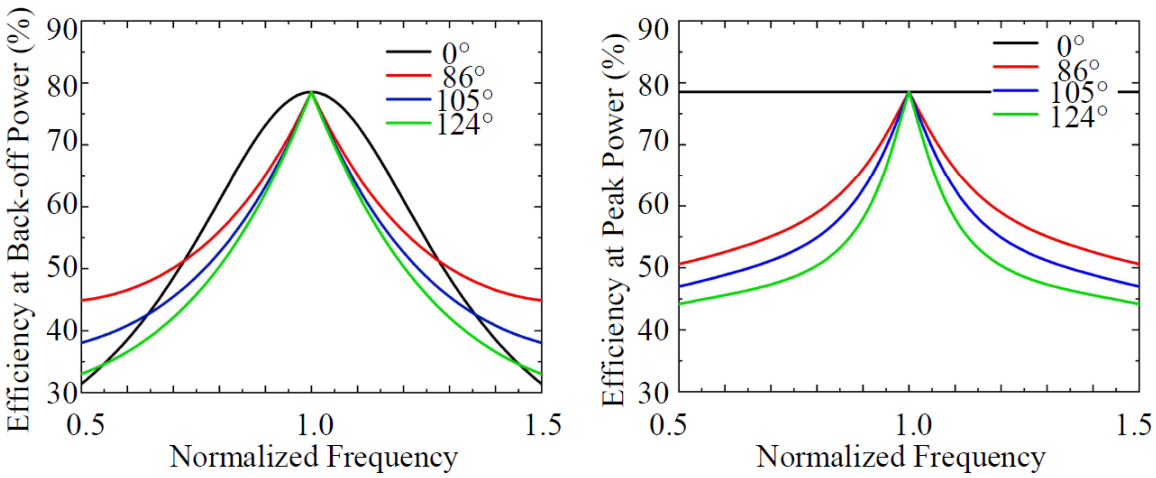


Figure 3.2: Efficiency Variation of PE-DPA with Respect to the Normalized Frequency at Saturation (Right) and Backoff (Left) Power, for Various OBO Levels.

whole frequency range, and the OBO efficiency drops by 9.5% when the frequency varies by +/-12% (f = 0.88, 1.12). At $\Delta\theta_1$ = 105°, the efficiency at OBO and saturation drops by 20% from maximum when f = 0.88, 1.12. Therefore, as the $\Delta\theta_1$ increases to achieve more OBO, efficiency rapidly drops, thus narrowing the efficiency bandwidth. This work presents a PE-DPA that employs a parallel load-combining network to mitigate the reduction in efficiency over frequency.

3.2.2 Concept of Parallel Combining

To overcome the frequency limitation of QWTLs, parallel combining can be employed in a DPA [25], [32] and [33], with its concept illustrated by the simple diagram of Figure 3.3. In this case, R_{Load} is the same as R_{Opt}. At saturation, the impedance seen by both amplifiers is R_{Opt}. At power backoff, when the peaking PA is switched off, the DPA combining node impedance (R_{Opt}) is converted to $2 \cdot R_{Opt}$. Therefore, for a parallel combining DPA at backoff, the ITR has reduced to 2:1 from 4:1 in the case of a conventional DPA. Two $\lambda/4$ transmission lines are used in the peaking branch

to provide correct impedance terminations at both peak and saturated power levels.

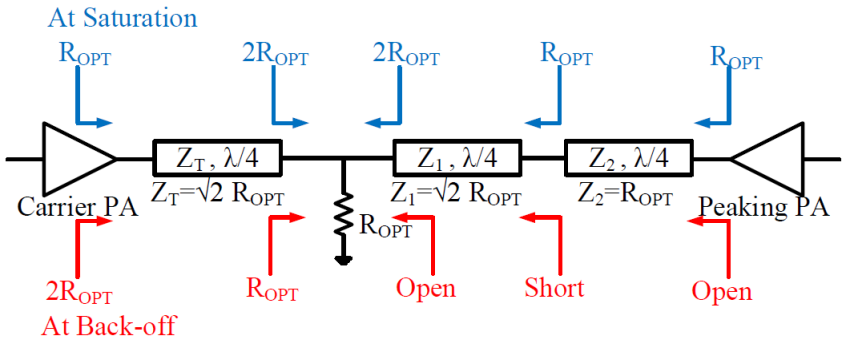


Figure 3.3: Conceptual Diagram of a DPA with Parallel Combining.

3.2.3 PE-DPA with Parallel Load Combining (PE-PDPA)

The efficiency of a PE-DPA reduces as the frequency drifts away from the center frequency. Moreover, it degrades more quickly as $\Delta\theta_1$ increases to achieve more OBO range. To overcome the narrowband limitation of the PE-DPA caused mainly by the QWTL, a parallel combining PE-DPA is presented (PE-PDPA).

The basic architecture of the PE-PDPA is shown in Figure 3.4. The transmission matrix for the carrier PA is the same as the equation 3.1, with a modification in $Z_T(=\sqrt{2}\cdot R_{Opt})$, and R_{Load}=R_{Opt}.

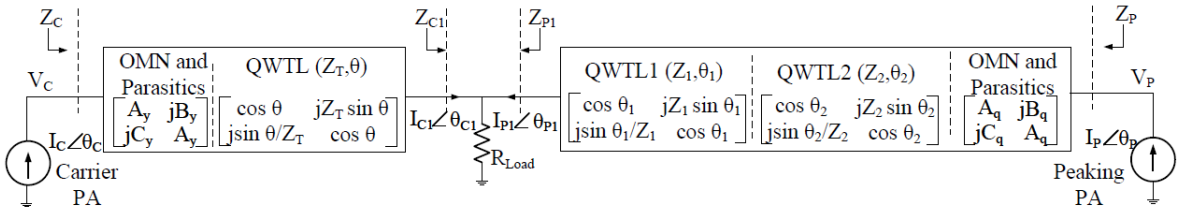


Figure 3.4: Proposed PE-PDPA Configuration for Bandwidth Extension.

The transmission matrix for the peaking PA is defined as:

$$\begin{bmatrix} A_P & jB_P \\ jC_P & jD_P \end{bmatrix} = \begin{bmatrix} \cos\theta_1 & jZ_1\sin\theta_1 \\ (j\sin\theta)/Z_1 & \cos\theta_1 \end{bmatrix} \cdot \begin{bmatrix} \cos\theta_2 & jZ_2\sin\theta_2 \\ (j\sin\theta)/Z_2 & \cos\theta_2 \end{bmatrix} \cdot \begin{bmatrix} A_q & jB_q \\ jC_q & jD_q \end{bmatrix} \tag{3.11}$$

Where $Z_1(=\sqrt{2}\cdot R_{Opt})$ and $Z_2 = R_{OPT}$ are the characteristics impedances of QWTL1 and QWTL2. θ_1 and θ_2 are the phase delays of QWTL1 and 2, and they would be $\pi/2$ at $f = 1$. The values of A_q, B_q, C_q, and D_q can be calculated using a similar procedure as the carrier PA's ABCD parameters in section 3.2.1. The overall ABCD matrices of the carrier and peaking PAs would be the same as [23], as the load modulation (at OBO, R_{Load} to $VSWR\cdot R_{OPT}$, and at saturation $Z_{C1,SAT}$ to R_{OPT}) remains the same as the PE-DPA.

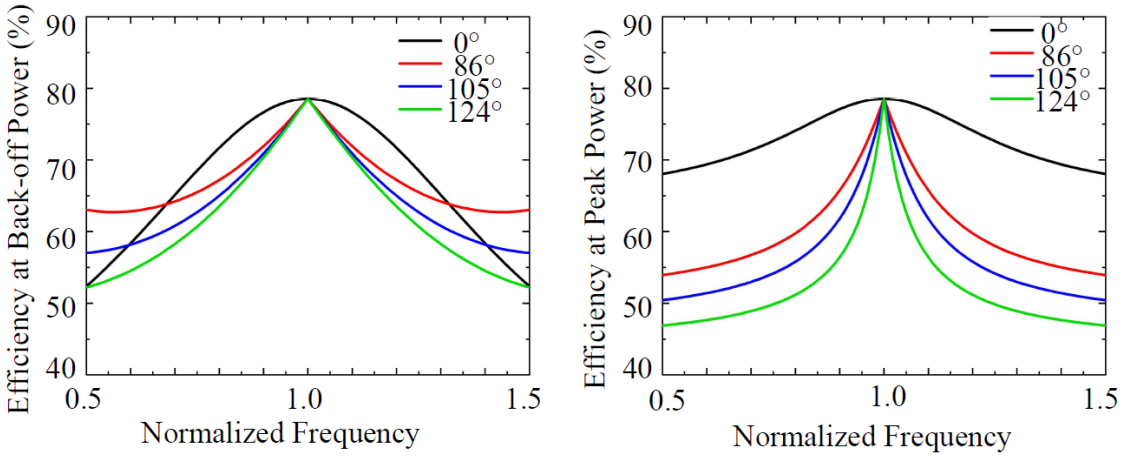


Figure 3.5: Efficiency Versus Normalized Frequency for the PE-PDPA at Saturation (Right) and Backoff (Left) for Various OBO Levels.

The resulting efficiency for the PE-PDPA at OBO and saturated power is shown in Figure 3.5. At $\Delta\theta_1 = 105°$, the efficiency at backoff remains within 20% from the maximum for +/-30% variation in frequency ($f = 0.7$, 1.3). It is clear from the result

that efficiency at OBO across the frequency band improves in the PE-PDPA. However, at saturated power for $\Delta\theta_1 = 0°$, efficiency rolls off more quickly in the PE-PDPA. At saturated power, the ITR becomes 2:1 for a parallel combining DPA, whereas the ITR is 1:1 in a conventional DPA. Therefore, bandwidth is expected to be smaller in a PE-PDPA at saturated power with $\Delta\theta_1 = 0°$. But, for $\Delta\theta_1 > 0°$ in a PE-PDPA, the efficiency across the frequency band at saturation remains almost the same as the PE-DPA. When $\Delta\theta_1 > 0°$, impedances at the combining plane are complex, as described in the equations 3.9 and 3.10. The absolute values of $Z_{C1,SAT}$ and $Z_{P1,SAT}$ are more than R_{Load}, which reduces the ITR at saturated power compared to the $\Delta\theta_1 = 0°$ case. Therefore, the PE-PDPA improves efficiency bandwidth at OBO while maintaining almost the same efficiency at saturated power across the frequency band compared to the PE-DPA architecture.

3.3 Implementation and Simulation Results

To verify the proposed concept, a symmetric PE-PDPA is designed from 3.3-3.6 GHz using Cree's CGH60015D bare die HEMT model and Rogers 04350B ($\varepsilon_r = 3.66$) substrate material. The schematic of the designed PA is shown in Figure 3.6. The DPA is designed for 8 dB OBO by selecting $\Delta\theta1 = 105°$. The carrier amplifier is biased in class AB (V_{GS} = -3 V, I_{DQ} = 29 mA) with 28 V drain voltage. The peaking amplifier is biased in class C (V_{GS} = -4.8 V) with the same 28 V drain voltage. Based on load-pull simulation data, R_{OPT} is chosen as 20Ω to achieve maximum efficiency at saturated power. The carrier and peaking PAs output networks are designed based on their ABCD parameters (derived in section 3.2.3 and later realized as transmission line circuits. A Gysel power combiner [35] is used at the input to split the RF signal equally, and a parallel RC network is used to stabilize both the carrier and peaking PAs. Two offset lines are used (marked red in the schematic of Figure 3.6) to achieve

phase adjustment for 8 dB OBO.

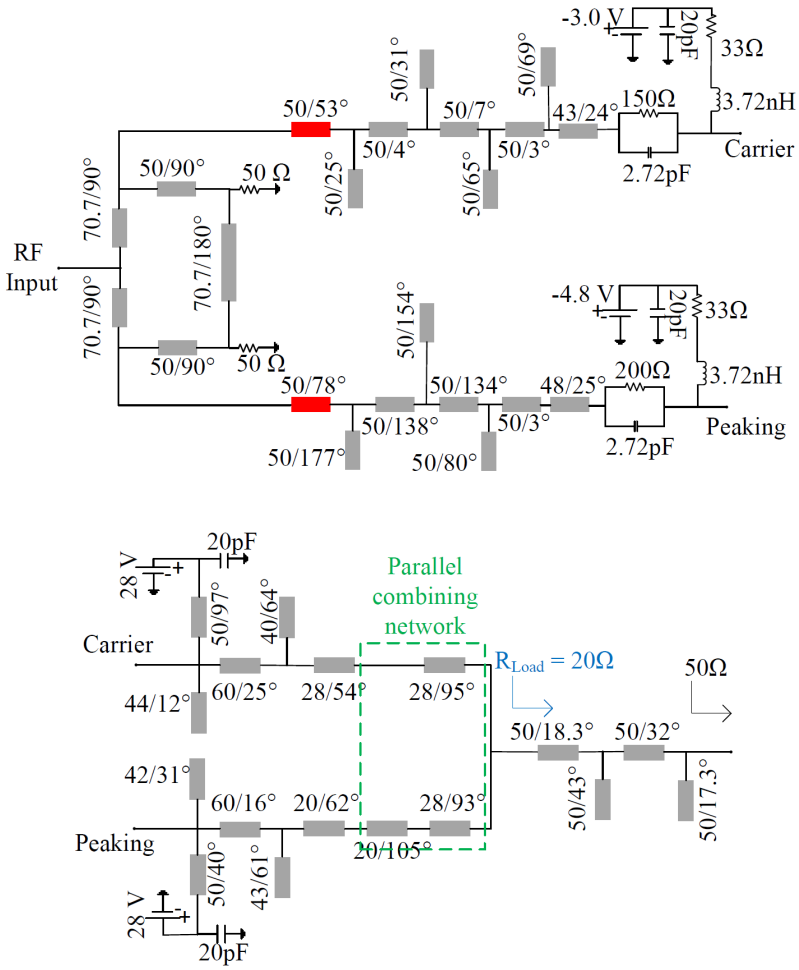


Figure 3.6: Circuit Schematic of PE-PDPA. Top: Input Matching, Bottom: Output Matching Networks.

Figure 3.7 shows the simulated results for the designed PE-PDPA. At saturated power, drain efficiency (DE) is 60-77% across the frequency band. The PA exhibits 43-54% DE for 8 dB OBO over the 3.3-3.6 GHz frequency band. As explained in section 3.2.3, parallel combining is beneficial only at power backoff; therefore, DE variation is higher (22%) at saturation compared to OBO (20%). The peak output power is above 42 dBm, and the transducer gain is above 10 dB in the band of operation. The PA's AM-AM and AM-PM follow similar trends to a conventional DPA, therefore the

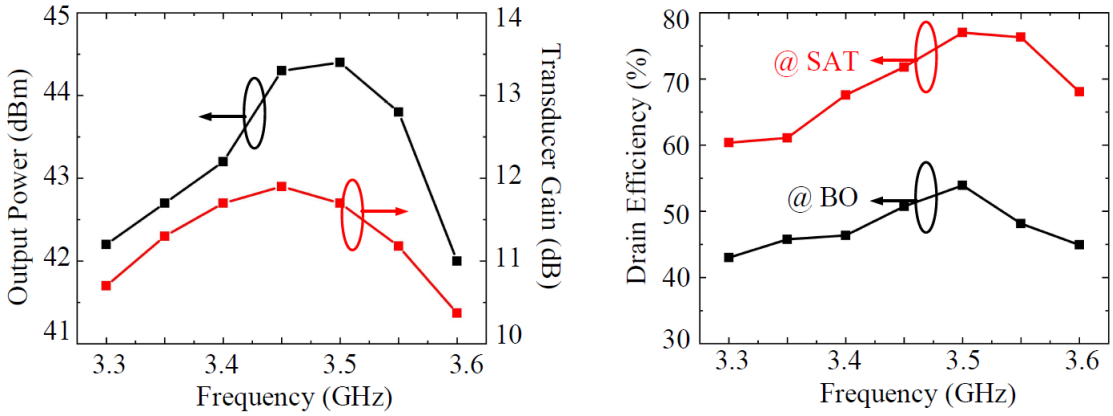


Figure 3.7: Output Power, Transducer Gain, and Drain Efficiency Versus Frequency.

Table 3.1

Performance Summary

Ref.	Freq. (GHz)	OBO (dB)	Pout (dBm)	Gain (dB)	DE,SAT (%)	DE,BO (%)
[23]**	2.1-2.3	9	42-43	>9	63-72	40-55
[25]*	3.3-3.6	8	43.6-45	>9	67-73	46-54
[34]**	3.4-3.6	6	40	>14.9	60-60.8	38
[28]**+	3.3-3.8	6	42.6	12	56-64	42-51
This work*	3.3-3.6	8	42-44.4	>10	60-77	43-54

* : Simulated result, **: Measured result, +:Different GaN device used

presented PE-PDPA is amenable to digital pre-distortion techniques.

3.4 Summary

This work presents a wideband extended efficiency range symmetric Doherty power amplifier (DPA) operating from 3.3 to 3.6 GHz. The presented DPA uses parallel combining to increase the bandwidth over a conventional DPA and phase

exploitation to extend the high-efficiency backoff point beyond 6dB. Detailed performance analysis with respect to frequency is presented for the phase exploited symmetric DPA with parallel load combining (PE-PDPA). To validate the presented technique, a prototype is designed using GaN HEMT devices, and simulation results demonstrate that the PE-PDPA achieves 60% - 77% efficiency at saturation and 43% - 54% efficiency at 8 dB backoff over the 3.3-3.6GHz operating band. The PA maintains a 10 dB gain and an average of 43 dBm saturated power over the entire frequency range. Table 3.1 summarizes the performance of the designed PA and compares it with other state-of-the-art PAs.

Chapter 4

ASYMMETRICAL CONTINUOUS MODE DOHERTY POWER AMPLIFIER USING COMPLEX COMBINING LOAD IMPEDANCE

4.1 Introduction

This work presents an asymmetrical DPA, with the DPA operating as a continuous mode class J at power backoff. Continuous mode (CM) PAs, including class J and class F PAs, have been successfully applied to DPAs and showed promising results for extending bandwidth when the DPA is operating at output power backoff (OBO) [31], [36]-[38]. However, most of the cases reported in [31], [36]-[40]are limited to 6 dB OBO. The OBO must be higher than 6 dB to support a high PAPR signal of 9 dB or more. The work in [41] reports an asymmetrical DPA with continuous class F carrier amplifier at backoff and achieves 9 dB OBO. Still, the class F amplifier typically has limited linearity and must have both 2nd and 3rd harmonics matched.

This continuous mode class J asymmetrical DPA topology is achieved by designing a post-matching output network (PMN) that transforms the complex load impedance to an optimum trajectory for a class J amplifier at OBO, thus resulting in a wider bandwidth asymmetrical DPA at backed-off powers. This work includes a detailed theoretical derivation and prototype design to demonstrate the effectiveness of the presented DPA. The presented asymmetrical continuous mode DPA (CM DPA) using complex load is designed for 9 dB OBO over a frequency range from 1.8 GHz to 2.6 GHz, thus demonstrating 36% fractional bandwidth.

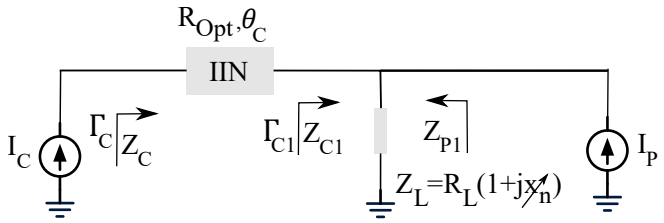


Figure 4.1: Proposed CM DPA Using Complex Combining Load.

4.2 Proposed Asymmetrical CM DPA Architecture

4.2.1 Proposed Architecture Description

Figure 4.1 shows the proposed asymmetrical CM DPA architecture. The current ratio $(I_P/I_C) = \alpha$, and $\alpha = 10^{((\delta/20)-1)}$, where δ is the targeted OBO in dB. The complex combining impedance is defined as $Z_L = R_L \cdot (1 + x_n)$, where the reactive component x_n is variable and can change with operating frequency. The impedance relationships for both the carrier and peaking amplifiers of the proposed CM DPA at the output combining node are described in equations 4.1 - 4.5.

$$R_L = \frac{R_{\text{Opt}}}{1+\alpha} \tag{4.1}$$

$$Z_{\text{C1-SAT}} = (1+\alpha) \cdot Z_L \tag{4.2}$$

$$Z_{\text{C1-BO}} = Z_L \tag{4.3}$$

$$Z_{\text{P1-SAT}} = \left(1 + \frac{1}{\alpha}\right) \cdot Z_L \tag{4.4}$$

$$Z_{\text{P1-BO}} = \infty \tag{4.5}$$

R_{Opt} is the optimum impedance for a class B carrier amplifier. Z_{C1-SAT} and Z_{C1-BO} are the impedances at saturated and backoff powers, respectively, looking into the combining node from the carrier PA. Similarly, Z_{P1-SAT} and Z_{P1-BO} are the impedance at saturated and backoff powers, respectively, looking into the combining node from the class C peaking amplifier. For a standard asymmetric DPA, equations

4.1 through 4.5 apply with $Z_L = R_L$. Γ_{C1} and Γ_C are the reflection coefficients at the combining node and intrinsic node, respectively.

To account for the dependency of the DPA's reflection coefficients over frequency (phase), this work analyzes the IIN as a lossless QWTL, with the generalized s-parameters for this QWTL expressed in equation 4.6.

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0 & e^{j\theta_C} \\ e^{j\theta_C} & 0 \end{bmatrix} \tag{4.6}$$

θ_C is the phase of the QWTL that changes with frequency. $\theta_C = \frac{\pi}{2} \cdot \frac{f}{f_0}$, where f_0 is the center frequency of operation. The reflection coefficients Γ_{C1} and Γ_C are presented in equations 4.7-4.8.

$$\Gamma_{C1-k} = \frac{Z_{C1-k} - Z_{C1-SAT}}{Z_{C1-k} + Z^*_{C1-SAT}}, \quad k = \text{BO or SAT} \tag{4.7}$$

$$\Gamma_{C_k} = \Gamma_{C1-k} \cdot e^{2j\theta_C} \tag{4.8}$$

The asymmetric DPAs reflection coefficient at OBO expressed in equation 4.8, is plotted in Figure 4.2 for varying θ_C at $\delta = 9$dB, with $x_n = 0$ ($Z_L = R_L$). The target of this work is to modify this backoff impedance trajectory of the asymmetrical DPA (blue) to the continuous mode class J amplifier trajectory (red), as shown in Figure 4.2, to extend the overall DPA bandwidth at OBO. The continuous mode class J impedance Z_J (at fundamental frequency f_0) and Z_{2J} (at $2f_0$) can be expressed by equations 4.9-4.10.

$$Z_J = (1+\alpha)(1+j\gamma)R_{\text{Opt}}, \quad -1 \leq \gamma \leq 1 \tag{4.9}$$

$$Z_{2J} = -j\frac{3\pi\gamma}{8}(1+\alpha)R_{\text{Opt}} \tag{4.10}$$

where γ is an empirical parameter with range: $-1 \leq \gamma \leq 1$. These Z_J and Z_{2J} impedances are also plotted in Figure 4.2 for varying γ. The class J amplifier's

reflection coefficient is shown in equation 4.11.

$$\Gamma_J = \frac{Z_J - R_{\text{Opt}}}{Z_J + R_{\text{Opt}}} \tag{4.11}$$

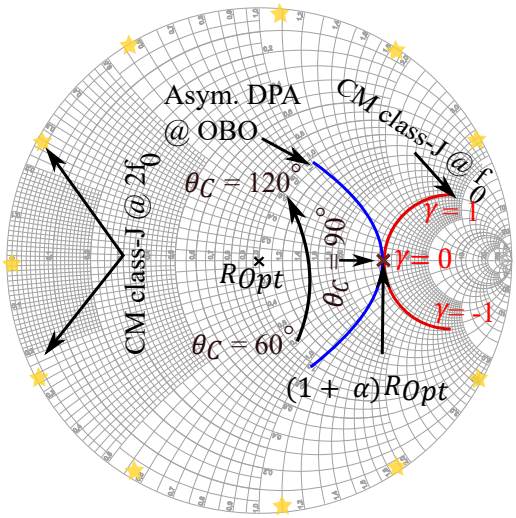


Figure 4.2: Impedance Trajectories for an Asymmetrical DPA at OBO Plotted from $\theta_C = 60°$ to $120°$ (Blue), and for a Continuous Mode Class J (Red).

4.2.2 Procedure for Transforming the Trajectory

To achieve the continuous mode class J characteristics at backoff, the reflection coefficient at the carrier PA's node at backoff should match with the class J reflection coefficient, Γ_J shown in equation 4.12.

$$\Gamma_{C-BO} = \Gamma_J \tag{4.12}$$

The carrier PA's impedance at the power backoff region can be easily altered using x_n. Choosing different x_n values at different frequencies is possible by correctly designing the PMN. For example, when $f = f_0$:

$$\theta_C = 90°, \quad x_n = 0, \quad Z_{C1-BO} = R_L$$

However, at $f \neq f_0$, x_n will be varied to another value to map the impedance trajectory to class J, and:

$$\theta_C \neq 90°, \quad x_n \neq 0, \quad Z_{C1-BO} = R_L(1 + jx_n)$$

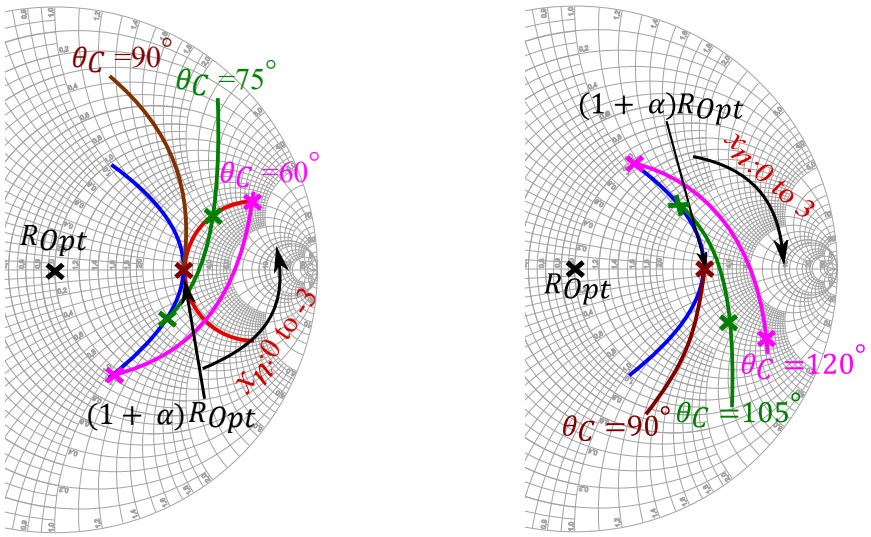


Figure 4.3: Impedance Trajectories for Left: $\theta_C = 90°, 75°, 60°$, x_n = -3 to 0, and for Right: $\theta_C = 90°, 105°, 120°$, $x_n = 0$ to 3.

Trajectory Change

The blue circle in Figure 4.2 shows the asymmetrical DPA's impedance trajectory at backoff power level for varying θ_C ($x_n = 0$), where θ_C is a function of frequency. At $f = f_0$, $\theta_C = 90°$ and the DPA and class J impedance trajectories intersect. Figure 4.3a depicts 3 different impedance trajectories when $\theta_C = 90°, 75°, 60°$, and x_n is varied from -3 to 0. Each of these curves intersects reactive points with the original asymmetrical DPA at OBO and continuous class J. For example, at $\theta_C = 75°$, x_n is varied from -3 to 0 and intersects the asymmetrical DPA curve (shown in blue) when $x_n = 0$ and the continuous class J curve (shown in red) at x_n = -1.05. This shows

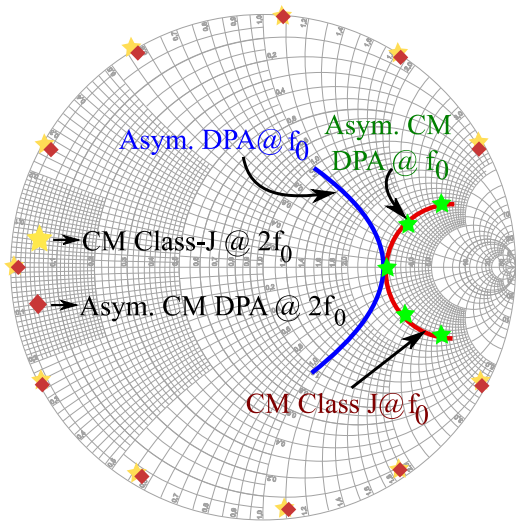


Figure 4.4: Impedance Trajectory after Transformation.

that if x_n is added to the asymmetrical DPA's backoff impedance, the impedance trajectory could be changed to continuous class J. Similarly, in Figure 4.3b, when $\theta_C = 90°, 105°, 120°$, and x_n is varied from 0 to 3, the impedance trajectories for varying reactance intersect both the asymmetric DPA and continuous class J. This work theoretically proves that the asymmetrical DPA impedance at OBO can be transformed to an impedance for continuous class J operation by varying the reactance (x_n) with θ_C. This transformation is realized through the design of a post-matching network (PMN) described in Section 4.3.

Modified Trajectory Calculation

The reactance, x_n, is found using the intersection points of Figure 4.3. These x_n values are listed in table 4.1 for various θ_C. The modified impedance trajectory (green star symbols for f_0 and red diamond symbols for $2f_0$) for the asymmetrical CM DPA after the transformation is given in Figure 4.4. It is evident from the results that by varying the reactive part of the impedance (x_n), it is possible to achieve continuous class J characteristics at backoff power levels. Figure 4.4 also shows the 2nd harmonic of the

Table 4.1

Calculated x_n for Various θ_C

θ_C	x_n	Modified impedance at BO
60°	-2.21	$R_L(1+j(-2.21))$
75°	-1.05	$R_L(1+j(-1.05))$
90°	0	$R_L(1+j(0))$
105°	1.05	$R_L(1+j(1.05))$
120°	2.21	$R_L(1+j(2.21))$

CM DPA, which accurately follows the continuous mode class J 2nd harmonic. At the saturated power level, the carrier amplifier in this topology theoretically operates as a class B amplifier.

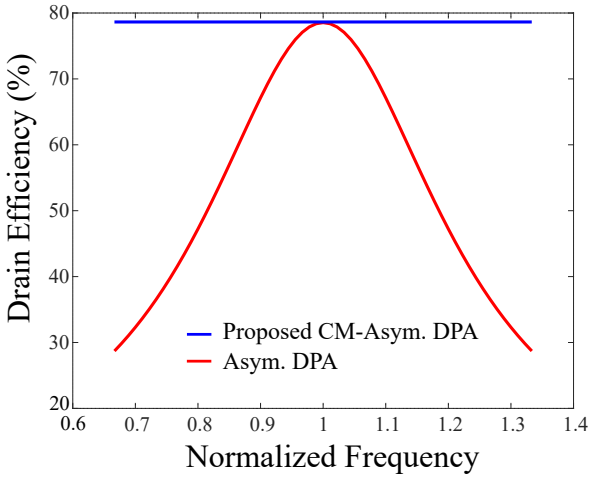


Figure 4.5: Theoretical Ideal Drain Efficiency Versus Normalized Frequency at OBO for the Asymmetrical DPA and the Proposed Asymmetrical CM DPA.

Figure 4.5 plots the theoretical (ideal) drain efficiency (DE) over the normalized frequency of the standard asymmetrical DPA architecture and the presented asymmetrical CM DPA at the backoff power level. The proposed technique theoretically

maintains 78.5% drain efficiency over the entire frequency range, whereas the standard asymmetrical DPA efficiency drops rapidly as it moves away from the center frequency.

4.3 CM DPA Design and Simulation Results

A prototype has been designed to verify the proposed concept using CREE's GaN HEMT bare die models. CGH6008D and CGH60015D are used as the carrier and peaking amplifier, respectively. The schematic is shown in Figure 4.6. The carrier amplifier is biased in class AB (V_{GS} = -3.1 V), and the peaking amplifier operates in class C (V_{GS} = -7 V). Drain voltages for the carrier and peaking amplifiers are 26 V and 30 V, respectively. To achieve 9dB OBO, α is selected as 2.8. R_{Opt} is chosen as 28Ω for the carrier and peaking amplifiers. R_L is selected as 17.5 Ω and x_n is varying with frequency, as given in table 4.1. The variable x_n is achieved through the PMN design, shown in Figure 4.6.

A double-section Wilkinson power splitter evenly splits the input signal between the two branches. To stabilize both amplifiers, a series RC network is used at the gate.

To compare between a standard asymmetrical DPA and the presented asymmetrical CM DPA, both architectures are designed for a frequency band from 1.8 GHz to 2.6 GHz. To fairly compare the DPAs, identical IMN and OMN are used. The only difference between the PAs is the PMN design. For the standard asymmetrical DPA, 17Ω is converted to 50Ω using PMN-1 (shown in Figure 4.6). The PMN is realized with PMN -2 of Figure 4.6 for the proposed CM DPA. Figure 4.7 shows the simulated results for the designed DPAs. At saturated power, drain efficiency for the CM DPA is 61-76% and for the standard asymmetrical DPA is 64-77% across the frequency band. The CM DPA exhibits 43-60% DE at 9 dB OBO over the entire frequency

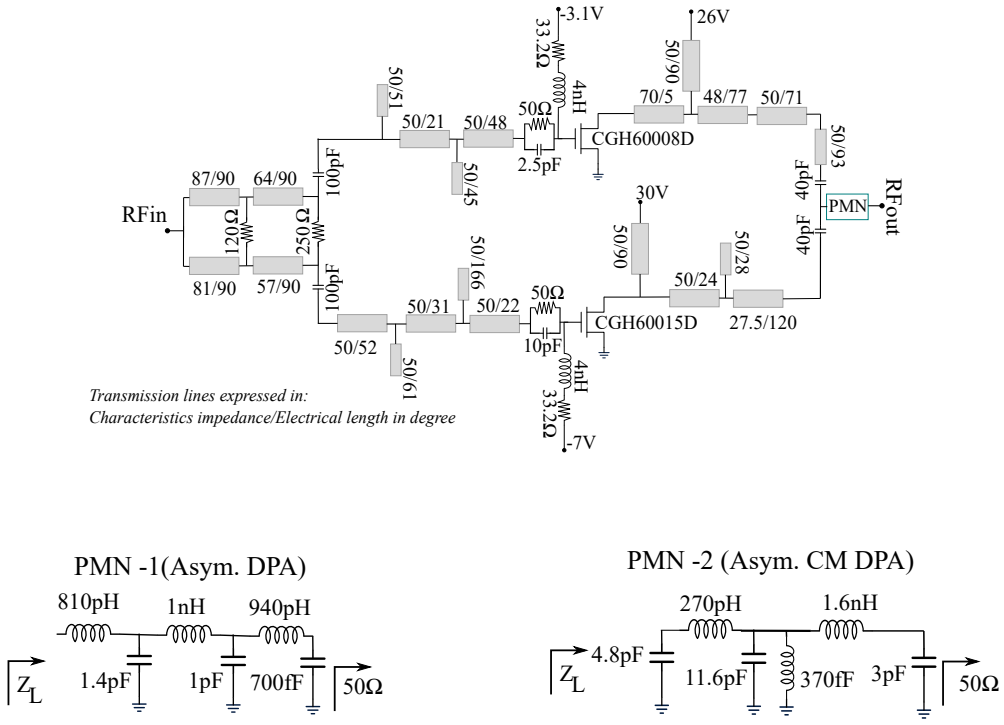


Figure 4.6: Circuit Schematic of the Presented Asymmetrical CM DPA (Top) and PMN Networks (Bottom).

band, whereas the standard asymmetrical DPA's efficiency varies from 36-64% at 9 dB OBO. Although the plots do not follow the exact theoretical trend described in Figure 4.5 due to numerous circuit nonidealities, it is evident from the results that the asymmetrical CM DPA has improved DE over frequency at 9 dB OBO compared to the standard asymmetrical DPA. The average peak output power and transducer gain for both DPAs are 43 dBm and 10 dB, respectively.

4.4 Summary

This work presents a detailed theoretical analysis of an asymmetrical continuous mode DPA. To demonstrate the effectiveness of the proposed architecture, two asymmetrical DPAs (one standard asymmetrical DPA and one asymmetrical CM DPA) were designed using GaN HEMT devices and compared to one another. Table 4.2

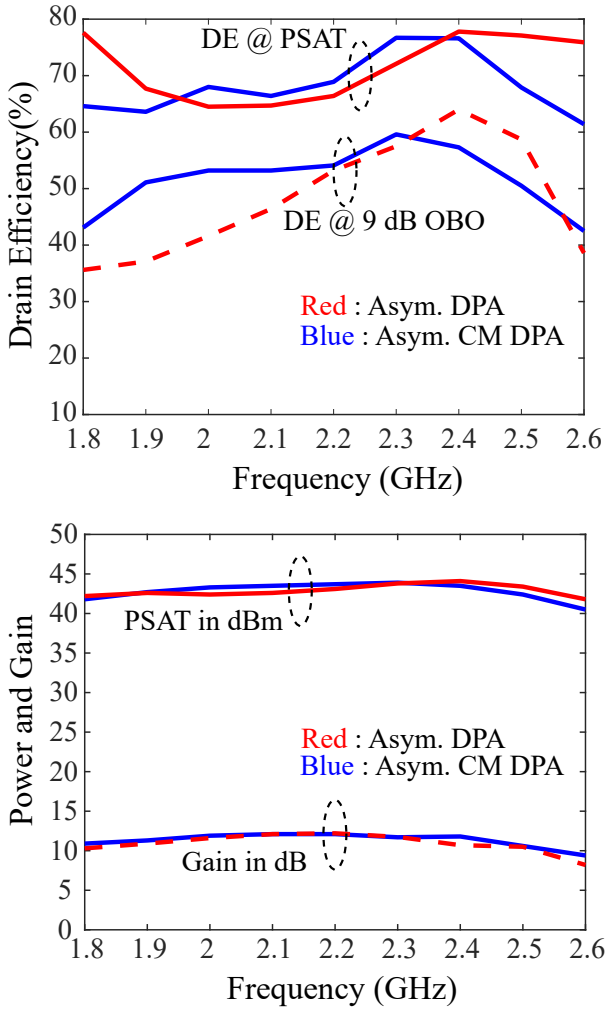


Figure 4.7: Simulation Results of the CM Asymmetrical DPA.

summarizes the performance of the designed asymmetrical CM DPA and compares it with other state-of-the-art architectures. Although only verified in simulation, the presented asymmetrical CM DPA promises broader bandwidth and higher efficiency across the band than other implemented DPAs.

Table 4.2

Performance Summary

Ref.	Freq. (GHz)	OBO (dB)	Pout (dBm)	DE,SAT (%)	DE,BO (%)	Device used
[36]**	1.2-2.8	6	43.7-44.1	60.5-74.2	48.1-57.6	2 X Cree 10 W packaged GaN HEMT
[37]**	1.5-2.55	6	42.6-44.4	50.7-69.7	43.3-57	2 X Cree 10 W packaged GaN HEMT
[38]**	4.1-5.6	6	38.4-39.5	51.7-60.8	38.5-46.5	250 nm GaN from WIN semi. Size: 6 X 125 µm
[39]**	1.6-2.7	6	43.8-45.2	56-75.3	46.5-63.5	2 X Cree 10 W packaged GaN HEMT
[40]**	1.1-2.4	6	43-44.4	59.1-78.8	46.8-63	2 X Cree 10 W packaged GaN HEMT
[41]**	1.8-2.6	9	44.8-45.2	53-70	49.6-63.4	Cree 10 W and 25W packaged GaN HEMT
This work*	1.8-2.6	9	40.5-43.9	61-76	43-60	Cree 8 W and 15W bare die GaN HEMT

* : Simulated result, **: Measured result

Chapter 5

X-KU DUAL-BAND HYBRID-MODE POWER AMPLIFIER

5.1 Introduction

Dual-band and multi-band PAs are preferable to obtain higher performance (better PAE and Pout than distributed and non-uniform distributed PAs) over a wide-band. Multi-band PA performs well at the narrow frequency bands of interest and is not focused on the instantaneous bandwidth over a wide band of operation. Hybrid mode PA, briefly introduced in Chapter 1, is a particular case of dual-band PA, where PA has different modes of operations at other frequency bands. This chapter discusses a dual-band hybrid mode PA design in detail. The PA will operate as a class F amplifier at 10 GHz (X band)and class F^{-1} amplifier at 15 GHz (Ku band).

5.2 Implementation of Dual-Band Hybrid-Mode PA

This design is implemented using HRL T3 40nm GaN HEMT device technology. The advantages of HRL's T3 GaN MMIC technology include high f_t and f_{max} (up to 220 and 400 GHz, respectively) with a scaled gate length of 40 nm while maintaining the high breakdown voltage (2-terminal more than 50 V) [60]. This technology offers 750mS/mm transconductance, R_{on} is 0.8 Ω.mm, power density 2W/mm at mm-wave frequencies, drain voltage 2-12V. The nonlinear large signal model includes the self-heating and via inductance effect. The gate metal electromigration current limit is 1.32mA/gate finger.

5.2.1 Design Details of X-Ku Hybrid Mode PA

HRL T3 GaN PDK includes the large signal model of FET devices. Although the gate finger and width are scalable, a recommended range is provided by HRL(based on measurement results), shown in table 5.1. 12X50 (No of fingers = 12, gate width = 50 μm) device is chosen to maximize the gain from a single-stage PA while maintaining good PAE and output power.

Table 5.1

Recommended Active Device Sizes in

40 nm GaN-on-SiC Process

Device size	No. of fingers	Width of gate (μ m)
2 X 25	2	10-50
4 X 37p5	4	15-75
2 X 50	6 and 8	25-100
2 X 50	10 and 12	25-100

The dual-band PA is targeted for the X and Ku frequency bands. f_1 is chosen as 10 GHz (from the X band), and f_2 is 15 GHz (from the Ku band). Both f_1 and f_2 are located around the mid-point of both frequency bands.

The selected 12X50 FET device is biased at class AB mode with I_{DQ} = 40mA (V_{GS} is -0.6V) and V_{DQ} = 12 V. After fixing the DC biasing, load-pull simulation has been performed and optimum impedances are chosen at 10 GHz and 15GHz to achieve maximum efficiency while maintaining reasonable Pout and Gain. At 10 GHz R_{opt} is 33+j*15 Ω, it can generate 30 dBm Pout, 13 dB low power gain, and 50% PAE. At 15 GHz, 40+j*18 Ω R_{opt} can maintain the same Pout and PAE with 11 dB low power gain. The load-pull simulations were performed after stabilizing the FET

using a parallel RC network.

At the targeted frequencies, the PA will operate as class F at f_1(at 10 GHz) and as class F^{-1} at f_2 (at 15 GHz). The target impedance terminations are shown in table 5.2.

Table 5.2

Target Design Impedances at f_1 and f_2

Mode	Z_{f_0}	Z_{2f_0}	Z_{3f_0}
Class F at f_1	33+j*15 Ω	Short	Open
Class F^{-1} at f_2	40+j*18 Ω	Open	Short

The schematic and layout of the proposed dual-band hybrid mode PA are shown in Figures 5.1 and 5.2. The layout in Figure 5.2 depicts different sections of the designed PA. The proposed PA size is 3mm X 5mm.

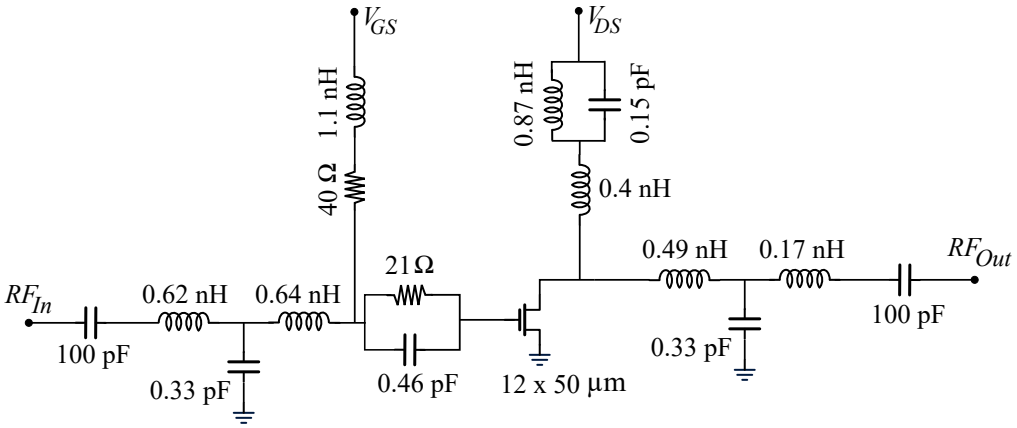


Figure 5.1: Proposed Hybrid Mode PA Schematic.

The input matching uses a two 2-section L matching network (region 2 in Figure 5.2) to ensure good matching for maximum gain at f1 and f2. Region 3 in Figure 5.2 shows the output matching network of the hybrid mode PA. This section is the most critical, as the harmonic terminations for both frequencies are taken care of

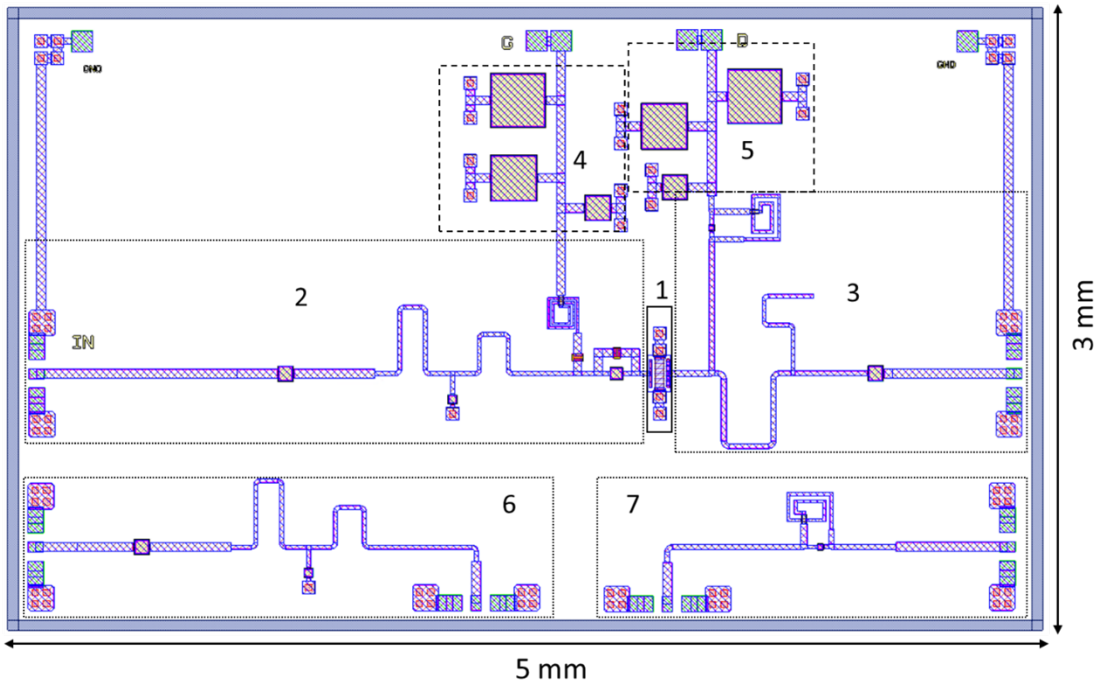


Figure 5.2: Proposed Dual Band Hybrid PA Layout. Different Parts of PA Are as Follows - 1. FET Device (12x50), 2. IMN, 3. OMN, 4. Gate Decoupling Network, 5. Drain Decoupling Network, 6. Test Structure 1, 7. Test Structure 2.

here. The device C_{DS} (approximately 130 fF at 10 GHz) is absorbed in the matching network to ensure a compact matching network design. At first, the 2nd and 3rd harmonic terminations were designed, and later R_{Opt} is matched to 50Ω. The region marked with a green dotted line in Figure 5.3 (left) is used to match the fundamental, and the rest of the area marked by a black line is used for harmonic tuning. Figure 5.3 (right) shows the realized impedance from the output matching network. The realized impedances at fundamental and harmonics for both f_1 and f_2 closely match the target design impedances tabulated in table 5.2. Some of the inductors in the schematic (Figure 5.1) are implemented using transmission lines in the final layout. This is done to utilize the design space in the best possible way and to establish good matching conditions for both frequency bands for maximum PAE at PSAT.

The design layout (in Figure 5.2) has two test structures (6 and 7). This will be used to troubleshoot the design if required during testing.

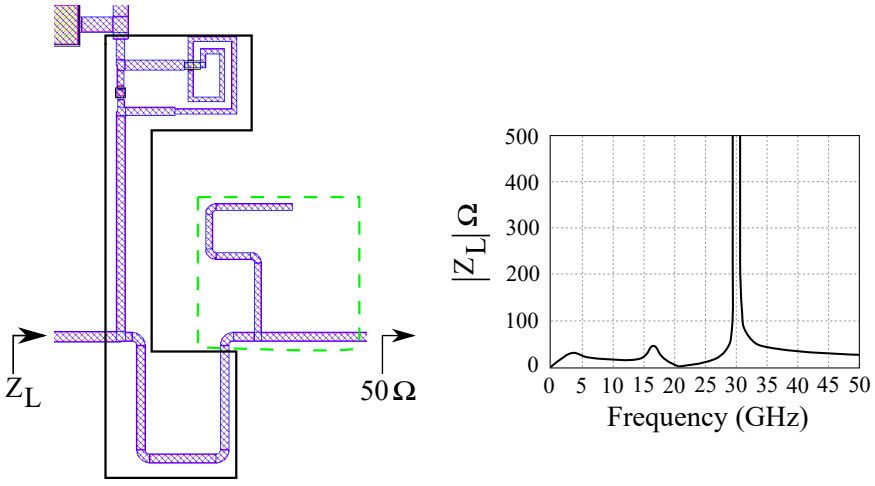


Figure 5.3: Left - Zoomed Output Matching Network, Right - Realized Impedance.

5.2.2 Simulation Results

Figure 5.4 shows the small signal simulation results of the proposed PA. The small signal gain (S_{21}) is 13.5 dB and 11.1 dB at 10 GHz and 15GHz respectively. The PA is well matched at both operational frequency bands (S_{11} < -10 dB). The PA in the wide frequency band range is unconditionally stable (K > 1, $\Delta > 0$).

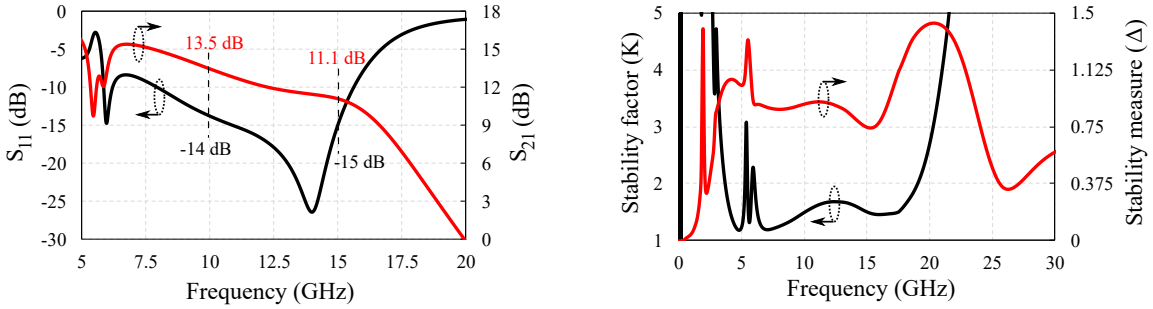


Figure 5.4: Left – S_{11} and S_{21} in dB, Right – Stability Factor and Measure (K and Δ) of the Proposed PA.

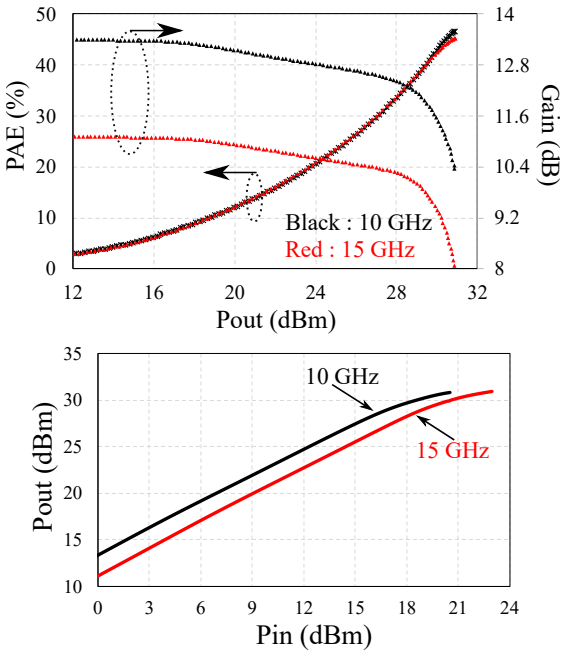


Figure 5.5: Top: PAE and Gain Vs. Output Power, Bottom: Pout vs Pin.

Figure 5.5 depicts large signal simulation results at 10 and 15 GHz. PSAT is 30.7 dBm and 30.6 dBm at 10 and 15 GHz, respectively. The PA has above 45% PAE at PSAT in both operational frequency bands. Gain is 13.5 dB and 11 dB at 10 and 15 GHz, respectively. Low power gain is 2.5 dB lower in f_2 (15 GHz) compared to f_1 due to the standard FET operation (gain drops with increase in frequency). Gain could be further improved by multistage PA design. Figure 5.6 shows the drain voltage and current waveforms at 10 GHz (left) and 15 GHz (right). Figure 5.6 (left) shows that voltage and current waveforms are square and half sinusoidal, showing class F PA mode. The dual situation for class F^{-1} is noticed in Figure 5.6 (right), square current, and half sinusoidal voltage waveforms. One point should be noted, as the gain at f_2 is lower than f_1; therefore, at f_2, the PA will need more input power to reach PSAT. This is observed in the results reported in Figure 5.5. The PA at f_1 reaches the PSAT when Pin = 20 dBm, whereas for f_2 Pin = 22 dBm at PSAT.

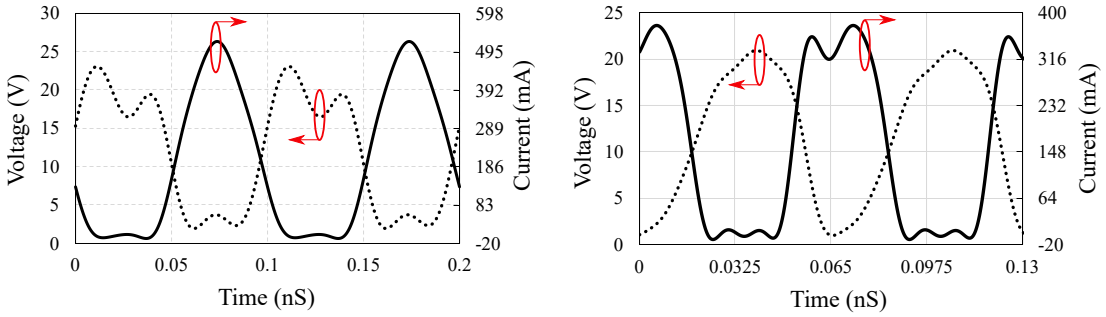


Figure 5.6: Voltage and Current Waveforms at Left - 10 GHz and Right - 15 GHz.

5.3 Summary

This work presents a hybrid-mode dual-band X-Ku band PA implementation in the HRL GaN-on-SiC 40 nm process. The detailed design procedure is explained in this chapter. Table 5.3 summarizes the performance of the designed PA and compares it with other state-of-the-art PAs.

Table 5.3

Performance Summary

Ref.	Process used	Freq. (GHz)	PAE (%)	Pout (dBm)	Gain (dB)	Topology
[56]**	150 nm GaAs	9 16.1	45.5% 40%	20.2 20.5	16.9 14.5	2 stage class AB
[57]**	250 nm GaAs	8.5-9.5 15.5-16.5	33.5-44.4% 37.1-38.4%	28.8-29.6 39.7-30.1	21-24.8 23	Reconfigurable 2 stage. 2nd stage cascaded
[58]**	250 nm GaN	6-10.2 10.2-18	15-34% 15-34%	34-36 34-38.5	17-27 15-22	Reconfigurable 2 stage.
[59]**	250 nm GaN	9-10 13.5-16	31-36.5% 30-35.7%	36.5-37.2 35-36.4	12 10	2 parallel HEMTs
This work*	40 nm GaN	10 15	45.9% 45.4%	30.7 30.6	13.5 11	Single stage hybrid mode

* : Simulated result, **: Measured result

Chapter 6

LOW OVERHEAD BUILT-IN SELF-TEST TO MEASURE POWER AMPLIFIER OUTPUT IMPEDANCE MISMATCH

6.1 Introduction

Following-generation communication systems are designed to provide higher capacity, cost-effective, and efficient transmitters to serve more users. In this regard, the massive multiple input/output (MIMO) breakthrough has enabled extended spectrum efficiency to increase the capacity and reliability of the overall transmitter system. However, integrating large active antennas of the MIMO system at transmitters to the power amplifiers (PA) imposes many design challenges [66], [77]. In an ideal scenario, PA is permanently terminated with a 50Ω load, but in MIMO, antenna impedance changes with the beamforming steering angle. Therefore, the PA load is no longer fixed, which affects its power and efficiency characteristics. Furthermore, it can also degrade the stability and linearity of the PA. The digital pre-distortion (DPD) technique could be used to recover the linearity performance of the PA. However, dynamic load variation also degrades the DPD performance [67], and prior knowledge of variable loads is needed to recover it.

Different techniques have been employed to mitigate the performance degradation of PA due to the variable load. Some of the popular methods involved : (1) using a circulator between PA and output load, but the larger form factor of the circulator makes it difficult for integration. (2) Tunable matching networks [65],[70],[71] are used to cover a wide impedance range, but most of the time it is limited by the Q of the circuit elements. (3) Balanced PAs [69] is sometimes used due to their good

matching capabilities, but in large signal operation, the linearity gets affected; for that reason, it operates with low efficiency at power back off. (4) Directional couplers [68] also measure the load variation.

The most prominent method to measure variable impedance is multi-port reflectometry [72] due to its low overhead and more straightforward implementation. Using the multi-port technique, the reflection coefficient can be measured by the scalar measurement of the RF power detectors. The most common multi-port reflectometer has six ports, typically called a six-port reflectometer, where two ports are for RF input and output, and the remaining four are terminated with power detectors and used as measurement ports. The number of measurement ports (number of power detectors) is adjusted depending on the system's complexity. The measurement ports are connected by a linear network where the power detectors are strategically positioned to yield a singular solution for the reflection coefficient. Several works [63], [65], [72]-[75] have been reported that used multi-port reflectometry in printed circuits and integrated circuit boards to measure variable loads.

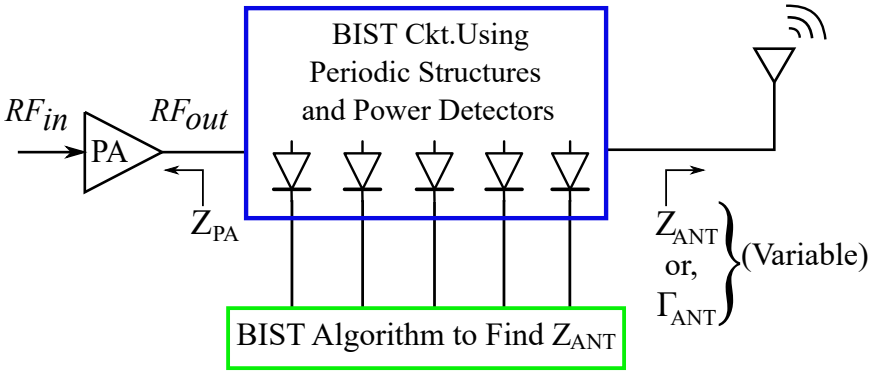


Figure 6.1: BIST for Impedance Monitoring Using Periodic Structures.

This work implements a multi-port reflectometer with a periodic structure, simplifying the overall measurement and calibration procedure. This technique was originally reported in [62] with a detailed close-form reflection coefficient calculation.

Most of the multi-port reflectometers [63], [76] use >5 loads for calibration, whereas this method used only 3-4 loads. Figure 6.1 shows the top-level block diagram of the periodic structure-based BIST monitoring system, where these periodic structures are easily integrated into the existing output matching network of a PA by partitioning any existing series lumped component into four segments and placing power detectors in each segment. This simplifies the overall impedance monitoring circuit implementation and integration to a PA.

The prior work integrated the BIST for impedance monitoring with a two-section LC output matching network. However, it did not report any results with high input power to the BIST. This work proposes two BIST circuit prototypes to withstand the high output power of the PA without interfering with the impedance monitoring capability proposed in the original work. The current work reports the impedance monitoring results with a commercially available PA for the 1.5-2.5 GHz frequency range. The measurement results show considerable agreement with the test loads. The maximum measured magnitude and phase errors of impedance estimation are 0.72 dB and 11.6°, respectively.

6.2 Output Impedance Monitoring Using Periodic Structure

The proposed periodic structure [62] measurement system uses a transmission matrix and admittance measurement to calculate the output reflection coefficient (Γ_{ANT} in Figure 6.1). An example of a low-power implementation using a single-section LC match circuit is shown in Figure 6.2. The series element in the matching network, L_{match} in Figure 6.2, is divided into four periodic sections, $L_{match}/4$, each section called a unit cell. The power detectors are placed at the edge of these unit cells; therefore, 5 power detectors are required. Next, the calibration is performed using 3 known loads, and the eigenvalue (λ) of the unit cell is calculated. λ is unique

to the unit cell and will not change with variable Z_{ANT}. Once the λ is known, the error box correction approach is used to find the variable load explicitly. All these calculations are part of the BIST algorithm. The variable load will be estimated by feeding the information of three calibration loads and five-diode DC voltage (V_1-V_5) measurements to the BIST algorithm. The algorithm is discussed in detail in the prior work, and the same is followed here.

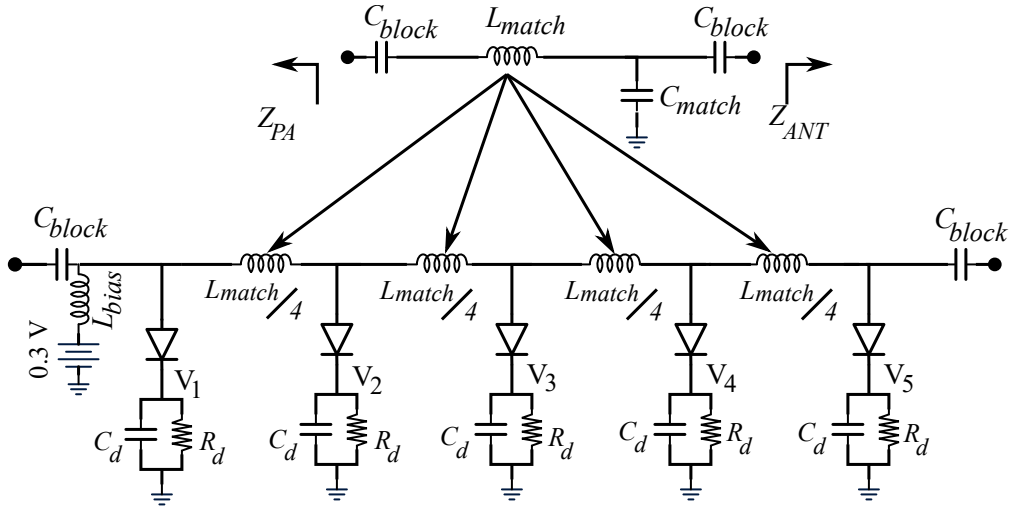


Figure 6.2: Example Design Implementation of BIST Impedance Monitoring with Output Matching Network for Low-power Applications. C_d = 10pF, $R_d = 100k\Omega$, L_{bias} = 10nH, C_{block} = 10pF.

The design example shown in the prior work and Figure 6.2 is valid for low-power applications as the diodes (BAT15-02LRH) will be saturated in high-power regions (> 17 dBm). Moreover, if high power is applied, the RF Schottky diodes will move from the square law region. This work proposes a design modification using a capacitive network (shown in Figure 6.3) to mitigate this high-power application limitation. It is assumed that 50 Ω terminates both the PA and antenna ($Z_{PA} = Z_{ANT} = 50\Omega$). Therefore, a 50$\Omega$ transmission line connects the PA and the antenna. To calculate the impedance variation of the antenna (Z_{ANT}), a 50Ω line is equally divided into 4 parts, as shown in Figure 6.3, and power detectors are connected at the edges.

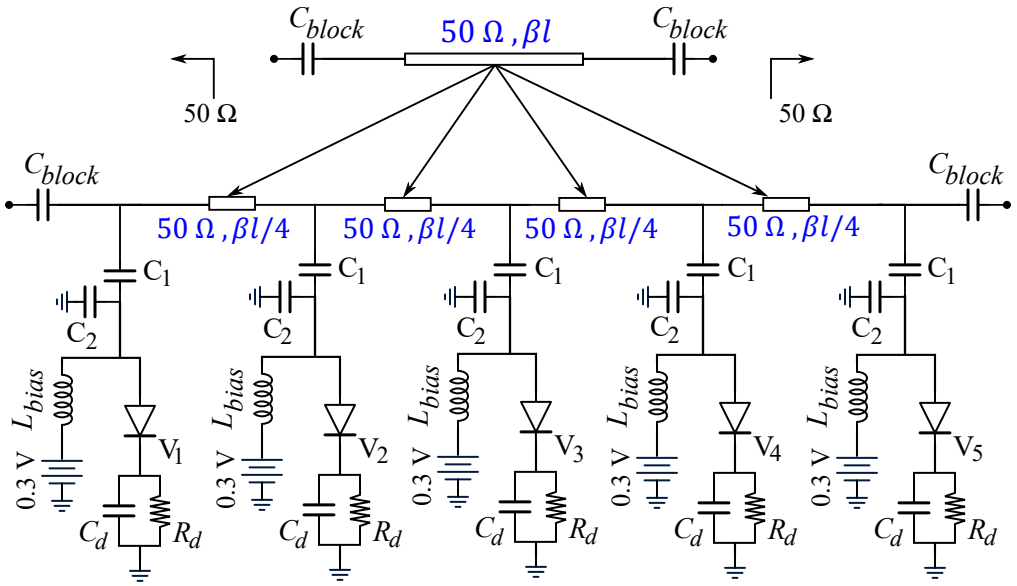


Figure 6.3: Proposed Impedance Monitoring Using a Capacitive Network for High-power Applications. C_1 = 500fF, C_2 = 5pF,C_d = 10pF, $R_d = 100k\Omega$, L_{bias} = 10nH, C_{block} = 10pF.

V_1-V_5 DC voltages are measured across C_d and R_d (10pF and 100kΩ, respectively) and used for the Γ calculation. The value of the C_1 and C_2 will depend on the specific diode model and frequency of operation. The same diode from Infineon as the prior work is used in this implementation. The C_1 and C_2 are calculated to ensure the diode's input power is small enough to keep it in the square law region. In this implementation, the center frequency is selected as 2 GHz. The value of C_1 is calculated to be 500 fF. This small-value capacitor is realized using an inter-digitized capacitor in practical circuit implementation. C_2 is calculated as 5 pF.

Another design option using a resistive network (R_1 and R_2) is shown in Figure 6.4. The same design targets as the capacitive network are followed in this case. To set the correct input drive levels to this specific diode, the ratio of R_1/R_2 has become very high (10^6), which will cause a significant loss in the system, and values of the resistors would be difficult to implement on a PCB. To overcome this problem, a shunt capacitor (C_3 = 4pF) is connected, as shown in Figure 6.4. C_3 reduces the

R_1/R_2 to 5.

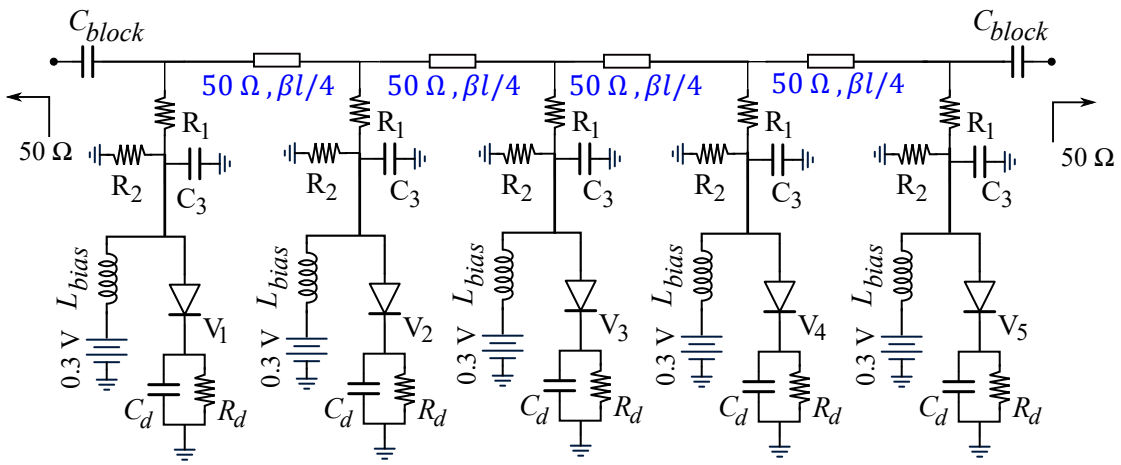


Figure 6.4: Proposed Impedance Monitoring Using a Resistive Network for High-power Applications. $R_1 = 1k\Omega$, $R_2 = 200\Omega$, $C_3 = 4$pF, $C_d = 10$pF, $R_d = 100k\Omega$, $L_{bias} = 10$nH, $C_{block} = 10$pF.

The designs shown in Figures 6.3 and 6.4 are simulated in Keysight's ADS at 2 GHz with 96 test loads distributed across the Smith chart. The input power is set to 26 dBm to check the viability of the impedance monitoring at high output power. Figure 6.5 depicts the test and the measured loads obtained through power detector measurements using the capacitive and resistive networks, respectively. The measured loads closely follow the test loads. Three calibration loads are selected far apart to maximize the information contributed by each load.

In the proposed designs, it is assumed that Z_{PA} is 50Ω. However, the practical PA's reflection coefficient at the output does not always perfectly match (> -10 dB). Figure 6.6 illustrates how Z_{PA}'s variation impacts the impedance monitoring function of the BIST. For this analysis, the VSWR of test loads is selected below 3:1, and calibration loads are not considered. The colormaps in Figures 6.6 top and bottom exhibit the maximum magnitude and phase errors, respectively. The red box in both figures represents the optimal value for Z_{PA} (50+j0Ω), where the error is minimal. The black dotted box in Figure 6.6: top highlights the impedances where the magni-

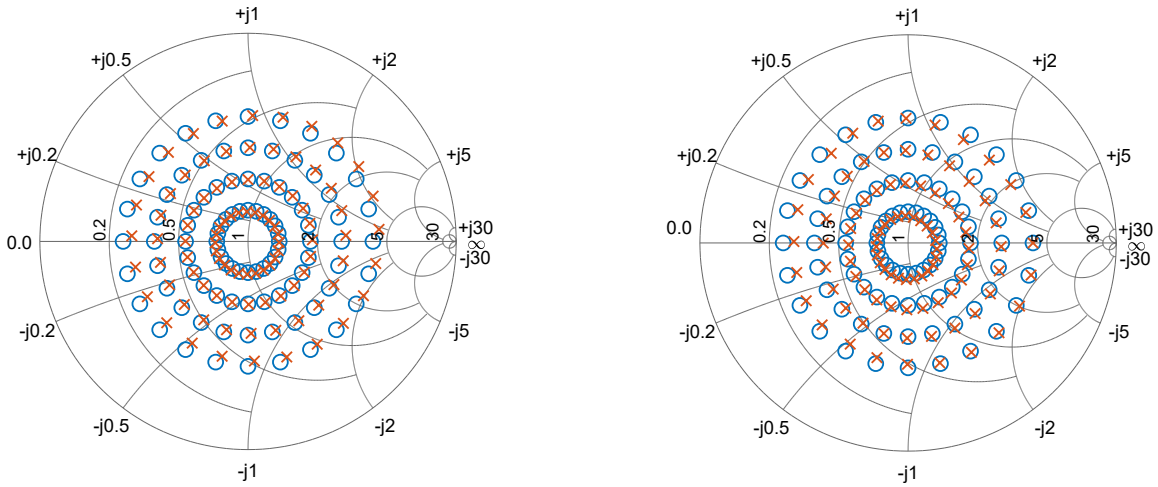


Figure 6.5: Design Simulation Results of Test Loads (o) and Measured Loads (×) at 2 GHz. Left: Capacitive Network. Right: Resistive Network.Calibration loads: (48+j31)Ω, (12+j6)Ω, (24-j24)Ω.

tude estimation error is below or at 1dB. Figures 6.6: bottom shows that the phase estimation error remains within 8°, apart from the area highlighted in black. Based on this analysis, it is recommended to use the gray-shaded region in Figure 6.6: top as the preferred zone for Z_{PA} since both the magnitude and phase error are minimal. This study is done for the capacitive circuit, and the resistive circuit follows the same trend. To avoid the impedance estimation error, the BIST monitoring circuit should be co-designed with the PA's output matching circuit.

6.3 Hardware Experiment Results

To validate the proposed BIST circuits, both capacitive and resistive circuits are fabricated in Rogers 4350B material, as shown in Figure 6.7. The center design frequency is selected as 2 GHz. RF Schottky diode from Infineon (BAT15-02LRH) is used as the power detector and is biased at 0.3V. To compare the reflection and transmission scattering parameters, the 50Ω line without any power detectors is also realized.

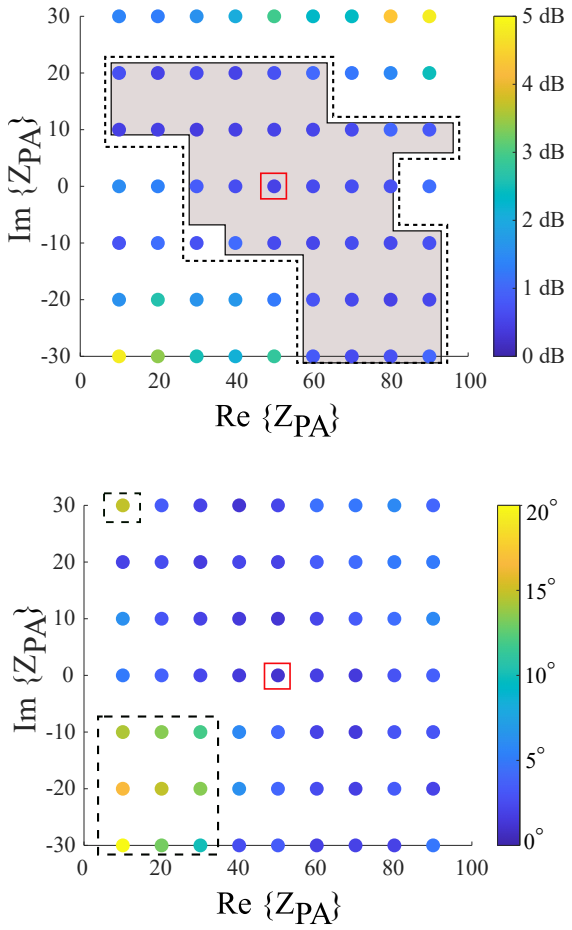


Figure 6.6: Effect of Z_{PA}'s Variation on Impedance Estimation. Top: The Maximum Magnitude Error, and Bottom: Maximum Phase Error.

Figure 6.8 depicts the small signal measurement results of the BIST circuits. The return loss (S_{11}) characteristics of the fabricated BIST circuits are shown in Figure. 6.8a, which displays a good match and follows the same characteristics as the 50Ω line. Figure 6.8b shows the insertion loss (S_{21}) of the BIST circuits. The capacitive BIST circuit (red curve in Figure 6.8b) closely follows the 50Ω line, with S_{21} at 2 GHz being 0.5dB. However, due to the lossy resistance, the resistive BIST circuit shows more loss (S_{21} at 2 GHz being 1.45 dB). The resistors used in this implementation do not have precise RF performance; therefore, a low pass characteristic is observed, which was not present in the ADS simulation. This problem can be overcome by

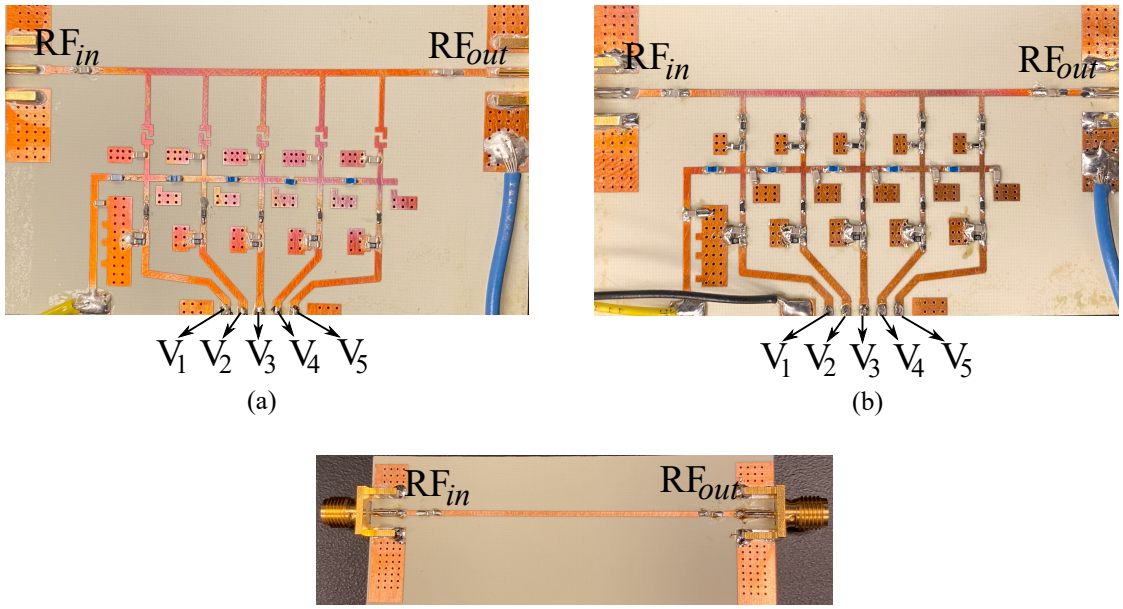


Figure 6.7: Fabricated Boards. (a) Capacitive BIST Circuit. (b) Resistive BIST Circuit. (c) 50Ω Line Without Power Detectors.

using high RF precision resistors or implementing them in any IC process.

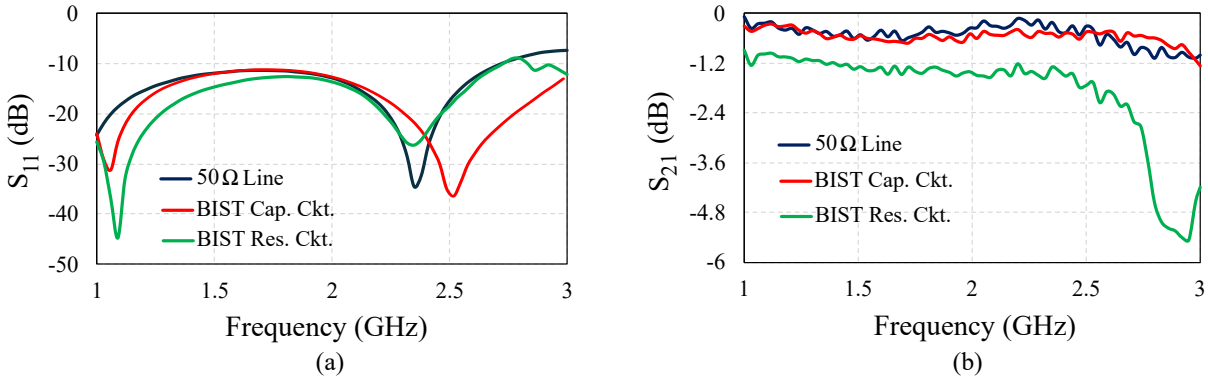


Figure 6.8: Small Signal Measurement Results of the Fabricated BIST Circuits.

To check the viability of the proposed BIST circuits with PA, a large signal simulation has been performed using a commercially available 5W power amplifier. The small signal gain of the PA is 24 dB at 2 GHz. The BIST circuits are connected at the output of the PA under test. The low-power circuit (reported in [62]) is also

fabricated in the Rogers material and used in larger signal simulations to make a fair comparison. Figure 6.9 exhibits the power sweep result of the PA without and with three BIST circuits (capacitive, resistive, and low power). The output power in the low-power BIST circuit saturates after 22 dBm Pout, whereas the capacitive and resistive BIST circuits maintain the normal PA performance. Similar to the small signal results, the resistive BIST has more loss in large signal simulation compared to the capacitive BIST circuit. The power sweep shows the same performance trend across the 1.5-2.5 GHz frequency band.

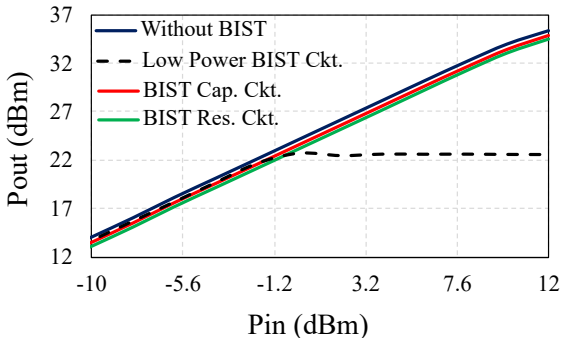


Figure 6.9: Large Signal Measured Results of the BIST Circuits at 2 GHz.

Figure 6.10 shows the hardware experiment set up to test the BIST's impedance monitoring capability. The output of the BIST is connected to a manual impedance tuner from Maury Microwave, and a 50Ω RF load terminates the end of the tuner. The screw positions are changed to create variable load conditions at the BIST output, and the voltage measurements (V_1-V_5) from the multimeter are saved to estimate the variable impedance. The true test loads are measured using a Power Network Analyzer (Agilent E8361A), and then the tuner scale positions are repeated to create the same load conditions. To ensure accuracy, the tests are repeated multiple times.

Figure 6.11 presents the impedance monitoring results from the capacitive and resistive BIST circuits at 2 GHz. During the impedance estimation, the output power

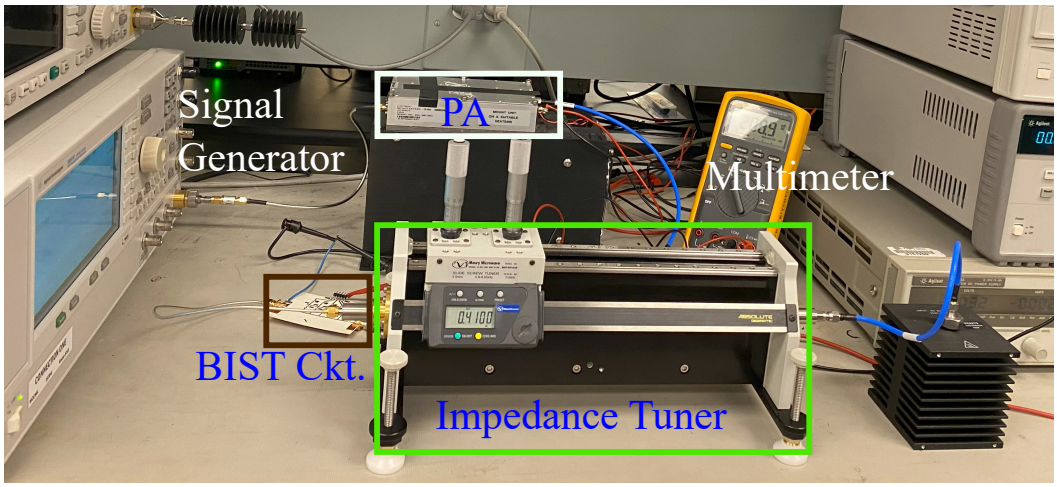


Figure 6.10: Experiment Set-up to Test the Impedance Monitoring of the BIST Circuits.

from the PA is kept at 27.5 dBm. The true test loads are randomly selected by using the impedance tuner. The calibration loads are excluded from the reported results. Overall, the impedance estimation from both the BIST circuits is close to the true test loads. The maximum magnitude and phase error in impedance estimation from the capacitive BIST circuit is 0.72 dB and 11.6°, respectively. The resistive BIST circuit exhibits 2.4 dB and 17° maximum magnitude and phase error. The main source of this error is the PA's output impedance. From the small signal measurement of the PA, the output impedance at 2 GHz is measured as (12+j10)Ω. As discussed in Section 6.2, the magnitude and phase estimation error around that impedance would be $\leq$1 dB and $<$ 8° (Figure 6.6). However, the resistive BIST circuit has more errors than the capacitive circuit. The probable cause is the low-precision resistors used in the circuit.

The measurement results show that the capacitive BIST circuit performs better than the resistive one. Although the degradation in RF performance comes from the low-precision resistors, the resistive circuit is inherently more lossy than the capacitive one.

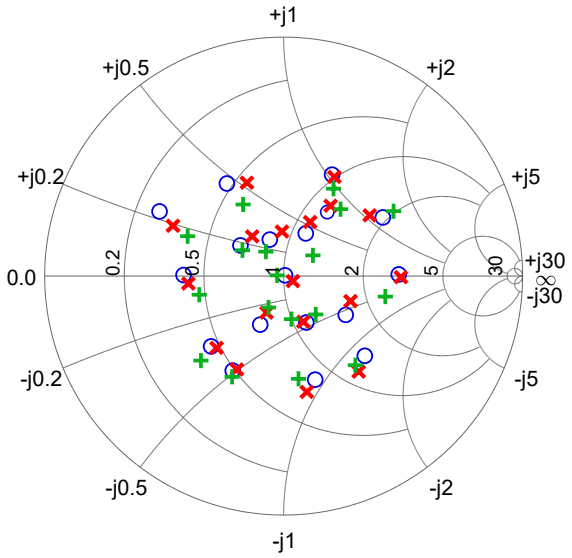


Figure 6.11: Impedance Monitoring Experiment Results at 2 GHz. True Test Loads (o), Capacitive (×), and Resistive (+) BIST Circuit.

The capacitive BIST circuit is measured across 1.5-2.5 GHz, and the impedance monitoring results at 1.5 and 2.5 GHz are shown in Figure 6.12 (a-b). The estimated loads closely follow the true test loads. The magnitude and phase estimation errors are 1.6 dB and 0.75 dB, and 11.2° and 13° at 1.5 GHz and 2.5 GHz, respectively. The overall impedance estimation error will be minimized if the BIST circuit is co-designed with the PA's output matching network.

6.4 Summary

This work reports two BIST circuits for monitoring the PA's output impedance without affecting its normal operation. The detailed design procedure for both circuits is discussed here. The prototype for both circuits is designed at 2 GHz in a Rogers 4350B substrate and measured with a commercially available PA. The experimental results show that the resistive circuit has more loss than the capacitive BIST circuit, and the latter is a more viable option. The capacitive BIST circuit exhibits

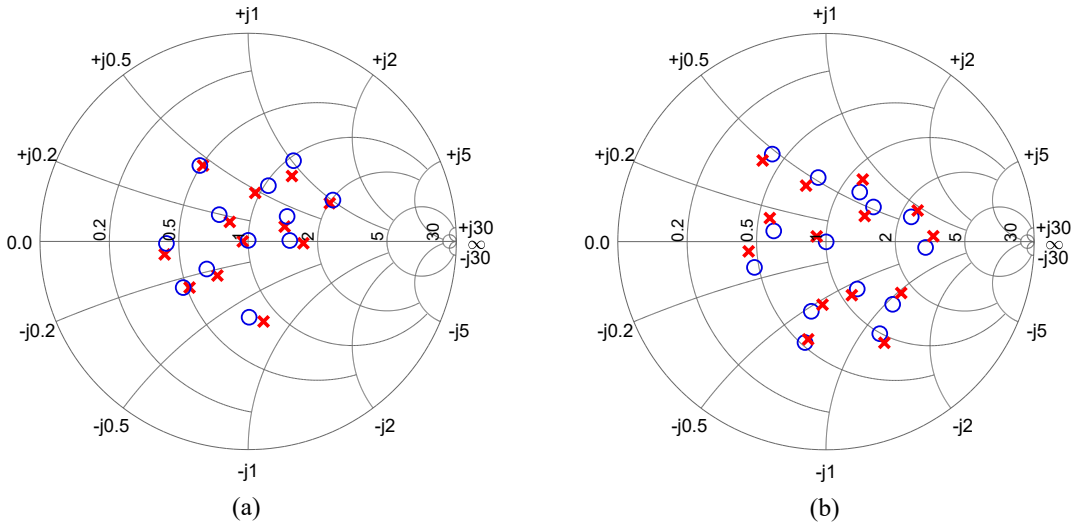


Figure 6.12: Impedance Monitoring Results (a) 1.5 GHz, (b) 2.5 GHz. True Test Loads (o), Capacitive (×) BIST Circuit.

a maximum of 0.72 dB and 11.6° magnitude and phase estimation error.

Chapter 7

CONCLUSION

This dissertation presents five cutting-edge high-performance RF PAs designed for high dynamic range and/or high bandwidth wireless applications. In Chapter 2, an optimized load network for a phase-exploited symmetrical DPA (PE-DPA) is presented. The presented work explores the effect of nonlinear phase distortion and its effect on drain efficiency. This work compares PE-DPA behavior from two different output networks and selects the one with superior performance for hardware implementation. The PE-DPA is implemented using GaN HEMT devices and achieved 44.3 dBm saturated output power (PSAT), a drain efficiency of 73% at PSAT and 44% at 8 dB OBO under continuous wave (CW) excitation. The implemented PA also processes a 20 MHz LTE signal. The proposed PE-DPA shows competitive performance compared to state-of-the-art DPAs. In Chapter 3, the PE-DPA is re-designed using parallel combining to increase the bandwidth over a conventional DPA. A detailed performance analysis with respect to frequency is presented for the PE-DPA with and without parallel load combining. To validate the presented technique, a prototype is designed using GaN HEMT devices, and simulation results demonstrate that the PE-PDPA achieves state-of-the-art performance (60% - 77% and 43% - 54% drain efficiency at 43 dBm PSAT and 8 dB backoff, respectively) over the 3.3-3.6GHz operating band. Chapter 4 presents a detailed theoretical analysis of an asymmetrical continuous mode class J DPA. The reported DPA achieves continuous mode class J operation by varying the reactive part of the complex load, which is realized by a novel post-matching network. In this work, two asymmetrical DPAs (one standard asymmetrical DPA and one asymmetrical CM DPA) are designed using GaN HEMT

devices and compared to one another. The prototype DPA achieves 61% - 76% efficiency at 43 dBm PSAT and 43% - 60% at 9 dB OBO when operating from 1.8-2.6 GHz under CW excitation. Chapter 5 describes a hybrid-mode dual-band X-Ku band PA that is implemented in the HRL GaN-on-SiC 40 nm process. The implemented PA functions as class F at 10 GHz and as class F^{-1} at 15 GHz. The dual-band PA holds state-of-the-art performance at both operating frequencies by incorporating the advantage of hybrid mode PA operation. The proposed PA shows competitive performance with other state-of-the-art PAs. Chapter 6 presents a periodic structure-based built-in self-test (BIST) technique integrated into a PA to monitor impedance variation at the PA's output. A capacitive divider circuit is introduced in this work to prevent the power detectors from saturating at high PA output power. The implemented BIST with the PA minimally affects the nominal operation of the PA. The designed prototype of the BIST monitoring circuit integrated into a commercial class B PA shows good agreement with the proposed theory. The simulation results illustrate the proposed BIST monitoring circuit is effective over a wide range of frequencies. Experimental validation results are also reported with an industry-provided PA prototype at 1.5-2.5 GHz.

In this dissertation, PA architectures are proposed to support the demand for high dynamic range and wideband operation in modern wireless infrastructure. A detailed analysis and design implementation procedure is presented for each of the proposed designs. The hybrid mode PA design could be further extended to process high PAPR signals to support complex modulation techniques. Moreover, the information gained from the BIST monitoring circuit can be used for wideband PA implementation. An interesting addition would be an impedance correction circuit along with the BIST monitoring to dynamically tune the PA's impedance accordingly with frequency.

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