# An Active EMI Cancellation Technique Achieving a 25-dB Reduction in Conducted EMI of LIN Drivers in System Basis Chips.

by

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ABSTRACT

Modern day automobiles are becoming more connected and reliant on wireless connectivity. Thus, automotive electronics can be both a cause of and highly sensitive to electromagnetic interference (EMI), and the consequences of failure can be fatal. Technology advancements in engineering have brought several features into the automotive field but at the expense of electromagnetic compatibility issues. Automotive EMC problems are the result of the emissions from electronic assemblies inside a vehicle and the susceptibility of the electronics when exposed to external EMI sources. In both cases, automotive EMC problems can cause unintended changes in the automotive system operation.

Robustness to electromagnetic interference (EMI) is one of the primary design aspects of state-of-the-art automotive ICs like System Basis Chips (SBCs) which provide a wide range of analog, power regulation and digital functions on the same die. One of the primary sources of conducted EMI on the Local Interconnect Network (LIN) driver output is an integrated switching DC-DC regulator noise coupling through the parasitic substrate capacitance of the SBC. In this dissertation an adaptive active EMI cancellation technique to cancel the switching noise of the DC-DC regulator on the LIN driver output to ensure electromagnetic compatibility (EMC) is presented. The proposed active EMI cancellation circuit synthesizes a phase synchronized cancellation pulse which is then injected onto the LIN driver output using an on-chip tunable capacitor array to cancel the switching noise injected via substrate. The proposed EMI reduction technique can track and cancel substrate noise independent of process technology and device parasitics, input voltage, duty cycle and loading conditions of the DC-DC switching regulator. The EMI cancellation

system is designed and fabricated on a 180nm Bipolar-CMOS-DMOS (BCD) process with an integrated power stage of a DC-DC buck regulator at a switching frequency of 2MHz along with an automotive LIN driver. The EMI cancellation circuit occupies an area of 0.7 $mm^2$, which is less than 3% of the overall area in a standard SBC and consumes 12.5 mW of power and achieves 25 dB reduction of conducted EMI in the LIN driver output's power spectrum at the switching frequency and its harmonics.

DEDICATION

*To Baba, Ma, Dada, and all the wonderful teachers and friends I have been blessed with!*

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# CHAPTER 1

# INTRODUCTION

## 1.1. Serial Communication Protocols in Automobiles

In recent times as technology advances, the need to place a larger number of electrical and electronic systems into automobiles has increased dramatically. Modern day vehicles rely extensively on sensing and controlling many mechanical/electronic parameters for safe and comfortable driving with reduced fuel consumption. Serial communication protocols are typically used for communication or exchange of information between Electronic Control Units (ECUs) and sensors in vehicles. As shown in Fig. 1.1, various automotive serial communication protocols are used inside vehicles such Controller Area Network (CAN), Local Interconnect Network (LIN) and FlexRay [1]. The CAN bus is often used to run real time critical functions inside vehicles like engine management, antilock brakes, cruise control etc. The LIN bus manages non-critical applications such as door module, headlight, wiper control etc. and is supplemental to CAN bus as shown in Fig. 1.2 [1]. The FlexRay protocol is used for applications which require high bitrate with error detection and correction such as adaptive cruise control, active suspension etc. The robustness of these serial communication protocols is of utmost importance to maintain safe and secure communication in a noisy automotive environment.

## 1.2. Electromagnetic Interference (EMI) in Automotive Environment

Environmental electromagnetic pollution has drastically increased over the last few years. The wireless communication systems, various electronic appliances and cellular frequencies contribute to a noisy electromagnetic environment, thereby adversely affecting

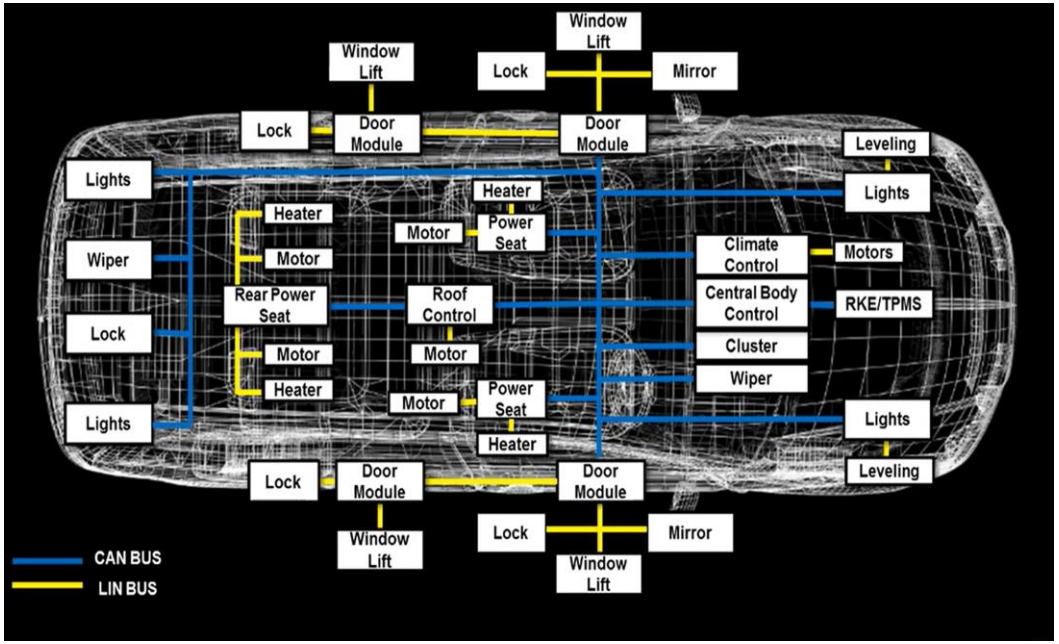



Figure 1.1: LIN and CAN Bus in Automotive Body Network.

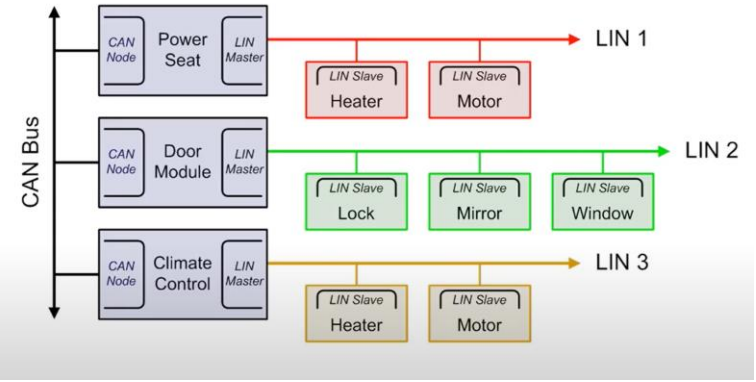



Figure 1.2: LIN and CAN Bus Connecting Multiple Nodes in a Vehicle.

sensitive electronic systems. The electromagnetic environment associated with automotive applications is critical and detrimental to electronic circuits due to the presence of multiple electromagnetic interference (EMI) sources like motors, ignition, and infotainment systems. There are two main classes of EMI – radiated and conducted emissions. The conducted EMI is typically coupled via cables and physical conductors such as power connections, parasitic impedances as well as ground connections. The radiated EMI gets coupled via radio transmission sources through the air due to electric fields (capacitive coupling) or magnetic fields (magnetic coupling). Advanced automotive electronic control which includes features like GPS, self-driving functionality coupled with electric vehicle (EV) technology resulted in denser atmosphere of electromagnetic waves. This results in greater EMI inside the vehicle leading to malfunctioning of the electronic devices. EMI also adversely affects the performance of an integrated circuit internally and other electronic components within a close range in an automotive electronic system. EMI from external sources like mobile phones and other broadcasting signals can interfere with the vehicle's electronic system when close to the transmitting antenna.

### 1.3. Electromagnetic Compatibility (EMC) for Communication Protocols

There are several popular automobile communication protocols such as the Local Interconnect Network (LIN), the Controller Area Network (CAN), FlexRay and the Media Oriented Systems Transport (MOST). The biggest challenges in automobile communication networks are Electromagnetic Interference (EMI), serviceability, and cost constraints. Strong EMI pulses often couple into the communication system through wiring and cause burst errors. EMI from other wireless applications, such as cellular phone systems, citizen band radio, weather radar, etc., also contribute to single-bit or burst errors in automobile networks. It is the major reason for performance degradation which often increases the number of retransmissions, reduces network efficiency, and occasionally causes a total halt in communications. Using shielded cables helps to reduce the effect of EMI significantly. However, it also reduces the serviceability and increases the cost significantly. Cable shielding needs to be carefully grounded at both ends of the communication link which is often vulnerable in practical systems. Replacing and repairing shielded cables are also more costly, inconvenient, and unreliable. Therefore, shielded cable is considered as the last solution by the automobile industry. Measures to improve electromagnetic compatibility commonly include filtering, shielding, and optimizing wiring. In addition, EMC performance of electronic equipment is improved, and filtering technology is adopted to suppress conduction coupling, etc.

## 1.4. Organization of the Dissertation

The rest of the thesis is organized as follows: Chapter 2 describes LIN transceiver/driver and conducted EMI in LIN driver. Chapter 3 discusses about the LIN driver integrated in a system basis chip (SBC) and gives a brief overview of EMI issues in LIN driver in presence of switching regulators. Chapter 4 introduces the theory of the proposed Active EMI Cancellation Technique along with the architecture. The design blocks used in the architecture are also described in this section along with the closed loop simulation results. Chapter 5 shows the measured results of the proposed EMI cancellation scheme and noise cancellation achieved. Chapter 6 concludes the thesis with the research conclusion and gives an account of the future improvements for complete product development.

# CHAPTER 2

# LIN DRIVER

LIN is defined as a single-wire, serial communications protocol which is low cost, low speed (maximum transmission 20 kbits/s) and primarily intended to be used for distributed electronic systems in automotive applications. The core of LIN is a serial network protocol controller and a physical layer transceiver. Typical applications controlled by LIN include the car door control (windows, door locks, mirrors,), seats, lighting, rain sensors, intelligent lighting systems and so on. Owing to the very stringent EMC requirements concerning automotive electronics, the main concept behind the LIN definitions of the physical layer is that it should be able to withstand strong levels of electromagnetic noise, without in turn generating excessive electromagnetic emission which could disturb neighboring circuits. All this makes LIN a valuable communication system, not only in automotive applications, but eventually also in home appliances.

## 2.1. LIN Transceiver

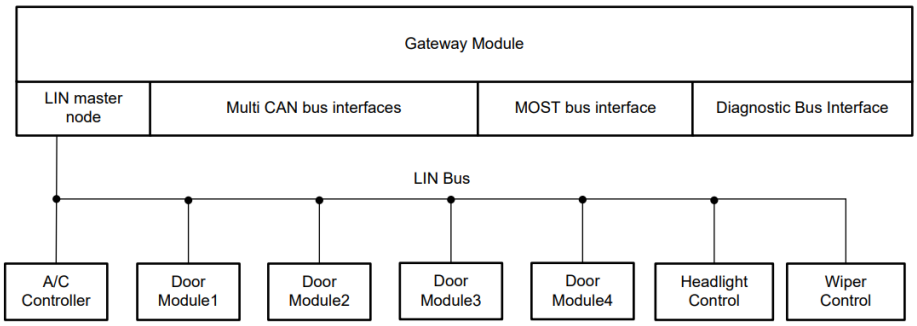



Figure 2.1: LIN Transceiver.

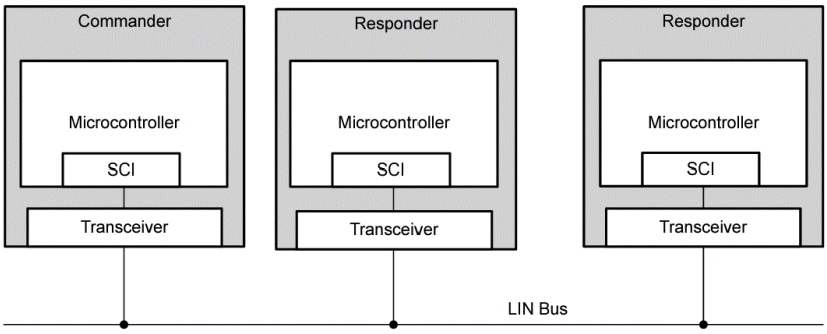



Figure 2.2: High-Level LIN Transceiver in Network.

As shown in Fig. 2.1, a LIN transceiver network relies on single master communicating with up to 16 slave devices (A/C Controller, Door, Headlight Control, Wiper Control etc.) [2]. The transceiver transmitter converts the logic level LIN protocol data stream on the LIN input into a battery level LIN bus signal. The transceiver receiver converts the high voltage data stream from the LIN bus to logic level signals that are sent to the microprocessor for further processing. The network protocol controller provides synchronization, logic, error detection, and other features that are usually associated with LIN. As shown in Fig. 2.2, the network protocol controller for LIN is software controlled and uses SCI interface [2]. The gateway module includes the interfaces with all the buses which typically comprise the vehicle network. The LIN master is configured as part of the gateway module. The different localized control modules connected to the LIN bus are the slave modules. A microcontroller is programmed with the LIN protocol and used to drive communication to the transceiver. The typical voltage levels for the transmitter and the receiver are of most microcontroller levels – 3.3V and 5V. The LIN bus usually operates at battery voltage ranging from 9 V to 24 V.

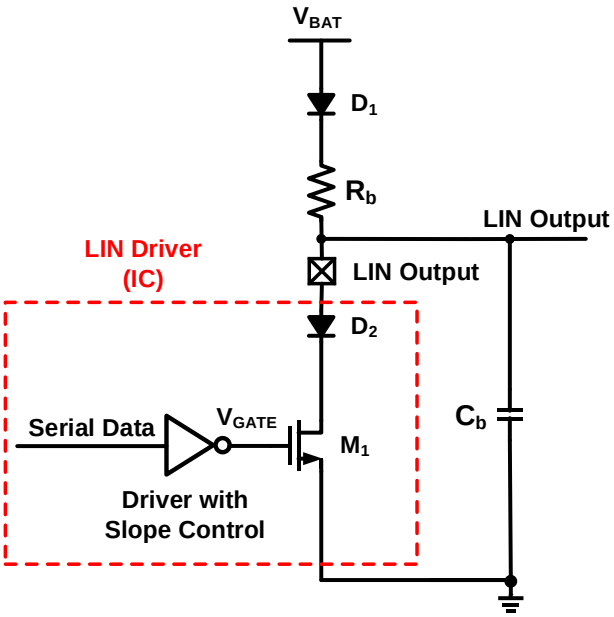



Figure 2.3: LIN Driver.

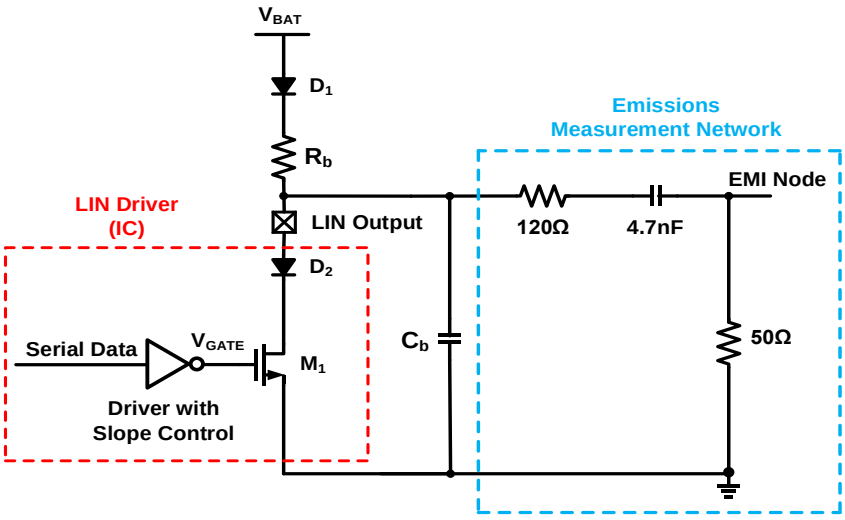



Figure 2.4: LIN Driver with EMI Measurement Network

## 2.2. LIN Driver

With reference to the LIN driver shown in Fig. 2.3, the serial data intended for communication is transmitted using a transistor $M_1$ driven by a slope-controlled driver. A logic '1' is transmitted on the LIN bus with a voltage of ($V_{BAT} - V_{D1}$) where $V_{D1}$ is the voltage drop across the diode $D_1$ whereas a logic '0' is transmitted with a voltage of $V_{D2}$ where $V_{D2}$ is the voltage drop across the diode $D_2$. The function of diodes $D_1$ and $D_2$ is to provide reverse polarity protection to the LIN bus connected to the battery voltage whereas $R_b$ (= 1kΩ) is the external pull up resistance and $C_b$ (~ 170-220 pF) is the total bus capacitance. $D_1$ is an external diode on the board while $D_2$ is an on chip high voltage diode.

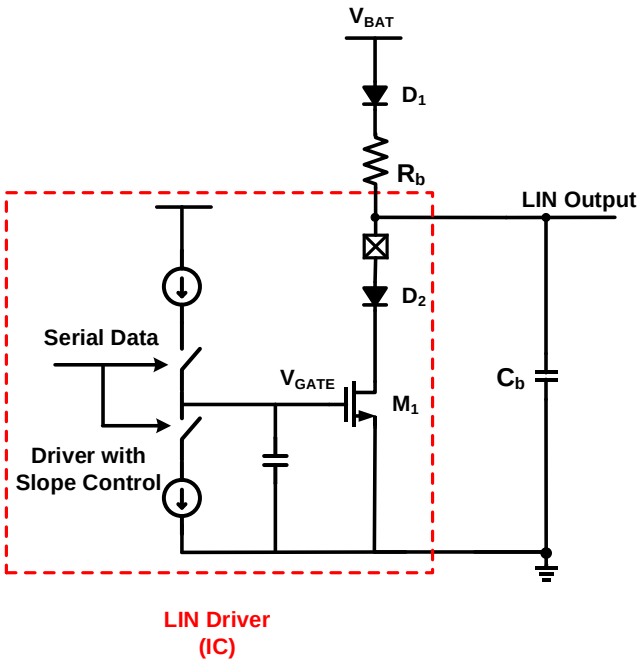



Figure 2.5: LIN Driver with Slope Control.

### 2.3. LIN Driver with an EMI Measurement Network

To ensure error-free data transmission, the duty cycle of the signal on the LIN bus should not be corrupted by EMI [3]. Undesirable EMI coupled on to the LIN bus can result in a logic change at the LIN output, leading to an error in serial communication. Thus, EMI filtering for the LIN bus is highly recommended and should be done to mitigate any EMI issues (from or into the transceiver) as well as help with transient pulses and ESD strikes. In addition to the LIN messages themselves radiating noise with rising and falling edges as well as asymmetrical waveforms, noise from the rest of the vehicle can penetrate the LIN bus. This can be done through cabling, the ground, or the battery line itself. The battery line is very noisy as it is connected to every other system in the vehicle. The minimum bus filtering consists of a shunt capacitor at the master/commander and each slave/responder node. Careful consideration must be taken as to not overload the capacitance on the bus, as this slows down the edges too much and corrupts the information on the bus. Other methods used are inductors in line with the bus, ferrite beads, and inductor-capacitor-inductor T-filters. This creates an LC filter along the bus, which is a suitable low-cost EMI suppression technique. Thus, the electromagnetic emissions are measured at the EMI node through the emissions measurements network as shown in Fig. 2.4 [4]. The emissions measurement network is basically a high pass filter implemented off chip to capture high frequency spectral components at the LIN output. To ensure electromagnetic compatibility (EMC), the LIN specification defines a limit on the power spectrum measured at the EMI node [3],[5].

## 2.4. LIN Driver with Slope Control

Additionally, fast logic changes at the LIN output may cause the LIN driver to radiate EMI that can affect other sensitive circuits. To improve the electromagnetic compatibility (EMC) of the LIN system, the LIN specification states that the signal which is placed on the LIN bus should have a small slope to reduce the fast-switching transients and their corresponding high frequency spectral components which contaminate the electromagnetic environment and possibly perturb the correct operation of neighboring circuits. This slope time (usually 5 us) must further be independent of the load of the bus and of the battery voltage (ranging between 8 V and 24 V). A LIN driver which provides an output signal with a constant slope is depicted in Fig. 2.5. Two current sources are intermediately switched on and off based on LIN input data to be transmitted, hereby charging a fixed

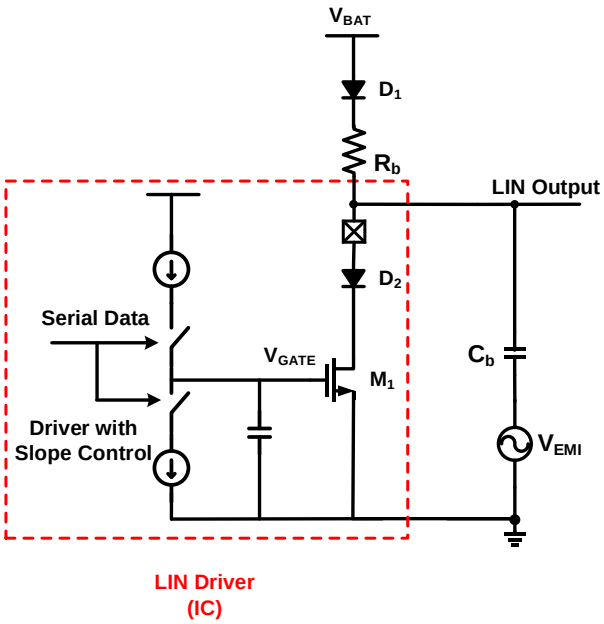



Figure 2.6: LIN Driver with EMI Source.

capacitor connected at the gate of the LIN driver. A constant current flowing in a capacitor connected at the gate of the LIN driver results in a LIN output which has well defined and controlled slope. This in turn ensures that no high frequency spectral content appears at the LIN output or at the EMI node. Moreover, the LIN driver with a slope control also ensures that it is not a source of radiated EMI.

### 2.5. Conducted EMI in LIN Driver

This circuit as shown in Fig. 2.5 performs fine if it is not influenced by external EMI disturbance. If a disturbance is present on the LIN bus (modeled by voltage source coupling into the LIN bus through bus capacitance) as shown in Fig 2.6, it may reach the gate of $M_1$ through, hereby corrupting the duty cycle of the signal on the LIN bus. The simulation results as shown in Fig. 2.7 depict the LIN serial data, LIN output and the EMI node without any EMI disturbance. The amplitude of the EMI disturbance strongly affects the duty cycle of the LIN output signal. This may result in miscommunication within the LIN transceiver system. The EMI disturbance as shown here can also be an on-chip phenomenon generated by DC-DC switching converters sharing the same substrate with the LIN driver. The LIN driver as shown in Fig. 2.6 is prone to EMI disturbances coupling to the LIN output either through the LIN bus or through a common substrate in a die/chip.

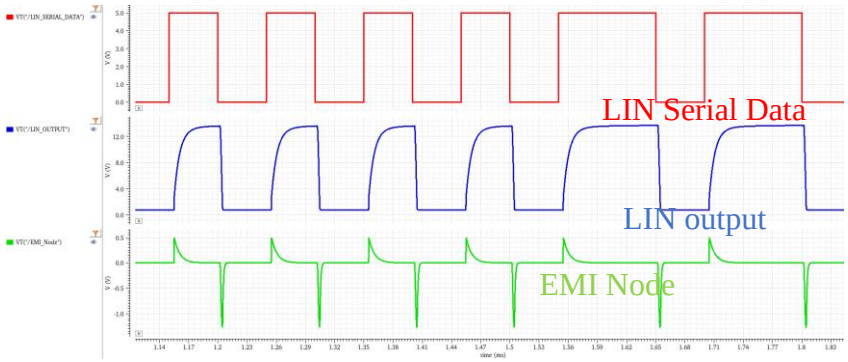



Figure 2.7: Simulation Results – LIN Serial Data, LIN Output and EMI Node.

# CHAPTER 3

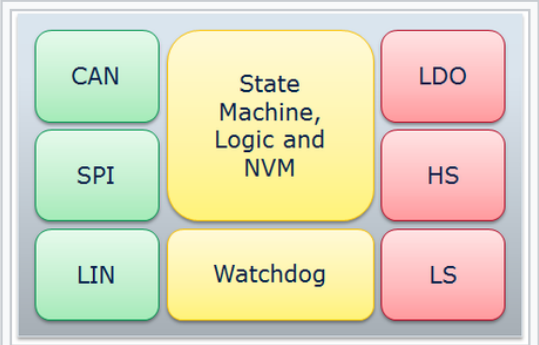
# LIN DRIVER IN SYSTEM BASIS CHIP

## 3.1. System Basis Chip (SBC)

A system basis chip (SBC) is an integrated circuit that includes various functions of automotive electronic control units (ECU) on a single die. SBC offer high integration and high performance at an optimized system cost for various automotive applications – Body Control Modules, Gateways, Closure Modules (door, roof, tailgater, trailer), Seat Control Modules, Gear Shifter, Light Control Modules etc. In general, SBCs are integrated circuits that integrate Controller Area Network (CAN) or Local Interconnect Network (LIN) transceivers with either a low-dropout regulator (LDO), a DC/DC converter or both. Fig. 3.1 shows the block diagram of a typical SBC that includes [6]:

1. Voltage Regulators
2. Supervision functions
3. Reset generators.
4. Watchdog functions
5. **Bus Interfaces – LIN and CAN**
6. **Power Switches**

In general, SBCs are aimed to function in harsh automotive electromagnetic environments and are subjected to strong levels of EMI. Apart from external EMI sources, SBCs can also suffer from radiated and conducted EMI from its on-chip circuits and systems. Conducted EMI coupling through substrate capacitance from DC-DC switching




Example partitioning of a system basis chip with bus interfaces (green), central logic (yellow), and outputs (red) for voltage regulators (LDO), high-side, and low-side switches (HS, LS)

Figure 3.1: A System Basis Chip.

regulator onto the LIN driver output in the same SBC can make the LIN driver noncompliant to EMC requirements. SBCs implemented on expensive SOI technology nodes are inherently known to withstand high-interference levels of conducted EMI through the common substrate on the same chip [7],[8]. However, economical, power friendly BCD processes have low-resistivity silicon substrate and are unable to shield noise sensitive circuits like LIN drivers from EMI disturbances coupling through the substrate [9]-[11]. Hence, SBCs implemented on inexpensive BCD processes fail to comply with the EMC requirements as per the LIN specification due to the DC-DC switching regulator on the same chip. BCD is a family of silicon processes, each of which combines the strengths of three different process technologies onto a single chip: Bipolar for precise analog functions, CMOS (Complementary Metal Oxide Semiconductor) for digital design and

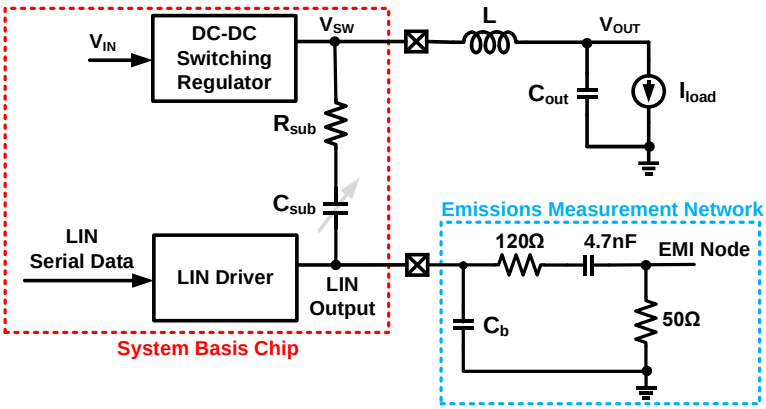



Figure 3.2: Typical LIN driver and DC-DC Switching Regulator in a System Basis Chip and Its Representative Parasitic Substrate Coupling Mechanism.

DMOS (Double Diffused Metal Oxide Semiconductor) for power and high-voltage elements [12]. SBCs implemented in non-SOI BCD processes consists of only LDOs as power converters rather than DC-DC switching regulators [13], [14].

### 3.2. LIN Driver with DC_DC Switching Regulator

In SBCs, the LIN driver and switching DC-DC regulator share the same substrate. Fig. 3.2 shows a simplified switching noise coupling model for a switching regulator and LIN driver in a typical SBC. The model depicts the distributed parasitic substrate resistance ($R_{sub}$) and capacitance ($C_{sub}$) between the switching node ($V_{SW}$) of the DC-DC switching regulator and the LIN driver output. A cross sectional view of the LIN driver and switching regulator sharing a common substrate in a typical BCD process is shown in Fig. 3.3. The parasitic noise coupling path from $V_{SW}$ to the LIN driver output (N+ drain, on shallow N well) through the parasitic substrate Rsub and Csub is also shown in Fig. 3.3.

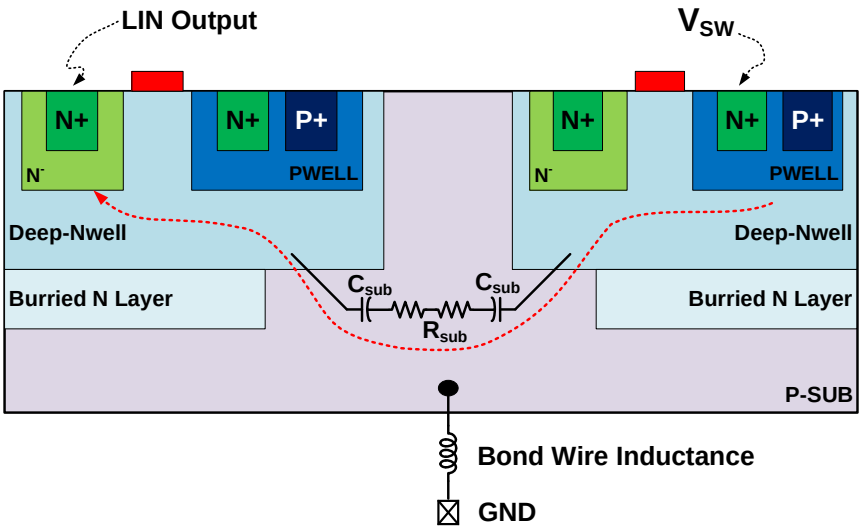



Figure 3.3: Cross Sectional View Depicting LIN Driver and DC-DC Switching Regulator Sharing the Same Substrate in a Bi-CMOS Process.

The power spectra at the EMI node with the emissions mask limit are shown in Fig. 3.4 and Fig. 3.5. When the switching DC-DC regulator is turned OFF, no tonal content of the switching frequency and its harmonics are observed in the power spectrum as shown in Fig. 3.4 and the EMC requirements at EMI node are not violated. When the switching DC-DC regulator is turned ON, the total content of the switching frequency (2MHz) and its harmonics are observed in the power spectrum as shown in Fig. 3.5. In general, automotive PMICs/SBCs commonly use the switching frequency of 2 MHz due to automotive EMI band requirements thereby ensuring no AM radio band (530 kHz to 1.8 MHz) interference. The conducted emissions at the EMI node significantly violates the mask limit by 20 dB. The primary source of this spurious emission is coupling from the switching node ($V_{SW}$) of the DC-DC regulator through substrate parasitic passives such as $R_{sub}$ and $C_{sub}$. The switching activity at $V_{SW}$ leads to conduction of switching noise to LIN

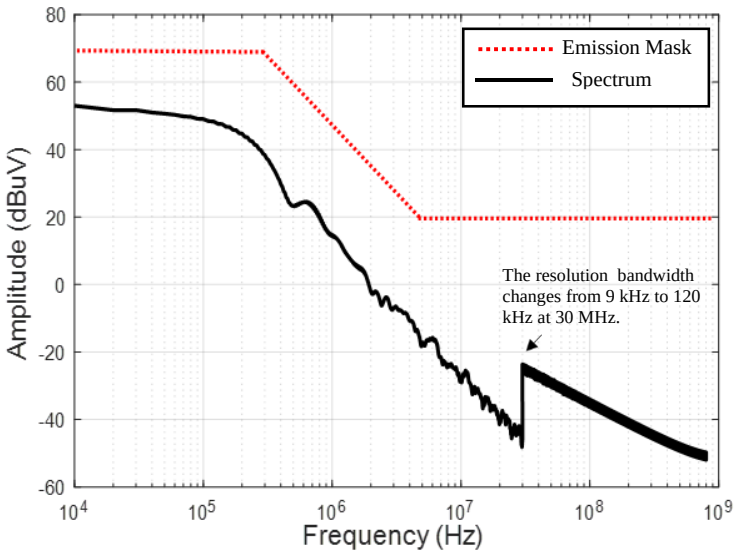



Figure 3.4: Spectrum at the EMI Node with the DC-DC Switching Regulator OFF.

output through $C_{sub}$ and $R_{sub}$. As shown in the cross-sectional view (Fig. 3.3), owing to the bond wire inductance, the switching noise travels through the low-resistivity substrate and capacitively couples to the output of the LIN driver, instead of being shunted to ground.

### 3.3. LIN Output States and Switching Noise

There are two main logic levels for the LIN driver output that we would consider, a Logic '0' state and '1' state.

*1) LIN Output = Logic '0':* With reference to the circuit in Fig. 2.4, $V_{GATE}$ goes high to transmit a logic '0' on the LIN output. $M_1$ is thus turned ON in the triode region, thereby setting the LIN output to a voltage of $V_{D2}$. $M_1$ is appropriately sized to sink a maximum current of 40mA as per the LIN specification. The low ON resistance of $M_1$ attenuates the ripple injected from $V_{SW}$ to the LIN output when the LIN output is logic '0'. As a result,

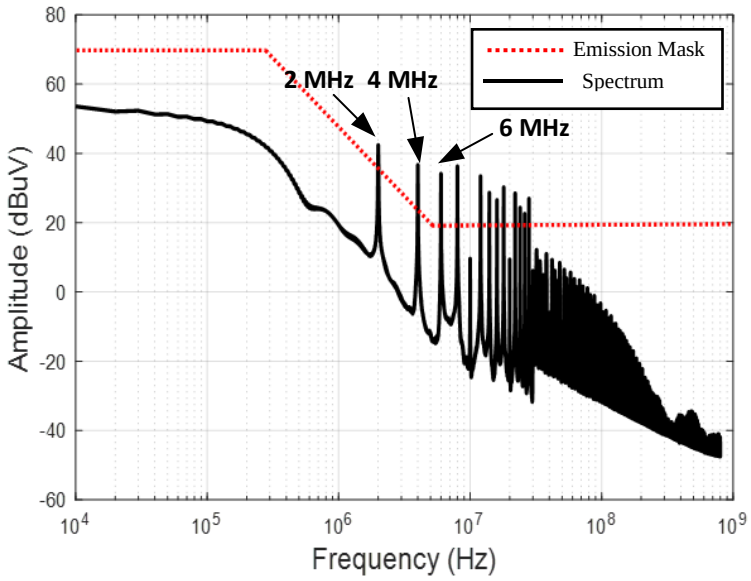



Figure 3.5: Spectrum at the EMI Node with the DC-DC Switching Regulator ON.

conducted EMI is less severe for the LIN driver when the output is logic '0'. It is observed that for logic '0', the ripple on the LIN output is attenuated when the switching DC-DC regulator is turned ON as per the simulation results shown in Fig. 3.6.

*2) LIN Output = Logic '1':* With reference to the circuit in Fig 2.4, $V_{GATE}$ goes low to transmit a logic '1' on the LIN output. $M_1$ is thus turned OFF, thereby setting the LIN output to a voltage of ($V_{BAT}$ - $V_{D1}$). As $M_1$ is turned OFF when the LIN output is logic '1', ripple is directly injected from the DC-DC regulator switching node, $V_{SW}$ to the LIN output. As a result, conducted EMI becomes critical for the LIN driver when the output is logic '1'. As shown in Fig 3.6, it is observed that for logic '1', the switching noise is directly

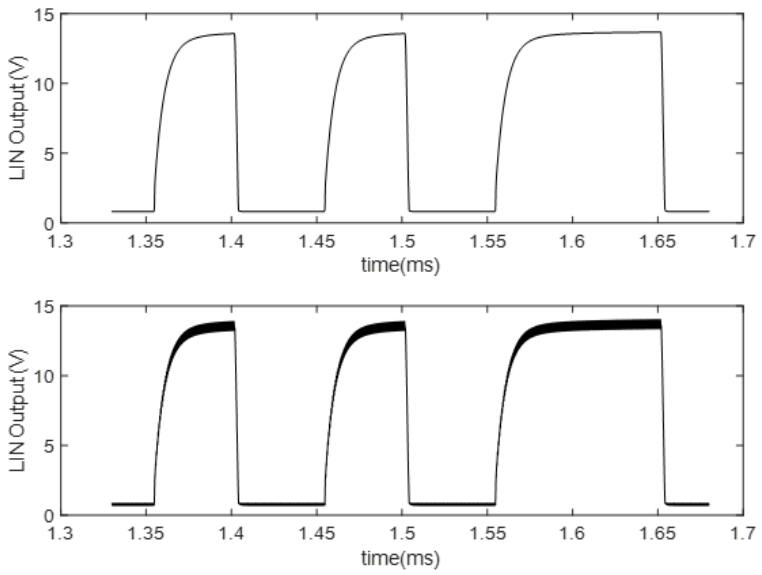



Figure 3.6: LIN Output with DC-DC Switching Regulator ON and OFF Respectively.

injected onto the LIN output without any attenuation when the DC-DC switching regulator is turned ON.

As shown in Fig. 3.7, the ripple observed at the LIN output is synchronized with the switching node $V_{SW}$. The rising and the falling edge of $V_{SW}$ results in a positive and negative ripple respectively at LIN output. The ripple magnitude coupled onto the LIN output from $V_{SW}$ primarily depends on the amplitude of $V_{SW}$ and the coupling substrate capacitance ($C_{SUB}$). The ripple coupled through $C_{SUB}$ at the LIN output also depends on the rise-fall time of $V_{SW}$. The amplitude of the spurs observed in Fig. 3.5 is directly proportional to the ripple magnitude.

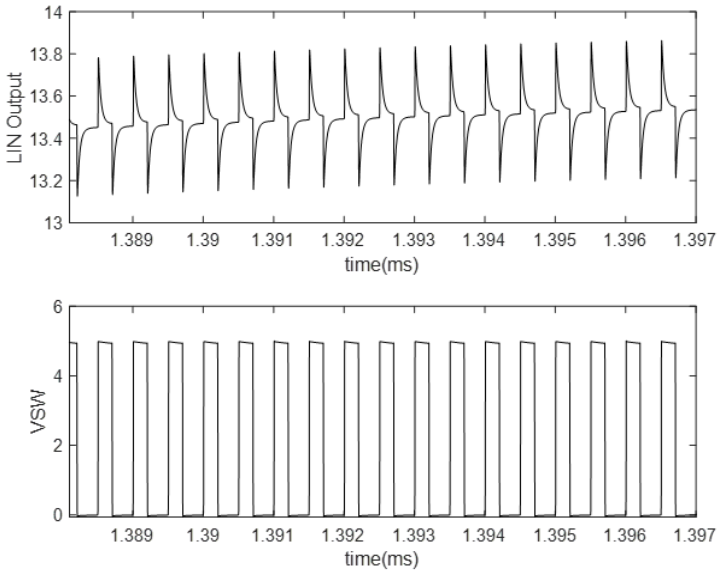



Figure 3.7: Ripple at the LIN Output Aligned with the Switching Node.

### 3.4. EMI Reduction Techniques and Limitations

As described in [15], a LIN driver with a slope-controlled output does not radiate EMI, however it is prone to conducted EMI injected onto the LIN bus. LIN driver architectures resistant to conducted EMI have been explored in [4],[16] - [20], where the conducted EMI is modeled by coupling the EMI disturbance onto the LIN bus through the bus capacitance. But these architectures do not address the issue of substrate coupling. Parasitic capacitance cancellation techniques for EMI suppression using mutual capacitance and mutual inductance have been described in [21]. Mitigation schemes for increased EMI caused by RF substrate coupling in automotive integrated circuits has been discussed in [22],[23]. Passive methods such as an increased physical distance between victim and aggressor circuits, better layout techniques such as placing more guard rings have been explored to reduce conducted EMI. However, passive techniques do not always

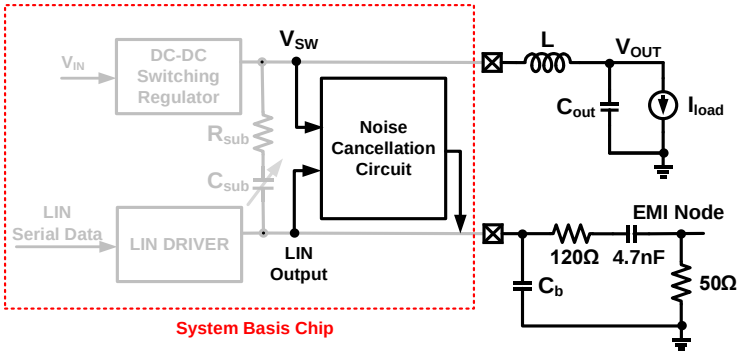



Figure 3.8: A System Basis Chip with the Proposed Active EMI Cancellation Circuit.

lead to a sufficiently reduced parasitic substrate coupling [11]. Some generic ripple and spur cancellation techniques have been discussed in [24],[25] but those are not suitable for this application.

### 3.5. Research Motivation

The primary solution to reduce the coupled EMI from $V_{SW}$ to LIN output is to minimize $C_{SUB}$. The intrinsic parasitic substrate capacitance in a BCD process depends on the process and varies from die to die. The noise injected can be minimized by reducing the $V_{IN}$ of the DC-DC switching regulator, however $V_{IN}$ is primarily defined by the SBC application.

The noise coupled to the output of the LIN driver is proportional to $C_{SUB}$ x (dV/dt), where dV/dt denotes the slew rate of $V_{SW}$. So, the coupled noise can also be reduced by decreasing the driver strength driving the power FETs of the switching DC- DC regulator. This reduces the slew rate of $V_{SW}$ thereby lowering the injected noise on the LIN output. However, this results in a direct trade off with efficiency of the DC-DC switching regulator as the switching losses are proportional to the turn ON/OFF time of the power FETs.

To meet the emission requirements of conducted EMI as per the LIN specification, a cancellation circuit integrated on the SBC that actively cancels the noise from the LIN output is required, as shown in Fig. 3.8. The amplitude of the spurs observed in Fig. 3.5 has to be attenuated by at least 20 dB to satisfy the mask requirements. This serves as the motivation for this research to develop and design an area and power efficient active EMI cancellation circuit to reduce emissions from the LIN output.

# CHAPTER 4

# PROPOSED EMI CANCELLATION CIRCUIT

## 4.1. Theoretical Analysis of Active EMI Cancellation

The coupling from the switching node through $C_{SUB}$ generates noise ripple at the LIN output, as shown in Fig. 4.1. The fundamental idea of the proposed EMI cancellation scheme is to generate a switching node ($V_{SW}$) synchronized cancellation pulse ($V_{CP}$) and inject it at the LIN output through a cancellation capacitance ($C_{CAN}$) as shown in Fig. 4.2, with a closed loop control. The extent of ripple cancellation is dependent on the duty cycle and the phase difference of $V_{CP}$ w.r.t $V_{SW}$ as evident in Fig. 4.2. The degree of noise cancellation also depends on the matching of the capacitances $C_{CAN}$ with $C_{SUB}$. In the proposed system, the EMI cancellation loop tracks the ripple on the LIN output and modulates the rise and fall time of $V_{CP}$. Moreover, the value of $C_{CAN}$ is also optimized by the cancellation loop so that it matches with actual $C_{SUB}$. The simultaneous dual control of the rise/fall time of $V_{CP}$ and $C_{CAN}$ has been explained with a flowchart, as depicted in Fig. 4.3. As described in the flowchart, the integrated value of the sensed ripple is compared with the target value (ideally zero) until the steady state is reached. The slew counter is incremented by 1 till the slew count is maximum. Next the $C_{CAN}$ is incremented by 1 LSB and the slew counter is reset. Noise cancellation is achieved by comparing the integrated value of the ripple with its previous sample iteratively and minimizing that with the cancellation loop. As shown in Fig. 3.8, the noise cancellation block takes LIN output and $V_{SW}$ as inputs and synthesizes $V_{CP}$ and $C_{CAN}$.

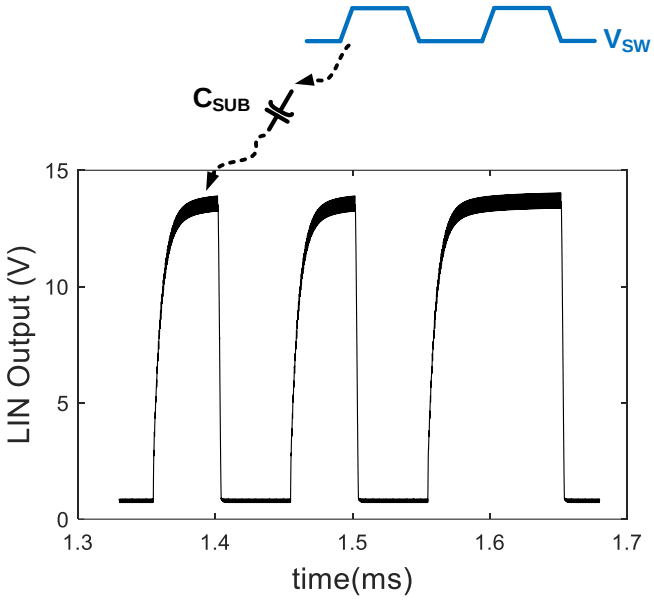



Figure 4.1: LIN Output with the Ripple.

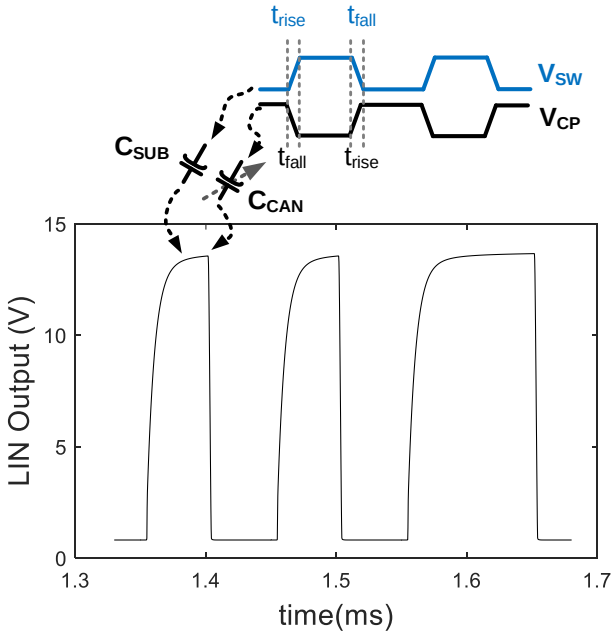



Figure 4.2: LIN Output with Capacitive Ripple Cancellation.

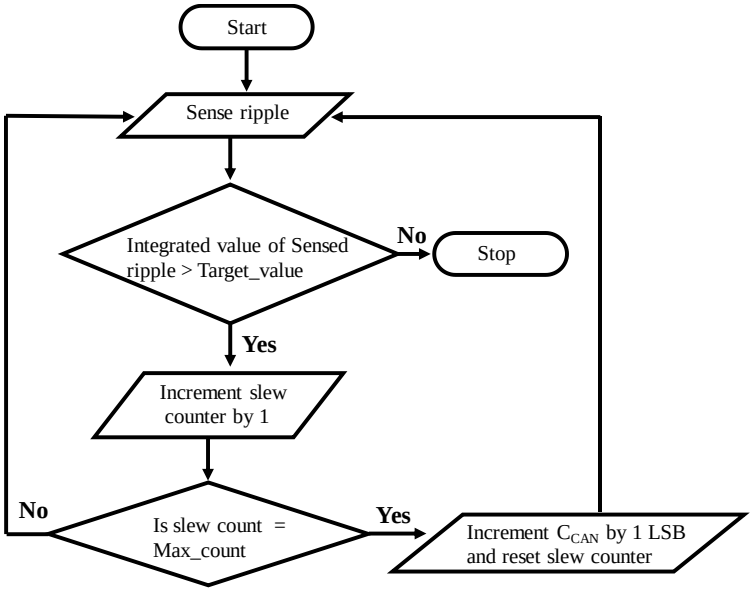



Figure 4.3: Flowchart of the Ripple Cancellation Scheme.

### 4.2. Architectural Analysis of EMI Cancellation Loop

The proposed noise cancellation architecture at the system level is shown in Fig. 4.4. The cancellation loop tracks the ripple at the LIN output using a high pass filter (HPF), positive and negative ripple processing blocks. The inverse cancellation pulse is generated by an edge alignment block while its ($V_{CP}$) rise and fall time is modulated by a slew-controlled buffer. In the slew-controlled buffer, the currents controlling the rise and fall time of the cancellation pulse are digitally tuned by the positive and negative ripple processing blocks. A digitally modulated binary capacitor bank array is used to generate $C_{CAN}$, through which $V_{CP}$ is injected at the LIN output.

A passive HPF filters the ripple on the LIN output and superimposes the ripple on a common mode voltage ($V_{CM}$ = 2.5V). The filter R (= 50 kΩ) and C (= 2 pF) are designed to set its cutoff frequency to approximately 1.5 MHz. This ensures that the ripple content

at switching frequency (2 MHz) passes through the HPF while the low frequency LIN data is filtered out. The cut-off frequency of the HPF should be set w.r.t the minimum switching frequency to make this noise cancellation scheme compatible with a wide range of switching frequencies, requiring more die area.

However, while communicating serial data the passive HPF may pass the LIN transitions leading to erroneous ripple information. Thus, a blanking clock derived from the LIN serial data is used to mask the LIN transitions. The blanking time has to be adjusted w.r.t the cut off frequency of the HPF – a higher blanking time might be required to filter out LIN transitions with a lower cut off frequency of the HPF. The blanking clock is also used to mask the ripple when the LIN output is logic ‘0’, since during this time the noise coupling is insignificant as explained in section II (C). In summary, the cancellation loop processes the ripple information only when the LIN output is logic ‘1’.

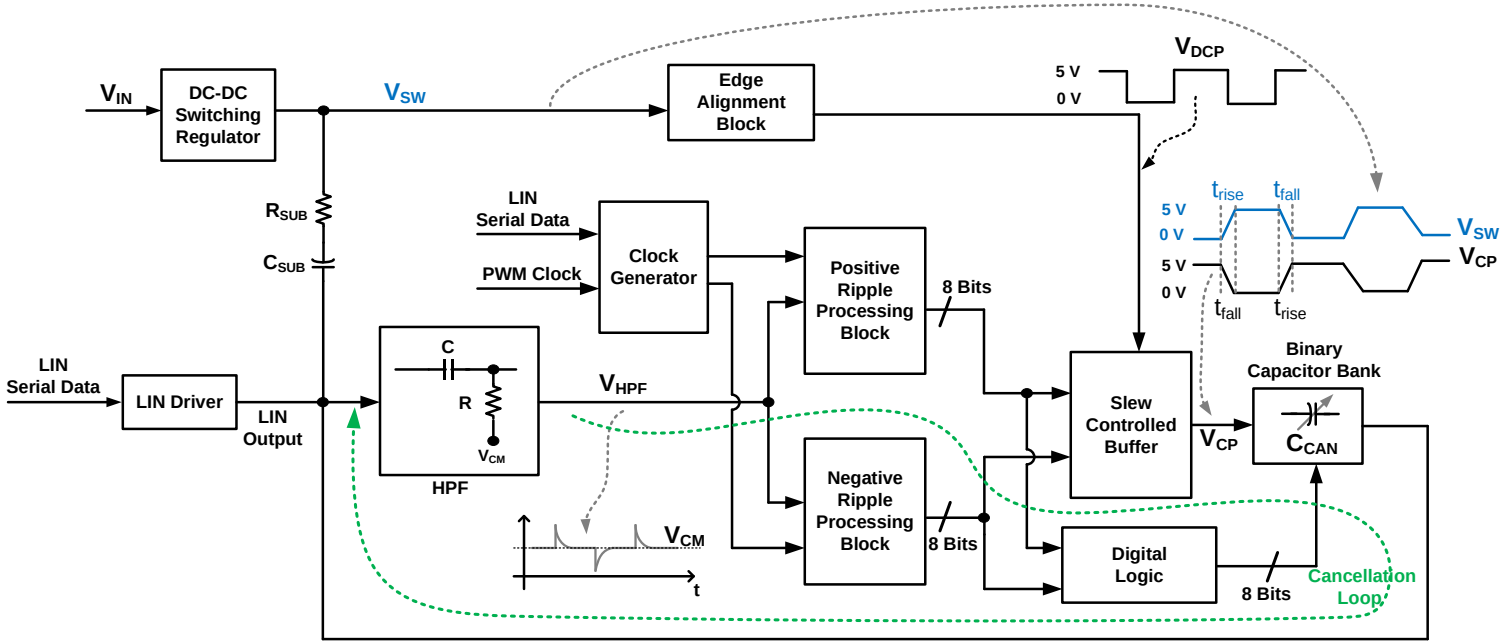



Figure 4.4: Proposed Active LIN Driver EMI Sensing and Cancellation Circuit.

### 4.3. Positive and Negative Ripple Processing Blocks

The ripple processing blocks are shown in Fig. 4.5 and consist of a unity gain buffer, an active RC integrator, a clocked comparator, and an 8-bit digital counter to process the ripple on the LIN output. The ripple information, after high pass filtering and blanking is extracted and computed by the ripple processing blocks. The rising edge of $V_{SW}$ generates positive ripple and is processed by the positive ripple processing block. Similarly, the falling edge of $V_{SW}$ generates negative ripple and is processed by the negative ripple processing block. Also, asymmetrical rise and fall time of $V_{SW}$ may result in different positive and negative ripple content on the LIN output. Thus, both positive and negative ripple processing blocks are required to process the ripple. The 8-bit digital output of the ripple processing blocks control currents in a slew-controlled buffer as shown in Fig. 4.4.

*1) Clock Generator:* A clock generator as shown in Fig. 4.6 is designed to generate the various clocks required by the ripple processing blocks. The clock generator takes the LIN serial data and the PWM clock as inputs and generates the clocks for integrators, comparators, and the digital counters. The integrating clocks ($\Phi_{INT\_P}$, $\Phi_{INT\_N}$), derived from the PWM clock are used to capture the ripple information. The reset clocks ($\Phi_{RES\_P}$, $\Phi_{RES\_N}$) goes high after 10 cycles of the integrating clocks and are derived from the PWM clock with a divide-by-10 counter. The comparator clocks ($\Phi_{COMP\_P,}$ $\Phi_{COMP\_N}$) are also derived from the PWM clock. The comparator clock goes high after 10 cycles of integrating clock just before the reset clock. The counter clocks ($\Phi_{COUNT\_P,}$ $\Phi_{COUNT\_N}$) are delayed w.r.t the comparator clocks and triggers once the comparator outputs are sampled. The clock

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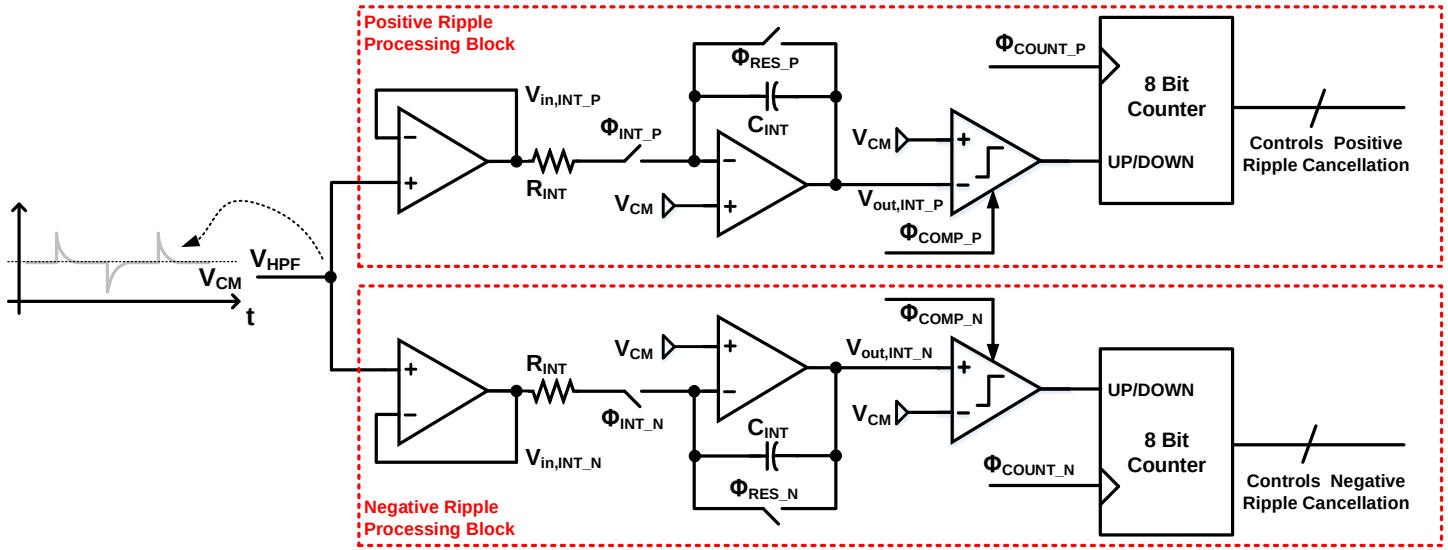


Figure 4.5: Positive and Negative Ripple Sensing and Processing Blocks.

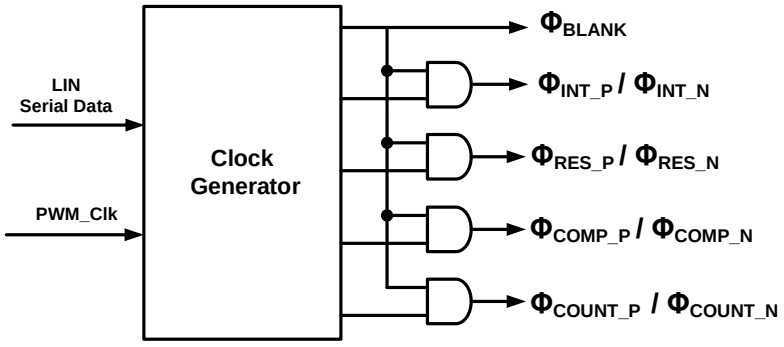


Figure 4.6: Clock Generator Within the Cancellation Circuit.

generator also generates a blanking clock phase ($\Phi_{BLANK}$) from the LIN serial data. The blanking clock is AND-ed with other clocks as shown in Fig. 4.6 to ensure that the signal processing block does not process the ripple when the LIN output is making transitions and when the LIN output is at logic '0'.

*2) Unity Gain Buffer:* As shown in Fig. 4.5, the ripple from the output of the HPF is fed to two unity gain buffers. The unity gain buffers provide isolation required for processing the positive and negative ripple separately. As shown in Fig. 4.7, they are designed with folded cascode operational transconductance amplifier (OTA) having an open loop gain of 70 dB and UGF of 50 MHz, to replicate the ripple at the inputs of the integrators. The OTA is designed with an offset correction block to trim out the input referred offset to account for any shift in the common mode voltage of the ripple. A 7-bit binary current DAC with an LSB current of 31.25 nA is used for offset correction as shown in Fig. 4.7. A differential current is injected into the drain of the input pair to correct the offset. The unity gain buffers are designed to have low output impedance to drive the active RC integrators.

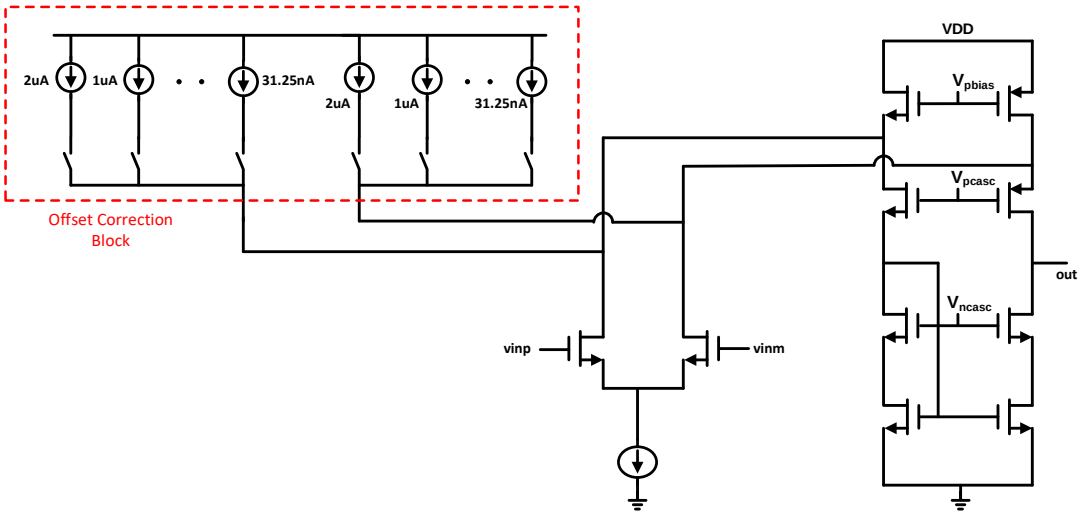


Figure 4.7: Folded Cascode OTA with Offset Correction Block.

As depicted in Fig. 4.8, an auto calibration circuit is used for offset correction of the unity gain buffers. The auto calibration consists of a few switches, an XOR gate, a D flip flop and a 7-bit counter. A slow clock derived from the PWM clock of the system is used in this calibration circuit. During calibration, the OTA is in comparator mode with the inputs connected to a common mode voltage (vcm = 2.5V) as shown in Fig. 4.8. With every clock edge, the 7-bit counter increments the offset correction code by 1. The digital logic comprising of the D flip flop and the XOR gate captures any transition of the OTA output from high to low or vice versa. As the transition is detected, the offset code is written onto the binary current DAC shown in Fig. 4.7. Simultaneously, the inputs of the OTA are disconnected from vcm and connected to their respective inputs. This auto calibration circuit can also be used to correct any temperature coefficient of the offset by taking the OTA offline at the expense of longer settling time of the noise cancellation loop.

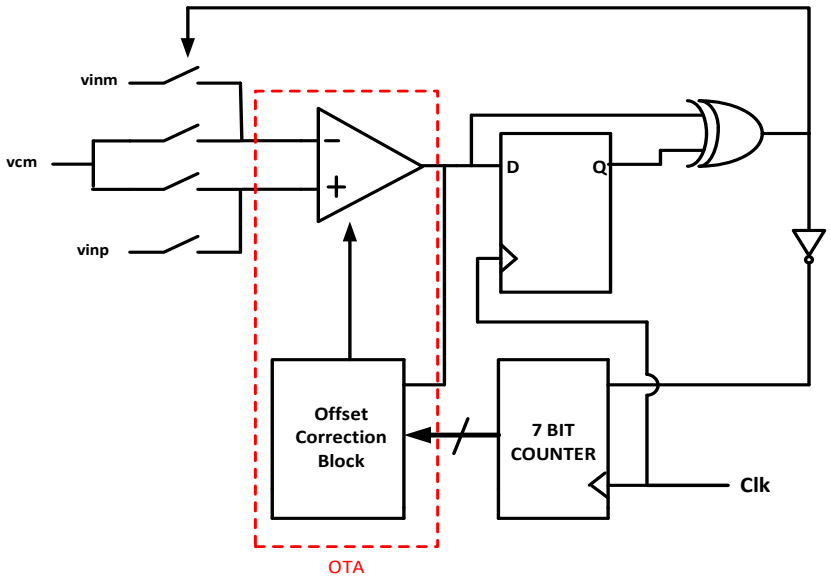


Figure 4.8: Auto Calibration Scheme for the OTA.

*3) Active RC integrators:* The active RC integrators as shown in Fig. 4.5 are designed with folded cascode OTAs having an open loop gain of 70 dB and UGF of 50 MHz, which is well beyond the UGF (8 MHz) of the integrator. The transfer function of the active RC integrator while the integrating clocks ($\Phi_{INT\_P}$, $\Phi_{INT\_N}$) are ON and reset clocks ($\Phi_{RES\_P}$, $\Phi_{RES\_N}$) are OFF is given by:

$$\frac{V_{out}}{V_{in}} = \frac{1}{sR_{INT}C_{INT}+1/A(s)} \qquad (1)$$

$$A(s) = A_0/(1 + s/w_p) \qquad (2)$$

where *A(s)* is the open loop response of the OTA. The OTA has a DC gain of $A_0$ and a 3-dB bandwidth of $w_p$. The unity gain frequency ($f_{UGB}$) of the integrator is:

$$f_{UGB} = \frac{1}{2 \times \pi \times R_{INT} \times C_{INT}} \qquad (3)$$

The DC gain of the integrator is limited by the DC gain of the OTA to be around 70 dB. The integrator R ($R_{INT}$) and C ($C_{INT}$) values are chosen to set the $f_{UGB}$ of the integrator to 8 MHz. The $f_{UGB}$ (8 MHz) is chosen to capture sufficient ripple content at the switching frequency (2 MHz) and its harmonics. Increasing $f_{UGB}$ helps to capture more ripple content however, the higher sensitivity may lead to saturation of the integrator output.

The waveforms showing positive ripple ($V_{in,INT\_P}$), the integrating clock ($\Phi_{INT\_P}$), the reset clock ($\Phi_{RES\_P}$) and the positive integrator output ($V_{out,INT\_P}$) are shown in Fig. 4.9. Similarly, the waveforms showing negative ripple ($V_{in,INT\_N}$), the integrating clock ($\Phi_{INT\_N}$), the reset clock ($\Phi_{RES\_N}$) and the negative integrator output ($V_{out,INT\_N}$) are shown in Fig. 4.10. The positive and negative ripple is integrated for 10 cycles of integrating clocks.

When the integrating clocks are ON, the ripple is integrated over the common mode voltage $V_{CM}$ for 10 clock cycles. This is depicted in the integrator outputs ($V_{in,INT\_P}$, $V_{out,INT\_N}$) as shown in Fig. 4.9 and Fig. 4.10 respectively. For the positive ripple the integrated noise is subtracted from $V_{CM}$ whereas for the negative ripple the integrated noise is added to $V_{CM}$. After 10 cycles of integration, the reset clock resets the integrator output to $V_{CM}$.

As the noise cancellation loop relies on reverse injection of cancellation pulse, the integrated value of ripple reduces after every 10 cycles. As shown in Fig 4.9 and Fig 4.10, the integrated value of the ripple at point A/C is less as compared to point B/D. The noise cancellation loop reaches a steady state when the differential input to the active RC integrators is less than the input referred offset of the OTA.

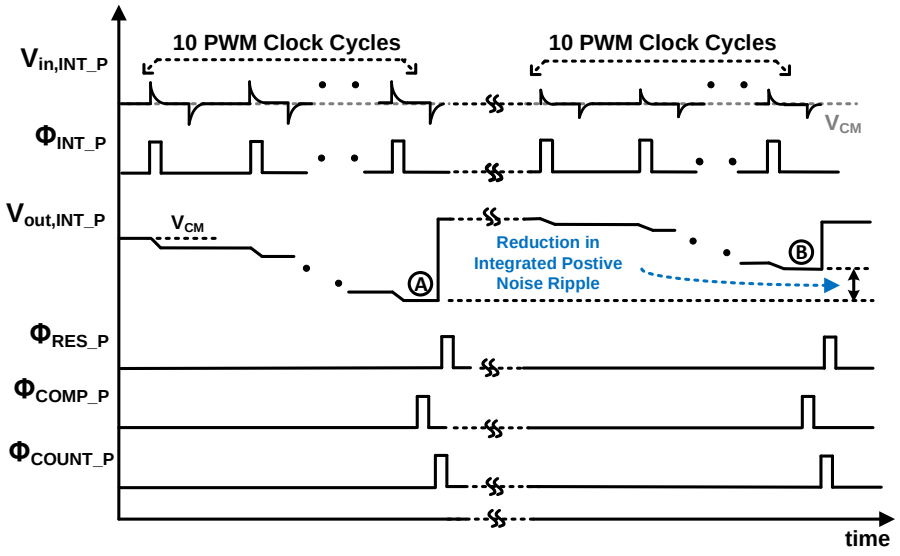


Figure 4.9: Signal Waveforms w.r.t the Positive Ripple Processing Block

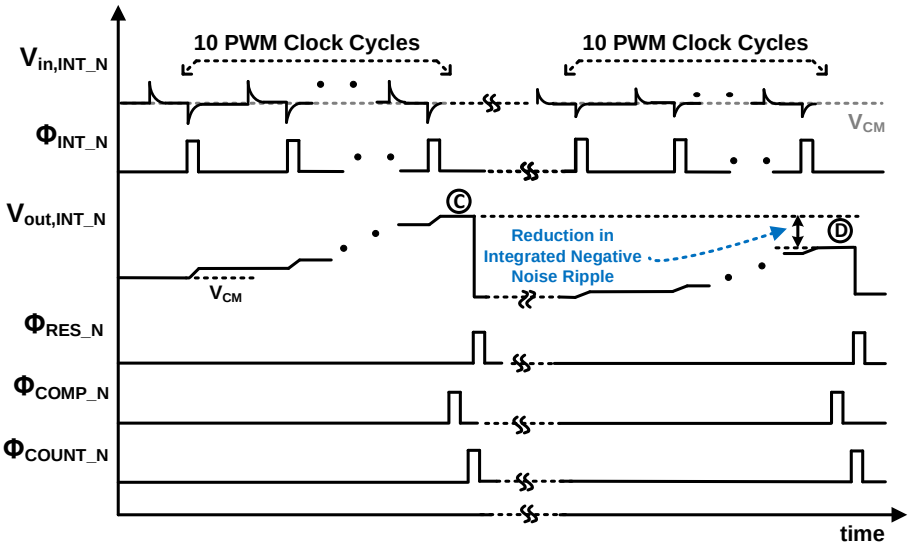


Figure 4.10: Signal Waveforms w.r.t the Negative Ripple Processing Block.

The input offset of the integrator is critical for the integration of the ripple. Unintentional offset at the integrator input may be considered as ripple information leading to the saturation of the integrator output. The auto calibration scheme as shown in Fig. 4.8, is also used to calibrate out any unintentional offset at the integrator inputs. The number of integration cycles is designed to be 10 for optimum processing of noise information. A higher number of integration cycles may lead to the saturation of the integrator outputs and increased settling time for the loop. A lower number of integration cycles may lead to lesser ripple information thus requiring high precision and fast comparators.

*4) Comparators:* The clocked comparators in the ripple processing block are implemented using an OTA in open loop configuration followed by a D Flip Flop (FF). The D FFs are clocked with the comparator clocks ($\Phi_{COMP\_P,}$ $\Phi_{COMP\_N}$). The comparators compare the integrated value of the ripple after 10 integration cycles with the common mode voltage ($V_{CM}$). The timing waveforms of the comparator clocks w.r.t the integration of ripple is shown in Fig. 4.9 and Fig. 4.10. Before the integrator output is reset to $V_{CM}$, the comparator output is sampled by the comparator clock. The frequency of the comparator clock is set to 0.2 MHz as the comparator makes a decision after 10 cycle of ripple integration. The comparator is designed for low input referred offset.

The input polarities of the clocked comparators in the positive and negative ripple processing blocks are opposite. Thus, in the positive ripple processing block, the comparator output remains high if the integrated value of the ripple is lower than $V_{CM}$. However, in the negative ripple processing block, the comparator output remains high if the integrated value of the ripple is higher than $V_{CM}$. The comparator output toggles

between high and low as the noise cancellation loop reaches steady state.

*5) Counters:* The outputs of the comparators drive two 8-bit digital counters as shown in Fig. 4.5. A comparator output of high/low results in an UP count/DOWN count respectively for the counter. As shown in Fig. 4.9 and Fig. 4.10, the counter clocks ($\Phi_{COUNT\_P,}$ $\Phi_{COUNT\_N}$) are delayed w.r.t the comparator clocks and drive the counters once the comparator outputs are sampled. As shown in Fig. 4.4 and Fig. 4.5, the counters digitally control the currents in a slew-controlled buffer. As the noise cancellation loop reaches steady state, the counter settles as the comparator output toggles between high and Low.

The number of bits in the counter is chosen to be '8' based on the unit LSB current in the slew-controlled buffer to accommodate a wide range of rise-fall time of $V_{CP}$ to match $V_{SW}$.

### 4.4. Edge Alignment Circuit

The edge alignment circuit as shown in Fig. 4.11 consists of two delay locked loops (DLLs), a digital recombination logic circuit and a dummy slew-controlled buffer (identical to the primary slew-controlled buffer). This circuit takes $V_{SW}$ as input and generates an aligned digital cancellation pulse ($V_{DCP}$), which after being processed by the primary slew-controlled buffer is injected at the LIN output. The primary role of this block is to align $V_{CP}$ with $V_{SW}$ so that optimum cancellation is achieved even with timing mismatches across different duty cycles of the switching regulator. Two separate DLLs ensure alignment of rising edge of $V_{DCP}$ with the falling edge of $V_{SW}$ and vice-versa. Simulation results in Fig. 4.12 show the alignment of $V_{DCP}$ and $V_{SW}$ with a timing offset.

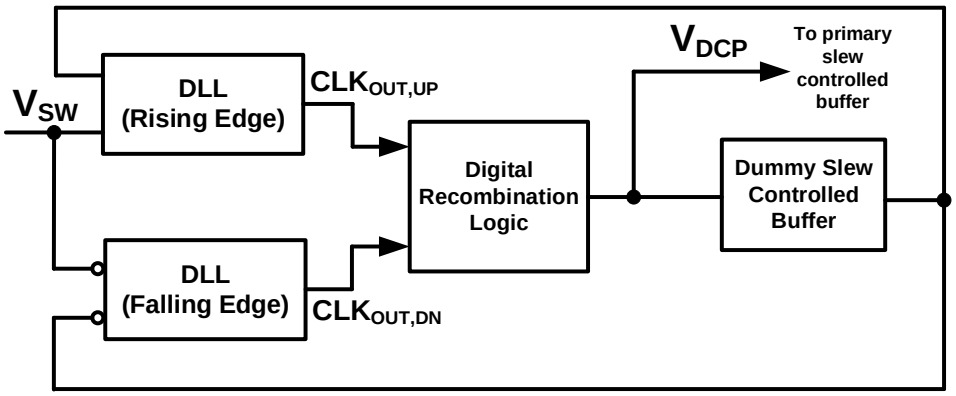


Figure 4.11: Edge Alignment Circuit.

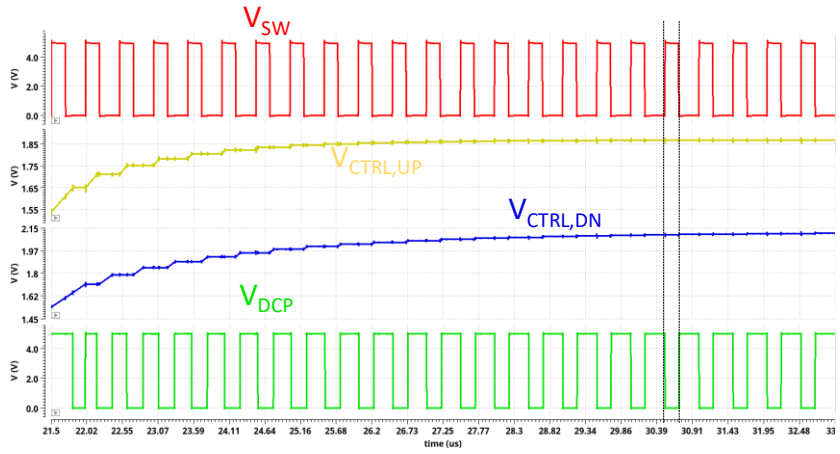


Figure 4.12: Alignment of $V_{SW}$ with $V_{DCP}$ with a Timing Offset.

This offset is due to the delay associated with the dummy slew-controlled buffer in the feedback path of this circuit, which is added to account for the delay of the primary slew-controlled buffer in the cancellation loop. The edge alignment circuit is designed to track the switching frequency and duty cycle of the DC-DC switching regulator sharing the same substrate with the LIN driver. This is because the ripple on the LIN output is fully synchronous with the switching frequency and duty cycle of the DC-DC regulator.

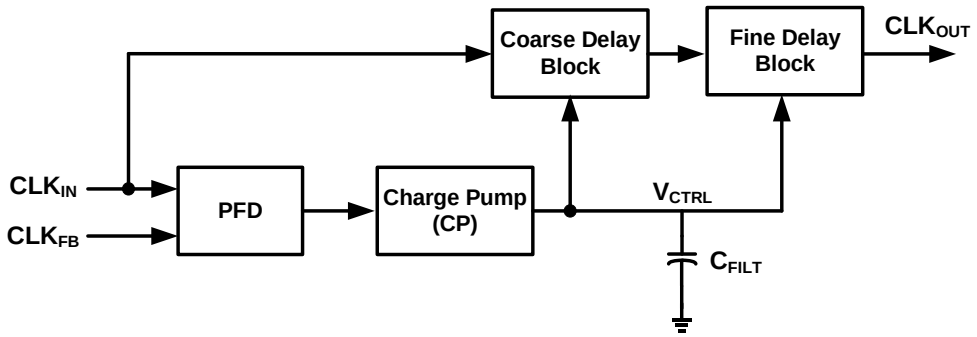


Figure 4.13: Delay Locked Loop (DLL).

The architecture of the DLL used in the edge alignment circuit is shown in Fig. 4.13 and consists of PFD, Charge Pump, Loop filter, Coarse and fine delay cells. The bandwidth of the DLL [26] is given by:

$$w_N = I_{CH}.K_{DL}.F_{REF}.\frac{1}{C_{FILT}} \qquad (4)$$

where $I_{CH}$ = charge pump current, $K_{DL}$ = VCDL gain, $F_{REF}$ = reference/input frequency, $C_{FILT}$ = loop filter capacitance.

The DLL is unconditionally stable if $w_N < F_{REF}/10$. $I_{CH}, K_{DL}$ and $C_{FILT}$ are so chosen to set the DLL bandwidth to 1/10$^{th}$ of the switching frequency (≈ 200 kHz). DLL (Rising Edge) works on the rising edge of $V_{SW}$ while DLL (Falling Edge) works on the falling edge of $V_{SW}$. The digital recombination circuit combine the outputs ($CLK_{OUT,UP}$, $CLK_{OUT,DN}$) of the two DLLs and generates $V_{DCP}$, which tracks the duty cycle of $V_{SW}$. Simulation results in Fig. 4.12 also show the settling of $V_{CTRL}$ nodes of both the DLLs as $V_{DCP}$ aligns with $V_{SW}$. The DLL has been designed to lock in a wide range of switching frequencies to

generate a frequency independent aligned cancellation pulse. Simulation results in Fig. 4.14 and Fig 4.15 show the alignment of $V_{DCP}$ and $V_{SW}$ with switching frequencies of 4 MHz and 100 kHz respectively. In general, this ensures generation of $V_{DCP}$ irrespective of switching frequency of the DC-DC converter.

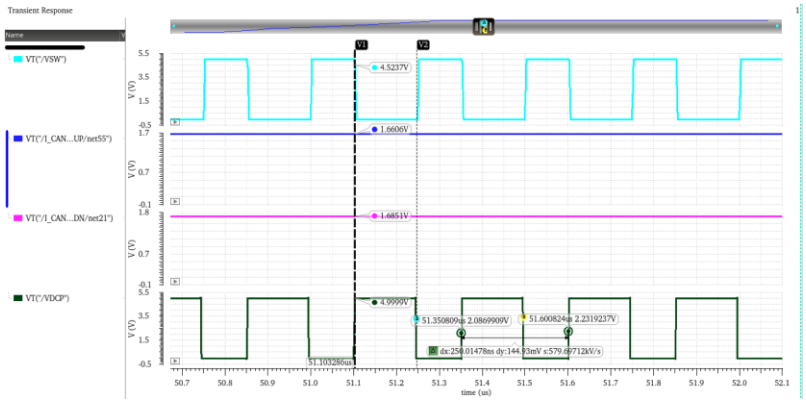


Figure 4.14: Alignment of $V_{SW}$ with $V_{DCP}$ with a Timing Offset @ $F_{SW}$ = 4 MHz

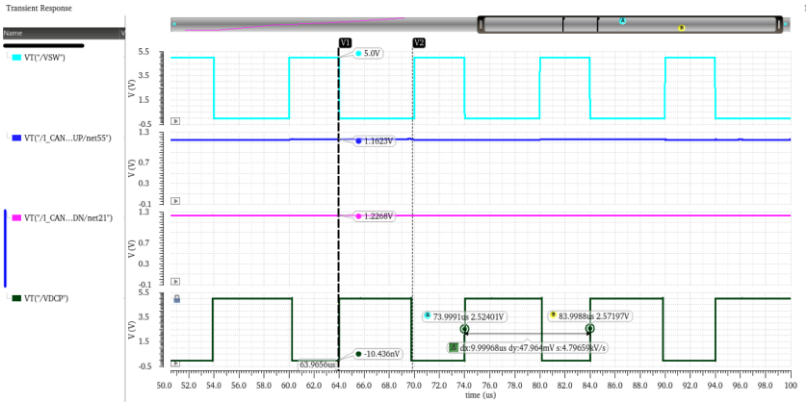


Figure 4.15: Alignment of $V_{SW}$ with $V_{DCP}$ with a Timing Offset @ $F_{SW}$ = 100 kHz.

### 4.5. Slew Controlled Buffer

The architecture of the slew-controlled buffer is shown in Fig. 4.16. The slew-controlled buffer is fed with $V_{DCP}$ from the edge alignment circuit and it generates $V_{CP}$. The rise-fall time of $V_{CP}$ is modulated by the slew-controlled buffer before injecting it at the LIN output. A current starved inverter forms the core of the slew-controlled buffer, where the charging and discharging currents are digitally controlled by the counters of positive and negative ripple processing blocks. The cancellation loop settles as the rise/fall time of $V_{CP}$ matches with the fall/rise time of $V_{SW}$. This leads to cancellation of ripple at the LIN output caused by rising and falling edge of $V_{SW}$. The 8 bits from each of the positive and negative ripple processing blocks control the rise time and fall time of $V_{CP}$ respectively. The unit LSB current is chosen as 100 uA to to accommodate a wide range of rise-fall time (1ns – 4ns) of $V_{CP}$ to match $V_{SW}$. The output stage of the slew-controlled buffer is sized accordingly to source/sink max current of (255 x 100 uA = 25.5 mA).

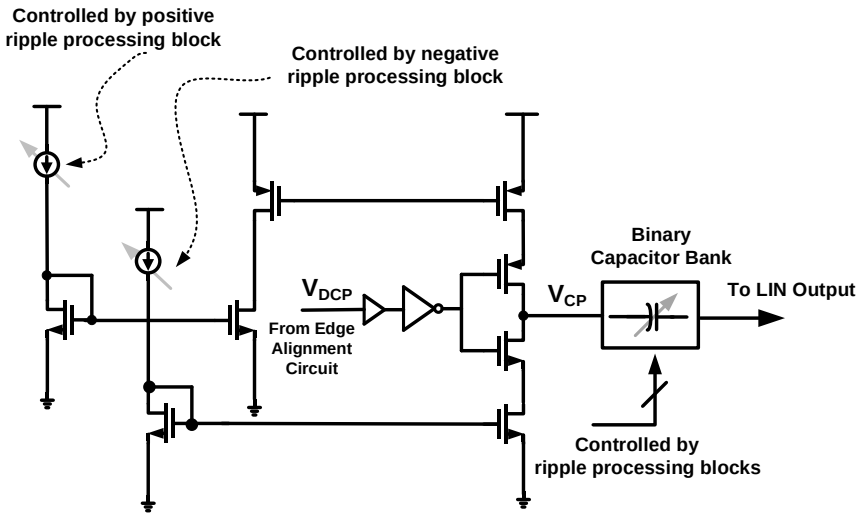


Figure 4.16: Slew Controlled Buffer.

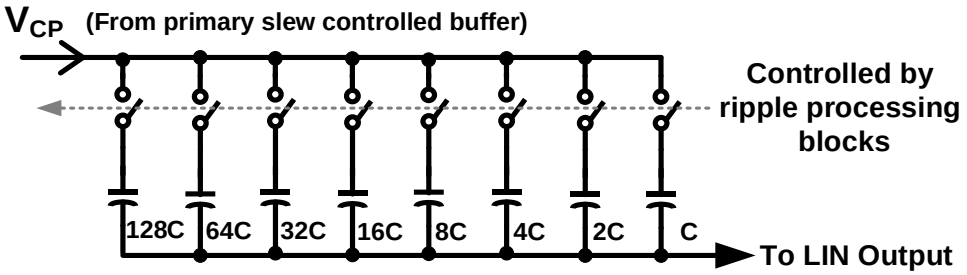


Figure 4.17: Binary Capacitor Bank.

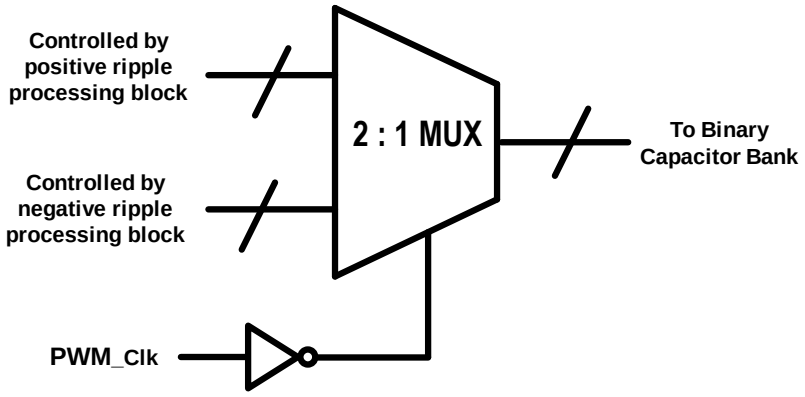


Figure 4.18: Digital Logic to Control Binary Capacitor Bank.

### 4.6. Binary Capacitor Bank

The architecture of the 8-bit binary weighted capacitor bank is shown in Fig. 4.17. $V_{CP}$ generated by the slew-controlled buffer is injected on to the output of the LIN driver through the binary capacitor bank. The cancellation loop drives the binary capacitor bank to fine tune the value of $C_{CAN}$ to match with $C_{SUB}$. The binary capacitor bank is digitally controlled by the positive and negative ripple processing blocks. The digital bits driving the slew-controlled buffer also control the binary capacitor bank through some digital logic. The digital logic used for the control is implemented using a few logic gates, two 8-bit counters and eight 2:1 MUXs. The binary capacitor bank is shared on a time multiplexing basis through PWM_Clk as shown in Fig. 4.18 for both positive and negative ripple cancellation. With an initial LSB setting (00000001) of the binary capacitor bank, the cancellation loop tries to cancel the ripple at the LIN output by modulating the rise-fall time of $V_{CP}$. But without the matching $C_{CAN}$ with $C_{SUB}$, the cancellation loop is unable to cancel the ripple. Thus, the cancellation loop increments $C_{CAN}$ by 1 LSB and tries to cancel out the ripple with new $C_{CAN}$ by modulating the rise-fall time of $V_{CP}$. This process goes on until the cancellation loop settles as the rise/fall time of $V_{CP}$ matches with the fall/rise time of $V_{SW}$ and $C_{CAN}$ matches $C_{SUB}$ with good accuracy. The maximum and minimum value of $C_{CAN}$ generated by the binary capacitor bank is so chosen to account for the entire range of $C_{SUB}$. Once the rise/fall time of $V_{CP}$ matches with the fall/rise time of $V_{SW}$, the degree of the ripple cancellation at the LIN output depends on the matching of $C_{CAN}$ with $C_{SUB}$.

### 4.7. Closed Loop Simulation Results

The cancellation loop settles as the rise/fall time of $V_{CP}$ matches with the fall/rise time of $V_{SW}$ and $C_{CAN}$ matches $C_{SUB}$ with a good accuracy. The simulation results as shown in Fig. 4.19 depicts the outputs of the two counters controlling the rise/fall time of $V_{DCP}$ in steady state. Both counter settles as the EMI cancellation loop reaches steady state and the ripple on the LIN output/EMI Node reduced to a minimum value. The simulation results as shown in Fig. 4.20 depicts the EMI node before and after noise cancellation - the magnitude of the ripple is reduced by 100 mV with this EMI cancellation scheme. Some high frequency glitches are visible on the EMI node after noise cancellation. Package parasitics induce high frequency ringing on the switching node of the DC-DC converter as shown in Fig. 4.21. This leads to some residual ripple content and energy at higher frequencies which cannot be cancelled easily. The edge of the inverted cancellation pulse as shown in Fig. 4.21 cannot cancel out the high frequency noise even with proper timing alignment with the edge of injection pulse.

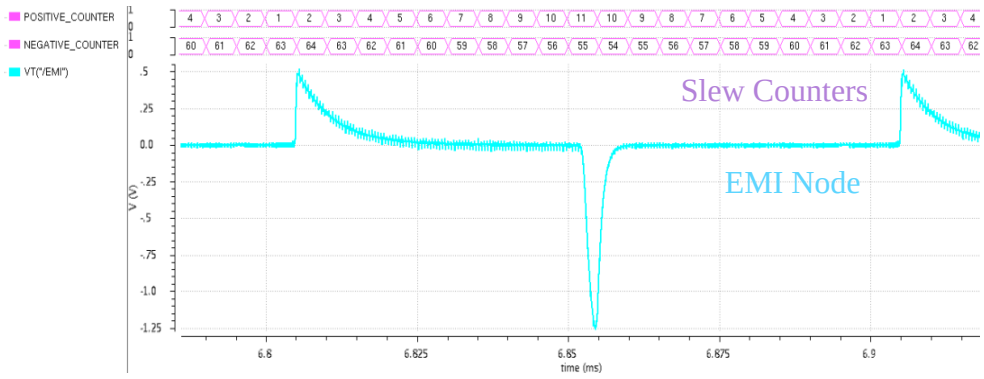


Figure 4.19: Simulation Results – Counters in Steady State and the EMI Node.

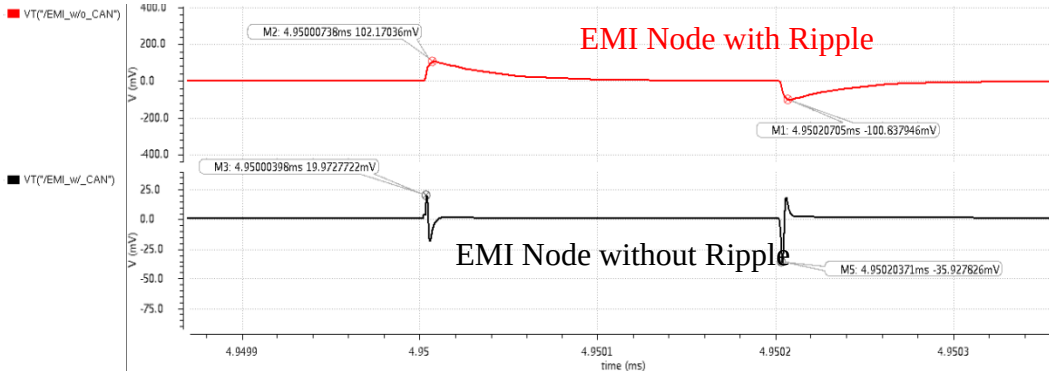


Figure 4.20: Simulation Results – EMI Node and Noise Cancellation.

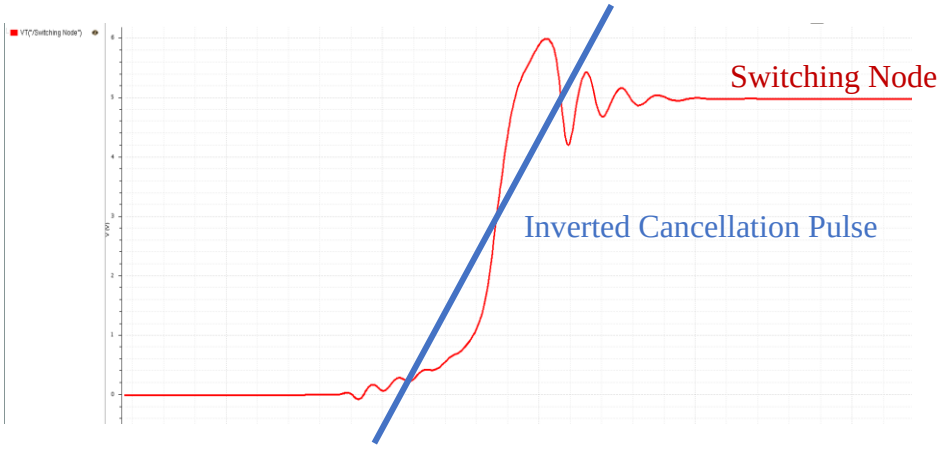


Figure 4.21: Simulation Results – Switching Node and the Inverted Edge of the Cancellation Pulse.

# CHAPTER 5

## MEASUREMENT RESULTS

The proposed SBC with the LIN driver, power stage of the DC-DC switching regulator and active EMI cancellation circuit is fabricated in a 180nm BCD process. The die micrograph is shown in Fig. 5.1. The core area of the EMI cancellation circuit is 0.7 $mm^2$ excluding the LIN driver, power FETs, bond pads and the additional circuitry used for programming and testing, which is less than 3% of the overall area in a standard SBC [8], [27]. A QFN 32 package has been used for the die. The electromagnetic emissions are measured using the emissions measurement setup (consisting of 120 ohm, 4.7 nF and 50 ohm) connected to the to the LIN output pin on the PCB as shown in Fig. 5.2. The external

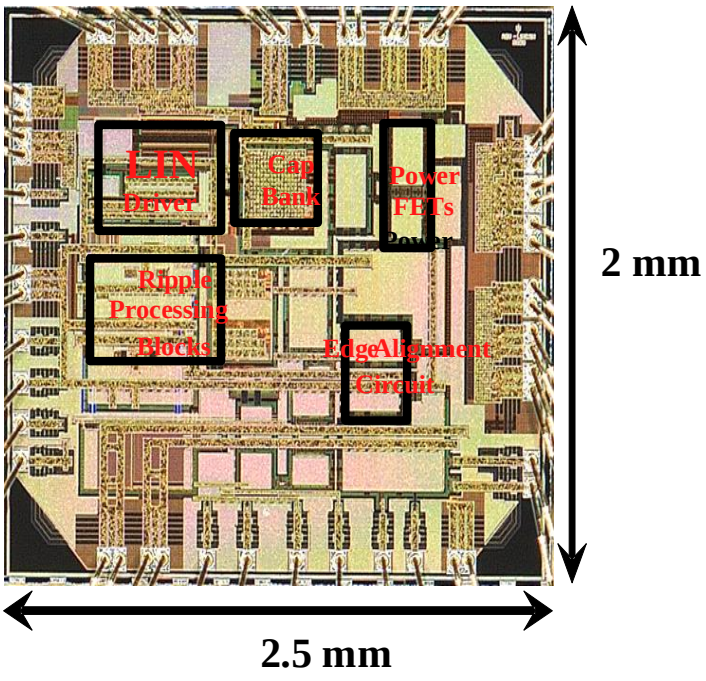


Figure 5.1: Die Micrograph.


Figure 5.2: PCB for Active EMI Cancellation Measurement.

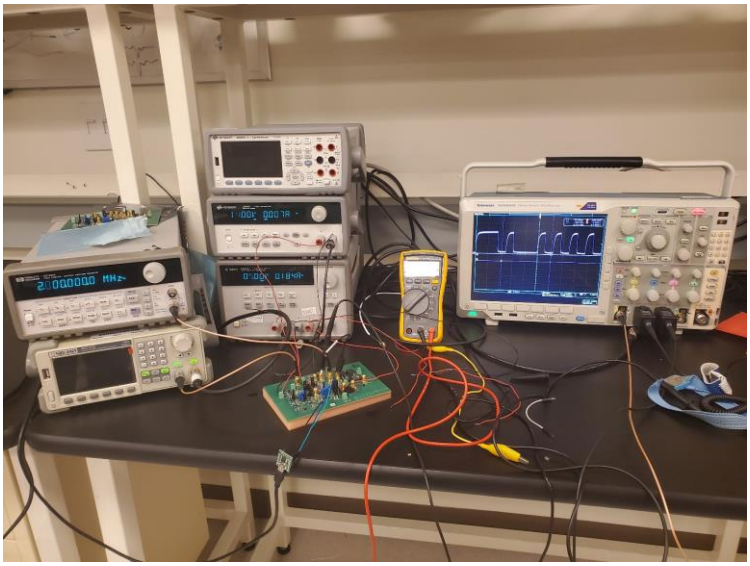

Figure 5.3: Measurement Setup for the Proposed EMI Cancellation Circuit Along with the PCB.

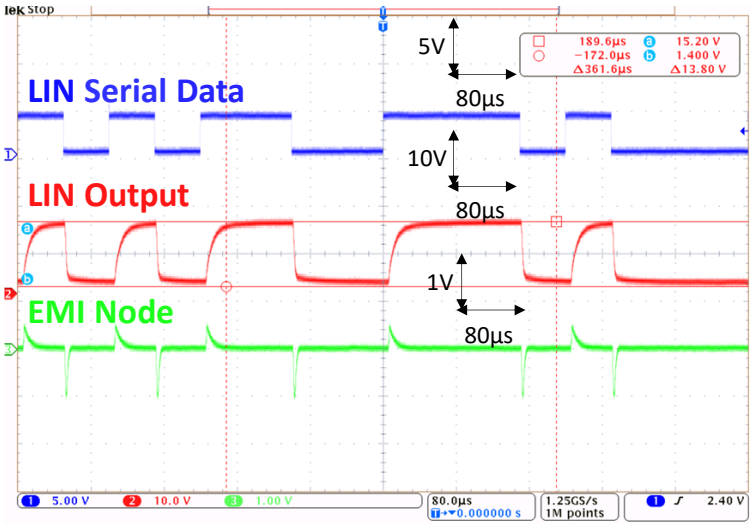


Figure 5.4: Measured Results with the DC-DC Switching Regulator OFF.

pull up resistance (Rb) and the diode $D_1$ are also connected to the LIN output pin on the PCB. The measurement setup is shown in Fig. 5.3. The MCP2210 serial peripheral interface (SPI) module is used for digital programming of the EMI cancellation circuit. This is done by writing the registers internally present in the block. SPI is used for programming of offset correction bits used to correct the offset voltages of unity gain buffers, integrators and comparators inside the ripple processing blocks. This is done to have high DC accuracy of the EMI cancellation loop and reduce the integrated noise ripple. Some bits are also used to program $C_{SUB}$ to check the effectiveness of the proposed ripple cancellation scheme with different $C_{SUB}$. The SPI module is also used for enabling the sub blocks in test mode for debugging purpose.

The LIN serial data, LIN output and the EMI node with the switching regulator turned OFF and ON are shown in Fig. 5.4 and Fig. 5.5 respectively. There is no ripple on the EMI node while the switching regulator is OFF as shown in Fig. 5.4. While the switching noise

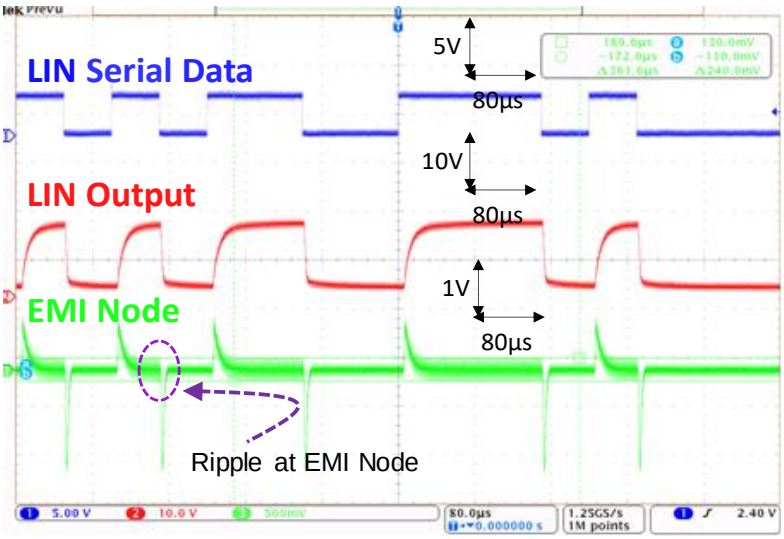


Figure 5.5: Measured Results with the DC-DC Switching Regulator ON.

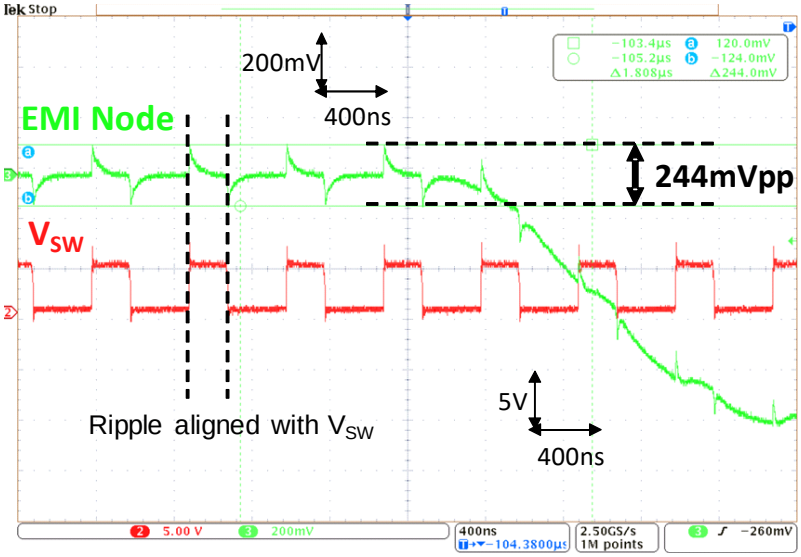


Figure 5.6: Measured results – EMI Node and $V_{SW}$.

of the DC-DC switching regulator shows up as a ripple on the EMI node when the switching regulator is turned ON as shown in Fig. 5.5. A zoomed in view shows that switching noise synchronized with $V_{SW}$ appears on the LIN output and EMI node as shown in Fig. 5.6. A peak-to-peak ripple of 244 mV appears on the EMI node as $V_{SW}$ switches between 5V and GND. Fig. 5.7 shows the output ($V_{DCP}$) of the edge alignment circuit which is synchronized with $V_{SW}$ with a timing offset along with the EMI node and $V_{SW}$. The spectrum at the EMI node is shown in Fig. 5.8. The EMI receiver measures the frequency spectral components radiated by the LIN network in a determined bandwidth [3]: 9 kHz: 150 kHz ≤ f ≤ 30 MHz; 120 kHz: 30 MHz ≤ f ≤ 1 GHz. The test specification mandates increasing the resolution bandwidth from 9 kHz to 120 kHz for frequencies higher than 30 MHz. Without the active EMI cancellation circuit enabled, tones at the switching frequency (2 MHz) and its harmonics exceeding the emission limits are observed in the spectrum. Fig. 5.9 shows the reduction of ripple at EMI node with the active EMI cancellation circuit turned ON. The peak-to-peak value of the ripple has reduced to 18 mVpp from 244 mVpp with the EMI cancellation circuit enabled. The tones at 2 MHz and its harmonics shown in the spectrum are reduced by more than 25 dB as evident in Fig. 5.10. The measurement results with varying programmable $C_{SUB}$, duty cycles of the DC-DC switching regulator and the corresponding ripple cancellation achieved are shown in Tables I and II. The solution has been implemented with a total current consumption of 2.5 mA which is nominally much lower than the supply current consumption in such SBCs [28]. The active EMI cancellation circuit ensures smooth functioning of the LIN driver implemented in standard BCD process in the presence of switching regulators sharing the same substrate.

The proposed noise cancellation technique works for switching converters with different gate driver strengths as $V_{CP}$ tracks rise-fall time of $V_{SW}$. The edge alignment circuit ensures that it also works for different duty cycles of the switching regulator. Die to die variations in $C_{SUB}$ are also overcome by accurate modulation of $C_{CAN}$.

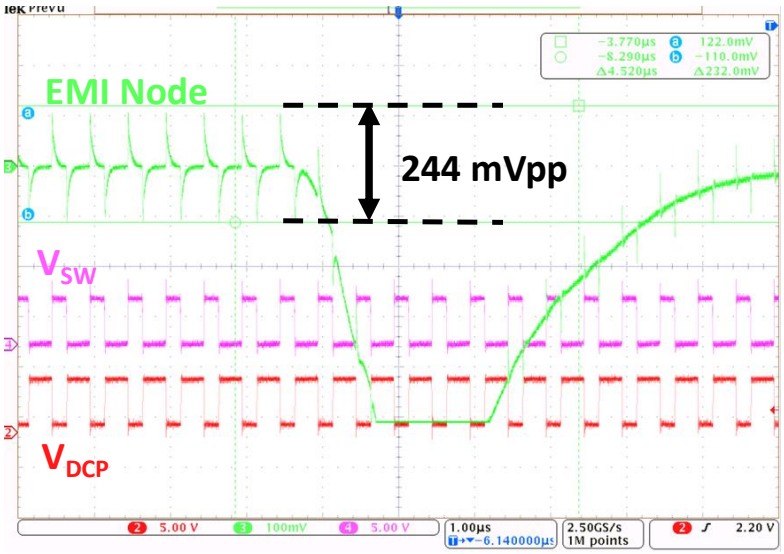


Figure 5.7: Measured results – Noise at the EMI Node with Active EMI Cancellation Circuit OFF.

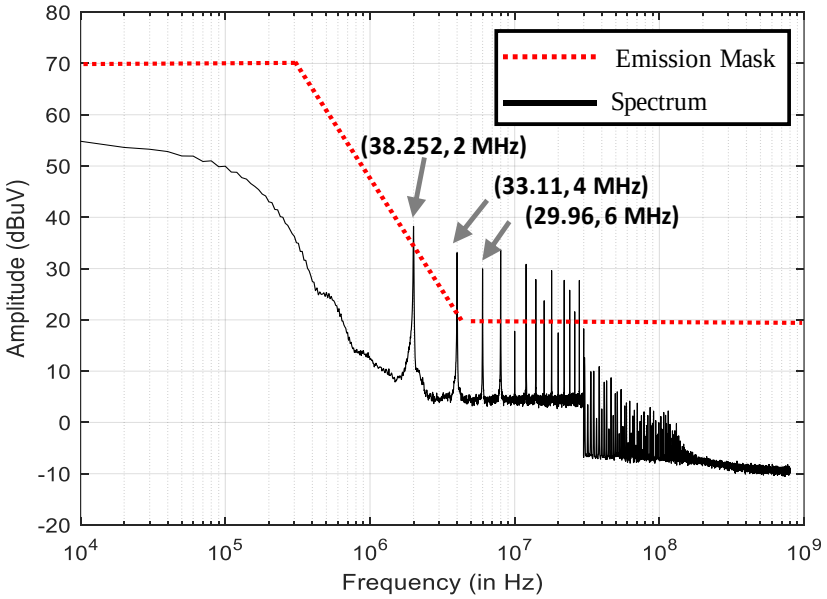


Figure 5.8: Measured results – Spectrum at the EMI Node with the Active EMI Cancellation Circuit OFF.

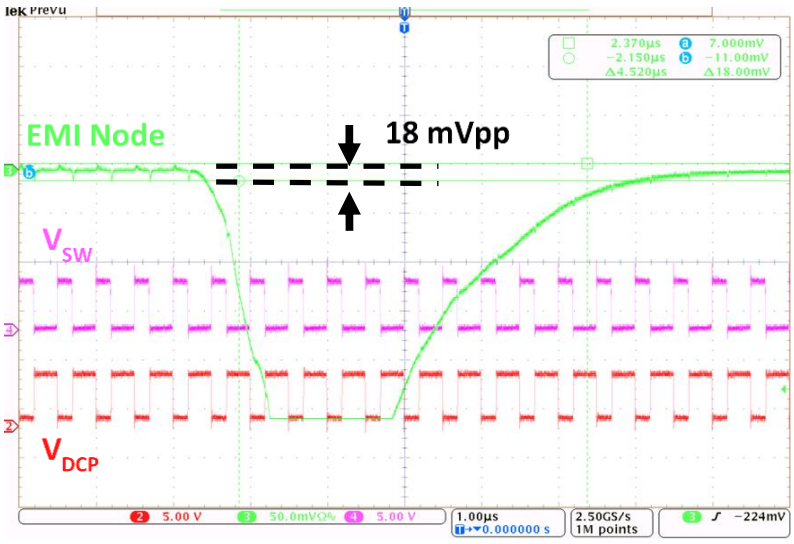


Figure 5.9: Measured results – Noise at the EMI Node with Active EMI Cancellation Circuit ON.

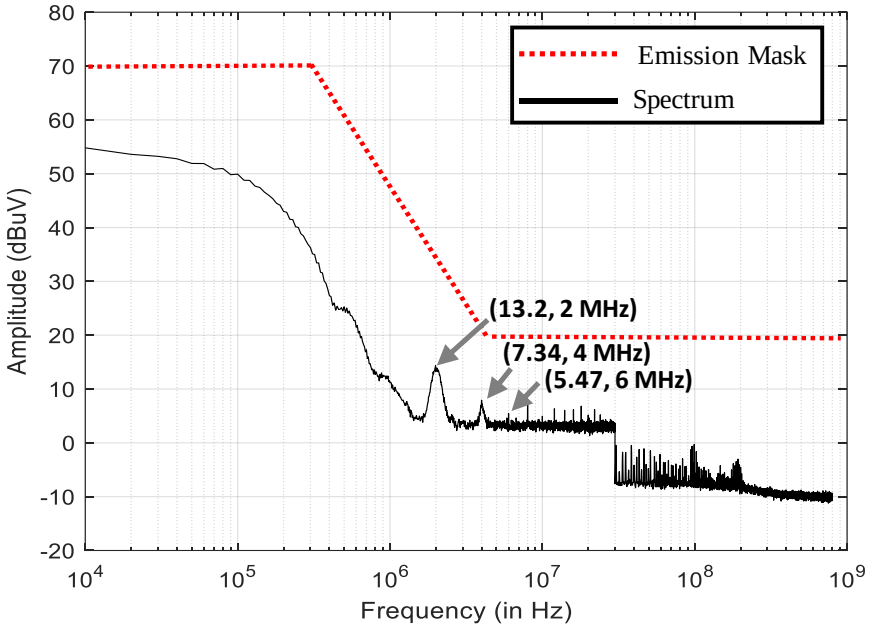


Figure 5.10: Measured results – Spectrum at the EMI Node with the Active EMI Cancellation Circuit ON.

Table I: Measurement Results with Varying $C_{SUB}$ (VIN_BUCK = 5V, Duty Cycle = 40%, Slew rate @VSW = 2V/ns

| $C_{SUB}$ | Magnitude (dB) of spurs before ripple cancellation at | | | Magnitude (dB) of spurs after ripple cancellation at | | |
|---|---|---|---|---|---|---|
| | 2 MHz | 4 MHz | 6 MHz | 2 MHz | 4 MHz | 6 MHz |
| 14 pF | 36.4 | 31.4 | 28.5 | 11.6 | 5.9 | 4.2 |
| 16 pF | 38.3 | 33.1 | 30 | 13.2 | 7.3 | 5.5 |
| 18 pF | 40.3 | 35.7 | 32.8 | 15.7 | 10.1 | 8.4 |
| 20 pF | 42.2 | 37.1 | 33.7 | 17.4 | 11.8 | 9.6 |

Table II: Measurement Results with Varying Duty Cycle (VIN_BUCK = 5V, $C_{SUB}$ = 16 pF, Slew rate @VSW = 2V/ns

| Duty Cycle | Magnitude (dB) of spurs before ripple cancellation at | | | Magnitude (dB) of spurs after ripple cancellation at | | |
|---|---|---|---|---|---|---|
| | 2 MHz | 4 MHz | 6 MHz | 2 MHz | 4 MHz | 6 MHz |
| 30 % | 39.1 | 34 | 30.7 | 14.4 | 8.7 | 5.9 |
| 40 % | 38.3 | 33.1 | 30 | 13.2 | 7.3 | 5.5 |
| 50 % | 37.7 | 32.4 | 29.4 | 12.3 | 6.4 | 5.1 |
| 60 % | 37.1 | 31.5 | 28.7 | 11.8 | 5.2 | 4.7 |

# CHAPTER 6

# CONCLUSION AND FUTURE WORK

## 6.1. Conclusion

This dissertation presents an active EMI cancellation scheme applicable for LIN drivers within an SBC implemented in standard BCD process. The EMI cancellation circuit offers a high degree of immunity for a LIN driver against conducted EMI from DC-DC switching regulator, sharing the same substrate on an SBC. Measurements at the EMI node with the EMI cancellation circuit ON shows that spurious emissions at the LIN output have been reduced by more than 25 dB and are well within the defined emission mask. The robustness of the EMI cancellation circuit has also been checked with varying substrate capacitance, LIN bus capacitance and different duty cycles, load currents of the DC-DC switching regulator. The design of the proposed solution is based on tracking the switching frequency of the DC-DC switching regulator and thus can work across a wide range of switching frequencies if the DLLs generating the cancellation pulse have a wide locking frequency range.

## 6.2. Future Work

In terms of the system level improvement, the major addition would be to integrate an on-chip fully compensated buck/boost regulator [29]-[31] with a wide range of load current. The EMI cancellation can be verified with a wide range of load current. The drive strength of the driver can also be made programmable to check the effectiveness of this EMI cancellation scheme with varying slew of the switching node.

Few other improvements can be made to this EMI cancellation scheme. These are listed as below:

1. The number of clock cycles used in the integration of the noise ripple can be made programmable with the switching frequency. Lower switching frequency requires more integration cycles to capture the same ripple information.
2. The current consumption of the integrators used in this scheme can also be made programmable based on how fast the ripple information needs to be captured.
3. Shared substrate is a huge problem from a noise standpoint. PMIC and SOC solution is dominant right now – All integration is not possible. We can explore active noise cancelling techniques to have total integration.
4. The DC-DC Converter in this work is well behaved operating in CCM. We can tweak the cancellation pulse generation scheme in this work and make it work for converter working in DCM.

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