Built-in Self Test for Monitoring Analog Circuits.

by

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A Thesis Presented in Partial Fulfillment
of the Requirements for the Degree
Master of Science

Approved April 2024 by the
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May 2024

ABSTRACT

Integrating analog circuits with the most advanced digitally-tuned processes increases the defect rates and the risk of in-field wearout. Coupled with the reduced accessibility arising from this level of integration, increasing defect rates necessitate systematic approaches to analog testing. Structural built-in self-test (BIST) for analog circuits can reduce test development complexity. Proposing a robust and low-cost structural BIST method for analog circuits. The proposed method relies on perturbing the analog circuit at an injection point and observing the result at an observation point as a digitally measurable time delay. Injection can be achieved via simple ON/OFF keying while the observation can be achieved by a self-referencing comparator. Multiple injection points can be selected at low cost (single transistor) while the observation circuit can be shared across many injection points and different circuit blocks.

ACKNOWLEDGMENTS

I would like to express my deepest gratitude to Professor Sule Ozev for providing me with the invaluable opportunity to work under her guidance. Her unwavering support, encouragement, and mentorship have been instrumental throughout my journey. I am truly grateful for her continuous assistance and belief in my abilities.

I extend my heartfelt thanks to Professor Jennifer Kitchen and Professor Bertan Bakkaloglu for graciously serving on my defense committee and for their insightful contributions, which have enriched my work.

I also wish to extend my sincere appreciation to all the professors who have imparted their knowledge, wisdom, and expertise to me during my Master's degree. Each class, lecture, and interaction has contributed significantly to my growth, both academically and personally. Their dedication to teaching and commitment to excellence have inspired me to pursue my passions with diligence and integrity.

Special appreciation goes to my colleague, Suhas Kashyap, for his collaboration, guidance, and unwavering support during this project and throughout my master's program.

Lastly, I am profoundly grateful to my parents for their unconditional love, unwavering support, and belief in me.

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INTRODUCTION

Within the realm of System-on-Chip (SOC) development, semiconductor testing and packaging constitute a significant segment, accounting for 15% of the overall SOC cost. The semiconductor testing market is expected to grow steadily at a rate of 7% each year. Complexity has grown immensely, so the test techniques must become unique to meet the challenges of modern days. The process of testing semiconductor devices is crucial for validating their performance against defined specifications and ensuring adherence to quality standards. This critical step in the manufacturing workflow not only identifies and mitigates defects but also prevents substandard components from reaching the market, thereby safeguarding device functionality. By integrating testing early and throughout the production cycle, manufacturers significantly enhance the reliability of their products, reducing the incidence of operational failures. Furthermore, this preemptive approach to quality control contributes to cost efficiency by minimizing the financial impact of defects and optimizing manufacturing processes.

1.1 History of Semiconductor Testing

With the invention of the transistor, Initial testing methods involved basic electrical measurements to validate the fundamental functionality of semiconductor devices. As integrated circuits became more complex, manual testing was no longer viable. Then came the bed of nails method, also known as flying probe testing, is a non-intrusive testing technique for circuit boards. Instead of using fixed test fixtures, it employs movable probes to make contact with specific points on the board. The bed

of nails method evolved to the present day Automated Testing Equipment (ATE), which made testing quicker and more precise.

Figure 1.1: Modern-day Automatic Test Equipment

The exponential increase in the number of transistors and the challenges associated with accessing internal blocks necessitated modifications in design approaches to enable effective testing. This need led to the emergence of Design for Testability (DFT) principles, which focus on integrating testability features into the design phase to streamline and enhance the testing process. The shift to System-on-Chip (SoC) designs introduced new testing challenges due to the integration of entire systems onto single chips. This necessitated advancements in testing methods, including mixed-signal testing for both analog and digital components and System-Level Testing to verify devices within larger systems.

1.2 Design for Testablility

Design for Testability (DFT) has emerged as a pivotal aspect of semiconductor design, evolving significantly over the years to meet the growing complexity and demands of integrated circuits. Initially conceived as a response to the challenges posed by increasing circuit complexity and manufacturing variability, DFT gained prominence in the late 20th century as a proactive approach to enhancing the testability

of semiconductor devices. The rise of DFT can be attributed to the escalating costs associated with testing, particularly as the number of transistors per chip continued to rise exponentially. Over time, DFT methodologies have evolved to encompass a wide array of techniques, including scan chains, boundary scan cells, automatic test pattern generation (ATPG), and structural testing approaches.

Scan chains, for instance, facilitate the efficient capture of internal node states during testing. Boundary scan cells serve as interfaces between internal circuitry and external test equipment, enabling boundary scan testing for fault detection related to pin connections and interconnections. Additionally, ATPG algorithms automatically generate test patterns to detect faults, contributing to comprehensive testing coverage.

Most of the previous methods listed serve well for digital circuits. Analog Design for Testability (DFT) techniques are not as developed as their digital counterparts due to several inherent challenges. Unlike digital circuits, analog circuits exhibit greater sensitivity to variations in manufacturing processes, temperature, and voltage, making them more susceptible to performance deviations. The complexities associated with analog circuitry, including the continuous nature of signals and the presence of noise, make it challenging to implement effective DFT methodologies.

1.3 Built-In-Self-Test

Built-in self-test (BIST) is a design technique that allows them to perform self-diagnosis to check for faults or malfunctions. These structures enable devices to test themselves without the need for external testing equipment. Digital ICs have numerous forms of Built-In-Self-Test with Memory BIST(MBIST) and Logic BIST(LBIST)

being the most prominent ones. MBIST generates patterns to the memory and reads them to log any defects. LBIST on the other hand constitutes a pattern generator and analyser that catches any defects present.

Analog BIST typically involves the integration of specialized test circuitry within the analog circuit itself. This embedded test circuitry is designed to generate specific test signals and assess the responses from various analog components. The test results are then analyzed to identify potential faults or deviations from expected behavior.

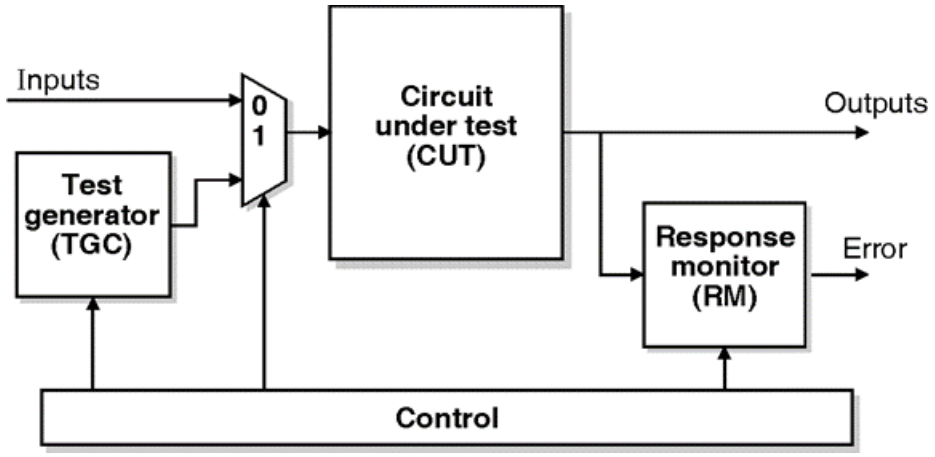

Figure 1.2: Typical Built-In-Self-Test Circuit

This thesis proposes an Analog BIST technique that uses ON/OFF keying and delay monitors. This method, utilizing mostly digital circuits, is scalable and can be applied to analog circuits without domain knowledge in a plug-and-play fashion. The ON/OFF keying inputs can be applied to non-sensitive nodes, such as DC bias points, and the observation can be done by either directly treating the output signal as a digital signal or using a self-referencing comparator. Injection points can easily be added to increase fault coverage while the observation circuit can be shared among all injection/observation points.

1.4 Thesis Outline

The thesis is organized as follows: Chapter 2 provides an overview of past research and the motivation behind this thesis. Chapter 3 discusses the design methodology and the fault models used for verification. Chapter 4 offers details of the BIST implementation, architecture, and the circuits on which fault simulation is conducted. Chapter 5 presents the results and fault coverage analysis. The thesis concludes in Chapter 6, which outlines potential future improvements to the work.

Chapter 2

PRIOR WORK

2.1 Literature Survey

Traditionally, analog circuits have been tested using the list of functional specifications as a basis for test development [8]. Many BIST approaches that have been developed also follow this process and aim at measuring specifications directly or indirectly [23, 21, 17, 35, 32]. Specification-based BIST methods can also be effective in terms of fault coverage [19, 21, 17].

However, specification-based BIST requires design and domain knowledge and can take significant design effort, which the designers may not be willing to provide. Furthermore, high fault coverage cannot be guaranteed in specification-based testing, regardless of whether external or internal measurements are conducted. A structural test (or BIST) method can alleviate some of these problems. Structural methods are agnostic of the circuit functionality and rely on the injection and observation of signals at multiple circuit nodes. In digital circuits, already existing storage components (flip-flops) have been altered and fitted for injection and observation of test signals in the test mode. Unfortunately, there is no such storage unit in analog circuits, thus injection and observation need to be done within the functional circuit components. This requirement favors built-in tests since connecting multiple internal nodes to primary inputs and outputs is cumbersome.

Structural testing relies on finding an invariant from the circuit that can be mon-

itored and is closely related to the structure of the circuit. This invariant can be a specification parameter (e.g. gain), a functional parameter (e.g. transfer function), or another measurable quantity (e.g. supply current). The principle is that the invariant will be significantly altered if there is a structural deviation in the circuit. The significant change needs to be quantified concerning process variations. In other words, a structural defect is only detectable if it deviates from the determined invariant beyond process variations. It is desirable to have a monitoring method with a low area overhead and negligible performance overhead. To provide a systemic monitor insertion method that does not rely on significant design effort, monitors need to have an almost all-digital interface. The monitor should not be susceptible to process variations, but it needs to be sensitive to structural defects. Various monitors have been explored in the literature, including supply current [11, 26, 1], and the parameters (poles, zeros, resonant frequency, etc.) of the transfer function [39], which can provide coverage up to a point. Increasing fault coverage and systemic monitor insertion requires identifying digital-friendly monitors. When a circuit is disturbed at one location, this disturbance often propagates to other parts of the circuit. This propagation is dependent on the circuit structure and thus can be taken advantage of to provide an invariant that can be digitally measured. If the input disturbance is provided digitally, and the output response is converted to a digital response easily, this process reduces measuring a time delay between a digital input and a digital output.

Analog components have become as vulnerable as their digital counterparts for long-term degradation and wearouts and require in-field built-in self-test (BIST) [31, 25, 9]. Any BIST technique needs to be evaluated in terms of fault coverage. Typically, analog fault models have been categorized as catastrophic faults (resistive

opens and shorts in the circuit) or parametric faults (out-of-tolerance deviations in process parameters) [38]. Fault simulation can be achieved by injecting the model representing each defect location and simulating the circuit based on the given input conditions [27, 41, 6, 37]. [5] and [34] provide a strong framework for analog test coverage, pass/fail of devices and different types of faults.

BIST methods can be functional or structural. Functional methods aim at the extraction of the performance parameters of the circuit based on the measurements obtained from the BIST circuit. In [24, 22, 20, 18, 36], a digital PRBS input sequence is used to perturb a closed-loop circuit while the output response is converted to the digital domain and cross-correlated with the input signal to measure the parameters of the transfer function. In [15], the authors propose to predict one of the specifications, the natural frequency, of filters via digital signatures based off current measurements from a 4-input current comparator. In [3], the authors implement an RF impedance measurement scheme using periodic structures. In [28], measured sensor values are fed into a neural network to predict pass/fail. In [16, 4, 10], the authors aim at indirectly classifying the specification test results. In [40], the authors build an on-chip transfer function measurement system. Many such BIST circuitry have been developed to measure specific performance parameters, such as gain, input intercept, phase mismatch, DC offsets, of various analog and RF circuits. Functional BIST methods can directly provide the specifications of the circuit, which, until recently has been the golden standard of analog testing. However, functional BIST requires significant design effort and domain knowledge. Furthermore, specification-oriented testing cannot guarantee the detection of all faults, especially in circuits with closed-loop operation [22].

Structural BIST methods aim at developing monitoring approaches that are agnostic of the circuit functionality. Hence, structural methods are more amenable to plug-and-play BIST insertion. In [33], the authors exploit structural symmetries in analog circuits to construct signals and detect faults based on the abnormal behavior of those signals. This method cannot be generalized to circuits where symmetry is not present. IDDQ-based techniques refer to the measurement of the supply current and checking that the current is within pre-determined bounds, typically determined via Monte-Carlo simulations [29, 13, 14]. Alternatively, supply current measurements can be used to predict performance parameters [2]. In [30], the authors develop a built-in-current sensor while [12] proposes a microcontroller based current measurement method. Since almost all components contribute to the supply current, the effect of a given fault diminishes as the circuit gets larger. Thus, fault coverage of supply current-based BIST methods is typically not at desirable levels. While supply measurement can be one of the BIST monitors, additional monitors may be necessary to improve fault coverage.

Recently, a structural method for security assessment of analog circuits has been proposed based on delay measurements [7]. While experimental results have been shown to detect changes in the performance locking bits, no effort has been made to assess or increase fault coverage to satisfactory levels. Even though there has been significant progress in analog BIST techniques, there is a gap for plug-and-play structural BIST techniques where the aim is to provide high fault coverage at low hardware and performance cost.

2.2 Motivation

The surveyed methods, while effective in their targeted applications, often require extensive domain knowledge and manual intervention, limiting their ease of implementation. This underscores the necessity for an analog BIST technique that not only is capable of detecting structural faults but also adheres to the following criteria:

1) Ease of Implementation: The method should be straightforward to integrate into various circuit designs without the need for extensive modifications or specialized knowledge.

2) Low Area and Performance Overhead: To ensure minimal impact on the circuit's size and operational efficiency, the BIST technique must have a low footprint and should not significantly detract from the circuit's performance.

3) Independence from Domain Knowledge: The approach should minimize the necessity for in-depth domain-specific knowledge, making it accessible to a broader range of designers and engineers.

4) Generic and Scalable: It is imperative that the BIST solution be versatile and scalable, making it suitable for a wide array of analog circuits, regardless of their complexity or function.

5) Capability to Detect Structural Faults: Above all, the method must reliably identify and diagnose structural faults within the circuit, ensuring the highest level of integrity and functionality.

This thesis proposes to overcome the limitations found in previous approaches, offering a versatile and efficient solution for analog circuit testing.

Chapter 3

DESIGN METHODOLOGY

There are two primary methodologies for testing integrated circuits-structural testing and functional testing. Structural testing focuses on evaluating the physical integrity and connectivity of the circuitry at the transistor and interconnection levels. It involves the direct examination of the underlying architecture to detect defects such as shorts, opens, and bridging faults. In contrast, functional testing assesses the behavior of the circuit under specified input conditions, verifying its compliance with the intended functionality.

Structural testing typically offers faster test times compared to functional testing due to its targeted approach toward fault detection at the physical level. By directly probing the circuit's structure, structural tests can rapidly identify and isolate defects, contributing to quicker test cycles and improved throughput.

The design methodology employed in this thesis is grounded in a fundamental principle of circuit behavior: a perturbation introduced at one point will propagate through structurally connected nodes. Building upon this principle, a technique is devised wherein an analog circuit is subjected to perturbation at a designated injection point through a digital signal. This injection circuit may entail simple ON/OFF keying of circuit components or the incorporation of supplementary components tailored for Built-In Self-Test (BIST) purposes.

To monitor the circuit's response to this perturbation, an observation node is

designated. Subsequently, the response is converted into a 1-bit digital signal. The time delay between the injection and observation points serves as an invariant, which is exploited to assess the structural integrity of the circuit. Notably, the injection process requires minimal additional circuitry, facilitating the straightforward addition of multiple injection points to enhance fault coverage as needed. Moreover, to streamline the process, a single observation circuit can be utilized for all injection and observation points through multiplexing.

One significant advantage of this proposed methodology lies in its independence from domain-specific knowledge beyond the identification of suitable injection or observation nodes. This information, including nodes to be included or avoided, can be easily provided by the circuit designer, thereby simplifying the implementation process. This method has the potential to be automated and evolve into a process similar to that of Automatic Test Pattern Generation (ATPG).

The initial step involves identifying specific points for both the injection of perturbation and the observation of its response. The circuit designer can provide a list of potential injection/observation nodes or sensitive nodes, or sensitivity simulations can determine these nodes. The selection of the observation circuit is based on the DC operating point of the circuit. The delay between the digital input and output signals serves as the structural invariant of the circuit, with deviations indicative of process variations or faults. Monte Carlo simulations during the design phase estimate the expected delay between each injection and observation point, establishing thresholds for go/no-go testing during test time. The observation circuit may require adjustments, such as modifying its storage capacitor, to accommodate the measurement time. Fault coverage estimation for a given injection/observation point involves running fault simulations at the transistor level, with faults above or below the de-

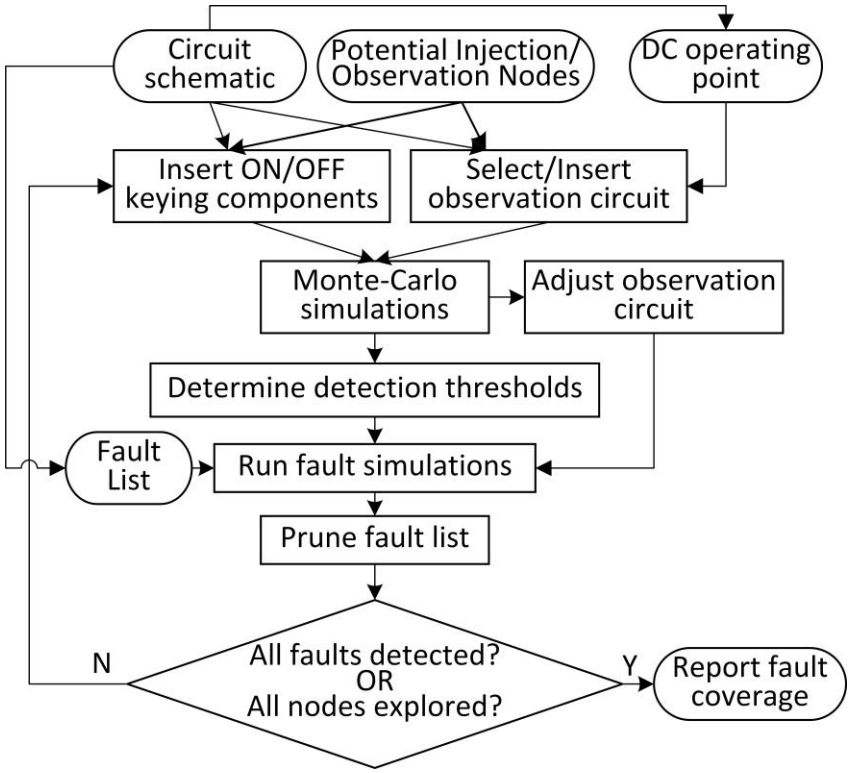

Figure 3.1: Flow of Proposed Methodology

termined thresholds classified as detected. To achieve desired fault coverage levels, a greedy approach is employed. Evaluation begins with the first injection/observation node pair, with subsequent pairs evaluated iteratively until reaching the desired fault coverage or exhausting all potential nodes. Fault coverage is calculated as the ratio of the total detected faults to the total simulated faults, including faults in transistors used for injection and observation.

3.1 Injection Points

Numerous methods exist for injecting perturbations into a circuit, with a key consideration being the minimization of overhead associated with the injection circuitry. Given the structural nature of this test, considerations of the circuit's operational or DC operating point are unnecessary. This flexibility allows for the selection of

various injection points. Given that circuit operation is not a concern, employing a large signal for perturbation aids in detecting significant changes in the observation circuit. Simple ON/OFF keying is proposed for perturbing circuit nodes.

The two main injection methods used are:-

1) Bypassing Passive Components:-

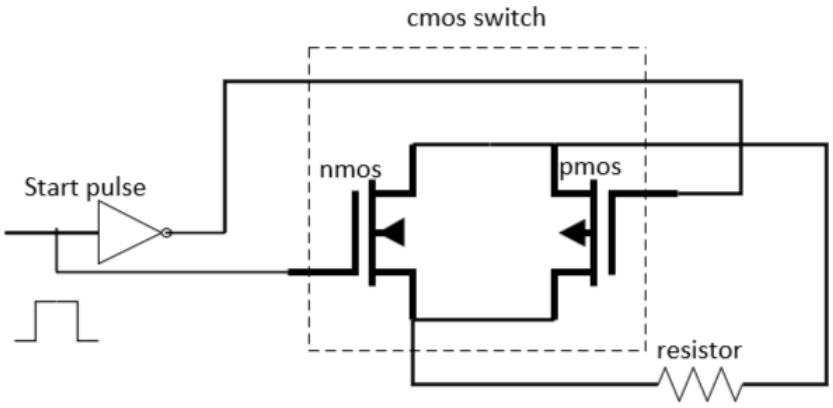

Figure 3.2: Injection Method by Bypassing Passive Components

Passive components like resistors and capacitors can be bypassed by connecting a pass transistor across their terminals, effectively short-circuiting them. Although this doesn't create an exact short circuit due to the pass transistor's ON resistance, the effect is similar when the ON resistance is significantly smaller than the resistance being bypassed. While capacitors exhibit more complex behavior involving exponential changes, the desired effect of generating a large signal perturbation in the circuit is achieved. Short-circuiting certain circuit components may result in minor perturbations but as long as the perturbation is detectable, the magnitude of the signal does not matter. A CMOS transistor might be a better alternative than an NMOS or PMOS as it has a reduced ON resistance during the BIST operation.

2) Perturbing DC points:-

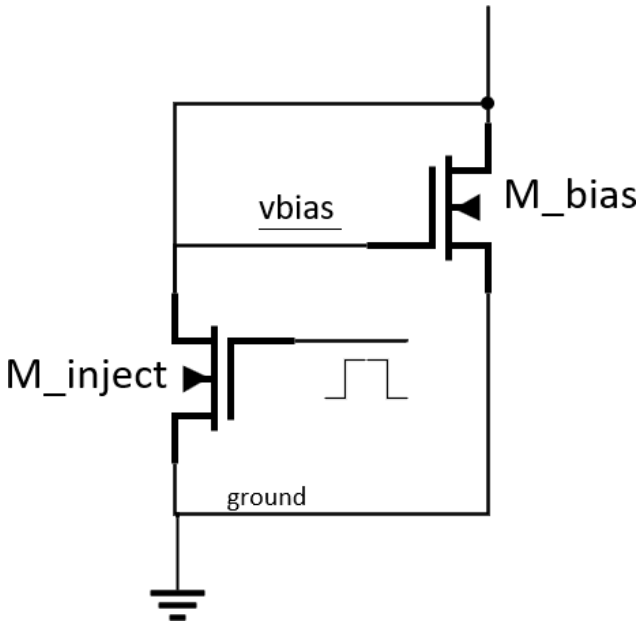

Figure 3.3: Injection Method by Perturbing DC Points

Bias voltages and generators offer a strategic approach to perturbing the circuit due to their influence on multiple points simultaneously. This characteristic proves advantageous as it enables broader structural coverage, thereby enhancing fault detection capabilities. Analog circuits commonly employ bias generators to establish the DC operating point of transistors, often featuring multiple bias points across the circuit, thus providing numerous injection opportunities. Starting with bias voltages that have the greatest effect on the circuit, we progressively integrate additional bias voltages to enhance coverage as needed.

The injection circuitry for perturbing bias voltages is depicted in Figure 3.3. Here, the gate of the bias transistor (V_{bias}) is grounded via the injection transistor (M_{inject}). The injection transistor must be sufficiently sized to ensure its drain-to-source voltage (V_{ds}) remains below the NMOS transistor threshold. Although this bypass circuit

may not completely deactivate M_{bias}, it effectively restricts its current flow and hence perturbs the circuit.

3.2 Observation Circuit

The observation circuit needs to be able to capture the delay between the input perturbation and the output response. This delay measurement necessitates converting the output response into a 1-bit digital form. While the circuit response is in the analog domain, it is desired to have a digital pulse as the response of the observation circuit Two methods facilitate this: Firstly, if the circuit's DC point is approximately mid-supply (Vdd/2), a digital pulse can be captured by directly linking a chain of inverters to the observation node. These inverters only need to shift the output beyond their switching point, and due to their high gain around mid-supply, a chain of inverters (two to three inverters) can fully restore the signal to a digital swing.

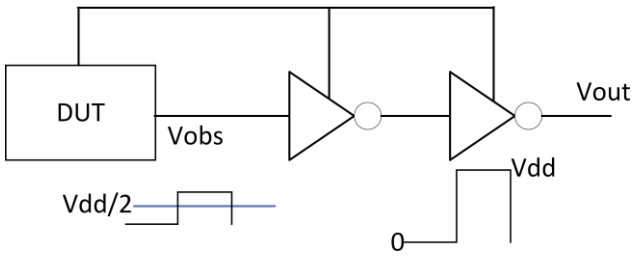

Figure 3.4: Observation Circuit Using an Inverter Chain

Figure 3.4 shows an observation circuit where Vobs is the observation node and Vout is the output after full-swing restoration. If a fault shifts the DC point to a degree where the inverters fail to respond to the minor perturbation, the delay becomes infinite, facilitating the detection of such faults. Furthermore, DC points farther from mid-supply can also be directly observed using this method, provided inverters are designed to switch at different voltages.

If the observation node is not at a DC level close to mid-supply, an alternative method for extracting the 1-bit response is by utilizing a self-referencing comparator, as depicted in Figure 3.5.

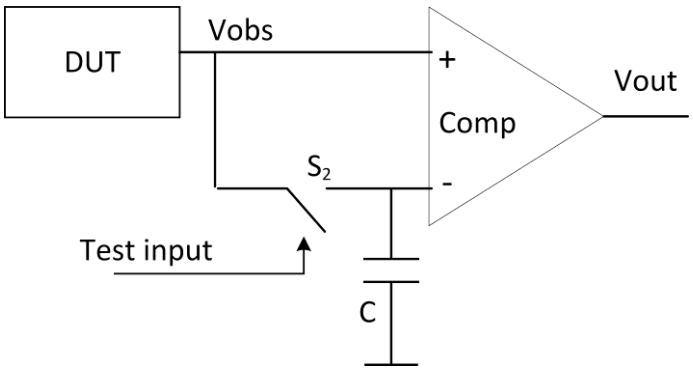

Figure 3.5: Observation Circuit Using a Self-referencing Comparator.

During normal operation of the circuit, the switch (S2) is closed, allowing the capacitor to store the DC value. Subsequently, the perturbation circuit is activated in the test mode. The capacitor is precharged to a value depending on the circuit. The circuit is perturbed once the test signal goes from low to high. The capacitor voltage then becomes the comparison threshold for the new measurement.

A counter is employed to measure the delay. The difference between the voltages at the output node before and after the disturbance is amplified by a pre-amplifier and passed through the comparator. If the circuit response to the perturbation is strong enough, the pre-amplifier may be removed from the observation circuit.

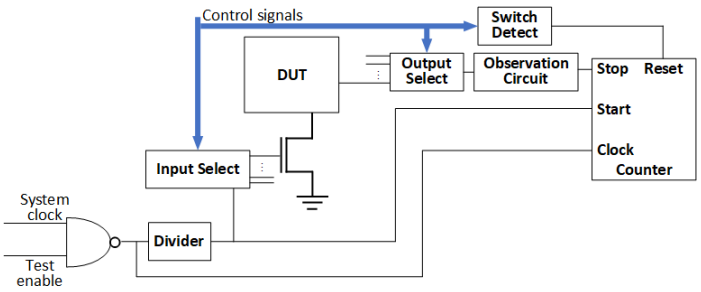

Figure 3.6: Measuring Delay Using a Counter.

The clock input is gated during normal operation and enabled using the test enable signal. Given the potential presence of multiple injection and observation points, their selection necessitates control signals. Activation of switching inputs results in the counter reset, allowing a single injection/observation pair to be activated multiple times for averaging purposes. Additionally, the test input signal is derived from the system clock via a divider. The counter commences upon the signal switch at the input and halts upon the switch in the output response.

3.3 Fault Models

To validate the methodology, fault models must be employed to simulate faults within the circuit. Figure 3.7 (a) depicts an open circuit at the drain of the transistor and (b) shows the physical implementation of a short circuit between the source and drain of the transistor.

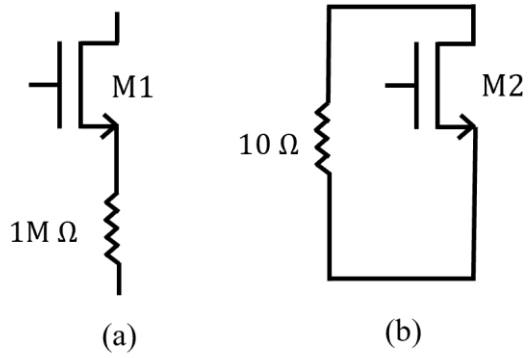

Figure 3.7: Fault Model Circuit Implementation.

The two primary catastrophic faults in a transistor are open circuit and short circuit faults. Open circuit faults may manifest on any terminal of the transistor - namely gate (G), source (S), and drain (D). Typically, short circuit faults occur between the gate and source, as well as between the drain and gate. However, the likelihood of a short circuit fault occurring between the drain and the source is lower due to the significant distance between these two terminals. Based on previous re-

search, open circuit faults are represented as a resistive connection of 1MΩ at the source and drain terminals. Applying the same approach to the gate terminal is ineffective since no significant DC is flowing into the gate terminal. Thus, gate open faults are modeled using a resistive termination for the gate node on both sides of the open circuit. Short circuit faults are represented as a 10Ω resistive connection between the terminals. Modifying the length of the transistor is used to introduce parametric faults. Additionally, process variations can cause shifts in the threshold voltages of transistors. All of these faults can be readily simulated by adjusting the netlist.

3.4 Establishing Limits

Delays measured during simulation may differ from those observed after fabrication. To accommodate variations in delay caused by process variations, Monte Carlo simulations must be conducted. Monte Carlo simulations utilize random sampling methods to model process variations, such as variations in doping concentration, oxide thickness, and other fabrication parameters. By performing numerous iterations with randomly generated input parameters, Monte Carlo simulations provide insights into the statistical distribution of device characteristics, such as transistor performance, power consumption, and reliability.

To determine the thresholds for observed delays, we conduct Monte Carlo simulations using 200 samples. Subsequently, we apply a Gaussian distribution to the collected delay data and employ a 3σ guard banding approach to establish the expected delay. Any circuit response falling beyond these guard-banded limits is considered faulty.

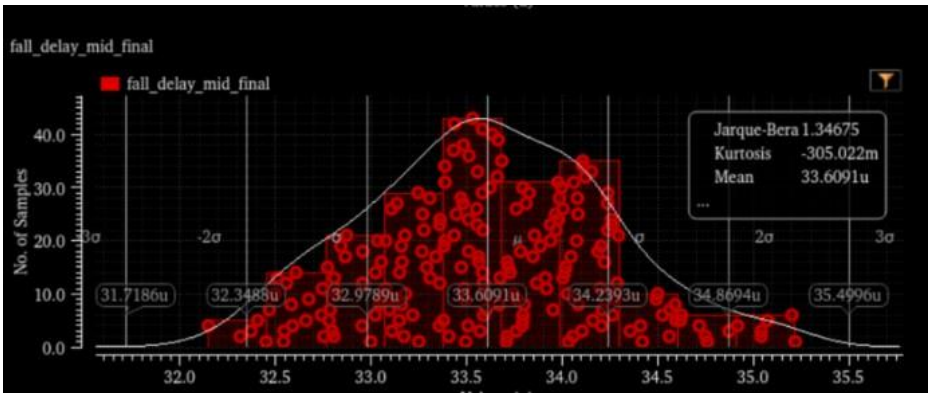

Figure 3.8: Example of Monte Carlo Simulation.

It's important to recognize that because delay isn't a specification parameter, it will be constrained from both ends. Put simply, certain faults may extend the delay beyond the $\mu + 3\sigma$ limit, while others may reduce it below the $\mu - 3\sigma$ limit, where μ represents the mean and σ represents the standard deviation of the distribution. This variation can be understood by examining the nature of the faults. For instance, a resistive open fault at the drain of a transistor could lengthen the delay if the transistor is involved in charging or discharging parasitic capacitance along the signal path. Conversely, a resistive short across the gate-drain or gate-source connection of a transistor might expedite this process by circumventing the transistor and offering a more direct current path. Consequently, both delay limits can be utilized to identify faults.

Chapter 4

IMPLEMENTATION

The methodology described in Chapter 3 was applied to analyze three different analog circuits with varying functionality and complexity. The initial circuit is a linear dropout voltage regulator. It is augmented with a Built-In Self-Test (BIST) pre-amplifier and comparator setup to transform its output into a 1-bit digital signal. This employs an ideal current source. To explore a more practical approach involving actual circuit biasing, the subsequent circuit experimented with was a third-order Sallen-Key filter utilizing cascode amplifiers. As a filter undergoes AC analysis, conducting a structural test that disregards the specific circuit operation proved to be particularly insightful. Since a time delay method is utilized, it was imperative to verify its suitability for high-speed applications. Consequently, the final assessment was conducted on a Phase-Locked Loop (PLL).

4.1 LDO

A Linear Dropout Voltage Regulator (LDO) operates by maintaining a stable output voltage despite variations in input voltage and load conditions. At its core, an LDO employs an error amplifier and a resistor divider network in its feedback loop. The error amplifier compares the reference voltage with the output voltage, generating an error signal proportional to the difference between the two. This error signal is then amplified and fed back to control the pass transistor, adjusting its resistance to regulate the output voltage. The resistor divider network divides the output voltage to provide feedback to the error amplifier, ensuring precise regulation. This dynamic feedback mechanism allows the LDO to efficiently regulate the output

voltage, making it a vital component in various electronic systems where stable voltage supply is critical.

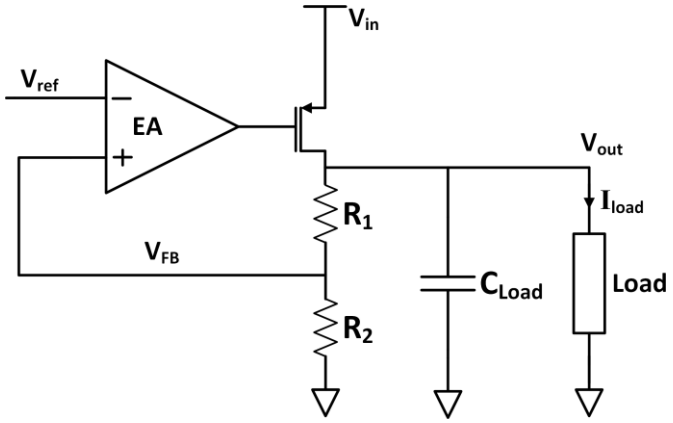

Figure 4.1: Linear Dropout Voltage Regulator Design.

BIST pre-amplifier functions to amplify and condition analog signals within a circuit by improving the signal-to-noise ratio. In addition to amplifying analog signals, it may also perform signal conditioning tasks such as filtering, offset correction, and gain adjustment. By incorporating these features, the BIST preamplifier contributes to the overall robustness and reliability of the BIST system, ensuring thorough testing coverage and accurate diagnosis of circuit faults.

The pre-amplifier is followed by a comparator, which acts as a decision-making component. It compares the amplified analog signal against a predefined threshold voltage, converting the analog signal into a digital output based on whether it exceeds this threshold. This process facilitates fault detection and analysis. Additionally, the comparator helps filter out noise and interference, ensuring accurate and reliable results.

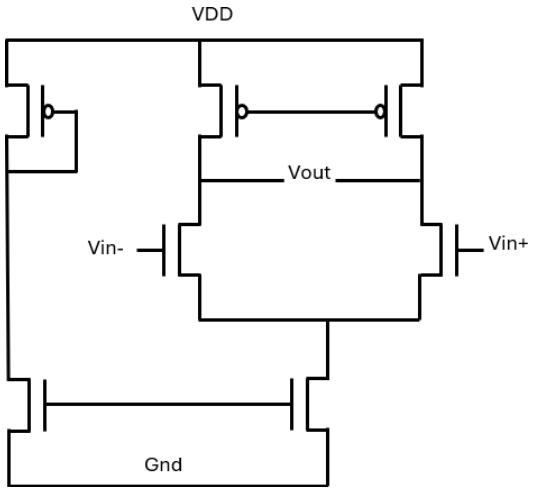

Figure 4.2: BIST Pre-amplifier

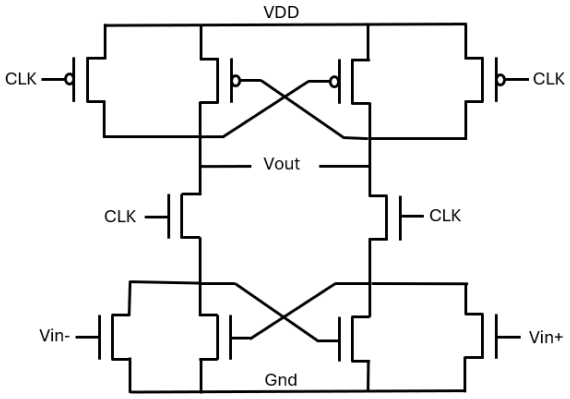

Figure 4.3: BIST Comparator

For the LDO, the injection point selected is the Vref node. Employing an on-and-off keying technique, this node is transiently pulled down from 1.2 volts to 0.7 volts. This perturbation is propagated throughout the circuit, extending to other nodes, including the output of the LDO, which serves as the observation point.

The observation circuit consists of a pre-amplifier and comparator. In normal operation, both nodes of the preamplifier are connected to the LDO output via switch S. Meanwhile, capacitor Co is charged to match the value of the LDO output. When

the perturbation is introduced, switch S is opened. Subsequently, the alteration in the LDO output and capacitor Co is directed to the preamplifier. The voltage difference is then amplified and transmitted to the comparator, which converts the analog output into a digital signal. Figure 4.4 shows the BIST circuit integrated with the LDO circuit.

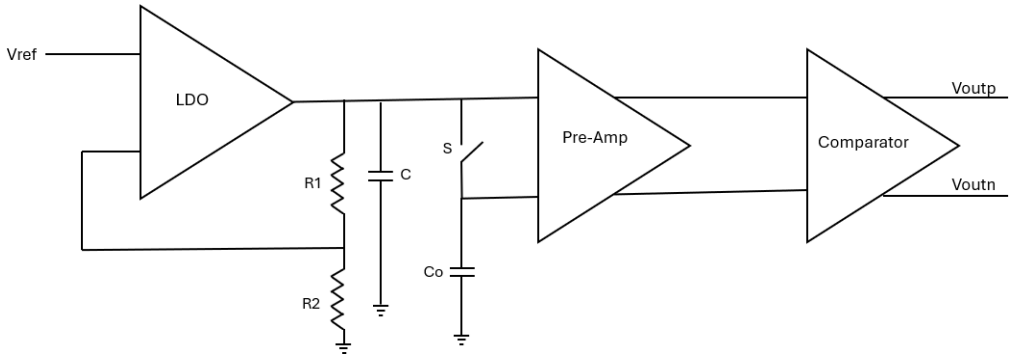

Figure 4.4: LDO Implemented with BIST Circuitry

The delay between the perturbation and the response in the LDO output is quantified. Monte Carlo simulations are conducted to accommodate process variations, and thresholds are set accordingly. Employing this approach, delays can be assessed post-fabrication and during field operations to identify potential defects or faults in the circuit.

4.2 Sallen-Key Filter

The LDO is a relatively straightforward analog circuit with a smaller number of transistors. Its operation is evaluated using transient analysis, which is also used for delay measurement in structural testing. Then we verify the methodology using a Sallen-Key filter, whose behavior is observed through AC analysis. Since delay is measured using transient analysis, the actual functioning of the circuit is not the primary concern in this context.

An ideal current source was employed in the LDO to produce biases, thereby reducing the potential for faults. In contrast, for the Sallen-Key filter, a fully transistor-level biasing circuitry was implemented to establish the operating points. This approach gives us a greater number of potential faults to be detected within the Sallen-Key filter.

The circuit designed is a 3rd-order Sallen-Key filter with a cutoff frequency of 10kHz. It utilizes two cascode amplifiers followed by a class AB stage. The circuit is comprised of four resistors and four capacitors, which help set the cutoff frequency of the filter. Sallen-Key filters are commonly employed in audio systems for shaping frequency responses and removing noise.

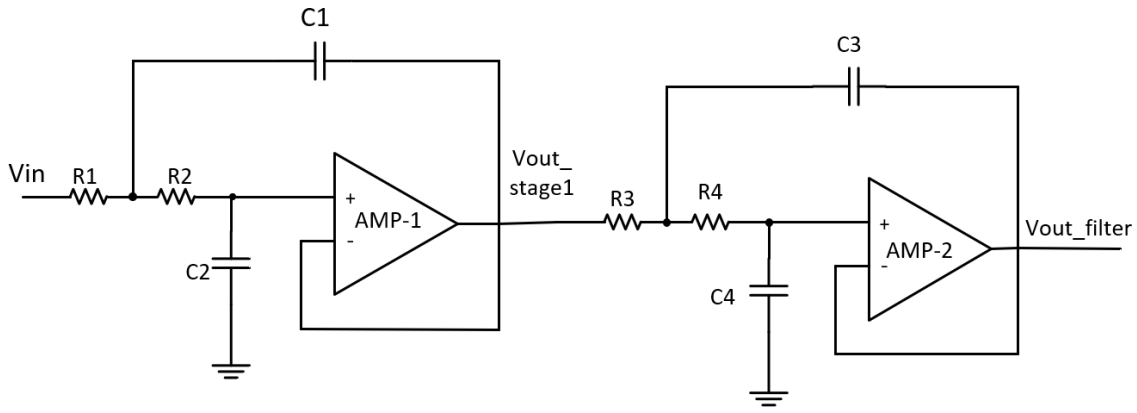

Figure 4.5: Circuit Diagram for Sallen Key Filter

Short-circuiting passive components to introduce stimuli are used as the first few injection points. The observation points selected are the output nodes of both the first and second amplifiers. Passive components are short-circuited to give six injection points. Among these, short-circuiting R1 and R2 constitute one injection point, while short-circuiting R3 and R4 constitute another. Additionally, the four capacitors serve as the remaining injection points. This helped detect 80% of the simulated faults. Most of the faults detected are in the amplifier, as the bias circuit is not directly connected to the output any faults or defects in the bias circuit are difficult to detect using passive components as injection points.

The bias circuit used in the folded-cascode amplifier consists of 6 different bias points. These six bias points could be disturbed to introduce perturbations to the circuit. Using bias points as infection nodes helps affect the circuit at multiple points at the same time that are connected structurally. Figure 4.6 shows the bias circuit used in the sallen-key filter.

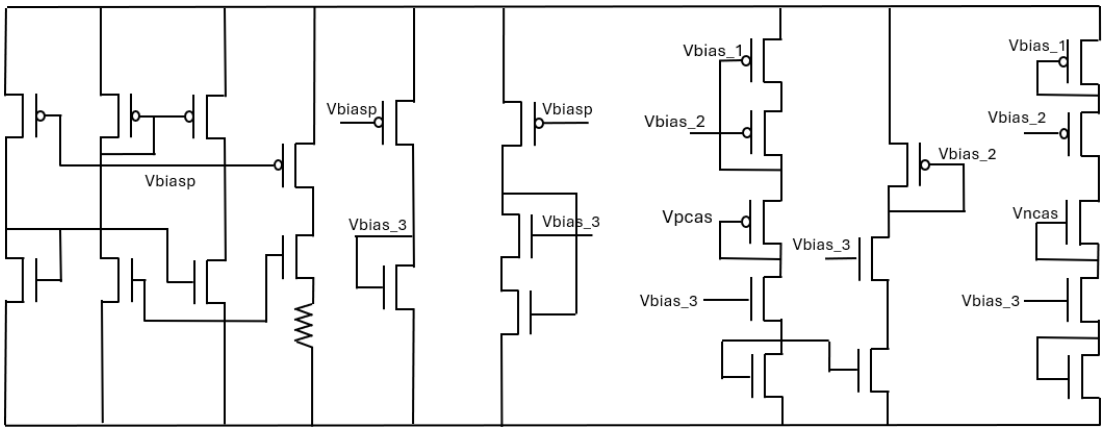

Figure 4.6: Bias Circuit for Cascode Amplifier in Sallen Key Filter

The six bias points that are disturbed to perturb injections are Vbiasp, Vbias_1, Vbias_2, Vbias_3, Vpcas, and Vncas. Each injection point requires only an additional

transistor, ensuring minimal overhead as only one extra transistor is needed for each injection point.

Either a PMOS or an NMOS transistor can be utilized for injecting a stimulus, based on which one induces a more significant perturbation. The NMOS transistor is grounded, while the PMOS transistor remains connected to Vdd to maintain normal functionality. When the test mode is activated, the NMOS transistor is pulled to Vdd, while the PMOS transistor is grounded to inject a stimulus. The injection circuitry makes up 0.01% of the BIST overhead.

Using the bias voltages as an injection point, we increase the fault coverage. However multiple copies of the same bias voltage used in each branch of the bias circuit make it difficult to detect faults in them.

Power gating is an alternative method to help detect faults in the transistors of the bias circuit. We can cut off the branch that contains the same bias circuit. This forces the other branch to set up the operating points on the amplifier. Biasing the voltages on that branch can help detect the faults in that branch.

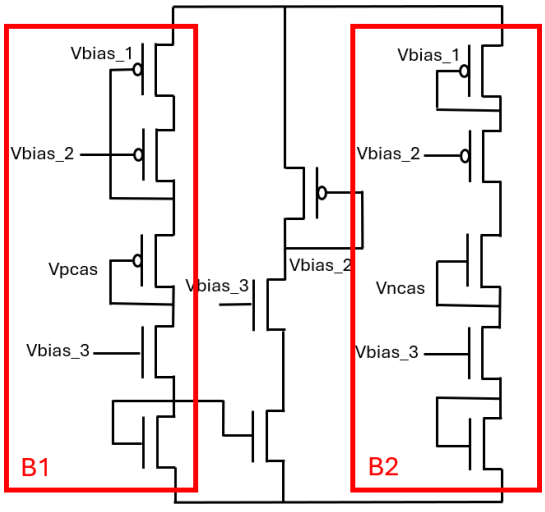

Figure 4.7: Branches with Similar Bias Voltages

Figure 4.7 illustrates two branches, B1 and B2, comprising an equal number of

transistors and nearly identical biases. If a fault occurs in B2, it may go undetected at the output since B1 assists in establishing the amplifier's operating points. To identify faults in B2, we can deactivate the B1 branch and pulse the bias points accordingly. B1 can be deactivated using two transistors one connected to VDD and the other two ground as shown in figure 4.8.

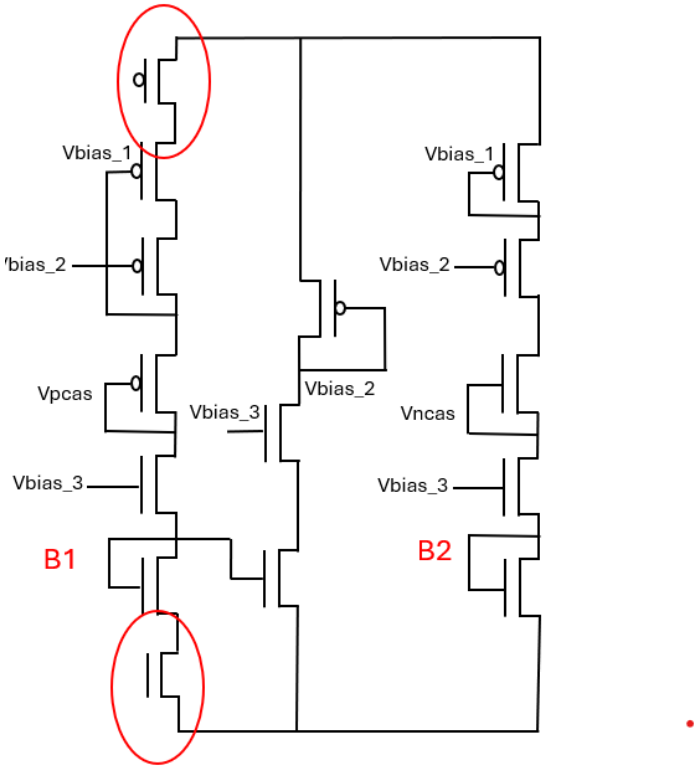

Figure 4.8: Power Gating Implementation

The power-gating transistors are going to be turned off by connecting them to VDD and ground. The bias points in B2 are injected to detect faults in the same branch. The undetected faults in the amplifier were also attributed to the presence of alternative current paths and the structural disconnection of certain transistors from the output. Figure 4.8 depicts

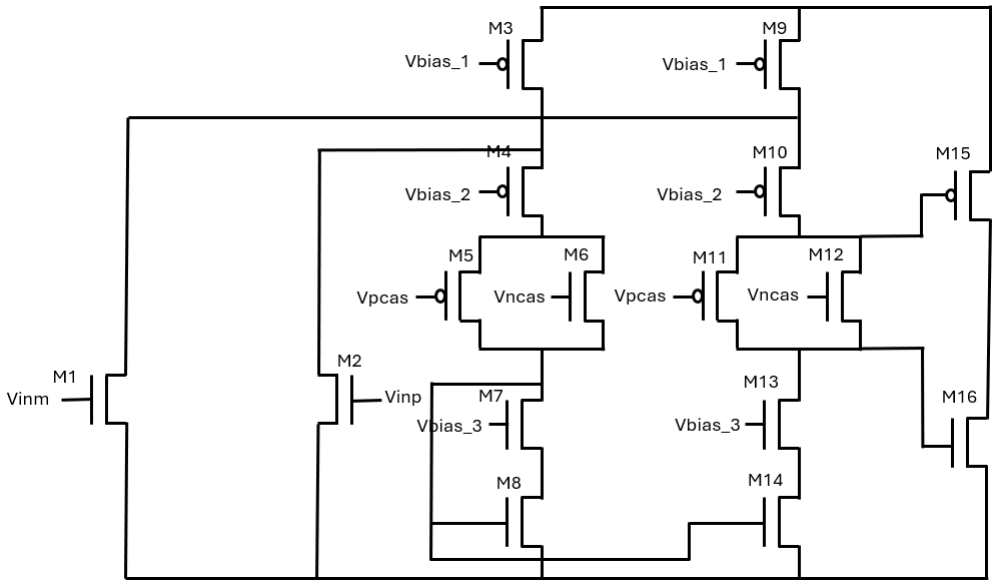

Figure 4.9: Folded-Cascode Amplifier Followed by a Class AB Stage

In the above circuit, the current passing through M3 and M5 has two alternative routes: one through the PMOS and the other through the NMOS (M5-M6 and M11-M12). Faults in M11 and M12 are detected because they bias the class AB buffer (M15 and M16). However, faults in M5 and M6 go undetected as their sole function is to ensure balanced currents in both branches for symmetry, and they lack structural or functional connection to the output.

To detect faults in a circuit with alternative current paths, the alternate paths must be disabled to ensure that the transistor with the fault becomes the sole path for current flow. If the circuit lacks a functional connection to the output, another internal node should be selected to observe the perturbation.

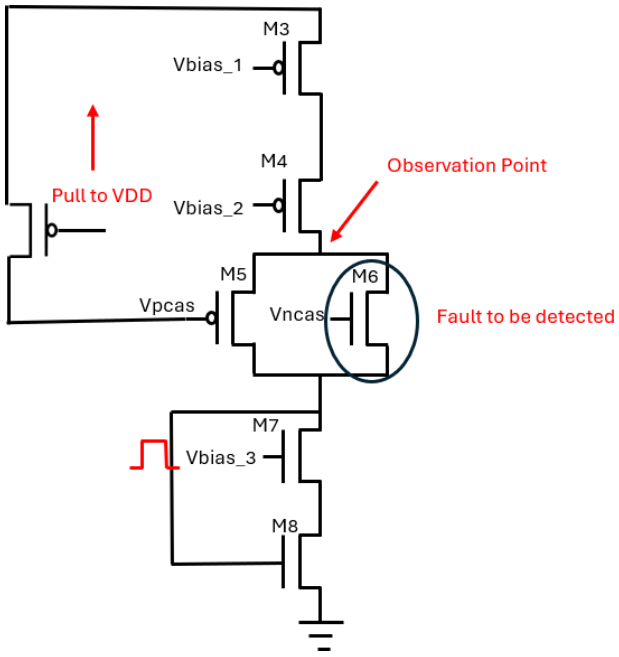

Figure 4.10: Circuit Implementation to Detect Faults in Alternate Current Paths

The depicted circuit illustrates a method for identifying faults in alternative current paths. To disable the alternate path, a transistor is connected to the gate of the transistor to be disabled. If it's a PMOS, it's pulled up to VDD, and if it's an NMOS, it's connected to the ground. In this case, a PMOS is linked to the gate of transistor M5, effectively disabling it. To introduce a perturbation, Vbias3 is disturbed. Since these circuits aren't linked to the output, the drain of transistor M4 serves as the observation point.

In conclusion, the injection points involve short-circuiting and disturbing bias points. Depending on the desired fault coverage, we can opt to enhance it by disabling alternate current paths and implementing power gating strategies.

4.3 Phase Locked Loops

As the methodology used depends on measuring time delay, it is important to make sure it works for high-speed circuits Phase-locked loops (PLLs) play a critical role in high-speed serializer/deserializer (SerDes) circuits, where they are employed for clock recovery and data synchronization. In SerDes systems, data is transmitted serially over a high-speed link, making precise clock recovery essential for accurate data reception. PLLs are used to recover the clock signal from the incoming data stream, ensuring proper timing alignment for reliable data recovery.

A Phase-Locked Loop (PLL) is a feedback control system used in electronics to generate stable output signals. It operates by comparing the phase of the output signal to that of a reference signal. The PLL continuously adjusts the phase and frequency of its output signal until it matches the input reference signal. This is achieved through a feedback loop consisting of a phase detector, a charge pump, a loop filter, and a voltage-controlled oscillator (VCO).

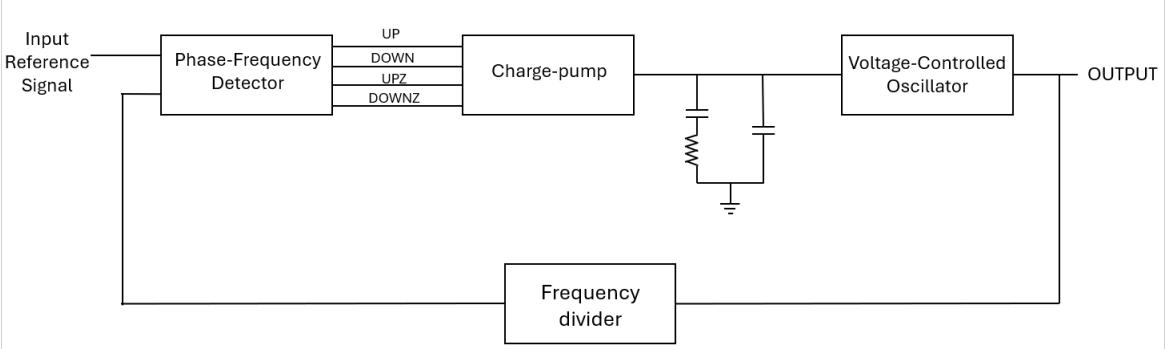

Figure 4.11: Phase Locked Loop Block Diagram

The phase detector first compares the phase of the output signal to the reference signal, producing an error signal that reflects their phase difference. This error signal

is then processed by the charge pump, which converts it into a variable analog voltage. The loop filter then removes all the high-frequency components of this voltage. Then the voltage-controlled oscillator produces a signal whose frequency is proportional to the voltage. As the loop iterates, the output signal of the PLL converges to the phase and frequency of the input signal, and this process is known as locking.

A Phase-Locked Loop (PLL) is a mixed-signal circuit, that seamlessly integrates both analog and digital functionalities. At its core, a PLL consists of analog components like the Voltage-Controlled Oscillator (VCO) and the loop filter, which work in harmony to generate stable output signals. On the other hand, digital elements such as the phase detector and digital control logic play pivotal roles in comparing phase differences and making fine adjustments to ensure precise synchronization. In this methodology, it is assumed that the digital components are addressed by Automatic Pattern Generation and scan techniques, while the focus is on detecting defects in the analog components.

Since the circuit is implemented in blocks, it is important to select injection and observation points strategically to maximize fault coverage. The most beneficial injection point would be the one that covers all the blocks from the input to the output.

The first injection point selected is the input to the phase-frequency detector, where the reference signal and the output of the frequency divider are compared. To preserve the integrity of the reference signal, which serves as the baseline, a transistor is connected to the output of the divider. This transistor can be perturbed after the locking process is completed.

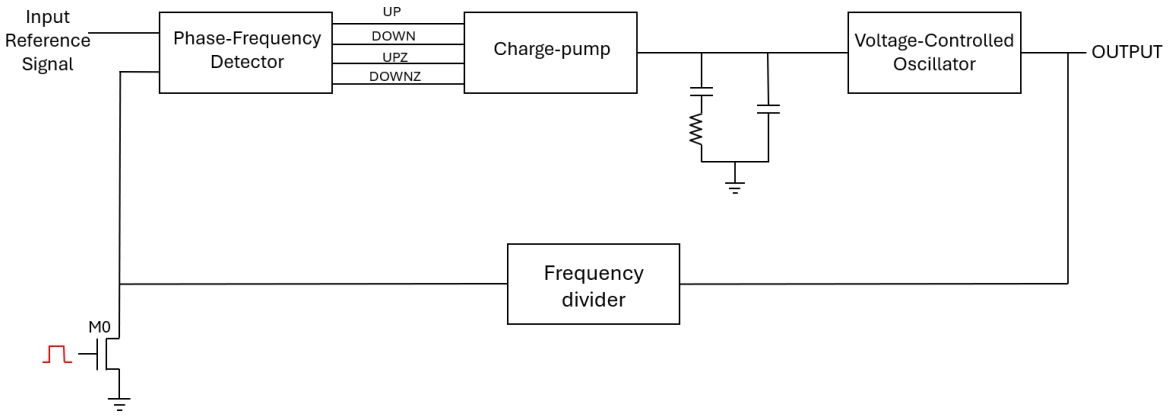

Figure 4.12: First Injection Point for the Phase Locked Loop

In Figure 4.12, M0 is linked between the output of the frequency divider and the ground. In regular operation, the gate of M0 is grounded, rendering the transistor M0 inactive since the gate-to-source voltage is zero. However, when the device enters test mode, the gate of M0 is raised to VDD, introducing a stimulus to be monitored at the output. It is crucial to recognize that injecting a stimulus into a Phase-Locked Loop completely interrupts its normal operation. Given that the output is disrupted, we can utilize the settling time as the measure of delay. This delay is subsequently employed to set limits and aid in characterizing faults.

Since the majority of undetected faults were found in the charge pump and the voltage-controlled oscillator, the second injection point is selected as the input of the charge pump. The delay is then measured between the stimulus and Vc (the output of the charge pump), as well as between the stimulus and the output. This ensures that both the VCO and charge pump are covered.

Transistor M1 is connected between between VDD and the output of the phase-

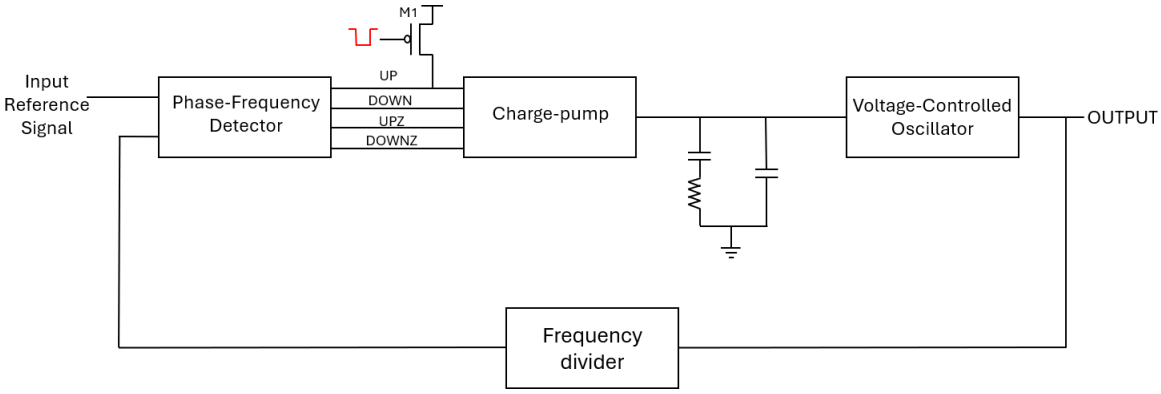

Figure 4.13: Second Injection Point for the Phase Locked Loop

frequency detector. During normal operation the gate of M1 is connected VDD, hence gate to source voltage is zero and the transistor M1 is off. When the circuit enters test mode, the gate of M1 is pulled to the ground to inject stimuli.

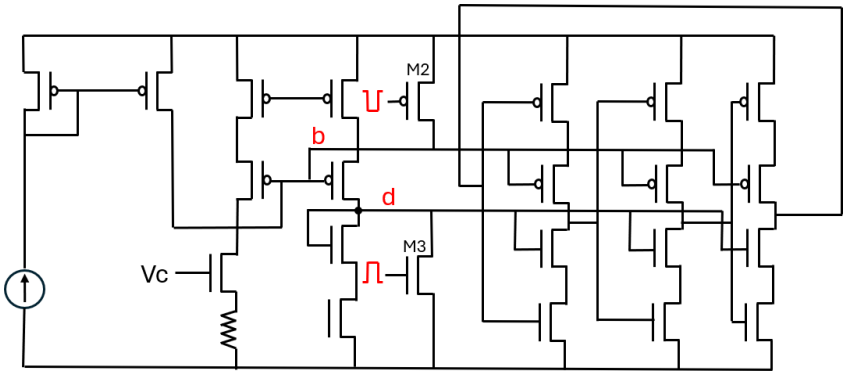

Figure 4.14: Bias Injection Points in Voltage Controlled Oscillator

The next two selected injection points are bias circuits, particularly within the Voltage-Controlled Oscillator (VCO), which comprises two bias points. These points are designated as the subsequent injection points. Despite being part of a closed-loop system, the effects of the stimulus near the output can still be observed in the

subsequent cycle. Figure 4.13 illustrates the next two injection points, the gate of the transistor M2 and M3.

By strategically selecting these points, we can effectively detect a wide range of faults, particularly those in critical components like the charge pump and voltage-controlled oscillator. The analysis of settling time as a measure of delay provides a robust framework for characterizing faults and establishing limits. Moving forward, these findings pave the way for enhanced fault detection strategies in integrated circuits, contributing to the overall reliability and performance of electronic systems.

Chapter 5

RESULTS

Fault coverage is a crucial metric in the field of integrated circuit testing, representing the extent to which potential faults in a circuit are detected by a testing methodology. It quantifies the effectiveness of the testing process in identifying and diagnosing faults, ultimately ensuring the reliability and quality of the circuit. High fault coverage indicates that a significant portion of potential faults, including both systematic and random errors, are successfully detected during testing. It is imperative to ensure that the methodology achieves industry-standard fault coverage to validate its viability. In this chapter, we are going to look at the fault coverage numbers and discuss the undetected faults.

5.1 LDO Results

The LDO is implemented with the BIST pre-amplifier and comparator. The LDO consists of 9 transistors, each transistor is simulated for 6 faults - drain open, gate open, source open, gate-source, drain-source short, and gate-drain shorts. We make sure not to simulate gate-source faults for diode-connected transistors. The preamplifier and comparator consist of 7 and 10 transistors respectively.

Figures 5.1 shows that the fault free delay for a perturbation. The fault free delay is 14.5us. Monte Carlo simulations are run for this delay and limits are computed. Figure 5.2 illustrate the response of a faulty circuit which shows a 25.125us delay. This delay lies outside the limits, hence this fault get detected

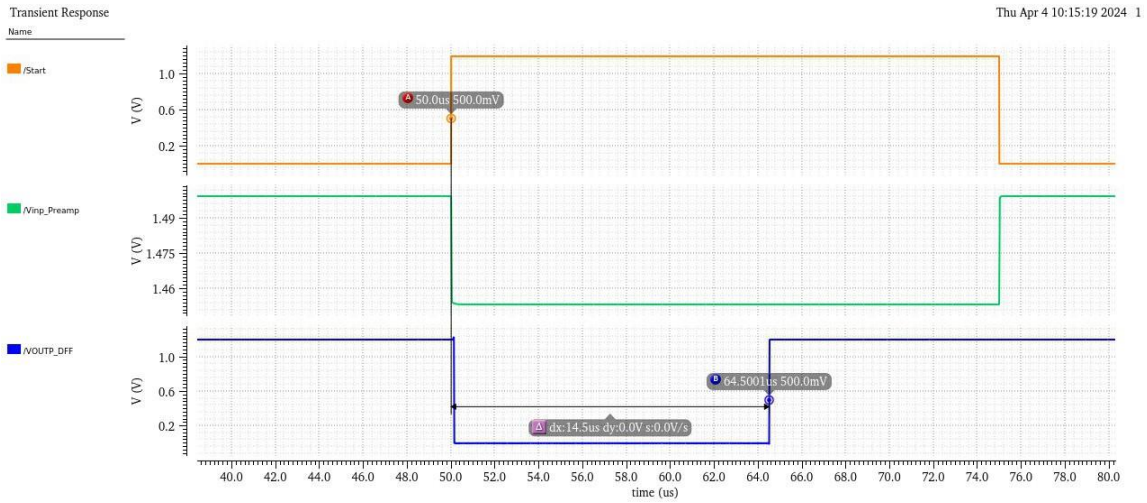

Figure 5.1: Reaction of a Fault-Free LDO circuit to Perturbation

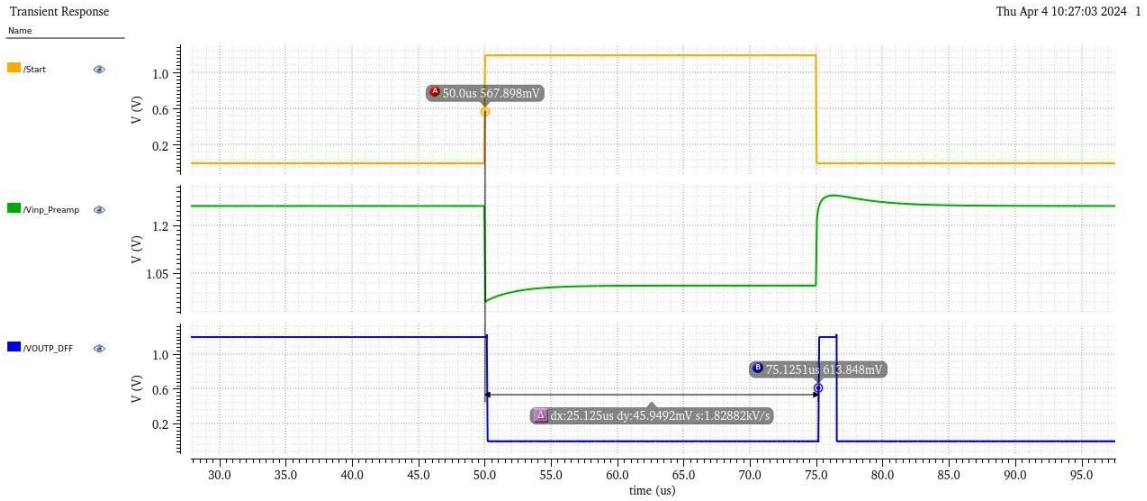

Figure 5.2: Reaction of a Fault-Free LDO Circuit to Perturbation

The same methodology is applied to detect faults in the preamplifier and the comparator. Using, a single observation point, the fault coverage for all three circuits - LDO, pre-amplifier, and comparator is documented in Table 5.1.

Table 5.1: Fault Coverage for Linear Dropout Voltage Regulator

type	simulated faults			detected faults			coverage
	total	shorts	opens	total	shorts	opens	
LDO	45	21	24	43	21	22	96%
BIST	98	47	51	90	43	47	92%
param	3	NA	NA	2	NA	NA	66%
Total	146	68	75	136	64	70	93%

The LDO Circuit has 4 undetected faults. The same methodology was applied to the BIST observation circuit as well. The coverage for the BIST observation circuit is 92%, Making the total as 93%.

The fault coverage is only for a single injection and observation point. This fault coverage can be increased by increasing the number of injection points.

5.2 Sallen Key filter Results

The Sallen Key filter consists of two folded cascode amplifiers that contain 42 transistors each, making the total 84 transistors. Figures 5.1 and 5.2 illustrate the response of a fault-free and a faulty circuit to perturbation respectively.

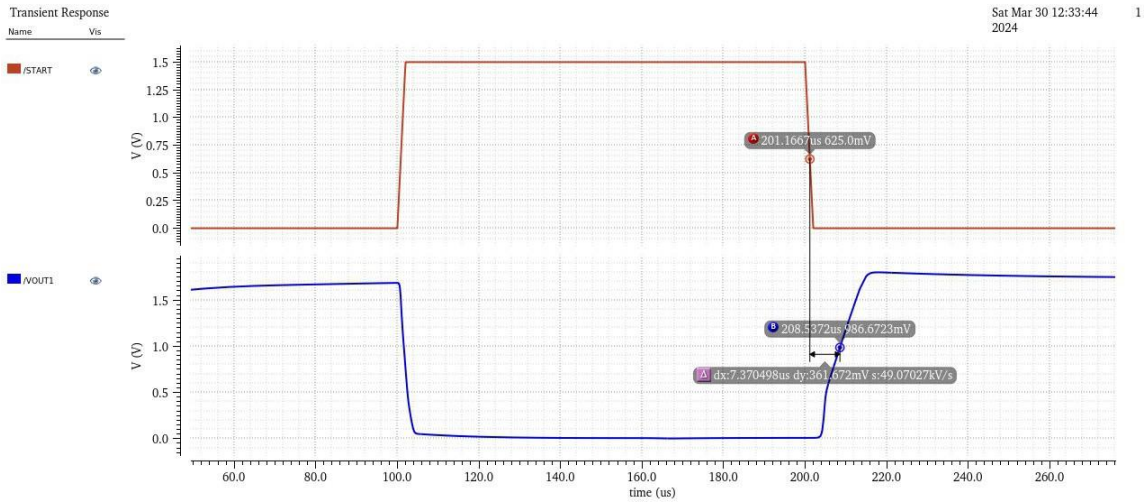

Figure 5.3: Reaction of a Fault-Free Sallen Key Filter to Perturbation

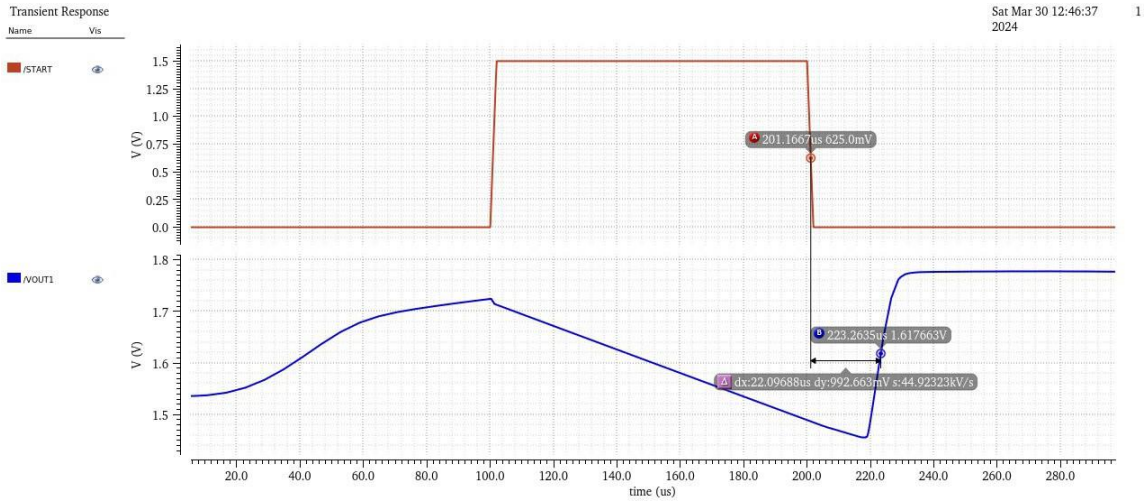

Figure 5.4: Reaction of a Faulty Sallen Key Filter to Perturbation

An algorithmic approach was utilized to enhance fault detection in the Sallen-

Key filter. The strategy involved augmenting the number of injection points and maintaining an ongoing tally of undetected faults. Adjustments to the injection points were made in response to the locations of these undetected faults. This systematic method led to the successful identification of all previously undetected faults, thereby significantly improving the fault coverage of the Sallen-Key filter. The final fault coverage for the Sallen Key filter is documented in Table 5.2.

Table 5.2: Fault Coverage for the Sallen-Key Filter

type	**simulated faults**			**detected faults**			**coverage**
	total	**shorts**	**opens**	**total**	**shorts**	**opens**	
Amp	170	68	102	166	68	98	98%
Bias	246	90	156	232	90	142	94%
Total	416	158	258	398	158	240	96%

Table 5.3 demonstrates the impact of incrementally adding injection points on enhancing fault coverage for the Sallen-Key filter.

A greedy approach was employed, whereby once a fault was detected, it was excluded from consideration for subsequent faults. This strategy suggests that some injection points might have contributed to even greater fault coverage if reassessed.

Table 5.3: Impact of Multiple Injection Points on Fault Coverage (Sallen-Key Filter)

Injection Points	Faults Detected	Total Faults Detected	Fault Coverage
1	320	320	76.9%
2	32	352	84.6%
3	14	366	88%
4	9	375	90.1%
5	8	383	92.1%
6	8	391	94%
7	4	395	95%
8	4	399	95.9%
9	3	402	96.9%
10	3	405	97.4%
11	2	407	97.8%
12	2	409	98.3%
13	2	411	98.8%
14	1	412	99%
15	1	413	99.3%
16	1	414	99.5%
17	1	414	99.8%
18	1	416	100%

5.3 Phase Locked Loops Results

Settling time is utilized as a key metric for identifying issues within PLL circuits. This metric specifically measures the time required for the circuit to stabilize and resume normal oscillation after experiencing a disturbance.

Figure 5.7 illustrates the phase-locked loop's settling time, capturing the period from the moment a disturbance is eliminated to the commencement of oscillations,

which is pinpointed at 295.8ps for a system without faults. Conversely, Figure 5.8 demonstrates a scenario where the presence of a fault prevents the onset of oscillations, leading to an immeasurable delay. Such an immeasurable delay serves as a clear indicator of a malfunction within the system.

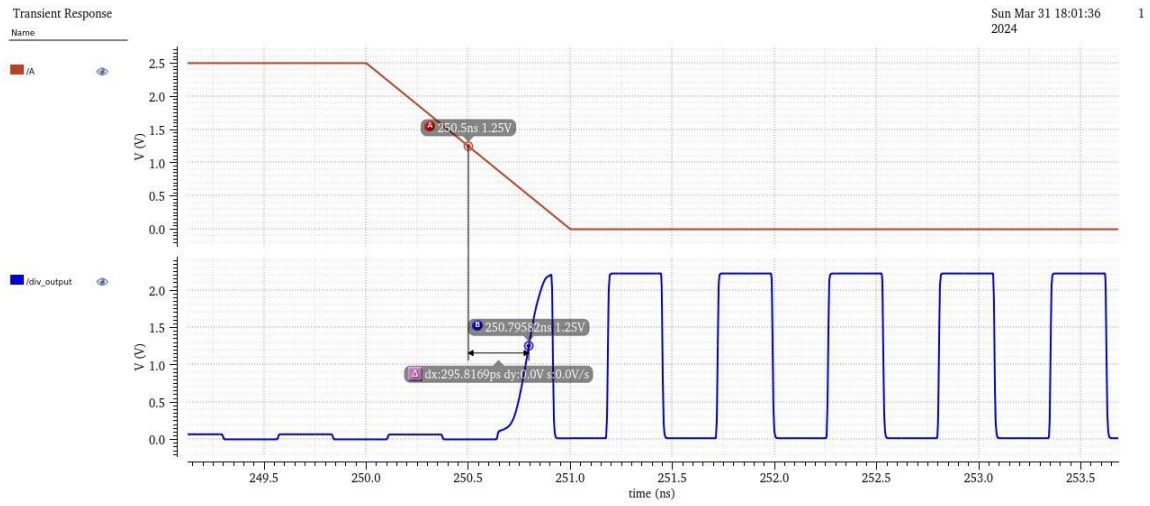

Figure 5.5: Settling Delay for a Fault-Free Phase-Locked Loop Circuit

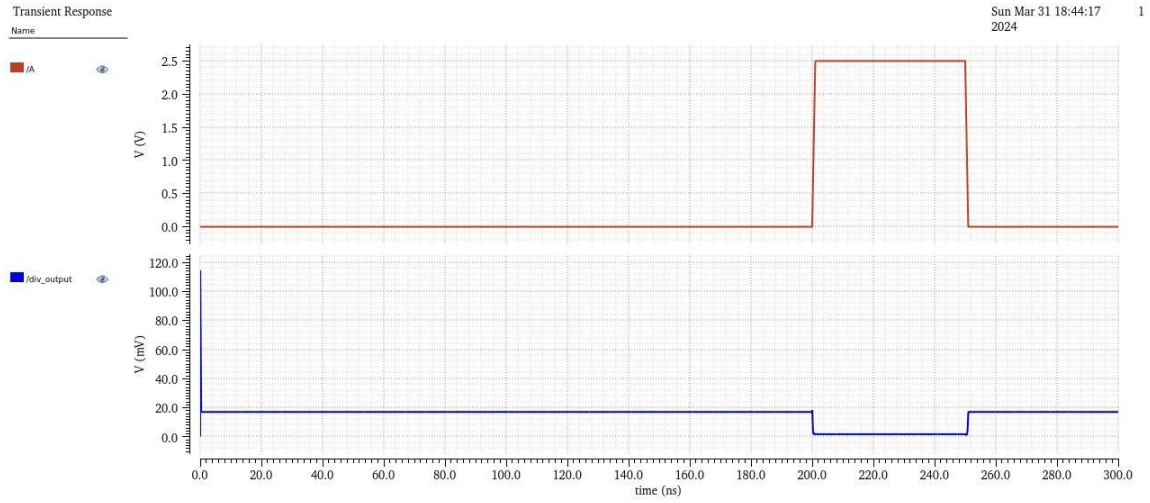

Figure 5.6: Settling Delay for a Faulty Phase-Locked Loop Circuit

To comprehensively evaluate the fault coverage within PLLs, a methodology involving 4 injection points and 2 observation points was employed. This approach

allows for a detailed analysis of the circuit's ability to detect and manage various fault conditions effectively.

Table 5.4: Fault Coverage for Phase Locked Loops

Type	Simulated Faults			Detected Faults			Coverage
	Total	Shorts	Opens	Total	Shorts	Opens	
PFD	12	6	6	12	6	6	100%
Charge Pump	36	18	18	34	17	17	94.44%
VCO	64	32	32	64	32	32	100%
Clock Divider	6	3	3	6	3	3	100%
Param Faults	9	NA	NA	9	NA	NA	100%
Total	118	59	59	116	58	58	98.31%

The fault coverage results reveal that all faults in the phase frequency detector (PFD), voltage-controlled oscillator (VCO), clock divider, and all parametric faults were detected using the implemented fault injection points. However, the charge pump exhibited 2 undetected faults, leading to a fault coverage of 94.44% for this component. Overall, the total coverage for the entire PLL circuit reached an impressive 98.31%, highlighting the effectiveness of the chosen methodology in identifying and assessing potential faults within the PLL design.

Chapter 6

CONCLUSION

6.1 Conclusion of Results

This work introduces a comprehensive methodology for the structural built-in testing (BIST) of analog circuits. The cornerstone of this methodology is its utilization of simple circuitry alongside a predominantly digital interface, leveraging ON/OFF keying of circuit components coupled with delay monitoring. This strategic approach not only simplifies the testing process but also enhances its efficacy, ensuring a robust evaluation of the circuit's integrity.

A distinguishing feature of the proposed methodology is its inherent low-cost nature, generic applicability, and scalability. These characteristics render the methodology highly adaptable across various circuit designs, making it an ideal candidate for widespread automation in the testing process. Such adaptability is crucial in today's rapidly evolving technological landscape, where the demand for versatile testing solutions is ever-increasing.

To validate the effectiveness of the proposed methodology, fault simulations were meticulously conducted on three experimental primary circuits: a Low-Dropout Regulator (LDO), a two-stage active filter, and a Phase-Locked Loop (PLL). These circuits were implemented using the cutting-edge TSMC 65nm technology, representing a broad spectrum of applications and complexities in modern circuit design. The results were remarkable, demonstrating over 95% of fault coverage for structural faults,

including resistive opens and shorts. This level of fault coverage is not only commendable but also surpasses that of previously proposed structural test methods, highlighting the superiority of the proposed approach.

One of the pivotal advantages of this methodology is its simplicity and cost-effectiveness in input injection. Such simplicity allows for the systematic enhancement of fault coverage by merely selecting additional circuit nodes for injection. This flexibility in enhancing fault coverage without incurring significant costs or complexities is a testament to the method's innovative design. It offers a scalable solution that can adapt to varying circuit complexities and requirements, ensuring comprehensive fault detection and diagnosis.

In conclusion, the methodology presented in this work represents a significant leap forward in the domain of analog circuit testing. By combining simplicity with efficiency, cost-effectiveness with scalability, and generic applicability with high fault coverage, this method sets a new benchmark for structural BIST approaches. It paves the way for more reliable, versatile, and accessible testing solutions that can keep pace with the rapid advancements in circuit design and technology.

6.2 Future Work

For the proposed methodology to achieve full automation, it's imperative to develop an algorithmic strategy to identify potential injection and observation points within the circuit systematically. This entails adopting a top-down approach, beginning with a comprehensive system-level analysis. Such an approach would involve scanning the entire system to evaluate fault coverage comprehensively. Should the

initial coverage assessment fall short of expectations, the focus would then shift to scrutinizing the internal blocks more closely.

The crux of enhancing this methodology lies in the strategic selection of injection points. The goal is to pinpoint these locations with precision, prioritizing those that promise the highest fault coverage. This optimization process is crucial for maximizing the efficiency of the testing process, ensuring that the most critical areas of the circuit are thoroughly examined.

By harnessing these algorithms, the vision is to streamline the process of stimulus injection and fault detection, thereby achieving a fully automated testing process. This automation would not only expedite the testing procedure but also increase its accuracy and reliability. The ability to systematically navigate through the circuit—from a broad system-level overview to the nuanced examination of internal blocks—ensures a meticulous and comprehensive testing framework. This strategic approach lays the groundwork for a more efficient, accurate, and fully automated method of circuit testing, revolutionizing the way analog circuits are verified and validated.

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