Transceiver Architectures with Wireless Synchronization

by

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ABSTRACT

Advancements in technologies like the Internet of thing causes an increase in the presence of wireless transceivers. A cooperative communication between these transceivers opens a doorway for multiple novel applications. A mobile distributed transceiver architecture is a much more dynamic environment dictating the necessity of faster synchronization among the transceivers.

A possibility of simultaneous synchronization in parallel with the communication will theoretically ensure a high-speed synchronization without affecting the data rate. One such system has been implemented using a Costas loop and an extension of such synchronization technique to the full-duplex model has also been addressed. The rise in spectral demand is hard to meet with the regular Time duplex and frequency duplex communication systems. A full-duplex system is theoretically expected to double the spectral efficiency. However it comes with tremendous challenges, This thesis works on one of those challenges in implementing full-duplex synchronization.

A coherent full-duplex model is designed to overcome the issue of transmitter leakage modeled as injection pulling, A known solution for this effect has been used to resolve the issue and complete the coherent full-duplex model. This establishes the simultaneous synchronization and communication system.

DEDICATION

Dedicated to my parents Krishna Dhulipala, Sarada Devi Challa, to my dear sister Sindhura Dhulipala and all my friends. I am grateful to Prof. Saeed Zeinolabedinzadeh for his teachings on Radio frequency design and support during the research

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INTRODUCTION

1.1 Distributed Transceiver Systems and Synchronization

Distributed transceiver architecture is a type of cooperative communication in which multiple transceivers send a common message at the same time and manage the phase of their transmissions so that the signals combine constructively at their destination[12]. However, coordinating the sources is a major barrier in achieving these benefits. Information sharing and synchronization of timing, as well as, most importantly, distributed carrier synchronization, such that the transmissions work together in a better way.

In traditional wireless systems, for an efficient communication, several temporal, spectral and spatial techniques are used. A transceiver is a device typically used in Frequency Division Duplexing that encompass both a transmitter and a receiver operating simultaneously. A conventional transceiver use different frequencies for transmission and reception. A full duplex system is by definition expected to ensure communication in both directions to be on same frequency.Such type of a system doubles the spectral efficiency over the same resources[5]. These eminent properties of full duplex transceivers made them a reliable means for distributed radio network[6].

The main topic of this research is on developing a high speed synchronization technique, where all the transceiver get synchronized while communicating with each other.

1.2 Methods of Synchronization

In 1932 while proposing the first model of a Phase locked loops, Bellescize, French engineer introduced synchronous detection theory and in early 60's viterbi introduced the principle of coherent communication[16]. An Rf receiver with a property of being frequency synchronous with the received signal carrier is called a coherent receiver. In a transmitter and receiver pair the transmitter dictates the modulation frequency and a coherent Receiver is expected to follow all the frequency variations in the carrier used by that transmitter.

This synchronization of carrier frequency among the transceivers can be achieved using several techniques both in analog and digital domains of the transceiver. However, when we aim to ensure the synchronization in mobile transceivers, it causes an entirely dynamic environment. Consider, two transceivers moving apart from each other. When they try communicating with each other the frequency they receive from each other gets shifted because of Doppler effect. In order to establish synchronization even in these circumstances there is a requirement of high speed synchronization. Keeping this in mind and in order to maintain low latency in synchronization digital domain synchronization has to be avoided as by the time the correction signal gets generated the frequency might get even more shifted. Hence, an analog domain synchronization has been preferred for the distributed transceiver architecture in this thesis.

The well known synchronization techniques can be categorized into two types[12]

- **Closed loop**: When multiple transceivers trying to communicate to a single destination, all of them will be maintained in sync by the destination. The inter communication is minimized among the source transceivers
- **Open loop**: The destination sends out a beacon of unmodulated carrier and all

the sources lock to the carrier communicating among themselves when necessary

In either of the techniques there is a necessity of coherent transceivers where they can both communicate and synchronize with the incoming carrier

1.3 Motivation and Challenges

In order to address the need for developing a high speed low latency synchronization technique. This thesis focus on developing a simultaneous synchronization and communication technique in analog domain to maintain the data rate during synchronization. The thesis also aims to extend the design to a full duplex synchronization architecture over coming its limitations like internal frequency pulling. Developing a full duplex system in coherent transceivers is found to have major applications like Internet of Things. However, they are expected to cause the majority challenge in design. A Costas loop is being used, for coherent detection and simultaneous communication in this research, causing the Voltage Controlled Oscillator (VCO) to operate in the carrier frequency which in turn will be used for modulating the transmitting signal.

As discussed in the previous subsection after being modulated the transmitted signal tends to pull the VCO out of its operating frequency, there by dropping the effective reception and synchronization of the transceiver.

In short, the major contributions of this work are as follows:

- Developing a Simultaneous Synchronization and Communication technique for BPSK communication using Costas loop
- Design of an LC Voltage controlled oscillator and modeling it for injection pulling.

- Proposed a solution to alleviate the issue of Local Oscillator pulling for coherent detection
- Performed experimental comparative analysis on the impact of the the solution on synchronization and communication.

1.4 Thesis Organisation

The rest of the thesis is organised as follows, Chapter 2, discusses the background information of the modulation scheme that has been implemented and its mathematical properties along with the transceiver architecture model and its various parts with their functions that were considered. Chapter 3 involves a development of coherent detection. It also discusses the design and working of costas loop as a coherent detector. Chapter 4 goes over the challenge in designing a coherent receiver in a full duplex system and modeling of injection pulling, which will be extensively studied.The practical implementations of all the concepts in a developing sequence towards the transceiver model design including the effect of injection pulling and its solution being implemented with their effect on the transceiver function are studied. Finally chapter 5 discusses the observations through the study and possibilities of future work with suggested improvements of the existing design.

Chapter 2

TRANSCEIVER DESIGN

2.1 Transceiver Models

Multiple Distributed Transceiver Architecture: The distributed transceiver model shown in Fig.2.1 is the expected design out of this thesis. It involves a Full duplex master transceiver which dictates the operating frequency and multiple slave transceivers which follow the master's instruction[11]. All the slave transceivers are expected to get synchronized to the carrier transmitted by the master while simultaneously communicating, with each other or with the master. Each of the master and slave are explained in the following parts of the sub-section.

Master Transceiver model: Fig.2.2 describes the architectural model of the master transceiver. It consists of a configurable master local oscillator(LO) operating at the transmitter's will. Usually these LOs are made up of phase locked crystal oscillators which are considered to be extremely stable and easily configurable using digital controlled dividers. For a full duplex transceiver, the receiver module is also operated on the same master LO at the same frequency. The obvious challenge of a full duplex transceiver is considered to be the self interference of the strong transmitted signal from its own transmitter. With several self interference cancellation techniques, like LMS FIR filter cancellation, we are neglecting this issue and considered this in future work. The data that has to be transmitted is generally pulse shaped in order to conserve the energy over bandwidth. Using the master LO this pulse shaped data is encoded and transmitted using direct conversion BPSK modulation technique. The simple receiver structure in it is expected to directly convert (demodulate) into a

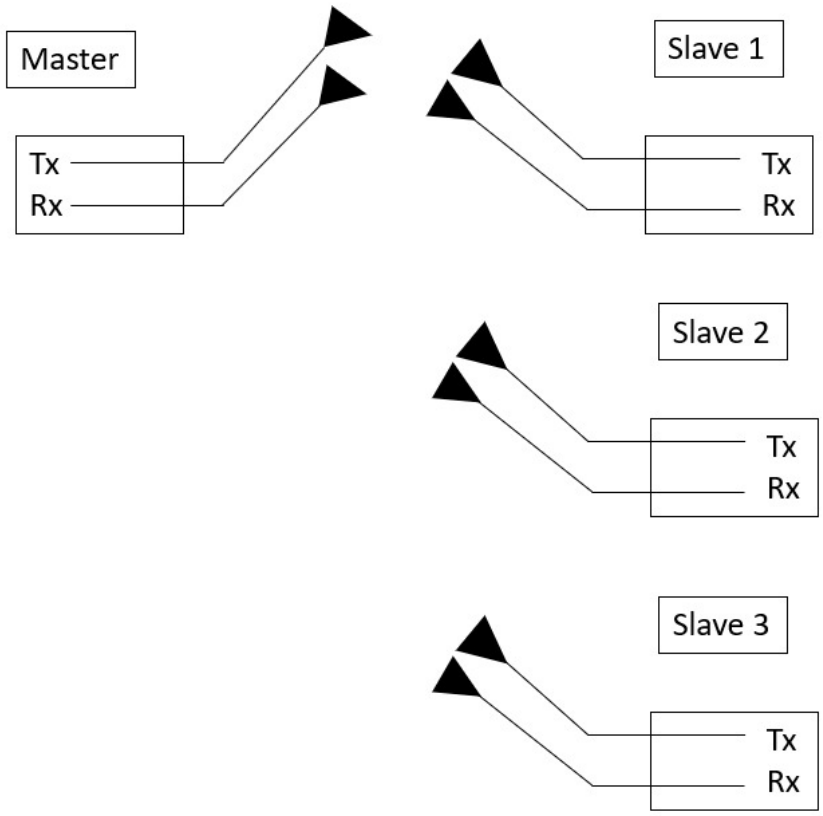

Figure 2.1: Distributed Transceiver Architecture

message signal .

Slave Transceiver model: The slave is expected to follow the master's operating frequency. In order to ensure that a coherent detector is used which estimates the received frequency and shifts the slave's LO operating frequency. Further this modified LO frequency is used for demodulating the received signal as shown in Fig.2.3. Once the LO frequency is set to the current operating value, the slave transmitter can use this frequency for modulating the baseband signal that has to be transmitted. This transmitter operates similar to the one as of the master transmitter, the data pulses are pulse shaped and BPSK modulated.

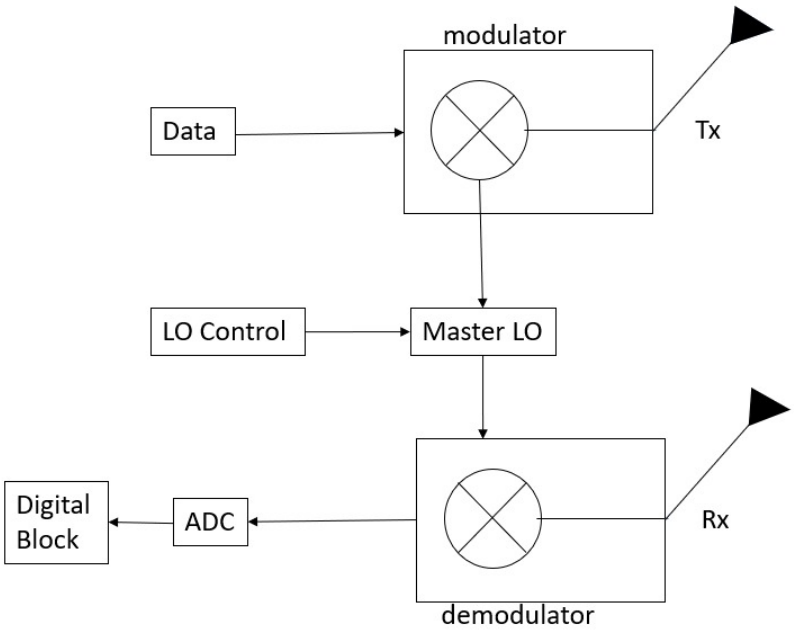

Figure 2.2: Master Transceiver Architecture

2.2 BPSK Modulation and Demodulation

Binary phase shift keying (BPSK) is a phase modulation technique in which the message bits shift the carrier between 0 and 180 degrees phases. As demonstrated in the Fig.2.4,this can be accomplished via analog multiplication of bipolar base-band to the RF carrier. The resultant modulated output can be represented as:[1]

$$b(t) = \sum_{l=-\infty}^{\infty} b_l P_T(t - lt), \qquad b_l \in \{+1, -1\}$$

The bipolar encoded message signal $b_(t)$ maps bit 1 to +1V and bit 0 to -1V. $P_T(t)$ is the function of a pulse given as follows: f_c indicates carrier frequency and

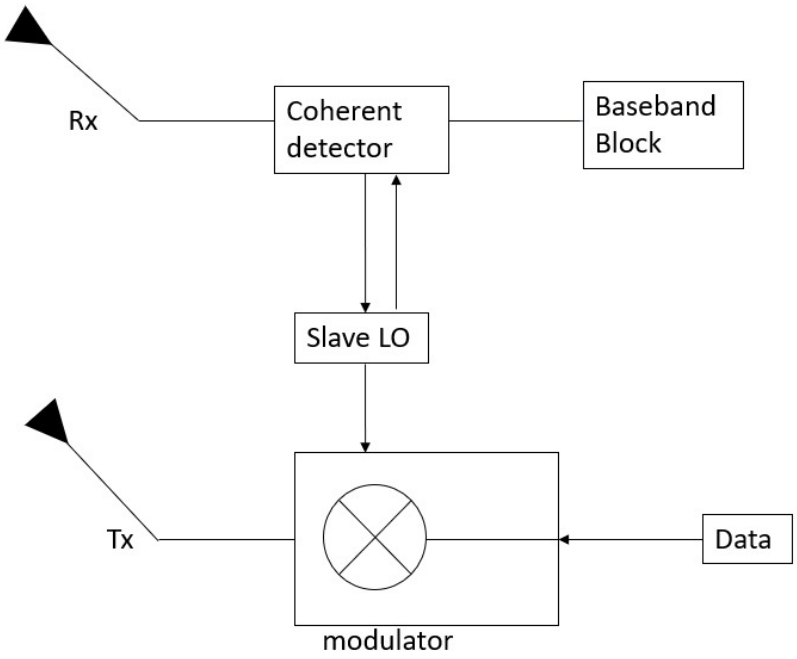

Figure 2.3: Slave Transceiver Architecture

$P_T(t)$ represents the function of a pulse given as follows:[1]

$$P_T(t) = \begin{cases} 1, & 0 \leq t \leq T \\ 0, & otherwise \end{cases}$$

The BPSK modulated signal is given by:

$$s(t) = \sqrt{2P}(cos2\pi f_c t + \Phi(t))$$

Where $\Phi(t)$ denotes the phase waveform displayed in Fig. The signal power is P, and each bit's energy is $E = P_T$.

Demodulation:The best receiver for BPSK in the presence of additive white Gaussian noise is shown in Fig.[2.3]. The low pass filter (LPF) is a filter that is "matched" to the baseband signal that is being sent. In BPSK, this is simply a rectangular pulse with duration T. $h(t) = P_T(t)$ is the impulse response. The low pass filter's output[1]. The sampled version of the output is given by[1]

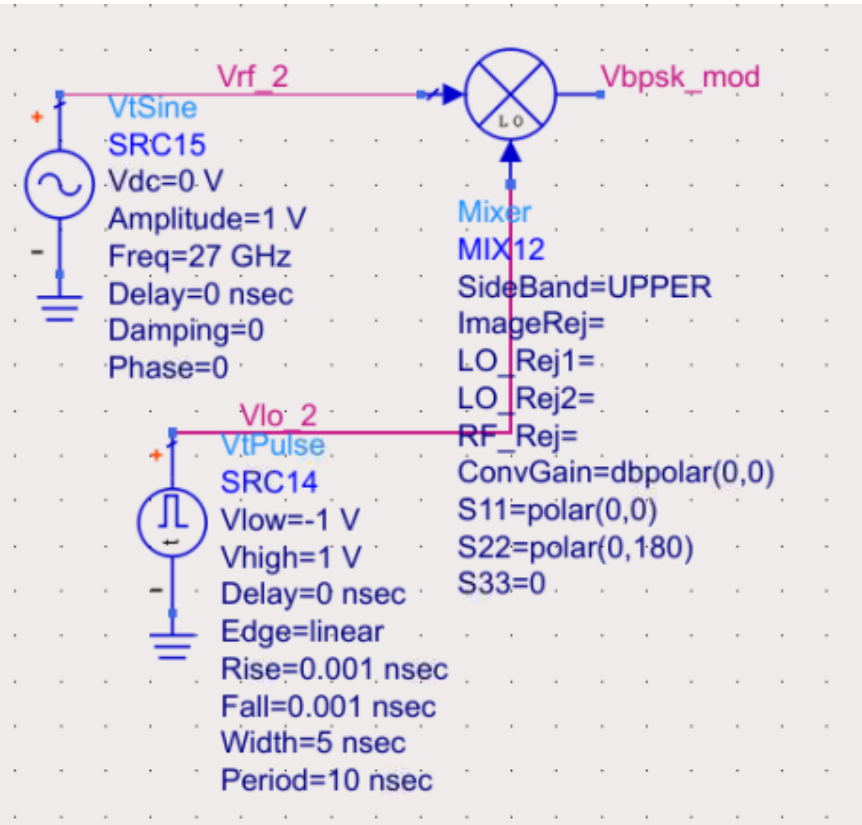

Figure 2.4: BPSK Modulator.

$$X(iT) = \int_{-\infty}^{\infty} 2\sqrt{2P/T}b_i - 1cos(2\pi f_c\tau)cos(2\pi f_c\tau)d\tau + \eta_i$$

ηi is a Gaussian random variable with a mean of zero and a variation of N0/2. For some integer n, assume $2\pi f_c T = 2\pi n$(or that $f_c T >> 1$).

$$X(iT) = \sqrt{PT}b_i - 1 + \eta_i = \sqrt{E}b_i - 1 + \eta_i$$

Bit Error Probability of BPS

$$p_e, b = Q(\sqrt{2E/N_0}) = Q(\sqrt{2E_b/N_0})$$

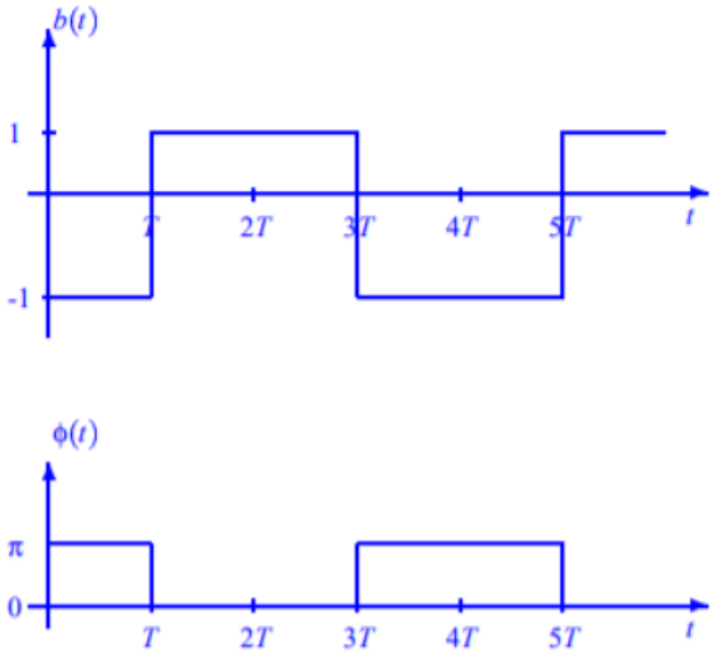

Figure 2.5: Phase Waveform.[1]

Where

$$Q(x) = \int_x^\infty \frac{1}{2\pi} e^{\frac{u^2}{2}} du$$

This is the least bit error probability for binary signals, i.e. BPSK transmissions are ideal, and the receiver illustrated above is optimal (in additive white Gaussian noise). The energy transmitted each information bit E_b in binary signals is the same as the energy transmitted per signal E. We need a bit-energy, E_b to noise density, N_0 ratio of $9.6dB$ for $P_{e,b} = 10^{-5}$. Note that for $x = 0$, $Q(x)$ is a declining function that is $1/2$. There are efficient procedures for calculating $Q(x)$ that use Taylor series expansions. The error probability can be higher bounded by $Q(x) \leq e^{-x^2/2}/2$ since $Q(x) \leq e^{-x^2/2}/2$.

$$P_{e,b} \leq \frac{1}{2} e^{-E_b/N_0}$$

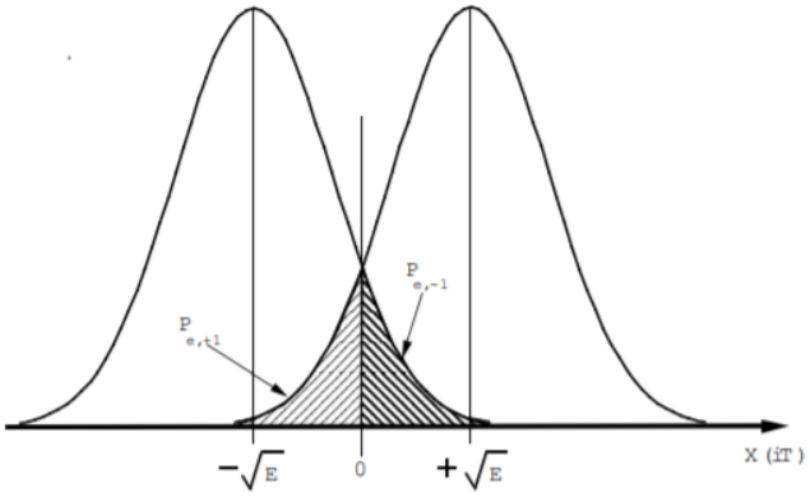

Figure 2.6: Probability Density of Decision Statistic for Binary Phase Shift keying.[1]

which decreases exponentially with signal-to-noise ratio.

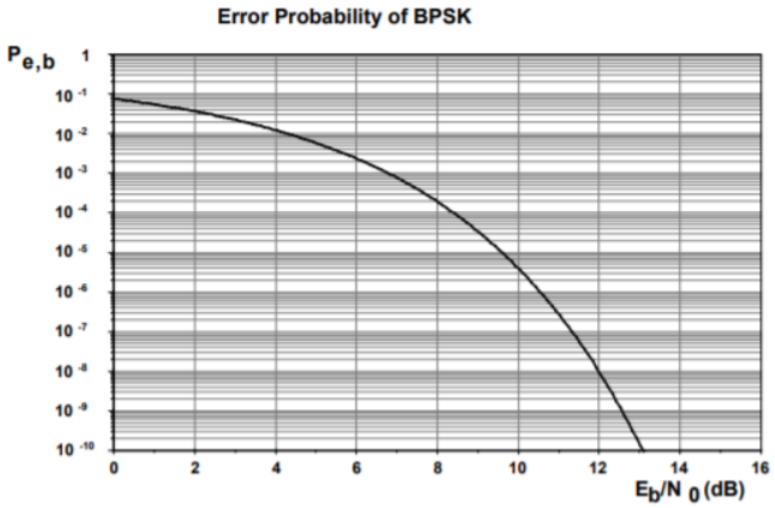

Figure 2.7: Error Probability of BPSK[1]

Bandwidth of BPSK The power spectral density is a measurement of the power distribution in terms of frequency.

The power spectral density for BPSK has the form

$$S(f) = \frac{PT}{2}[sinc^2((f - f_c)T) + sinc^2((f + f_c)T)]$$

Where

$$sinc(x) = \frac{sin(\pi x)}{\pi x}$$

Notice that

$$\int_{-\infty}^{\infty} S(f)df = p$$

Except for $i = 0$, the power spectrum has zeros or nulls at $f - fc = i/T$; that is, the first null is at $f - fc = pm1/T$, the second null is at $f - fc = pm2/T$, and so on. The null-to-null bandwidth is the distance between the first nulls. The null-to-null bandwidth in BPSK is $2/T$. As f goes away from f_c, the spectrum falls off as $(f - f_c)2$. (The spectrum of MSK goes off as the fourth power, whereas the spectrum of BPSK falls off as the second power.)

Filtering can be used to lower the bandwidth of a BPSK signal. If the filtering is done correctly, the signal's (absolute) bandwidth can be decreased to 1/T without creating inter-symbol interference; this means that all of the power is concentrated in the frequency range.

$-1/(2T) \leq |f - f_c| \leq 1/(2T)$ The signal loses its constant envelope property (which is important for nonlinear amplifiers) and is much more sensitive to timing faults as a result. Filtering to a little wider bandwidth can considerably reduce the timing sensitivity problem. $-(1 + \alpha)/(2T) \leq |f - f_c| \leq (1 + \alpha)/(2T)$

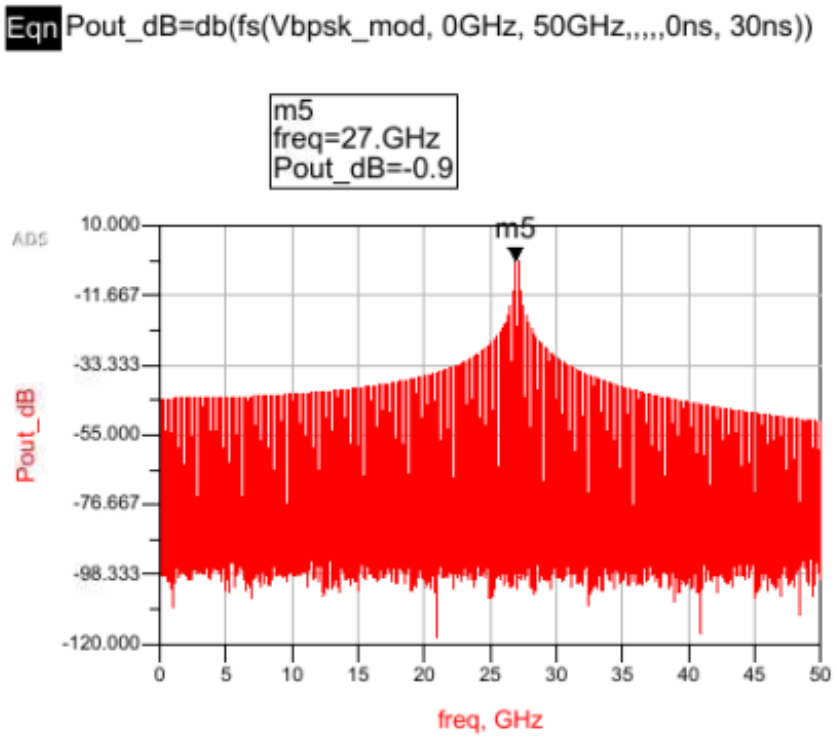

Figure 2.8: Spectrum of BPSK

Chapter 3

COHERENT DETECTION

3.1 Analog PLL Design

When it comes to synchronizing two oscillators a PLL is widely known application for the requirement. A PLL is a looped feedback system that ensures a reference and a local oscillators to stay in phase sync. It contains a VCO, phase detector, and low pass filter. When the VCO is in lock, it is forced to repeat and track the frequency and phase of the reference. PLL stands for phase lock loop, and it is a control method that allows one oscillator to track another. It is possible to have a phase difference between the input and output, but the frequencies must track exactly when locked.

$$\phi_{out}(t) = \phi_{in}(t)const$$

$$\omega_{out}(t) = \omega_{in}(t)$$

Depending on the application, the PLL output can be derived from either V_{cont}, the filtered (nearly DC) VCO control voltage, or the VCO output. The former generates a baseband output that tracks the input phase variation. The VCO output can be used to provide a clock signal for a digital system or as a local oscillator. The input or output variables can be either phase or frequency.

Naturally, phase and frequency are linked by:

$$\omega(t) = \frac{d\phi}{dt}$$

$$\phi(t) = \phi(0) + \int_0^t \omega(t^1)dt^1$$

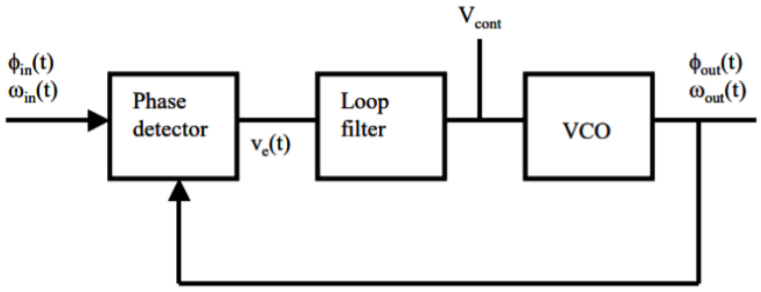

Figure 3.1: Phase Locked Loop.[2]

Phase detector: checks the phase of each input and outputs a $v_e(t)$ error signal proportionate to the phase difference between the two inputs. The phase detector's gain (V/rad) is K_D.

$$v_e(t) = K_D[\phi_{out}(t) - \phi_{in}(t)]$$

An analog multiplier or mixer can be used as a phase detector, as one well-known circuit example. Keep in mind that the mixer takes the sum of two inputs. $v_e(t) = A(t)B(t)$ If

$$A(t) = Acos(\omega_0 t + \phi_a)$$

$$B(t) = Bcos(\omega_0 t + \phi_b)$$

Then

$$A(t)B(t) = (AB/2)[cos(2\omega_0 t + \phi_A + \phi_B] + cos(\phi_A - \phi_B)]$$

We have one output at twice the input frequency and one output proportionate to the cosine of the phase difference since the two inputs are at the same frequency when the loop is locked. The lowpass loop filter must eliminate the doubled frequency component. After filtering, any phase difference appears as the control voltage to the VCO, a DC or slowly changing AC signal.

The VCO is handled as a linear, time-invariant system in PLL applications. The system output is the VCO's excess phase.

$$\phi_{out} = K_O \int_{-\infty}^{t} V_{cont} dt^1$$

The VCO oscillates at ω_{out} angular frequency. When the control voltage is zero, the frequency is set to a nominal ω_0 . With a gain coefficient of K_O or K_{VCO} (rad/s/v), frequency is assumed to be linearly proportional to the control voltage.

$$\omega_{out} = \omega_0 + K_O V_c ont$$

Lock range. After capturing the input signal, the loop remains locked over a range of input signal frequencies. The phase detector or the VCO frequency range can also limit this.

a. If limited by phase detector:

The active range where lock can be maintained is $0 < \phi < \pi$. The voltage v_s. phase slope flips outside this range for the phase detector type specified (Gilbert multiplier or mixer). As a result, the frequency would shift in the opposite direction of that required to keep the locked state.

$$V_{c-max} = \pm K_D \pi/2$$

The phase detector output voltage is applied to the VCO through the loop filter.

$$\Delta\omega_{out-max} = \pm K_V \pi/2 = \omega_L$$

where $K_V = K_O\ K_D$ is the product of the phase detector and the VCO gains. This is the frequency range that the loop can follow around the free running frequency. It is independent of the loop filter and depends on the gain of the DC loop.

b. The tuning range of the VCO could also limit the lock range. The tuning range of an oscillator is restricted by capacitance or current ratios and is finite. In many

circumstances, the maximum lock range can be set by the VCO.

Capture range: When starting from an unlocked state, the loop will lock onto a range of input frequencies around the VCO centre frequency. Alongside aid in the early acquisition of lock, a frequency detector is sometimes added to the phase detector.

Frequency and phase tracking loop:

We'll start with a PLL with feedback = 1, which means the input and output frequencies are the same. The input and output phases should match, however depending on how the phase detector is implemented, there may be a fixed offset.

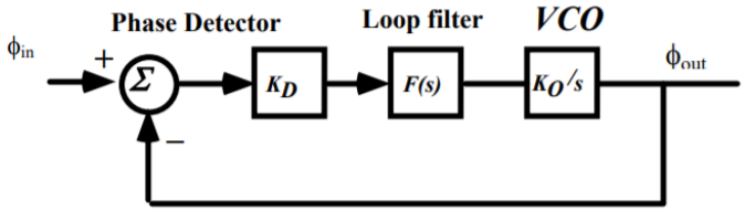

Figure 3.2: Phase Domain Model of Phase Locked Loop.[2]

Transfer Function: $H(s) = forwardpathgain/[1 + T(s)]$.

With feedback = 1,

$H(s) = T(s)/[1 + T(s)]$

$$H(S) = \frac{\phi_{out}}{\phi_{in}} = \frac{K_D K_O F(S)/S}{1 + K_D K_O F(S)/S}$$

Phase error function:

$$\epsilon_S = \phi_{in} - \phi_{out} = \frac{s\phi_{in}}{S + K_D K_O F(S)}$$

We want excellent phase tracking for phase and frequency steps for the frequency synthesis application. It is a discontinuous step in modulus when the synthesizer frequency changes, and we wish to have zero steady state phase error in this scenario.

We'll begin with the open loop gain, T(s).

$$T_{(S)}K_D F_{(S)}K_O/s$$

We know that the phase detector will produce an output that is equal to or double the carrier frequency, so we'll need some low pass filtering. The low pass loop filter's transfer function gains a zero when a resistor is added to it.

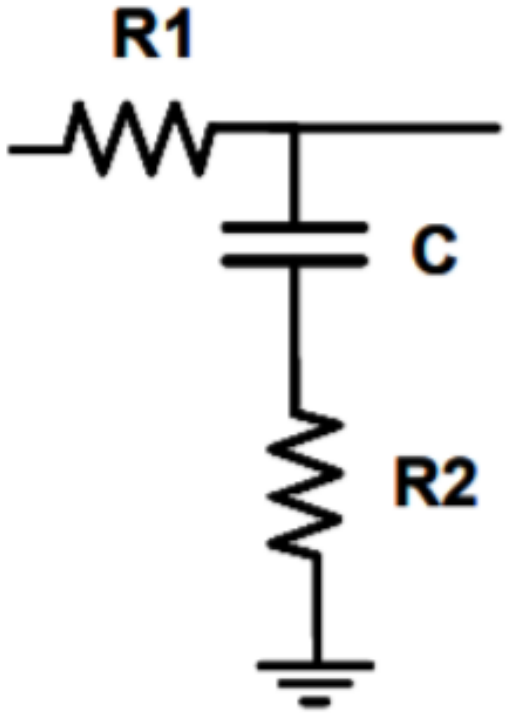

Figure 3.3: Compensation Circuit.[2]

$$F(s) = \frac{1 + s/\omega_2}{1 + s/\omega_1}$$

Where,

$$\omega_1 = \frac{1}{(R_1 + R_2)C}$$
$$\omega_2 = \frac{1}{R_2 C}$$

As a result, the zero frequency always outnumbers the pole frequency.

Examine the Bode plot, the root locus, and the transient reaction once more.

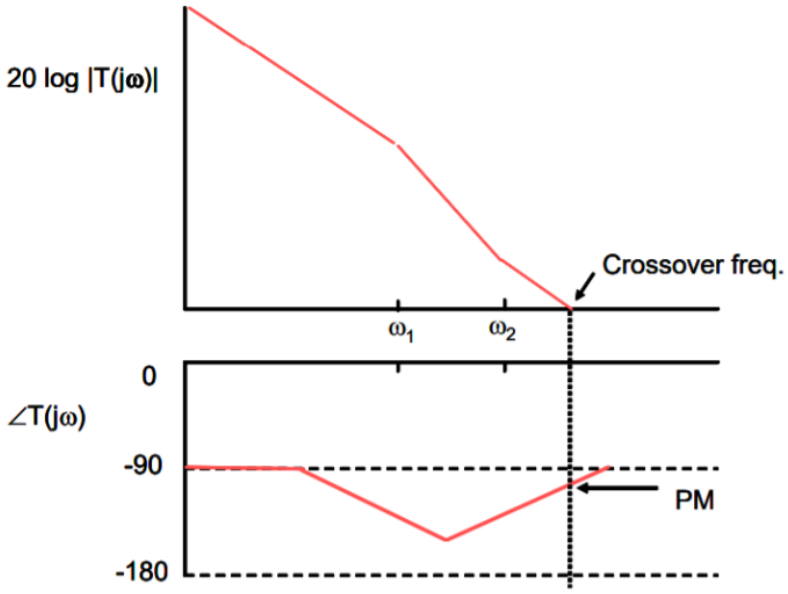

Figure 3.4: Bode Plot of T (jω).[2]

It's worth noting that the phase margin has widened. Smaller ω_1 values can now be used to narrow the filter bandwidth, while higher K_V values can be used to reduce phase error without sacrificing phase margin. When the crossover frequency is increased due to higher gain, the phase margin improves.

Root Locus: Using the pole-zero loop filter, calculate the closed loop transfer function for this PLL.

$$\frac{\phi_0}{\phi_{in}} = \frac{(1 + s/\omega_2)}{\frac{s^2}{K_V \omega_1} + S[\frac{1}{K_V} + \frac{1}{\omega_2}] + 1}$$

The numerator is in the shape of $1 + T(s)$. Because the denominator is in one of the usual forms, we can also extract $omega_n$ and ζ from the closed loop transfer function.

$$\omega_n = \sqrt{K_V \omega_1}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_1}{K_V}} + \frac{1}{2}\frac{\omega_n}{\omega_2}$$

After that, find s; these are the poles.

$$S = -\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1}$$

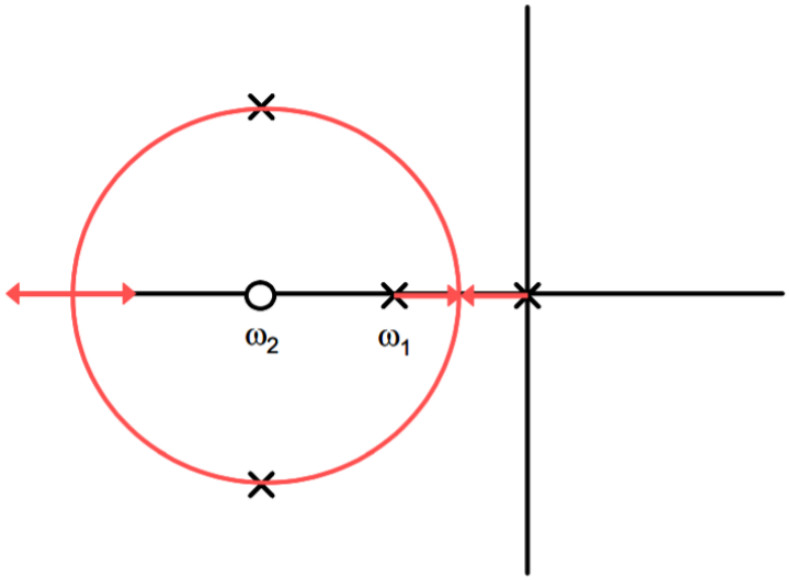

Figure 3.5: RC Filter of T $(j\omega)$.[2]

The damping factor has an extra term, but $omega_n$ is the same as with the conventional RC filter. In most circumstances, the first term is fairly modest, but by increasing K_V or lowering ω_2, the second term can be made quite large. We still have a type 1 system, but we now have a new term, zero frequency, that we can employ to increase stability. The zero appears in the closed loop transfer function since it is in the forward path. The frequency and transient response will be affected.

The loop bandwidth for this Type 1, second-order loop with a forward path zero, according to Gardner1, is:

$$\omega_h = \omega_n[1 + 2\zeta^2 + \sqrt{(1 + 2\zeta^2) + 1}]^{1/2}$$

According to this, for $\zeta = 0.707$, we have a bandwidth of roughly $2\omega_n$.

Bandwidth: For noise considerations, the loop 3 dB bandwidth is critical. Because ωn and ζ determine bandwidth, it must be calculated in conjunction with overshoot and settling time parameters. We discover that the formula for the situation with a forward path zero differs from the feedback zero scenario addressed in the feedback lectures.

$$\omega_h = \omega_{3dB} = \omega_n[1 + 2\zeta^2 + \sqrt{(2\zeta^2 + 1)^2 + 1}]^{1/2}$$

$$\omega_{3db} = 2\omega_m for \zeta = 0.707$$

$$\omega_{3db} = 2.5\omega_m for \zeta = 1$$

We should expect bandwidth to be higher when the loop gain peaking and overshoot are bigger when the zero is present, as this indicates.

APLL practical implementation: In general a charge pump with digital phase detector will be used as a PLL for its infinite response. However, as we are trying to synchronize to a remote carrier the reference signal amplitude changes in amplitude, a digital phase detector assumes the amplitude variation as a phase variation and corrupts the lock. Moreover the CPPLL circuits are known to be operating at low band width which in not desired for this application[15]. Hence, an analog phase locked loop is designed, shown in Fig.3.6. In order to achieve the desired specification certain alterations have been made. This APLL is meant to be extended for a

costas loop design, so it is expected to maintain a high bandwidth to maintain a fast synchronization, faster than the data bandwidth.

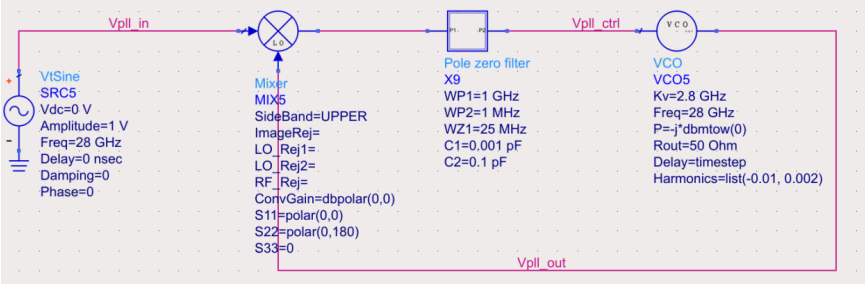

Figure 3.6: APLL Circuit

The Bode Plots in Fig.3.9 and Fig.3.10 are a phase domain system response of the APLL. This shows that there is a trade off between control line ripple(Phase noise) and speed of the loop(Band width). As Fig.3.7 represents the locked voltage control line, the ripple is because of the $2f_0$ signal which cannot be completely eliminated by the filter. This ripple is expected to cause phase noise in the output of the VCO, hence its power has to be maintained below the noise floor. Fig.3.8 shows the reference and the output frequencies of the APLL as one can observe a $90^0(degree)$ phase shift, this is caused due to the cosine relationship of the Vcont on the phase difference. This APLL loop has $85^0(degree)$ phase margin and a $0.15GHz$ bandwidth.

3.2 Costas Loop Design

Focusing on our major aim of simultaneous synchronization and communication, an APLL only focus on synchronization. If you give a BPSK modulated carrier as reference to the APLL it corrects the response of vcont to the data. Hence, a Costas loop is an extension of the APLL slightly manipulated to regenerate the demodulated signal as well as recovering the carrier.

1) squaring the BPSK signal then dividing by two and 2) the 180° Costas loop are the two most frequent approaches for BPSK carrier recovery. Because BPSK modula-

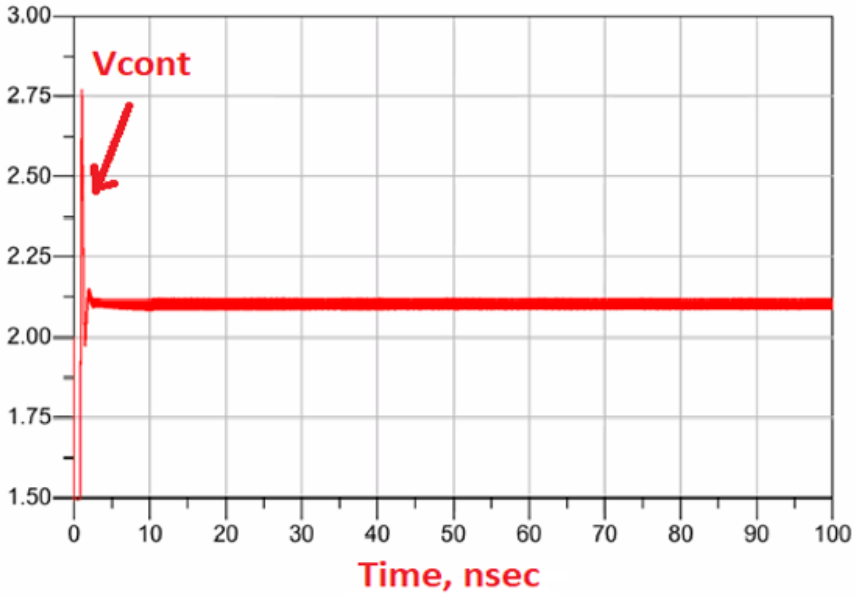

Figure 3.7: APLL Control Voltage

tion creates ±180° phase transitions, the second harmonic will be phase-modulated by an unclear ±360°. The second harmonic is a carrier with twice the frequency that is unmodulated. When you divide the carrier's second harmonic by two, you get a theoretically phase-coherent carrier. The squaring-then-divide circuit has the advantage of being mathematically straightforward to examine. In practise, however, managing the phase offset will be more difficult and layout-dependent; the recovered carrier follows a different path than the demodulator, resulting in a time difference and a phase inaccuracy. Additionally, numerous filters are necessary, making maintaining appropriate phase over the working frequency range problematic.

The Costas loop is based on feedback notions related to the PLL, whereas the first method is a feed-forward technique. The Costas loop has the potential to self-correct the phase (and frequency) of the recovered carrier, and it is no more difficult to construct than the first technique. Its biggest drawback is the need for a loop settling time[8].

Analyzing the Costas Loop: The Costas loop carrier recovery mechanism is founded

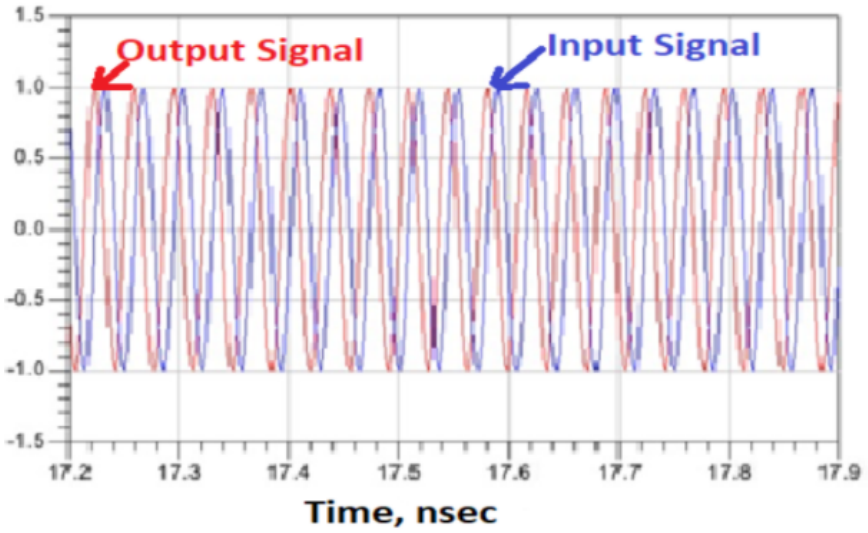

Figure 3.8: APLL Vref and Vout

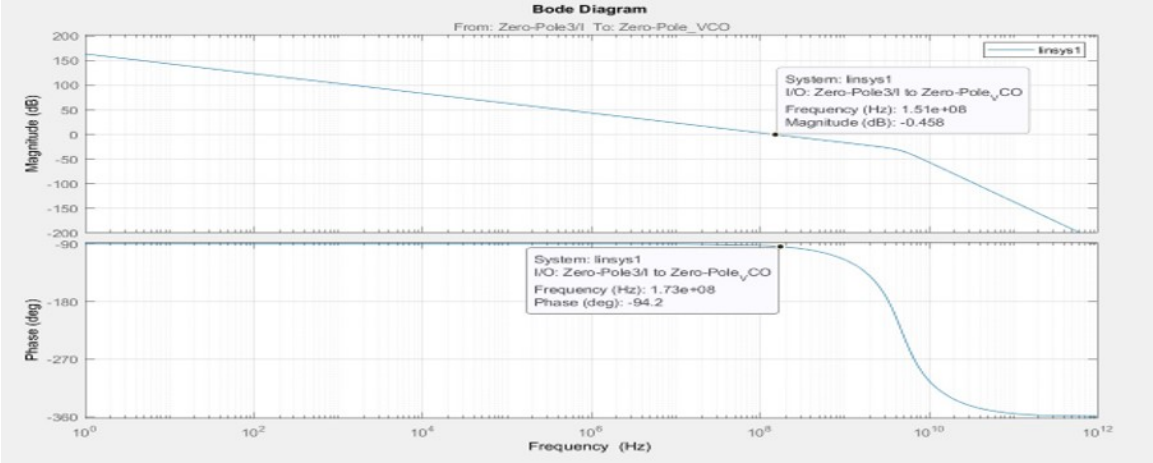

Figure 3.9: APLL Open Loop Response

on the idea of coherency and orthogonality, and iterates its internally generated carrier, the VCO, into the correct phase and frequency. The demodulated information is the low-frequency product of a BPSK signal and its coherent carrier, whereas the low-frequency component of a BPSK signal multiplied by its orthogonal carrier (a carrier 90° out of phase with its coherent carrier) is completely cancelled (there will be no low-frequency component at all). Equations below have already mathematically established the coherent case. The following trigonometric identity is shown for

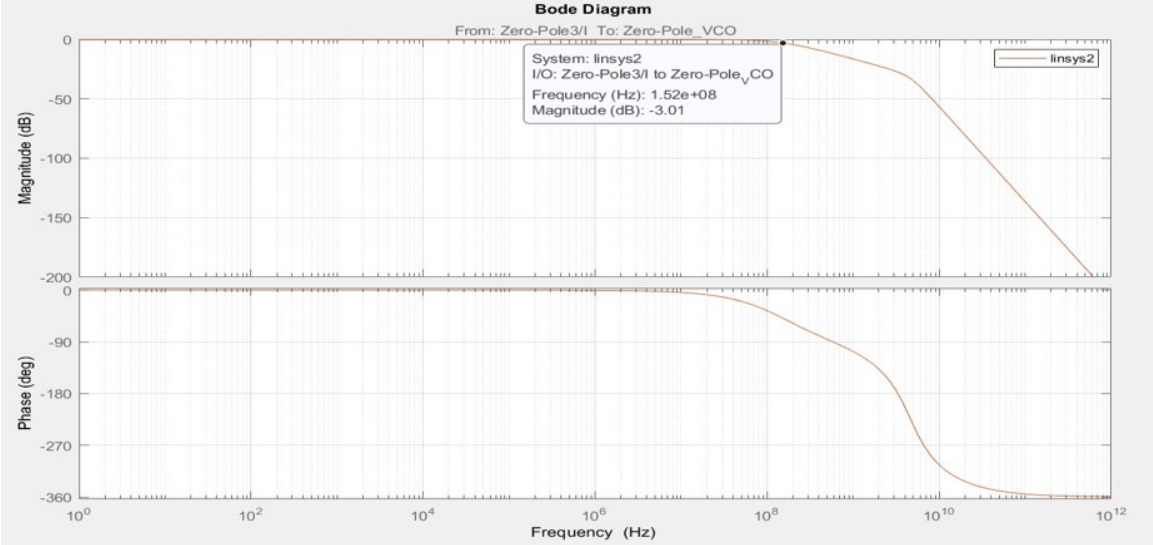

Figure 3.10: APLL Closed Loop Response

the orthogonal case:

$$cos(a).sin(b) = \frac{1}{2}[]sin(a-b) + sin(a+b)]$$

The coherent BPSK carrier is represented by a cosine function, while the orthogonal carrier is represented by a sine (or negative sine) function. This orthogonal multiplication's time-domain representation is:

$$BSPK_N(t).sin(2\pi f_c t) = DATA_N(t).cos(2\pi f_c t).sin(2\pi f_c t)$$

Equation's trigonometric identity yields the following result:

$$\frac{1}{2}[DATA_N(t).sin(0) + DATA_N(t).sin(2\pi f_c t)]$$

Now, because the sine of zero is zero, the product of this multiplication is solely a "high side" component, and the BPSK signal has been shifted by 90° to a frequency twice as high as before.

$$\frac{1}{2}DATA_N(t).sin(2\pi f_c t)$$

The high-frequency component is then removed using a low-pass filter, leaving nothing:

$$LPF[\frac{1}{2}.[DATA_N(t).sin(2\pi f_c t]] = 0$$

When the Costas loop has adjusted its VCO phase and frequency until the 'I' signal is a maximum and the 'Q' signal is zero (in actuality, the locked-loop 'Q' signal is near to zero, but not quite zero), it is said to be "locked." The phase doubler, the third multiplier, creates the product of the 'I' and 'Q' signals, which determines the VCO input voltage.The aim of LPF3 is to remove spurious components and L$PF1/LPF2$ "high side" leakage; it is not intended to contribute significantly to the loop response and is frequently omitted in theoretical Costas loop block diagrams. LPF_1 is a data filter that also functions as a pseudo-integrator when used in conjunction with LPF_2 (these two should be identical to avoid imbalances that lengthen settling time) (a low-pass filter is related to an integrator). This enables the circuit to operate in a manner comparable to a second-order PLL.

When the loop settles, the carrier that will become coherent is represented as a cosine function with some phase error. As a result, the 90° orthogonal carrier must be a negative sine function with the same phase error as the coherent carrier. The resultant product of the 'I' mixer is represented by: Considering the incoming BPSK signal as a cosine with zero phase offset relative to time zero, a radial frequency of $\omega BPSK$ (the radial frequency is 2π times the periodic frequency), and the Costas loop VCO frequency as ωvco with a phase error relative to the BPSK carrier of $\phi phaseerror$, the resultant product :

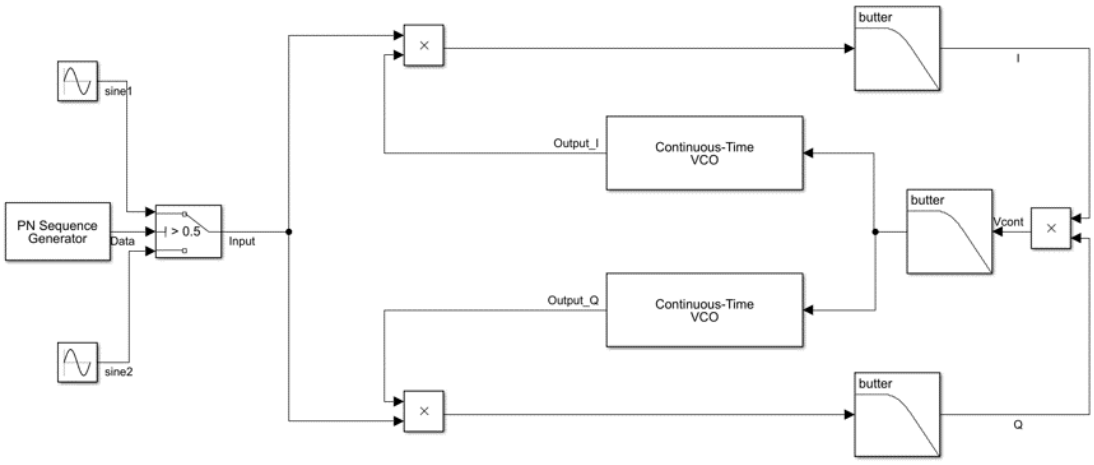

Figure 3.11: Costas Loop MATLAB Implementation.

$$I\_Output = cos(\omega_{vco}t + \theta_{phase-error}).DATA_N(t).cos(\omega_{bpsk}t)$$

The 'Q' mixer, on the other hand, provides the following result:

$$Q\_Output = -sin(\omega_{vco}t + \theta_{phase-error}.DATA_N(t)$$

Replacing DATAN(t) with ± 1, the resulting Vcontrol product is as follows[8]:

$$V_{control} = -\frac{1}{8}sin(2((\omega_{vco} - \omega_{bpsk})t + \theta_{phase-error}))$$

Costas loop design: Costas loop circuit has been designed to function as a coherent detector as shown in Fig.3.11. This circuit is to ensure the slave transceiver to be synchronous in frequency to that of the master's. This property has been verified by the testbench result shown in Fig.3.14 where the 14 GHz costas loop is synchronized to a 14.1 GHz received signal. The range of this Costas Loop is determined by the bandwidth of the loop.

Costas loop is expected to reconstruct the transmitted data which is also verified by the testbench in Fig.3.11. A pseudo random data is used to verify the data

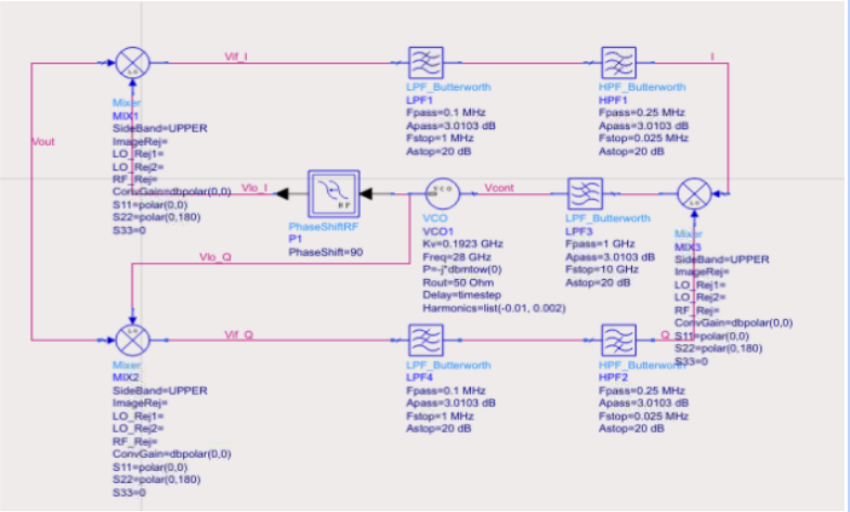

Figure 3.12: Costas Loop Circuit in Keysight ADS

reconstruction from the IQ channel of the Costas loop as shown in Fig.3.13. If the received signal frequency is same as that of the slave LO (QVCO) the reconstructed data should only appear in the I channel, and the Q channel stays silent. If there is a frequency shift, both the channels produce the reconstructed data, according to the property of Costas loop as discussed.

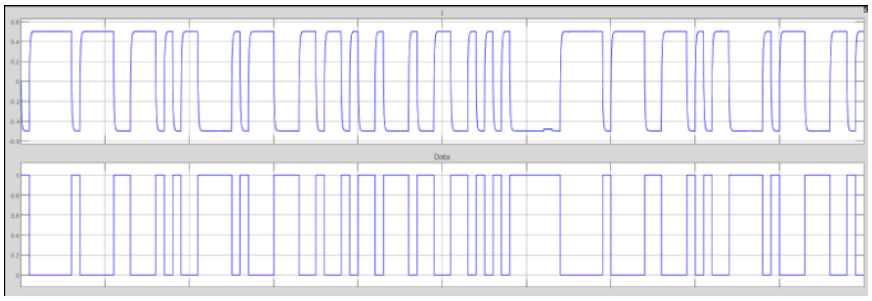

Figure 3.13: Data_in and Data_out

Once locked to the incoming signal that slave LO frequency can be used for transmission. However the control line of the VCO is inherently noisy causing the LO to produce phase noise rising the noise floor and dropping the Signal to Noise Ratio (SNR) of the receiver.

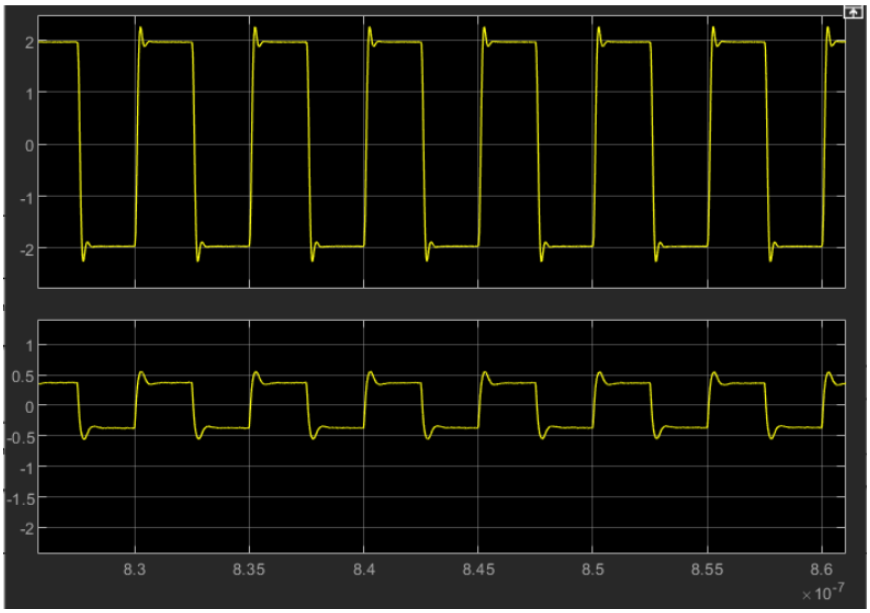

Figure 3.14: I and Q Outputs of Costas Loop

Chapter 4

FULL DUPLEX SYNCHRONIZATION

The Costas Loop successfully demodulate the data and extract the carrier from the received signal. However, when we try to extend this simultaneous synchronization and communication to a full duplex communication system we have to deal with several complications like self interference as the powerful signal coming out of the transmitter's power amplifier will get leaked into the receiver and pull the VCO off the synchronized frequency. Inorder to understand and mitigate this effect of transmitted signal on the receiver synchronization, this effect is modeled as well known injection pulling and has been extensively studied in this chapter

4.1 Analysis of Injection Pulling

The universal theory of synchronization, where apparently identical oscillatory systems tend to pull each other towards unison, was also observed in electronic oscillators and their effects were first studied by Adler [3]. This process of pulling is physically established by the common substrate, power line , ground line and external reflections. Local oscillator pulling is critical for direct conversion transmitters, as the modulated signal after the power amplifier consists of adjacent frequencies close to the LO frequency. The power amplifier makes all these frequency components stronger than the LO signal resulting in pulling as illustrated in the Fig.4.1. The Adler's equation describes the time domain and frequency domain variations of these pulling effects[3].

$$\frac{d\theta}{dt} = \omega_0 - \omega_{inj} - \omega_L sin\theta$$

where,θ is the instantaneous phase at the output of the oscillator

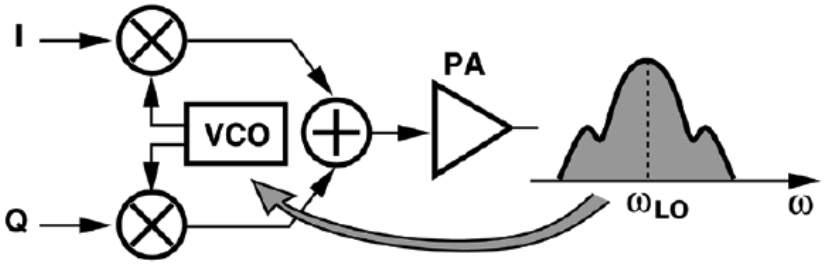

Figure 4.1: Oscillator pulling in direct conversion transmitters.[14]

The oscillator pulling is modeled as an injection current signal loading the oscillator[14]. As shown in the Fig.4.2(b).

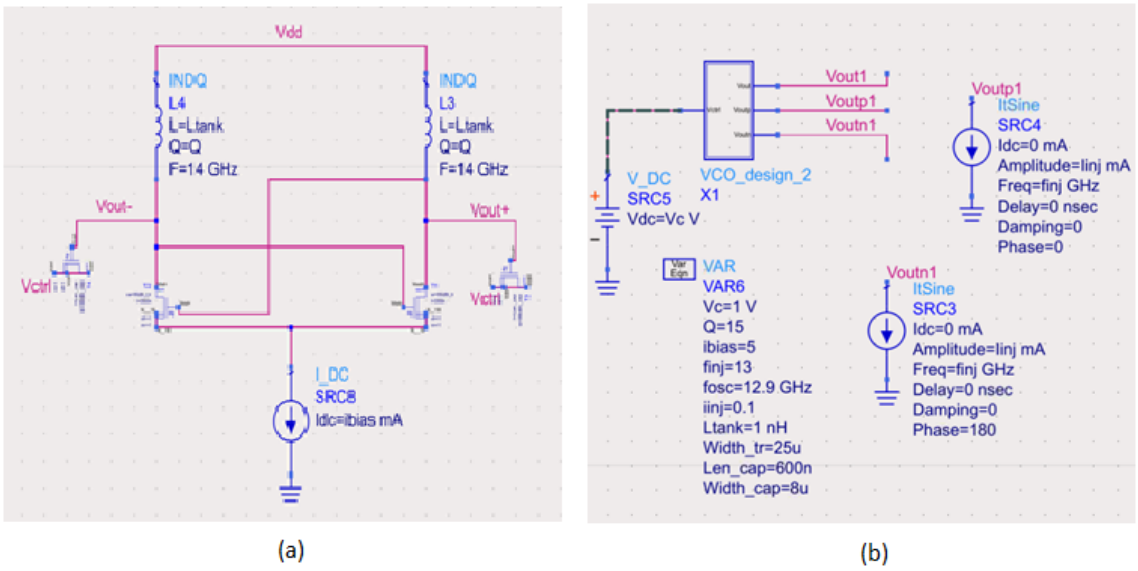

Figure 4.2: (a) VCO Circuit (b)Currunt injection model of the pulling effect.

The impact of the injection signal on an oscillator is defined by several parameters like

- Oscillator frequency(ω_0)
- Injection signal frequency(ω_{inj})
- Injection signal strength(I_{inj})

- Oscillator sterngth(I_{osc})

These parameters can be understood as lock range of the oscillator

$$\omega_L = \omega_0 - \omega_{inj} = \frac{\omega_0}{2Q}.\frac{I_{inj}}{I_{OSC}}.\frac{1}{\sqrt{1-\frac{I_{inj}^2}{I_{osc}^2}}}$$

Oscillator's behavior varies as the injection signal frequency approaches the lock range. If a strong enough injection signal frequency is below the lock range from oscillator's frequency, it pulls the oscillator away toward the injection frequency. As the injection frequency approach the edge of lock range the oscillator produces suprs as shown in Fig.

VCO design: A standard LC oscillator has been designed in Fig.4.2 for the study of the injection metrics. The transistor that has been used is a Global foundries 2.5V NFET. The operating frequency is set to 13.61 GHz. Two MosCaps are used for frequency tuning and the Voltage sensitivity is set to 0.9 GHz/V. The injection port is modeled as a current source which is affected by the output spectrum of the transmitter power amplifier. Fig.4.4 shows the Fast Fourier Transform of the output transient in Fig.4.3. Fig.4.5 describes the VCO's frequency variation with respect to it's control line voltage(Vcont).

Pulling simulations In this part of the section the pulling behaviour of the oscillator has been analysed extensively, re-establishing the concepts discussed in Razavi's[14]. Initially a weak injection signal has been provided as a current source, loading the VCO later the pulling response of the VCO is analysed in an APLL, as discussed below.

VCO pulling: Oscillator's behavior varies as the injection signal frequency approaches the lock range. If a strong enough injection signal frequency is below the lock range from oscillator's frequency, it pulls the oscillator away toward the injection frequency. As the injection frequency approach the edge of lock range the oscillator

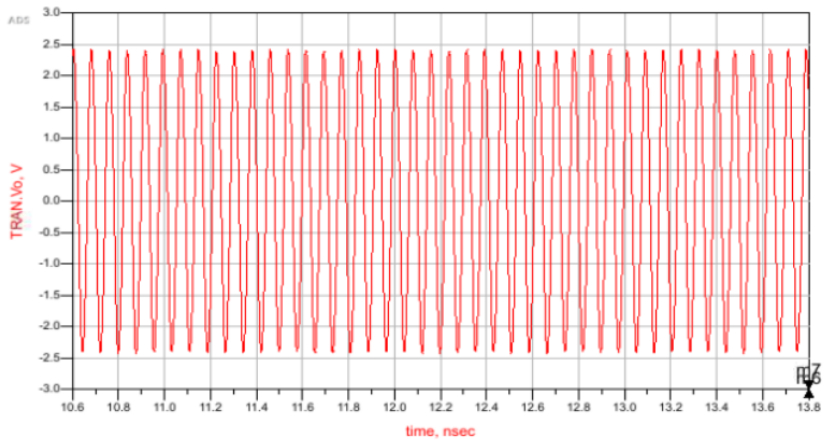

Figure 4.3: VCO output transient

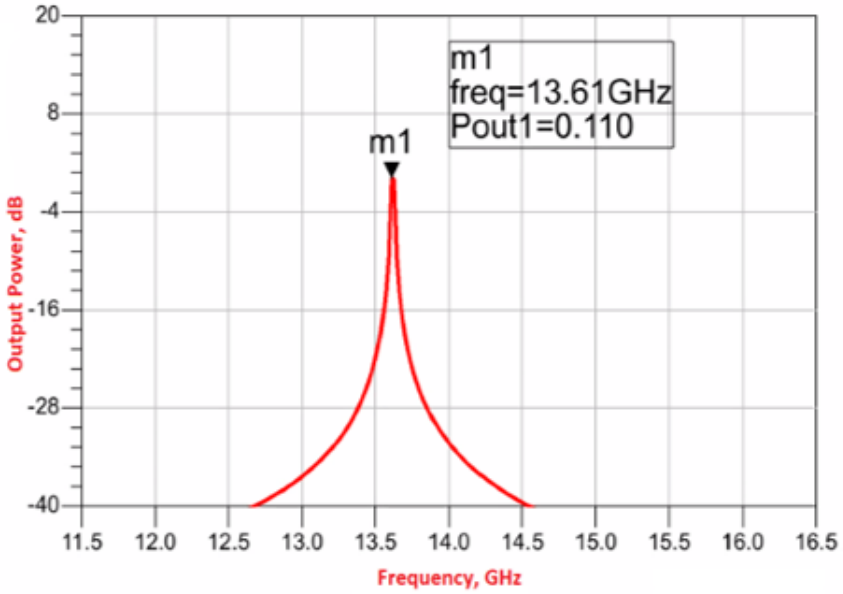

Figure 4.4: Free Running VCO Spectrum

produces suprs as shown in Fig.4.6, called as a Quasi beat response where none of the tones are of the required oscillation frequency[14].

PLL pulling A VCO in the phase locked loop is expected to be much more immune to the injection pulling as there will be a correction signal in response to the frequency variations. If the injection frequency is closer to the operating frequency VCO, inside the PLL bandwidth, the quasi beat suprs still exist but the primary

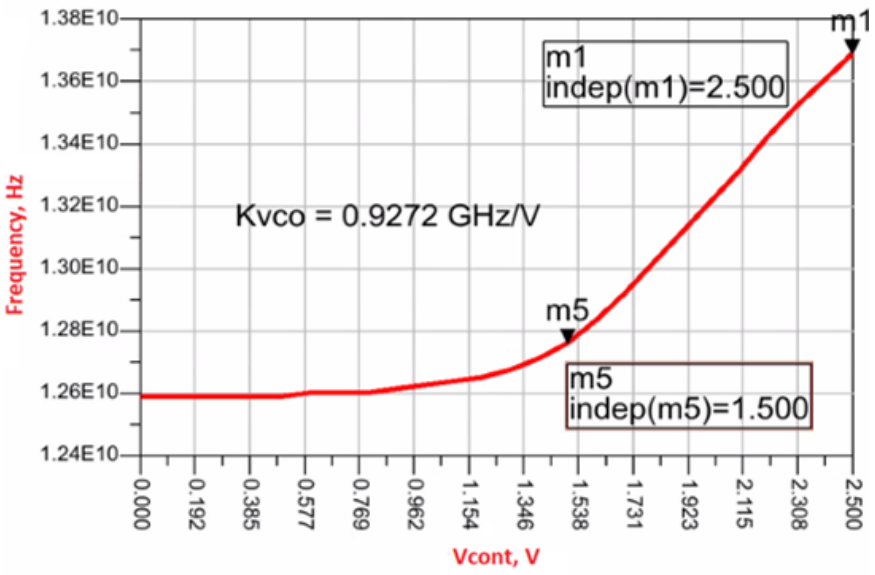

Figure 4.5: Frequency vs Control Voltage

tone will be held at oscillator(reference signal) frequency, as shown in Fig.4.7. If the injection frequency is far out of the bandwidth the strength of its effect diminishes. However the output of the PLL is amplitude modulated by the loading of injection current source spectrum as shown in Fig.4.8. The PLL's output spectrum without the effect of injection is shown in Fig.18 as a reference.

Effect of injection pulling on demodulation: These spurs caused by the injection pulling on the demodulation of the signal when applied to a VCO in costas loop. As Costas loop is basically an extension of a PLL all the limitations of the APLL will be applied to the Costas loop. A Costas loop has been implemented including the injection model to its local oscillator in Fig.4.9.

The costas loop was set to operate at $13.52GHz$ but the injection spurs around the LO frequency caused by $13.5GHz$ injection signal disrupt the demodulated signal, amplitude modulating the base band signal as shown in Fig.4.10. Using a Band pass filter on the required LO frequency is not an option here as the filter might affect the stability of the loop. This effect is much more prominent in coherent receivers

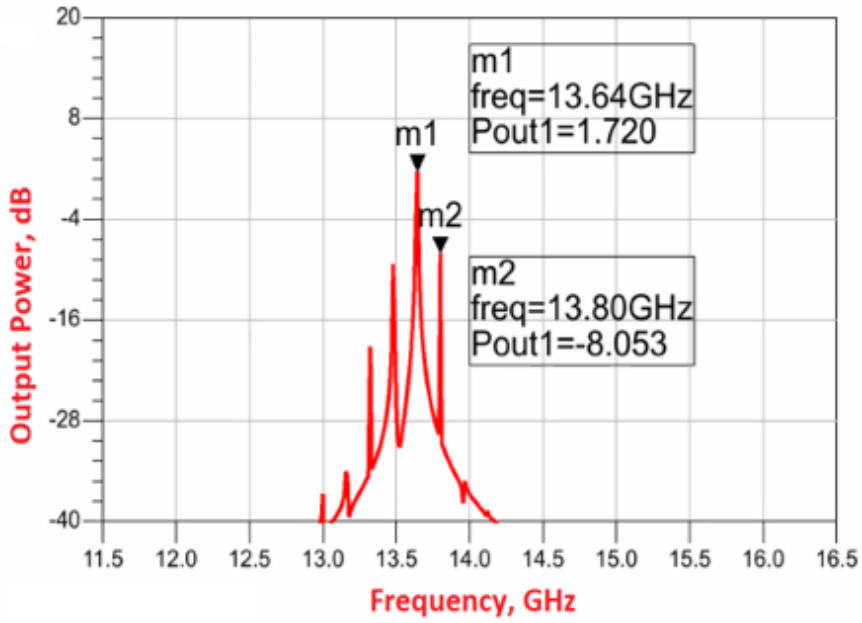

Figure 4.6: VCO Pulled Spectrum

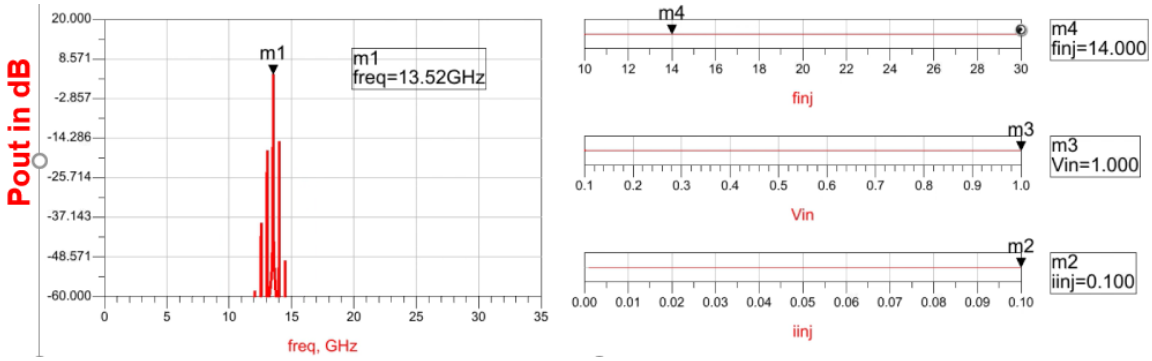

Figure 4.7: PLL Pulled Spectrum When Injection Signal is Inside the Bandwidth

because the strength of PLL in holding the VCO from frequency shift is dependent on the reference signal power. In coherent receivers as the reference signal is being transferred to the receiver it will be weaker. If the PLL is weak and a strong injection signal is leaked it will pull the VCO away.

4.2 Proposed Solution for Pulling Effect

If the injected noise has a frequency near to the oscillator's native frequency, the LO output becomes progressively disturbed as the noise magnitude increases,

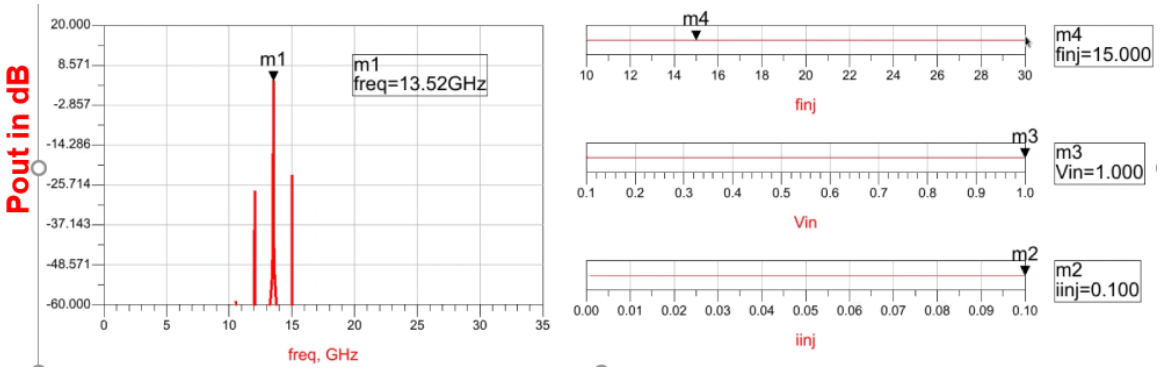

Figure 4.8: PLL Pulled Spectrum When Injection Signal is Outside the Bandwidth

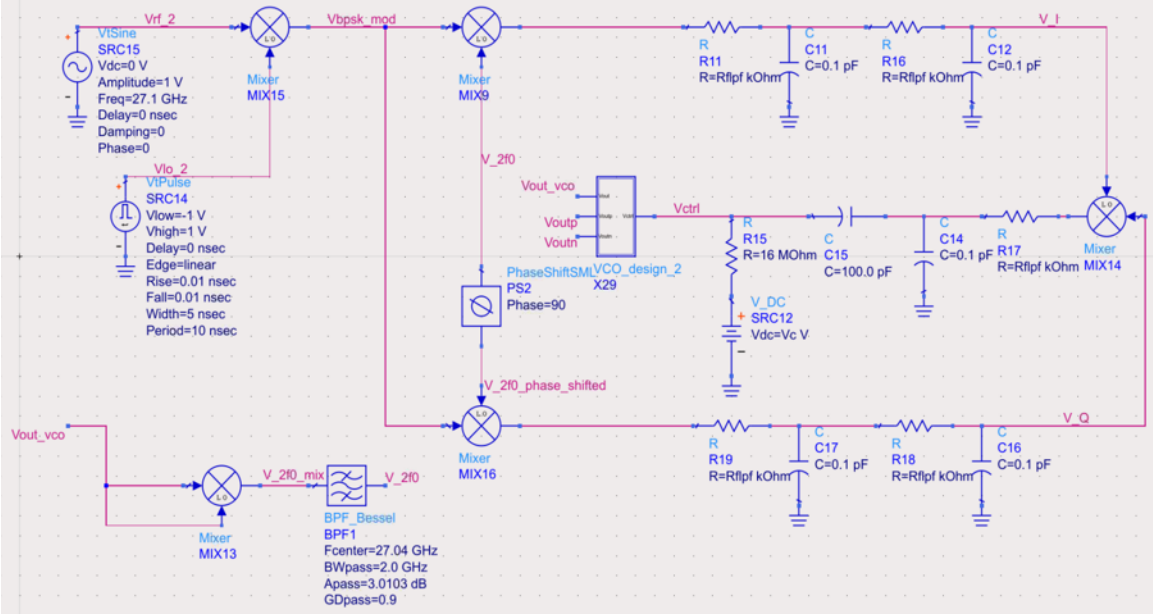

Figure 4.9: Costas Loop Circuit with Injection Locking Model

eventually "locking" to the noise frequency. In practise, noise levels as low as 40 decibels below the oscillation level can cause significant disruption. If the PA output spectrum is sufficiently far from the oscillator frequency, the phenomena of LO pulling is reduced. This can be done for quadrature up conversion by "offsetting" the LO frequency, or adding or subtracting the output frequency of another oscillator . depicts an example in which the VCO_1 and VCO_2 output signals are blended and the result is filtered so that the carrier frequency is equal to $\omega_1 + \omega_2$, which is far from either $\omega_1 + \omega_2$.

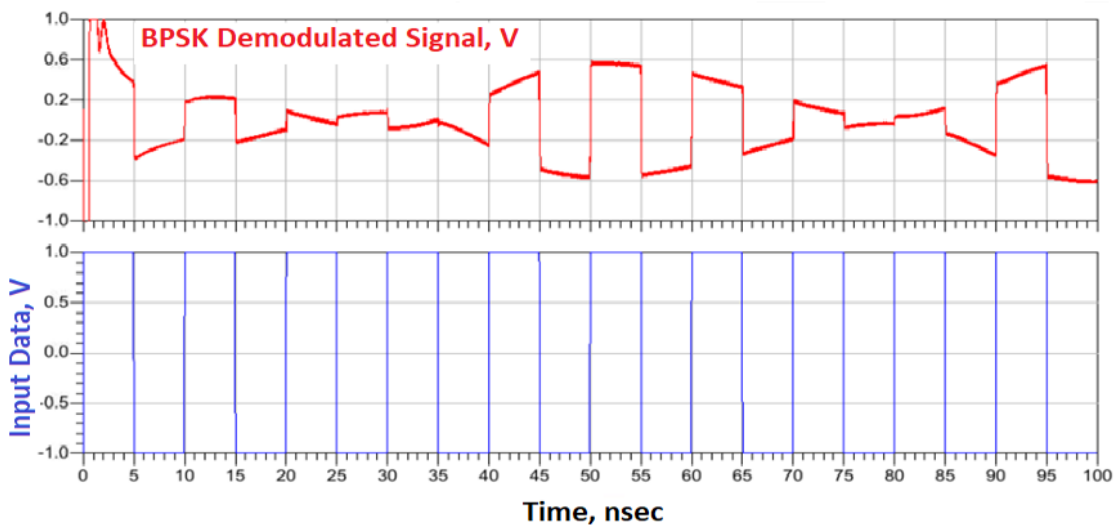

Figure 4.10: Effect of Injection Puling on Demodulation

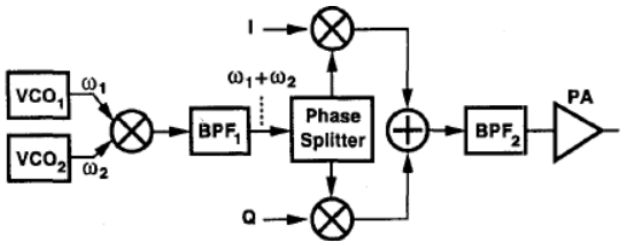

Figure 4.11: Transmitter with Offset LO[13]

The first bandpass filter's selectivity, BPF_1. Many spurs of the form m $\omega_1 \pm n\omega_2$ emerge at the input of BPF_1 due to nonlinearities in the offset mixer. Such components weaken the quadrature production of the carrier phases and cause spurs in the upconverted signal if they are not effectively suppressed by the filter.

Solution simulation: Even under the protection of PLL the spectrum response of the LO under injection produces unnecessary spurs which might have an impact on the receiver performance. Hence the solution provided can be used to generate a spurious free injection response. Fig.4.9., shows a Full duplex model of slave transceiver which consists of a Costas loop working as a coherent detector at double the operating frequency of the designed VCO. A mixer has been used as a non linear frequency

multiplier to double the frequency of the VCO in order to meet the desired specification. As the current operating frequency of the slave transceiver is double that of oscillator's frequency, the BPSK modulated signal at the transmitter's power amplifier will have a minimal pulling effect on the VCO. Fig.4.12 shows the demodulated signal at the output of costas loop under the injection pulling.

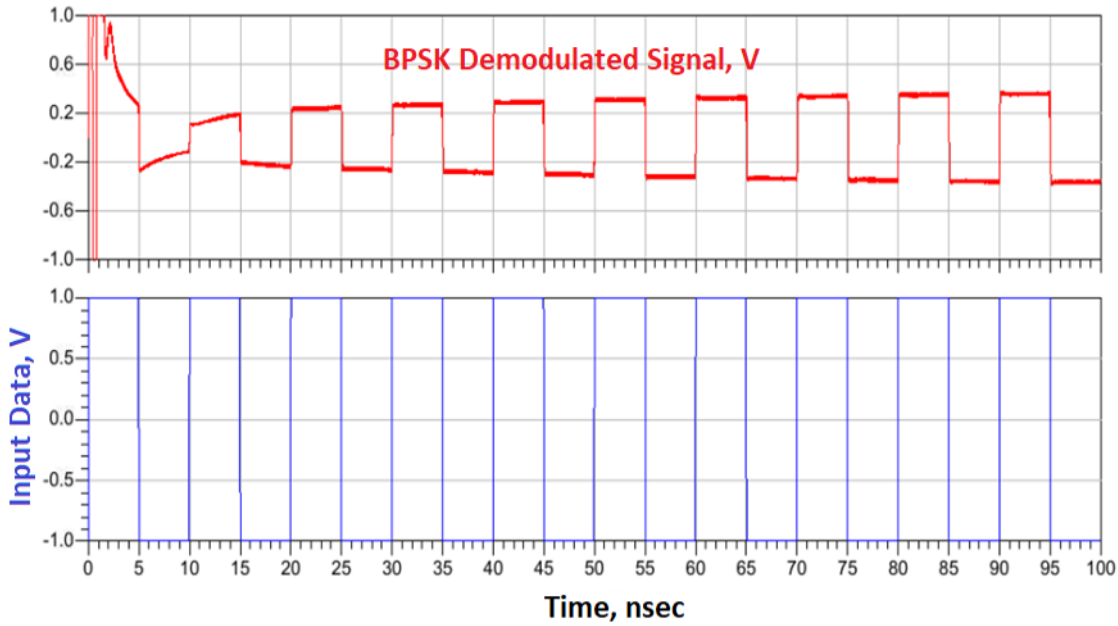

Figure 4.12: Demodulated Signal After Eliminating the Injection along with Input Data

Chapter 5

CONCLUSION AND FUTURE WORK

5.1 Discussion and Conclusion

With the advancement in technologies like Internet of Things(IoT) and rise in demand on higher data rates these types for full duplex distributed transceiver architectures proves to be extremely useful[7]. Rise in necessity often comes with more complicated challenges, this study is one such situation. Designing a coherent receiver might have been easier if the communication system is operating in frequency duplexing, transmitting and receiving the data on different frequencies, as there won't be an issue of injection pulling at varied frequencies. Similarly, it would be easier to implement a Full duplex system with a fixed crystal oscillator generating or controlling the local oscillator frequency, as it is harder to disturb a crystal oscillator than a remotely synchronized VCO. This Thesis involves a Coherent full duplex architecture design, which gave rise to the issue of injection pulling causing a complicated challenge in design. Fortunately this issue has been alleviated by shifting the primary oscillator to a lower frequency and regeneration the LO by unconventionally using a multiplier in the phase locked loop. Towards this end we developed an APLL using the designed VCO locking to the required frequency. With that as a base we designed a costas loop operating as the coherent receiver. Meanwhile, the transmitter power amplifier leaks a pull signal into the injection port of the VCO pulling it out of the operating frequency cursing the drop in functionality of the receiver. We replace the existing VCO with a lower frequency version connected to a frequency multiplier to avoid the pulling effect. The performance of the receiver throughout this process has

been observed and recorded. A frequency enhancement technique is discussed in the future works below, which can be considered as an extension for this topic on the same application for wider bandwidth.

5.2 Future Work

Frequency enhancement: For a distributed transceiver network a slave transceiver with wider bandwidth can accommodate several applications by a better spectral utility. The slave count can be increased for global applications using such wide band transceivers. The two things limiting the bandwidth of the receiver in a slave transceiver are the VCO's tuning range and the limitation of frequency detection using a linear phase detector. Although the VCO's tuning range can be increased by several circuit techniques, a simple APLL cannot lock to a huge frequency step. This limitation can be alleviated by using a frequency detection technique in parallel with the usual phase detection as discussed in the paper[10]. An example transceiver is shown in Fig.5.1.

Self Interference cancellation : All the full duplex models that have been discussed in this work do not consider the obvious and unavoidable issue of self interference from direct leakage and from reflections. This issue can be addressed by using techniques like bulk isolation[9] or LMS FIR cancellation[4] or both together. However these techniques are still known to contribute to the SNR degradation. The injection model that has been discussed only considers the internal pulling but it is known that the self interference will also have an effect on the frequency acquisition if not properly cancelled. These effects are expected to be addressed in the further course of research.

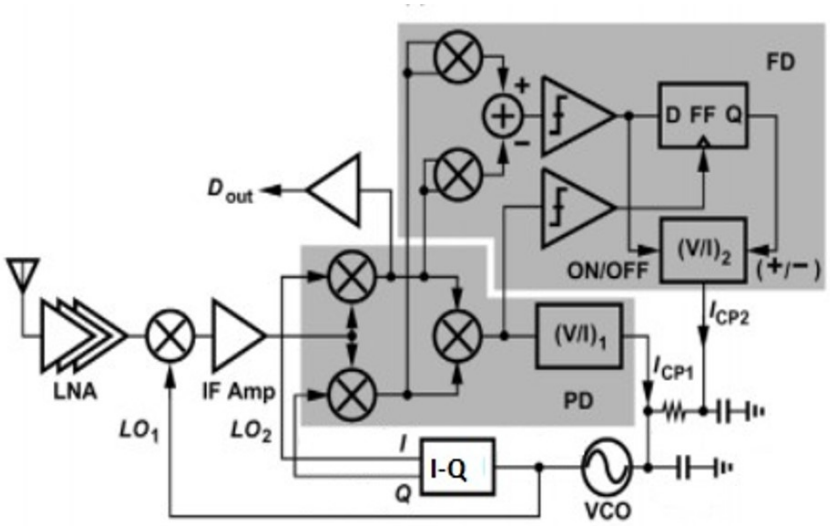

Figure 5.1: Frequency Enhancement[9]

REFERENCES

[1] https://www.eecs.umich.edu/courses/eecs555/lect06.pdf.

[2] https://web.ece.ucsb.edu/ long/ece594a/PLL$_i ntro_5 94a_s 05.pdf$.

[3] R. Adler. A study of locking phenomena in oscillators. *Proceedings of the IEEE*, 61(10):1380–1385, 1973.

[4] S. Ayati. Full duplex cmos transceiver with on-chip self-interference cancelation. 2017.

[5] D. W. Bliss, P. A. Parker, and A. R. Margetts. Simultaneous transmission and reception for improved wireless network performance. In *2007 IEEE/SP 14th Workshop on Statistical Signal Processing*, pages 478–482, 2007.

[6] W. Cheng, X. Zhang, and H. Zhang. Full duplex wireless communications for cognitive radio networks, 2011.

[7] A. Fehske, G. Fettweis, J. Malmodin, and G. Biczok. The global footprint of mobile communications: The ecological and economic perspective. *IEEE Communications Magazine*, 49(8):55–62, 2011.

[8] J. Feigin. Practical costas loop design - designing a simple and inexpensive bpsk costas loop carrier recovery circuit, rf design. *RF DESIGN*, 25:20–37, 2002.

[9] F. U. Haq, M. Englund, Y. Antonov, K. Stadius, M. Kosunen, J. Ryynänen, K. B. Östman, and K. Koli. Full-duplex wireless transceiver self-interference cancellation through fd-soi buried-gate signaling. In *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5, 2018.

[10] S.-J. Huang, Y.-C. Yeh, H. Wang, P.-N. Chen, and J. Lee. w -band bpsk and qpsk transceivers with costas-loop carrier recovery in 65-nm cmos technology. *IEEE Journal of Solid-State Circuits*, 46(12):3033–3046, 2011.

[11] S. R. Mghabghab, A. Schlegel, and J. A. Nanzer. Adaptive distributed transceiver synchronization over a 90 meter microwave wireless link, 2020.

[12] R. Mudumbai, D. R. Brown Iii, U. Madhow, and H. V. Poor. Distributed transmit beamforming: challenges and recent progress. *IEEE Communications Magazine*, 47(2):102–110, 2009.

[13] B. Razavi. Rf transmitter architectures and circuits. In *Proceedings of the IEEE 1999 Custom Integrated Circuits Conference (Cat. No.99CH36327)*, pages 197–204, 1999.

[14] B. Razavi. A study of injection locking and pulling in oscillators. *IEEE Journal of Solid-State Circuits*, 39(9):1415–1424, 2004.

[15] B. Razavi. *Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level*. Cambridge University Press, 2020.

[16] Zhai, Bingcong. Understanding of the coherent demodulation with phase-locked loop. *MATEC Web Conf.*, 176:01028, 2018.