Metallization to Silicon Solar Cells:

Improving Optothermal Performance of PERC

and Developing New Systems for TOPCon and SHJ

by

Jonathan Bryan

A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved December 2021 by the
Graduate Supervisory Committee:

Zachary Holman, Chair
Mariana Bertoni
Stuart Bowden
Michael Goryll

ARIZONA STATE UNIVERSITY

May 2022

ABSTRACT

Metallization of solar cells is a critical process step in the manufacturing of silicon photovoltaics (PV) as it plays a large role in device performance and production cost. Improvements in device performance linked to metallization and reduction in material usage and processing costs will continue to drive next-generation silicon PV technology. Chapter 1 introduces the context for the contributions of this thesis by providing background information on silicon PV cell technology, solar cell device physics and characterization, and metallization performance for common silicon cell structures. Chapter 2 presents a thermal model that links sub-bandgap reflectance, an important metric at the rear metal interface, to outdoor module operating temperature. Chapter 3 implements this model experimentally with aluminum back-surface field (Al-BSF), passivated emitter and rear contact (PERC), and passivated emitter rear totally diffused (PERT) mini-modules, where the PERT cells were modified to include an optimized sub-bandgap reflector stack. The dedicated optical layer was a porous low-refractive index silica nanoparticle film and was deposited between the dielectric passivation and full area metallization. This created an appreciable boost in sub-bandgap reflectance over the PERC and Al-BSF cells, which directly lead to cooler operating temperature of the fielded module. Chapter 4 investigates low-temperature Ag metallization approaches to SiO_2/polysilicon passivating contacts (TOPCon architecture). The low-temperature Ag sintering process does not damage TOPCon passivation for structures with 40-nm-thick poly-Si but shows higher contact resistivity than sputtered references. This disparity is investigated and the impact of Ag diffusion processes, microstructure changes, ambient gases, and interfacial chemical reactions are evaluated. Chapter 5 investigates sputtered Al metallization to silicon heterojunction contacts of both polarities. This In-free and Ag-free metallization process can achieve low contact resistivity and no passivation loss when annealed between 150-180 °C. The passivation degradation at higher temperatures was studied with high-resolution microscopy and elemental mapping, where the interdiffusion processes were identified. Lastly, Chapter 6 summarizes the contribution of this work.

ACKNOWLEDGMENTS

I thank my advisor, Dr. Zachary Holman, for his guidance, feedback, and invaluable perspective throughout the PhD journey. I also thank my committee members, Dr. Mariana Bertoni, Dr. Stuart Bowden, and Dr. Michael Goryll for their engagement and support in helping me complete the journey. I thank all my lab mates, past and present, for training me on tools and processes, generously sharing knowledge, and always providing needed guidance, encouragement, and friendship. I thank all my professors and all my teachers, past and present, who helped me build the personal and educational foundation to complete this work.

I thank Arizona State University and the numerous organizations, staff, and research facilities that made this work possible and that also supported my success outside the lab. I also thank the funding agencies and all collaborators for support and valuable contributions.

Last but not least, I thank my family and friends for their constant love and support.

TABLE OF CONTENTS

Page

LIST OF TABLES

Table Page

LIST OF FIGURES

Figure Page

CHAPTER 1

INTRODUCTION

1.1 Background

The photovoltaic (PV) solar cell is a promising technology to supplant non-renewable fossil energy in the global energy mix. According to the United States Energy Information Administration (EIA), from 2006 to 2020, annual PV module shipments increased from approximately 320,208 to 21,770,903 [1]. During the same time span, the average PV module price dropped from \$3.50 to \$0.38 [1]. These improvements have allowed solar PV to become an increasingly major electricity provider in the United States, growing from an estimated 0.01% of utility-scale electricity generation in 2006 to 2.3% in 2020 [2]. Further, solar PV has become the fastest growing source of added electricity capacity in the United States, accounting for 15.4 GW or 39% of planned electricity capacity additions in 2021 [3].

Industrial manufacturing of solar PV cells and modules is dominated by silicon technology, which accounts for about 95% of production capacity [4]. For several decades leading up to 2016, the dominant technology in production was Aluminum Back-Surface Field (Al-BSF) due to its simple and reliable manufacturing processes and suitable energy conversion efficiency [5]. Figure 1-1 shows the market share for Al-BSF and Passivated Emitter Rear Contact (PERC) PV technologies from 2013 to 2020, according to ITRPV [4, 6-12]. This data highlights the tail-end of industry reliance on Al-BSF, the onset of the rise of PERC between 2015 and 2016, and its subsequent rapid industry takeover.

Although Al-BSF was the industry standard from 1999 to 2014, the record efficiency for a single junction silicon cell was held by a 25%-efficient passivated emitter rear locally-

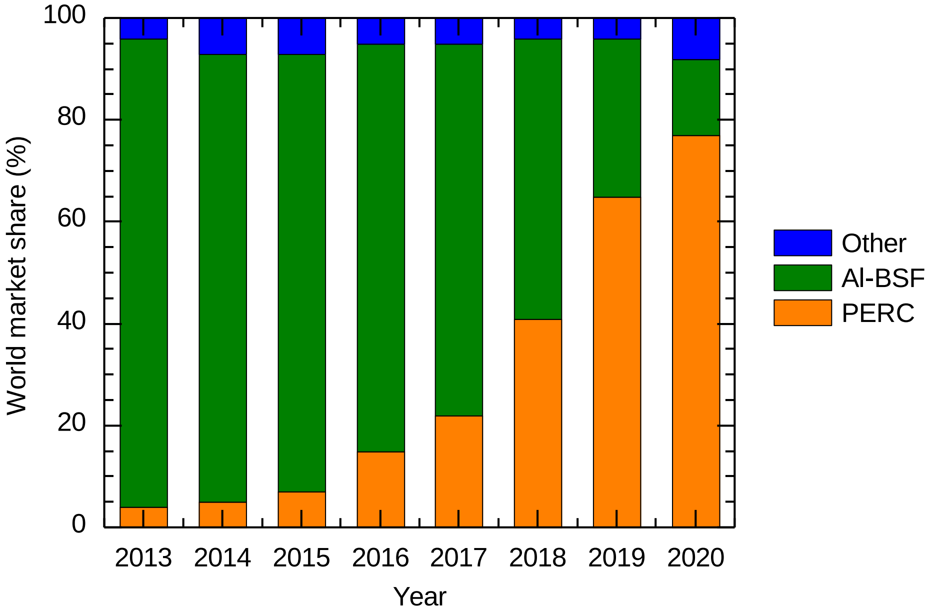


Figure 1-1. World market share of PV technology from 2013 to 2020 [4, 6-12].

diffused (PERL) device [13-15]. While this device benefited from laboratory-scale processes and materials (float-zone wafer, metal evaporation, photolithography), it embodied the primary improvement of the PERC-family of architectures over Al-BSF structures: adding state-of-the-art rear passivation and optimizing the area of direct metallization to the silicon absorber [14]. In the UNSW world-record PERL device, the silicon oxide (SiO_2) dielectric passivation layer covered 99% of the rear area; the combination of effectively suppressing recombination and enhancing rear reflectivity directly led to the record-setting efficiency improvements [16]. Improving cell efficiency is a crucial lever for PV technology as efficiency improvements propagate through to reduce area-related costs at the module and system level through reduced use at constant power of labor, glass, backsheet, frames, land preparation, racking, cabling, and more [17, 18].

In order to capture the possible efficiency gains of PERC at the manufacturing scale, key processes had to be added to standard Al-BSF processing at low cost, high throughput, and high reliability. These include the removal of rear phosphorous-diffused layer, the deposition of rear surface-passivation films, the definition of openings through the passivation layer to make local metal contact, and the modification of metallization pastes [5]. The phosphorous-diffused region on the rear-side of the wafer is typically removed with single-side wet chemical polishing [5]. The rear-passivation stack of Al_2O_3/SiN_x has become the dominant choice for rear surface passivation with deposition generally performed via plasma enhanced chemical vapor deposition (PECVD) or atomic layer deposition (ALD) [19]. The metal-contacted areas are defined by a process called laser contact opening (LCO), where select areas of the passivation stack are removed through laser ablation [5]. Al metallization pastes were modified to avoid damaging the SiN_x layer, and the passivation and optical benefit it affords, while also achieving good depth of Al doping into the silicon absorber during firing through the reduced-area contact openings [16]. Several decades of intense research effort following the demonstration of the cell concept in 1989 allowed the key additions to become worthwhile industrially around 2015-2016, contributing to the subsequent increased PERC market share [16].

While there are multiple design variations within the PERC family, the p-type monocrystalline silicon variant (bifacial or monofacial) utilizing the above processes has become the dominant design, capturing 80% of the world market share in 2020 and a projected 90% in 2021 [16, 20]. The 2021 ITRPV reports average efficiency values for these cells in mass production at approximately 21%, while more recent reports claim that the efficiencies of current mainstream products are approaching 23% [12, 21]. This performance significantly exceeds Al-BSF average efficiencies in mass production, listed in the 2020 ITRPV report as 19% and 20.2% for multicrystalline and monocrystalline wafers, respectively [12]. As of October 2021, large-scale manufacturing operations producing 22.7% efficient mono-PERC cells have achieved module costs of $0.261/Watt, with module price being $0.286/Watt (for 9.6% gross margin) [22]. While this is currently the most competitive benchmark for PV technology, continued efficiency and cost improvements are expected in the immediate future. Projections anticipate median cell efficiency to achieve 24% with continued cost reductions, resulting in module prices below $0.2/Watt within the next several years [23, 24]. Such continuous improvement of PERC creates a moving benchmark for which new, competing technologies must outperform.

In parallel with the recent rapid PERC manufacturing growth, various institutions have developed new cell architectures that surpassed the previous long-standing UNSW FZ-PERL efficiency record: 25.2% by SunPower, 25.6% by Panasonic, 26.7% by Kaneka, 25.8% by F-ISE, and 26.1% by ISFH [25-30]. These efforts have boosted the single junction silicon efficiency record by 1.7% absolute since 2014, compared to 1.8% absolute in the 25 years prior (1989 to 2014) [13]. Though the process sequences, materials, and cell architectures vary significantly for each of the listed devices, the common feature is removing the directly metallized contact to the silicon absorber [31]. While the silicon PV industry has long relied on these contacts in Al-BSF and now PERC architectures, recombination from these metallization schemes limits the upper limit of their efficiency to about 24.5% [21]. The metallization-induced recombination losses leave a significant gap to the silicon intrinsic limit of 29.4% [32]. In order to produce devices closer to the intrinsic efficiency limit of silicon, cells require contacts that limit recombination but still support carrier extraction. These contacts are called “carrier-selective passivating contacts” [31, 33, 34].

The most promising interlayers to passivate the silicon interface and conduct carriers are SiO_2/polysilicon (TOPCon architecture) or stacks of intrinsic and doped hydrogenated amorphous silicon (SHJ) [21]. The market share of each of these cell technologies is expected to increase over the coming decade, as seen in Figure 1-2 [4, 34]. Currently, the module prices for n-TOPcon and SHJ modules are \$0.293/Watt and \$0.311/Watt [22]. Although these architectures enable an efficiency improvement, translating this benefit at the industrial scale still comes at a higher cost, just as PERC did pre-2016. The non-silicon cost for TOPCon and SHJ are higher than PERC by about \$0.013/Watt and \$0.053/Watt, respectively [22]. Metallization accounts for a significant role in this gap, as these structures utilize metallized interfaces that are fundamentally different from traditional Al-

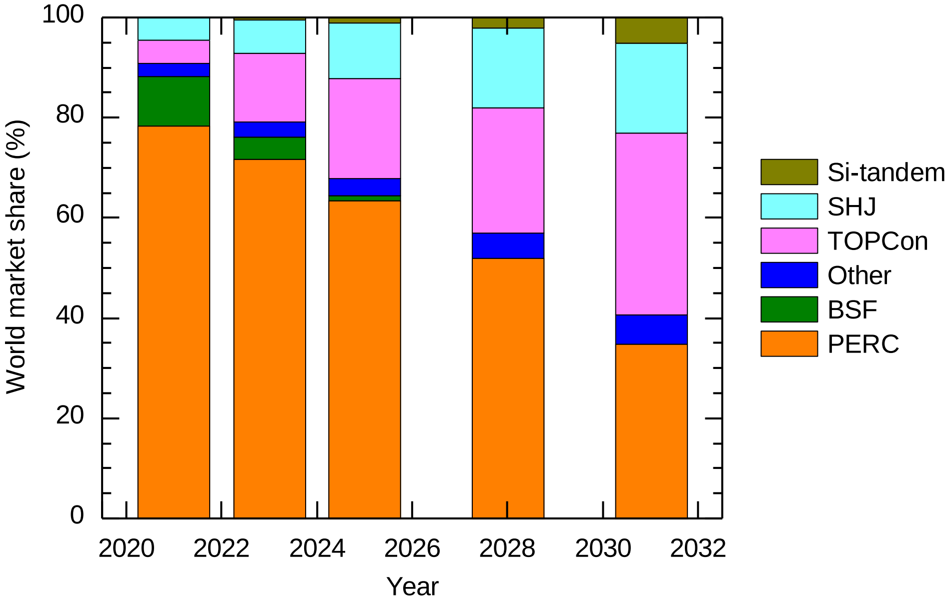


Figure 1-2. Projections of future world market share for different PV Technologies [4].

BSF and PERC. Thus, metallization is a dynamic research space with the primary goal being to drive down costs while simultaneously improving cell performance in order to enable these cell technologies to capture market share [35]. Regardless of the metallization approach, decades-long robust PV device operation—absorbing sunlight and producing electrical energy—is required.

1.2 Driving charge currents to metal electrodes

Photovoltaic solar cells convert thermal radiation into electrical power. To maximize energy conversion efficiency, the PV absorber should maximize the absorption of above bandgap light and the conversion of these photons into populations of electrons (n_e) and holes (n_h). These processes dictate upper limits for device current and internal voltage, respectively [36]. To perform external work, PV devices must direct the flow of the photogenerated electron and hole charge currents from the site of their generation in the absorber to their respective spatially separated metal electrodes, with minimal reduction of their electrochemical potential. [37].

Ideal contacts are designed to be passivating, conductive, and carrier selective. Passivation refers to the ability to maintain the maximum achievable quasi-Fermi level splitting of a given absorber material by minimizing non-radiative recombination at interfaces. Ideal performance is achieved when measured implied open-circuit voltage (iV_{oc}) is as close as possible to the maximal theoretical voltage ($V_{oc,ideal}$) of the absorber, a characteristic material property. Conductivity refers to minimizing the resistive losses experienced by the collected majority carriers through the contact. Contacts are conductive when series resistance (R_s) and fill factor (FF) losses are minimized. Selectivity refers to the ability to achieve the desired asymmetry of charge currents. Contacts are selective when they successfully route the charge carriers to their intended electrode, resulting in open-circuit voltage (V_{oc}) as close as possible to iV_{oc} [37]. Achieving these characteristics at the device level requires an internal mechanism to effectively drive carriers out of the absorber. The material properties to enable such mechanisms can be elucidated from the equations for electron and hole charge currents within a semiconductor material, j_e and j_h, respectively [38].

$$j_e = \frac{\sigma_e}{q} \nabla E_{F,e} = \frac{\sigma_e}{q} \frac{dE_{F,e}}{dx} \tag{1.1}$$

$$j_h = \frac{\sigma_h}{q} \nabla E_{F,h} = \frac{\sigma_h}{q} \frac{dE_{F,h}}{dx} \tag{1.2}$$

In Equation 1.1 (1.2), σ_e (σ_h) is electron (hole) conductivities, $E_{F,e}$ ($E_{F,h}$) is the electron (hole) quasi-Fermi level (qFL), and q is the elementary charge. These expressions for charge currents embody the total driving force on each respective carrier population. For simplicity, the expressions have been detailed in 1D here, though in real cells the gradients are often better described by 2D or 3D. For solar cells, the most impactful force contributions are the electric force and the generalized force from concentration gradients of particles via diffusion. These force contributions contained within the gradient of the qFL cannot be selectively applied to drive the electron and hole currents to different terminals except by applying an external bias. Thus, charge carrier separation must be achieved by establishing regions with a large difference in conductivity between each carrier type: an electron contact should have high electron conductivity and low hole conductivity, while the inverse should be true for the hole contact [37-39].

Conductivity of each charge carrier within a semiconductor is described by the product of mobility and carrier concentration.

$$\sigma_e = \mu_e n_e \tag{1.3}$$

$$\sigma_h = \mu_h n_h \tag{1.4}$$

Charge carrier density and mobility, the components of conductivity, represent the available levers to guide charge currents. Mobility, characterized in a first order approximation by the time between collisions with obstacles within the periodic lattice, cannot be varied between electrons and holes to a large extent within a single material [39]. As a result, tuning carrier concentrations within specific regions of a PV device is the primary approach of contact design.

As the electrical quality of silicon wafers has become extremely high, enabling longer bulk lifetimes and thinner wafers, recombination at surface and contact regions have become increasingly impactful for improving device performance [32]. The periodic lattice of the silicon absorber discontinues abruptly at its surface. The resultant dangling surface bonds contribute a semi-continuum of energy states within the bandgap [40]. These midgap energy states mediate recombination through “defect-assisted recombination”, described in early semiconductor research [41]. For a semiconductor surface, a common simplification of the full recombination statistics is made by lumping the activity of all surface defect states into a concentration of defects, D_{it}, localized to a single energy at the midgap energy level [40]. These defect energy levels have electron recombination velocity (S_{e0}) and hole recombination velocity (S_{h0}) shown here:

$$S_{e0} = v_{th} D_{it} \sigma_e \tag{1.5}$$

$$S_{h0} = v_{th} D_{it} \sigma_h \tag{1.6}$$

In Equation 1.5 and 1.6, $\sigma_{e/h}$ is the capture cross-section of electrons/holes and v_{th} is the thermal velocity. This relation reveals approaches to reduce surface recombination by reducing the amount of defect states or their capture probability. The (100) silicon surface has a density of bonds of approximately $7 \cdot 10^{14}$ cm^{-2} [39]. This can be lowered by several orders of magnitude by depositing a dielectric or semiconductor film at the silicon surface, where the introduction of the new chemical species at the interface can terminate the dangling silicon bonds through covalent bonding [39]. Another chemical passivation mechanism to reduce the density of defect states is a hydrogenation treatment. The small size of atomic hydrogen allows it to diffuse to dangling silicon bonds, further reducing surface defect density [39]. This is a near ubiquitous approach for surface passivation as seen in a-Si:H, SiN_x, Al_2O_3, and more.

The total surface recombination can be described by an effective surface recombination value [40]:

$$S_{eff} = \frac{1}{\Delta n_d} \frac{n_{e,s} n_{h,s} - n_i^2}{(n_{h,s} + n_i)/S_{h0} + (n_{e,s} + n_i)/S_{e0}}. \tag{1.7}$$

The steady-state carrier concentration at the surface for electrons and holes are $n_{e,s}$ and $n_{h,s}$, respectively. Surface charges create a space charge region of width d, where the excess minority carrier concentration at the edge of this region is Δn_d. The conclusion of tuning carrier concentration described above can also be seen through Equation 1.7, as surface recombination increases with increasing presence of both carrier types. The overall rate can be reduced by increasing the majority carrier concentration, which suppresses the minority carrier concentration and reduces the total surface recombination rates. The deliberate manipulation of carrier concentrations at a surface can be done by intentionally introducing impurity atoms through doping. Dopant diffusion near the surface of a wafer can change equilibrium carrier populations by over 8 orders of magnitude, increasing the lifetime of an unpassivated wafer from 1-3 microseconds to tens or hundreds of microseconds [42]. Although doped regions suppress surface-defect-assisted recombination, the high concentration of one carrier type leads to higher rates of Auger recombination. In addition to containing atomic hydrogen, dielectric films can possess positive or negative fixed charges. These charges attract carriers of the opposite type, creating a region where the carrier concentration of the one type is much larger than the other. Ranges for charge density, Q_f, and D_{it} for several materials deposited on the silicon

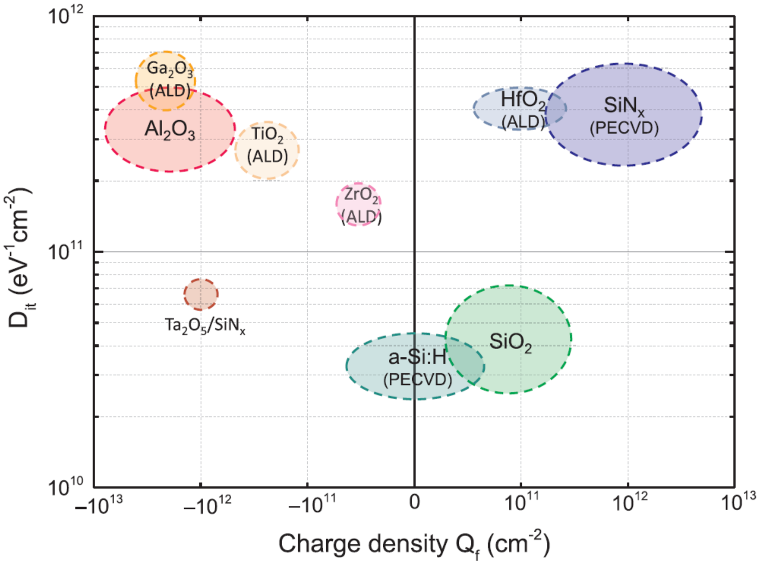


Figure 1-3. Ranges of measured fixed charge density and surface defect density for common surface passivation materials. Figure taken from Cuevas *et al.* [39].

surface are shown in Figure 1-3 [39]. This summarizes these material's capacity for chemical passivation and carrier population control via fixed charge. Additionally, differences in work function between the deposited contact material and the silicon absorber can induce carrier concentration asymmetries [43]. These mechanisms for chemical passivation and selective control of carrier populations are ubiquitously used in solar cell design.

Since metals cannot maintain separate qFL, any population of minority carriers that reach the opposite-polarity electrode will necessarily recombine as seen in Figure 1-3 [44]. Consequently, the electrical forces at the metal contact are the final determining factor of the device's voltage. Relatedly, the metallized-interface is a significant barrier contributing to resistive losses before extraction to the external load through the grid. Therefore, characterizing contact performance post-metallization is a crucial process for PV device optimization.

1.3 Quantifying post-metallization contact performance: ρ_c and $J_{0,met}$

The recombination parameter, J_0, is a common conceptualization to represent the degree of recombination between holes and electrons within a particular region of a device [45]. For metallized areas, this is commonly represented as $J_{0,met}$, while $J_{0,pass}$ represents a non-metallized, passivated region. J_0 was first used to describe the total recombination of a doped region and surface, designated as the emitter saturation current density, J_{0E} [46]. It was calculated from transient or quasi-steady-state photoconductance (QSSPC) data with a method proposed by Kane and Swanson and utilized frequently after [42, 46, 47]. The original application relied on measuring transient photoconductance of specialized test structures and isolating an injection-level range (10 times the base doping) where emitter recombination is dominant over the remaining defect-assisted recombination after subtracting out Auger and radiative contributions with analytical models. This approach, known as the Kane and Swanson technique, has been modified to include more exact modelling of several processes including Auger recombination and bandgap narrowing, with the following expression being implemented directly in Sinton WCT-120 lifetime testers [48, 49].

$$J_0 = qW \frac{d}{d\Delta n_{av}} \left(\frac{n_{i,eff}^2}{\tau_{corr}} \right). \qquad 1.8$$

In Equation 1.8, W is sample thickness, Δn_{av} is average excess carrier density, $n_{i,eff}$ is the effective intrinsic carrier concentration, and τ_{corr} is the Auger-corrected lifetime. Though designed to capture recombination of doped regions/surfaces, the applicability of this method was argued to extend to non-diffused samples provided they have sufficiently high surface charge, thereby inducing a depletion region physically similar to a doped layer [50]. In that study, J_0 of an undiffused n-type silicon sample coated with symmetric Al_2O_3 was extracted using the modified Kane and Swanson technique from Equation 1.8. This J_0 was referred to as the surface saturation current density, J_{0s}, and was introduced as an analog to J_{0E} [50]. Since then, this approach has been used to quantify J_0 (J_{0s} or $J_{0,\mathrm{pass}}$) for many dielectric materials on wafers with dopant diffusions [51-53]. It is also commonly used to quantify surface recombination for passivating contacts. Some attempts have been made to apply this technique to metallized samples by using very thin metal layers or patterned point-contact structures [54-56].

In general, this approach is limited for passivation contacts, even without metallization, as the injection level of device operation is higher and the ability to reliably distinguish between different recombination mechanisms from a single global measurement becomes lower. Its accuracy is also limited for metallized structures as the founding assumption of uniform excess carrier density along the surface are almost always violated after metallization [57]. Further, the QSSPC-based approach relies on inductively coupled measurements of sample conductivity and the high conductivity of metallized samples make measurements difficult or impossible [58]. Consequently, $J_{0,met}$ measurements are more typically accessed through luminescence behavior.

Photon emission occurs when carriers recombine from the conduction band to the valence band via radiative recombination. From a thermodynamic view, the efficiency of external luminescence, or external radiative efficiency, η_{ext}, relates iV_{oc} to $V_{oc,ideal}$ calculated from the material's detailed balance limit [59].

$$iV_{oc} = V_{oc,ideal} - kT\left|\ln \eta_{ext}\right| \tag{1.9}$$

For a solar cell at open-circuit voltage, radiative recombination efficiency should be as high as possible, otherwise, incident photons are being wasted in parasitic optical absorption or exciting carriers that recombine nonradiatively, such as at a metal interface [60]. In photoluminescence (PL) characterization, samples are optically excited to a steady-state and the emitted luminescence is captured. The result is high-resolution image of radiative recombination, which with calibration, can be converted to lifetime or iV_{oc} [58]. With a calibrated relationship between area-averaged PL signal and iV_{oc}, metallization-induced voltage losses can be quantified. These approaches rely on making measurements of multiple identically-processed-samples varying only in their metallization area fraction. The area of the passivated region can be calibrated with QSSPC or with full-device simulations through finite element modelling [61-65]. Although this requires complex calibration procedures, it is compatible with many sample sizes, metallization deposition techniques, and contact geometries. As a consequence $J_{0,met}$ from luminescence data is increasingly common to quantify metallized-induced recombination losses.

The other primary metric for metallized-contact description is specific contact resistivity, ρ_c, which quantifies the resistive loss of majority carriers across the metal interface. This value is generally calculated via the transfer length method (TLM) or Cox and Strack method [66, 67]. The large number of degrees of freedom at a semiconductor/metal interfaces (dangling bonds, metal induced gap states, interface dipoles) make predictions of contact resistivity based purely on bulk and surface electronic properties difficult [68]. Consequently, demonstrating contact resistance performance is a crucial step in development of a metallization system. To minimize measurement errors, the current path of test structures should replicate the current transport environment of a full device as closely as possible. An understanding between the interplay of semiconductor sheet resistance, expected contact resistivity, and metal pad geometry (length and width) can help design test structures to minimize measurement error. For TLM, measurement errors can be minimized by ensuring pad length is more than 2.5-fold greater than the transfer length, and that structures with several pad widths near the optimal width from simulations are fabricated [69].

Quantifying these contact properties for a given metallization scheme allows for the optimization an additional cell parameter—the metallized area fraction, c_f—that can also be used to optimize device performance. Together, these parameters provide a powerful framework to design, fabricate, and evaluate PV devices. Figure 1-4 shows how cell efficiency changes with the contact performance. Also shown are upper-limit voltage and the c_f in the black and gray contour lines, respectively. Minimizing $J_{0,met}$ and ρ_c is desirable, but without being able to fabricate ideal performance, understanding their tradeoffs is important to use cell design to drive better performance. For instance, higher ρ_c can be tolerated if $J_{0,met}$ is low and full-area contacts are used. If ρ_c is low and $J_{0,met}$ is high, then minimizing c_f is desired, such as in PERC.

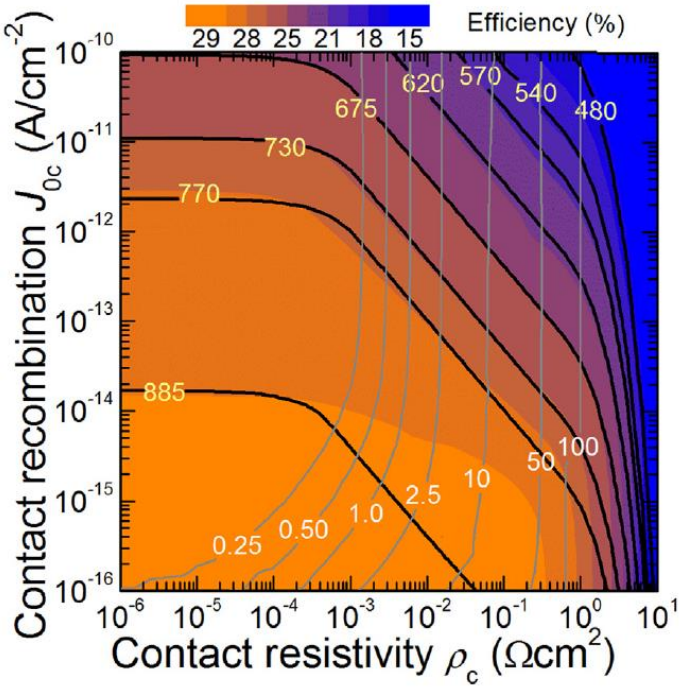


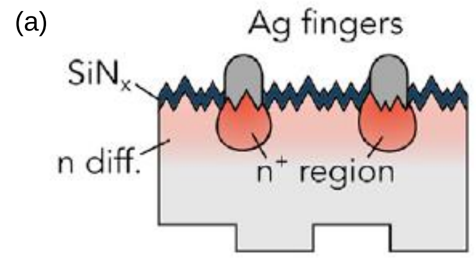
Figure 1-4. Contour plot mapping the idealized efficiency of a silicon solar cell for combinations of J_{0c} and ρ_c, with c_f and upper-limit voltage contours also shown in black and gray, respectively. Figure taken from Cuevas *et al.* [39].

1.4 State of the Art of Silicon Solar Cell Metallization

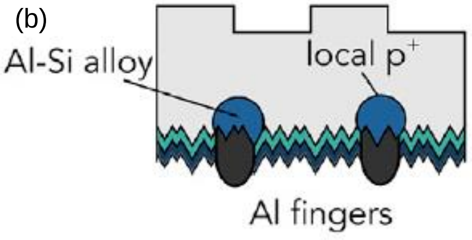
Screen-printing is the dominant technology for silicon solar cell metallization for its ability to deposit laydown metals across large areas at high-throughput (8,000 wafers per hour) and high performance (35 micron finger width with 10 micron alignment precision)

[4]. Metallization of PERC solar cells uses Ag paste on the front-side for the electron contact and Al paste on the rear side for the hole contact [4]. The front-side Ag paste contains glass frit, which, during firing, etches through the SiN_x film and creates an opening to the silicon surface. Some of the Ag powder is dissolved during firing which crystallizes on the highly-doped n+ region of the silicon wafer or precipitates within the glass, which also serves to improve adhesion to the wafer [70]. Also during high-temperature firing, the Al paste forms a eutectic alloy with silicon; during cooling, silicon epitaxially recrystallizes at the silicon wafer surface and incorporates Al dopants according to the Al solid solubility limit and creates a heavily doped p-type layer [5]. Figure 1-5 (a) and (b) shows typical performance of Ag and Al metallization for the electron and hole contact, respectively. While the Ag and Al paste can achieve low contact resistivity, $J_{0,met}$ is significantly higher than $J_{0,pass}$ for both metallization schemes due to the direct metal contact to the silicon absorber, which creates a large density of midgap defect states.

While there are opportunities to improve PERC metallization losses through improved doping profiles, optimal metallization depths, and reduced finger linewidths, these improvements are increasingly difficult as the cell performance become increasingly closer to the technology's upper limit dictated by the metal-Si recombination [24]. As a consequence, an appealing approach to improve energy generation is to focus on the fielded energy of PERC cells through thermal management. The operating temperature of a fielded solar cell is typically much higher than during standard test conditions, which causes power losses and accelerates degradation. The metal contacts can play an optothermal role by maximizing the rejection of sub-bandgap light, thereby reducing the module operating temperature. Chapter 2 focuses on a practical model to isolate the impact of sub-bandgap reflectance on operating temperature of fielded modules from an energy balance between the module and the ambient consisting of module and meteorological quantities that are standard to measure. Chapter 3 then focuses on implementing this thermal management



$J_{0,pass} = 22$ fA/cm^2
$J_{0,met} = 500$ fA/cm^2
$\rho_c = 1.5$ mΩ·cm^2
$c_f = 3\%$
$J_{0,total} = 36$ fA/cm^2

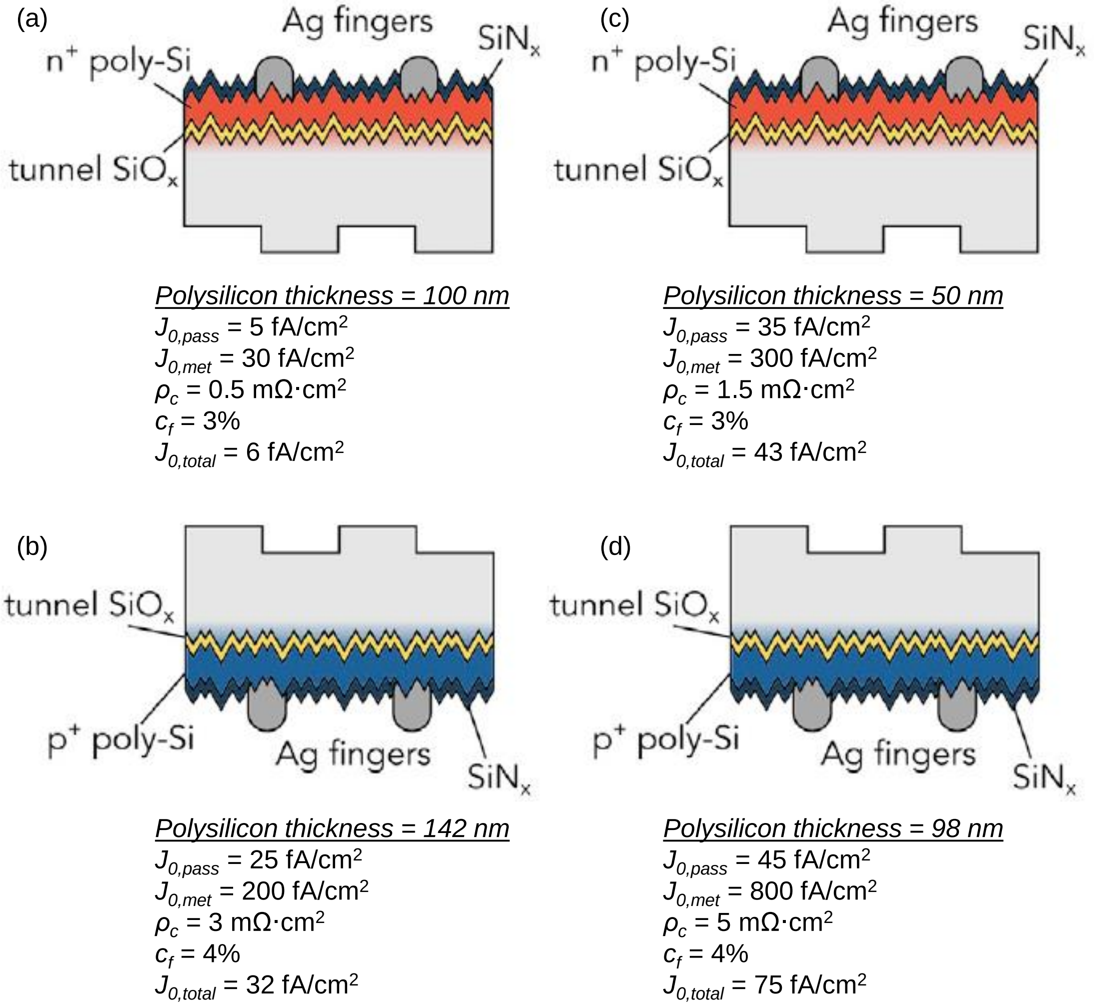


$J_{0,pass} = 12$ fA/cm^2
$J_{0,met} = 400$ fA/cm^2
$\rho_c = 1.3$ mΩ·cm^2
$c_f = 4\%$
$J_{0,total} = 28$ fA/cm^2

Figure 1-5. Schematic and contact properties of a typical PERC (a) electron contact and (b) hole contact. Figure taken from D. Yan *et al*. [36]. Data taken from Dullweber *et al.* [71].

approach experimentally by adding a dedicated optical layer to the rear contact stack of a PERC-like cell. While minimizing the contact fraction of the metallized area in PERC cells can limit the total recombination losses ($J_{0,total}$), these high $J_{0,met}$ values show how important it is to separate the metal terminals from the silicon surface for improved performance.

TOPCon structures separate the metal electrode from the silicon wafer and use Ag paste for both contacts, eliminating the Al paste used for PERC. In initial TOPCon metallization work, the same fire-through Ag paste chemistries used for PERC were adopted to TOPCon structures with 200-nm-thick poly-Si layers, resulting in high $J_{0,met}$ around 385 fA/cm^2 [34]. As a result, dedicated effort to optimize Ag fire-through paste chemistries specifically for



(a) *Polysilicon thickness = 100 nm*
$J_{0,pass}$ = 5 fA/cm^2
$J_{0,met}$ = 30 fA/cm^2
ρ_c = 0.5 mΩ·cm^2
c_f = 3%
$J_{0,total}$ = 6 fA/cm^2

(c) *Polysilicon thickness = 50 nm*
$J_{0,pass}$ = 35 fA/cm^2
$J_{0,met}$ = 300 fA/cm^2
ρ_c = 1.5 mΩ·cm^2
c_f = 3%
$J_{0,total}$ = 43 fA/cm^2

(b) *Polysilicon thickness = 142 nm*
$J_{0,pass}$ = 25 fA/cm^2
$J_{0,met}$ = 200 fA/cm^2
ρ_c = 3 mΩ·cm^2
c_f = 4%
$J_{0,total}$ = 32 fA/cm^2

(d) *Polysilicon thickness = 98 nm*
$J_{0,pass}$ = 45 fA/cm^2
$J_{0,met}$ = 800 fA/cm^2
ρ_c = 5 mΩ·cm^2
c_f = 4%
$J_{0,total}$ = 75 fA/cm^2

Figure 1-6. Schematic and contact properties of a typical TOPCon (a) electron contact with 100-nm-thick poly-Si(n), (b) hole contact with 142-nm-thick poly-Si(p), (c) electron contact with 50-nm-thick poly-Si(n), and (d) hole contact with 98-nm-thick poly-Si(p). Figure taken from D. Yan *et al.* [36]. Data taken from P. Padhamnath *et al.* [72, 73].

TOPCon structures has become a major research topic [34, 35]. Figure 1-6 shows typical electron and hole contact performance for different poly-Si thicknesses, revealing significant improvement over the initial efforts with PERC paste. However, below 100 nm for poly-Si(n) and 150 nm for poly-Si(p), $J_{0,met}$ increases significantly due to etching of poly-Si and damaging of the SiO_x passivation [72, 73]. Poly-Si thickness over 100 nm is prohibitively thick for the front side of a solar cell as parasitic absorption in the doped poly-Si layer reduces short-circuit current (J_{sc}) by about 0.5 mA per 10 nm of poly-Si thickness [74, 75]. As a result, TOPCon structures will be unattractive for the front side of a cell until the etching mechanism of fire-through metallization pastes can be sufficiently controlled to enable cells with thinner poly-Si layers with minimal difference between $J_{0,met}$ and $J_{0,pass}$ (assuming low $J_{0,pass}$). Chapter 4 focuses on this challenges through use of a low-temperature contact process that can be applied to thin poly-Si without damaging passivation.

Instead of fire-through paste, SHJ cells rely on low-temperature paste as the high-quality surface passivation provided by the hydrogenated amorphous silicon films degrades at temperatures over 200 °C [76]. Figure 1-7 (a) and (b) show a typical SHJ electron contact and hole contact, respectively, along with representative contact performance with low-temperature Ag metallization. Since the SHJ metallization process relies on making physical contact to the underlying TCO layer (typically ITO), it does not cause passivation damage. Sputtering ITO, however, does induce passivation damage, but these losses are recovered during the curing of the low-temperature paste [77]. As a consequence, the difference between $J_{0,met}$ and $J_{0,pass}$ is generally minimal. The more significant contact performance issue is contact resistivity, which can contribute to the majority of series resistance losses [78]. Further, the cost of SHJ technology is still high ($0.311/Watt) and its reliance on scarce materials including In and Ag make its ability to sustain the growing PV market tenuous [22, 79]. Chapter 5 focuses on this issue by investigating In- and Ag-free SHJ metallization via sputtering of Al.

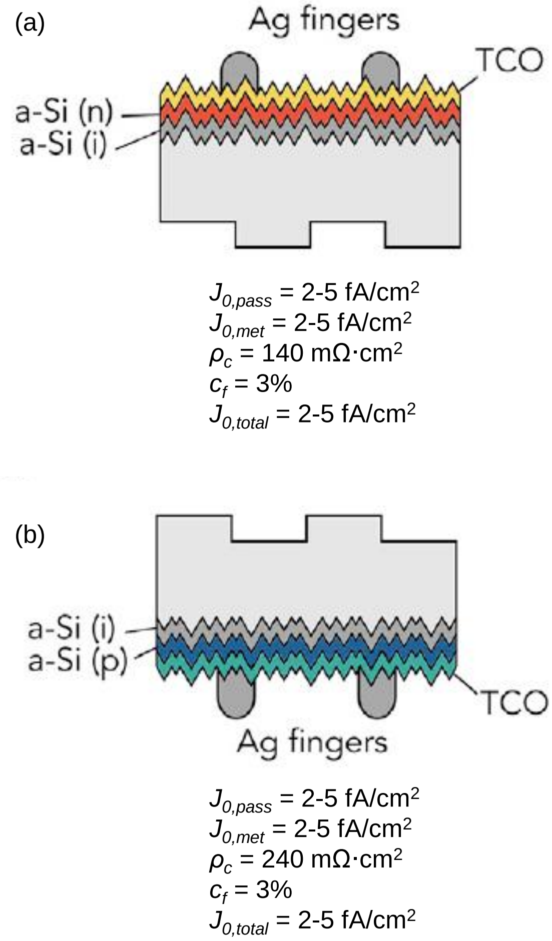


Figure 1-7. Schematic and contact properties of a typical SHJ (a) electron contact and (b) hole contact. Figure taken from D. Yan *et al.* [36]. Data taken from Lachenal *et al.* [78].

CHAPTER 2

THERMAL MODEL TO QUANTIFY THE IMPACT OF SUB-BANDGAP REFLECTANCE ON OPERATING TEMPERATURE OF FIELDED PV MODULES

2.1 Introduction

The operating temperature of photovoltaic (PV) modules affects the lifetime energy output of a PV system through its influence on energy conversion efficiency and degradation. For most PV cell structures, power output decreases with increased temperature [80]. Elevated temperature influences multiple PV conversion steps, but the most detrimental to performance is the reduction of the absorber's photogenerated carrier population from its theoretical maximum at open circuit, resulting in significant voltage loss [81]. Further, higher operating temperature accelerates most major module degradation mechanisms, including corrosion, encapsulant discoloration, delamination, and breakage, though direct correlations are difficult to ascertain due to complex interdependencies [82-84]. For instance, solder fatigue damage has been shown to depend on maximum daily temperature, maximum daily temperature range, and number of temperature reversals across a characteristic temperature, and not simply on average operating temperature [85]. In another study, field-aged BP Solar crystalline silicon (c-Si) modules underwent accelerated UV testing at three temperatures; the accelerated testing at higher temperatures showed increased rates of encapsulant browning, resulting in relative short-circuit current drops of 3.26% at 85 °C and 1.37% at 60 °C [86]. In addition to degradation that reduces energy production, thermal stresses can also induce secondary degradation mechanisms that lead to safety failures such as arcing or shorting in the module laminate or junction box. Lastly, it is worth noting that a sound prediction of operating temperature leads to more accurate predictions of power delivery, which is important to many downstream stakeholders [87].

PV module operating temperature is determined by the meteorological conditions (such as irradiance, ambient temperature, wind speed, and humidity), the module properties (such as efficiency, reflectance, temperature coefficient, emissivity, and thermal conductivity), and the installation configuration (such as tilt angle, mounting structure, and distance from the ground). Though these factors are numerous, three in particular largely dominate: the solar irradiance, the ambient temperature, and the wind speed [88]. Their large impact on operating temperature, coupled with the fact that they are explicit variables, makes these three factors the most commonly chosen for inputs in module temperature models. The remaining variables are generally not treated directly. Instead, their impacts are combined into empirical coefficients, which achieves a reasonable balance between practicality and physical accuracy.

This approach is applied in the IEC 61215-2 standard for Nominal Module Operating Temperature (NMOT), where module temperature is modeled as

$$T_{module} = T_{ambient} + \frac{G}{u_0 - u_1 v_w}. \tag{2.1}$$

T_{module}, $T_{ambient}$, G, and v_w represent the PV module temperature, ambient temperature, irradiance, and wind speed, respectively. The coefficients u_0 and u_1 are weighting factors for irradiance and wind speed, respectively, with site and seasonal impacts embedded within. These coefficients are derived empirically from data collected by reference modules for a period of at least six months. The installation properties, data-collection apparatuses, data-collection procedures, and data-filtering techniques are standardized according to IEC 61853-2 and aim to minimize deviations from the steady-state thermal equilibrium approximation [89]. The derived coefficients can then be used to calculate the expected performance of measured modules under any conditions, including the NMOT standard reference environment: irradiance of 800 $W \cdot m^{-2}$, wind speed of 1 $m \cdot s^{-1}$, and ambient temperature of 20 °C. Similar models using irradiance, ambient temperature, and wind speed as input factors and employing empirical correction coefficients have been developed by other researchers [90-92].

This modelling approach is useful for predicting operating temperature (and, subsequently, energy output) of planned systems, and, consequently, for comparing the thermal performance of different module technologies. However, it does not allow the thermal impacts of specific differences in module technologies to be examined. Other models of module temperature have been developed that also include experimentally measured or estimated implicit variables; these enable more resolution surrounding particular features of a PV system [93, 94]. For instance, efficiency is an important PV module quantity that links irradiance to waste-heat generation. In some module temperature models, the instantaneous measured efficiency is used [95], whereas in others the manufacturer-supplied STC efficiency is used [96]. Similarly, measured values can be included to derive descriptions of heat transfer between the module under test and the ambient, a process dominated by wind-forced convection and generally described as a function of wind speed [97]. In prior work, wind speed and actual measured waste heat (irradiance less power production) were used to derive a heat transfer function, which was also statistically optimized to capture a linearized radiative contribution [98]. Module optical properties have also been included in models, most notably in the Duffie-Beckman model [99]. In this model, the effective transmittance-absorptance term, τα, represents how much incident radiation transmits through the module materials above the cell and how much of that transmitted irradiance is subsequently absorbed by the cell itself. This quantity should vary based on the spectral content and module materials, but in practice, is most commonly assumed to be 0.9 to simplify calculations [96].

Missing from these models is a direct treatment of a particularly important module property: reflectance. More specifically, reflection of light with energy below the PV cell's bandgap energy—"sub-bandgap" reflection—is important because it is a parameter that PV engineers can control by modifying the cell or module materials. What's more, sub-bandgap reflection has recently been shown to have the greatest impact of any module property on thermal performance [100, 101]. In simulations performed by Silverman *et al.*, adding an ideal sub-bandgap reflector to a reference c-Si module reduced annual irradiance-weighted module temperature by 3.8 ºC [100]. This translates to a relative energy improvement (ratio of additional energy generated by the ideal module to total energy generated by reference module) of 1.7% and an estimated increase in time to failure of between 26% and 200% [100]. Thus, it is expected that appreciable future work on reducing module operating temperature will be oriented around reflecting light that is unusable for PV energy conversion. Indeed, simulation and initial experimental work toward this end has already been performed [102-104]. In outdoor measurements, a 12-layer photonic mirror fabricated on the module cover glass reduced operating temperature by 1.5 °C relative to a bare-glass reference module, though this was computed with a different method from the standard energy balance [105].

Given the considerable importance of reflectance on operating temperature, a full model that quantifies its impact during realistic outdoor testing would be a useful tool to evaluate thermal modifications focused on reducing sub-bandgap absorption. This chapter describes the development of a thermal model based on the standard fundamental energy balance, notably including a term for reflectance. This model is used to develop a method for comparing the temperature performance of modules on the basis of their reflectance from measured outdoor data. The approach here uses a correction factor, which eliminates variation from the significant factors other than reflectance.

2.2 Model

2.2.1 Model derivation

The steady-state energy balance of a PV module that is dissipating waste heat to its surroundings is

$$P_{in} = P_{out} + Q_{loss} . \tag{2.2}$$

where P_{in} is the power entering the module, P_{out} is the extracted electrical power, and Q_{loss} is the generated waste heat. These are given by

$$P_{in} = E_{POA}[1 - R], \tag{2.3}$$

$$P_{out} = E_{POA}\eta , \tag{2.4}$$

$$Q_{loss} = \frac{1}{c(v_w)}[T_{module} - T_{ambient}] . \tag{2.5}$$

$T_{ambient}$ is the ambient air temperature, v_w is wind speed, and E_{POA} is the plane-of-array irradiance; T_{module} and η are the module temperature, and efficiency, respectively. R is the spectral-irradiance-weighted reflectance, which represents the total reflectance of the module at any instant. This parameter depends on angle of incidence and incident spectrum, but can be, to a large degree, engineered in the cell and module material and design selection. In particular, the sub-bandgap reflectance should be as close to 100% as possible, while the above-bandgap reflectance is typically small and should be as close to 0% as possible. Thus, while the parameter R in our model refers to total reflectance, it is in fact dominated by sub-bandgap reflectance. For monofacial PV modules, transmittance is zero and can be neglected from the model. The factor $1/c(v_w)$ represents a lumped heat transfer coefficient and is the same for modules having identical packaging, deployment configurations, deployment locations, and sky conditions. This factor can be derived from measured data as described in previous work [98]. From this energy balance, the module temperature rise above ambient, ΔT, can be written as:

$$\Delta T = T_{module} - T_{ambient} = E_{POA} \times [1 - R - \eta] \times c(v_w)\ . \tag{2.6}$$

In Equation 2.6, module efficiency has an impact on the module temperature rise above ambient. The converse is also true: efficiency is reduced at higher temperature, in proportion to the cell's temperature coefficient, γ [106]:

$$\eta(T_{module}) = \eta_{STC}\{1 + \gamma[T_{module} - T_{STC}]\}\ . \tag{2.7}$$

Here, η_{STC} is the module efficiency at the standard-test-condition temperature, T_{STC} (typically 25 °C). To account for the interaction between temperature and efficiency, Equation 2.7 is inserted into the efficiency term, η, in Equation 2.6 which yields the following expression for temperature rise:

$$\Delta T = \frac{T_{ambient} + c(v_w)E_{POA}\{1 - R + \eta_{STC}[\gamma T_{STC} - 1]\}}{1 + c\left(v_w\right)E_{POA}\eta_{STC}\gamma} - T_{ambient}\ . \tag{2.8}$$

With this thermal balance, the expected temperature rise for any given set of conditions (E_{POA}, $T_{ambient}$, and v_w) and module properties (R, η_{STC}, γ) can be computed. Further, a reference temperature rise for a corresponding set of reference conditions and module properties can be chosen, and then, following outdoor testing, sets of measured values can be corrected back to this defined reference state. In this work, the reference parameters are denoted with superscript (A), while the measured parameters are denoted with superscript (B). This correction technique enables systematic differences in thermal performance of modules that have different properties or were measured under different conditions to be extracted from large data sets and quantified as a temperature difference. Mathematically, the correction is performed by taking the difference between the measured values of module temperature and ambient temperature, $\Delta T^{(B)}$, and multiplying that by a correction factor f, as follows:

$$\Delta T^{(A)} = (T_{module}^{(B)} - T_{ambient}^{(B)}) \times f \ . \tag{2.9}$$

This expression for corrected temperature rise above ambient, $\Delta T^{(A)}$, represents what the temperature rise of the module *would have been* if it had the same properties as the reference module and had been measured under the same reference conditions. By rearranging this expression, the correction factor, f, can be found:

$$f = \frac{\Delta T^{(A)}}{\Delta T^{(B)}} \ . \tag{2.10}$$

The complete correction factor, including the reflectance term, is then found by substituting the most rigorous expression of ΔT from Equation 2.8:

$$f_{complete+R} = \frac{E_{POA}^{(A)}}{E_{POA}^{(B)}} \times \frac{c(v_w^{(A)})}{c(v_w^{(B)})} \times \frac{1 - R^{(A)} - \eta_{STC}^{(A)}\{\gamma^{(A)}[T_{ambient}^{(A)} - T_{STC}] + 1]\}}{1 - R^{(B)} - \eta_{STC}^{(B)}\{\gamma^{(B)}[T_{ambient}^{(B)} - T_{STC}] + 1]\}} \times \frac{1 + c(v_w^{(B)})E_{POA}^{(B)}\eta_{STC}^{(B)}\gamma^{(B)}}{1 + c(v_w^{(A)})E_{POA}^{(A)}\eta_{STC}^{(A)}\gamma^{(A)}} . \qquad 2.11$$

The correction factor, $f_{complete+R}$, is designed to account for all differences that can lead to variations in the measured $\Delta T^{(B)}$ of modules outdoors. Applying $f_{complete+R}$ to given sets of measured data should ideally result in no variations in $\Delta T^{(A)}$ for different types of modules measured under different conditions; after correction, it is as if identical performing modules were measured in identical ambient conditions. The larger the deviation of the correction factor from 1, the more the measurement conditions or module properties varied from the chosen references. However, while measuring and correcting differences in irradiance, wind speed, ambient temperature, STC efficiency, and temperature coefficient is straightforward, reflectance cannot be readily corrected as there is no practical method to measure it in an outdoor installation. While it can be estimated from laboratory measurements, the instantaneous value in an outdoor setting will vary widely with angle of incidence (and thus time of day) and the proportion of diffuse and direct light. Thus, in order to mathematically extract the impact of reflectance in outdoor measurements, R is eliminated from $f_{complete+R}$ and a new correction factor, $f_{complete}$, is established, shown in Equation 2.12. In other words, it is assumed that $R^{(A)} = 0$, physically signifying that the reference module is corrected to absorbs all incident solar irradiance. In practice, the tested PV modules will indeed reflect some of the incident irradiance, which will manifest in the measured values of module temperature, from Equation 2.9. However, these deviations in temperature between different modules due to R will go uncorrected by $f_{complete}$, while deviations due to all other factors will be corrected. As a result, the impact from *R* will propagate through to $\Delta T^{(A)}$; differences in $\Delta T^{(A)}$ between modules will be entirely due to differences in their reflectances.

$$f_{complete} = \frac{E^{(A)}_{POA}}{E^{(B)}_{POA}} \times \frac{c(v^{(A)}_{w})}{c(v^{(B)}_{w})} \times \frac{1-\eta^{(A)}_{STC}\{\gamma^{(A)}[T^{(A)}_{ambient}-T_{STC}]+1\}}{1-\eta^{(B)}_{STC}\{\gamma^{(B)}[T^{(B)}_{ambient}-T_{STC}]+1\}} \times \frac{1+c(v^{(B)}_{w})E^{(B)}_{POA}\eta^{(B)}_{STC}\gamma^{(B)}}{1+c(v^{(A)}_{w})E^{(A)}_{POA}\eta^{(A)}_{STC}\gamma^{(A)}} \qquad 2.12$$

The complexity of $f_{complete}$ arises from the bi-directional dependence of cell efficiency and cell temperature. Whether such a rigorous expression is actually needed in practice is now examined. To do this, a simplified correction factor, f_{simple}, is established, given by

$$f_{simple} = \frac{E^{(A)}_{POA}}{E^{(B)}_{POA}} \times \frac{c(v^{(A)}_{w})}{c(v^{(B)}_{w})} \times \frac{1-\eta^{(A)}_{STC}}{1-\eta^{(B)}_{STC}} . \qquad 2.13$$

The simple correction factor uses STC efficiency in place of the temperature-dependent efficiency from Equation 2.7. This is equivalent to eliminating variations in ΔT that arise from temperature coefficient, or, mathematically, letting $\gamma^{(A)} = \gamma^{(B)} = 0$ in Equation 2.12. This simplifying assumption has also been made by Akhasassi *et al.* in several module temperature models, and it produced satisfactory results [96].

2.2.2 Sensitivity analysis and f_{simple} validation

To examine the impact that each parameter in Equation 2.8 has on ΔT, and to assess the validity of simplifying the correction factor to f_{simple}, we performed a sensitivity analysis. To do this, each variable in Equation 2.8 was varied above and below a defined reference value and the corresponding change in ΔT was calculated. The variations from the reference values used are the calculated standard deviations of a data set chosen to be reasonably representative of expected variations of module properties and ambient conditions in the field. More specifically, the reference values for E_{POA}, v_w, and $T_{ambient}$, were chosen to be the same as NMOT, and the standard deviations for these factors were calculated from measured data taken between October 17, 2018 and January 1, 2019 in Golden, Colorado. Only irradiance values greater than 500 $W \cdot m^{-2}$ were used in the calculation since those times dominate power production. The fitted function $c(v_w)$ was also derived from this data set using three c-Si mini-modules. The module properties η and γ were calculated from the data sheets of three industrial c-Si modules that represent the range of module performance presently available on the market. The modules used were Q Cells Q.Power Al-BSF, JA Solar mono-PERC, and Trina Solar i-TOPCON [107-109]. The reference and variation values for the module properties were the calculated average and standard deviation from these three modules, respectively. For R, the reference value and standard deviation were calculated from AM1.5G-weighted reflectance measurements of optical test structures representative of Al-BSF, PERC, and SHJ solar cells, reported in prior work [110].

The resultant tornado plot from the sensitivity analysis is shown in Figure 2-1, with the reference values listed in the caption. As expected, irradiance has the most impact on ΔT, followed by wind speed. However, taking into consideration the expected range of values that each quantity may theoretically assume, we find reflectance to be nearly as important. Here, a 4.9% absolute change in R results in a 1.08 °C change in temperature rise above ambient. This large effect of R on ΔT justifies the effort here to develop a model that isolates the impact of this factor. Conversely, we find the expected variations in temperature rise from temperature coefficient to be inconsequential, especially relative to the other factors. Changing temperature coefficient from -0.37 to -0.395 %/°C changes ΔT

by 0.01 °C. In order to get a 1 °C change in ΔT from the defined reference condition, the temperature coefficient would have to deviate drastically, from -0.37 to -2.7 %/°C. In the other direction, changing temperature coefficient from -0.37 %/°C to 0 changes ΔT by 0.2 °C.

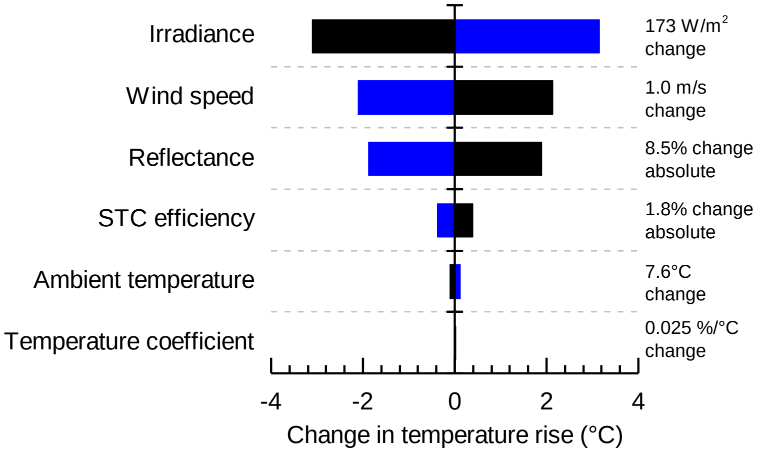


Figure 2-1. Tornado plot showing variation in ΔT due to variations in each factor of the complete thermal model. The reference values are: E_{POA} = 800 W·m^2, v_w = 1 m·s^{-1}, R = 16.2%, η_{STC} = 19%, $T_{ambient}$ = 20 °C, γ = -0.37 %/°C, and ΔT = 17.8 °C.

To ensure the efficiency simplification is robust in practice, we compare the impact that extreme combinations of measured values have on the correction factors $f_{complete}$ and f_{simple}, as shown in Table 2-1. Consistent with the low sensitivity of ΔT to temperature coefficient, f_{simple} (which omits γ) is always within 0.4% of $f_{complete}$ (which includes γ) for variations in γ of up to 35%, all other parameters held constant. Even in the cases with the most extreme combinations of measured values for all parameters, $f_{complete}$ and f_{simple} are always within 3% of each other. Thus, the difference in temperature that arises from a difference in temperature coefficient is expected to be negligible. This conclusion is in agreement with prior results from Silverman *et al.*, where a 50% decrease in temperature coefficient resulted in only 0.1 °C temperature improvement relative to a baseline module

Table 2-1. Comparison of correction factors.

E_{POA} (W·m^{-2})	v_w (m·s^{-1})	$T_{ambient}$ (°C)	η_{STC} (%)	γ (%/°C)	$f_{complete}$	f_{simple}	**Diff. (%)**
800	1	20	19	-0.37	*1*	*1*	0
500	1	20	19	-0.37	*1.61*	*1.60*	0.58
100	1	20	19	-0.37	*8.11*	*8.00*	1.34
1200	1	20	19	-0.37	*0.66*	*0.67*	0.78
800	0.25	20	19	-0.37	*0.90*	*0.90*	0.17
800	3	20	19	-0.37	*1.42*	*1.41*	0.45
800	1	0	19	-0.37	*1.02*	*1.00*	1.74
800	1	40	19	-0.37	*0.98*	*1.00*	1.74
800	1	20	13	-0.37	*0.93*	*0.93*	0.33
800	1	20	25	-0.37	*1.08*	*1.08*	0.30
800	1	20	19	-0.25	*1.00*	*1.00*	0.36
800	1	20	19	-0.50	*1.00*	*1.00*	0.40
800	1	20	25	-0.25	*1.08*	*1.08*	0.15
800	1	20	13	-0.50	*0.93*	*0.93*	0.056
500	3	20	19	-0.37	*2.28*	*2.26*	0.86
1200	0.25	20	19	-0.37	*0.595*	*0.60*	1.04
500	3	0	19	-0.37	*2.32*	*2.26*	2.59
1200	0.25	40	19	-0.37	*0.58*	*0.60*	2.81
500	3	0	25	-0.25	*2.51*	*2.44*	2.58
1200	0.25	40	13	-0.50	*0.55*	*0.56*	2.42

in simulation Silverman *et al.*, where a 50% decrease in temperature coefficient resulted in 0.1 °C temperature improvement relative to a baseline module in simulation [100].

The weak impact of temperature coefficient stems from the main physical process that influences it. Temperature coefficient is most strongly correlated with bandgap, as it is the bandgap that determines the required energy for thermal excitation of carriers. As module temperature increases, the PV absorber’s bandgap decrease while thermal excitation and intrinsic carrier concentration increase, resulting in decreased cell voltage. The rate at which voltage (and ultimately efficiency) is reduced with increasing temperature will thus not be drastically different for absorbers with the same bandgap, especially compared to the degree to which ambient factors change cell temperature. Thus, when all modules under test have the same absorber, the f_{simple} correction can safely be applied. In fact, since temperature rise is quite insensitive to temperature coefficient, the f_{simple} correction is applicable except in extreme cases. Using the f_{simple} correction rather than $f_{complete}$ simplifies the model implementation, but also reassigns temperature variations arising from temperature-dependent electrical performance from γ to waste heat rejection via (primarily sub-bandgap) reflection. The reduction of waste heat in the module occurs in two ways: by first reducing parasitic absorption of sub-bandgap light in the module and subsequently by enabling the cell to operate at a higher efficiency, thereby creating less waste. The simple version of this model attributes both of these sources of temperature increase to the module reflectance, though the former is expected to be significant and the latter, virtually negligible, as emphasized above.

2.3 Conclusions

There is a large opportunity to reduce the operating temperature of installed PV modules by rejecting as much unusable light as possible. We developed a model to quantify systematic temperature differences between fielded modules due to reflectance, which can help facilitate the practical realization of this potential temperature benefit. This approach uses a correction technique to transform large, highly variant, and unpredictable outdoor data sets to operating temperature values at the most relevant power-generating conditions. It can be applied to modules with significantly different power-conversion or heat-transfer properties, measured together or in different locations. For module data taken under identical test conditions (the same time and location), individual components of the f_{simple} correction can be applied during module temperature comparisons. This can elucidate correlations between the model variables of irradiance, wind speed, or other measured properties (for instance, diffuse-to-direct ratio of irradiance) and the temperature benefit from reflectance, enabling finer insights. The model is intended to be used in conjunction with best practices for device installation, data acquisition, and data filtering that preserve steady-state energy balance, and also with a previously developed wind-dependent fitted function that describes heat transfer.

From the complete thermal balance and subsequent analysis, we showed that the temperature dependence of efficiency can safely be ignored, as it does not lead to appreciable differences in operating temperature. That is, for modules with the same absorber and for which the absorber’s temperature dependencies are well understood, as is the case for c-Si, the STC efficiency of the modules can be used in our thermal model without regard for the modules’ temperature coefficients. Thus, this thermal model is particularly useful when comparing modules with the same absorber material but with cell or module optical modifications aimed at increasing sub-bandgap reflectance.

CHAPTER 3

SYSTEMATIC OPERATING TEMPERATURE DIFFERENCES BETWEEN AL-BSF, PERC, AND PERT-WITH-OPTIMIZED-REAR-REFLECTOR SOLAR MINI-MODULES DUE REAR REFLECTANCE

3.1 Introduction

Photovoltaic (PV) cells are typically characterized at standard test conditions (STC) of 25 °C and AM1.5G irradiance. When installed in the field, however, cells are encapsulated in module materials and operate at meteorological and irradiance conditions different than STC [111, 112]. This leads to operating temperatures higher than 25 °C, and even exceeding 70 °C in some cases [113, 114]. The waste heat generated in the module has a large impact on the energy yield of an outdoor system. The power output of the module decreases as its operating temperature increases; this loss is commonly described by a temperature coefficient [80]. For commercial silicon PV technology, the temperature coefficient of efficiency ranges from approximately -0.38 %/°C for high-quality monocrystalline passivated emitter rear totally diffused (PERT) to -0.4 %/°C for passivated emitter and rear contact (PERC) modules to -0.43 %/°C for traditional aluminum back-surface field modules (Al-BSF) [115]. Higher module temperature not only reduces instantaneous operating efficiency, it also accelerates nearly every type of module degradation [82]. Thus, reducing operating temperature in the field results in higher power conversion efficiency and longer system lifetime, manifesting as lower levelized cost of electricity and greater value for the end user [83]. As a result, a broad range of thermal mitigation strategies have been investigated [116].

The waste heat in the module originates from two sources: losses in the process of converting radiative energy to electrical energy (thermalization, non-radiative recombination, transport, Carnot, etc.) and parasitic absorption of light in the module that does not lead to electrical energy generation [117]. The former are fundamental limitations in the PV energy conversion process and minimizing their degree through efficiency enhancement has long been the focus of PV research; the single-junction silicon efficiency record is currently 26.7%, just short of the approximate 29% intrinsic limit [118]. A particularly insidious form of the latter heating mechanism is the parasitic absorption of light that does not contain sufficient energy to create electron-hole pairs in the absorber, known as sub-bandgap radiation. In the case of silicon, with a bandgap of 1.12 eV, approximately 19% of incident solar radiation is sub-bandgap [119]. Thermal modifications focusing on sub-bandgap radiation present a particularly attractive opportunity to reduce PV module operating temperature since the source of heat is both large and fundamentally avoidable in the energy conversion process. Indeed, multiple studies have found increasing sub-bandgap reflection to be among the most worthwhile thermal management approaches [100, 101, 120].

The ideal implementation of this thermal management strategy would result in 100% reflectance of sub-bandgap light. Silverman *et al.* modeled this idealized structure and calculated a 3.8 °C difference in annual irradiance-weighted temperature between a standard Al-BSF module and one with such an ideal sub-bandgap reflector [100]. For a module with a temperature coefficient of -0.4 %/°C, a 3.8 °C temperature decrease results in a 1.52% absolute gain in efficiency. In Silverman's work, the ideal sub-bandgap reflector operated on the front-side of the module. Slauch *et al.* further developed this approach to show how reflector designs at the front air/glass interface can impact thermal and energy benefits in real-world conditions [102]. In simulations, a 13-layer sub-bandgap mirror and 20-layer mirror on the outer air/glass interface increased reflectance at the peak sub-bandgap wavelength by 52% and 73%, and reduced parasitic absorption in the silicon module by 41 and 51 $W \cdot m^{-2}$, respectively. Each of these mirror designs increased calculated annual energy yield by at least 3.6% compared to a baseline module through a combination of higher transmittance of super-bandgap light (optical benefit) and higher reflectance of sub-bandgap light (thermal benefit) [121]. These energy benefit calculations are before accounting for accelerated module degradation associated with higher operating temperature of modules without optimized sub-bandgap reflectors.

Double-layer stacks provide an easier and less expensive route to implementation; simulated double-layer stacks of MgF_2/Al_2O_3 produced approximately 0.8% annual energy yield increase relative to standard module glass anti-reflection coatings [103]. While front-side reflectors can minimize parasitic absorption in the front module materials, a drawback of front-side reflectors is the additional constraint of effective transmission of light above the bandgap and a requirement for durable materials that can maintain their properties while exposed to the ambient for decades. More recent calculations by Slauch *et al.* found that an optimized reflector at the interface between the front encapsulant and the cell reduces annual power-weighted average operating temperature under realistic power-generating conditions by up to 2.2 °C for Al-BSF modules and 1.8 °C for PERC modules, respectively [122].

An alternative location for a sub-bandgap reflector is the rear side of the solar cell. Inserting dielectric/metal stacks on the rear side of a silicon wafer can drastically increase reflectance. For instance, SiN_x/Si/MgF_2/Ag test structures exhibited sub-bandgap reflectance over 90% and average per-bounce internal reflectance greater than 99.5% [123]. With these structures, Holman *et al.* showed that parasitic absorption in the metal is primarily caused by the evanescent field of high-incidence-angle p-polarized light reaching the metal surface, thereby exciting surface plasmon polaritons [124]. The thickness and the refractive index of the dielectric interlayer strongly affect the penetration depth of the electric field, and they can thereby be tuned to maximize reflectance. Further studies investigating the influence of surface texturing, dielectric refractive index, and metal composition have yielded some general design rules to optimize rear reflectance: the dielectric thickness should be at least 200 nm and its refractive index should be as low as possible [125]. While engineering the sub-bandgap reflector to be on the rear side leaves the cell prone to parasitic absorption by the layers at the front of the module and cell, it nonetheless has significant potential for module temperature reduction because of the outsized role that the rear metal plays. Slauch *et al.* found that increasing internal reflection at the rear surface of an Al-BSF cell from 67% to 100% can provide up to 1.2 °C annual average temperature decrease and up to 2.8 °C cooling under one-sun conditions [122].

Metal electrodes directly on the rear of silicon wafers—particularly those formed from pastes—can absorb the majority of longer-wavelength light that does not get absorbed in the wafer, as exhibited in Al-BSF cells. High-temperature firing of the printed Al paste forms Al+Si interface regions between the silicon wafer and pure Al electrode due to interdiffusion and alloying of Al and Si [126]. Optical modeling of silicon modules by Subedi *et al.* showed over a 20% difference absolute in reflectance at 1200 nm between Si/Al structures with and without the Al+Si interfacial region [126]. The same highly absorptive Al+Si region also exists in PERC devices, though minimizing its volume is the core design principle behind PERC. In addition to total contacted area, the three-dimensional geometry of the cell's contact region affects sub-bandgap optics, as the Al+Si region diffuses vertically from the contact opening into the Si wafer and also laterally into the absorber regions adjacent to the contact openings. Detailed models have recently been developed to simulate reflectance for Al-BSF cells and PERC cells with contact geometries consisting of lines or dashes. These results showed reflectances, R, at 1200 nm of 15.9, 23.1, and 28.1%, respectively, highlighting the optical benefit of the rear dielectric passivation stack of PERC [127].

As emphasized previously, this optical benefit can translate to a thermal benefit. Under computer-simulated AM1.5G irradiation, Vogt *et al.* showed that modeled PERC structures operated 1.7 °C cooler than Al-BSF, 0.8 ºC of which was due to higher efficiency (1.9% absolute in this study), and 0.9 °C of which was attributable to lower parasitic absorption in the rear metal electrode [128]. The reflected portion of the AM1.5G spectrum was 126.3 and 143.2 $W \cdot m^{-2}$ for Al-BSF and PERC, respectively. Though there is evidence to suggest the superior sub-bandgap reflectance of PERC would yield a temperature benefit in real outdoor operating conditions, this has not yet been demonstrated, to the authors' knowledge. Tests on fielded modules are an important step to validate thermal benefits of new materials and predict consequential energy production benefits, as spectral and angle-of-incidence variation affect module optics [113, 121]. Furthermore, while the dielectric passivation in the PERC cell has an appreciable impact on reflectance, and consequently on temperature, the reflectance is still far from the possible reflectance of 90% demonstrated by Holman *et al.* [123]. Thus, there is a large opportunity to lower module operating temperature by implementing ideal rear dielectric layers into industrially manufactured silicon PV cells.

In this study, we test this thermal management approach by including an optimized sub-bandgap reflector in PERT solar cells. These cells are fabricated into mini-modules that are deployed outdoors for testing. The dielectric layer introduced is a porous SiO_2 nanoparticle coating with optimized thickness and low refractive index, which yields a higher sub-bandgap reflectance than even PERC cells [110]. Also included in the outdoor tests are mini-modules with commercial Al-BSF and PERC cells. The three modules were exposed over 75 days to a wide range of irradiance and ambient conditions, representative of real, energy-generating environments. The module performance and meteorological conditions were measured throughout the test period and used as inputs in a previously developed thermal model to calculate systematic differences in thermal behavior attributable exclusively to differences in module reflectance [129].

3.2 Methods

3.2.1 Module fabrication, characterization, and outdoor installation

PERC, and modified n-PERT solar cells. Schematics of each of these cells are shown in Figure 3-1. The Al-BSF cells were obtained from a commercial vendor; the PERC and PERT (BiSoN) cells were from ISC Konstanz. No modifications were performed on the Al-BSF and PERC cells before incorporating them into modules. The as-received bifacial PERT cells, however, were augmented with a dielectric/Ag reflector stack on the rear side, thereby converting the cells to monofacial and allowing a straightforward comparison to the (also monofacial) Al-BSF and PERC. Here, silicon dioxide (SiO_2) nanoparticle (NP) films with a porosity of approximately 55%—corresponding to a refractive index of 1.2—an average pore size below 10 nm, and a thickness of at least 300 nm were deposited on the rear-side of the PERT cells via aerosol impact-driven assembly (AIDA) [130]. Silicon- and oxygen-containing precursors were used to synthesize stoichiometric SiO_2 NPs with average particle size of approximately 5 nm, which were accelerated from the synthesis chamber to the substrate by a controlled pressure gradient. This method has previously

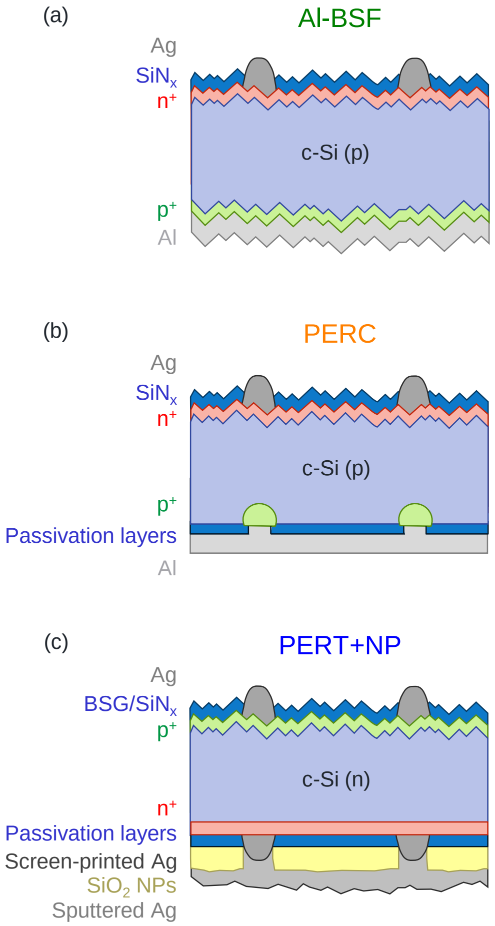


Figure 3-1. Schematics of (a) Al-BSF, (b) PERC, and (c) PERT+NP cells used in the mini-modules in this study.

been used to deposit low-refractive-index porous Si NPs as a rear reflector layer for silicon heterojunction cells [131]. The SiO_2 NP synthesis process used here enables lower-refractive-index films than our previously studied Si NPs. Further descriptions of the deposition and film characterization processes can be found in prior work [110].

During the deposition of the SiO_2 NPs on the rear of the PERT cells, the silver busbars were covered with a shadow mask to maintain the electrical contact already established by the rear-side screen-printed Ag grid. Sputtered Ag layers were then deposited on the full area of the rear-side, per Figure 3-1(c), using an MRC 944 tool with a DC source power of 1 kW. Hereafter, we call these cells "PERT+NP." This processing sequence is not industrially compatible, but was the most expedient and practical approach for the demonstration sought here, as prior tests integrating the porous SiO_2 NP film directly into an established PERC fabrication sequence yielded no optical benefit due to the fire-through paste reacting with the NP film [110].

Another set of PERT cells were converted to monofacial but did not include the SiO_2 NP film. Instead, Al was sputtered on the full area of these as-received cells to serve as optical references. These cells, referred to as "PERT no NP reference", were not converted into modules. External quantum efficiency (EQE) and reflectance spectra of each set of cells was measured from 300 to 2500 nm using a PV Measurements QEX10 tool and a PerkinElmer Lambda 950 spectrophotometer. These measurements were used to find active-area, AM1.5G-weighted R for each cell. After cell characterization, the Al-BSF, PERC, and PERT+NP cell batches were packaged into modules.

Each module contained nine M2-sized cells. The cells were electrically connected in series and arranged in a closely spaced 3 × 3 grid. The cells were packaged with conventional PV module materials: textured low-iron cover glass (no anti-reflection coating), ethyl vinyl acetate (EVA) encapsulant, and a polyvinyl fluoride (PVF)/polyethylene terephthalate (PET)/PVF backsheet. Each module used a pair of small, single-pole junction boxes, placed entirely in the margin area away from the cells. Electroluminescence imaging after module packaging was performed to ensure that interconnection and lamination had been completed without major damage to the cells. The Al-BSF, PERC, and PERT+NP modules had STC aperture efficiency values of 17.7%, 18.3%, and 18.5%, respectively. Module reflectance and EQE were measured using a Lambda 1050 and NREL's filter EQE system described in prior work [132].

We deployed the modules at NREL's outdoor test facility in Golden, Colorado for 75 days. They were oriented to the south at 40° tilt above horizontal. Current–voltage (I–V) curves were collected every five minutes and the modules were held at their maximum power points between measurements. In addition to I–V data, simultaneous measurements of ambient temperature ($T_{ambient}$), wind speed (v_w), and plane-of-array irradiance (E_{POA}) were also collected.

Module temperature (T_{module}) was derived from the I–V bilinear interpolation method [133]. Indoor pulse I–V sweeps of each module were performed at each combination of device temperature (15, 20, 25, 30, 35, 40, 45, 50, 55, 60 °C) and irradiance (200, 400, 600, 800, 1000 $W\cdot m^{-2}$). Sixteen thermistors were placed on the back of each module for temperature measurement. Module temperature was uniform to within ±2.25 °C. Once thermal uniformity was established, the I–V curve was recorded and associated with a single-point temperature measurement in the center of the module, made with a resistance temperature detector (RTD). The open-circuit voltage (V_{oc}) and I_{sc} from the outdoor I–V sweeps were plugged into an interpolation grid containing 50 grid points from the temperature controlled, indoor I–V sweeps, to extract T_{module}. This method has been shown to have good accuracy for measuring module temperature [134]. Systematic errors are assumed to affect each of the module types in the same way and are thus neglected for the purposes of comparing relative operating temperatures outdoors.

3.2.2 Outdoor data analysis

To assess differences in temperature caused by the differences in sub-bandgap reflectance between each module, a correction factor is applied to the measured data. This correction procedure eliminates temperature variation arising from the other major contributors of temperature variation: irradiance, wind, and module efficiency. The correction factor, *f*, is defined as,

$$\begin{aligned} f &= f_{irradiance} \times f_{wind} \times f_{efficiency} \\ &= \frac{E_{POA}^{(ref)}}{E_{POA}^{(meas)}} \times \frac{c(v_w^{(ref)})}{c(v_w^{(meas)})} \times \frac{1-\eta_{STC}^{(ref)}}{1-\eta_{STC}^{(meas)}} \end{aligned} \tag{1}$$

where E_{POA} is plane-of-array irradiance, $c(v_w)$ is the wind-dependent heat-transfer factor, and η_{STC} is STC efficiency. The lumped heat-transfer factor used here is an empirically-derived function of wind speed, the dominant heat transfer mechanism in fielded modules [97]. Its derivation method is detailed in prior work [98]. The full derivation of the correction term *f* is also described in detail in prior work [129]. Measured values are represented with superscript *(meas)* and reference values with superscript *(ref)*. The reference ambient conditions and reference module properties used in this experiment are shown in Table 3-1. These values were chosen to minimize the average magnitude of the correction and to be representative of the most relevant energy generating conditions.

The raw temperature rise above ambient, ΔT^{raw}, is:

$$\Delta T^{raw} = T_{module}^{(meas)} - T_{ambient}^{(meas)} \tag{2}$$

The correction factor based on the reference values is applied to the measured values for each module to calculate the corrected temperature rise above ambient, ΔT, as follows:

$$\Delta T = \Delta T^{raw} \times f \tag{3}$$

The corrected temperature rise, ΔT, represents what the module temperature rise above ambient *would have been* if the module under test had the reference properties and had been measured under the reference conditions [129]. As the correction factor eliminates temperature differences from other major factors, differences in ΔT between modules is caused exclusively from differences in reflectance. That is, two modules with the same reflectance will have the same ΔT, even if they have different efficiencies or were measured with different irradiances and wind speeds. The ΔT values of each module throughout the 75-day test period are used to facilitate comparisons between the modules, which have different reflectances.

In order to minimize deviation from the steady-state energy balance between the module under test and the ambient—the basis of the thermal model—data were removed at instances with appreciable snow, large changes in irradiance, or large changes in wind speed. For irradiance, the data were removed if the difference between the maximum and minimum measured values was greater than 3 $\text{W}\cdot\text{m}^{-2}$ for the 30 seconds before and after

Table 3-1. Correction factor variables and reference values.

Symbol	Quantity	Reference value
E_{POA}	plane-of-array irradiance	1000 W·m^{-2}
v_w	wind speed	1.43 m·s^{-1}
$c(v_w)$	lumped heat transfer factor	0.0256
η_{STC}	STC efficiency	17.7%

the measurement. For wind speed, the data were filtered if the difference between the maximum and minimum measured values was greater than 5 m·s^{-1} for the 12 minutes before the measurement. The presence of snow was detected by comparing the predicted I_{sc} of the module to the measured I_{sc}. The predicted I_{sc} is defined as the median I_{sc} between 950–1050 W·m^{-2} multiplied by the quantity (measured I_{sc} / 1000 W·m^{-2}). The data were removed if the ratio of the measured I_{sc} to the predicted I_{sc} was not between 0.85 and 1.15.

3.3 Results and Discussion

3.3.1 Sample characterization

The reflectance of the cells before module packaging is shown in Figure 3-2(a). As the front Ag fingers of the completed cells fell within the aperture of the reflectance measurements, the reflectance data were corrected to represent active-area reflectance by dividing by the unmetallized areal fraction. The reflectance at 1200 nm approaches 55% for the PERT+NP cells—the best ever demonstrated for a PERT or PERC cell, to the authors’ knowledge. The PERT+NP had higher reflectance than the PERT reference with full-area Al metallization, revealing the effectiveness of the SiO_2 NP film/Ag rear reflector stack. Additionally, the PERT+NP reflectance was higher than the Al-BSF and PERC cells. The reason the PERT+NP cells do not reach the over 90% reflectance seen in prior work is infrared parasitic absorption occurring in heavily doped regions besides the rear reflector.

EQE and $1-R$ for the fully fabricated modules is shown in Figure 3-2(b), with AM1.5G-weighted R values shown in parentheses. The module materials impart parasitic absorption and reduce the reflectance benefit of the rear reflector. R at 1200 nm for the PERT+NP cell was 54.5% and dropped by 17.3% absolute to 37.2% after module packaging. For PERC and Al-BSF, this drop after module packaging was 12.1% and 2.1%, respectively. The reduction in R is attributable to parasitic absorption by the glass and to larger degree by the EVA, which has several characteristic absorption peaks visible in Figure 3-2(b). Similarly, Vogt *et al.* calculated 38.0 $\mathrm{W{\cdot}m^{-2}}$ and 43.7 $\mathrm{W{\cdot}m^{-2}}$ of parasitic absorption in the glass and EVA layers for Al-BSF and PERC modules, respectively, in the 1210–2500 nm spectral range [128]. Haedrich *et al.* calculated annual energy loss of a PERC module to be 4.4% due to module embedding, primarily from front cover glass reflectance and also parasitic absorption in the module glass and EVA [113]. Higher reflectance also contributes to improved EQE in the 1000–1200 nm wavelength range because this light gets a longer path length through the silicon.

The impact of parasitic absorption by the module materials in the super- and sub-bandgap ranges for the devices tested here can be seen in Figure 3-2(c). Super-bandgap (250-1100 nm) reflectance is undesirable. While it does reduce module operating temperature, it also reduces I_{sc} and should thus be avoided. The most desirable outcome is to minimize the purple bars and maximize the red bars (though the red bars won’t exceed 19%). The AM1.5G-weighted reflectance for the PERT+NP module was 11.2%, 6.3% of which was in the 250–1100 nm range. This reveals that, of the approximately 19% sub-bandgap light, the PERT+NP module rejected just 4.9%, even though optimized test structures demonstrated a path to 90% reflectance at 1200 nm. The difference in sub-bandgap AM1.5G-weighted *R* (red bars) between cell and module for Al-BSF, PERC, and PERT+NP is 0.93, 2.59, and 3.14% absolute, respectively. This shows that the superior

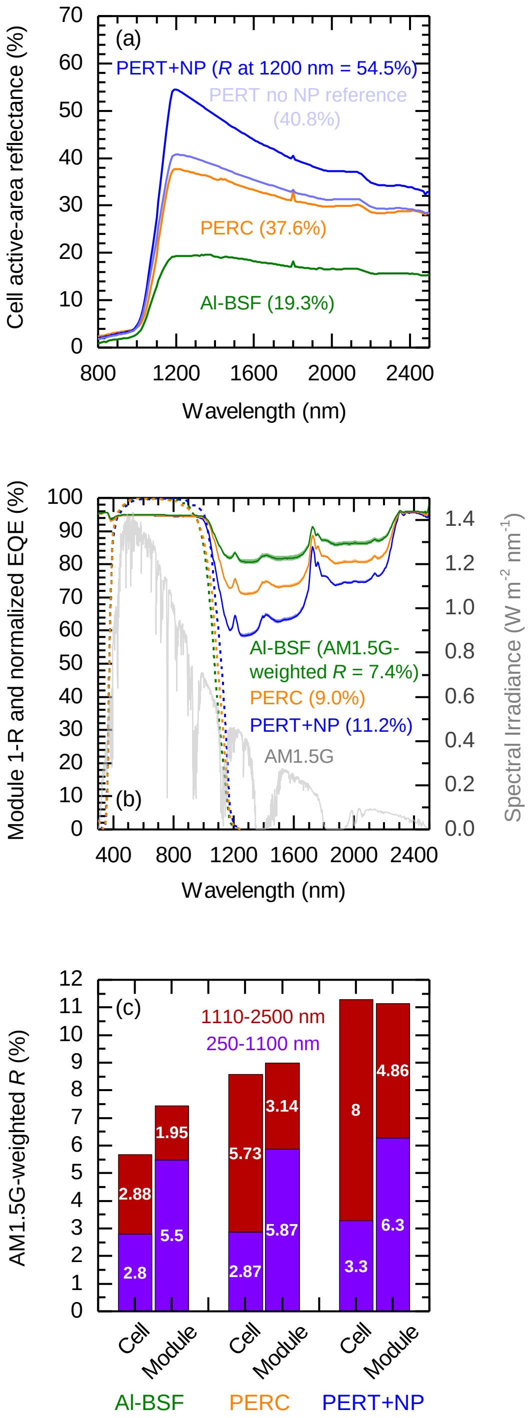


Figure 3-2. Plot of (a) active-area *R* for each cell, (b) 1-*R* and normalized EQE for the fully fabricated modules, and (c) AM1.5G-weighted *R* for each cell and module. The full height is the reflection from 250-2500 nm, with sub bands as indicated.

sub-bandgap reflectance of the PERT+NP cell does not entirely carry over after module packaging, revealing that improvements in sub-bandgap reflectance at the rear side must be in coordination with the optical properties of the fully fabricated module to capture the full thermal benefit.

3.3.2 Outdoor data

Figure 3-3(a) shows ΔT^{raw} with corresponding irradiance and wind speed data from one day in the test range where nearly all data met the steady-state energy balance requirements.

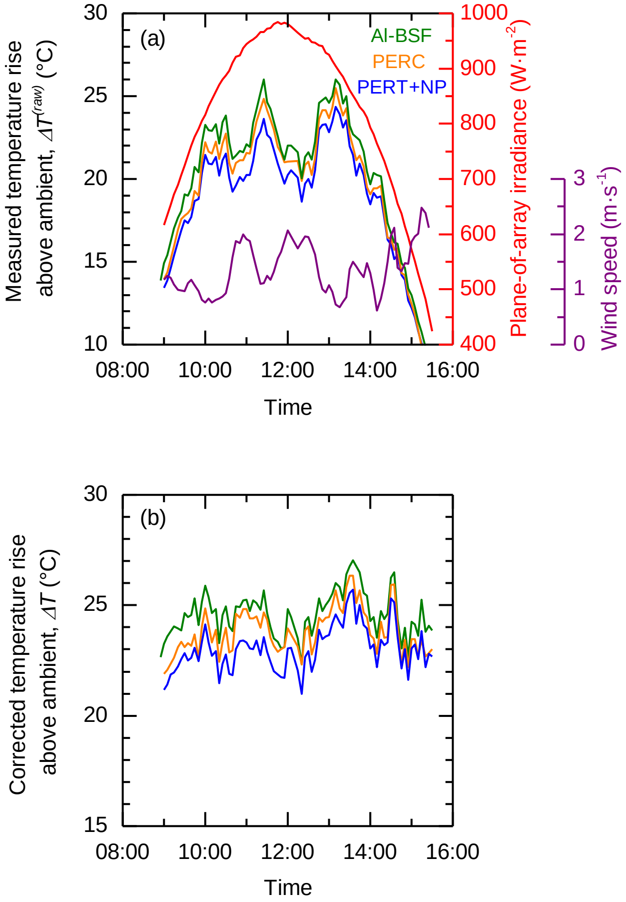


Figure 3-3. (a) Measured module temperature rise above ambient and irradiance for one day in the test period (Dec. 9th), and (b) corrected module temperature rise above ambient from the same day.

Since each set of module data is from the same moment, the differences between ΔT^{raw} values are not due to meteorological factors, but rather only from the differences in module performance (efficiency and reflectance). Systematic temperature differences on this day are revealed by the raw data: PERT+NP runs cooler than PERC, which in turn runs cooler than Al-BSF. As expected, in a given day with large irradiance changes, relatively large changes in module operating temperature are also observed. Note that the module temperature does not follow the irradiance precisely because of the variable wind speed: The approximately 1 $m \cdot s^{-1}$ increases in wind speed at 10:30 and 12:00 reduce temperature by several degrees. Figure 3-3(b) shows the corresponding ΔT for this same day, which collapses the data around a tighter distribution of temperature values. As a reminder, ΔT are the module temperature rise above ambient that the modules would have experienced if they all shared the performance characteristics and measurement conditions in Table I. The corrected data similarly shows a systematic difference in ΔT between modules, which in this corrected case, is due just to reflectance as the correction accounts for differences in efficiency.

Figure 3-4 plots ΔT for each module, in the 600–1000 $W \cdot m^{-2}$ irradiance range, as a cumulative distribution function (CDF). The median ΔT value occurs when the CDF equals 0.5; each module operates warmer than its median value for half of the time and cooler than this value for the other half of the time. For the Al-BSF, PERC, and PERT+NP modules, the median ΔT value was 24.2, 23.2, and 22.8 °C, respectively. The difference between these median values is a good metric into which all of the data can be consolidated to yield a single temperature benefit value attributable to reflectance. At the chosen reference conditions (1000 $W \cdot m^{-2}$, 1.43 $m \cdot s^{-1}$, and 25 °C), the PERC module operates

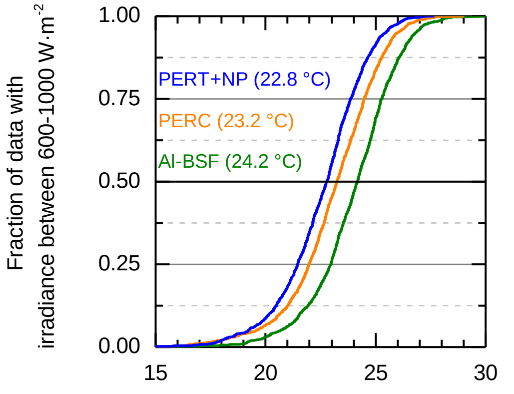


Figure 3-4. Corrected temperature rise above ambient for each tested module displayed as a cumulative distribution function. The median values for each tested module are shown in parentheses.

1.0 °C cooler than Al-BSF, and the PERT+NP module operates 1.4 °C cooler than Al-BSF and 0.4 °C cooler than PERC. For a module with a temperature coefficient of -0.4 %/°C, 1.4 and 0.4 °C temperature decreases result in 0.56 and 0.16% absolute gain in efficiency, respectively. The statistical significance of these median differences are validated with Mann-Whitney U tests: the medians are statistically different at over a 0.01 level (Z-scores of 7.9, 12.7, and 20.2, respectively). Thus, there is a clear and systematic difference in operating temperature attributable to the sub-bandgap reflectance of each module. The 1.0 °C temperature benefit of PERC relative to BSF from reflectance measured here is consistent with the 0.9 °C calculated by Vogt *et al.* for the same 1000 W·m^{-2} irradiance [128].

In evaluating the relative thermal performance of one cell design against others, it is instructive to compare the temperatures of pairs of modules. Figure 3-5 shows differences between module temperatures taken at the same time and corrected just for efficiency, making the temperature differences due solely to reflectance. The data are binned

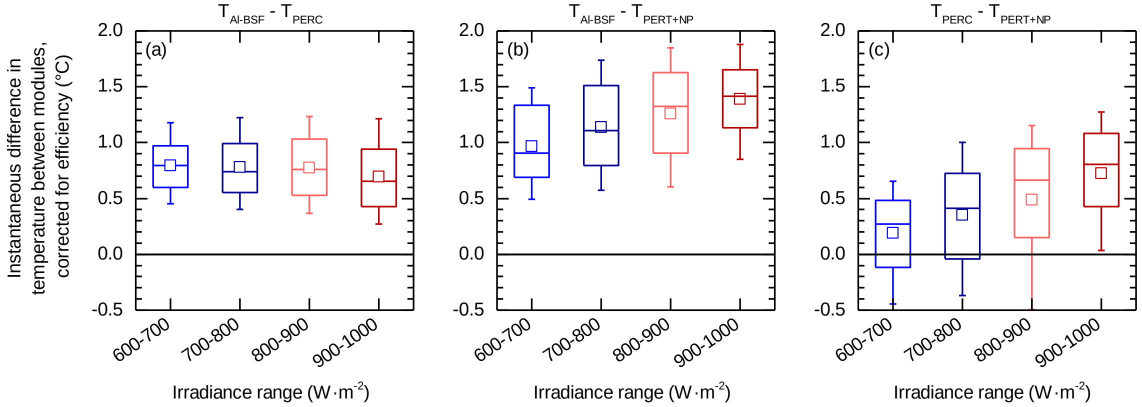


Figure 3-5. Temperature difference between (a) Al-BSF and PERC, (b) Al-BSF and PERT+NP, (c) PERC and PERT+NP modules displayed as boxes and whiskers and binned by irradiance. Boxes represents 25–75 percentiles, whiskers represent 10–90 percentiles, and inset boxes and lines represent mean and median values, respectively.

according to irradiance and the total plotted range of 600–1000 W·m^{-2} accounts for approximately 86% of the power production for the Al-BSF module in this study. The mean temperature benefit of the PERT+NP module over the Al-BSF and PERC modules increases at higher irradiance, revealing that this thermal management approach has the largest impact at the most important conditions: high irradiance and, consequently, high power generation. The Al-BSF and PERC comparison, surprisingly, does not show this same irradiance dependence. We hypothesize that this may be due to noise from the indoor interpolation method related to spectral mismatch between the Xenon flash lamp and typical outdoor irradiance.

3.4 Conclusions

Fielded modules can benefit from the thermal management strategy of rejecting unusable sub-bandgap light, thereby improving lifetime energy production. Here, we found that adding an optimized rear-reflector stack provides a temperature benefit of 1.4 and

0.4 °C over fielded Al-BSF and PERC modules, respectively. Importantly, we found that the rear SiO_2 NP/Ag reflector is most effective during periods of highest irradiance, when power generation is highest. In order to capture the full temperature benefit of approximately 2.8 °C associated with this approach, parasitically absorbing materials such as module glass and EVA should be replaced with low-infrared-absorbing alternatives, and heavily-doped regions in the cell should be strategically localized.

The technique used here to implement the reflector technology—converting a bifacial cell to monofacial—is not suitable for industrial application. In a previous study, we found the porous SiO_2 film to be chemically incompatible with the etching mechanism of fire-through Al pastes. However, this limitation is not insurmountable. Just as traditional Al-BSF paste chemistries were modified to prevent damage to the SiN_x passivation layers in PERC cells, additional paste optimization could enable an optimized optical film that complements the dielectric passivation stack [35]. Similarly, making pastes less damaging is an active area of research for polysilicon contacts [72]. Integrating low-refractive-index dielectric layers with more gentle paste chemistries could be a worthwhile cell development effort, especially in cases where bifaciality is irrelevant and thermal management via sub-bandgap reflectance is particularly important. Such cases include residential and commercial rooftop systems, where conductive/convective cooling of modules is reduced or completely suppressed and higher module temperatures create higher building cooling loads in summer [101]. Further, such dedicated optical films can be integrated into solar cells with full-area passivating contacts, such as polysilicon or silicon heterojunction. Augmenting the superior electrical performance of passivating contacts with the additional optical-thermal benefit from an optimized sub-bandgap reflector could further enhance their applicability in the PV module market.

CHAPTER 4

SILVER METALLIZATION TO c-Si(n)/SiO_2/poly-Si(n) CONTACTS WITH SPUTTERING AND NANOPARTICLE INK: INFLUENCE OF DIFFUSION AND GRAIN GROWTH ON CONTACT PROPERTIES AT LOW TEMPERATURES

4.1 Introduction

Silicon solar cells with SiO_2/poly-Si (TOPCon) passivating contacts have demonstrated excellent open-circuit voltage (V_{oc}), enabling efficiencies of 25.8 and 26.1% for double-side and single-side contacted architectures, respectively [25, 30]. As a result, they are receiving substantial industrial interest as an evolutionary upgrade to traditional silicon cell technologies that use direct metal contact to highly-doped regions of the silicon wafer [34]. Realizing the cell technology requires minimal process adjustments from the mainstream fabrication sequences of Al-BSF, PERC, and n-PERT, which solidifies its positioning as the top evolutionary-upgrade candidate [135]. In order to motivate transition to TOPCon structures, it is necessary to maintain compatibility with the mainstream fabrication processes, which for metallization, requires screen-printing.

Modifying traditional fire-through paste chemistries designed for contacting doped-emitter regions has enabled significant improvement in the contact performance to TOPCon. Padhamnath *et al.* metallized c-Si/SiO_2/100-nm-thick-poly-Si(n+) with fire-through pastes and reported contact recombination parameter ($J_{0,met}$) below 50 fA/cm^2 with average contact resistivity (ρ_c) of 2 mΩ.cm^2 [72]. When the poly-Si thickness was reduced from 100 nm to 50 nm, $J_{0,met}$ increased to 355 fA/cm^2. This highlights a significant challenge with fire-through paste: fine-tuning the etching mechanism with sufficient control to make benign contact to thin poly-Si while not damaging the chemical passivation provided by the underlying oxide. In reported works so far, the minimum poly-Si thickness that can maintain high V_{oc} after fire-through is approximately 100 nm [136-138]. From an industrial view, reducing poly-Si thickness provides valuable increase in tool throughput and lifetime [135]. What's more, the thicker the front poly-Si, the larger the optical losses; every 10 nm of poly-Si thickness contributes approximately 0.5 mA/cm^2 in short-circuit (J_{sc}) current losses from parasitic absorption [74, 75].

This tradeoff severely limits the attractiveness of front-side TOPCon implementation [139]. Consequently, metallization systems and process sequences that can enable thin poly-Si while simultaneously maintaining passivation are under investigation through many approaches. Young *et al.* used reactive ion etching after paste firing to reduce the front-side poly-Si thickness from 200 nm down to about 130 nm [140]. Plated Ni/Cu/Ag and Ni/Cu contacts have been reported [141, 142]. Numerous transparent conductive oxides (TCO) deposited on top of poly-Si have been studied including ITO, ITO:H, AZO, and IFO:H [143-147]. These structures capitalize on the low-temperature paste developed for silicon heterojunction (SHJ) technology. Low-temperature Ag paste systems establish contact through a particle sintering mechanism, where adjacent Ag particles densify and diffuse to make physical contact to the underlying TCO [148]. While the metallization step doesn't induce V_{oc} loss, the sputtering of TCOs on thin poly-Si typically does and also requires the addition of a costly physical vapor deposition (PVD) system. Further, constituents in TCOs can migrate and react at interfaces, causing increased contact resistance [144].

These drawbacks motivate the investigation of the low-temperature contact mechanism to thin poly-Si without TCOs. Such structures are screen-printing compatible, not known to damage passivation, and their practical realization only requires laser contact opening through a SiN_x anti-reflection layer, a process with proven industrial scalability by passivated emitter and rear contact (PERC) [149]. While the cell structure has high sheet resistance (R_{sheet}) in the thin poly-Si layer, appreciable transport losses are not necessary if other conditions are met: sufficient absorber conductivity, minimal contact resistivity between the absorber and poly-Si, and minimal contact resistivity of the Ag to the poly-Si [150]. Tuning the absorber conductivity and achieving low contact resistance for Si/SiO_2/poly-Si are readily achievable, making the poly-Si/Ag interface formed by a low-temperature sintering mechanism the largest unknown. Regarding passivation, the low-temperature Ag contact process is theorized to not damage passivation when thin poly-Si is used, but has not been demonstrated. Regarding interface conductivity, well-formed poly-Si(n)/Ag interfaces formed by PVD have demonstrated low ρ_c of 3.3 $m\Omega.cm^2$, indicating the approximate upper limit of an optimal low-temperature process to deliver Ag to the poly-Si surface [53]. Assuming linear scaling, reduced contacted areas of 50% and 15% result in ρ_c of 6.6 $m\Omega.cm^2$ and 22 $m\Omega.cm^2$, respectively, indicating potential compatibility with a range of organic components such as binder resins to assist with adhesion.

Initial work on the low-temperature Ag contact mechanism to TOPCon structures using SHJ paste revealed a fundamental incompatibility between the organic components of SHJ paste and TOPCon structures: the organic solvent strongly wets poly-Si(n) and delivers the binder resins to the poly-Si(n) surface in the wetting process, which impede contact of the Ag particles [151]. These studies showed that behavior of the poly-Si(n)/Ag interface formed with SHJ paste is largely inaccessible with existing paste chemistries. To circumvent these issues, we perform metallization tests using colloidal Ag nanoparticle (NP) ink that contains the same solvent as the paste, but no binder. This ink allows the performance of the low-temperature Ag particle sintering mechanism to poly-Si(n) to be isolated without the interference from the organic components, with the premise that these organic components are complimentary to the metal content and can be optimized later. These ink chemistries function by sequential evaporation of solvents, removal of surrounding dispersants, adhesion of particles to each other and the substrate, and sintering of the Ag NPs [152]. Similar ink sintering mechanisms are being investigated as an alternative for pastes in SHJ cells [153]. This study first focuses on characterizing the Ag ink properties as a function of temperature and identifying the dominant diffusion mechanisms at each curing temperature. Next, the Ag NP inks are used to study TOPCon contact properties with low-temperature Ag metallization. In particular, contact resistivity and metallized-induced drop in implied-voltage are quantified.

In addition to testing the Ag NP ink, we further investigate c-Si(n)/SiO_2/poly-Si(n)/Ag contacts formed with sputtered Ag. In prior studies, these structures had contact resistivity of 2.9 $m\Omega\cdot cm^2$ as-deposited, which degraded to 677 $m\Omega\cdot cm^2$ after annealing in air for 20 minutes at 200 °C, indicating a primary source of transport loss related to Ag content [151]. Similar transport degradation was observed by Hayes *et al.* with c-Si/SiO_2/poly-Si(p)/Ag metallized with sputtering; contact resistivity increased from 90 $m\Omega\cdot cm^2$ to over 250 $m\Omega\cdot cm^2$ after annealing at 400 °C in Argon ambient [154]. For the same structure metallized with Ag via electron beam evaporation, contact resistivity was over 200 $m\Omega\cdot cm^2$ as-deposited and dropped to 110 $m\Omega\cdot cm^2$ after annealing at 400 °C in Argon ambient [154]. The reasons for these behaviors are not clear. Evaporation and sputtering of Ag (and Al) are common processes to fabricate devices on the lab scale to both n- and p-type contacts, including in world-record device structures [30, 53, 155, 156]. Studying poly-Si(n)/Ag as a reference system can help diagnose the reasons behind limitations with the low-temperature contact approach via Ag particle sintering as well as provide insight into the allowable thermal processes for lab-scale investigations of TOPCon devices where the primary scope of work is outside metallization. Toward this, contact resistivity references with different wafer texturing, annealing ambient, and annealing temperature are performed. Microstructure characterization with SEM and XRD and high-resolution microscopy of the poly-Si(n)/Ag interface are performed to investigate possible mechanisms impacting contact resistance performance.

4.2 Sample Preparation

This study used four sample sets and two Ag deposition methods. Schematics of each sample set are shown in Figure 4-1 along with the characterization technique performed on each sample type. To test the low-temperature contact process, colloidal nanoparticle (NP) Ag ink was deposited with a Dimatix DMP-2381 inkjet printer. The Ag ink used in this study was Novacentrix JS-B40G, which contains an average particle diameter between 60-80 nm [157]. The printing recipe was set to 50-micron droplets with 50-micron drop spacings. The Ag was printed in 2 or 3 passes and cured between 200-300 °C for 5 minutes. A relatively short curing time was used to be able to distinguish the temperature ranges where the sintering regimes transition. The Ag for the sputtered reference samples was approximately 275 nm thick and was deposited using an MRC 944 tool with a DC source power of 1kW and a chamber pressure of 8.1 mTorr.

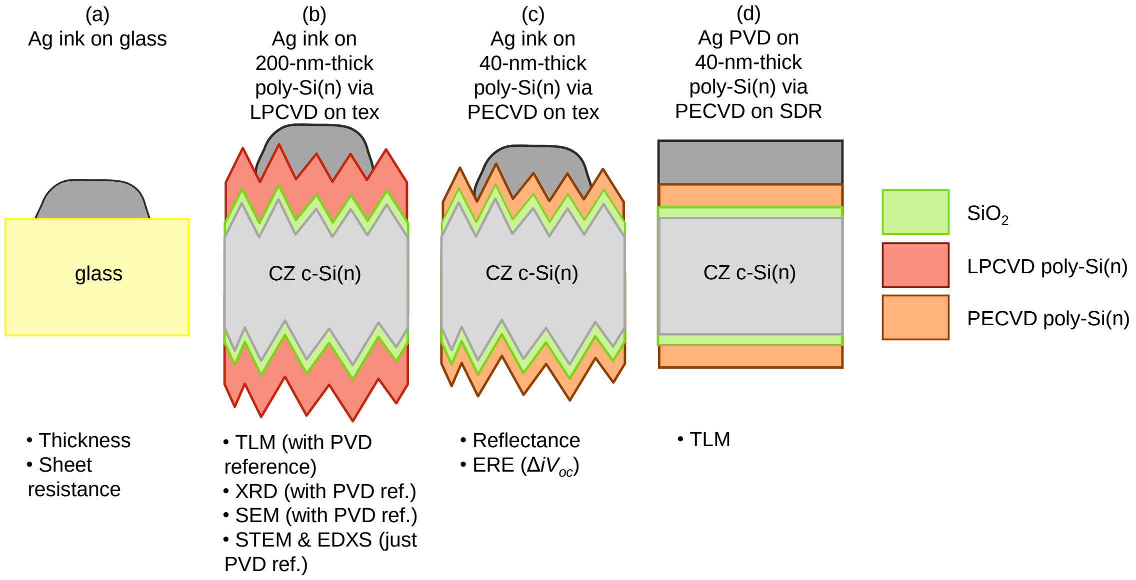


Figure 4-1. Schematics of each sample used in this work along with the corresponding characterization techniques.

Initial characterization of Ag ink properties as a function of curing temperature was performed on glass substrates from AMScope. Five thickness measurements for each Ag film (2-3 passes cured at 200-300 °C) were measured with a DektakXT stylus profilometer from Bruker to obtain an average thickness value. A custom-built four point probe was used to measure the sheet resistance of the same cured Ag ink samples.

Three sets of symmetric c-Si(n)/SiO$_2$/poly-Si(n) samples were used to study solar cell contact properties and Ag material properties. Investigations of Ag microstructure, contact resistivity, and high-resolution imaging of the poly-Si(n)/Ag interface were performed using symmetric c-Si(n)/SiO$_2$/poly-Si(n) with 200-nm-thick poly-Si(n), shown in Figure 4-1(b). These samples used KOH-textured Czochralski (Cz) solar wafers with 4 Ω·cm bulk resistivity. A 1.5-nm-thick SiO$_2$ layer followed by a 200-nm-thick poly-Si(i) were grown on these wafers in a low pressure chemical vapor deposition (LPCVD) furnace. The samples underwent a POCl diffusion to dope the intrinsic poly-Si to n-type. Symmetric SiN_x films were then deposited by PECVD. Before depositing Ag, the SiN_x was etched in buffered hydrofluoric acid (BOE). These structures were used to test contact resistivity of the Ag ink and sputtered Ag references using the transfer length method (TLM). Additional reference samples were included in the contact resistance test: sputtered ITO/Ag annealed in atmosphere and sputtered Ag annealed in a nitrogen glovebox. The ITO and Ag were sputtered sequentially without breaking vacuum, with the ITO process using a DC source power of 0.5 kW and a chamber pressure of 5.5 mTorr with an oxygen partial pressure of 0.11 mTorr (2% partial pressure). The Ag ink samples were cured at 250, 275, and 300 °C for 5 minutes, while the sputtered samples were annealed from 100 to 300 °C for 10 minutes. The microstructure of Ag ink and sputtered reference samples was characterized using a FEI Nova 200 NanoLab scanning electron microscope (SEM) and PANalytical Aeris Powder X-ray Diffractometer (XRD). To investigate surface morphology of the Ag ink on the textured wafer and the resultant microstructure following different curing temperatures, a printing recipe was used to print Ag lines with a target width of 250 microns. The poly-Si(n)/Ag interface was probed using scanning transmission electron microscopy (STEM). STEM lamellas were prepared by the conventional focused ion beam (FIB) lift-out method from the TLM structures with the final Ga ion beam polish at 2 kV. A JEOL ARM microscope was used to take medium angle annular dark field (MAADF) images of the interface at 200 kV electron beam. Energy-dispersive X-ray spectroscopy (EDXS) was used to map local concentrations of Ag, Si, O, and S.

Samples employing a thin poly-Si(n) layer of 40 nm, shown in Figure 4-1(c), were used to evaluate passivation quality and optical behavior. These samples used KOH-textured n-type Cz wafers with 4 Ω·cm bulk resistivity. A 1.5-nm-thick-low-temperature SiO_x layer was grown at 550 °C. Then, 40 nm of a-Si:H(n) was deposited using a PECVD cluster tool (MVSystems multichamber). The film was crystallized to poly-Si(n) during a high-temperature tube furnace anneal at 850 °C in nitrogen ambient. The poly-Si(n) was made thin to verify the low-temperature contact mechanism does not induce passivation damage, even for samples with thin poly-Si(n). The lifetime and implied-V_{oc} (iV_{oc}) were measured with a Sinton lifetime tester and photoluminescence (PL) images were taken of the completed samples. Three passes of Ag ink were deposited on half the area of each sample (3 by 5 cm pieces) and cured at 250, 275, 300, 450, and 600 °C. A custom-built tool that measures external radiative efficiency (ERE) was used to take spatial ERE maps of the samples pre- and post-Ag deposition as described in prior work [158]. The map had grid spacings of 2 mm in the x- and y-direction, for a total of over 300 measurements per sample. ΔiV_{oc} is calculated using the sets of pre-metallization and post-metallization ERE measurements with the following equation [159]:

$$\Delta iV_{oc} = \frac{kT}{q} \times \ln\left(\frac{ERE_{post-Met}}{ERE_{pre-Met}}\right) \qquad 4.1$$

When calculating ΔiV_{oc}, only data over 8 mm from the edge of the printed Ag was used so the minority carrier holes would not diffuse to regions outside where the Ag was printed. The reflectance spectra of each sample was measured from 900 to 1300 nm using a PerkinElmer Lambda 950 spectrophotometer.

The final sample batch, shown in Figure 4-1(d), was identical as the batch from Figure 4-1(c), but did not receive KOH texturing. Instead these wafers only had saw-damage removal (SDR) to create a more planar surface.

4.3 Results and Discussion

4.3.1 Ag ink properties

Figure 4-2(a) shows the thickness of the Ag films printed with 2 and 3 passes and cured from 200-300 °C. Every incremental increase in curing temperature resulted in further film densification. From 200 to 300 °C, the average sample thickness decreased by 27% and 33% for print recipes using 2 passes and 3 passes, respectively. Figure 4-2(b) shows the measured sheet resistance, which along with the average thickness, was used to calculate resistivity. A sharp reduction in R_{sheet} of 2-3 orders of magnitude occurred between 200

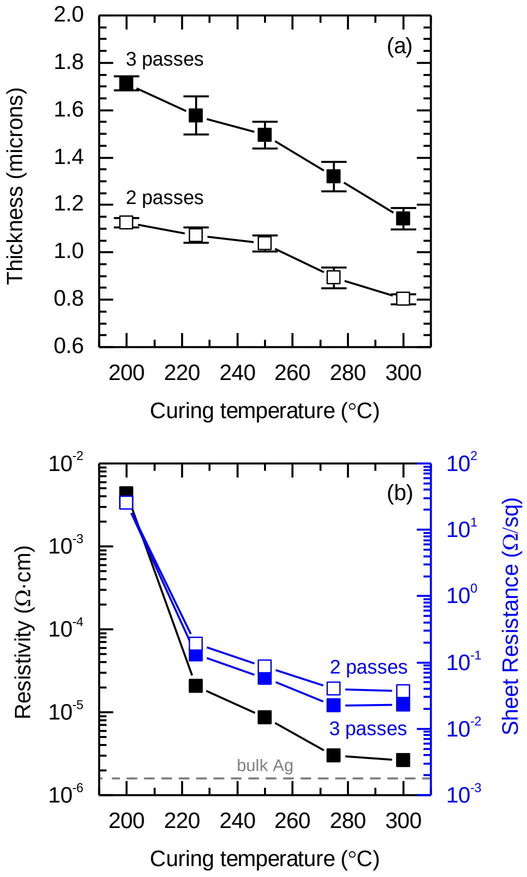


Figure. 4-2. Ag ink (a) thickness, and (b) sheet resistance and resistivity.

and 225 °C. This large drop in sheet resistance during the initial stage of the sintering process plays the largest role in reducing the film's resistivity, similarly observed by Greer *et al.* with 40 nm Ag particles, but cured at 150 °C [160]. After curing at 300 °C, the resistivity of the denser Ag films saturated at 2.9 and 2.6 μΩ·cm for 2 and 3 passes, respectively, which is 1.6-1.8 times more resistive than bulk Ag. These resistivity values are similar to other reports using this Ag ink chemistry of approximately 1.7 [161, 162]. Further, these values are actually lower than the resistivity of common low-temperature pastes (5-20 μΩ·cm) due to their 200 °C curing temperature restriction [79]. Thus, curing temperatures between 225 and 300 °C with this particular NP ink chemistry are representative of typical performance with the low-temperature Ag contact mechanism.

The microstructure and morphology of printed lines with target width of 250 microns on textured wafers was investigated with SEM, shown in Figure 4-3. After curing at 200 °C, the Ag line remains relatively thick, porous and highly-resistive, which can be attributed to negligible sintering between adjacent Ag NPs seen in Figure 4-3(a). In the initial stage of sintering, atomic movement is primarily driven by the reduction of surface energy of the Ag NPs particles. The predominant pathway for densification is through-lattice diffusion, which occurs in parallel with rapidly occurring surface diffusion [160, 163]. These diffusion processes lead to necking of adjacent particles, which drive film densification and a large increase in conductivity [162]. For the 5-minute anneals used in this study, this initial sintering process initiates between 200 and 225 °C, where the steep drop in resistivity was observed. This particle growth and necking can be seen in Figure 4-3(b) for a sample cured at 250 °C. As the sintering process continues, the surface energy release provided by the neck formations create an increasing amount of grain boundary

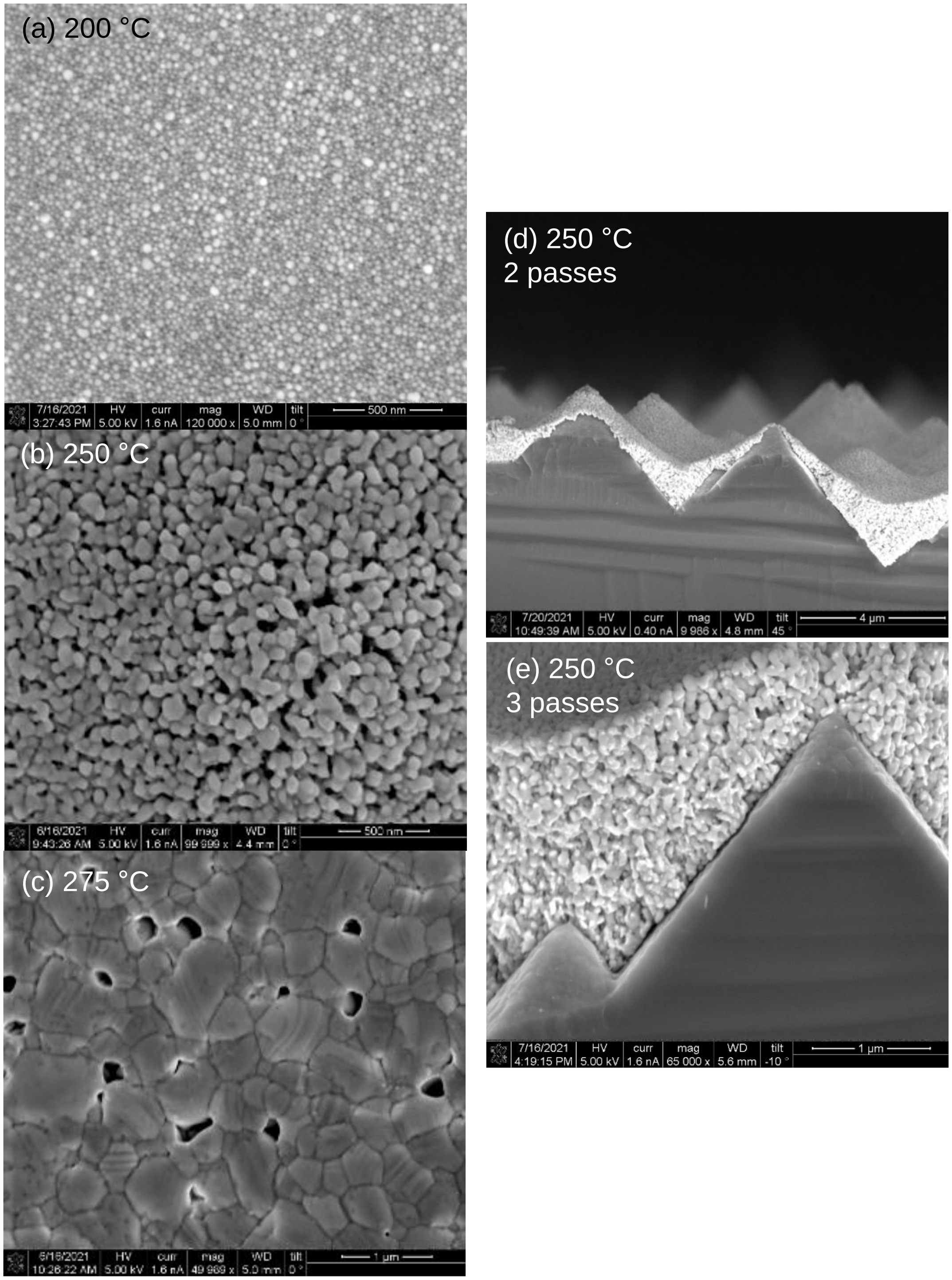


Figure 4-3. Surface SEM images of Ag ink cured for 5 minutes at (a) 200 °C, (b), 250 °C, and (c) 275 °C. Cross-section SEM images of Ag ink cured at 250 °C printed with (a) 2 passes and (b) 3 passes.

defects. This energy balance dictates the dominant diffusion pathways and eventually causes a change from through-lattice diffusion to grain boundary diffusion, corresponding to an approximate transition from “initial” to “intermediate” sintering regimes [160]. Even though grain boundary mobility is significantly higher than lattice, in the initial regime, the grain boundary regions are relatively small/thin and unable to accommodate a significant amount of atoms. In the intermediate regime, as these regions grow and free surfaces shrink, grain boundary diffusion becomes dominant and promotes the transition from porous, necked-particle network, to a dense and even more conductive network. The result of the intermediate sintering regime is observed between 250 and 275 °C, where the Ag NPs have sintered into large grains, seen in Figure 4-3(c). This coincides with another significant drop in resistivity. Curing temperatures of 225, 250, and 275 °C were then focused on for investigations on solar cell contact properties.

For screen-printing metallization, high aspect ratios are desired as they minimize front-grid shading [164]. Here, the lines printed with 3 printing passes in a 250-micron-wide pattern had widths of 700-1000 microns after curing, with higher curing temperatures resulting in wider lines. This reveals that the solvent has a strong tendency to wet the poly-Si(n) surface before it evaporate and that the degree of wetting increase at higher curing temperatures. As a result, the printed Ag features were not high-aspect ratio. Rather, the Ag thickness was greater in the pyramid valleys and the amount of coverage on the pyramid tops increased with increasing number of printing passes. This is shown in Figure 4-3(d) and (e). To ensure full coverage of the textured surface, 3 print passes were used for all contact property tests.

4.3.2 TOPCon contact properties with low-temperature Ag metallization

After identifying the Ag NP sintering regimes and the impact on Ag resistivity, experiments on the impact of the sintering process on passivation quality were performed on well-passivated TOPCon structures with 40-nm-thin poly-Si(n). The Sinton iV_{oc} for the passivation samples in Figure 4-1(c) were 725-730 mV. Ag was deposited on half of these samples as shown in Figure 4-4 (a) and cured from 250-600 °C. Figure 4-4 (b) shows a PL image of the precursor sample before it received Ag printing and curing at 275 °C. The ERE map of this same sample is shown in Figure 4-4 (c). Though the ERE maps have

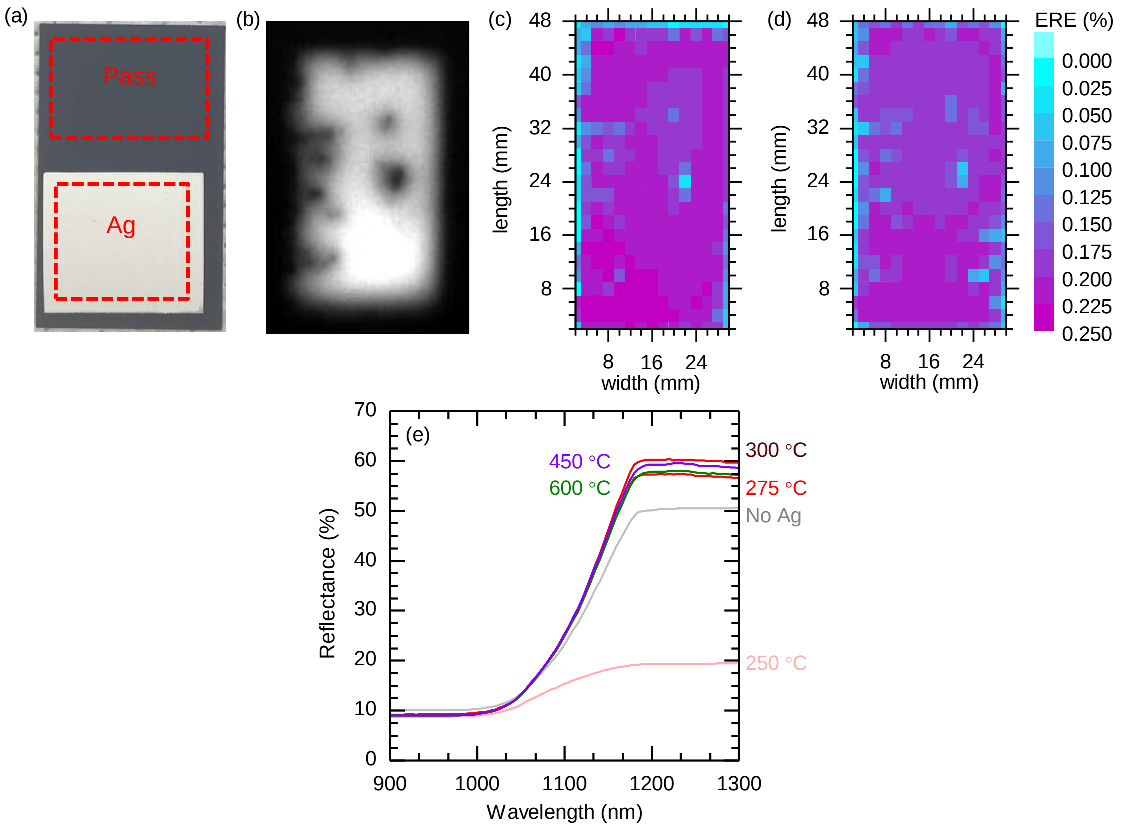


Figure 4-4. (a) Photograph of sample after Ag ink printing and curing. (b) PL image of pre-metallized sample. (c) ERE map of the same pre-metallized sample. (d) ERE map of the same sample post-metallization and curing at 275 °C. (e) Reflectance for each sample post-metallization cured from 250-600 °C with pre-metallized reference.

lower resolution due to the 2 mm spacings between measurements, there is good matching between the data from PL and ERE. Figure 4-4 (d) shows the ERE map for the same sample but after printing and curing at 275 °C. Qualitatively, a small drop in ERE signal (shift to lighter purple) appears across the full sample. To ensure the sintering process did not cause large variation in optics that could impact the ERE signal, reflectance was measured pre- and post-metallization, shown in Figure 4-4 (e). This plot shows significant parasitic absorption by Ag for the sample cured at 250 °C and improved rear reflectance for all curing temperatures over 275 °C. At 250 °C, the Ag film was formed predominantly through particle necking. The rear poly-Si(n)/Ag interface is likely comprised of regions with nanoscopic pores or rough features, inducing more absorption than an ideal, smooth surface. Since the rear poly-Si(n)/Ag surface is absorptive when cured at 250 °C, it was not used in subsequent ΔiV_{oc} calculations from the ERE data sets as the reduced luminescence signal would be from parasitic absorption of the silicon emission rather than metallization-induced recombination.

Figure 4-5 shows the distribution of ERE data from each map divided into each region of the sample (passivated vs. Ag), curing temperature (275-600 °C), and pre- and post-metallization. The plot also shows ΔiV_{oc} post-metallization, which was calculated with the average ERE value of the passivated area and the Ag-metallized area, respectively, with Equation 4.1. A minor systematic loss in passivation (0.4-3 mV) occurs pre- and post-metallization as seen qualitatively in the ERE maps in Figure 4-4. This is likely due to surface scratching from sample transfer onto the inkjet printing chuck and hotplate. These losses impact the passivated and Ag areas equally and no significant difference in ΔiV_{oc} is

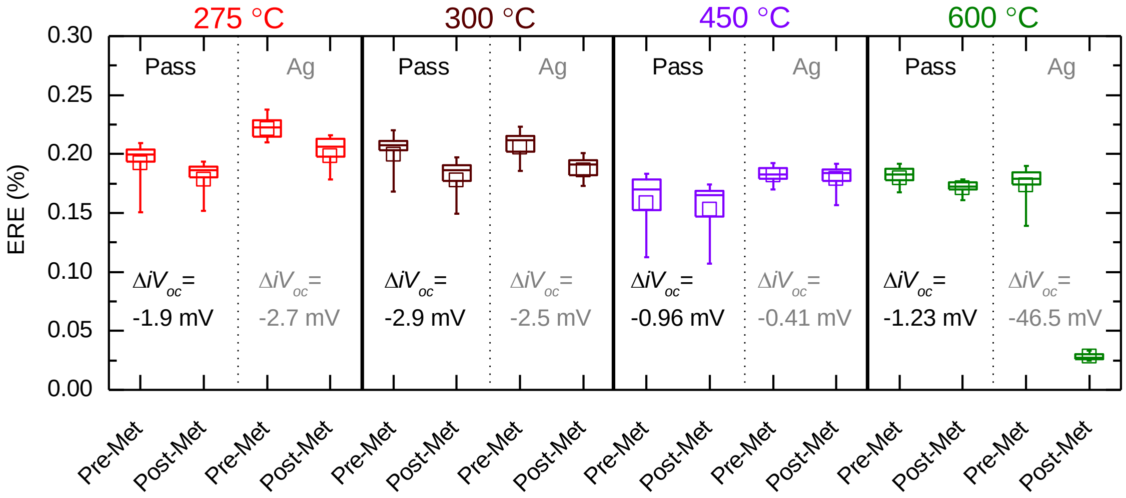


Figure 4-5. ERE data from the full maps divided into the passivated areas and Ag-metallized areas pre- and post-Ag metallization and curing at temperatures from 275-600 °C. Also shown is ΔiV_{oc} post-metallization calculated with the average ERE value. Boxes represent 25–75 percentiles, whiskers represent 10–90 percentiles, and inset boxes and lines represent mean and median values, respectively.

observed due to metallization, until curing at 600 °C. Thus, the sintering mechanics of the low-temperature Ag contact mechanism do not impact the passivation quality, even when poly-Si(n) is as thin as 40 nm, until thermal treatments far beyond what is required for high finger conductivity. At temperatures over 450 °C, Ag likely diffuses through polysilicon grain boundaries, reaches the c-Si/SiO_2 interface, and perturbs the chemical passivation, though more characterization is required to validate this. Although poly-Si grain boundary diffusivities haven't been studied for Ag to the author's knowledge, grain boundaries are preferential to polysilicon bulk diffusion for Al and P [165, 166]. Relatedly, the iV_{oc} of c-Si(n)/SiO_2/poly-Si(n) samples metalized with e-beam-evaporated Al dropped by over 50 mV after annealing at 400 °C for 30 minutes relative to as-deposited, likely from Al diffusion through polysilicon grain boundaries [167].

In addition to passivation quality, contact resistivity was studied by printing low-temperature Ag ink TLM pads onto c-Si(n)/SiO_2/poly-Si(n) samples, shown in Figure 4-1(b). I–V sweeps from -2 to 2 V between adjacent Ag pads revealed Ohmic contact for all curing temperatures, which was not observed in prior work on low-temperature Ag paste containing binder resins Figure 4-6 shows the contact resistivity data of samples cured at 225, 250, and 275 °C, revealing overlapping distributions and no apparent trend between sintering regime and contact resistivity. The relatively wide spread of data is attributable to variations in pad widths and lengths from solvent spreading during curing and also from probing variations observed while performing the standard TLM methodology. The pad area and spacings used for TLM calculations was not from the printer recipe, but rather from optical microscope measurements of the printed TLM pad dimensions after curing. Though this procedure increases accuracy relative to using the print recipe geometries, there is likely some discrepancy from the true dimensions as the solvent does not spread equally in all directions and for all curing temperatures. Additionally, the measured values

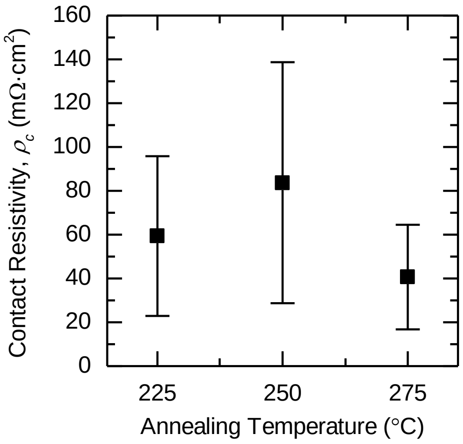


Figure 4-6. Contact resistivity of c-Si(n)/SiO_2/poly-Si(n)/Ag metallized with low-temperature Ag ink and cured at 225, 250, or 275 °C.

of pad-to-pad resistance dropped upon successive measurements with a 4-point I–V probe station or a multimeter. The application of downward pressure on the TLM pads, such as that applied during probing, caused a systematic reduction in the measured pad-to-pad resistance on every tested sample. Contact resistivity in Figure 4-6 was calculated from pad-to-pad resistance values that had saturated to a relatively stable, consistent value. Overall, the average ρ_c values from the printed Ag ink are about 20-fold higher than as-deposited sputtered Ag values [151]. This reveals that the low-temperature Ag contact mechanism in air is limited relative to well-formed sputtered or evaporated Ag interfaces with poly-Si(n).

4.3.3 Contact resistance of sputtered references

To investigate potential issues limiting contact resistance with Ag ink, an annealing series from 100-300 °C on several reference structures metallized with sputtered films was tested. The reference samples had varied substrate texture (saw damage removal etching or KOH-texture), anneal ambient (air or nitrogen glovebox), and metallization stack (ITO/Ag or Ag). As the focus is on the poly-Si(n)/Ag interfaces, no etching of poly-Si(n) between sputtered ITO/Ag or Ag TLM pads was performed. The contact resistivity anneal series are shown in Figure 4-7.

As expected, the as-deposited c-Si(n)/SiO_2/poly-Si(n)/Ag contact resistivity is low: 5.0 and 6.8 $m\Omega\cdot cm^2$ for textured and planar substrates, respectively. While the contact resistance degrades for both substrate types at relatively low temperatures (125-150 °C) in air, no degradation occurs when annealed in nitrogen ambient up to 300 °C. It is possible that even higher temperatures could have caused some degradation to the samples annealed in nitrogen since Hayes *et al.* found c-Si/SiO_2/poly-Si(p)/Ag contact resistivity increased from 90 m$\Omega\cdot$cm^2 to over 250 m$\Omega\cdot$cm^2 after annealing at 400 °C in argon ambient [154]. From these results, the annealing ambient clearly plays a significant role in contact resistance stability.

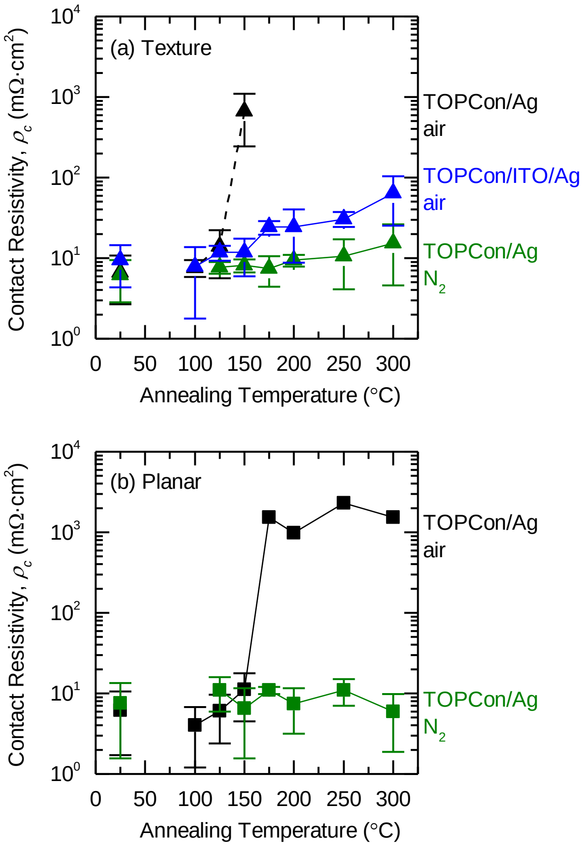


Figure 4-7. Contact resistivity data of sputtered reference samples on (a) fully textured wafers and (b) wafers with saw-damage removal etching and no KOH-texture.

Similarly, Alford *et al.* showed that the ambient plays a significant role in Ag thin film thermal stability due to its impact on Ag agglomeration during annealing; for a given annealing temperature, agglomeration and island formation of Ag thin films occurs much faster in oxygen ambient than under vacuum or an inert gas ambient and leads to a large rise in sheet resistance due to discontinuities in the Ag film [168]. The impact of oxygen on Ag films during annealing is primarily due to increased surface self-diffusion rates of Ag in addition to Ag vacancy transport from interacting with oxygen that has diffused to

Ag interstitial sites [169-171]. For this reason, simply curing the Ag NP ink in nitrogen ambient is not a solution to reduce its contact resistivity; after curing a sample with Ag ink in the same nitrogen glovebox at 350 °C for 90 minutes, the Ag film R_{sheet} was over 100 Ω/□, similar performance as a sample annealed in air at 200 °C for 5 minutes. The lack of oxygen during curing severely attenuated rates of Ag surface diffusion, which is a major diffusion pathway during the initial sintering regime, resulting in very little film densification and high resistivity.

While some contact resistance degradation occurs for poly-Si(n)/ITO/Ag in air with increasing annealing temperature, the degradation is much less severe than poly-Si(n)/Ag, indicating that in addition to the large impact of oxygen in the ambient, an interaction unique to the poly-Si(n)/Ag interface also accelerates degradation. Based on this data, the options that may cause poly-Si(n)/Ag degradation during annealing in air are a chemical interaction at the interface involving oxygen, a decrease in Ag-contacted area resulting from Ag diffusion, or a combination of both.

4.3.4 Materials characterization of Ag ink and sputtered Ag films

In order to investigate possible mechanisms leading to contact resistance degradation of the sputter-metallized interfaces, materials characterization was performed. Surface SEM images of several sputtered reference TLM samples are shown in Figure 4-8. For the TOPCon/Ag samples, annealing in air leads to drastic Ag grain growth. Additionally, the surface morphology of the sample annealed at 250 °C has deviated from the as-deposited condition; as-deposited, the Ag film completely conformed to the random pyramid texture

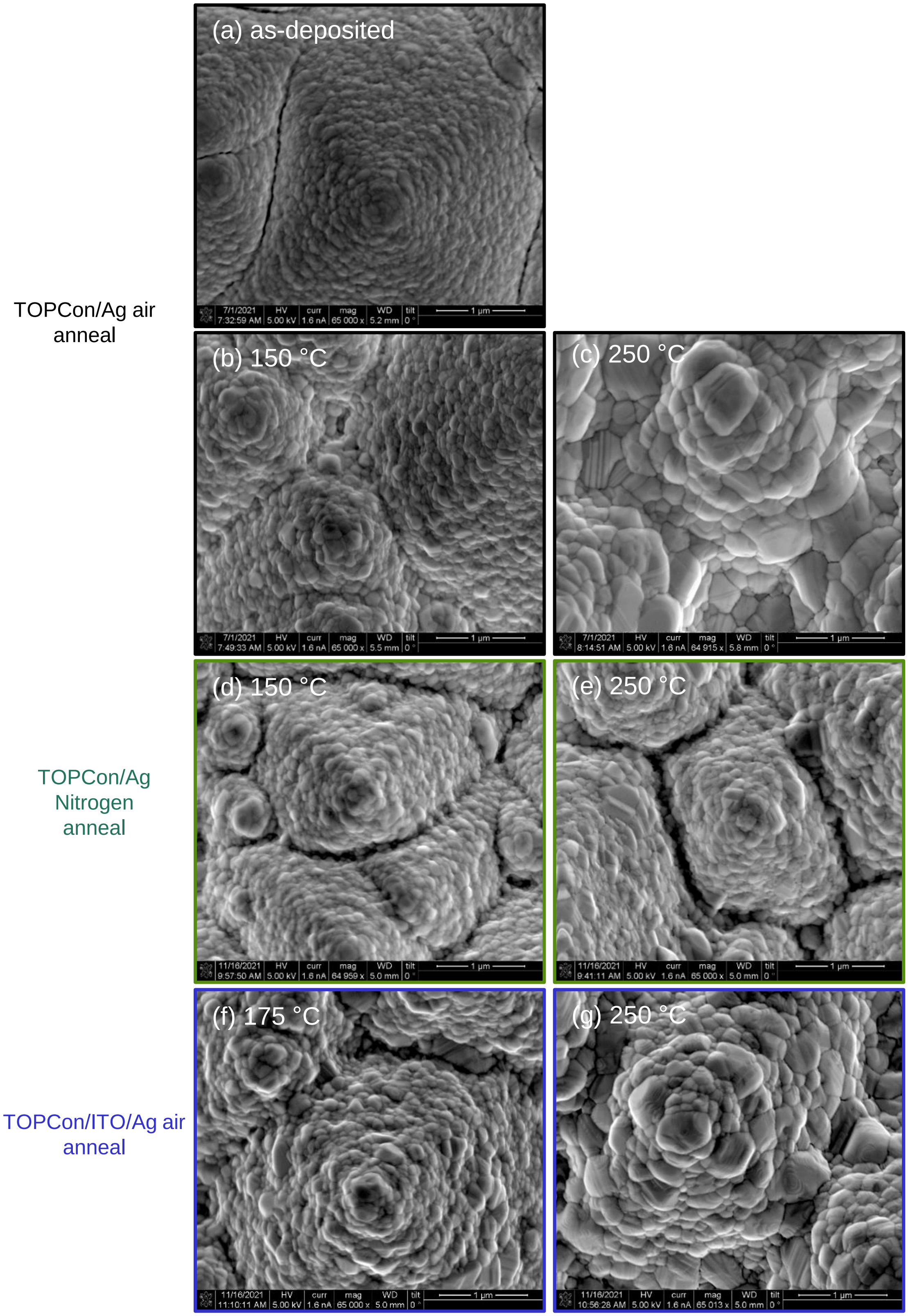

TOPCon/Ag air anneal
TOPCon/Ag Nitrogen anneal
TOPCon/ITO/Ag air anneal
(a) as-deposited
(b) 150 °C
(c) 250 °C
(d) 150 °C
(e) 250 °C
(f) 175 °C
(g) 250 °C
1 µm

Figure 4-8. Surface SEM images of the c-Si(n)/SiO_2/poly-Si(n)/Ag contact resistivity samples (a) as-deposited, (b) annealed in air at 150 °C, (c) annealed in air at 250 °C, (d) annealed in nitrogen ambient at 150 °C, (e) annealed in nitrogen ambient at 250 °C. Surface SEM images of the c-Si(n)/SiO_2/poly-Si(n)/ITO/Ag contact resistivity samples (f) annealed in air at 175 °C, and (g) annealed in air at 250 °C.

of the underlying substrate but after annealing at 250 °C, the texture morphology has become much less apparent, and seemingly more planarized. In contrast, SEM images of the poly-Si(n)/Ag samples annealed in nitrogen, which had no contact resistance degradation, show the Ag film conformably coated the substrate texture and no apparent difference in grain size between 150 and 250 °C. On the other hand, the poly-Si(n)/ITO/Ag samples exhibited increased thickness nonuniformities along the pyramid bases at 175 °C and significant grain size increase at 250 °C, though not as drastic as the poly-Si(n)/Ag sample annealed in air at the same temperature.

From the SEM images, it is apparent that the as-deposited Ag films are driven to agglomerate during annealing, similarly observed in several studies, with the driving force of agglomeration attributable to overall energy minimization of surfaces, interfaces, and grain boundaries [172-175]. As mentioned before and confirmed in these SEM images, oxygen plays a central role in Ag agglomeration by lowering the energetic barrier for Ag surface self-diffusion. Since surface self-diffusivity increases exponentially with increasing temperature, annealing temperature leads to more rapid kinetics and larger changes in film microstructure and morphology, also observed in the SEM images [173]. On the macroscale, characteristics of Ag agglomeration are hillock formations at the film surface and void formation and growth within the film [174, 175]. Additionally, grain growth within the polycrystalline film is a strong driver of the void/hole growth that can eventually lead to solid-state dewetting which reduces Ag contacted area fraction to the underlying substrate [173, 176].

As these SEM images show qualitative observations of Ag surface nonuniformities and grain growth, which are both characteristic of solid-state dewetting, XRD is performed on Ag ink and sputtered Ag samples to quantity the microstructure changes as a function of

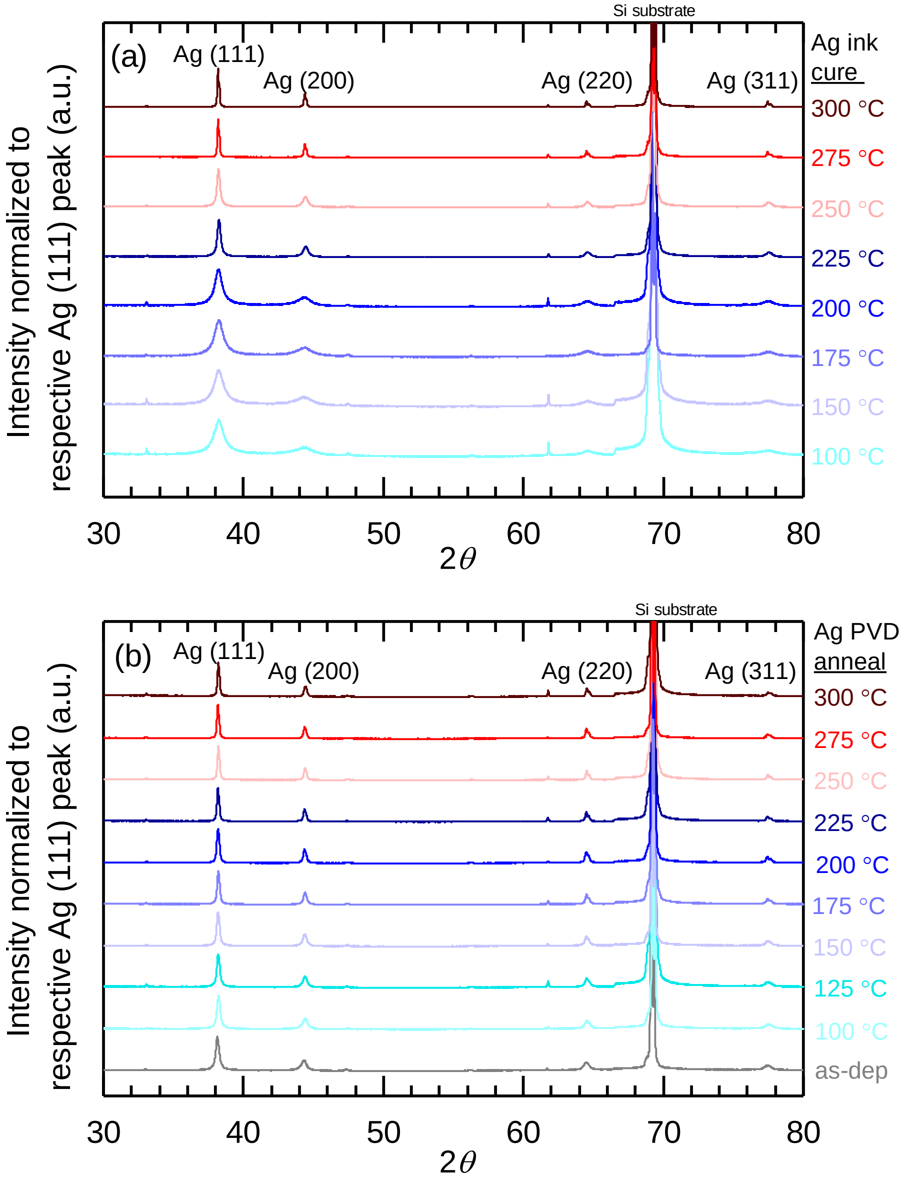


Figure 4-9. XRD line scan series for c-Si(n)/SiO_2/poly-Si(n)/Ag where metallization is performed with (a) Ag ink and (b) Ag sputtering.

annealing temperature. The XRD line scans for Ag ink and Ag PVD samples are shown in Figure 4-9(a), and (b), respectively. These plots show clear peak narrowing with increasing annealing temperature for all Ag peaks for both Ag ink and Ag PVD 2Θ line scans. The Williamson-Hall technique is used to calculate strain and crystallite size from each respective line scan. These values are shown in Table 4-1. Good linear fits with the Williamson-Hall technique could not be achieved for Ag ink line scan data below 225 °C, so they are omitted from the table. Qualitatively, the Ag ink displays minimal peak narrowing in the range between 100-200 °C. On the other hand, the Ag PVD sample does show significant crystallite size increase from as-deposited to 200 °C: 30.4 nm to 56.4 nm. Below 200 °C, the Ag NPs within the ink likely still have the dispersants which prevent surface diffusion and grain growth until they are burned off at a temperature above 200 °C.

The XRD line scans confirm and quantify the degree of grain growth for different temperature ranges for Ag ink and Ag PVD. The significant increase in grain growth is evidence that dewetting and consequently, a change in Ag contacted area could contribute to the drop in contact resistivity for sputtered Ag during annealing and be limiting the ability of Ag ink to reach lower contact resistivity. However, the role of the poly-Si(n)/Ag interface is certainly crucial to the contact resistivity behavior and still not understood. In the absence of a chemical basis, the energy of the film-substrate interface could impact diffusion pathways by providing a faster diffusion pathway and enabling larger grain growth. This has been demonstrated experimentally, where the substrate has been shown to have a large impact on thermal stability against dewetting during annealing [177]. The difference in Ag agglomeration in poly-Si(n)/ITO/Ag and poly-Si(n)/Ag samples shows the importance of interfacial energy between Ag and the underlying film and that the poly-

Table 4-1. Williamson-Hall analysis on Ag ink and Ag PVD XRD line scans.

Temp. (°C)	Ag PVD strain (ε)	Ag PVD crystallite size (nm)	Ag ink strain (ε)	Ag ink crystallite size (nm)
As-dep.	0.0018	30.4	-	-
100	0.0017	34.0	-	-
125	0.0015	39.6	-	-
150	0.0015	44.7	-	-
175	0.0015	54.0	-	-
200	0.0012	56.4	-	-
225	0.0013	71.8	0.0009	24.3
250	0.0013	74.5	0.0008	26.9
275	0.0013	75.2	0.0015	111.8
300	0.0013	76.6	0.0015	118.5

Si(n)/Ag interface is a significant contributor to greater agglomeration compared to ITO/Ag. In other words, diffusion of Ag atoms along the poly-Si(n)/Ag interface could be much faster than along the ITO/Ag interface.

While atmospheric gases impact diffusivities and consequently Ag grain growth, atmospheric gases could also be playing an important role in chemical interactions at the poly-Si(n)/Ag interface. Pure Ag is known to be highly sensitive to sulfur-containing atmospheric gases such as hydrogen sulfide (H_2S) and carbonyl sulfide (COS), with the reaction producing silver sulfide (Ag_2S) [178]. The corrosion of Ag through sulfurization only occurs in the presence of moisture, where surface water layers provide a medium for adsorption of H_2S and COS and lead to the dissolution of Ag [178, 179]. Although sulfur-containing gases have low concentration in ordinary atmospheric conditions (0.3-0.6 parts per billion), they are nonetheless commonly observed to corrode/tarnish Ag, causing a subsequent degradation of electronic devices [168, 179]. Device degradation is due to the properties of the sulfurization product, Ag_2S, which has resistivity 7-10 orders of magnitude higher than pure Ag as well as poor mechanical strength, which readily leads to detachment from underlying films or substrates [179]. Although Ag is much more chemically inert to oxidation under atmosphere compared to sulfurization, oxygen could impact the poly-Si(n) surface, creating an additional barrier to transport across the interface [179, 180].

To investigate the hypothesized mechanisms of contact degradation—solid-state dewetting of Ag and/or interfacial chemical reactions of atmospheric gases—high-resolution STEM imaging and EDXS elemental maps were performed on the Ag-metallized TLM structures. Figure 4-10 shows STEM images of the as-deposited c-Si(n)/SiO_2/poly-Si(n)/Ag TLM sample, which had an average contact resistivity of 5.0 $m\Omega\cdot cm^2$. These images show the Ag film establishing smooth contact to the underlying poly-Si(n) layer with no apparent interfacial disruptions. The surface SEM images from Figure 4-8(a) similarly showed the as-deposited Ag film smoothly conforming to the texture of the underlying substrate; though after annealing, the Ag surface appeared more non-uniform and the substrate texture became less apparent, seen in Figure 4-8(b) and (c).

Figure 4-11(a) and (b) show STEM images of a sister c-Si(n)/SiO_2/poly-Si(n)/Ag TLM sample that was annealed at 200 °C in atmosphere. Exact contact resistivity values could not be obtained for these samples due to non-linear pad-to-pad resistance, but increased by at least an estimated 1-2 orders of magnitude relative to the as-deposited sample. At 200 °C, the average Ag grain size grew to about 54 nm, calculated from XRD line scans. This growth can be seen qualitatively in the STEM images. Such Ag agglomeration is an indication that the Ag film is driving toward solid-state dewetting. These images do indeed reveal disruptions at the poly-Si(n)/Ag interface in the form of voids. Such voids are absent in the as-deposited STEM interfacial images from Figure 4-10. Thus, it seems likely that

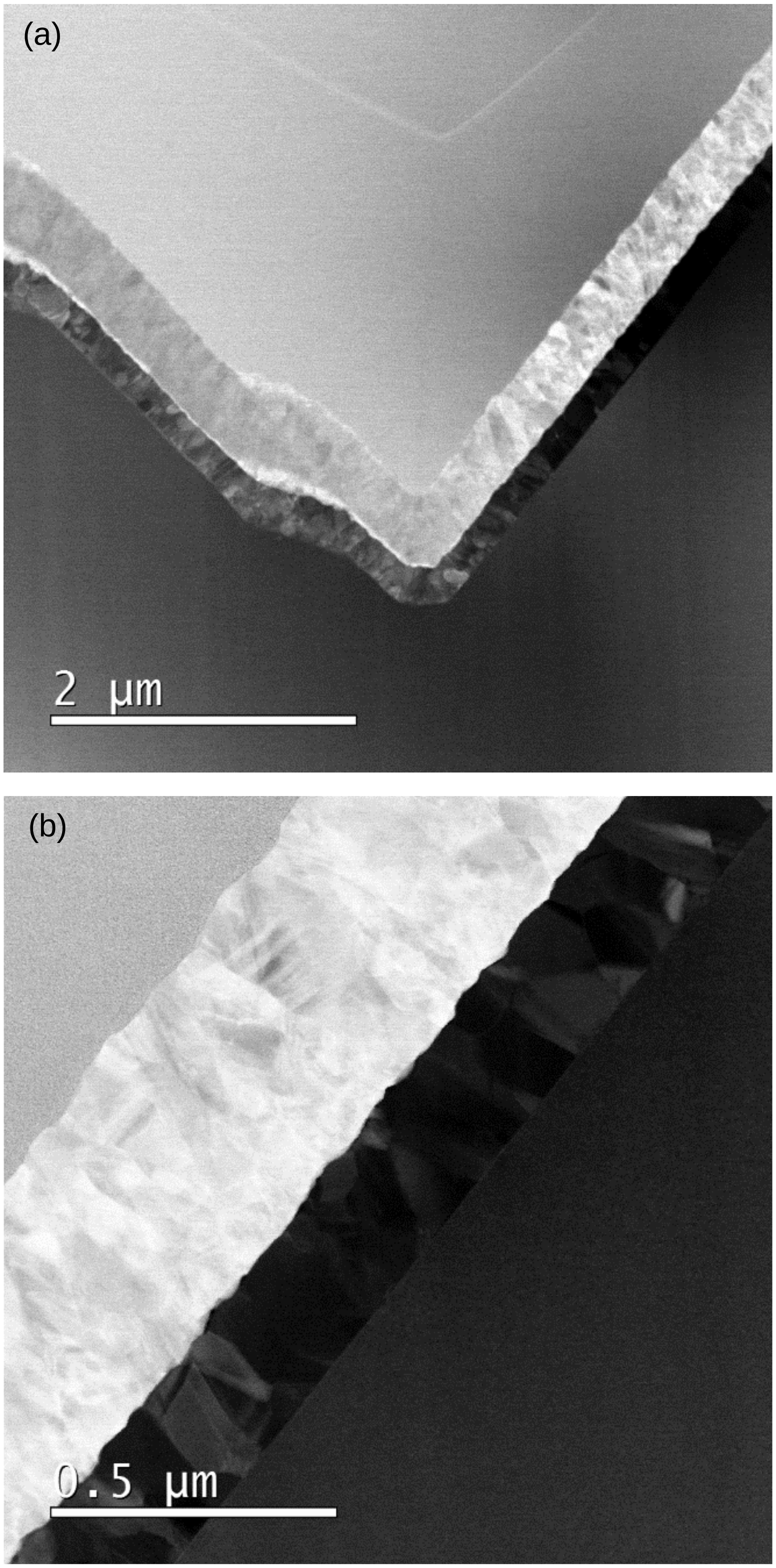


Figure 4-10. (a-b) Cross-section STEM images of a c-Si(n)/SiO_2/poly-Si(n)/Ag TLM sample with no annealing.

the Ag diffusion processes culminating in Ag grain growth do indeed drive structural changes that at a minimum reduce contact area. However, such reductions in contact area alone may not entirely reduce the contact resistivity after annealing as interfacial chemical reactions may also drive degradation.

EDXS elemental maps corresponding to Figure 4-11(b) for Ag, S, Si, and O are shown in Figure 4-11(c), (d), (e), and (f), respectively. The absence of Ag or Si signal in the void area further confirm that the poly-Si(n)/Ag interface has been separated. The elemental maps also reveal weak S signal in the Ag bulk with a marked increase in S signal at the Ag edge. As mentioned above, the sulfurization of Ag leads to the growth of Ag_2S, which has poor mechanical properties and much higher resistivity than pure Ag. These changes at the poly-Si(n)/Ag interface would certainly lead to large increases in contact resistivity and are consistent with the trends observed for c-Si(n)/SiO_2/poly-Si(n)/Ag TLM samples annealed in atmosphere. On the other hand, the samples annealed in nitrogen ambient did not increase in contact resistivity for temperatures up to 300 °C. While the ambient impacts Ag diffusion rates and consequently Ag grain growth due to oxygen concentration, another major difference between atmosphere and the nitrogen ambient is the humidity level. This may be crucial as the presence of moisture is required for Ag corrosion [178]. In the facilities used in this study, the nitrogen glovebox humidity was below 1 ppm, while the relative humidity (RH) in the open laboratory atmosphere was 38%, an over 3-order-of-magnitude increase over the nitrogen glovebox. While the lack of oxygen slowed down Ag diffusion in the nitrogen glovebox, leading to slower Ag diffusion and grain growth, the lack of moisture may have prevented Ag corrosion at the poly-Si(n)/Ag interface, leading

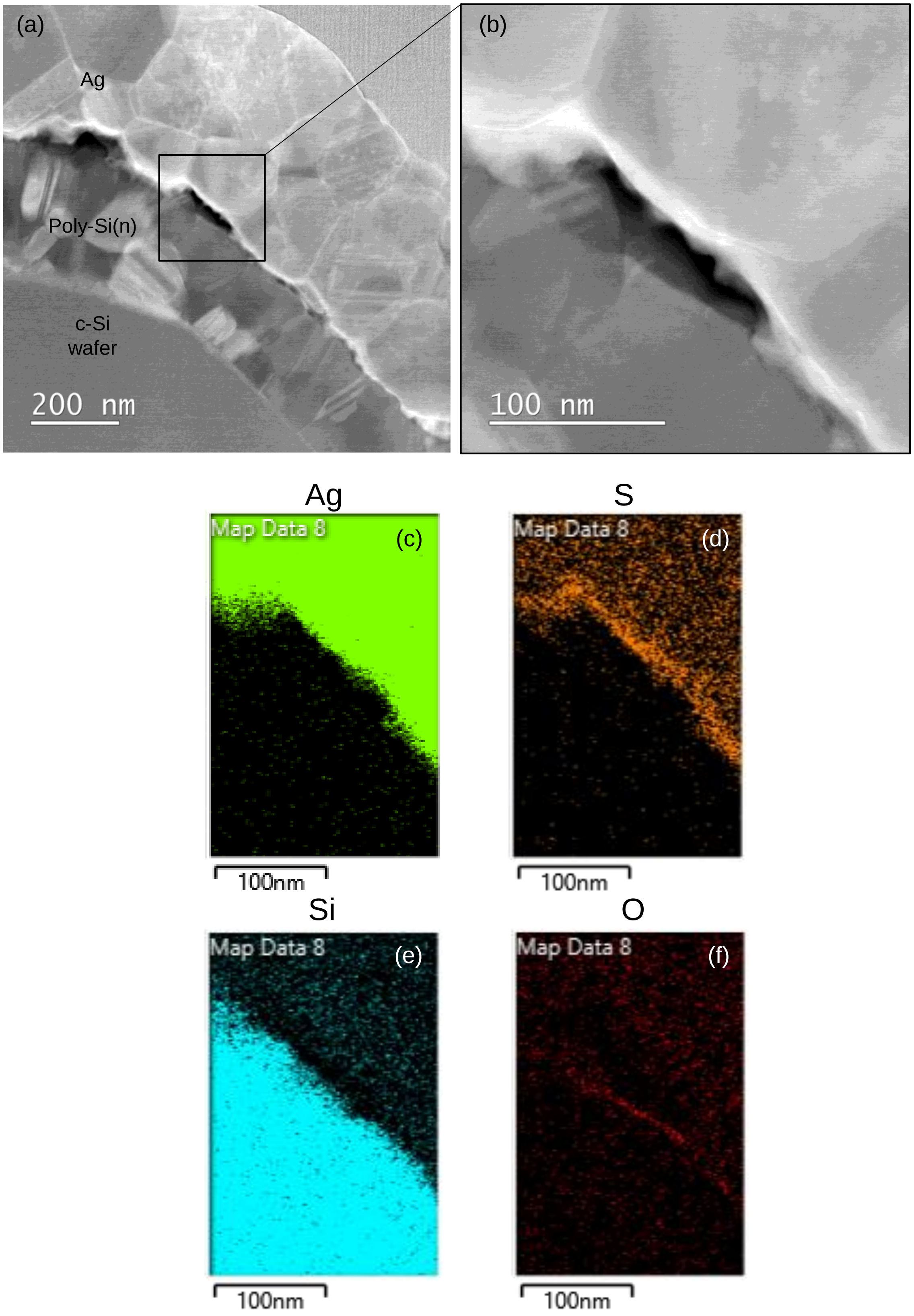

(a)
Ag
Poly-Si(n)
c-Si
wafer
200 nm
(b)
100 nm
Ag
Map Data 8
(c)
100nm
S
Map Data 8
(d)
100nm
Si
Map Data 8
(e)
100nm
O
Map Data 8
(f)
100nm

Figure 4-11. (a-b) Cross-section STEM images of c-Si(n)/SiO_2/poly-Si(n)/Ag TLM sample that was annealed at 200 °C in atmosphere. (c-f) EDXS elemental maps at the poly-Si(n)/Ag interface showing local concentrations of Ag, S, Si, and O, respectively.

to constant contact resistivity values across annealing temperatures from 100-300 °C. Thus, degradation of the poly-Si(n)/Ag interface due to sulfurization is a plausible hypothesis that is consistent with the contact resistivity results split between atmosphere and nitrogen annealing ambient.

It is also possible that the hypothesized mechanisms of grain growth and dewetting and interfacial chemical reactions are operating simultaneously. While the STEM results here strongly indicate that Ag grain growth leads to void formations which reduce Ag contact area, the observed reduction in contact area alone seems unlikely to cause a drop in contact resistivity of at least 1-2 orders of magnitude. It is possible that the prominent Ag microstructure changes during annealing lead to voids, pores, and hillocks at the Ag surface and interface which increases the permeability of the corroding sulfur-containing gases to the reactant Ag. The presence of moisture, increased reactant permeability, and elevated temperatures all increase silver corrosion rates and could be leading to formation of AgS_2 at the poly-Si(n) interface [179]. This would be consistent with the increased S concentration from the EDXS elemental maps.

4.4 Conclusion

A low-temperature Ag ink was studied as a model system for the low-temperature Ag contact mechanism to SiO_2/poly-Si(n) passivating contacts. The low-temperature contact process does not damage the high-quality passivation provided by the SiO_2/poly-Si(n) passivating contact, even with a thin poly-Si(n) layer of 40 nm, until over 450 °C, where

Ag diffusion through polysilicon grain boundaries likely leads to the degradation. The metallization approach did suffer from inferior contact resistivity compared to as-deposited sputtered poly-Si(n)/Ag. However, contact resistivity of poly-Si(n)/Ag also degraded when annealed in air. Materials characterization of the Ag ink and sputtered Ag films revealed that grain growth and solid-state dewetting likely contribute to the contact resistance degradation. Additionally, the gas species in the annealing ambient play a major role. The major differences between the atmosphere and nitrogen ambient were identified as oxygen and moisture. While oxygen impacts Ag diffusivity and grain growth rates, moisture is strongly linked to Ag sulfurization. Initial STEM and EDXS results indicate that Ag does detach from poly-Si(n) during annealing, which may be from a combination of solid-state dewetting or formation of AgS_2, which is known to be resistive and mechanically weak. Further work is needed to investigate these interfacial chemical reactions that may be limited contact performance as well as possible oxygen-based chemical interaction at the poly-Si(n) surface. Based on the sputtered reference poly-Si(n)/Ag contacts, such an interactions initiate between 125-150 °C.

Regarding application of the low-temperature Ag contact mechanism, both grain growth and chemical reaction considerations are important for stable contacts. Toward this end, dewetting could be mitigated by using an ink or paste with smaller particles to establish initial contact and then larger particles or flakes to establish lower bulk resistivity. Additionally, surface modifications to poly-Si could be performed to reduce the poly-Si/Ag interfacial energy. Investigations on near-infrared sintering of Ag inks show that Ag inks can be cured at reduced temperatures of 120 °C, which enables a pathway to avoid ambient anneals at temperatures where the sputtered samples degrade [181]. Finally, an annealing ambient with appreciable oxygen but no moisture could be used to ensure particle sintering to the poly-Si layer but avoid possible corrosion reactions.

CHAPTER 5

ALUMINUM-SILICON INTERDIFFUSION IN SILICON HETEROJUNCTION SOLAR CELLS WITH a-Si:H(i)/a-Si:H(n/p)/Al REAR CONTACTS

5.1 Introduction

To prevent degradation of the hydrogenated amorphous silicon (a-Si:H) layers in silicon heterojunction (SHJ) solar cells, the cells are typically metallized by screen-printing low-temperature Ag paste or sputtering Ag on indium-oxide-based transparent conductive oxides (TCOs) [182]. Techno-economic modeling by Louwen *et al.* in 2016 showed that Ag and In-containing films are the costliest components of a SHJ cell after the high-purity n-type c-Si wafer. Specifically, the rear ITO/Ag layers in screen-printed bifacial and full-area- sputtered configurations account for approximately 18% and 9% of cell production cost, respectively [183]. The low-temperature pastes used are more resistive than high-temperature Al-BSF/PERC pastes and, consequently, more costly due to the higher Ag consumption required to achieve sufficiently low lateral resistivity [182]. The PV industry already accounts for approximately 11% of the global Ag market supply, and because of continued demand, the bulk cost of Ag is expected to remain high [184].

As a result, metallization techniques to SHJ cells that reduce or eliminate Ag consumption are an active area of research. Alternative metallization approaches include Smart Wire Connection Technology, drop-on-demand printing of low-temperature Ag inks, screen-printing of Cu-based pastes, electroplating of Cu, and application of metals other than Ag with no TCO [185-190]. According to the aforementioned 2016 techno-economic modeling, embracing the latter approach and replacing physical-vapor-deposited (PVD) ITO/Ag with a single Al layer would reduce the cost contribution of the rear metallization from 2.6 ¢/Watt to 0.7 ¢/Watt [183]. For PVD metallization, an even more insidious cost effect than the material cost is the large capital investment requirements, which limits the manufacturing growth rate and makes competition difficult with incumbent screen-printing [191]. A single rear Al layer would reduce the number of tools—and thus the capital barrier—needed to enter into or expand cell manufacturing.

It is because of low cost and adequate electrical conductivity that the solar industry already employs Al metallization extensively; Al-BSF and Passivated Emitter and Rear Contact (PERC/PERL) technologies with Al metallization comprised over 95% of the worldwide silicon module market share in 2019 [11]. However, the direct contact of the Al paste to the c-Si absorber in these cell structures causes large recombination losses and severely limits the upper limit of device efficiency. Passivating contacts, such as SHJ contacts, avoid these recombination losses by electronically separating the absorber from the metal electrode and, consequently, are expected to capture increasing market share [11]. Existing Al pastes are not viable for SHJ cells, however, as the processing temperatures are incompatible: degradation of the surface passivation due to hydrogen effusion occurs well-below the paste firing temperature [192]. Further, no low-temperature Al paste analog currently exists for SHJ technology. Consequently, PV researchers exploring Al metallization for use in SHJ devices employ PVD processes such as thermal evaporation and sputtering.

Prior to use in SHJ solar cells, stacks of a-Si:H and Al were studied in depth due to the dramatic amount of atomic movement at surprisingly low annealing temperatures and for their potential to form low-cost poly-crystalline Si [193-196]. The degree of Si-Al interdiffusion upon low-temperature annealing is remarkable and can result in complete layer exchange of the Si and Al across the interface [197]. When applied as a contact for c-Si solar cells, a-Si:H/Al stacks exhibit low contact resistance. For instance, Labie *et al.* demonstrated contact resistivities of 10 mΩ·cm^2 for a-Si:H(i)/a-Si:H(n)/Al contacts [198]. Such low values make these contacts appealing for implementation in SHJ cells; however, simultaneously maintaining the excellent passivation afforded by the a-Si:H has proven to be a challenge due to the Si-Al interdiffusion at low temperatures.

For a-Si:H/Al stacks in SHJ devices, the Al atomic reservoir is significantly larger than the adjacent Si because the a-Si:H films are so thin. Further, a-Si:H contains relatively high free energy from its high degree of disorder and large amount of hydrogen, each of which promote atomic rearrangement within the a-Si:H film during thermal processing [199]. The atomic concentration gradient, coupled with the high free energy, creates a driving force for Al to be incorporated in the a-Si:H film. When Al is integrated into full SHJ cells, this interdiffusion is exhibited as a tradeoff between transport and passivation. Stang *et al.* fabricated SHJ cells with Al metallization and reported an increase in fill factor (*FF*) from 72.9 to 78.7% and a decrease in open-circuit voltage (V_{oc}) from 684 to 649 mV after 10 additional minutes of annealing at 150 °C (following an original 5-minute anneal) [189]. Konishi *et al.* reported the same *FF*–V_{oc} interchange and found that devices with thicker a-Si:H layers maintained their passivation at higher temperatures [190]. Each of these studies attributed this tradeoff to Si/Al interdiffusion, where Al entering the a-Si:H film increases conductivity, and thereby *FF*, but also increases recombination, degrading V_{oc} This general sensitivity of the solar cell figures of merit to a-Si:H thickness and annealing temperature has been observed consistently, but a detailed analysis of the interface interactions has not yet been reported.

Here, we investigate the properties of a-Si:H(i)/a-Si:H(n/p)/Al contacts with varying a-Si:H doped layer thickness and annealing temperatures. Specifically, we characterize the contact resistivity and passivation quality of test structures utilizing the transfer length method (TLM) and photoconductance measurements, respectively. Based on the test structure results, we fabricate and measure full SHJ devices with these contacts. We then link the electrical behavior of the devices to the morphology and composition of the contact interfaces observed in scanning transmission electron microscopy (STEM). By spanning a wide parameter space in a step-wise fashion, this work identifies promising processing conditions for high-performance SHJ cells utilizing Al metallization and provides finer insight into the materials interactions in the contacts.

5.2 Experimental Details

5.2.1 Electrical contact properties

The metrics selected to quantify resistance and passivation quality were, respectively, contact resistivity, ρ_c, and the difference between the implied open-circuit voltage (iV_{oc}) of the initially passivated wafer and the final V_{oc} after all sputtering and annealing steps, $iV_{oc}-V_{oc}$. The latter metric for passivation loss is unusual for contact characterization but functional in this instance. Typically, recombination attributable to diffused and metal contacted regions is quantified with the recombination current prefactor, J_0, which has been measured and reported for numerous solar cell technologies [42, 47, 200]. J_0 is most often calculated with the Kane and Swanson technique utilizing photoconductance data from a Sinton WCT-120 lifetime tester [46]. Since Al-Si atomic interdiffusion has a strong impact on contact recombination and majority carrier conductivity, it is essential to test processing conditions that are fully representative of the final devices, but fully metallized cells are not measurable with photoconductance. We tested 10-nm-thick Al layers, which are thin enough to be compatible with a Sinton WCT-120, but found from cross-sectional electron microscopy that, at least for thick a-Si:H layers (up to 40 nm), such thin Al layers are not representative of full device metallization. Nast *et al.* similarly observed that the film thickness ratio of Al to a-Si:H is a key driver in the interdiffusion process [197]. Therefore, to measure passivation quality, $iV_{oc}-V_{oc}$ was used instead of the drop in iV_{oc}.

For contact resistance samples, n- and p-type Czochralski (Cz) silicon solar wafers were used for a-Si:H(i)/a-Si:H(n)/Al and a-Si:H(i)/a-Si:H(p)/Al contacts, respectively. For passivation test structures, only n-type Cz wafers were used. The wafers were 180 µm thick with a resistivity of approximately 4 Ω·cm. Prior to a-Si:H deposition, all wafers went through texturing in KOH solution, cleaning in Piranha and RCA-B solutions, and final oxide stripping in BOE solution. Next, 6-nm-thick symmetric a-Si:H(i) layers were deposited on all samples using plasma-enhanced chemical vapor deposition (PECVD). For the contact resistance samples, symmetric doped a-Si:H layers with thicknesses of 5, 10, 20, or 40 nm were deposited. For the passivation samples, the rear doped a-Si:H layer was again 5, 10, 20, or 40 nm thick, while the front side had an 8-nm-thick doped a-Si:H layer of the opposite polarity.

For the contact resistivity samples, Al was sputtered using a DC source power of 1 kW and a chamber pressure of 7.1 mTorr through a shadow mask to create a TLM pattern, as shown in Figure 5-1(a). The spacings between adjacent pads were 0.25, 0.5, 1, 2, 4, and 8 mm respectively. For each a-Si:H thickness, the contact resistance of eight samples was measured after sputtering, and then remeasured after hot-plate annealing at 150, 180, 210, or 240 °C for 20 minutes in ambient atmosphere (two samples per temperature).

Additionally, reference samples with ITO/Ag metallization in place of Al were fabricated and measured for comparison. ITO and Ag were sputtered sequentially through a single shadow mask without breaking vacuum. The ITO was deposited using a DC source power of 1 kW, a chamber pressure of 7.1 mTorr, and an oxygen partial pressure of 0.36 mTorr, which is the recipe used at the rear of the final solar cells. For the ITO/Ag references, a single doped a-Si:H thickness (8 nm) was used, but the same annealing temperatures were tested.

The structure of the passivation samples is shown in Figure 5-1(b). iV_{oc} was measured on 16 locations of each wafer, immediately following the a-Si:H PECVD depositions, with a Sinton WCT-120 tool in transient mode. Next, sixteen 2 cm by 2 cm pads of front ITO and rear metal—either Al or ITO/Ag references—were sputtered onto the passivated wafers at the same locations where the iV_{oc} measurements were performed. The front ITO was deposited using a DC source power of 1 kW, a chamber pressure of 5.5 mTorr, and an oxygen partial pressure of 0.17 mTorr. The rear Al or ITO/Ag were deposited using the same conditions as for the contact resistivity samples. The V_{oc} was then measured in the as-deposited state using a Sinton Suns-Voc tool. Finally, the V_{oc} was remeasured after hot-plate annealing at 150, 180, 210, or 240 °C for 20 minutes in ambient atmosphere (four pads per temperature).

5.2.2 Solar cells with full-area rear metallization

The cells followed the same fabrication sequence as the passivation samples but included a final screen-printing step of Namics low-temperature Ag paste before the hot-plate anneal. However, rather than sweeping a range of thicknesses, a single rear doped a-Si:H thickness was chosen for both n-type (40 nm) and p-type (60 nm) contacts based on the performance of the contact resistivity and passivation samples. The a-Si:H(p) was thicker than targeted but nonetheless demonstrated the anticipated results. Additionally, the wafers used for solar cells were front-side textured and rear-side planar, as shown in Figure 5-1(c), to facilitate subsequent electron microscopy of the rear contact. The post-screen-printing annealing temperature was varied to generate cells demonstrating a wide range of contact performance: The a-Si:H(i)/a-Si:H(n)/Al cells were annealed at 150, 180, and 210 ºC, whereas the a-Si:H(i)/a-Si:H(p)/Al cells were annealed at 180, 210, and 240 ºC. All cells were annealed for 20 minutes in ambient atmosphere, except the p-type cell that was annealed at 240 °C, which was annealed for 40 minutes to magnify the effects of

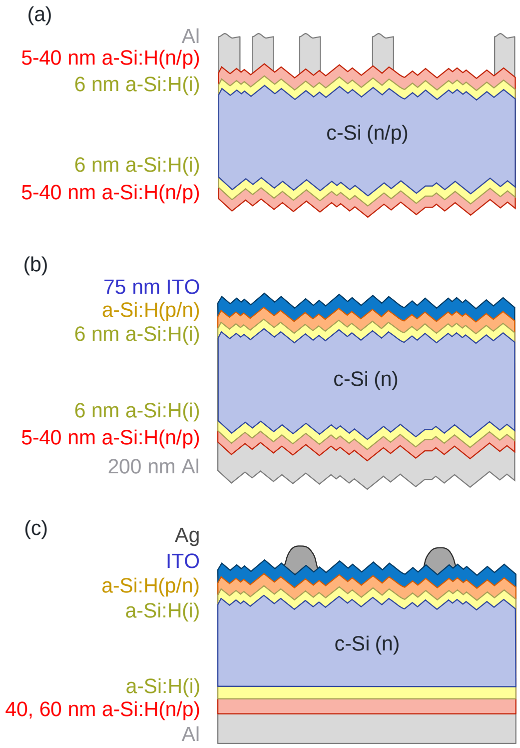


Figure 5-1. Schematics (not to scale) of the (a) test structures used to measure contact resistivity, (b) test structures used to measure passivation quality, and (c) fully fabricated solar cells.

Si-Al interdiffusion. Complementary reference cells with rear ITO/Ag in place of Al were also fabricated for performance comparison. The ITO/Ag cells were annealed after screen-printing at 220 °C for 20 minutes. Current–voltage measurements were performed on each cell using a Sinton FCT-450 I–V tester to extract the solar cell figures of merit. The Sinton FCT-450 I–V tester calculates series resistance by comparing Suns-V_{oc} and I–V sweeps at the maximum power point [201]. The a-Si:H(i)/a-Si:H(n)/Al cells also had TLM structures on the same wafer as the cells, which was not possible with the a-Si:H(i)/a-Si:H(p)/Al cells since n-type wafers were used for all cells.

5.2.3 Electron microscopy and elemental mapping

Changes to the contact interfaces following the annealing step were probed using scanning transmission electron microscopy (STEM). After electrical characterization of the complete solar cells, lamella were lifted out from their rear contacts by focused ion beam and thinned, with final thinning at 5 kV. Bright-field images were taken using a JEOL ARM microscope operated at 200 keV. Elemental maps of samples were obtained using energy-dispersive X-ray spectroscopy (EDXS) to show local concentrations of Al and Si. The n-type sample annealed at 150 ºC was mapped using electron energy-loss spectroscopy (EELS).

5.3 Results and Discussion

5.3.1 a-Si:H(i)/a-Si:H(p)/Al contacts

Figure 5-2(a) shows the contact resistivity of all a-Si:H(i)/a-Si:H(p)/Al test structures. After annealing, all Al-metallized TLM samples showed a significant decrease in contact resistivity to approximately 50 mΩ·cm^2. This initial decrease in contact resistivity can be attributed to breaking of the native silicon oxide overgrowth and improved interfacial

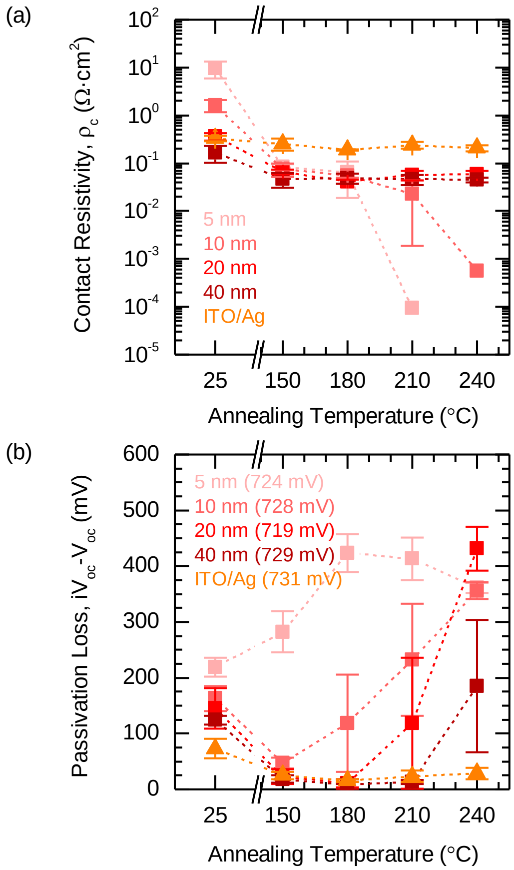


Figure 5-2. (a) Contact resistivity and (b) passivation quality of test structures with a-Si:H(i)/a-Si:H(p)/Al contacts in the as-deposited condition (indicated by 25 °C) and after annealing. The average iV_{oc} values of the initial passivated wafers are shown in parentheses in (b).

adhesion [199]. The contact resistivities of the annealed Al samples were significantly lower than the ITO/Ag controls—which were about 200 mΩ·cm^2, consistent with our previous findings [202]—showing potential for advanced cell architectures utilizing optimized contact fractions and rear reflectors. For an idealized solar cell simulated in Quokka 2 with J_0 = 10 fA, reducing ρ_c from 200 to 50 mΩ·cm^2 results in 0.7% absolute efficiency boost, and the optimized metalized area reduces from over 50% to approximately 25% [39, 203]. All Al samples annealed at low temperatures (150 and 180

°C) exhibited virtually identical contact resistivity. Higher thermal loads (210 and 240 °C) caused a drop of several orders of magnitude in the contact resistivity of the samples with thinner a-Si:H(p) layers (5 and 10 nm). As will be confirmed in Section IIID, such a drop in contact resistivity indicates that Al has entered the a-Si:H film at high concentrations and formed a highly conductive alloy, as observed in prior studies [56, 189, 204]. Additionally, the Al could be reaching the wafer, forming local c-Si/Al contacts with very low resistivity [205].

Further evidence of Al interdiffusion was observed in the passivation samples, in Figure 5-2(b). With sufficient thermal load, the passivation of every Al-metallized structure deteriorated (increase in $iV_{oc}-V_{oc}$), while the ITO/Ag references saw minimal losses. We found no conditions for which the 5-nm-thick samples can maintain high-quality passivation, and only a narrow, low-temperature range in which 10-nm-thick samples can. This result necessitates thicker a-Si:H(p) layers for implementation of direct Al metallization in solar cells. For 20- and 40-nm-thick samples, there is a wider range of acceptable annealing conditions that maintain surface passivation, as similarly observed by Konishi *et al.* [190]. For the 20- and 40-nm-thick samples annealed at 180 °C, the average $iV_{oc}-V_{oc}$ was 11 and 9 mV, respectively. These processing conditions simultaneously resulted in low contact resistivity (40–50 $\mathrm{m\Omega \cdot cm^2}$) and are promising for use at the rear side of full devices.

Another noteworthy result from the $iV_{oc}-V_{oc}$ data is the large variance observed for the intermediate values of a-Si:H(p) thickness and annealing temperature, highlighting the sensitive nature of these contacts to process variation. Conversely, at the extreme temperatures and thicknesses tested, there is greater consistency: A 10-nm-thick a-Si:H layer will almost certainly not maintain passivation when annealed at 180 °C or above, whereas a 40-nm-thick sample will almost surely perform well at most temperatures. Additionally, the lowest and highest annealing temperatures will almost surely result in high-quality and deteriorated passivation, respectively, for most a-Si:H(p) film thicknesses.

5.3.1 a-Si:H(i)/a-Si:H(p)/Al contacts

Figure 5-3(a) shows the contact resistivity of all a-Si:H(i)/a-Si:H(n)/Al contact structures. Contact resistivity decreased for all samples by 2–3 orders of magnitude, relative to the as-deposited values, after annealing at 150 °C. This is evidence that annealing treatments are imperative for direct Al metallization to both n- and p-type a-Si:H. The average contact resistivity of the 20-nm-thick a-Si:H(n) sample annealed at 150 °C was 3.5 $m\Omega\cdot cm^2$, considerably lower than the ITO/Ag references, which were generally around 500 $m\Omega\cdot cm^2$. (This value is on the high end for our reference SHJ process, but it is sensitive to the oxygen partial pressure when sputtering ITO, and that pressure is purposefully high for rear ITO layers because they do not need low sheet resistance and they should be as transparent as possible for IR wavelengths.) For the idealized solar cell simulated in Quokka with J_0 = 10 fA, reducing ρ_c from 500 to 3.5 $m\Omega\cdot cm^2$ results in an absolute efficiency gain of 1.8% and reduces the optimal contact fraction from nearly 100% to approximately 8% [39]. Further, 3.5 $m\Omega\cdot cm^2$ is considerably lower than the lowest reported resistivity value for an a-Si:H(i)/a-Si:H(n)/ITO/Ag contact of 55 $m\Omega\cdot cm^2$ [206]. An anneal at 180 °C further reduced the contact resistivity for the 20- and 40-nm-thick samples, while the thinner samples increased relative to the 150 °C anneal. At higher annealing temperatures (210 and 240 °C), the thicker samples exhibited this same drastic

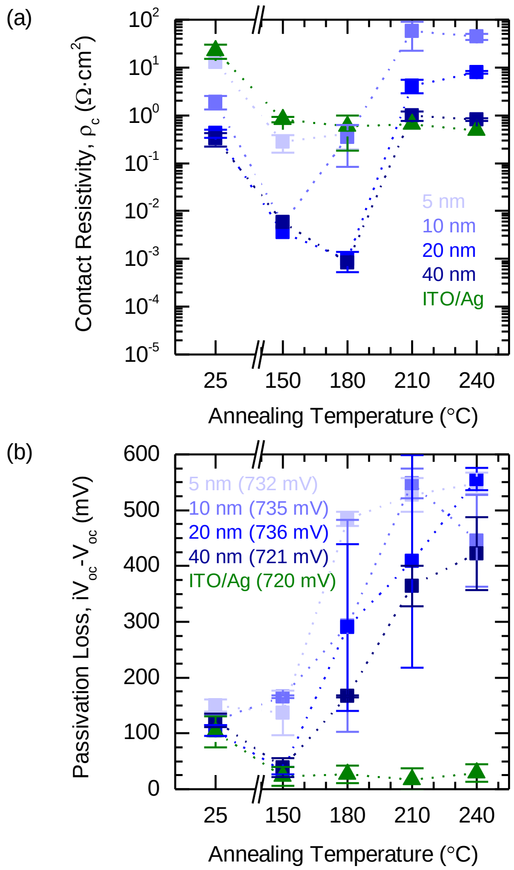


Figure 5-3. (a) Contact resistivity and (b) passivation quality of structures containing with a-Si:H(i)/a-Si:H(n)/Al contacts in the as-deposited condition (indicated by 25 °C) and after annealing. The average iV_{oc} values of the initial passivated wafers are shown in parentheses in (b).

increase in contact resistivity of several orders of magnitude. For the 5-nm-thick samples, the resistance values became immeasurable after annealing at 210 and 240 °C. These trends are in stark contrast to the resistivity decrease with annealing temperature observed for Al in contact with a-Si:H(p), indicating that a drastic event event—such as counter-doping—has occurred.

This hypothesis is supported by the passivation experiment, in Figure 5-3(b), in which $iV_{oc}-V_{oc}$ approached 600 mV (i.e., V_{oc} approached zero) for many samples annealed at the higher temperatures. 240 °C is not hot enough to drive Al into c-Si to induce extra bulk recombination, and surface recombination alone from Al reaching the c-Si surface cannot make the V_{oc} so low. Such a drastic reduction can occur only if both contacts are the same polarity, indicating that the n-type a-Si:H layers must have been counter-doped to p-type. This is in agreement with the TLM data and with prior results from Haque *et al.*, who showed a-Si:H(n) can be fully converted to p-type at 200 °C when in contact with Al [194].

The interaction of Al and a-Si:H(n) is sufficiently strong that, even at 150 °C, the 5- and 10-nm-thick samples were unable to maintain passivation: they had $iV_{oc}-V_{oc} \geq 137$ mV for every tested annealing temperature. On the other hand, the 20- and 40-nm-thick samples annealed at 150 °C had average $iV_{oc}-V_{oc}$ of 33 and 39 mV, respectively. These losses are nearly acceptable but still higher than desirable, though the ITO/Ag references also had 23 mV loss after annealing at 150 °C, indicating abnormally high systematic voltage losses for this particular batch of samples. All Al samples annealed at 180 °C or higher had $iV_{oc}-V_{oc} \geq 167$ mV. Thus, only the thickest samples (20 and 40 nm) annealed at the lowest tested temperature of 150 °C demonstrated the potential for maintaining quality surface passivation. These conditions simultaneously resulted in ρ_c = 1–10 mΩ·cm^2 and thus exhibit promise for implementation in full devices with low contact fraction.

5.3.3 Solar cells with full-area rear metallization

Figure 5-4(a) shows the V_{oc} of the fabricated cells. As expected, the Al-metallized hole and electron contacts exhibited a wide range of performance based on annealing temperature, with the electron contact varying more dramatically. The origins of this variation will be discussed in greater detail in the subsequent section. The devices with rear a-Si:H(i)/a-Si:H(n)/Al and a-Si:H(i)/a-Si:H(p)/Al contacts annealed at the lowest tested temperatures had V_{oc}s of 717 and 696 mV, respectively. Each of these values was higher than the respective ITO/Ag reference cells, indicating good potential for device performance when passivation is maintained.

The J_{sc} of the cells are shown in Figure 5-4(b). Though the ITO/Ag stack is known to have superior reflectance than Al alone, we observed <1 mA/cm^2 difference in J_{sc} between the best performing Al cells and the ITO/Ag references. We attribute this to the use of planar-rear wafers and front ITO thickness variation. In a separately prepared batch with symmetric random pyramid texture, we measured Al and ITO/Ag to yield integrated J_{sc}s of 37.5 and 40.3 mA/cm^2, respectively, with nearly all losses occurring at longer wavelengths. Minimizing these parasitic absorption losses at the rear Al layer will be essential for the best cell performance; fortunately, inserting a low-refractive-index dielectric film between the a-Si:H layers and rear metal has been shown to effectively reflect infrared light and has been demonstrated in SHJ cells [207, 208].

Figure 5-4(c) and (d) shows the resistivities and *FF* of the cells, respectively. In the TLM structures (which were possible only for the cells with electron contacts at the rear), the contact resistivity was more than an order of magnitude lower for the Al-metallized samples, as predicted in Figure 5-3(a). However, the Al-metallized cell did not exhibit superior series resistivity or *FF*. A significant contributing factor is the line resistance of the front Ag paste, which has a manufacturer's recommended curing temperature of 200 °C. The line resistivity for these cells annealed at 150, 180, and 210 °C were 3.0, 0.85, and 0.6 Ω/cm, respectively. For a 2 cm × 2 cm cell with 8 fingers, each separated by 2/7 cm, increasing line resistivity from 0.6 to 3.0 Ω/cm results in an increase in series resistivity

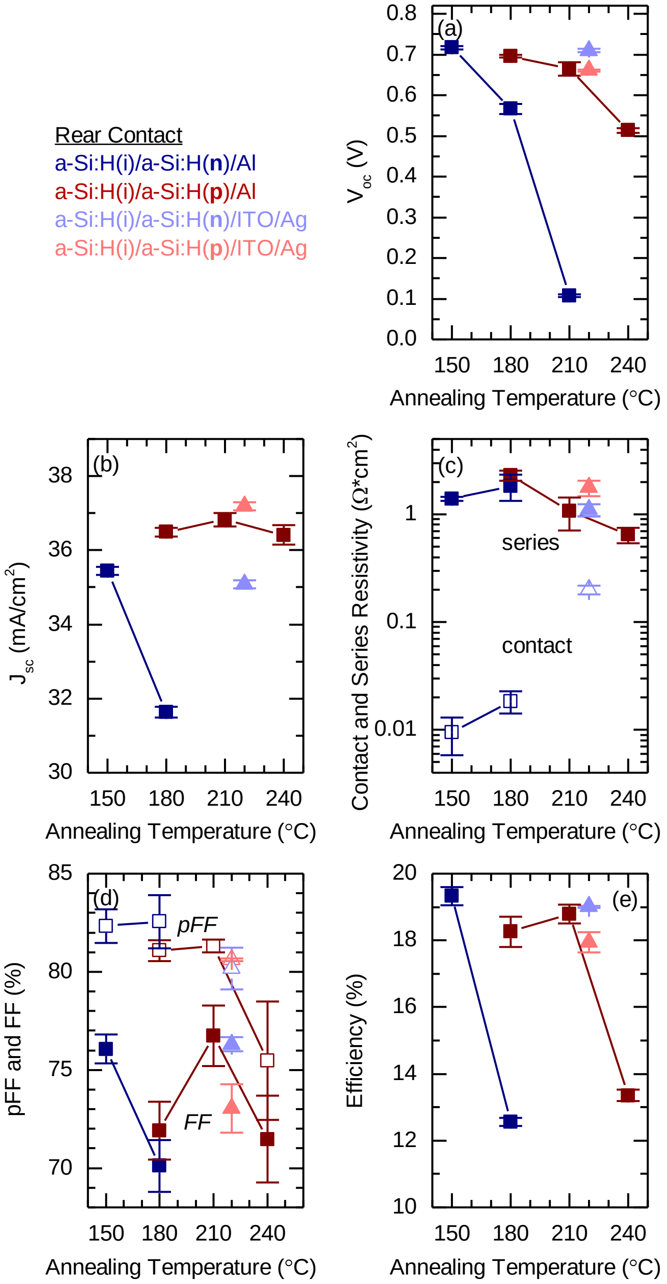


Figure 5-4. (a) V_{oc}, (b) J_{sc}, (c) contact and series resistivity, (d) *pFF* and *FF*, and (e) efficiency of SHJ solar cells with either Al or ITO/Ag metallization to rear n- or p-type a-Si:H layers.

from 0.12 to 0.61 Ω·cm^2, according to the analysis by Meier [209]. Thus, the low annealing temperatures to optimize the Al-metallized contacts must be considered with subsequent processing, and plating, for example, may be more compatible than screen-printed front fingers. The efficiency of the devices is shown in Figure 5-4(e). Overall, the devices exhibited the expected behavior based on the electrical test structures, and demonstrated performance on par with the ITO/Ag reference devices. The best performing cell with a-Si:H(i)/a-Si:H(n)/Al rear contact had V_{oc} = 722 mV while simultaneously achieving ρ_c = 9.4 mΩ·cm^2.

5.3.4 STEM and EDXS

Since these test structures and full devices exhibited an extremely wide range of performance, we examined the contacts using STEM and EDXS or EELS. We begin with the a-Si:H(i)/a-Si:H(n)/Al electron contacts. Figure 5-5(a) shows the contact annealed at 150 ºC; it exhibits a smooth a-Si:H(n)/Al interface with seemingly no interdiffusion. This sample was extracted from the best Al-metallized cell, which had high V_{oc} and low ρ_c.

Figure 5-5(b) shows significant diffusion of Al into the underlying a-Si:H(i)/a-Si:H(n) stack at 180 °C. The interdiffusion process in Al-induced crystallization and layer exchange initiates at the a-Si:H/Al interface due to mobile free electrons in Al screening Si-Si covalent bonds, creating approximately two monolayers of highly mobile, or free, Si atoms [210]. Similarly, bond screening from Al is believed to weaken Si-H bonds in a-Si:H(i)/Al stacks, causing hydrogen effusion at temperatures below 150 °C [211]. Thus, sufficiently thick Al adjacent to Si-Si and Si-H bonds increases the density of free Si atoms and Si dangling bonds, which, combined, facilitate extensive atomic rearrangement. The mobile Si atoms at or near the a-Si:H/Al interface typically find an energetically favorable position by wetting the grain boundaries of the polycrystalline Al film [210]. However, as Al enters the a-Si:H film at rapid rates and high concentrations, the free Si atoms deeper in the a-

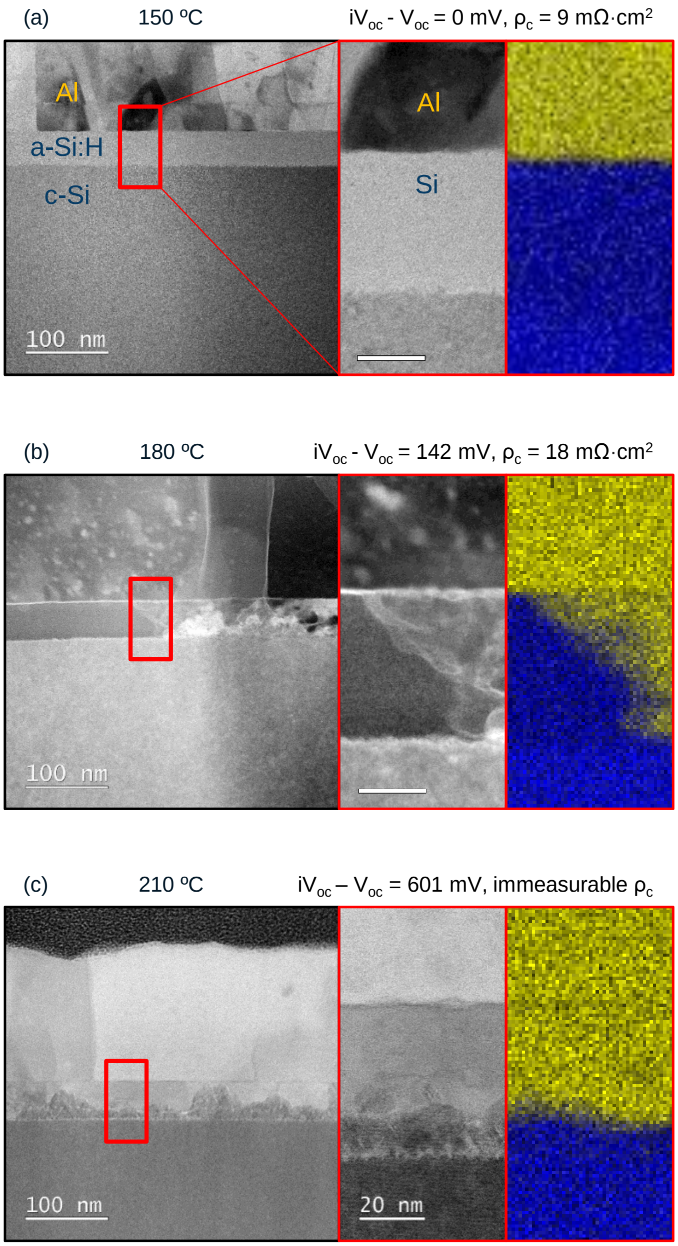


Figure 5-5. Low-magnification STEM cross-section, high-magnification STEM cross-section, and complementary EDXS or EELS map for a-Si:H(i)/a-Si:H(n)/Al contacts annealed at (a) 150 °C, (b) 180 °C, and (c) 210 °C. Also shown are the difference between the cell V_{oc} and the iV_{oc} of the initially passivated wafer, and the contact resistance from TLM.

Si:H film likely lose access to these grain boundaries and a meta-stable Al-Si mixed phase forms. This composition is unable to provide the same degree of c-Si surface passivation due to hydrogen loss, recombination losses in the Al-rich contact, and, likely, Al reaching the c-Si wafer in some areas. Together, these mechanisms are responsible for the low V_{oc} (563 mV) of this cell. This semi-metallic structure is, however, highly conductive, as observed in the TLM test structures and in comparable contact structures from prior work [204, 212]. During annealing, as Al enters the a-Si:H film in high concentrations and disrupts the a-Si:H bonding, we expect there to be a significant amount of free Si atoms. When these atoms exceed a critical thickness, based on the surrounding interfaces, crystallization becomes an energetically favorable process [210].

Figure 5-5(c), of the cell annealed at 210 °C, shows Si crystallization commencing at the c-Si wafer surface below a predominantly Al-rich layer. The directionality of the crystallized lattice within the former a-Si:H layer matches that of the substrate, indicating that the c-Si substrate has provided an energetically favorable site for epitaxial nucleation. This cell had a V_{oc} of 108 mV and the corresponding TLM structures had immeasurable contact resistance, which is evidence that, during the crystallization process, Al was incorporated into the Si lattice as a p-type dopant, as similarly observed by Haque *et al.* [199]. Given the high concentration of Al diffusion into the a-Si:H(i)/a-Si:H(n) stack and the Si crystallization far below the amorphous crystallization temperature, we hypothesize that covalent bond screening and the resultant hydrogen effusion and Si dissociation are major factors induced by Al in these electron contacts. Given the relatively low concentration of weakly bound higher hydrides in a-Si:H(i)/a-Si:H(n) stacks, thermally induced hydrogen effusion in the absence of Al bond screening is not expected to be a significant factor, as marginal hydrogen effusion occurs below 210 °C [213, 214].

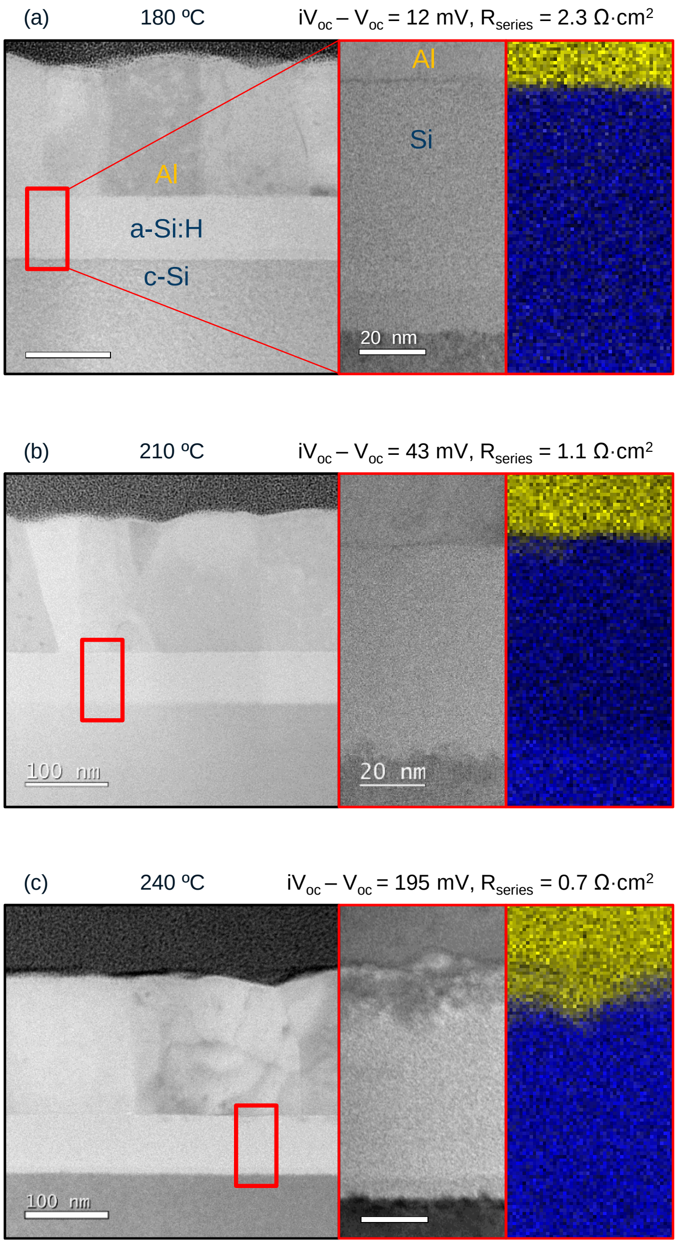


Figure 5-6. Low-magnification STEM cross-section, high-magnification STEM cross-section, and complementary EDXS map for a-Si:H(i)/a-Si:H(p)/Al contacts annealed at (a) 180 °C, (b) 210 °C, and (c) 240 °C. Also shown are the difference between the cell V_{oc} and the iV_{oc} of the initially passivated wafer, and the cell's series resistance.

We turn now to the a-Si:H(i)/a-Si:H(p)/Al hole contacts. In contrast to the a-Si:H(n)/Al interface, the a-Si:H(p)/Al interface annealed at 180 °C appears sharp, with seemingly minimal to no interdiffusion, as shown in Figure 5-6(a). This translated to a 12 mV loss relative to the iV_{oc} of the pre-metallized passivated wafers, and to higher V_{oc} than all ITO/Ag reference cells. We hypothesize that, rather than rapidly dissociating the Si and entering the a-Si:H, as for the a-Si:H(n) layer, Al diffuses at low temperatures in accordance with its ability to enter the a-Si:H(p) film as an active acceptor dopant. Near-UV photoelectron spectroscopy performed by Stang *et al.* indicated a 50 meV downward shift in the Fermi level of an a-Si:H(i)/a-Si:H(p)/Al contact when annealed at 150 °C, which was attributed to Al occupying acceptor positions [189]. Konishi *et al.* performed secondary ion mass spectrometry (SIMS) on c-Si/a-Si:H(i)/a-Si:H(p)/Al structures annealed at 150 and 200 °C for 30 minutes. The results showed no Al in the a-Si:H(i) layer after the 150 °C anneal and a concentration of $5.9 \cdot 10^{18}/\text{cm}^3$ at the c-Si wafer surface after the 200 °C anneal [190].]. In the 180 °C sample here, we do not directly observe Al interaction in STEM or EDXS, which has a detection limit of about 1%, corresponding to a concentration of approximately $4.9 \cdot 10^{20}$ cm^{-3} in a-Si:H [215]. Though, dopant-level concentrations of Al are not detectable, we do expect a modest level of p-type dopant incorporation, resulting in the cell maintaining good performance.

Figure 5-6(b) shows the a-Si:H(i)/a-Si:H(p)/Al contact annealed at 210 °C. We observe Al signal from EDXS only at the very top of the a-Si:H(p) film. In the high-magnification STEM image, we observe visible roughening at the c-Si/a-Si:H(i) interface, though it is not apparent what is causing this. One possibility is that dopant-level concentrations of Al have already been introduced throughout the a-Si:H(p) film (as active dopants) and the Al continues to diffuse through the a-Si:H(i) layer. As we have seen, Al diffuses more rapidly through intrinsic and n-type a-Si:H compared to p-type. Al could be diffusing through the a-Si:H(i) and reaching the wafer in smaller concentrations, causing some perturbation to the passivation (iV_{oc}−V_{oc} = 43 mV).

Heavy Al diffusion into a-Si:H(p) does not occur until 240 °C, as shown in Figure 5-6(c). Given the high concentration of higher hydrides in a-Si:H(i)/a-Si:H(p) stacks, some hydrogen effusion is expected at 210 °C [213, 214], but the effusion rates measured by De Wolf *et al.* show a significant increase between 210 and 240 °C. This is likely a major driver for the higher Al diffusion into the a-Si:H(p) layer at this higher temperature: Hydrogen effusion from the thermal treatment significantly increases the density of dangling bonds, thereby providing more energetically favorable pathways for Al diffusion. Further accelerating this process is the incorporation of Al as an active dopant within the a-Si:H(p) layer, which will drive the Fermi level closer toward the valence band, further increasing the hydrogen effusion rate by reducing the energetic barrier to bond rupture [213]. Thus, once this critical temperature is reached, multiple mechanisms self-propagate and facilitate alloy-level concentrations of Al diffusion into the a-Si:H(p) layer.

Finally, we note that growth-dependent structural properties and long-range disorder may also influence diffusion pathways. Diffusion through microstructural grain boundaries and microvoids has been linked to Al diffusion in prior work [216]. In the a-Si:H(i)/a-Si:H(n) stacks, the Al preferentially diffuses down to the c-Si wafer before moving laterally. On the other hand, Al seems to sweep more uniformly into a-Si:H(p).

5.4 Conclusions

We have explored the properties of SHJ electron and hole contacts with direct Al metallization to a-Si:H(n/p) for a wide range of a-Si:H(n/p) thicknesses and annealing temperatures. Thicker (20–40 nm) a-Si:H layers metallized with Al and annealed at 150 °C (for n-type) and 180 °C (for p-type) preserve the wafer surface passivation and provide lower contact resistance than their ITO/Ag counterparts. Each contact polarity is sensitive to the processing conditions in different ways, and microscopic analysis of the contact stacks revealed that this behavior stems from a combination of hydrogen effusion, Al screening, and Al incorporation into the a-Si:H(n/p) layers.

When these contacts were implemented at the rear of solar cells, J_{sc} and efficiency predictably suffered—relative to ITO/Ag reference cells—due to higher rear parasitic absorption and higher front grid resistivity. However, these losses can be remedied with existing technologies: partial-area dielectric reflectors and low-temperature plating. A significant outstanding challenge for Al metallization to SHJ cells, however, is expanding the processing window that yields excellent contact properties.

Although a-Si:H(i)/a-Si:H(n)/Al and a-Si:H(i)/a-Si:H(p)/Al contacts have different stability challenges with increasing annealing temperature, each type could benefit by buffering the onset of Al diffusion at its interface with the doped a-Si:H. This could be done by tuning the oxidation of the a-Si:H stack before Al deposition. This is a known approach to slow the interdiffusion process by increasing the Al-Si distance, but must be implemented in a way that does not become prohibitively resistive [217]. Another approach is to incorporate Si into the Al sputter target, which may reduce the driving force for Al diffusion into the a-Si:H layers and the strength of the Si-Si and Si-H bond screening compared to pure Al [218]. For the a-Si:H(i)/a-Si:H(n)/Al contact, a phosphine plasma before Al sputtering or deuterium treatment could increase the stability of the a-Si:H(n) layer and inhibit counter-doping [219, 220]. For the a-Si:H(i)/a-Si:H(p)/Al contact, more insight is needed into the Al diffusion mechanism and how this is impacting V_{oc}, but a diborane plasma on the a-Si:H(p) surface before Al metallization may sufficiently impede Al diffusion without compromising contact quality.

CHAPTER 6

CONCLUSION

This thesis first reviewed the state of silicon solar technology in order to establish the context for the contributions presented in the subsequent chapters. While PERC has become the dominant cell technology, future efficiency improvements for PERC are increasingly difficult, which makes capturing energy gains of fielded modules increasingly attractive. Within this broad space, the sub-bandgap reflectance at the rear metal interface is particularly attractive, given the large proportion of solar radiation that is sub-bandgap for silicon modules and the inability of these photons to contribute to productive electrical energy conversion.

Cell reflectance at the rear electrode play a large role in rejecting sub-bandgap light. To be able to quantify this, a methodology to isolate impact of R_{sub} on fielded module operating temperature for standard outdoor test setup was created. This was then used to demonstrate systematic temperature difference in power-generating conditions between PERC and Al-BSF. Further, the temperature improvements of an optimized, dedicated optical dielectric layer was demonstrated: 1.4 °C over Al-BSF and 0.6 °C over PERC for standard meteorological operating conditions. While these demonstrate a pathway to performance improvements, they are limited by parasitic absorption in other regions of the module, especially the module glass and encapsulant.

The strongest cell technology to supersede PERC is TOPCon, as it has close alignment of process sequence but removes the direct metal interface to the silicon absorber, eliminating the limiting recombination losses of PERC. The attractiveness of this cell structure is directly related to how closely compatible it is to workhorse process sequence, which means screen-printing is highly desired. Here, the potential and limitations of a low-temperature, screen-printing compatible Ag metallization process was introduced and characterized. The curing of Ag NPs on poly-Si(n) was shown to maintain high-quality passivation for thin poly-Si(n) films of 40 nm. The primary challenge was identified to be low contact resistivity of poly-Si(n)/Ag when cured in air, which was studied using sputtered Ag contacts. The most likely causes of poor transport after annealing in atmosphere were found to be dewetting due to Ag grain growth and interfacial chemical reactions from atmospheric-containing gases.

The silicon cell technology that represents a revolutionary leap over PERC is SHJ. Historically, SHJ has been limited by high cost, both material and capital investment. A route to reduce the initial cost is replacing scarce Ag and In-containing TCOs on the rear side with a single layer of Al directly on the passivating contacts. This work evaluated the interplay of a-Si:H thickness and post-metallization annealing temperature on contact performance for n- and p-type a-Si:H/Al contacts. Additionally, it identified Ag-free rear contact processes with promising cell properties: V_{oc}/iV_{oc} equal to 1 and ρ_c between 4-50 $m\Omega \cdot cm^2$. These performances were linked to interface interdiffusion of Al and Si, hydrogen effusion, and phase changes during annealing through TEM and elemental mapping.

REFERENCES

[1] *Annual Solar Photovoltaic Module Shipments Report*. Available: https://www.eia.gov/renewable/annual/solar_photo/

[2] United States EIA, "Monthly Energy Review.", 2021. Available: https://www.eia.gov/totalenergy/data/monthly/

[3] United States EIA, "Renewables account for most new U.S. electricity generating capacity in 2021.", 2021. Available: https://www.eia.gov/todayinenergy/detail.php?id=46416

[4] ITRPV, “International Technology Roadmap for Photovoltaics 2020 Results,” 2021.

[5] T. Dullweber and J. Schmidt, "Industrial silicon solar cells applying the passivated emitter and rear cell (PERC) concept—A review," *IEEE J. Photovolt.,* vol. 6, no. 5, pp. 1366-1381, 2016.

[6] ITRPV, “International Technology Roadmap for Photovoltaics 2013 Results,” 2014.

[7] ITRPV, “International Technology Roadmap for Photovoltaics 2014 Results,” 2015.

[8] ITRPV, “International Technology Roadmap for Photovoltaics 2015 Results,” 2016.

[9] ITRPV, “International Technology Roadmap for Photovoltaics 2016 Results,” 2017.

[10] ITRPV, “International Technology Roadmap for Photovoltaics 2017 Results,” 2018.

[11] ITRPV, “International Technology Roadmap for Photovoltaics 2018 Results,” 2019.

[12] ITRPV, “International Technology Roadmap for Photovoltaics 2019 Results,” 2020.

[13] NREL, "Best Research-Cell Efficiency Chart.", 2021. Available: https://www.nrel.gov/pv/cell-efficiency.html

[14] J. Zhao, A. Wang, and M. A. Green, "24.5% Efficiency silicon PERT cells on MCZ substrates and 24· 7% efficiency PERL cells on FZ substrates," *Prog. Photovolt., Res. Appl.,* vol. 7, no. 6, pp. 471-474, 1999.

[15] M. A. Green, "The path to 25% silicon solar cell efficiency: History of silicon cell evolution," *Prog. Photovolt., Res. Appl.,* vol. 17, no. 3, pp. 183-189, 2009.

[16] A. Blakers, "Development of the PERC solar cell," *IEEE J. Photovolt.,* vol. 9, no. 3, pp. 629-635, 2019.

[17] A. Blakers, N. Zin, K. R. McIntosh, and K. Fong, "High efficiency silicon solar cells," *Energy Procedia,* vol. 33, pp. 1-10, 2013.

[18] M. A. Green, "Commercial progress and challenges for photovoltaics," *Nature Energy,* vol. 1, no. 1, pp. 1-4, 2016.

[19] J. Liu, Y. Yao, S. Xiao, and X. Gu, "Review of status developments of high-efficiency crystalline silicon solar cells," *Journal of Physics D: Applied Physics,* vol. 51, no. 12, p. 123001, 2018.

[20] F. Colville. *Heterojunction prepares to replace p-mono PERC as mainstream PV offering from 2023*. Available: https://www.pv-tech.org/heterojunction-prepares-to-replace-p-mono-perc-as-mainstream-pv-offering-from-2023/

[21] V. Shaw. (2021). *The weekend read: Life after PERC*. Available: https://www.pv-magazine.com/2021/05/08/the-weekend-read-life-after-perc/

[22] C. Lin, "SHJ Cell Technology: Review and outlook for cost, price and trends," PV InfoLink2021.

[23] Y. Zhang, L. Wang, D. Chen, M. Kim, and B. Hallam, "Pathway towards 24% efficiency for fully screen-printed passivated emitter and rear contact solar cells," *Journal of Physics D: Applied Physics,* vol. 54, no. 21, p. 214003, 2021.

[24] P. P. Altermatt, Y. Chen, and Z. Feng, "Riding the workhorse of the industry: PERC," *J Photovolt. Int,* vol. 41, pp. 46-54, 2018.

[25] F. Haase *et al.*, "Laser contact openings for local poly-Si-metal contacts enabling 26.1%-efficient POLO-IBC solar cells," *Sol. Energy Mater. Sol. Cells,* vol. 186, pp. 184-193, 2018.

[26] (2014). *Panasonic HIT® Solar Cell Achieves World's Highest Energy Conversion Efficiency of 25.6% at Research Level*. Available: https://news.panasonic.com/global/press/data/2014/04/en140410-4/en140410-4.html

[27] S. Glunz *et al.*, "The irresistible charm of a simple current flow pattern–25% with a solar cell featuring a full-area back contact," in *Proceedings of the 31st European Photovoltaic Solar Energy Conference and Exhibition*, 2015, pp. 259-263.

[28] D. D. Smith, G. Reich, M. Baldrias, M. Reich, N. Boitnott, and G. Bunea, "Silicon solar cells with total area efficiency above 25%," in *2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC)*, 2016, pp. 3351-3355: IEEE.

[29] K. Yamamoto, K. Yoshikawa, H. Uzu, and D. Adachi, "High-efficiency heterojunction crystalline Si solar cells," *Japanese Journal of Applied Physics,* vol. 57, no. 8S3, p. 08RB20, 2018.

[30] A. Richter, J. Benick, F. Feldmann, A. Fell, M. Hermle, and S. W. Glunz, "n-Type Si solar cells with passivating electron contact: Identifying sources for efficiency limitations by wafer thickness and resistivity variation," *Sol. Energy Mater. Sol. Cells,* vol. 173, pp. 96-105, 2017.

[31] T. G. Allen, J. Bullock, X. Yang, A. Javey, and S. De Wolf, "Passivating contacts for crystalline silicon solar cells," *Nature Energy,* vol. 4, no. 11, pp. 914-928, 2019.

[32] T. Niewelt *et al.*, "Reassessment of the intrinsic bulk recombination in crystalline silicon," *Sol. Energy Mater. Sol. Cells,* vol. 235, p. 111467, 2022.

[33] J. Melskens, B. W. van de Loo, B. Macco, L. E. Black, S. Smit, and W. Kessels, "Passivating contacts for crystalline silicon solar cells: From concepts and materials to prospects," *IEEE J. Photovolt.,* vol. 8, no. 2, pp. 373-388, 2018.

[34] M. Hermle, F. Feldmann, M. Bivour, J. C. Goldschmidt, and S. W. Glunz, "Passivating contacts and tandem concepts: Approaches for the highest silicon-based solar cell efficiencies," *Applied Physics Reviews,* vol. 7, no. 2, p. 021305, 2020.

[35] S. K. Chunduri and M. Schmela, "Market Survey Metallization Pastes 2019/20," TaiyangNews2019.

[36] D. Yan *et al.*, "Polysilicon passivated junctions: The next technology for silicon solar cells?," *Joule,* 2021.

[37] A. Onno, C. Chen, P. Koswatta, M. Boccard, and Z. C. Holman, "Passivation, conductivity, and selectivity in solar cell contacts: Concepts and simulations based on a unified partial-resistances framework," *Journal of Applied Physics,* vol. 126, no. 18, p. 183103, 2019.

[38] U. Würfel, A. Cuevas, and P. Würfel, "Charge carrier separation in solar cells," *IEEE J. Photovolt.*, vol. 5, no. 1, pp. 461-469, 2014.

[39] A. Cuevas *et al.*, "Carrier population control and surface passivation in solar cells," *Solar Energy Materials & Solar Cells,* vol. 184, pp. 38-47, 2018.

[40] R. S. Bonilla, B. Hoex, P. Hamer, and P. R. Wilshaw, "Dielectric surface passivation for silicon solar cells: A review," *physica status solidi,* vol. 214, no. 7, p. 1700293, 2017.

[41] W. Shockley and W. Read Jr, "Statistics of the recombinations of holes and electrons," *Physical review,* vol. 87, no. 5, p. 835, 1952.

[42] A. Cuevas, "The effect of emitter recombination on the effective lifetime of silicon wafers," *Sol. Energy Mater. Sol. Cells*, vol. 57, no. 3, pp. 277-290, 1999.

[43] J. Bullock *et al.*, "Efficient silicon solar cells with dopant-free asymmetric heterocontacts," *Nature Energy,* vol. 1, no. 3, pp. 1-7, 2016.

[44] P. Würfel and U. Würfel, *Physics of solar cells: from basic principles to advanced concepts*. John Wiley & Sons, 2016.

[45] A. Cuevas, "The recombination parameter J0," *Energy Procedia*, vol. 55, pp. 53-62, 2014.

[46] D. Kane and R. Swanson, "Measurement of the emitter saturation current by a contactless photoconductivity decay method," in *IEEE 18th Photovoltaic Specialists Conference (PVSC)*, 1985, pp. 578-583.

[47] R. King, R. Sinton, and R. Swanson, "Studies of diffused phosphorus emitters: saturation current, surface recombination velocity, and quantum efficiency," *IEEE Transactions on electron devices,* vol. 37, no. 2, pp. 365-371, 1990.

[48] H. Mäckel and K. Varner, "On the determination of the emitter saturation current density from lifetime measurements of silicon devices," *Prog. Photovolt., Res. Appl.*, vol. 21, no. 5, pp. 850-866, 2013.

[49] A. Blum, J. Swirhun, R. Sinton, and A. Kimmerle, "An updated analysis to the WCT-120 QSSPC measurement system using advanced device physics," in *Proceedings of the 28th European Photovoltaic Solar Energy Conference and Exhibition*, 2013, pp. 1521-1523.

[50] K. R. McIntosh and L. E. Black, "On effective surface recombination parameters," *Journal of Applied Physics,* vol. 116, no. 1, p. 014503, 2014.

[51] J. Cui, Y. Wan, Y. Cui, Y. Chen, P. Verlinden, and A. Cuevas, "Highly effective electronic passivation of silicon surfaces by atomic layer deposited hafnium oxide," *Applied Physics Letters*, vol. 110, no. 2, p. 021602, 2017.

[52] Y. Wan, D. Yan, J. Bullock, X. Zhang, and A. Cuevas, "Passivation of c-Si surfaces by sub-nm amorphous silicon capped with silicon nitride," *Applied Physics Letters*, vol. 107, no. 23, p. 231606, 2015.

[53] D. Yan, S. P. Phang, Y. Wan, C. Samundsett, D. Macdonald, and A. Cuevas, "High efficiency n-type silicon solar cells with passivating contacts based on PECVD silicon films doped by phosphorus diffusion," *Sol. Energy Mater. Sol. Cells*, vol. 193, pp. 80-84, 2019.

[54] J. Deckers, M. Debucquoy, I. Gordon, R. Mertens, and J. Poortmans, "Avoiding parasitic current flow through point contacts in test structures for QSSPC contact recombination current measurements," *IEEE J. Photovolt.*, vol. 5, no. 1, pp. 276-281, 2014.

[55] J. Deckers *et al.*, "Injection dependent emitter saturation current density measurement under metallized areas using photoconductance decay," 2013, pp. 806-810.

[56] J. Bullock, A. Cuevas, D. Yan, B. Demaurex, A. Hessler-Wyser, and S. De Wolf, "Amorphous silicon enhanced metal-insulator-semiconductor contacts for silicon solar cells," *Journal of Applied Physics*, vol. 116, no. 16, p. 163706, 2014.

[57] R. W. Dumbrell, "Applications of dynamic photoluminescence measurements to metallised silicon solar cells," 2019.

[58] R. Dumbrell, M. K. Juhl, T. Trupke, and Z. Hameiri, "Extracting metal contact recombination parameters from effective lifetime data," *IEEE J. Photovolt.*, vol. 8, no. 6, pp. 1413-1420, 2018.

[59] R. T. Ross, "Some thermodynamics of photochemical systems," *The Journal of Chemical Physics*, vol. 46, no. 12, pp. 4590-4593, 1967.

[60] O. D. Miller, E. Yablonovitch, and S. R. Kurtz, "Strong internal and external luminescence as solar cells approach the Shockley–Queisser limit," *IEEE J. Photovolt.*, vol. 2, no. 3, pp. 303-311, 2012.

[61] D. Inns, "Understanding metal induced recombination losses in silicon solar cells with screen printed silver contacts," *Energy Procedia*, vol. 98, pp. 23-29, 2016.

[62] L. J. Koduvelikulathu, V. D. Mihailetchi, S. Olibet, D. Rudolph, E. Cabrera, and R. Kopecek, "Two-dimensional modeling of the metallization-induced

recombination losses of screen-printed solar cells," *IEEE J. Photovolt.,* vol. 5, no. 1, pp. 159-165, 2014.

[63] M. Glatthaar *et al.*, "Evaluating luminescence based voltage images of silicon solar cells," *Journal of Applied Physics*, vol. 108, no. 1, p. 014501, 2010.

[64] V. Shanmugam, T. Mueller, A. G. Aberle, and J. Wong, "Determination of metal contact recombination parameters for silicon wafer solar cells by photoluminescence imaging," *Solar Energy,* vol. 118, pp. 20-27, 2015.

[65] D. Herrmann, S. Lohmüller, H. Höffler, A. Fell, A. A. Brand, and A. Wolf, "Numerical simulations of photoluminescence for the precise determination of emitter contact recombination parameters," *IEEE J. Photovolt.,* vol. 9, no. 6, pp. 1759-1767, 2019.

[66] D. K. Schroder, *Semiconductor material and device characterization*. John Wiley & Sons, 2015.

[67] N. Folchert and R. Brendel, "Extended Cox & Strack analysis for the contact resistance of planar samples with carrier-selective junctions on both sides," *Sol. Energy Mater. Sol. Cells*, vol. 231, p. 111304, 2021.

[68] R. T. Tung, "The physics and chemistry of the Schottky barrier height," *Applied Physics Reviews*, vol. 1, no. 1, p. 011304, 2014.

[69] S. Grover, S. Sahu, P. Zhang, K. O. Davis, and S. K. Kurinec, "Standardization of Specific Contact Resistivity Measurements using Transmission Line Model (TLM)," in *2020 IEEE 33rd International Conference on Microelectronic Test Structures (ICMTS)*, 2020, pp. 1-6: IEEE.

[70] J. D. Fields *et al.*, "The formation mechanism for printed silver-contacts for silicon solar cells," *Nature communications*, vol. 7, no. 1, pp. 1-7, 2016.

[71] T. Dullweber *et al.*, "Evolutionary PERC+ solar cell efficiency projection towards 24% evaluating shadow-mask-deposited poly-Si fingers below the Ag front contact as next improvement step," vol. 212, p. 110586, 2020.

[72] P. Padhamnath *et al.*, "Development of thin polysilicon layers for application in monoPoly™ cells with screen-printed and fired metallization," *Sol. Energy Mater. Sol. Cells*, vol. 207, 2020, Art. no. 110358.

[73] P. Padhamnath, N. Nampalli, A. Khanna, B. Nagarajan, A. G. Aberle, and S. J. S. E. Duttagupta, "Progress with passivation and screen-printed metallization of Boron-doped monoPoly™ layers," vol. 231, pp. 8-26, 2022.

[74] S. Reiter *et al.*, "Parasitic absorption in polycrystalline Si-layers for carrier-selective front junctions," *Energy Procedia,* vol. 92, pp. 199-204, 2016.

[75] F. Feldmann, M. Nicolai, R. Müller, C. Reichel, and M. Hermle, "Optical and electrical characterization of poly-Si/SiOx contacts and their implications on solar cell design," *Energy Procedia,* vol. 124, pp. 31-37, 2017.

[76] S. De Wolf, A. Descoeudres, Z. C. Holman, and C. Ballif, "High-efficiency silicon heterojunction solar cells: A review," *Green,* vol. 2, no. 1, pp. 7-24, 2012.

[77] B. Demaurex, S. De Wolf, A. Descoeudres, Z. Charles Holman, and C. Ballif, "Damage at hydrogenated amorphous/crystalline silicon interfaces by indium tin oxide overlayer sputtering," *Applied Physics Letters,* vol. 101, no. 17, p. 171604, 2012.

[78] D. Lachenal *et al.*, "Heterojunction and passivated contacts: a simple method to extract both n/tco and p/tco contacts resistivity," vol. 92, pp. 932-938, 2016.

[79] Y. Zhang, M. Kim, L. Wang, P. Verlinden, and B. Hallam, "Design considerations for multi-terawatt scale manufacturing of existing and future photovoltaic technologies: challenges and opportunities related to silver, indium and bismuth consumption," *Energy Environ. Sci.,* vol. 14, no. 11, pp. 5587-5610, 2021.

[80] P. Singh and N. Ravindra, "Temperature dependence of solar cell performance—an analysis," *Sol. Energy Mater. Sol. Cells,* vol. 101, pp. 36-45, 2012.

[81] O. Dupré, R. Vaillon, and M. A. Green, "Physics of the temperature coefficients of solar cells," *Sol. Energy Mater. Sol. Cells,* vol. 140, pp. 92-100, 2015.

[82] A. Ndiaye, A. Charki, A. Kobi, C. M. Kébé, P. A. Ndiaye, and V. Sambou, "Degradations of silicon photovoltaic modules: A literature review," *Solar Energy,* vol. 96, pp. 140-151, Oct. 2013.

[83] S. Kurtz *et al.*, "Evaluation of high-temperature exposure of photovoltaic modules," *Prog. Photovolt., Res. Appl.,* vol. 19, pp. 954-965, 2011.

[84] V. Sharma and S. Chandel, "Performance and degradation analysis for long term reliability of solar photovoltaic systems: A review," *Renewable and Sustainable Energy Reviews,* vol. 27, pp. 753-767, 2013.

[85] N. Bosco, T. J. Silverman, and S. Kurtz, "Climate specific thermomechanical fatigue of flat plate photovoltaic module solder joints," *Microelectronics Reliability,* vol. 62, pp. 124-129, 2016.

[86] H. Gopalakrishna, A. Sinha, K. Dolia, D. Jordan, and G. Tamizhmani, "Nondestructive Characterization and Accelerated UV Testing of Browned Field-Aged PV Modules," *IEEE J. Photovolt.*, vol. 9, no. 6, pp. 1733-1740, Nov. 2019.

[87] D. C. Jordan and S. R. Kurtz, "Photovoltaic degradation rates—an analytical review," *Progress in Photovoltaics: Research and Applications*, vol. 21, no. 1, pp. 12-29, 2013.

[88] IEC 61215-2, Terrestrial photovoltaic (PV) modules - Design qualification and type approval - Part 2: Test procedures, 2016.

[89] IEC 61853-2, Photovoltaic (PV) module performance testing and energy rating – Part 2: Spectral responsivity, incidence angle and module operating temperature measurements, 2016.

[90] D. Faiman, "Assessing the outdoor operating temperature of photovoltaic modules," *Prog. Photovolt.: Res. Appl.*, vol. 16, no. 4, pp. 307-315, 2008.

[91] J.-M. Servant, "Calculation of the cell temperature for photovoltaic modules from climatic data," in *Intersol Eighty Five*, 1986, pp. 1640-1643: Elsevier.

[92] D. L. King, J. A. Kratochvil, and W. E. Boyson, "Photovoltaic Array Performance Model," *Sandia National Laboratories*, pp. SAND2004-3535, 2004.

[93] I. Santiago, D. Trillo-Montero, I. Moreno-Garcia, V. Pallarés-López, and J. Luna-Rodríguez, "Modeling of photovoltaic cell temperature losses: A review and a practice case in South Spain," *Renewable and Sustainable Energy Reviews*, vol. 90, pp. 70-89, 2018.

[94] E. Skoplaki and J. Palyvos, "Operating temperature of photovoltaic modules: A survey of pertinent correlations," *Renewable Energy*, vol. 34, no. 1, pp. 23-29, 2009.

[95] M. Mattei, G. Notton, C. Cristofari, M. Muselli, and P. Poggi, "Calculation of the polycrystalline PV module temperature using a simple method of energy balance," *Renewable Energy*, vol. 31, no. 4, pp. 553-567, 2006.

[96] M. Akhsassi *et al.*, "Experimental investigation and modeling of the thermal behavior of a solar PV module," *Sol. Energy Mater. Sol. Cells*, vol. 180, pp. 271-279, 2018.

[97] J. Palyvos, "A survey of wind convection coefficient correlations for building envelope energy systems' modeling," *Appl. Thermal Eng.*, vol. 28, no. 8-9, pp. 801-808, 2008.

[98] H. Schulte-Huxel, T. J. Silverman, M. G. Deceglie, D. J. Friedman, and A. C. Tamboli, "Energy yield analysis of multiterminal Si-based tandem solar cells," *IEEE J. Photovolt.*, vol. 8, no. 5, pp. 1376-1383, Jul. 2018.

[99] J. A. Duffie, W. A. Beckman, and N. Blair, *Solar engineering of thermal processes, photovoltaics and wind*. John Wiley & Sons, 2020.

[100] T. J. Silverman *et al.*, "Reducing operating temperature in photovoltaic modules," *IEEE J. Photovolt.*, vol. 8, no. 2, pp. 532-540, Mar. 2018.

[101] R. Vaillon, O. Dupré, R. B. Cal, and M. Calaf, "Pathways for mitigating thermal losses in solar photovoltaics," *Sci. Rep.*, vol. 8, no. 1, 2018, Art. no. 13163.

[102] I. M. Slauch, M. G. Deceglie, T. J. Silverman, and V. E. Ferry, "Spectrally selective mirrors with combined optical and thermal benefit for photovoltaic module thermal management," *ACS Photonics*, vol. 5, no. 4, pp. 1528-1538, 2018.

[103] I. M. Slauch, M. G. Deceglie, T. J. Silverman, and V. E. Ferry, "Two-layer anti-reflection coatings with optimized sub-bandgap reflection for solar modules," in *New Concepts in Solar and Thermal Radiation Conversion and Reliability*, Bellingham, WA, USA, 2018, vol. 10759, pp. 133-140: International Society for Optics and Photonics.

[104] B. Zhao, M. Hu, X. Ao, Q. Xuan, and G. Pei, "Spectrally selective approaches for passive cooling of solar cells: A review," *Applied Energy*, vol. 262, p. 114548, 2020.

[105] I. M. Slauch, M. G. Deceglie, T. J. Silverman, and V. E. Ferry, "Outdoor Testing of c-Si Photovoltaic Modules with Spectrally-Selective Mirrors for Operating Temperature Reduction," in *2019 IEEE 46th Photovoltaic Specialists Conference (PVSC)*, 2019, pp. 0112-0117: IEEE.

[106] E. Skoplaki and J. A. Palyvos, "On the temperature dependence of photovoltaic module electrical performance: A review of efficiency/power correlations," *Solar Energy*, vol. 83, no. 5, pp. 614-624, 2009.

[107] Q Cells, Available at: <https://www.q-cells.com/dam/jcr:f391e618-7f78-4d84-a071-d59b76897025/Hanwha_Q_CELLS_Data_sheet_QPOWER_L-G5_315-335_Global_2017-08_Rev02_EN.pdf> (Accessed 17 June 2020).

[108] JA Solar, Available at: <https://www.jasolar.com/uploadfile/2018/0807/20180807045422860.pdf> (Accessed 17 June 2020).

[109] Trina Solar, Available at: <https://static.trinasolar.com/sites/default/files/N_Type_i-Topcon_NEG16MC.20%28II%29_EN_2019_APME_A_web_0.pdf> (Accessed 17 June 2020).

[110] J. L. Bryan *et al.*, "Inserting a Low-Refractive-Index Dielectric Rear Reflector into PERC Cells: Challenges and Opportunities," in *IEEE 46th Photovoltaic Specialists Conference (PVSC),* 2019, pp. 0648-0652.

[111] R. Dubey *et al.*, "Performance degradation in field-aged crystalline silicon PV modules in different Indian climatic conditions," in *Proc. 40th IEEE Photovolt. Specialists Conf.*, Denver, CO, USA, 2014, pp. 3182-3187.

[112] J. Y. Ye, T. Reindl, A. G. Aberle, and T. M. Walsh, "Performance degradation of various PV module technologies in tropical Singapore," *IEEE J. Photovolt.*, vol. 4, no. 5, pp. 1288-1294, Sep. 2014.

[113] I. Haedrich, D. C. Jordan, and M. Ernst, "Methodology to predict annual yield losses and gains caused by solar module design and materials under field exposure," *Sol. Energy Mater. Sol. Cells,* vol. 202, Nov. 2019, Art. no. 110069.

[114] N. Strevel, L. Trippel, and M. Gloeckler, "Performance characterization and superior energy yield of First Solar PV power plants in high-temperature conditions," *Photovolt. Int.,* vol. 17, pp. 148-154, 2012.

[115] J. Haschke *et al.*, "The impact of silicon solar cell architecture and cell interconnection on energy yield in hot & sunny climates," vol. 10, no. 5, pp. 1196-1206, 2017.

[116] A. Anand, A. Shukla, H. Panchal, and A. Sharma, "Thermal regulation of photovoltaic system for enhanced power production: A review," *J. of Energy Storage,* vol. 35, p. 102236, Mar. 2021.

[117] O. Dupré, R. Vaillon, and M. A. Green, "A full thermal model for photovoltaic devices," *Solar Energy,* vol. 140, pp. 73-82, Dec. 2016.

[118] L. C. Andreani, A. Bozzola, P. Kowalczewski, M. Liscidini, and L. Redorici, "Silicon solar cells: toward the efficiency limits," *Advances in Physics: X,* vol. 4, no. 1, 2019, Art. no. 1548305.

[119] I. M. Slauch, M. G. Deceglie, T. J. Silverman, and V. E. Ferry, "Spectrally selective mirrors with combined optical and thermal benefit for photovoltaic module thermal management," *ACS Photonics,* vol. 5, no. 4, pp. 1528-1538, Mar. 2018.

[120] G. Perrakis, A. C. Tasolamprou, G. Kenanakis, E. N. Economou, S. Tzortzakis, and M. Kafesaki, "Passive radiative cooling and other photonic approaches for the temperature control of photovoltaics: a comparative study for crystalline silicon-based architectures," *Opt. Express*, vol. 28, no. 13, pp. 18548-18565, 2020.

[121] I. M. Slauch, M. G. Deceglie, T. J. Silverman, and V. E. Ferry, "Model for characterization and optimization of spectrally selective structures to reduce the operating temperature and improve the energy yield of photovoltaic modules," *ACS Appl. Energy Mater.*, vol. 2, no. 5, pp. 3614-3623, 2019.

[122] I. M. Slauch, M. G. Deceglie, T. J. Silverman, and V. E. Ferry, "Optical approaches for passive thermal management in c-Si photovoltaic modules," *Cell Reports Phys. Sci.*, vol. 2, no. 5, p. 100430, 2021.

[123] Z. C. Holman, A. Descoeudres, S. De Wolf, and C. Ballif, "Record infrared internal quantum efficiency in silicon heterojunction solar cells with dielectric/metal rear reflectors," *IEEE J. Photovolt.*, vol. 3, no. 4, pp. 1243-1249, Oct. 2013.

[124] Z. C. Holman, S. De Wolf, and C. Ballif, "Improving metal reflectors by suppressing surface plasmon polaritons: a priori calculation of the internal reflectance of a solar cell," *Light: Sci. Appl.*, vol. 2, no. 10, p. e106, 2013.

[125] Z. C. Holman *et al.*, "Parasitic absorption in the rear reflector of a silicon solar cell: Simulation and measurement of the sub-bandgap reflectance for common dielectric/metal reflectors," *Sol. Energy Mater. Sol. Cells*, vol. 120, pp. 426-430, Jan. 2014.

[126] I. Subedi, T. J. Silverman, M. G. Deceglie, and N. J. Podraza, "Al+ Si interface optical properties obtained in the Si solar cell configuration," *Phys. Status Solidi A, Appl. Mater. Sci.*, vol. 214, no. 12, 2017, Art. no. 1700480.

[127] I. Subedi, T. J. Silverman, M. G. Deceglie, and N. J. Podraza, "PERC silicon PV infrared to ultraviolet optical model," *Sol. Energy Mater. Sol. Cells*, vol. 215, Sep. 2020, Art. no. 110655.

[128] M. R. Vogt *et al.*, "Reduced module operating temperature and increased yield of modules with PERC instead of Al-BSF solar cells," *IEEE J. Photovolt.*, vol. 7, no. 1, pp. 44-50, Nov. 2016.

[129] J. L. Bryan, T. J. Silverman, M. G. Deceglie, and Z. C. Holman, "Thermal model to quantify the impact of sub-bandgap reflectance on operating temperature of fielded PV modules," *Solar Energy*, vol. 220, pp. 246-250, May 2021.

[130] P. Firth and Z. C. Holman, "Aerosol Impaction-Driven Assembly System for the Production of Uniform Nanoparticle Thin Films with Independently Tunable Thickness and Porosity," *ACS Appl. Nano Mater.*, vol. 1, no. 8, pp. 4351-4357, 2018.

[131] M. Boccard *et al.*, "Low-refractive-index nanoparticle interlayers to reduce parasitic absorption in metallic rear reflectors of solar cells," *phys. status solidi (a),* vol. 214, no. 10, p. 1700179, 2017.

[132] K. Emery, D. Dunlavy, H. Field, and T. Moriarty, "Photovoltaic spectral responsivity measurements," National Renewable Energy Lab., Golden, CO (United States)1998.

[133] B. Marion, S. Rummel, and A. Anderberg, "Current–voltage curve translation by bilinear interpolation," *Prog. Photovolt., Res. Appl.,* vol. 12, no. 8, pp. 593-607, Nov. 2004.

[134] Y. Tsuno, Y. Hishikawa, and K. Kurokawa, "Modeling of the I–V curves of the PV modules using linear interpolation/extrapolation," *Sol. Energy Mater. Sol. Cells,* vol. 93, no. 6-7, pp. 1070-1073, Jun. 2009.

[135] R. Peibst *et al.*, "For none, one, or two polarities—How do POLO junctions fit best into industrial Si solar cells?," *Prog. Photovolt.: Res. Appl.,* vol. 28, no. 6, pp. 503-516, 2020.

[136] M. Stodolny *et al.*, "PolySi Based Passivating Contacts Enabling Industrial Silicon Solar Cell Efficiencies up to 24%," in *2019 IEEE 46th Photovoltaic Specialists Conference (PVSC)*, 2019, pp. 1456-1459: IEEE.

[137] A. Chaudhary, J. Hoß, J. Lossen, R. van Swaaij, and M. Zeman, "Screen printed Ag contacts for n-type polysilicon passivated contacts," in *AIP Conference Proceedings*, 2019, vol. 2147, no. 1, p. 040002: AIP Publishing LLC.

[138] A. Chaudhary *et al.*, "Influence of Polysilicon Thickness on Properties of Screen-Printed Silver Paste Metallized Silicon Oxide/Polysilicon Passivated Contacts," *Physica status solidi*, p. 2100243, 2021.

[139] Radovan Kopecek, a. Jan Hoß, and J. Lossen, "TOPCon technology: What exactly is it and how mature is it in production?," International Solar Energy Research Center (ISC) Konstanz e.V., Germany 2020.

[140] D. L. Young *et al.*, "Reactive ion etched, self-aligned, selective area poly-Si/SiO2 passivated contacts," *Sol. Energy Mater. Sol. Cells*, vol. 217, p. 110621, 2020.

[141] B. Grübel *et al.*, "Plated Ni/Cu/Ag for TOPCon solar cell metallization," in *36th European Photovoltaic Solar Energy Conference*, 2019, pp. 1-5.

[142] V. Arya *et al.*, "Laser Ablation and Ni/Cu Plating Approach for Tunnel Oxide Passivated Contacts Solar Cells with Variate Polysilicon Layer Thickness: Gains and Possibilities in Comparison to Screen Printing," *physica status solidi,* p. 2000474, 2020.

[143] A. B. Morales-Vilches *et al.*, "ZnO: Al/a-SiOx front contact for polycrystalline-silicon-on-oxide (POLO) solar cells," in *AIP Conference Proceedings*, 2018, vol. 1999, no. 1, p. 040016: AIP Publishing LLC.

[144] T. F. Wietler *et al.*, "High temperature annealing of ZnO: Al on passivating POLO junctions: Impact on transparency, conductivity, junction passivation, and interface stability," *IEEE J. Photovolt.,* vol. 9, no. 1, pp. 89-96, 2018.

[145] E. Bruhat, T. Desrues, D. Blanc-Pélissier, B. Martel, R. Cabal, and S. Dubois, "TCO contacts on poly-Si layers: High and low temperature approaches to maintain passivation and contact properties," in *AIP Conference Proceedings*, 2019, vol. 2147, no. 1, p. 040001: AIP Publishing LLC.

[146] L. Tutsch *et al.*, "Implementing transparent conducting oxides by DC sputtering on ultrathin SiOx/poly-Si passivating contacts," *Sol. Energy Mater. Sol. Cells,* vol. 200, p. 109960, 2019.

[147] C. Han *et al.*, "Realizing the Potential of RF-Sputtered Hydrogenated Fluorine-Doped Indium Oxide as an Electrode Material for Ultrathin SiO x/Poly-Si Passivating Contacts," *ACS Appl. Energy Mater.*, vol. 3, no. 9, pp. 8606-8618, 2020.

[148] A. Khanna *et al.*, "Screen printed metallisation for silicon heterojunction solar cells," in *Proc. 28th Eur. Photovoltaic Solar Energy Conf. Exhib*, 2013, pp. 1336-1339.

[149] J.-S. Chiu, Y.-M. Zhao, S. Zhang, and D.-S. Wuu, "The role of laser ablated backside contact pattern in efficiency improvement of mono crystalline silicon PERC solar cells," *Solar Energy,* vol. 196, pp. 462-467, 2020.

[150] J. Haschke, G. Christmann, C. Messmer, M. Bivour, M. Boccard, and C. Ballif, "Lateral transport in silicon solar cells," *Journal of Applied Physics,* vol. 127, no. 11, p. 114501, 2020.

[151] J. L. Bryan, D. Young, P. Stradins, and Z. C. Holman, "Investigation of the Interactions Between Low-Temperature Ag Paste Components and SiO2/Poly-Si(n) Contacts and the Impact on Contact Properties," in *SiliconPV*, 2021.

[152] G. Vandevenne *et al.*, "A study on the thermal sintering process of silver nanoparticle inkjet inks to achieve smooth and highly conducting silver layers," *physica status solidi*, vol. 213, no. 6, pp. 1403-1409, 2016.

[153] J. F. Mousumi, T. Li, G. Kulkarni, A. Kar, R. Kumar, and K. O. Davis, "Localized Laser Printing and Sintering of Silver Nanoparticles for Silicon Solar Cell Metallization," in *2021 IEEE 48th Photovoltaic Specialists Conference (PVSC)*, 2021, pp. 2544-2546: IEEE.

[154] M. Hayes, B. Martel, S. Dubois, A. Morisset, and O. Palais, "Study of non fire-through metallization processes of boron-doped polysilicon passivated contacts for high efficiency silicon solar cells," in *AIP Conference Proceedings*, 2019, vol. 2147, no. 1, p. 040006: AIP Publishing LLC.

[155] Y. Tao *et al.*, "Large area tunnel oxide passivated rear contact n-type Si solar cells with 21.2% efficiency," *Prog. Photovolt.: Res. Appl.*, vol. 24, no. 6, pp. 830-835, 2016.

[156] F. Feldmann, C. Reichel, R. Müller, and M. Hermle, "The application of poly-Si/SiOx contacts as passivated top/rear contacts in Si solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 159, pp. 265-271, 2017.

[157] www.novacentrix.com, "Metalon® JS-B40G."

[158] G. Yeung *et al.*, "Robust passivation of CdSeTe based solar cells using reactively sputtered magnesium zinc oxide," *sol. Energy Mater. Sol. Cells*, vol. 233, p. 111388, 2021.

[159] Y. Zhao, X.-H. Zhao, and Y.-H. Zhang, "Radiative recombination dominated n-type monocrystalline CdTe/MgCdTe double-heterostructures," in *2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC)*, 2016, pp. 0545-0548: IEEE.

[160] J. R. Greer and R. A. Street, "Thermal cure effects on electrical performance of nanoparticle silver inks," *Acta Materialia*, vol. 55, no. 18, pp. 6345-6349, 2007.

[161] P. A. Hanlon, "Optimization and Characterization of an Inkjet Process for Printed Electronics," Ohio University, 2018.

[162] S. Mypati, S. R. Dhanushkodi, M. McLaren, A. Docoslis, B. A. Peppley, and D. P. Barz, "Optimized inkjet-printed silver nanoparticle films: theoretical and experimental investigations," *RSC advances*, vol. 8, no. 35, pp. 19679-19689, 2018.

[163] M. Keikhaie, J. Akbari, M. R. Movahhedi, and H. Alemohammad, "Sintering Characterizations of Ag-nano Film on Silicon Substrate," in *Advanced Materials Research*, 2014, vol. 829, pp. 342-346: Trans Tech Publ.

[164] S. Tepner, N. Wengenmeyr, M. Linse, A. Lorenz, M. Pospischil, and F. Clement, "The Link between Ag-Paste Rheology and Screen-Printed Solar Cell Metallization," *Advanced Materials Technologies*, vol. 5, no. 10, p. 2000654, 2020.

[165] J. Hwang, P. Ho, J. Lewis, and D. Campbell, "Grain boundary diffusion of aluminum in polycrystalline silicon films," *Journal of Applied Physics*, vol. 51, no. 3, pp. 1576-1581, 1980.

[166] P. Holloway, "Grain boundary diffusion of phosphorus in polycrystalline silicon," *Journal of Vacuum Science Technology*, vol. 21, no. 1, pp. 19-22, 1982.

[167] M. Schnabel *et al.*, "Approaches to metallization for poly-Si/SiOx passivated contacts," National Renewable Energy Lab.(NREL), Golden, CO (United States)2019.

[168] D. Adams, T. L. Alford, and J. W. Mayer, *Silver metallization: stability and reliability*. Springer Science & Business Media, 2007.

[169] J. Ye, D. Zuev, and S. J. I. M. R. Makarov, "Dewetting mechanisms and their exploitation for the large-scale fabrication of advanced nanophotonic systems," vol. 64, no. 8, pp. 439-477, 2019.

[170] T. E. Jones, T. C. Rocha, A. Knop-Gericke, C. Stampfl, R. Schlögl, and S. Piccinin, "Adsorbate induced vacancy formation on silver surfaces," *Physical Chemistry Chemical Physics*, vol. 16, no. 19, pp. 9002-9014, 2014.

[171] J.-P. Crocombette, H. de Monestrol, and F. Willaime, "Oxygen and vacancies in silver: A density-functional study in the local density and generalized gradient approximations," *Physical Review B*, vol. 66, no. 2, p. 024114, 2002.

[172] F. Eshaghi and A. Zolanvari, "Effects of high temperature and film thicknesses on the texture evolution in Ag thin films," *The European Physical Journal Plus*, vol. 132, no. 4, pp. 1-14, 2017.

[173] C. V. Thompson, "Solid-state dewetting of thin films," *Annual Review of Materials Research*, vol. 42, pp. 399-434, 2012.

[174] S. Sharma and J. Spitz, "Void growth in thin silver films," *Thin Solid Films*, vol. 67, no. 1, pp. 109-116, 1980.

[175] S. Sharma and J. Spitz, "Hillock formation, hole growth and agglomeration in thin silver films," *Thin Solid Films,* vol. 65, no. 3, pp. 339-350, 1980.

[176] P. Jacquet *et al.*, "Grain growth: The key to understand solid-state dewetting of silver thin films," *Scripta Materialia,* vol. 115, pp. 128-132, 2016.

[177] T. Alford, L. Chen, and K. S. Gadre, "Stability of silver thin films on various underlying layers at elevated temperatures," *Thin Solid Films,* vol. 429, no. 1-2, pp. 248-254, 2003.

[178] T. Graedel, "Corrosion mechanisms for silver exposed to the atmosphere," *Journal of the Electrochemical Society,* vol. 139, no. 7, p. 1963, 1992.

[179] Y. Huo, S.-W. Fu, Y.-L. Chen, and C. C. Lee, "A reaction study of sulfur vapor with silver and silver–indium solid solution as a tarnishing test method," *Journal of Materials Science: Materials in Electronics,* vol. 27, no. 10, pp. 10382-10392, 2016.

[180] F. P. Fehlner and N. F. Mott, "Low-temperature oxidation," *Oxidation of metals,* vol. 2, no. 1, pp. 59-99, 1970.

[181] D. Reenaers, W. Marchal, I. Biesmans, P. Nivelle, J. D'Haen, and W. Deferme, "Layer Morphology and Ink Compatibility of Silver Nanoparticle Inkjet Inks for Near-Infrared Sintering," *Nanomaterials,* vol. 10, no. 5, p. 892, 2020.

[182] J. Haschke, O. Dupré, M. Boccard, and C. Ballif, "Silicon heterojunction solar cells: Recent technological development and practical aspects-from lab to industry," *Solar Energy Materials & Solar Cells,* vol. 187, pp. 140-153, 2018.

[183] A. Louwen, W. Van Sark, R. Schropp, and A. Faaij, "A cost roadmap for silicon heterojunction solar cells," *Solar Energy Materials & Solar Cells,* vol. 147, pp. 295-314, 2016.

[184] E. Bellini. (2019). *Silver demand for PV manufacturing may have peaked in 2019*. Available: https://www.pv-magazine.com/2020/06/04/silver-demand-for-pv-manufacturing-peaked-in-2019/

[185] P. Papet *et al.*, "New cell metallization patterns for heterojunction solar cells interconnected by the Smart Wire Connection Technology," *Energy Procedia,* vol. 67, pp. 203-209, 2015.

[186] A. M. Jeffries, A. Mamidanna, L. Ding, O. J. Hildreth, and M. Bertoni, "Low-Temperature Drop-on-Demand Reactive Silver Inks for Solar Cell Front-Grid Metallization," *IEEE Journal of Photovoltaics,* vol. 7, no. 1, pp. 37-43, 2017.

[187] B. H. Teo *et al.*, "Development of nanoparticle copper screen printing pastes for silicon heterojunction solar cells," *Solar Energy,* vol. 189, pp. 179-185, 2019.

[188] A. Aguilar *et al.*, "Development of Cu plating for silicon heterojunction solar cells," in *IEEE 43rd Photovoltaic Specialists Conference (PVSC)*, 2016, pp. 1972-1975: IEEE.

[189] J. C. Stang *et al.*, "Optimized metallization for interdigitated back contact silicon heterojunction solar cells," *Solar RRL,* vol. 1, no. 3-4, p. 1700021, 2017.

[190] T. Konishi, K. Koyama, K. Ohdaira, and H. Matsumura, "Performance of silicon heterojunction solar cells with various metal-electrodes directly formed on a-Si films without insertion of TCO," in *2018 IEEE 7th World Conference on Photovoltaic Energy Conversion (WCPEC)(A Joint Conference of 45th IEEE PVSC, 28th PVSEC & 34th EU PVSEC)*, 2018, pp. 2036-2038: IEEE.

[191] D. M. Powell, R. Fu, K. Horowitz, P. A. Basore, M. Woodhouse, and T. Buonassisi, "The capital intensity of photovoltaics manufacturing: barrier to scale and opportunity for innovation," *Energy & Environmental Science,* vol. 8, no. 12, pp. 3395-3408, 2015.

[192] S. De Wolf and M. Kondo, "Boron-doped a-Si: H∕ c-Si interface passivation: Degradation mechanism," *J Applied Physics Letters,* vol. 91, no. 11, p. 112109, 2007.

[193] S. Herd, P. Chaudhari, and M. Brodsky, "Metal contact induced crystallization in films of amorphous silicon and germanium," *Journal of Non-Crystalline Solids,* vol. 7, no. 4, pp. 309-327, 1972.

[194] M. Shahidul Haque, H. Naseem, and W. Brown, "Interaction of aluminum with hydrogenated amorphous silicon at low temperatures," *Journal of Applied Physics,* vol. 75, no. 8, pp. 3928-3935, 1994.

[195] D. Van Gestel, I. Gordon, and J. Poortmans, "Aluminum-induced crystallization for thin-film polycrystalline silicon solar cells: Achievements and perspective," *Solar Energy Materials & Solar Cells,* vol. 119, pp. 261-270, 2013.

[196] S. Tutashkonko and N. Usami, "Effects of the Si/Al layer thickness on the continuity, crystalline orientation and the growth kinetics of the poly-Si thin films formed by aluminum-induced crystallization," *Thin Solid Films,* vol. 616, pp. 213-219, 2016.

[197] O. Nast and S. R. Wenham, "Elucidation of the layer exchange mechanism in the formation of polycrystalline silicon by aluminum-induced crystallization," *Journal of Applied Physics,* vol. 88, no. 1, pp. 124-132, 2000.

[198] R. Labie, T. Bearda, O. El Daif, B. O'Sullivan, K. Baert, and I. Gordon, "Resistance and passivation of metal contacts using n-type amorphous Si for Si solar cells," *Journal of Applied Physics,* vol. 115, no. 18, p. 183508, 2014.

[199] M. S. Haque, H. Naseem, and W. Brown, "Aluminum-induced crystallization and counter-doping of phosphorous-doped hydrogenated amorphous silicon at low temperatures," *Journal of Applied Physics,* vol. 79, no. 10, pp. 7529-7536, 1996.

[200] J. Bullock, A. Cuevas, T. Allen, and C. Battaglia, "Molybdenum oxide MoOx: A versatile hole contact for silicon solar cells," *Applied Physics Letters,* vol. 105, no. 23, p. 232109, 2014.

[201] R. A. Sinton and A. Cuevas, "A quasi-steady-state open-circuit voltage method for solar cell characterization," in *Proceedings of the 16th European photovoltaic solar energy conference,* 2000, vol. 1152, pp. 1-4.

[202] M. A. Leilaeioun, W. Weigand, M. Boccard, J. Y. Zhengshan, K. Fisher, and Z. C. Holman, "Contact resistivity of the p-type amorphous silicon hole contact in silicon heterojunction solar cells," *IEEE Journal of Photovoltaics,* vol. 10, no. 1, pp. 54-62, 2019.

[203] A. Fell, "A free and fast three-dimensional/two-dimensional solar cell simulator featuring conductive boundary and quasi-neutrality approximations," *IEEE Transactions on Electron Devices,* vol. 60, no. 2, pp. 733-738, 2012.

[204] H. Plagwitz, M. Nerding, N. Ott, H. Strunk, and R. Brendel, "Low-temperature formation of local Al contacts to a-Si: H-passivated Si wafers," *Progress in Photovoltaics: Research Applications,* vol. 12, no. 1, pp. 47-54, 2004.

[205] K. C. Fong *et al.*, "Contact Resistivity of Evaporated Al Contacts for Silicon Solar Cells," *IEEE Journal of Photovoltaics,* vol. 5, no. 5, pp. 1304-1309, 2015.

[206] G. Nogay *et al.*, "Nanocrystalline silicon carrier collectors for silicon heterojunction solar cells and impact on low-temperature device characteristics," *IEEE Journal of Photovoltaics,* vol. 6, no. 6, pp. 1654-1662, 2016.

[207] Z. C. Holman, S. De Wolf, and C. Ballif, "Improving metal reflectors by suppressing surface plasmon polaritons: a priori calculation of the internal reflectance of a solar cell," *Light: Science Applications,* vol. 2, no. 10, p. e106, 2013.

[208] M. Boccard *et al.*, "Low-refractive-index nanoparticle interlayers to reduce parasitic absorption in metallic rear reflectors of solar cells," *physica status solidi,* vol. 214, no. 10, p. 1700179, 2017.

[209] D. Meier *et al.*, "Determining components of series resistance from measurements on a finished cell," in *2006 IEEE 4th World Conference on Photovoltaic Energy Conference,* 2006, vol. 2, pp. 1315-1318: IEEE.

[210] Z. Wang, J. Wang, L. Jeurgens, and E. Mittemeijer, "Thermodynamics and mechanism of metal-induced crystallization in immiscible alloy systems: Experiments and calculations on Al/a-Ge and Al/a-Si bilayers," *Physical review B,* vol. 77, no. 4, p. 045424, 2008.

[211] H. Ohmi, K. Yasutake, Y. Hamaoka, and H. Kakiuchi, "Metal induced hydrogen effusion from amorphous silicon," *Applied Physics Letters,* vol. 91, no. 24, p. 241901, 2007.

[212] J. Bullock *et al.*, "Amorphous silicon passivated contacts for diffused junction silicon solar cells," *Journal of Applied Physics,* vol. 115, no. 16, p. 163703, 2014.

[213] S. De Wolf and M. Kondo, "Nature of doped a-Si: H/c-Si interface recombination," *Journal of Applied Physics,* vol. 105, no. 10, p. 103707, 2009.

[214] C. Sun *et al.*, "Origins of hydrogen that passivates bulk defects in silicon heterojunction solar cells," *Applied Physics Letters,* vol. 115, no. 25, p. 252103, 2019.

[215] J. Custer *et al.*, "Density of amorphous Si," *Applied physics letters,* vol. 64, no. 4, pp. 437-439, 1994.

[216] M. Haque, H. Naseem, and W. Brown, "Aluminum-induced degradation and failure mechanisms of a-Si: H solar cells," *Solar Energy Materials & Solar Cells,* vol. 41, pp. 543-555, 1996.

[217] M. Al-Barghouti, H. Abu-Safe, H. Naseem, W. D. Brown, and M. Al-Jassim, "The effects of an oxide layer on the kinetics of metal-induced crystallization of a-Si: H," *Journal of The Electrochemical Society,* vol. 152, no. 5, pp. G354-G360, 2005.

[218] K. Katkhouda *et al.*, "Aluminum-based rear-side PVD metallization for nPERT silicon solar cells," *IEEE Journal of Photovoltaics,* vol. 4, no. 1, pp. 160-167, 2014.

[219] J.-H. Wei and S.-C. Lee, "The retardation of aluminum-amorphous silicon interaction by phosphine plasma treatment," *Journal of Vacuum Science Technology A: Vacuum, Surfaces, Films*, vol. 16, no. 2, pp. 587-589, 1998.

[220] L. Sidhu, T. Kosteski, S. Zukotynski, and N. Kherani, "Infrared vibration spectra of hydrogenated, deuterated, and tritiated amorphous silicon," *Journal of applied physics*, vol. 85, no. 5, pp. 2574-2578, 1999.