A Current-Mode, Dynamic Hysteresis Hybrid Supply Modulator for Wideband LTE Applications

by

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ABSTRACT

The world has seen a revolution in cellular communication with the advent of 5G (fifth-generation), which enables gigabits per second data speed with low latency, massive capacity, and increased availability. These modern wireless systems improve spectrum efficiency by employing advanced modulation techniques, but result in large peak-to-average power ratios (PAPR) of the transmitted signals that degrades the efficiency of the radio-frequency power amplifiers (PAs) in the power back-off (PBO) region. Envelope tracking (ET), which is a dynamic supply control technology to realize high efficiency PAs, is a promising approach for designing transmitters for the future. Conventional voltage regulators, such as linear regulators and switching regulators, fail to simultaneously offer high speed, high efficiency, and improved linearity. Hybrid supply modulators (HSM) that combine a linear and switching regulator emerge as promising solutions to achieve an optimized tradeoff between different design parameters. Over the years, considerable development and research efforts in industry and academia have been spent on maximizing HSM performance, and a majority of the most recently developed modulators are implemented in CMOS technology and mainly targeted for handset applications.

In this dissertation, the main requirements for modern HSM designs are categorized and analyzed in detail. Next, techniques to improve HSM performance are discussed. The available device technologies for HSM and PA implementations are also delineated, and implementation challenges of an integrated ET-PA system are summarized. Finally, a Current-Mode with Dynamic Hysteresis HSM is proposed, designed, and implemented. With the proposed technique, the HSM is able to track LTE signals up to 100 MHz bandwidth. Switching at a peak frequency of 40 MHz, the design is able to track a 1 Vpp sinusoidal signal with high fidelity, has an output voltage ripple around 54 mV, and achieves a peak static and dynamic efficiency of

92.2% and 82.29%, respectively, at the maximum output. The HSM is capable of delivering a maximum output power of 425 mW and occupies a small die area of 1.6mm^2. Overall, the proposed HSM promises competitive performance compared to state-of-the-art works.

DEDICATION

To my kind father, beloved mother, and dear sister.

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Chapter 1

INTRODUCTION

Recent advancements in wireless communications have led to the use of spectrally efficient complex modulation schemes, such as quadrature amplitude modulation (QAM) and orthogonal frequency division multiplexing (OFDM), to achieve higher data-rates within a limited spectrum. The growing demand for high data rate cellular systems has pushed the adoption for 4G/5G long-term evolution (LTE) which bring high data capacity, low latency, long battery life, more device connectivity etc. using sub-6 GHz and mm-Wave spectrum [1] as shown in Figure 1.1. Channel bandwidths have also increased with each generation of wireless technology to support faster communication, as illustrated in Figure 1.2(a). Unfortunately, wide channel bandwidths create signals with high peak to average power ratio (PAPR), as demonstrated in Figure 1.2(b) for cellular handset communications [2]. The RF transmitter's power amplifier (PA) is the most power-hungry block in the transceiver, as it can consume more than 60% of the total power in the entire transmitter chain [3][4]. Therefore, to amplify signals with high PAPR levels, the PA needs to demonstrate high efficiency not only at peak power, but also at power back-off levels (PBO). Standalone PAs are not highly efficient at PBO [5], thus motivating the need for advanced architectures and techniques to boost PBO efficiency [6][7][8][9][10][11][12][13][14][15].

Envelope Tracking (ET) is a popular technique to improve the efficiency of a radio frequency PA at PBO levels. In this technique, the PA's drain bias is modulated as a function of the RF input signal's time-varying envelope to minimize the DC power dissipation within the PA. This forces the PA to always operate near its compression point, where it usually demonstrates highest efficiency. Figure 1.3(a) and 1.3(b) show

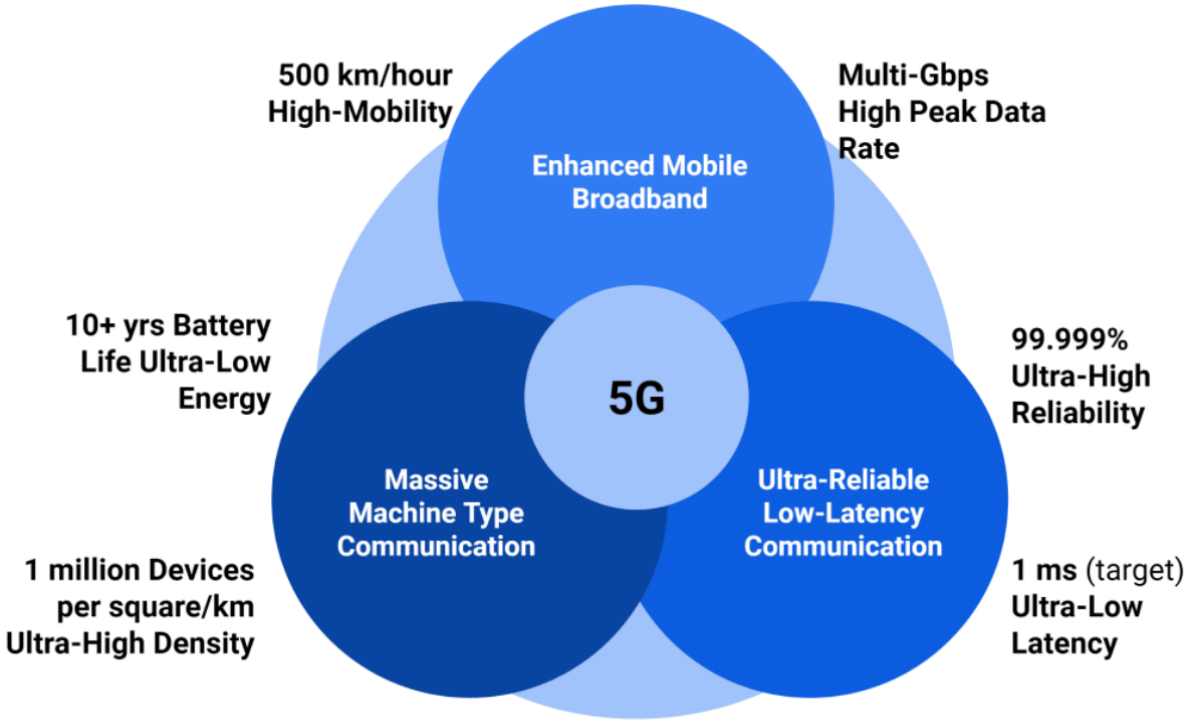
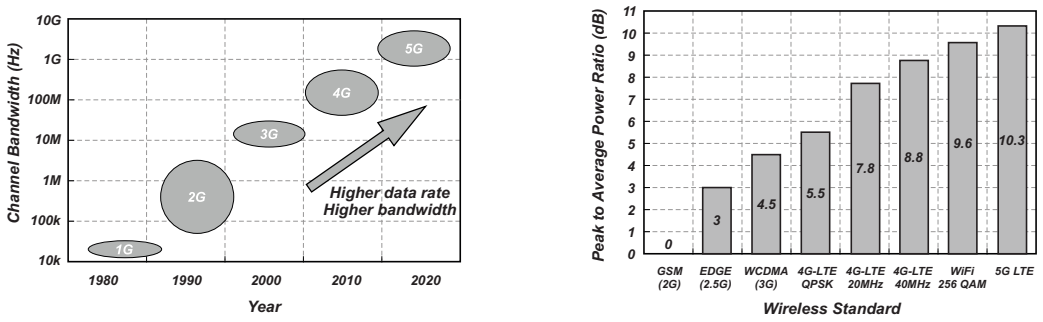


Figure 1.1: The Key Characteristics of 5G, or Fifth-generation Wireless Technology

a PA using a conventional fixed supply and a modulated supply, respectively. The reduction in PA energy dissipation is conceptualized in Figure 1.3(c) and 1.3(d) by illustrating that the modulated supply reduces the overhead DC power consumption. The ET technique leads to efficiency enhancement at PBO levels, as the supply modulates with power level (envelope) and therefore shifts the PA's efficiency curve with PA output power, as illustrated in Figure 1.4.

ET systems have high integration capability within cellular handset devices, and therefore the demand for ET integrated circuits (ICs) to support the smart-phone market continues to rapidly grow (Figure 1.5) [16]. Figure 1.5 demonstrates that the importance of ET has increased over the years and continues to do so as the wireless communication market moves closer to the fifth-generation (5G) era. ET can also be used in conjunction with other efficiency enhancement structures, such as Doherty



(a) (b)

Figure 1.2: (a) Trend in Channel Bandwidth with Evolving Communications' Standards (b) PAPR Trend in Cellular Handset Communications

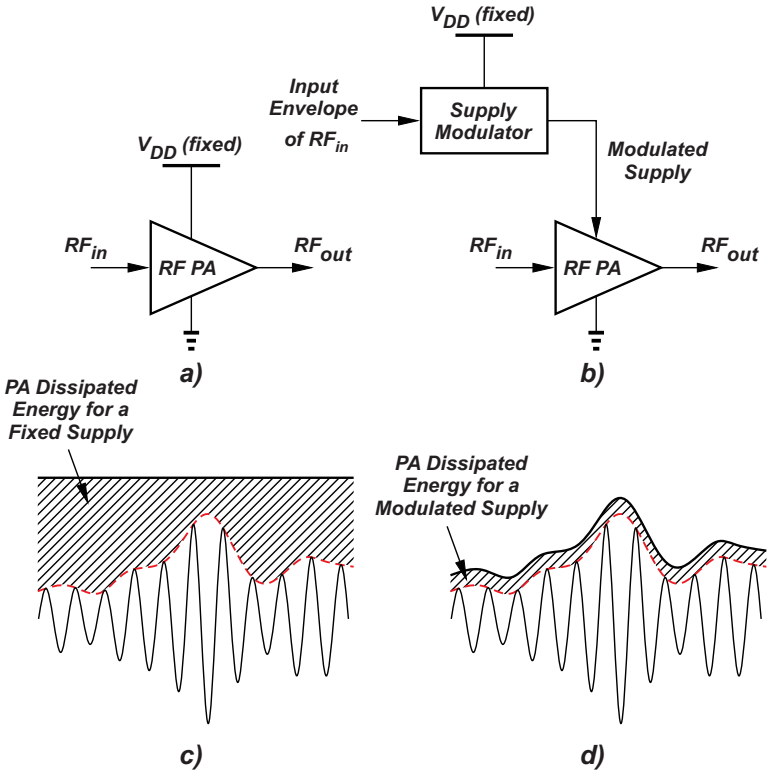


Figure 1.3: A Conventional RF PA (a) with Fixed, and (b) with Modulated Supply, PA Energy Dissipation (c) with Fixed Supply, (d) with Modulated Supply.

or load modulation techniques [17][18], switched-mode [19], and outphasing [20], to

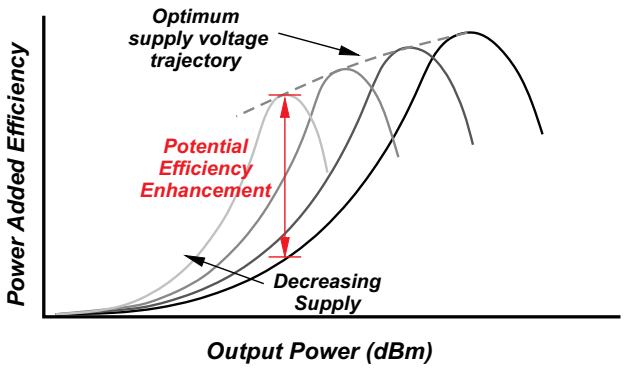


Figure 1.4: PA Power Added Efficiency Versus Output Power Showing Efficiency Enhancement at PBO Levels with a Modulated Supply in an ET-PA System

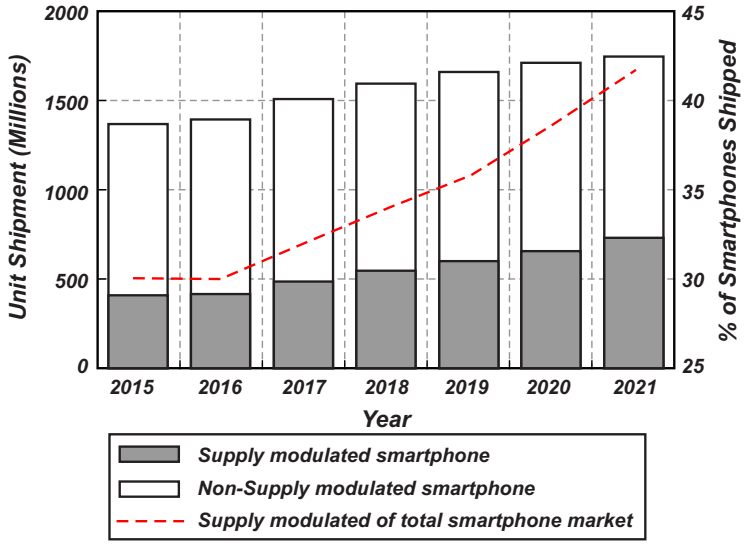


Figure 1.5: Number of ET-ICs Deployed over the Years (and Projections)

further improve ET-PA performance.

In an ET system, the supply modulator (SM) acts as the power management unit for the PA. Therefore, in order to successfully realize an ET-PA, the SM must satisfy the continuously increasing performance demands of evolving wireless transmit hardware. Over the years, considerable development and research efforts in industry and academia have been spent on maximizing SM performance, and a majority of the most recently developed modulators use a hybrid SM (HSM) topology implemented

in various CMOS technologies and mainly targeted for handset applications. In light of the recent technology trends in ET-PAs and the importance of SM performance on overall ET-PA system performance, this dissertation initially gives a comprehensive review that also categorizes and explains the various HSM developments implemented in CMOS to-date. This dissertation begins with a discussion of different performance requirements on SM design and covers the various SM topologies and explains the operation of the most widely adopted HSM topology in Chapter 2. Chapter 3 categorizes the performance parameters on HSM. Various published techniques/architectures in the literature to optimize the performance of HSMs are delineated. Furthermore, different device technologies for HSM and PA implementations and discusses challenges of an ET-PA system are covered in Chapter 4. Then, the proposed HSM design with the simulation and measurement results are detailed in Chapter 5. This dissertation concludes with Chapter 6 that gives the overall conclusion and future work.

Chapter 2

SUPPLY MODULATOR FOR ENVELOPE TRACKING

The growing demand for high data rate cellular systems has pushed the adoption for 4G/5G long-term evolution (LTE) which uses high PAPR modulation schemes with rapid deployment and replacement. 5G will bring high data capacity and low latency using sub-6 GHz and mm-Wave spectrum, with the first deployment using sub-6 GHz bands. The increased adoption of powerful worldwide smartphones has been in part possible due to increase of CMOS technology in lower feature nodes as FinFET 7 nm/14 nm [21]. This has made also possible to essentially enhance RF CMOS through digital signal processing (DSP) and digital calibration which are part of smartphone modem and application processor. Also, this has made possible the adoption of an "old" techniques such as envelope tracking (ET) into smartphone. The ET technique was mentioned back in 1952 [22] by Leonard R. Kahn who introduced a related technique envelope elimination and restoration (EER). Envelope tracking improves the linearity and efficiency RF for power amplifier. The RF power amplifiers are typically the most power-hungry components and take a lot of area in a wireless transmitter. With explosive band proliferation as well as the use of carrier aggregation (CA) and multiple input multiple output (MIMO) techniques, the research area of improving the cost, size, and the performance of RF transmit solution is very active with many developments and product deployment over the last years.

Supply modulators for ET-PA systems have three main performance requirements: efficiency, speed, and linearity (ripple). To adequately achieve these performance requirements for continuously evolving wireless standards, various SM topologies have been proposed and are discussed in the following subsections.

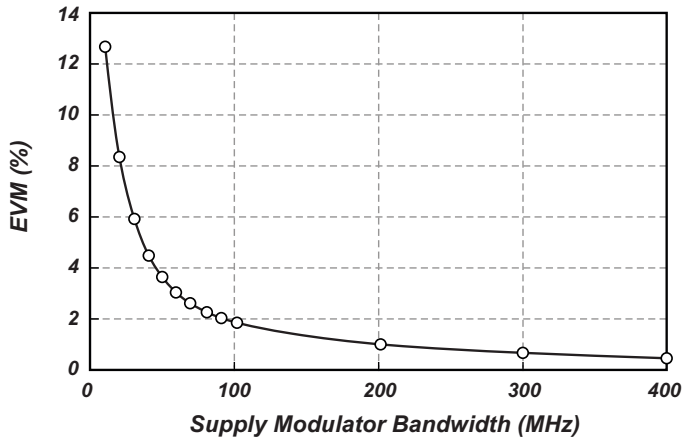


Figure 2.1: Simulated EVM Versus SM Bandwidth for a WLAN IEEE 802.11g OFDM Signal

2.1 Supply Modulator Design Requirements

Firstly, a SM needs to demonstrate high efficiency in order to maximize the overall efficiency of an ET-PA system (η_{ET-PA}), which can be expressed as:

$$\eta_{ET-PA} = \eta_{SM} \times \eta_{PA} \tag{2.1}$$

where η_{SM} and η_{PA} represent the individual efficiencies of the SM and PA, respectively. As can be seen from equation 2.1, the overall ET-PA system efficiency is limited by the SM efficiency, thus motivating the need for high efficiency SMs.

Secondly, a SM needs to demonstrate high-speed in order to track fast input envelopes. The term speed for a SM is expressed in terms of both bandwidth and slew-rate (covered in Chapter 3). It should be noted that the envelope of a modulated RF signal has a much higher bandwidth than the bandwidth of the actual RF signal itself. As explained in [23], the envelope signal's power is distributed from DC to the envelope signal's higher order harmonics. In order to process most of the envelope signal and avoid significant distortion at the output, the SM is required to have much higher bandwidth (usually around $4-5$ times) than the RF input signal's bandwidth. To demonstrate the importance of SM bandwidth on RF signal quality, Figure 2.1

shows the effect of SM bandwidth on the RF signal's error vector magnitude (EVM) when tracking a WLAN envelope signal of 20 MHz bandwidth.

Finally, a SM needs to demonstrate low ripple at the output in order to achieve high linearity. At the SM's output, the processed input envelope signal is replicated along with an additional ripple that can be represented by a frequency f_s. As shown in Figure 2.2, there is a mixing effect [24] that up-converters the ripple around the fundamental carrier frequency (f_c) at the side-bands $f_c \pm f_s$, with a separation entirely dependent on the ripple frequency. Although the linearity of an ET-PA system is mainly dictated by the PA, the effect of ripple on the SM output can be observed in the PA's output spectrum [25]. If the input RF signal is $S_{in} = v_{in}cos(2\pi f_c t)$ and the ripple from the SM is $S_{ripple} = v_s cos(2\pi f_s t)$, then the amplitude ($v_{out}$) of the supply ripple at the sidebands is given by:

$$v_{out}(v_{in}, v_{ripple}) = \sum_{i,j=0}^{\infty} a_{i,j} {v_{in}}^{\mathrm{i}} {v_{ripple}}^{\mathrm{j}} \tag{2.2}$$

where $a_{i,j}$ are the gain terms as a function of the i^{th} order of the input voltage and the j^{th} order of the voltage ripple. The first order ripple induced side-bands (at $f_c \pm f_s$) around the RF carrier (at f_c) is:

$$v_{out}(f_c \pm f_s) = \frac{1}{2} a_{11} v_{in} v_{ripple} \tag{2.3}$$

where v_{in} and v_{ripple} are the amplitude of the signals at f_c and f_s, respectively, and a_{11} represents the first order inter-modulation product between the RF signal and SM ripple. From equation 2.3, the PA's output linearity is directly affected by the SM's output ripple (v_{ripple}).

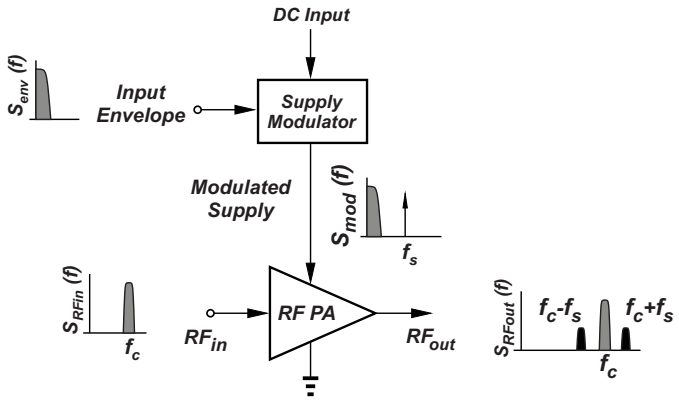


Figure 2.2: Frequency Spectrum at Different Locations in an ET-PA System

2.2 Supply Modulator Topologies

There are four main SM topologies [26], namely linear, switching, series, and hybrid, as illustrated in Figure 2.3. All topologies are optimized for the main specifications of efficiency, speed, and linearity (ripple). Most recent advancements in SM are direct implementations, variations, or extensions of these four basic topologies.

In the first topology of Figure 2.3(a), the SM is implemented with a linear regulator. A linear topology can achieve high bandwidth and high linearity, but a main drawback is poor efficiency at low power levels. The efficiency of a linear regulator is directly proportional to its output voltage [27], so the efficiency drops rapidly as the output voltage level decreases. Since existing (and future) communication standards depict high PAPR levels, this linear topology is not effective because the PA operates mostly in the PBO region.

The second SM topology of Figure 2.3(b) uses a switching regulator. This topology provides higher efficiency than the linear regulator for a wider range of voltage levels, as this efficiency can reach above 90% depending upon frequency and load current [28]. But, the disadvantage is that the switching function produces high ripple content at the output, which degrades the SM linearity. Filtering this ripple through the use

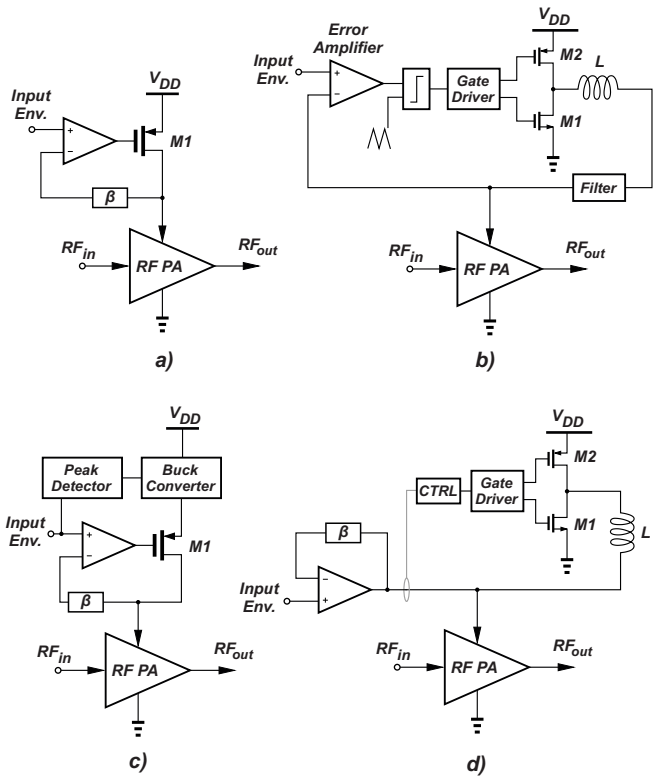


Figure 2.3: Different Supply Modulator Topologies: (a) Linear (b) Switching (c) Series, and (d) Hybrid

of a high order filter is one option, but filtering reduces the maximum achievable bandwidth and would not be suitable for wideband applications. Another option is to increase the regulator's switching speed, but the switching losses increase with the frequency [29] and efficiency degrades. In order to demonstrate the increase in switching loss with switching frequency, a mostly ideal switching regulator (with control/driver circuitry excluded) was designed in a TSMC 65nm CMOS process. This case study uses the TSMC device (FET) models, but all drivers and output passive circuitry are ideal. Although the exact value of switching loss depends upon the sizing of transistors and quality factor of passives, the general behavior of efficiency with respect to switching frequency is demonstrated in Figure 2.4 and shows efficiency

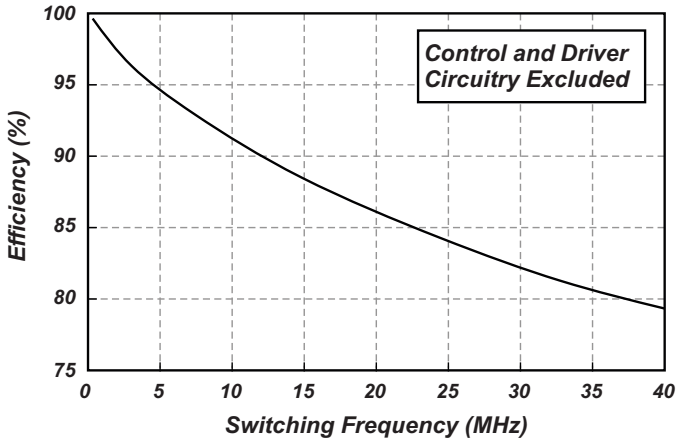


Figure 2.4: Case Study Illustrating Idealized Switching Regulator Efficiency Versus Switching Frequency

decay with increasing frequency.

The third SM topology of Figure 2.3(c) uses a series connection of linear and switching regulators [30]. This is mainly used to enhance the efficiency of the linear regulator and maintain good SM linearity, as the linear regulator exhibits low output ripple and provides power supply rejection that attenuates the ripple from the switching regulator. While this topology has higher efficiency than the stand-alone linear regulator of Figure 2.3(a), the main drawbacks of this topology are high switching losses for wideband applications, conduction loss due to the presence of a pass-device in the load current path, degradation of the linear regulator's power supply rejection, and most importantly the required additional overhead to operate the series switching regulator. The added overhead makes this architecture difficult to realize in most CMOS process technologies.

The fourth SM topology of Figure 2.3(d) uses a parallel combination of linear amplifier and switching amplifier. This topology is popularly known as a hybrid supply modulator (HSM), and it is currently the most prevalent and widely used SM

Table 2.1: Performance Comparison of SM Topologies

SM Topology	Efficiency	Speed (Bandwidth)	Linearity
Linear	Low	High	High
Switching	High	Low	Low
Series	Moderate	Low	Moderate
Hybrid	High	Moderate	High

topology. The linear amplifier (LA) is responsible for wide bandwidth operation and high linearity due to ripple compensation, while the switching amplifier (SA) provides high efficiency current to the load. This topology is discussed in detail in Chapter 3. Table 2.1 provides a qualitative performance comparison amongst the four different SM topologies.

2.3 Hybrid Supply Modulator

The HSM architecture [31][32][33][23][34][35] emerges as a promising solution to the efficiency, speed, and linearity trade-offs observed in different SM topologies. The working principle of the HSM and different loop control methods involved in HSM design are explained in detail in the following subsections.

2.3.1 Description of HSM operation

A typical HSM design consists of two amplifiers working simultaneously as shown in Figure 2.5. The left side of Figure 2.5 is a voltage-control/linear amplifier (LA), which is responsible for regulating the output voltage to the input envelope voltage via feedback. The right side of the HSM in Figure 2.5 is a current-control/switching amplifier (SA), which is responsible for providing high efficiency inductor current to the load. The majority of the low-frequency load current is provided by the SA, while

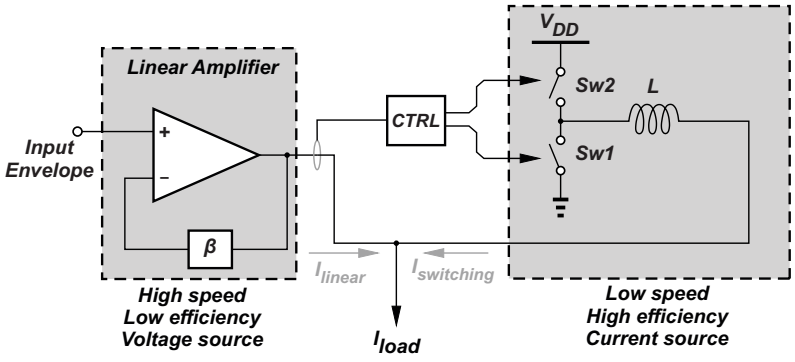


Figure 2.5: The Hybrid Supply Modulator (HSM) Architecture

the wideband LA supplies the remainder of the higher frequency current. The ripple on the switching current is compensated by the LA to provide a highly linear power supply to the load (i.e. PA).

Depending upon the input signal's envelope bandwidth, the transition frequency (F_{tr}) of a HSM [37], defined as the frequency where the current provided by the SA and LA are equally split, is chosen based on an efficiency and linearity trade-off. Figure 2.6(a) and (b) illustrate the frequency response of SA and LA currents for low and high values of F_{tr} with a fixed input envelope power spectral density. If F_{tr} is chosen too small, the low efficiency LA supplies the majority of the current to the load, which degrades the efficiency of the HSM. If F_{tr} is chosen too large, the SA must switch at higher speed with higher switching loss and generates more current ripple that can result in linearity degradation.

The basic operation of a HSM is demonstrated through the example plots of Fig. 2.7, which are generated via simulation of a HSM using verilog-A models of the LA and SA. In this example, the LA is modeled with a DC gain of 60 dB and 3-dB bandwidth of 50 kHz and the SA has an output inductor of 1μH. The HSM's load is modeled as 5 Ω || 10 pF to emulate a PA's drain impedance. For this case study, an input sinusoidal signal is provided to the circuit to generate 200 mA of DC current

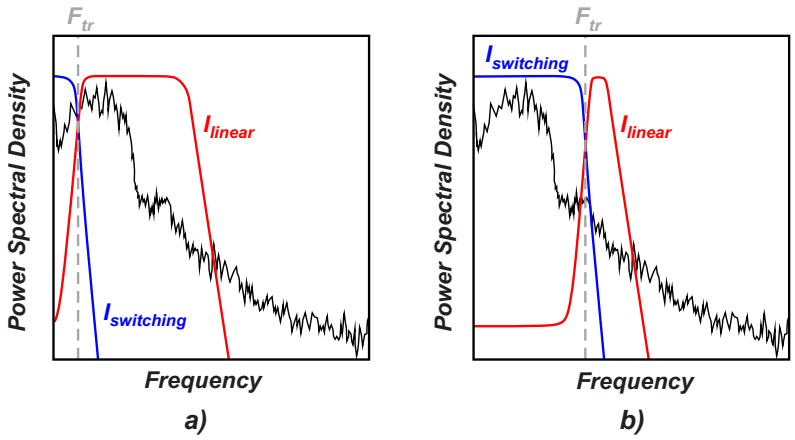


Figure 2.6: HSM With (a) Low and (b) High Transition Frequency (F_{tr})

with 100 mA of AC swing. The frequency of the input signal is varied, and the current waveforms I_{linear}, $I_{switching}$, and I_{load} are observed in Fig. 2.7.

When the input signal is a DC input as in Figure 2.7(a), the SA provides the average current to the load with switching ripple caused by the SA's switching operation. The ripple is compensated by the LA to generate a constant load current. For a low frequency 100 kHz input signal as in Figure 2.7(b), the SA current moves with the input signal because the SA generates the average current and the ripple cancellation is provided by the LA. As the signal frequency is increased to 1 MHz in Figure 2.7(c), the SA begins to slew due to its limited bandwidth. The load current still follows the input signal, but the magnitude of the LA current increases where the SA cannot provide current during the fast signal transitions (high frequency). Finally, at a high input signal frequency of 10 MHz in Figure 2.7(d), the SA ramps up slowly and cannot adequately follow the input signal. The low-efficiency LA provides a significant amount of the load current, thus degrading HSM efficiency.

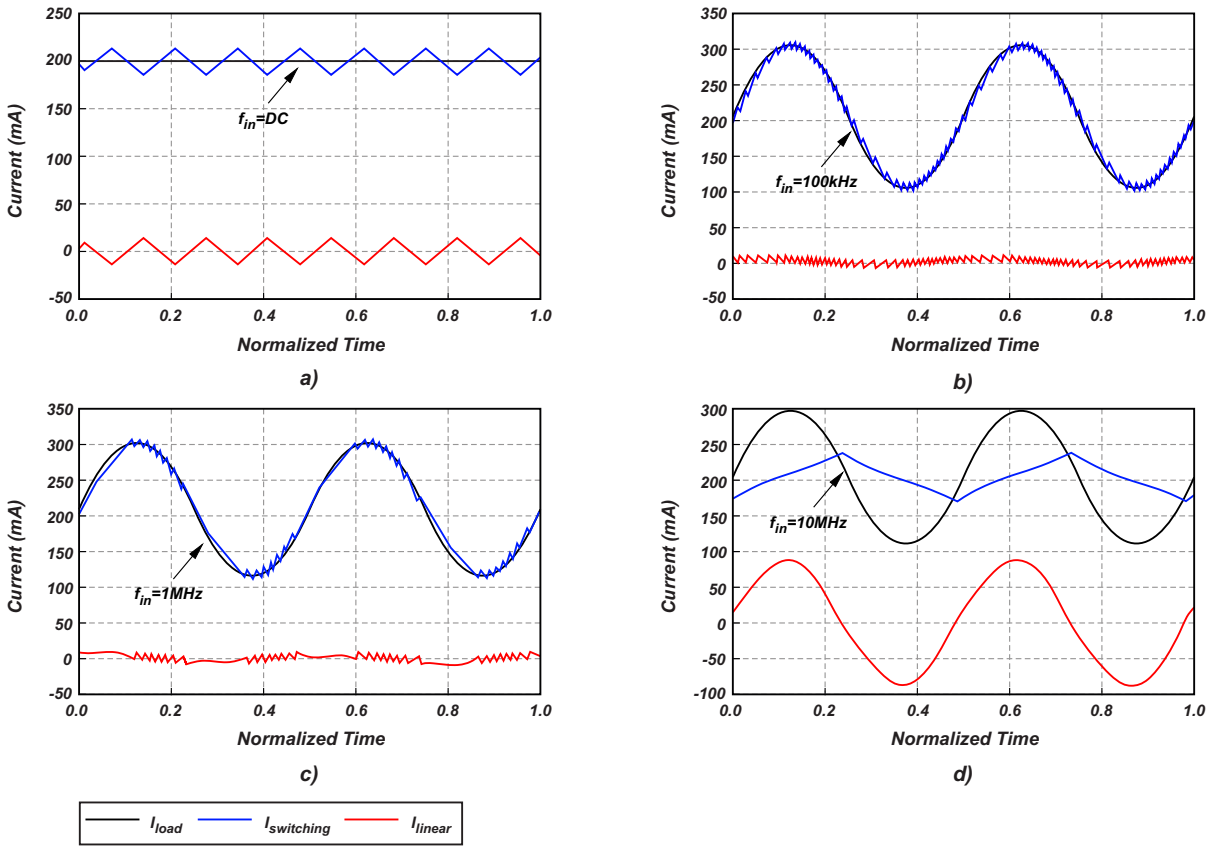


Figure 2.7: Linear (I_{linear}), Switching ($I_{switching}$), and Load (I_{load}) Current Waveforms for (a) DC, (b) 100 kHz, (c) 1 MHz, and (d) 10 MHz Input Signals.

2.3.2 Loop Control Methods

There are two main methods to generate the SA's control signal ($CTRL$ shown in Figure 2.5) and regulate the switching loop. The first method is known as pulse width modulation (PWM) control and is illustrated in Figure 2.8(a) [31][32][33]. In this method, the LA current (I_{linear}) is converted to a voltage, using an I-to-V converter, that drives the compensator A(s). The output of the compensator is compared with a synchronization waveform, which can be a ramp or a triangular signal, to modulate the duty cycle of the switching loop to adjust the SA current ($I_{switching}$). In PWM control, the switching loop bandwidth is limited to a fraction of its switching frequency, thus

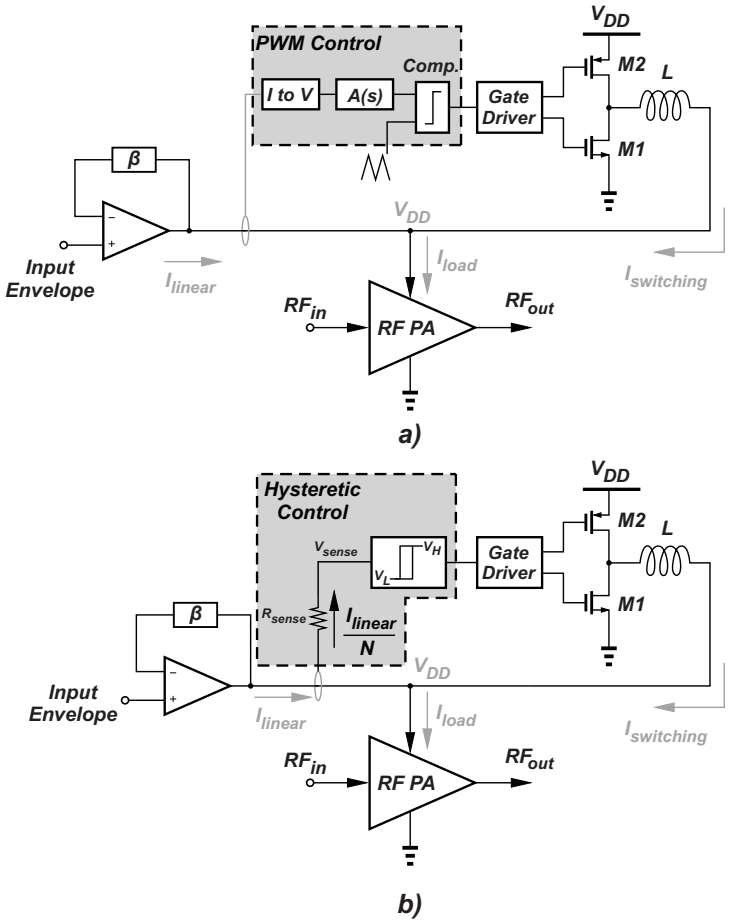


Figure 2.8: Loop Control Methods in a HSM Design (a) PWM Mode and (b) Hysteretic Mode

leading to a slower loop response.

The second method shown in Figure 2.8(b) is known as hysteretic control [23][34][35]. In a hysteretic controller, a fraction of I_{linear} current is first converted to a voltage (V_{sense}) typically by using a sense resistor (R_{sense}). The value of V_{sense} is then compared to two threshold voltage values set by the designer using a hysteretic comparator, and the output of this comparison controls the switching loop to adjust the SA current ($I_{switching}$). Since hysteretic control uses a window comparator instead of a clocked comparator as in PWM control, the loop response of the hysteretic control is faster, which means wider SA bandwidth. A hysteresis loop is also inherently stable

across a wide load range and does not require compensation circuitry, which leads to simpler loop design compared to PWM control.

In PWM control, the switching frequency is independent of the input signal and remains constant. But in the case of hysteretic control, the switching frequency varies with the magnitude of the input signal [36]. The expression for its average switching frequency (f_{sw}) is given by:

$$f_{sw} = \frac{R_{sense} V_{out} (V_{DD} - V_{out})}{2 V_{DD} N L V_{hys}} \tag{2.4}$$

where V_{DD}, V_{out}, V_{hys}, R_{sense}, N, and L are the supply voltage, the output voltage, the hysteresis window of the comparator, the sense resistor, the current sensing ratio, and the inductor value, respectively. The highest switching frequency (f_{sw_max}) is reached when the output voltage equals $V_{DD}/2$ and this maximum frequency can be expressed as:

$$f_{sw\_max} = \frac{R_{sense} V_{DD}}{8 N L V_{hys}} \tag{2.5}$$

It can be seen from equation 2.4−2.5, that the f_{sw} depends on two important factors, the hysteresis window and the output inductor value. Therefore, the value of V_{hys} and L should be optimized for highest achievable HSM efficiency, speed, and linearity. Furthermore, the hysteresis can be implemented in both voltage and current mode, which is generally not the case in PWM control. Since hysteretic control provides several advantages compared to PWM control as outlined above, hysteretic controllers are used in the majority of present-day HSMs.

Hybrid supply modulators must be continuously advanced to follow the continuously more demanding requirements of wireless communication standards. HSMs must track wideband/fast-changing signals in present and future communications. Obtaining adequate output power from a HSM has also become a significant challenge in recent years due to battery voltage variation over time and aggressive scaling

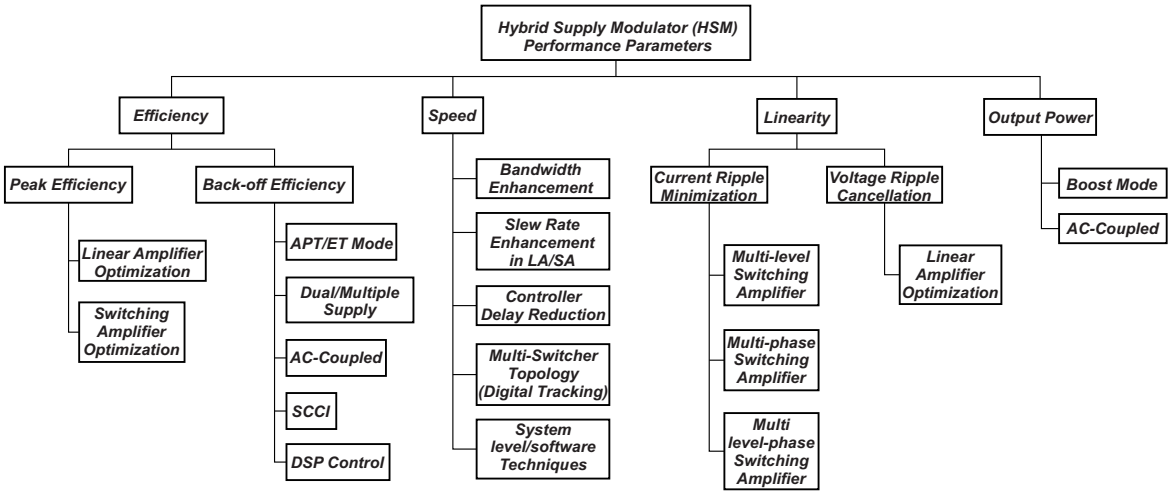


Figure 2.9: Various Methods for Optimizing HSM Performance

in CMOS process technologies. Various techniques and architectures have been proposed to optimize performance of HSMs in terms of efficiency, speed, linearity, and output power. For the purposes of this review, and in order to organize the various architectures and differentiate them from one another, these techniques have been categorized in the diagram of Figure 2.9. Various methods and architectures are organized into these categories based on their primary performance parameter for improvement, but it is important to note that most of these works improve multiple performance parameters such as both output power and efficiency. The following Chapter 3 provide more details on these different techniques.

Chapter 3

PERFORMANCE PARAMETERS OF HYBRID SUPPLY MODULATOR (HSM)

3.1 Efficiency Improvements in HSM

A HSM needs to demonstrate high efficiency to maximize overall ET-PA system efficiency (from equation 2.1). Since the PA operates mostly in its power back-off (PBO) region, it is desirable for the HSM to maintain high efficiency at both peak and back-off power levels. In the following subsections, this work presents a brief analysis of the loss mechanisms contributed by different components in a HSM and reviews the proposed efficiency enhancement techniques.

3.1.1 HSM Peak Efficiency Improvement

In order to maximize peak efficiency of a HSM, it is important to acknowledge the HSM's different sources of loss and minimize them using improved design techniques.

Analysis of Loss

Many different sources, such as the linear and switching amplifiers, controller block, off-chip inductor, and board parasitics, contribute to the overall static and dynamic losses in a HSM. A simplified model of the HSM for loss analysis is shown in Figure 3.1. The majority of the losses in a HSM are contributed by the LA and the SA [38]. Therefore, most optimization efforts focus on minimizing the losses in these circuit blocks. The LA loss is mainly dominated by the voltage drop of the class-AB output stage (V_{drop}xI_{linear}), where the voltage drop V_{drop} depends upon the output voltage [38][39]. Apart from this, the biasing circuitry of the amplifier and the quiescent

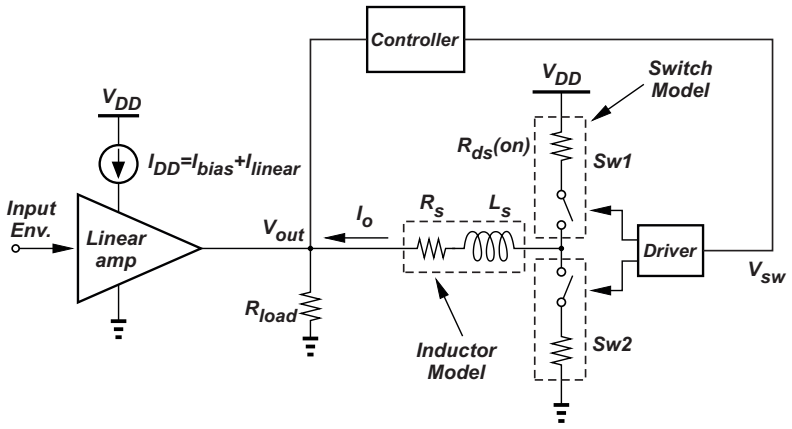


Figure 3.1: A Simplified Model of the HSM for Loss Analysis

current in the LA output stage (e.g. class-AB stage) contribute to the static DC loss (P_{LA_bias}). Hence, the total loss in the LA (P_{LA}) can be expressed as the sum of $P_{LA\_classAB}$ and P_{LA_bias}.

The loss mechanisms in a SA (P_{SA}) include, but are not limited to: switching losses (gate drive loss, diode-recovery loss etc.), conduction losses due to the on-resistance of the switches and dc resistance of the inductor, and capacitor losses due to finite ESR (equivalent series resistance). The SA losses are dependent upon several design parameters like switching frequency, load current, duty cycle etc., and a detailed breakdown of the different losses with their expressions can be found in [40].

The loss mechanism in the HSM's controller block is static DC power dissipation and can be expressed as P_{Ctrl}, whose magnitude depends upon the type of control used (hysteretic or PWM control). The HSM's extra sources of loss (P_{ext}) consists of non-ideal effects caused due packaging, board routing, board parasitics etc. It should be noted that the losses described thus far are broadly analyzed in existing works such as [41], and are highly dependent upon implementation and system specifications. If V_{out} is the output voltage across a load resistor R_{load}, then the power obtained at the output of a HSM is P_{out} and the expression for its efficiency (η_{HSM}) is given by:

$$P_{out} = \frac{V_{out}^2}{R_{load}} \tag{3.1}$$

$$\eta_{HSM} = \frac{P_{out}}{P_{out} + P_{LA} + P_{SA} + P_{Ctrl} + P_{ext}} \times 100 \tag{3.2}$$

Different circuit techniques and methods to reduce the HSM loss (dominated by LA and SA) are discussed in the next subsections.

Reducing LA Loss

The LA's output devices are generally of large size to drive a large amount of transient current I_{linear}, to compensate for the switching ripple. Hence, there is need for design techniques that reduce the amount of I_{linear} to reduce $P_{LA\_classAB}$ and also static DC loss, P_{LA_bias}, in the LA.

In order to reduce LA static power dissipation P_{LA_bias}, class-AB devices can be biased more towards a class-B configuration. But, a class-B output stage generates more cross-over distortion and reduces the current providing capability of the LA. Therefore, adaptive-biasing for the class-AB devices can be employed to save DC power, in which the bias is shifted between class-AB and class-B depending upon the output current requirements [42]. Additionally, LA designs are sensitive to process, voltage, and temperature (PVT) variations that can change the class-AB quiescent current significantly (by more than 300%). Therefore, circuit levels techniques like accurate current quiescent control and supply voltage and temperature insensitive quiescent current control can be used to control the variation of class-AB current and avoid wasting P_{LA_bias} [43][44].

In order to reduce conduction loss $P_{LA\_classAB}$, the LA's output current I_{linear} needs to be reduced. For low-frequency operation, I_{linear} equals the ripple current

from the SA (from Figure 2.7 (b)). So, the value of I_{linear} can be reduced by adopting improved SA designs like multi-level or multi-phase [45] architectures that generate lower switching current ripple. These architectures detailed in Section 3.3.1. For high-frequency input signals, I_{linear} increases because the SA cannot provide the entire load current (from Figure 2.7 (d)). The SA's switching frequency can be increased to reduce I_{linear}, but the trade-off is increased SA loss as discussed in the next subsection.

Reducing SA Loss

In a SA design, the magnitude of the SA's average output current (I_o) is determined by the PA's load requirement, which in turn determines the SA device size and therefore conduction losses. The SA's driver and power stage devices are typically sized at the optimum crossover point between conduction loss and switching loss. The SA power loss can be decreased by two methods. In the first method, the switching frequency, f_{sw}, of a HSM can be lowered, but this leads to a slower response from the SA and is not effective for tracking wideband signals, as was previously illustrated in Figure 2.7(c). In the second method, advanced topologies for the SA are implemented to reduce various losses, which can improve the HSM efficiency.

The work in [46] shows that the conduction loss due to the inductor peak-to-peak current ripple is proportional to the voltage swing at the switching node. For an input voltage of V_{DD}, the voltage swing at the switching node is V_{DD} (for 2-level SA), $V_{DD}/2$ (for 3-level SA), $V_{DD}/4$ (for 5-level SA) and so on. So, in the case where conduction losses are dominant over other SA losses, moving to a multi-level SA topology can lead to reduction of conduction losses and boosting of efficiency. Another work in [47] explains that the multi-level SA topology allows stacking of multiple shorter channel length devices, as shown in Figure 3.2. Hence, due to reduced parasitics, the switching losses in high frequency SAs can be reduced [48], and better

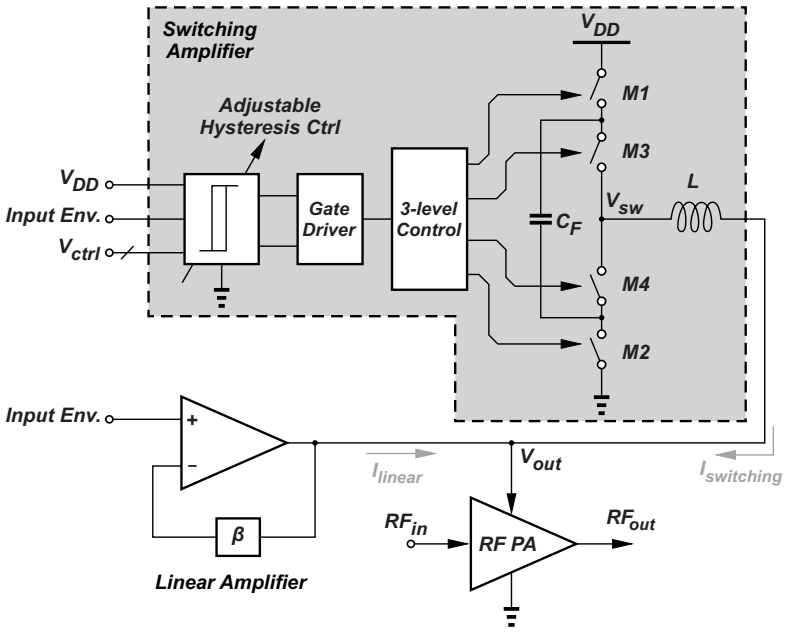


Figure 3.2: HSM Design with a Three-level SA Implementation

efficiency can be achieved while tracking wide bandwidth signals. Furthermore, the [49] shows that if the load current requirements are high (in the case of a high power PA), then the SA may benefit from a multi-phase topology because the conduction losses become a significant factor for high load current. In cases where load current changes significantly, digital controllers can be further employed to improve efficiency by adaptively changing the number of phases based on magnitude of the load current [50].

In addition to peak HSM efficiency, the HSM's efficiency at back-off power levels is also important because the ET-PA, and hence HSM, operate at back-off power during the majority of the transmit time to process high PAPR signals.

3.1.2 HSM Back-off Efficiency Improvement

At backed-off input signal levels, the HSM's required load current is low and the static power dissipation P_{LA_bias} in the LA becomes a dominant factor of loss. Due to this, the HSM demonstrates poor efficiency in the PBO region. There are various architectures proposed in literature to improve the back-off efficiency of a HSM by eliminating or reducing P_{LA_bias} at PBO. The efficacy of each architecture is explained in the following subsections.

Dual Mode (APT/ET) HSM

A dual mode architecture improves the PBO efficiency of a HSM by avoiding the use of a LA in the back-off region when the RF PA's input power is also low. For peak average output power, the HSM operates using both the LA and SA. But, for output power levels lower than some threshold that is set based on system design requirements, the HSM is reconfigured to work as a stand-alone SA using an additional lower bandwidth SA. This SA demonstrates significantly higher efficiency than the combination of both LA and SA because the high biasing current of the LA is eliminated and the stand-alone SA is optimized for lower power levels. The stand-alone SA must have a lower output filter bandwidth (i.e. higher inductor value) than the SA+LA combination to attenuate switching ripple that is normally canceled by the LA. Therefore, the stand-alone SA cannot track as wide of an input signal bandwidth as the combined SA+LA HSM. This dual mode modulator therefore supports ET in high power mode, and average power tracking (APT) of PAs at PBO.

The work in [51] adopts a dual mode HSM architecture and the measured results are shown in Figure 3.3. The results demonstrate that the efficiency of the HSM at 9 dB PBO was boosted up from 60% in ET mode (using the HSM with combined

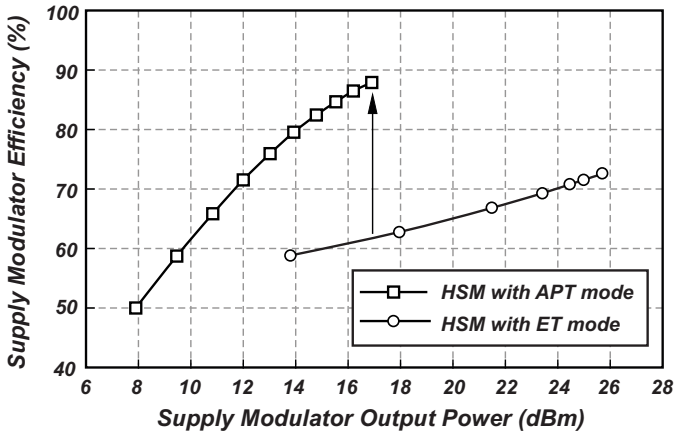


Figure 3.3: Efficiency of the Dual Mode HSM (with both APT and ET Modes) for a 16-QAM LTE Input Signal

SA+LA) to approximately 87% in APT mode using the stand-alone SA. However, the trade-off of this architecture is that it requires an additional stand-alone SA with additional circuit level components like a comparator, switching driver, power devices, control switches, and off-chip inductor, which leads to extra die-area/board space.

Dual/Multiple Supply HSM

The static power loss in the LA remains constant irrespective of the input envelope power level for a fixed LA supply voltage. It can be seen from Figure 3.4(a) that in the PBO region when the envelope power level is low and V_{DD} is high, there is wasted DC power. But when the V_{DD} is reduced for lower power signals, DC power can be saved and efficiency is enhanced, as illustrated in Figure 3.4(b). Therefore, the LA's supply voltage can be varied with the HSM's input signal level to reduce LA static losses, P_{LA_bias}. The work in [52] proposes a dual supply HSM architecture in which the V_{DD} of the LA is set to 5 V in high-power mode and reduced to 2.5 V in low-power mode (or back-off). The measured results of the dual supply HSM are recaptured in Figure 3.4(c) and demonstrate about 20% improvement in efficiency at 9 dB PBO

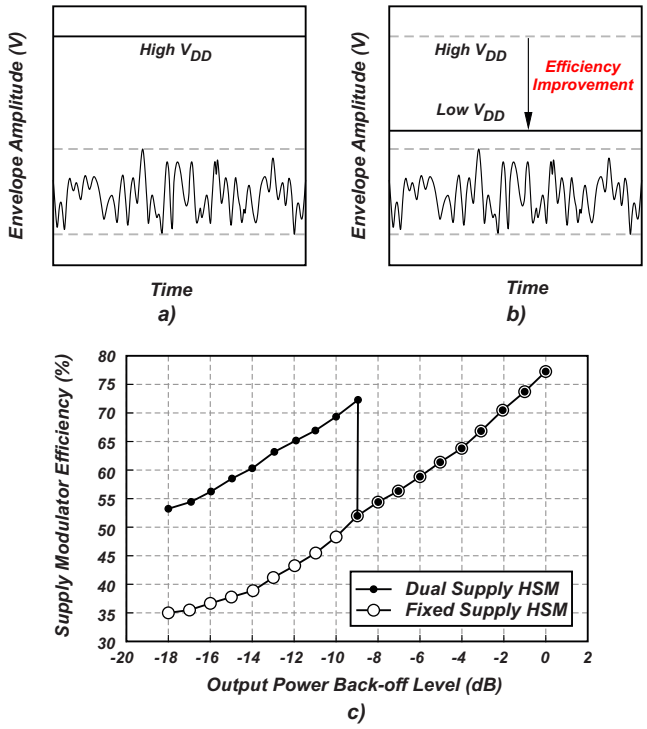


Figure 3.4: (a) Fixed Supply (b) Dual Supply Voltage at the Lower Power Levels, (c) Efficiency of Conventional (Fixed Supply) and Dual Supply HSM

when compared with an HSM using a single fixed-supply LA. The disadvantage of this architecture is that it requires two LAs working individually for low and high power modes, with extra control switches that add die/board area and circuitry.

The dual supply architecture provides only two supply voltage levels. But, this structure can be further expanded to change the LA's supply voltage to multiple levels based on tracking of the HSM's input envelope. Adding more levels increases the complexity of design and there is a minimum supply voltage required to provide sufficient headroom for proper operation of the LA's transistors. The work in [53] proposes a multiple supply HSM architecture that adjusts the DC supply of the LA adaptively with the average power of the envelope signal. As the bias state of the class-AB output stage determines the distortion in the LA, the class-AB is tied to a separate supply. As shown in Figure 3.5, the efficiency of the multiple supply HSM

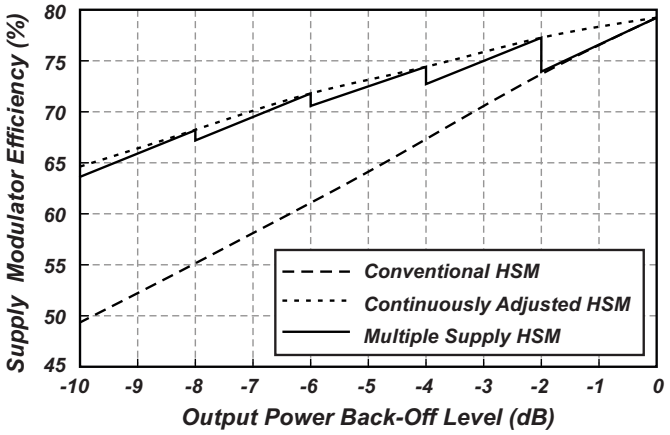


Figure 3.5: Efficiency of the Conventional and Multiple Supply HSM

is improved from 49.5% to 63.6% at 10 dB PBO. However, this architecture requires additional components like a low-pass filter for the envelope detection and a voltage-current converter. Moreover, the LA's adaptive supply needs to be realized using finite bandwidth supply modulators (e.g. an HSM), which was not implemented in work [53].

AC-Coupled HSM

An alternative method that enables a reduced LA supply voltage is an AC-coupled architecture. Most of the conventional HSM architectures are DC-coupled, i.e. the LA and the SA are directly connected to the HSM output (or PA load). But in AC-coupled designs, the output of the LA is isolated from the HSM output using an AC-coupling capacitor, as shown in Figure 3.27, and the supply voltage of the LA does not need to be as high as the peak envelope voltage [54]. Instead, the supply voltage just needs to provide the AC signal swing plus the LA's device headroom. By using a smaller V_{DD} for the LA, the value of P_{LA_bias} is reduced and PBO efficiency is improved. The detailed operation of the AC-coupled architecture is covered in

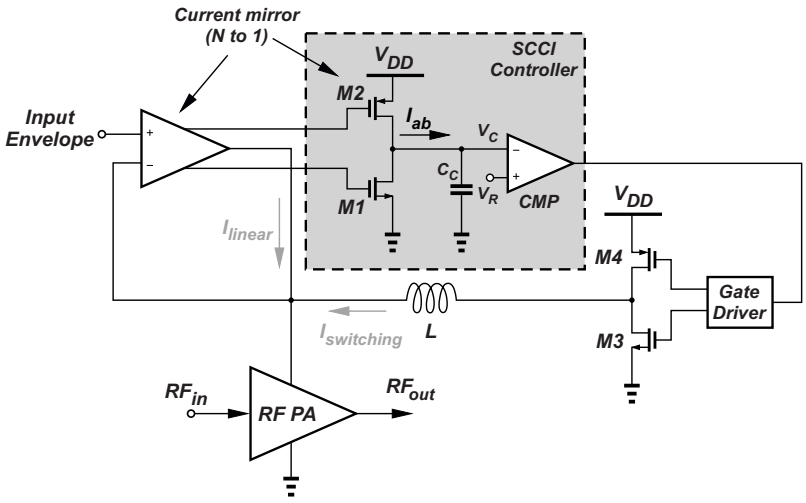


Figure 3.6: A *SCCI* HSM Architecture

Section 3.4.2 for more information.

SCCI HSM

In a HSM design, the LA is designed to provide only the compensating ripple created by the SA, ideally making its average current zero (excluding P_{LA_bias}). Typically, a SA can be more than 90% efficient [28] and a LA is around a maximum efficiency of 50% due to its class-AB output stage biasing. Therefore, it is desirable to have most of the HSM's load current provided by the SA in order to maximize efficiency. The LA provides ripple compensation with maximum and minimum current ripple values of I_H and I_L, as labeled in Figure 2.7(a). For the realistic case when $I_L = 0$ or $I_L \neq -I_H$, the average value of current ripple is a finite value. But for the ideal case when $I_L = -I_H$, the average value of the current ripple is zero and there is no flow of LA current to the load in the steady state.

The work in [55] introduces a Single-Capacitor Current-Integration ($SCCI$) HSM architecture, as shown in Figure 3.6. This architecture forces the average output

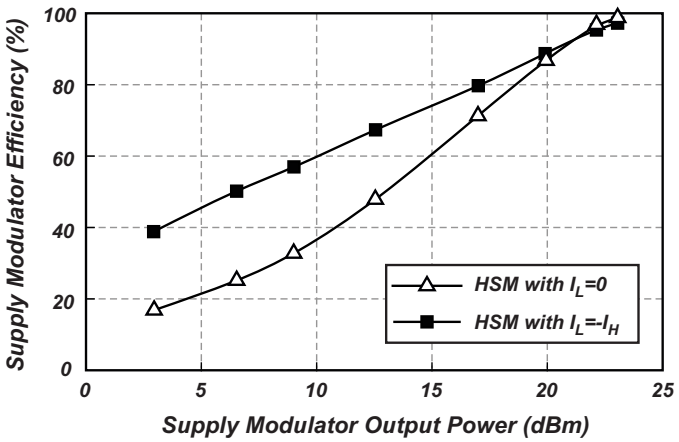


Figure 3.7: Conventional HSM Efficiency with I_L= 0 and with SCCI HSM $I_L = -I_H$

current from the LA to be around zero, hence reducing the LA's average output current and improving HSM efficiency. In the $SCCI$ design, a scaled version of the LA output current (I_{ab}) is used to modulate charge on the capacitor C_c to generate a control voltage V_c. This V_c is compared with a reference voltage (V_R) to regulate the switching loop. After each switching cycle, the voltage level of V_c returns to the same value, which forces the net charge accumulated on C_c during each cycle to zero. As a result, the average value of I_{ab} and the average output current from the LA are also approximately zero. It can be seen from Figure 3.7 that the efficiency of a HSM that uses $I_L = 0$ is improved by approximately 20% at 10 dB PBO when using a $SCCI$ architecture with $I_L = -\ I_H$ instead [55].

More efficiency enhancement is observed in the PBO region, as the LA's average current (along with P_{LA_bias}) becomes more dominant with the reduction of signal power. The trade-off of this architecture is the addition of an extra capacitor (C_c) in the main switching path, which can slow down the loop response thus reducing HSM speed, and the SCCI HSM can face stability challenges.

Optimizing Losses through DSP Control

Conventionally, most of the HSM designs use analog based hysteresis comparison for the controller block. The controller detects the direction of LA current by using a current/voltage sensing circuit. Once the LA sources or sinks large current, the controller regulates the charging state of the SA. The hysteresis controller is sensitive to the slew-rate difference between the SA output current ($I_{switching}$) and the desired load current (I_{load}). Figure 3.8(a) categorizes the current waveforms of HSM into 3 cases according to the current slew-rates of the SA (e.g. case-1, case-2, and case-3). In case-1 and case-2, the slew-rate difference between $I_{switching}$ and I_{load} is large, which results in high switching frequency of the SA and high tracking error, respectively. Due to high switching losses, the efficiency of the HSM decreases and due to mismatch in tracking, more I_{linear} current goes to the load, which is again detrimental to the HSM efficiency. But if the slew rates of $I_{switching}$ and I_{load} are close, the SA can provide more high-efficient current without increasing switching frequency, as shown in case-3. However, case-3 is very hard to maintain due to the irregular variations of the RF envelope. Also, the loop delay of the hysteresis controller (also the SA driver stage) makes the phase of $I_{switching}$ always lag behind that of I_{load}, which prevents the HSM from reaching the relatively ideal (or desirable) state of case-4.

The work in [56] proposes an open-loop digitally controlled HSM as a good alternative to close-looped hysteresis based HSM designs to improve efficiency while tracking wide bandwidth envelopes. Open-loop control does not suffer from the inherent lag of closed-loop control. Also, the digital processor can realize more flexible control methods. In the work, using an existing processors such as field-programmable gate array (FPGA) or digital signal processing (DSP), an extended efficiency model is put forward to systematically analyze the energy loss of a HSM from the aspect of current

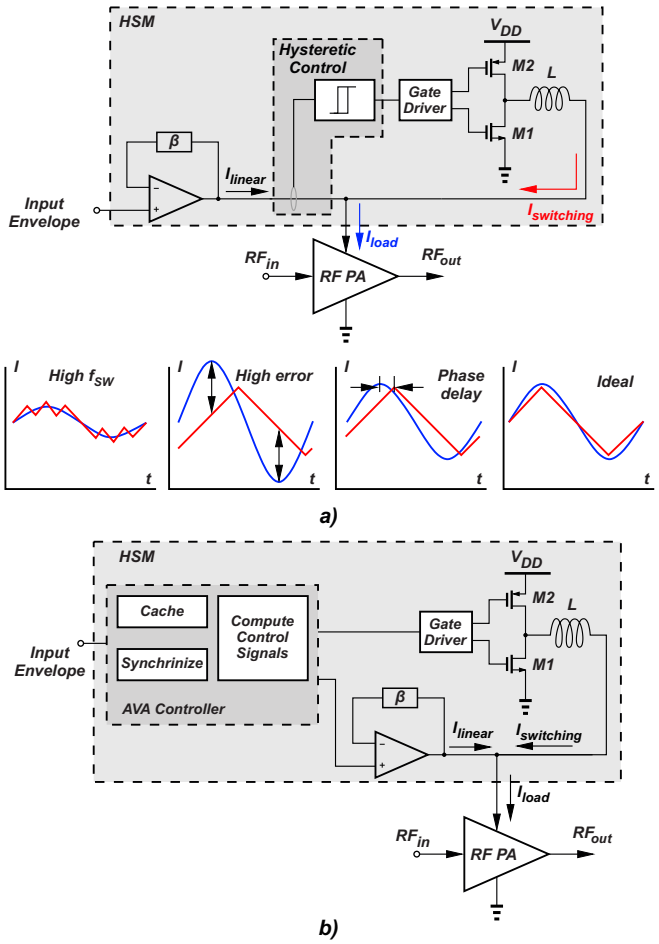


Figure 3.8: (a) Conventional Hysteretic Control Based HSM. Current Waveforms for Different SA Slew-rates Are Summarized into 3 Cases (Case-1 to Case-3). Case-4 Shows the Relatively Ideal Condition, but It Is Very Hard to Be Realized by Hysteretic Control Strategy. (b) Proposed AVA Based HSM That Aims to Realize Case-4

loss. The relationship between the SA output and RF signal envelope is analyzed by a short time Fourier Transform method. Thus, an average voltage alignment (AVA) algorithm is proposed to overcome the limitations of the close-looped controller. The AVA controller caches the signals in discrete segments, which is conducive to system-level SA control. The control method reduces power loss in the HSM by ignoring the phase limitation and small waveform fluctuations. In addition, a digital low pass filter

is applied to shape the input of the AVA, which helps to control the SA's switching frequency while tracking different envelope bandwidths. The measurement results for the proposed technique show the tracking bandwidth from 10 MHz up to 200 MHz. The HSM achieves an efficiency improvement of 20% under a maximum PAPR condition of ∼9 dB with a maximum switching frequency of 10 MHz compared with the conventional hysteresis comparison controller block.

The recent work in [57] uses a Viterbi-like Trellis search (TS) DSP algorithm to find the optimal switching sequence for the SA in the HSM, thus lowering RMS error current in the LA and minimizing SA switching frequency. Using the proposed TS search for 20 MHz envelope tracking, the measurement results show that the average LA current drops by 27% and TS improves efficiency of the HSM by 3% (from 71.2% to 74.2%) at 6 dB back-off, when compared with a conventional hysteresis comparison controller block. Furthermore the work in [58] demonstrates an open-loop digitally control HSM with just a SA (without a LA). The SA controller implements envelope shaping and transient filtering processes to reduce the envelope bandwidth and corresponding SA switching frequency.

Since, the controller algorithm can be implemented in a baseband modem, the proposed techniques of digitally optimizing the HSM losses shows promise for tracking wideband envelopes with improved DSP and machine-learning algorithms.

3.2 Speed Improvements in HSM

Increasing communication data-rates requires the use of wideband envelopes. Therefore, HSM designs are continuously increasing in speed to track the increasing envelope signal bandwidths. In order to track high frequency (fast varying) envelopes, the speed of the transistors in a HSM should be maximized. As there is a trend towards CMOS scaling, the transition frequency (f_T) of a transistor can be increased by us-

ing shorter channel length processes, but this is not always beneficial to the overall ET-PA system or within the designer's control. Therefore, this Section discusses the various architectures that have been proposed to maximize HSM speed.

3.2.1 LA Bandwidth Enhancement

The term bandwidth is a small signal phenomenon (calculated around a DC operating point) and signifies how fast an amplifier can track a signal. As discussed in Section 2.1, the input envelope consists of fundamental and multiple harmonics, which requires bandwidth of the LA (BW_{lin}) to be higher than that of the envelope (BW_{in}). In order to demonstrate the effect of LA bandwidth on tracking performance of a modulated signal, a simulation setup with a test LTE signal of 100 MHz bandwidth is chosen for a case study. The LA's tracking performance for different bandwidths is observed from Figure 3.9(a), (b) and (c). The simulation results show that the LA needs to demonstrate BW_{lin} of at least three times the BW_{in} to track an envelope signal with high accuracy. Although high accuracy or minimal tracking error is desired to maximize ET-PA efficiency, the value of BW_{lin} also depends upon the linearity requirements for the HSM.

The LA is typically used in a closed-loop configuration (in Fig. 2.5), therefore research efforts have been made to improve its open-loop unity gain bandwidth (UGB). This is because the 3-dB bandwidth of the LA's closed-loop is equal to the UGB of the open-loop LA (assuming a single-pole system). The UGB of a LA depends upon the transconductance (G_m) of the input devices [168][169] and the load capacitor (C_L), as:

$$UGB = \frac{G_m}{2\pi C_L} \tag{3.3}$$

As the value of C_L is generally decided by the PA load, the magnitude of G_m (from equation3.3) should be increased in order to achieve a higher UGB. Different

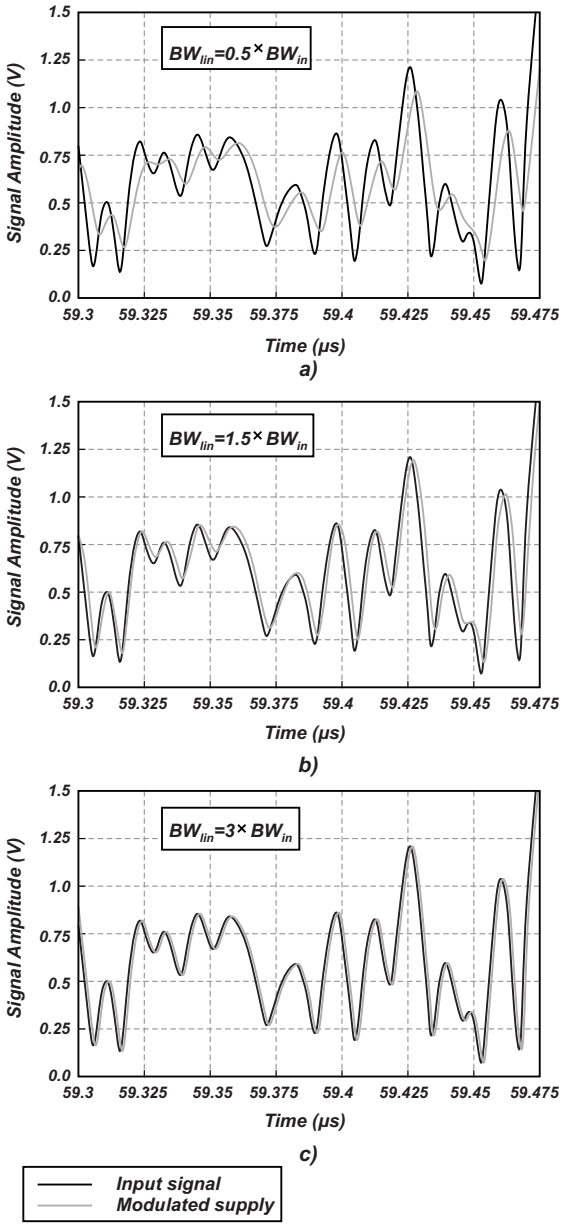


Figure 3.9: Transient Waveforms to Show Tracking of an LTE 100 MHz Envelope for LA Bandwidth of (a) 0.5× (B) 1.5× (C) 3× the Signal Bandwidth.

methods [59][60][61][62] are proposed in literature to boost the value of G_m, such as G_m boosting, cross-coupled structure employing positive feedback, current recycling structure, dual-path crossover current-reuse mechanism, etc. In case of a multi-pole

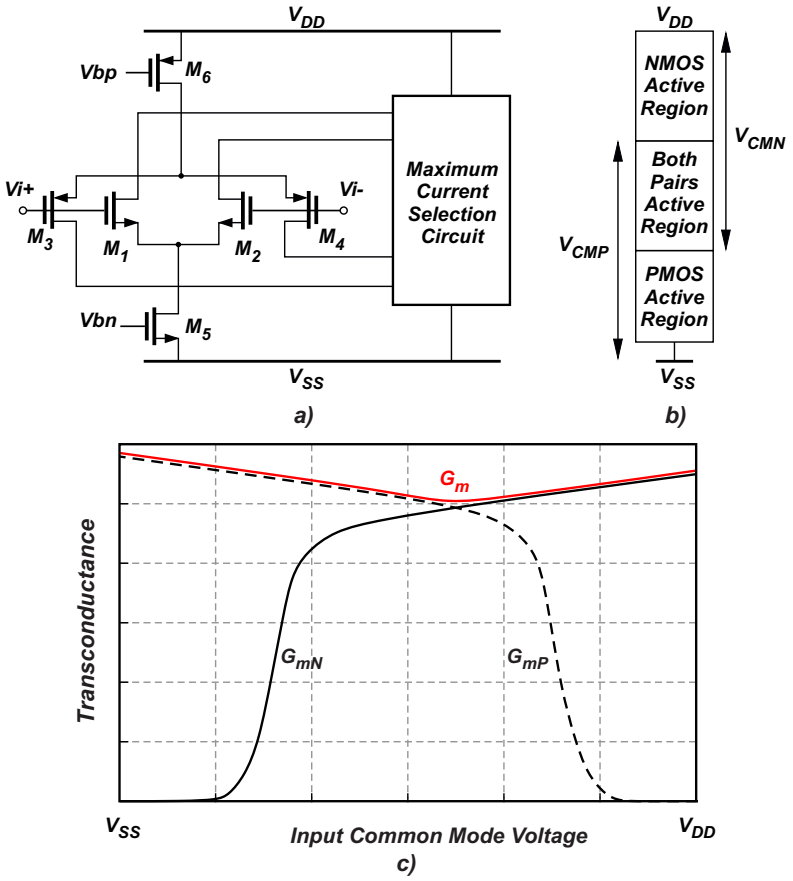


Figure 3.10: (a) Maximum Current Selection Circuit, (b) Active Region of Both PMOS and NMOS, (c) Effective G_m Value (Almost Constant).

system, the non-dominant poles can be pushed to higher frequencies (by consuming more current) or zeroes can be inserted (pole-zero cancellation [70]) in order to increase the UGB value.

As the input signal envelope spans multiple DC operating points, it is important for the LA to maintain a high bandwidth over the entire DC operating range. Usually, a LA is designed with both pmos and nmos input pair in order to process the entire envelope range (from supply rail to ground). Since both pmos and nmos input pairs show different transconductance values depending upon the operating point, the total value of the G_m doesn't remain constant and hence, the LA's UGB varies significantly

(from equation 3.3). Therefore, there have been different techniques proposed in the literature to force the G_m of the LA to remain almost constant over signal swing [63]. The work in [47] adopts one of these constant G_m techniques by using a maximum-current selection circuit as shown in Figure 3.10(a). This circuit always selects the maximum of the pmos or nmos currents at any given DC operating point. As the maximum current value remains almost constant, this technique helps in reducing the variation in the overall G_m (dependent on current), as demonstrated in Figure 3.10(b) and (c), and therefore achieves constant UGB over the entire envelope.

3.2.2 LA Slew-Rate Enhancement

The term slew-rate for an LA is a large signal phenomenon (covers multiple DC operating points) that signifies how fast an amplifier can track transient changes [64]. It is an important attribute of LA speed, as the envelope signal is usually a transient waveform whose value changes over time. Figure 3.11 shows the trend of slew-rate for different modulation bandwidths of an LTE signal, illustrating that the slew-rate requirements go up with higher modulation bandwidth. In a LA, the expression for the slew-rate (SR) is given by:

$$SR = \frac{2I_{Tail}}{C_L} \tag{3.4}$$

where I_{Tail} is the tail current of the input stage, and C_L is the load capacitor. In order to increase the slew-rate, the value of I_{Tail} should be increased. But, it is important to note that the increase in I_{Tail} value should happen only in the case of transient change and not at DC in order to avoid an increase in P_{LA_bias} and prevent efficiency degradation.

To improve the slew-rate in a LA, the most popular technique is addition of an auxiliary slew-rate enhancement (SRE) circuit in parallel with the main LA. The

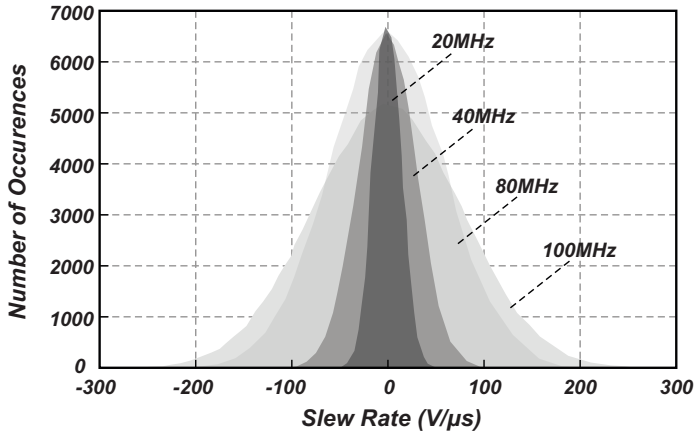


Figure 3.11: Slew-rate Trend for Different Bandwidths of an LTE Signal

SRE circuit consists of a large signal detector (LSD) to detect a transient change and additional mechanism to increase the value of I_{Tail}. The SRE does not affect nominal operation of the LA and does not significantly add to the P_{LA_bias}. In conventional LA designs, the SRE circuit is added in parallel to the input stage to change the value of tail current, as shown in Figure 3.12(a). But this requires a large amount of current (from another branch/circuit) to increase I_{Tail} and there is a delay (due to multiple stages in the LA) to see the increased current effect from input to the output.

To avoid additional circuitry for providing current (to increase I_{Tail}) and reduce input to output delay, a better alternative is to add the SRE circuit at the gate of the output class-AB stage, as shown in Figure 3.12(b). The SRE circuit senses the voltage difference between the inputs during transients through the LSD and adjusts the bias of the class-AB pair adaptively. As the class-AB transistors demonstrate a high value of transconductance, they can respond to the input gate voltage change faster by sourcing/sinking the required amount of current to cancel the SA's current ripple. The work in [65] implements an LA with a slew-rate that is enhanced from 178 $V/\mu s$ to 325 $V/\mu s$ and from -169 $V/\mu s$ to -307 $V/\mu s$ after adding the SRE circuit.

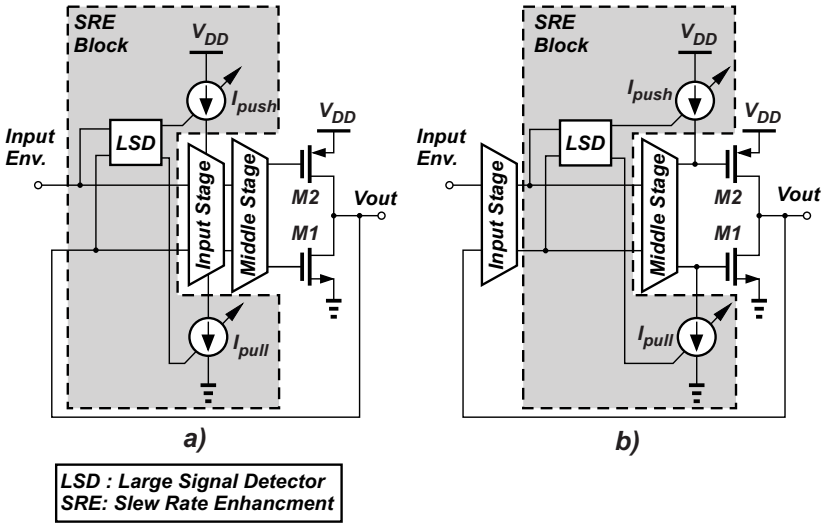


Figure 3.12: SRE Circuit Added (a) at the Input Stage and (b) at the Output Class-AB Stage

Another work in [66] reports the enhancement in the positive and negative slew-rate of their designed LA by 86.8% and 75.3%, respectively.

3.2.3 SA Slew-Rate Enhancement

The slew-rate in a SA is determined by the slope of the load current, which depends on the value of the off-chip inductor. Typically, a SA uses a single inductor in a HSM, whose value is selected based on SA design requirements for bandwidth and ripple. Therefore, the SA is slew-rate limited and cannot provide the current instantaneously to track the fast transient changes. To overcome this challenge, multiple SAs (with different inductor values) can be used, and the slew-rate can be varied based upon the input envelope transients using an additional control knob. The work in [67] introduces a dual switch HSM architecture given in Figure 3.13, which uses a LA, two SAs (fast and slow) with inductors L_1, L_2 respectively and $L_1 < L_2$, and an adaptive slew-rate controller. The current in the LA is monitored using four different controller switch states and both SA currents ($I_{switching1}$ and $I_{switching2}$) are adaptively

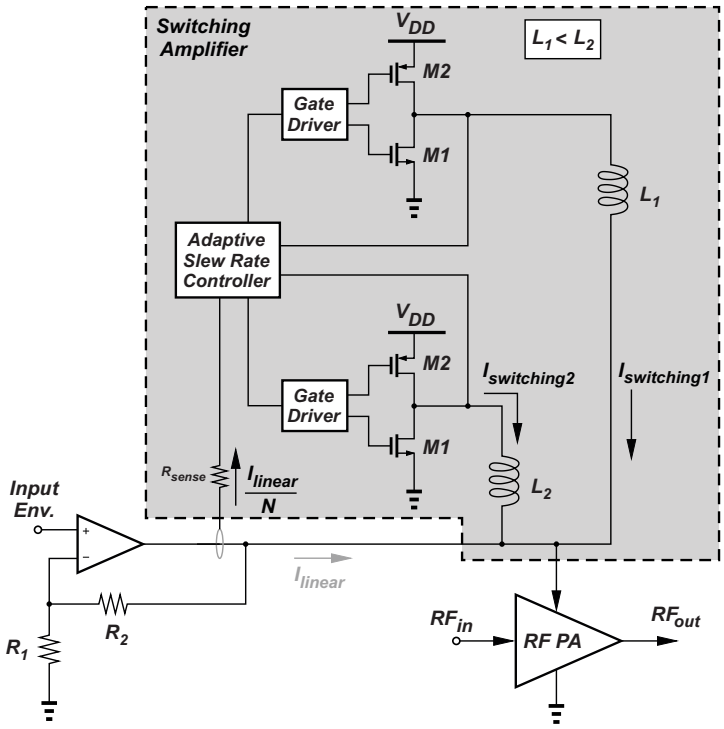


Figure 3.13: Slew-rate Enhancement Using Dual Switch HSM Architecture

changed, which improves the SA slew-rate and enables faster tracking. The dual switch architecture can be expanded to multi-switch architectures, with the trade-off of adding multiple SAs and extra die-area/board space.

Slew-rate enhancement using fast and slow SAs can also be implemented, as the work in [68] implements a topology where the low frequency portion of the output power is provided by a standalone slow buck-boost SA and the high frequency portion of the output power is provided by a multi-level SA. The slow buck-boost SA uses an inductance L_{slow} of 4.7 μH and operates from 1.9 MHz to 7 MHz (2 MHz typical), while the fast multi-level SA uses an inductance L_{fast} of 22 nH and its switching frequency can reach up to 140 MHz (80 MHz typical). Another extension of the SA slew-rate enhancement concept is implemented in [69], where a fast SA and a slow SA are implemented in the same design for tracking a 5G NR envelope signal

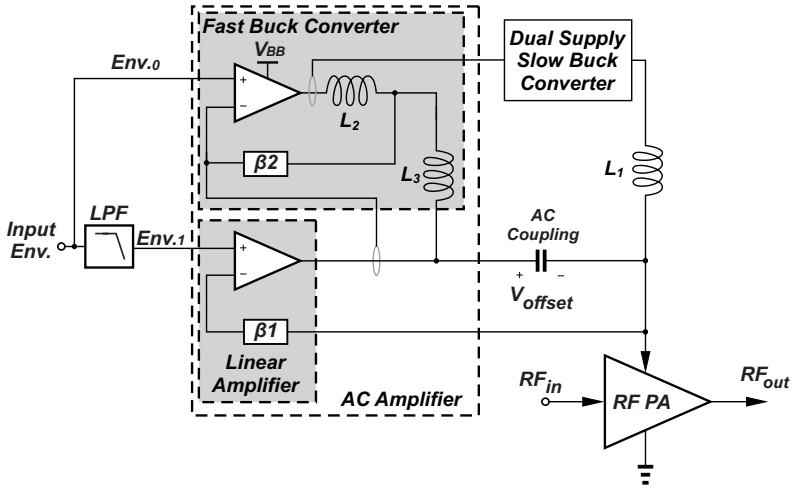


Figure 3.14: A Simplified Version of the HSM Architecture with LA Bandwidth and SA Slew-rate Enhancement

of bandwidth of 40 MHz. The slow SA is implemented using a PWM control and a larger inductor is used (as compared to the fast SA) to provide 60% of the total power to the load. The fast SA is implemented using Hysteretic control and two smaller inductors are used in a multi-phase configuration to provide the remaining 40% of the total power to the load. The fast SA inductors are sized to ensure that the HSM bandwidth is higher than the tracking signal's bandwidth and to provide correct phasing between the two inductor current paths.

3.2.4 Combined LA Bandwidth and SA Slew-Rate Enhancement

As discussed above in Section 3.2.1 and 3.2.3, there are different circuit level techniques in literature to make speed improvements in a HSM: increase LA bandwidth and increase SA slew-rate. In order to track high bandwidth envelopes for sub-6 GHz 5G NR applications, a balanced combination of these two techniques is used. The work in [70] proposes a HSM to track 100 MHz envelope bandwidths, in which a dual-supply buck and an AC amplifier operate jointly to provide the modulated supply

voltage to the RF PA, as illustrated in Figure 3.14. The AC amplifier supports three operating modes according to the signal bandwidth and communications standard: 1) For low bandwidth, a feedforward fast-switching (FFFS) buck converter is used, 2) For medium bandwidth, the FFFS buck converter assisted by a LA is used, and 3) For large bandwidth, a voltage-buffer-compensated (VBC) class-AB LA is used. The technique for enhancing bandwidth using a VBC class-AB LA and enhancing slew-rate using a fast-switching SA is explained in the work of [70].

A similar implementation can also be found in [71] that proposes a HSM to track 130 MHz of envelope bandwidth. In the ET operation, there are 4 modes according to the required bandwidth and output power; LBLP (low bandwidth and low power), LBHP (low bandwidth and high power), HBLP (high bandwidth and low power), HBHP (high bandwidth and high power). Depending upon the bandwidth, different circuitry is activated. The operational details for these modes is found in [71]. All of the above mentioned high speed tracking techniques come at the cost of increased design complexity and extra die-area/board space.

3.2.5 Reducing Controller Delay

Most recent works in improving HSM speed focus on improving the speed of both LA and SA. But, little attention has been paid to the controller block, which contributes to a finite propagation delay. For narrowband applications (e.g., low-bandwidth signals such as EDGE, CDMA envelopes) whose HSM switching frequency is low, the effect of controller delay can be neglected because the switching period is much longer than the delay. But for wideband applications (e.g., high-bandwidth signals such as LTE, 5G-NR envelopes), the switching period becomes comparable to the controller delay. Due to this significant delay, the SA cannot respond quickly to fast signal transitions, which results in increased current flow from the LA (low effi-

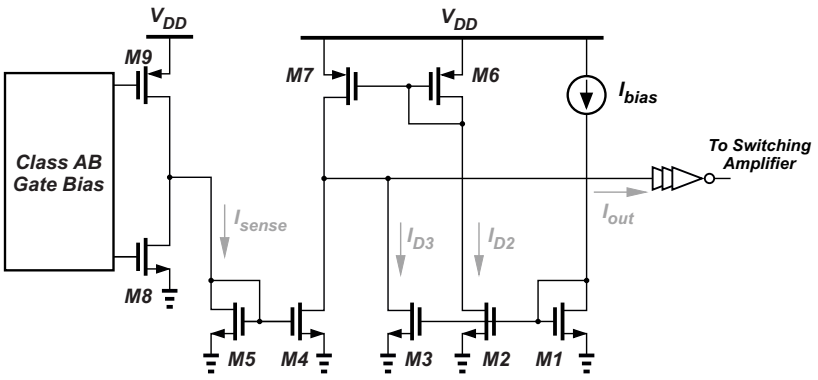


Figure 3.15: A Simplified Version of the Delay-based Hysteretic Controller

ciency) to the load (from Figure 2.7(d)). This leads to HSM performance degradation in terms of efficiency and output power.

As explained in Section 2.3.2, a HSM works by either PWM or hysteretic control. In PWM control, the switching loop bandwidth is limited to a fraction of its switching frequency. But in the case of hysteretic control, the switching loop bandwidth can be as high as the switching frequency. Therefore, most of the existing HSM designs use hysteretic control to achieve faster loop response that is suitable for tracking wideband envelopes. For a hysteretic controller with upper (I_U) and lower (I_L) current limit and hysteresis threshold currents ($\pm I_T$), the more accurate controller limits, (I'_U) and (I'_L), that include the intrinsic controller delay (t_D) can be expressed as [43]:

$$I'_U = +I_T + \left(\frac{V_{DD} - V_{out}}{L_o}\right) \times t_D \tag{3.5a}$$

$$I'_L = -I_T + \left(\frac{0 - V_{out}}{L_o}\right) \times t_D \tag{3.5b}$$

$$I_{HYS} = I'_U - I'_L = 2I_T + \left(\frac{V_{DD}}{L_o}\right) \times t_D \tag{3.6}$$

where V_{out}, L_o and I_{HYS} are the output voltage, external inductor, and hysteresis window, respectively. The comparison time in the controller, which is dictated by the

value of I_{HYS}, leads to a finite delay between the LA and the SA. Therefore, various works in literature focus on reducing the magnitude of I_{HYS}. As can be seen from equation 3.6, there are mainly two ways to reduce the delay: 1) by reducing the value of intrinsic controller delay, t_D, or 2) by reducing the value of threshold current, I_T. A conventional hysteretic controller works in voltage-mode that involves voltage sensing across a series resistor [72]. This increases the loop delay and output impedance of the class-AB buffer. Alternatively, a current-mode hysteretic controller can be used, which demonstrates less t_D because signal mirroring and comparison is much faster in the current domain. The work in [73] proposes a current-mode hysteretic controller that enables the SA to source/sink current in synchronization with the fast input envelope transients of 20/40 MHz bandwidth for a 802.11n WLAN transceiver.

The second method for reducing delay focuses on reducing the value of hysteresis threshold currents ($\pm I_T$) in order to the reduce the overall magnitude of I_{HYS}. Since I_T is a design parameter that can be set through internal or external control, its value can be made smaller at the cost of high switching frequency. The work in [43] proposes the hysteretic controller shown in Figure 3.15 for tracking LTE signals up to 40 MHz bandwidth. With this structure, there is no requirement of generating the hysteresis reference currents, thus making $I_T \approx 0$, and hence reducing the value of I_{HYS}. There is a just one reference signal (I_{bias}) in the design along with an input signal (I_{sense}), which is a fraction of the output current from the LA's class-AB stage. Instead of comparing I_{sense} within a hysteresis window of $\pm I_T$ as typically done in conventional controller designs [23], the proposed structure of Fig. 3.15 compares (I_{sense} + I_{bias}) with I_{bias} through a basic current comparison, which significantly reduces the delay. Another work in [74] introduces a programmable hysteretic controller that uses an external voltage to control the value of I_T, and hence I_{HYS}. The control voltage is varied to change the value of I_T depending upon the input signal's bandwidth.

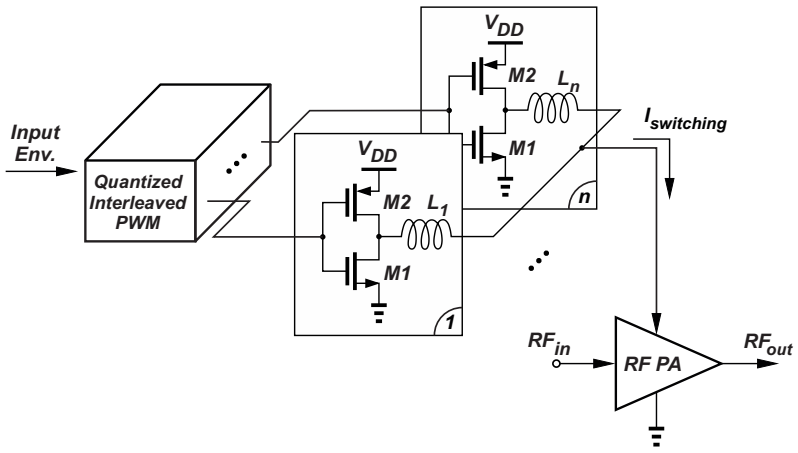


Figure 3.16: A Multi-switcher Architecture (Digital Tracking)

3.2.6 Multi-Switcher Topology (Digital Tracking)

The conventional HSM architecture operates in an analog fashion, which generally supports carrier channel bandwidths for the 5G Frequency Range 1 ($FR1$) standard up to 100 MHz [75]. In order to support the 5G $FR2$ standard (or mmWave bands), there are two main design bottlenecks. First, it is difficult to design a LA that can support higher channel bandwidths (typically more than 100 MHz) due to stability challenges and power consumption. Second, the switching losses increase significantly in the SA due to the requirement for high switching frequency.

In order to remove the analog limitations of a HSM, the SM can potentially be operated with a multi-switcher topology in a digital manner [76]. A multi-switcher topology [77] typically uses multiple switches (or power stages) connected together in parallel as shown in Figure 3.16, and avoids the use of a LA. The switches are controlled digitally by a pulse-width modulated (PWM) signal [78] and operate in an interleaved manner. With interleaving, the switching rate of each switcher is reduced by the number of interleaved stages, as illustrated in Figure 3.17. Furthermore, the digital tracking is less sensitive to the RF-Envelope path delay mismatch [79].

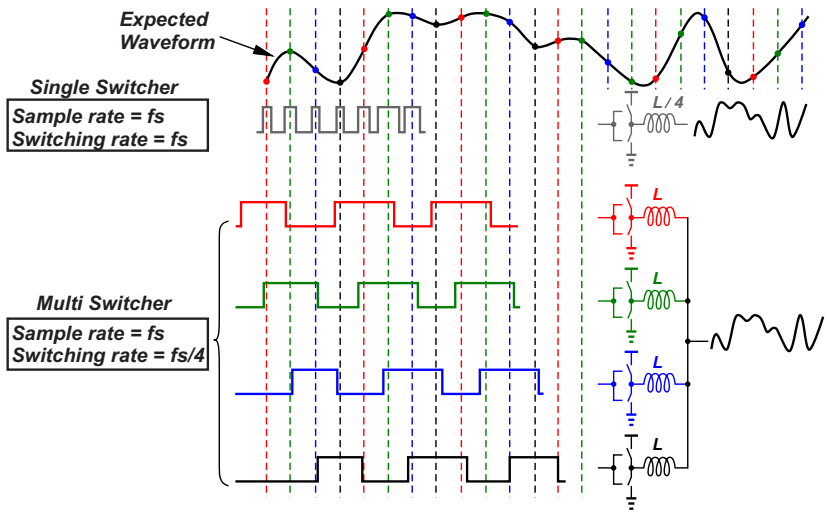


Figure 3.17: Transient Waveforms of Single and Multi-switcher Topologies

Hence, this topology can potentially lead to tracking of wideband envelopes. Multiple improved techniques like zero-voltage switching [80] and soft switching [81] can also be employed with the power stages to further reduce the switching losses.

To avoid the use of multiple power stages and inductors in the digital tracking topology, several improvements have been made. A recent work [79] in literature proposes a SM using a multi-switcher/digital tracking topology to track 200 MHz of channel bandwidth. The proposed design employs a switched-capacitor voltage divider with level-selection switches (which can be controlled at the system-level) to generate six uniform voltage levels for the envelope supply voltage. This digital tracking supports wider bandwidth than the traditional analog HSM amplifier because it dynamically changes a supply voltage level by connecting one of multiple voltages generated by the switched-capacitor voltage divider to the output via switches [82].

3.2.7 System Level / Software Techniques

The above proposed methods that improve speed by enhancing bandwidth, enhancing slew-rate, or reducing controller delay add additional challenges to the orig-

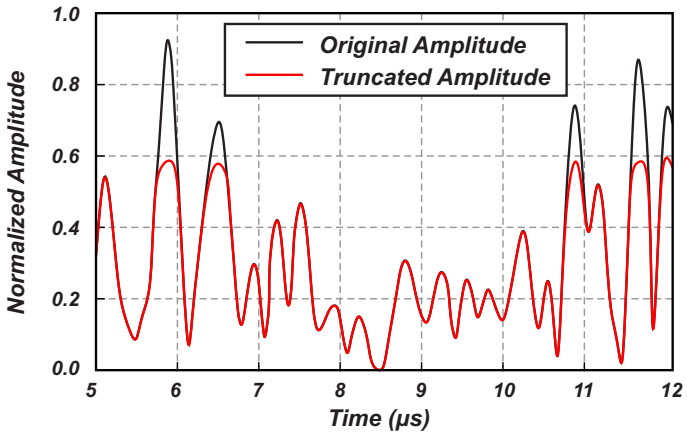


Figure 3.18: Time Domain Waveform of the WCDMA Signal and Its Truncated (or De-crested) Version

inal HSM design. The improved topologies/architectures increase complexity of the circuit, introduce stability challenges [83], increase switching frequency, add to static DC power consumption, and/or increase the physical size. On the other hand, system level/software techniques that perform digital signal processing on the input envelope signal require minimal hardware overhead. With these proposed techniques, the bandwidth, slew-rate, and delay requirements are significantly relaxed with some compromise on the ET performance. There are three popular input signal processing techniques, namely: PAPR reduction, bandwidth reduction, and slew-rate reduction of the input envelope. Each of these techniques is discussed below.

The first technique focuses on PAPR or crest-factor reduction of the input envelope using various algorithms [84] such as: clipping and filtering, selective mapping, partial transmit sequence, linear block coding, and peak insertion. These methods generate a de-crested version of the input envelope signal, which essentially reduces the peak of the input envelope above a certain voltage level (decided by design requirements). Notably, the work in [85] introduces an algorithm that generates a de-cresting function

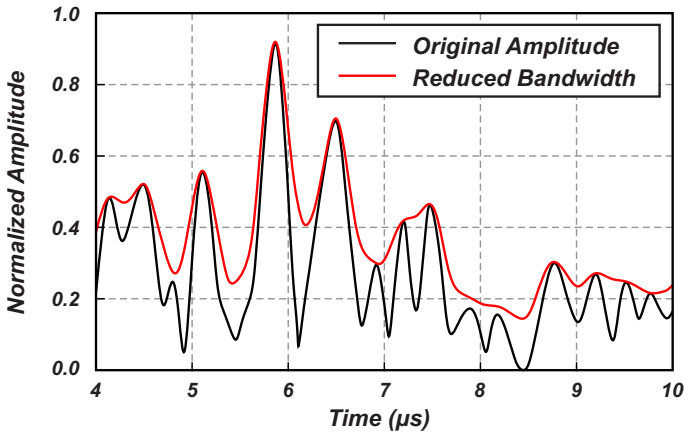


Figure 3.19: Time Domain Waveform of the WCDMA Signal Before and after Bandwidth Reduction

for the RF input signal to reduce the PAPR of an input WCDMA envelope from 7.6 dB to 5.2 dB with minimal impact on its linearity and efficiency performance. Figure 3.18 shows the time domain waveform of a WCDMA signal before and after this PAPR reduction.

The second technique primarily focuses on reducing the bandwidth of the input envelope using different algorithms such as: low-pass finite impulse response filtering, power envelope tracking [86], and elimination of drastically changing peaks [87]. These methods essentially generate a slow varying version of the actual envelope and feed it to the PA supply. With a slower varying supply signal, the PA's efficiency is affected, but the design constraints on the HSM are more relaxed. The work in [88] introduces a filtering technique where the envelope signal is low pass-filtered and subtracted from itself to derive a difference signal, which is then rectified. The rectified residue signal is filtered and then added back to the filtered envelope signal. This technique reduces bandwidth of the original envelope signal from 20 MHz to 5 MHz. Figure 3.19 shows the time domain waveform of this WCDMA signal before and after bandwidth reduction.

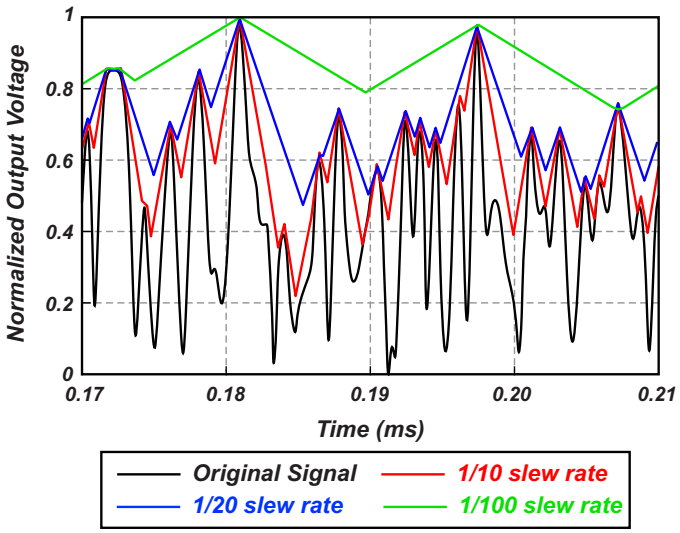


Figure 3.20: Envelope Signal with Different Slew-rates

The third technique focuses on generating a slew-rate limited version of the original envelope to control the PA's dynamic supply. Multiple algorithms [89][90][91] have been proposed to reduce the input envelope's slew-rate. The work in [92] generates several envelopes with reduced slew-rate (1/10, 1/20 and 1/100 of the original signal), as shown in Figure 3.20, using an algorithm that re-samples the original envelope, $E(n)$, at a lower rate of F_S defined by the designer. The slew-rate limited instantaneous envelope, $SL\_E(n)$, can be defined as:

$$SL\_E(n) = \left| \frac{E(n) - E(n-1)}{T_S} \right| . V_{MAX} \tag{3.7a}$$

$$= |\Delta E(n)| . F_S . V_{MAX} \tag{3.7b}$$

where $E(n)$ is the input envelope, V_{MAX} is the maximum voltage value at the HSM output that corresponds to the maximum desired transistor drain bias, and T_S and F_S are the sampling time and sampling frequency, respectively. From equation 3.7(a) and (b), the resulting slew rate $SL\_E(n)$ is reduced from the original envelope signal's slew rate and dependent upon the sampling frequency F_S (which can be set externally).

3.3 Linearity Improvement in HSM

A HSM needs to demonstrate high linearity at its output, as any ripple component injected to the PA from the power supply mixes with the RF carrier and is upconverted to the PA's output signal sideband frequencies (as was illustrated in Figure 2.2). The magnitude of the sidebands due to PA supply ripple can be calculated from equation 2.3. The work in [25] demonstrated through measurements that the supply ripple component present at a frequency of 41 MHz was upconverted to the PA's output signal sidebands around the RF carrier frequency of 2.14 GHz, as shown in the PA's output signal power spectral density (PSD) plot of Figure 3.21. Figure 3.21 also demonstrates that increasing the PA's supply ripple magnitude increases the magnitude of the sidebands in the PSD. If the PA demonstrates insufficient power supply rejection, the ripple from the HSM is likely to cause violations of the transmit spectral mask [93].

The ripple content at the output of a HSM can be reduced by using a higher order output LC filter. But, the use of such filters limits the maximum HSM bandwidth of operation and is not suitable for wideband applications. The ripple voltage at the output node (V_{out}) of the HSM can be expressed as:

$$V_{out\_ripple}(s) = I_{ripple}(s) \times (Z_{out}(s) \parallel R_{PA}) \tag{3.8}$$

where V_{out_ripple}, I_{ripple}, Z_{out} and R_{PA} represent the output ripple voltage, switching ripple current, closed loop output impedance of the LA, and PA load resistance, respectively. As seen from equation 3.8, the value of V_{out_ripple} can be reduced by two methods. First, the magnitude of I_{ripple} can be minimized by reducing the amount of generated ripple content. Second, the magnitude of the parallel combination of $Z_{out}(s)$ and R_{PA} can be decreased by providing ripple cancellation from the LA.

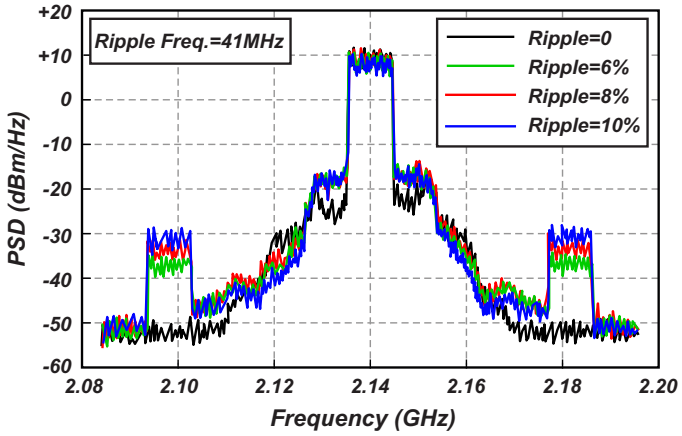


Figure 3.21: Effect of Supply Ripple (HSM Output) on the PA's PSD

Different methods for reducing the HSM output voltage ripple are explained in the following subsections.

3.3.1 Minimizing Current Ripple (I_{ripple})

The SA is responsible for providing the average supply current to the load. This current also includes switching ripple. The linearity of a HSM can be improved if the inductor's ripple current I_{ripple} from the SA is reduced. This can be achieved by adopting one of the advanced SA topologies discussed below:

Multi-Level SA

In the first topology, a multi-level converter design is used for the SA, as shown in Figure 3.22(a). The basic idea behind the multi-level converter is to reduce the inductor current ripple by reducing the voltage swing across the inductor (or at the switching node V_{sw}). The magnitude of maximum current ripple for a multi-level converter ($I_{max\_ripple-n}$) compared to the maximum current ripple ($I_{max\_ripple-2}$) for a

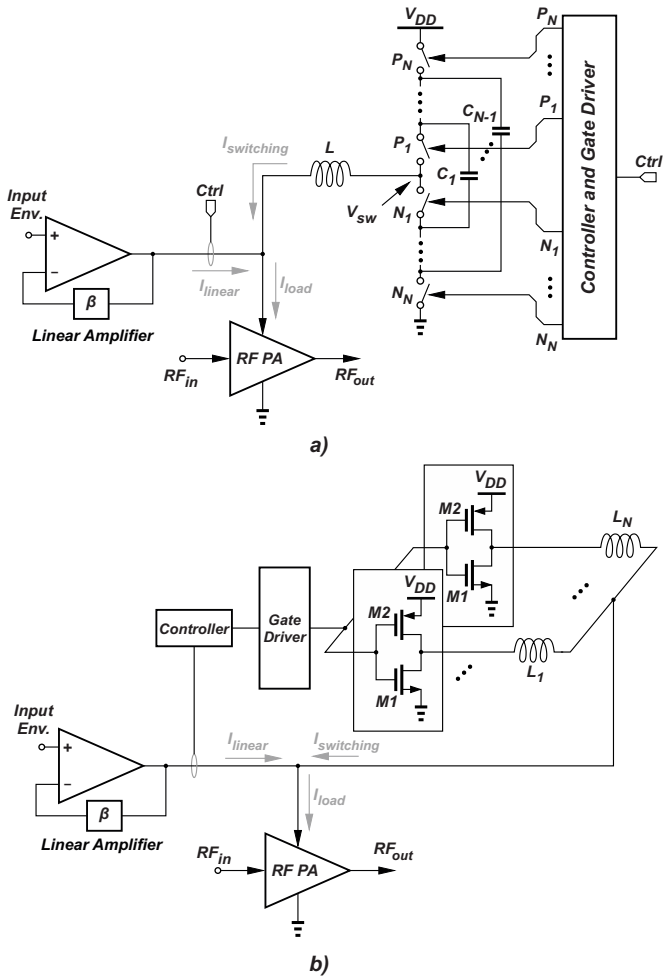


Figure 3.22: A HSM with (a) Multi-level, and (b) Multi-phase SA Topologies

basic two-level converter is described by the following relationship:

$$I_{max\_ripple-n} = \frac{1}{(n-1)^2}\, I_{max\_ripple-2} \tag{3.9}$$

where 'n' represents the number of switching levels. Due to its low output ripple (or noise), a multi-level SA topology is used for improving linearity in ET-PA systems [68][94][95].

The most commonly used multi-level SA topology is a three-level converter, as previously shown in Figure 3.2. A complementary signal drives the outer devices, M1 and M2, with duty cycle D = V_{OUT}/V_{DD}, similar to the two-level converter. A

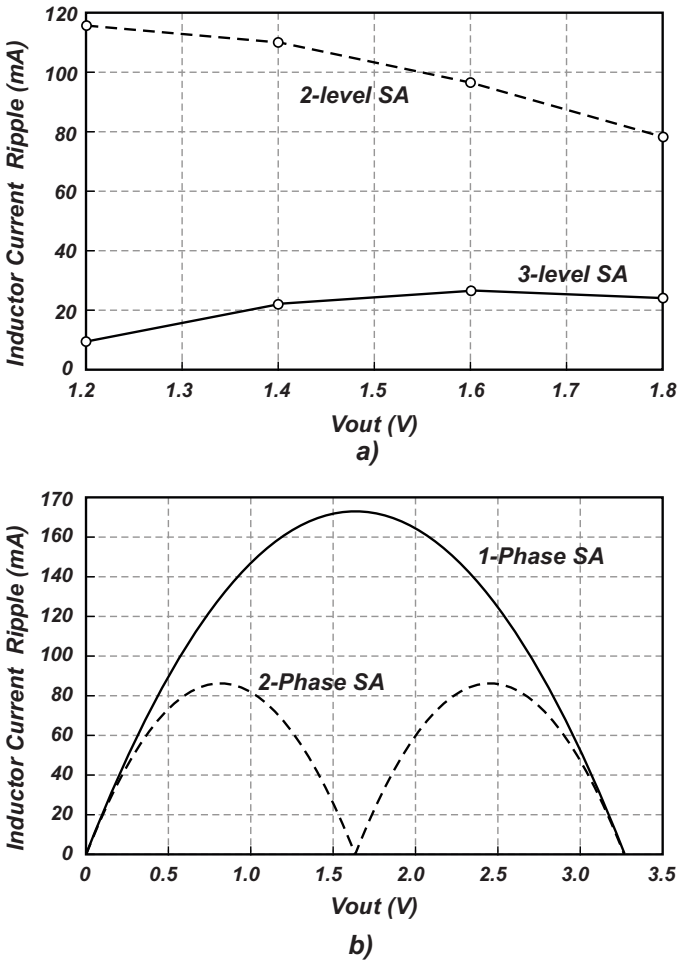


Figure 3.23: Current Ripple Reduction with (a) Three-level, and (b) Two-phase SA Topologies

second complementary signal of equal duty cycle drives the inner devices, M3 and M4, but is 180 degrees out-of-phase from the outer device's signal. By keeping the flying capacitor, C_F, balanced at $V_{DD}/2$, the V_{sw} switch node alternates between V_{DD}, $V_{DD}/2$, and 0 (or ground); hence the term "three-level." In three-level operation, when V_{out} is smaller than $V_{DD}/2$, the V_{sw} node switches between either ground and $V_{DD}/2$, and when V_{out} is larger than $V_{DD}/2$, the V_{sw} node switches between $V_{DD}/2$ and V_{DD}. The smaller step of V_{sw} voltage reduces the slope of the inductor current ripple. Moreover, the frequency of the inductor current is twice of the switching frequency.

As a result, the inductor current ripple of the three-level topology is smaller than one-fourth of the standard two-level topology with the same LC value [48]. A detailed description of the charging/discharging for different duty cycle ratios and control logic to always regulate $V_{DD}/2$ across the flying capacitor is given in [96][97]. The work in [98] adopts a three-level SA converter topology and demonstrates a reduction of more than 65% in I_{ripple} (as compared to a two-level SA) over the HSM output voltage range, as shown in the measured I_{ripple} results in Figure 3.23(a).

Multi-Phase SA

In the second topology, a multi-phase converter design is used to implement the SA, as described by the diagram in Figure 3.22(b). In a conventional single-phase SA converter, all of the load current (along with I_{ripple}) is provided through a single inductor. Whereas in the case of a multi-phase SA converter, the total load current is split between multiple inductors. Based on alignment between the multiple phases, ripple cancellation can be achieved [49] to minimize the effective magnitude of I_{ripple}. To achieve this operation, a current-sharing control circuit is needed to balance the phase currents in the multiple inductor paths. The most commonly used multi-phase topology is a two-phase SA converter. The work in [33] adopts a two-phase SA converter topology and demonstrates a reduction of more than 50% in I_{ripple} (as compared to single-phase SA) over the HSM output voltage range as shown in the measured I_{ripple} results in Figure 3.23(b).

Combined Multi-Level and Multi-Phase SA

As discussed in previous subsections, there have been works which implement advanced SA topologies like multi-level and multi-phase. But to the best of the authors knowledge, works that implement both multi-level and multi-phase together have not

been well explored for CMOS HSMs. Although this paper focuses on HSM implementations in CMOS technology, there are notable works that use discrete/off-the-shelf components and employ both multi-level and multi-phase in the same design as well as some current ripple reduction techniques in the SA [99][100][101][102]. However, it is important to note that these works implement the supply modulator as a SA (not within a HSM architecture) and focus on improving multiple performance parameters like efficiency, speed, linearity etc. [103]. The devices are driven by pulse-width modulated (PWM) signals, but due to high switching ripple at the output (because there is no ripple cancellation from the LA), the system linearity can be jeopardized. The works in [104][105] explain the choice of output filter passive components based on cutoff frequency. The sources of non-linearity in linear and switched assisted SMs are also explained and the optimum values of bandwidth, feedback ratio, switching frequency, and digital control hardware clock frequency can be identified to achieve the desired ET-PA system linearity. The multi-level and multi-phase architectures offer performance advantages and may be explored for realizing the SA within future CMOS-based HSMs.

The work in [99] proposes a two-phase three–level SM to track a 20 MHz 4G LTE envelope signal, as shown in Figure 3.24. The design uses Gallium Nitride (GaN) FETs (field-effect transistors) for the power devices and a discrete gate driver with adjustable dead time and switching frequency to drive the power stage. The SM uses a zero-voltage switching (ZVS) technique for better efficiency and a fourth-order ZVS low pass filter to track large bandwidth envelope signals and to maintain current self-balancing in the multi–phase converter system. Another work [100] extends the work in [99] to propose a cascaded switching capacitor-based four-phase three-level SM and experimental results are provided to validate the proposed concept.

The work in [101] introduces a novel single-flying capacitor multi-phase converter

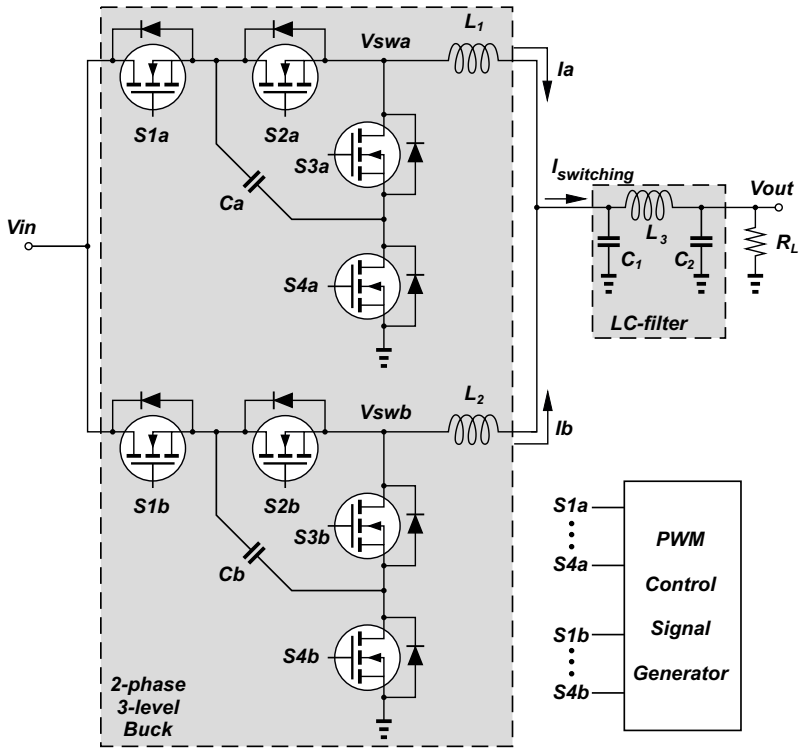


Figure 3.24: Switching Amplifier with Two-phase and Three–level Converter Topology

with negatively coupled output inductors as an attractive alternative to multi-phase solutions based on conventional two-level SA topologies that are almost exclusively used in industry. With the combination of relatively low switch-node voltages and the output inductors being negatively coupled together, each phase's current ripple is significantly less than a multi-phase with the conventional two-level SA and magnetically isolated inductors. The architecture of [102] explores a multi-phase flying capacitor multi-level SA with coupled inductors for ripple reduction and intrinsic flying capacitor voltage balancing.

Depending upon the HSM's linearity requirements, the numbers of levels or phases are selected in multi-level and multi-phase topologies of the SA. But, both of these SA current ripple reduction topologies suffer from some inherent trade-offs. The multi-level SA converter design requires the use of flying capacitors for its operation. The

value of each capacitor is generally large (≈ nano to micro farad range) and difficult to integrate on-chip. The multi-phase SA converter design requires the use of more than one off-chip inductor for its operation, which also consumes extra area on the board and increases complexity for assembly. Furthermore, both SA converter topologies require additional control circuitry for their operation, which ultimately increases the complexity of the HSM design.

3.3.2 Voltage Ripple Cancellation

Another way of reducing ripple is to optimize the LA's gain and bandwidth. Since the PA load, R_{PA}, is generally fixed and set by the PA's design requirements, ripple reduction efforts focus on reducing the magnitude of the LA's closed loop output impedance, $Z_{out}(s)$ in equation 3.8. A simplified model for calculating $Z_{out}(s)$ of the LA is shown in Figure 3.25. The value of $Z_{out}(s)$ depends on the output impedance (R_{out}) of the mainly class-AB stage, the gain of the LA ($A(s)$), and the feedback factor (β), as:

$$Z_{out}(s) = \frac{R_{out}}{1 + A(s)\beta} \tag{3.10}$$

Therefore, a low value of $Z_{out}(s)$ can be accomplished by designing a high-gain amplifier with a proper feedback network. Since R_{out} and β are nearly constants (based on the design), $Z_{out}(s)$ shows a reverse frequency response to $A(s)$ from equation 3.10, and its value gets higher as the frequency increases. Therefore, it is important for the LA to maintain a high value of $A(s)$ to keep the value of $Z_{out}(s)$ low. When doing this, the magnitude of output voltage ripple, V_{out_ripple}, approaches zero, which means that the LA absorbs all of the ripple from the SA and therefore provides voltage ripple cancellation. But, with aggressive channel length scaling in CMOS technologies, it is increasingly more difficult to achieve high LA gain because the intrinsic low-frequency

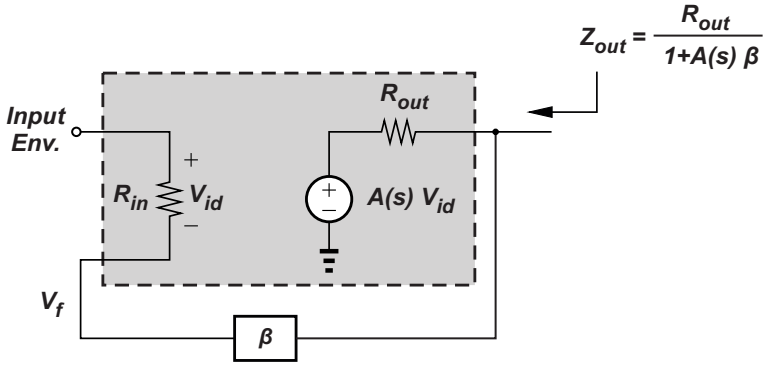


Figure 3.25: A Simplified Model of the LA for Calculating Output Impedance

gain of a transistor drops, as described by:

$$Intrinsic\ gain \propto \frac{L}{V_{ov}} \tag{3.11}$$

With smaller channel lengths, the transistor's intrinsic gain becomes so low (on order of 10's V/V) [106] that a single-stage LA does not provide sufficient gain. Also, the supply voltage level decreases with advancing CMOS generations, which reduces the device headroom in a LA and makes it difficult to cascode transistors. Therefore, horizontal cascading of multiple stages is performed to maximize the overall LA gain, $A(s)$. Cascading of multiple stages can provide higher gain, but LA stability must be ensured at all operating points of the input signal envelope. The works in [55] and [61] adopt a three-stage cascaded LA architecture to achieve a high value of $A(s)$. Due to this high gain, [61] demonstrates a low ripple voltage ($\approx 3{-}8\ mV$) at the HSM's output with attenuation for the second harmonic remaining below $-40\ dBc$.

3.4 Output Power Improvement in HSM

In an ET-PA system, the HSM acts as a power source that modulates the PA's supply power with respect to input envelope. The HSM's output power depends upon the maximum supply voltage that the LA can support (via feedback) and load

resistor (from equation 3.1). When the battery voltage level supplying the LA remains constant, delivering output power to the load is not difficult. But, due to voltage variation in the battery over time, the supply level of the LA decreases, thus reducing the LA's output power. Moreover, the maximum supply voltage level decreases with advancements in CMOS technologies, which limits the LA's supply voltage and hence HSM output power. Various architectures to prevent LA supply voltage degradation and improve HSM output power are discussed in the following subsections.

3.4.1 Boost-Mode HSM

A wireless handset device is generally powered by a Li-Ion battery whose voltage degrades with time and discharge. For instance, when the battery is fully charged, its voltage is nearly 4.2 V, but as it is discharged, the voltage level reduces to 3.5 V and drops quickly thereafter [107]. Since the output voltage of the LA depends upon the battery voltage, the HSM output power degrades as the battery drains. Therefore, a boost converter can be added between the LA's supply and the battery to maintain a constant voltage supply for the LA, irrespective of battery voltage variations, as illustrated by the diagram in Figure 3.26. With this architecture, the LA can process envelope levels up to the constant boosted supply voltage (V_{DD-LA}), while the battery voltage varies from V_{max} to V_{min}. The work in [108] adopts a boost-mode HSM architecture that maintains a constant 5 V supply for the LA and provides constant HSM output power with battery voltage variation from 4.2 V to 2.8 V.

The major disadvantage of a boost-mode HSM architecture is that efficiency of the additional boost converter limits the maximum HSM efficiency. Also, due to the presence of a switched-mode boost converter, the LA receives additional ripple at its supply node, which can propagate through the HSM and degrade the ET-PA system linearity.

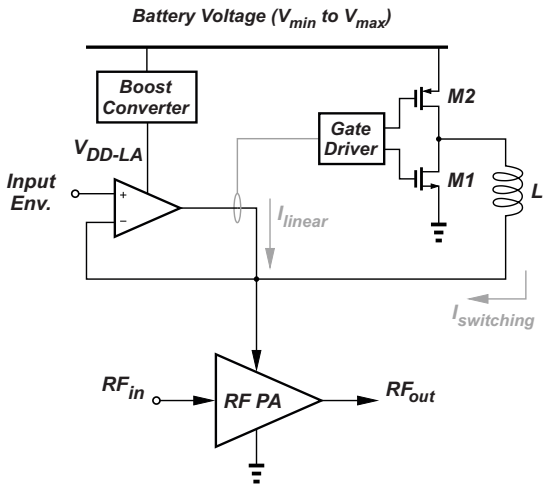


Figure 3.26: A Boost-Mode HSM architecture

3.4.2 AC-Coupled HSM

A boost-mode HSM architecture prevents the degradation of output power but does not improve HSM output power beyond its nominal value. Furthermore, the boost-mode HSM does not provide a solution for achieving higher output powers (large envelope voltage) with decreasing supply levels. An AC-coupled HSM architecture can be used to overcome these challenges.

Most of the conventional HSM designs are DC-coupled, where the LA and SA are directly connected to the output. But in the AC-coupled HSM of Figure 3.27, the output of the LA is isolated from the HSM's output via a large AC-coupling capacitor. This capacitor maintains a constant offset voltage (V_{offset}) across it, which makes the sum of the LA supply (neglecting device headroom) and V_{offset} equal to the input envelope voltage value. With this architecture, the LA's supply voltage can be lowered (V_{DD_L}), and an HSM can be implemented in smaller CMOS technology nodes to support faster tracking of input envelopes (as discussed in Section 3.2). Furthermore, depending upon the value of V_{offset}, the envelope signal's voltage magnitude can

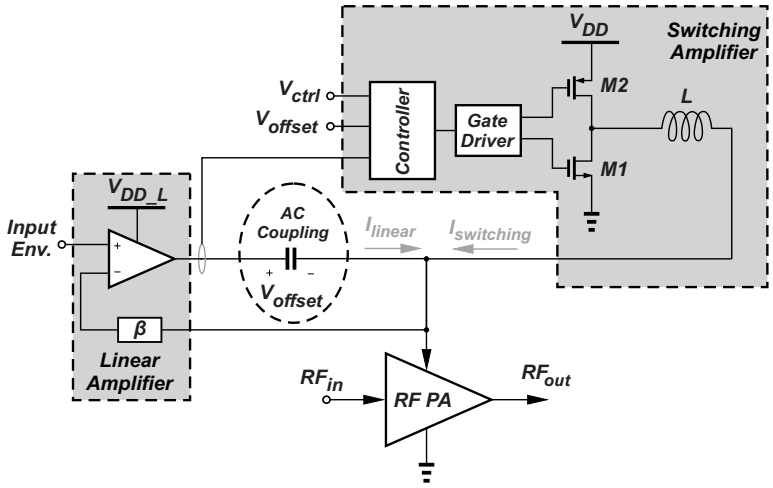


Figure 3.27: An AC-Coupled HSM Architecture

Table 3.1: Performance Comparison of AC-Coupled Hybrid SM

Ref	CMOS Tech.	Modulation	V_{DD} (V)	Max Eff (%)	Max Pout (W)
[70]	$90\,nm$	LTE 6RB	5.0	88.0	3.2*
[70]	$90\,nm$	LTE 10M	5.0	83.0	3.2*
[110]	$0.153\,\mu m$	LTE 20M	3.8	87.1	3.5
[111]	$0.13\,\mu m$	LTE 40M	4.0	83.0	0.92*
[110]	$0.153\,\mu m$	LTE 40M	3.8	85.5	3.5
[112]	$90\,nm$	LTE 40M	4.0	83.0	1.8
[110]	$0.153\,\mu m$	LTE 60M	3.8	82.3	3.5
[110]	$0.153\,\mu m$	LTE 80M	3.8	81.2	3.5
[70]	$90\,nm$	5G NR 100M	5.0	77.0	3.2*

* Extracted from Graph

be increased to increase the HSM's output power. To-date, the AC-coupled HSM architectures have achieved highest reported output powers in CMOS.

A disadvantage of the AC-coupled architecture is that it requires an extra AC-

coupling capacitor that has large value ($\approx$ nano to micro farad range) and is therefore difficult to integrate on-chip. The value of V_{offset} also needs to be carefully controlled to attain the proper envelope signal at the HSM output. Additionally, an extra control loop is required [109] to maintain V_{offset}, which leads to increased HSM design complexity. Table 3.1 summarizes the state-of-the-art works using the AC-coupling technique. The majority of the most recent works in HSM design focus on AC-coupled architectures and demonstrate highest reported envelope tracking bandwidths.

Chapter 4

DEVICE TECHNOLOGIES AND ET-PA SYSTEM CHALLENGES

A SM alleviates the PA's impact on transmitter power consumption, which leads to considerable power savings, extended battery lifetime, smaller heat-sink designs (for base-station applications), and potentially higher reliability. But, this improvement in efficiency comes at the cost of extra die area and an increased bill-of-materials (BOM). As multiple SM and PA device technologies are industrially available, selecting the most suitable technologies for hardware realization is a key decision to achieving optimum performance for an ET-PA system.

4.1 Supply Modulator Device Technologies

Most of the developments in HSM target cellular handset applications in sub-6 GHz bands. CMOS and SiGe-BiCMOS are the two main device technologies typically chosen for HSM implementation. Due to their lower cost, low power consumption, and high integration capability with the baseband processor and RF front-end, CMOS processes are the favored choice. Furthermore, CMOS allows integration of on-chip calibration and self-test circuitry [113]. Table 4.2 summarizes performance of the state-of-the-art CMOS HSMs. It can be observed from Table 4.2 that lower CMOS nodes are preferred for tracking higher modulation bandwidths, but they also lead to lower output power (due to lowered supply). Therefore, the AC-coupled architectures for HSM are gaining traction (in both academia and industry), as they provide the ability to track high bandwidths using more advanced CMOS process nodes without compromising on power. This is demonstrated in Table 4.2, where [70], [155], [156], [57] are the AC-coupled architectures that also achieve highest tracking bandwidths

Table 4.1: Comparison of Different PA Device Technologies

Parameters	Device Technology			
	CMOS	GaAs	SiGe	LDMOS
Passives Quality	Low	High	Low	Low
Transition Freq.	Moderate	High	High	Low
Breakdown Voltage	Low	High	Moderate	High
Cost	Low	High	High	Moderate
Integration	High	Low	Moderate	Moderate
Availability	High	Moderate	Moderate	Low

of 100 MHz and above.

4.2 Power Amplifier Device Technologies

There are multiple technologies for PA implementation, most popularly CMOS, gallium arsenide (GaAs), silicon germanium (SiGe) and laterally-diffused metal-oxide semiconductors (LDMOS), which are industrially available for cellular mobile applications. Gallium nitride (GaN) has yet to be adopted for commercial handsets due to its higher cost, knee voltage, and typically lower yields. The PA technology is typically chosen based on the PA's RF performance specifications and integration requirements. A qualitative performance comparison of different PA device technologies is given in Table 4.1.

It is important to note that while CMOS is usually preferred for HSM realization, GaAs is mainly chosen for implementing PAs because of its superior ability to support high frequency and high power applications with good efficiency and reliability. Therefore, GaAs processes dominate the existing PA market [114].

4.3 Power Amplifier Integration

The commercial wireless handset market demands high levels of sophistication [115] with low component cost and power. Modern solutions require multi-standard and multi-band functionality, along with a platform to support wireless connectivity features such as GPS, Bluetooth, WLAN etc.

Due to significant channel length scaling, the transition frequency of transistors in CMOS technology has reached well beyond 100 GHz, which makes CMOS popular for RF applications [116]. Therefore, to achieve complete integration of baseband functionality and the radio chain, it is desirable to also integrate the PA in CMOS [117][118][119][120][121][122][123]. CMOS technology has already proliferated hardware for Bluetooth and ZigBee applications that include integrated PAs. However, these PAs typically operate at lower power levels and demand lower bandwidths, therefore having more relaxed performance requirements compared to cellular communications hardware.

Unfortunately, PA implementation in CMOS processes faces some technical hurdles. Low breakdown voltage levels, lower device gain, linearity issues due to high compression characteristics, lack of through-wafer ground-vias, high substrate loss, poor thermal dissipation, and lack of high voltage capacitors are among the technical challenges. The cost of research and development (R&D) for deep submicron CMOS IC design has also increased dramatically due to the high cost of photo masks [124]. The ability to overcome these challenges will largely determine if and when production PAs can be integrated in CMOS (with the HSM). There is a recent trend toward implementing PAs in Silicon-on-Insulator (SOI) processes, as SOI processes provides higher speed, low power, higher intrinsic gain, much less substrate loss/coupling, no source-body and drain-body diodes (in fully depleted version of SOI), separate back-

gate terminal for reducing leakage current, and higher device density compared to most bulk CMOS processes [125][126][127].

4.4 ET-PA System Challenges

An ET-PA system consists of the SM, the PA, and extra control circuitry. Typically, the SM and PA are designed separately, and the connection between the separate blocks can become a bottleneck in ET-PA system performance. There are multiple challenges in interfacing the SM with PA, which are briefly analyzed in the following subsections.

4.4.1 Delay Mismatch

In an ET-PA system, the baseband input envelope signal and the RF signal are provided separately to the SM and the PA, respectively. The delay in the RF path is usually substantially shorter than that of the envelope (SM) path. Therefore, the delay mismatch [128] between these two paths is a source of distortion. As explained in [129], the inter-modulation distortion (IMD) introduced by this delay mismatch can be described as:

$$IMD = 2\pi B_{RF}^2 \Delta_\tau \tag{4.1}$$

where B_{RF} is the modulation bandwidth of the RF signal, and Δ_τ is the magnitude of delay mismatch. The minimum lower and upper band inter-modulation distortion ($IMD_{l,u}$) determines the PA output signal's ACLR value as:

$$ACLR = min(IMD_{l,u}) + k \tag{4.2}$$

where k is a correction factor determined by the PAPR level and the PA's compression point [130]. An example of the effect of delay mismatch on ACLR can be

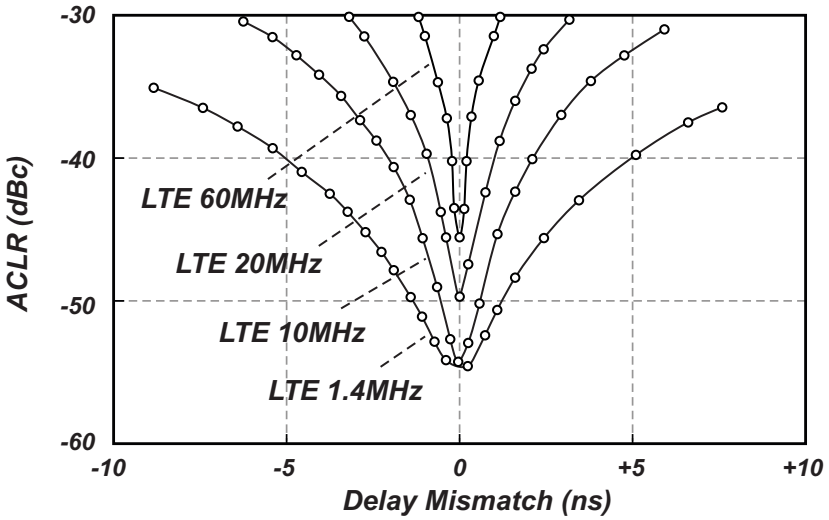


Figure 4.1: ACLR Versus Delay Mismatch for Various LTE Envelope Signal Bandwidths

observed in Figure 4.1 for various bandwidth LTE signals. As the LTE envelope signal's bandwidth increases, the delay mismatch between the RF and the envelope path must decrease to satisfy the required output signal quality (EVM). The delay mismatch can be fixed through calibration techniques with fine delay tuning capability.

4.4.2 SM Load Variation

Historically, a SM is designed and optimized for a fixed value of PA load (drain impedance) [61][55]. But, this fixed resistive model for the PA does not hold true in practical ET operation. The works in [131][132] have demonstrated that the PA's drain impedance varies with the V_{DD} supply. As the SM efficiency is dependent on the PA's drain impedance (from equation 3.1), this variation leads to a change in SM efficiency. The work in [18] measures HSM efficiency under different resistive loads (Figure 4.2) and shows that SM efficiency can change significantly under different loading conditions. Therefore, the variation in PA drain impedance should be ac-

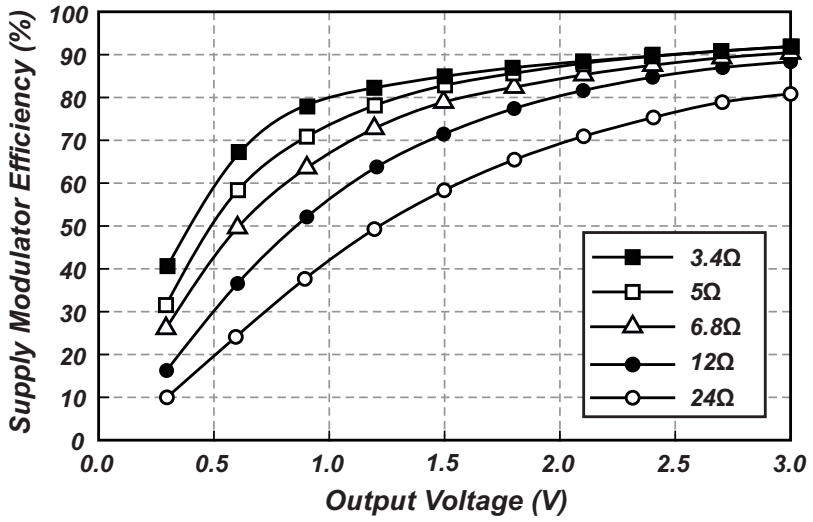


Figure 4.2: Measured HSM Efficiency for Various Load Resistances

counted when optimizing any HSM design in order to minimize any kind of efficiency degradation.

4.4.3 Envelope Shaping

Most SMs are designed to process the entire input envelope's voltage swing, and this swing appears at the drain of the PA as its supply voltage. If the PA's supply voltage becomes lower than the PA device's knee voltage (V_{knee}), the nonlinear output capacitance in the PA device would suddenly increase [137] and the PA would demonstrate a highly nonlinear behavior with high amplitude-to-amplitude modulation (AM-AM) and amplitude-to-phase modulation (AM-PM) distortion at the output. To avoid this problem, the input envelope is shaped to avoid lower power levels below the V_{knee} region. As demonstrated in Figure 4.3, different functions can be used to shape the original envelope. Notably, the work in [138] introduces a shaping function for the entire envelope voltage range to achieve improved PA linearity through third order inter-modulation distortion ($IMD3$) cancellation.

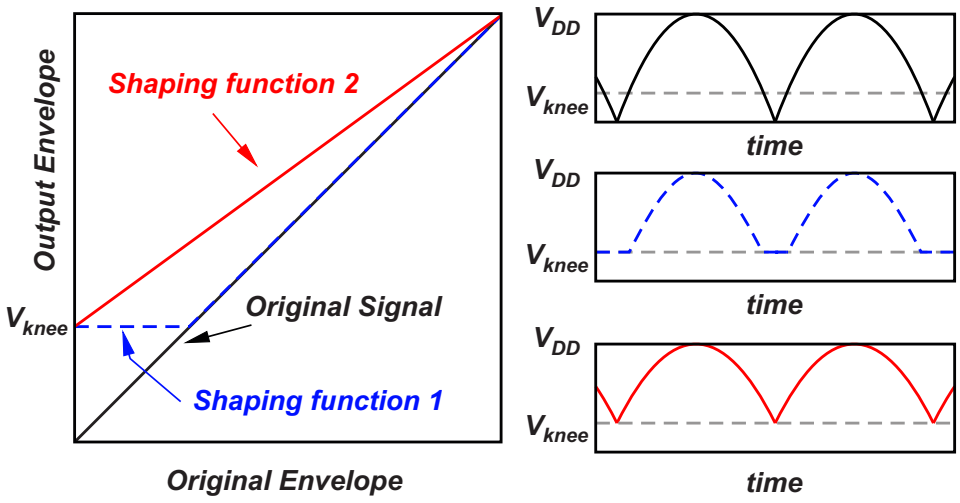


Figure 4.3: (Left) Envelope Shaping Using Different Functions, and (Right) Their Respective Time Domain Waveforms

4.4.4 SM-PA Physical Interface

Usually, a coupling inductor (L_{couple}) is used to connect the SM's output to the PA's drain node, since these are typically implemented on separate die [167]. The L_{couple} can be a bondwire or can be used as a choke for the PA, but the presence of L_{couple} degrades the PA's linearity because it increases the PA's memory effects and adds to the output noise [139]. The work in [140] implements an ET-PA system in which the supply modulator is implemented in a 0.18 μm process and connected to a heterojunction bipolar transistor (HBT) class-E PA via L_{couple}. The ET-PA system is excited with different LTE signals of varying bandwidths (10, 20, and 40 MHz). The value of L_{couple} is varied and the $IMD3$ response at the output of the PA is measured as shown in Figure 4.4. It can be observed that PA linearity degrades severely with higher envelope bandwidths and for increased values of L_{couple}. In addition to the coupling inductor, the non-ideal effects of wirebonds, pad capacitances, and board PCB routing have a detrimental impact on the ET-PA system performance. For

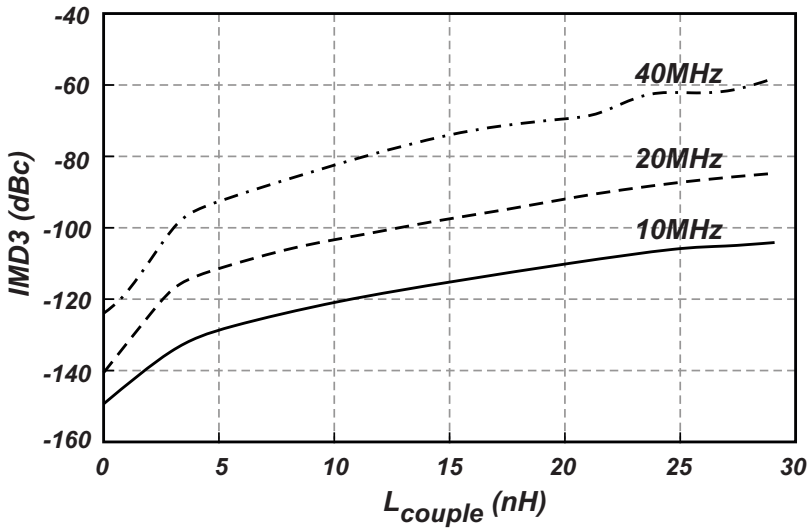


Figure 4.4: $IMD3$ Response Versus Coupling Inductor (L_{couple})

wideband applications, these parasitics become the bottleneck for operating bandwidth. These effects can be minimized by implementing a fully integrated single-chip ET-PA system or integrating the supply modulator and PA on a multi-chip module package with advanced packaging techniques [141][142], at the expense of higher cost and potentially lower assembly yield.

4.4.5 Variation in PA's Optimum Load Impedance

A linear PA is designed for an optimum load impedance (Z_{opt}) that is typically found through load-pull simulations/measurements. The work in [133] proves that the value of Z_{opt} does not remain constant and changes with the PA's V_{DD} supply in an ET operation. This effect is more pronounced for wideband systems, where the value of Z_{opt} can vary significantly over the range of instantaneous operating frequencies, thus complicating the design of the PA's output matching network. Incorrect matching degrades the PA efficiency and limits the maximum power that can be delivered to the load. Furthermore, variation in the Z_{opt} value leads to non-linearity in the ET-PA

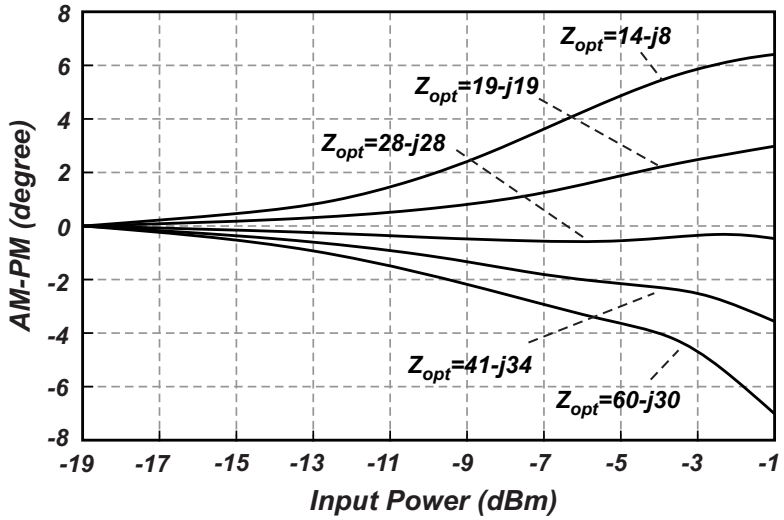


Figure 4.5: PA's AM-PM Response for Various Z_{opt} Values

system. The work in [134] concludes that when different Z_{opt} values are presented to a PA, the PA exhibits varying AM-PM response. This variation was measured in [134] using a nmos-input common-source differential PA architecture implemented in GlobalFoundries 45 nm SOI CMOS process, and the results are shown in Figure 4.5. The need for dynamically variable matching networks has driven developments in tunable on-chip matching techniques and passive structures [135][136].

4.4.6 Heat Management

The management of heat is a another major challenge for the ET-PA system. Since the PA dissipates significant power, the unused energy in the form of heat can lead to impaired linearity, reduced effective power density, and the heat affects the SM performance [143]. In integrated ET-PA systems, catastrophic failure may occur due to self-heating, especially under mismatch conditions typically occurring in the mobile user equipment (UE) environment [144]. Therefore, significant design consideration must be given to power density, thermal dissipation techniques through

the substrate, assembly materials for die attach and bonding to the substrate, and grounding techniques, as heat-sinks are not available in mobile handsets due to limited area (unlike base-stations).

Many of the discussed ET-PA interface problems can be eliminated by implementing a fully integrated single-chip ET-PA system, but single-chip implementations face another set of challenges including: noise coupling, large die areas, thermal dissipation, monolithic integration of the passive devices, and non-optimal choice of process technology for either the SM or PA that leads to reduced RF performance. To-date, single-chip implementations have generally not achieved the efficiency and output power performance of multi-chip module implementations.

Table 4.2: Performance Comparison of State-of-the-art CMOS HSM Solutions (Sorted Based on Modulation Bandwidth)

Ref.	CMOS Tech.	BW (Hz)	V_{DD} (V)	Load (Ω)	Max Pout (W)	Max Eff (%)	Die (or Chip) Area (mm^2)	Off-Chip Ind	AC-Cap
[26]	0.15 μm	10M	4.5	8.0	0.93	82.0	1.60	1 μH	NA
[70]	90 nm	10M	5.0	3.2	3.2*	83.0	5.14	3 ind	1 cap
[66]	0.18 μm	10M	3.6	6.0	1.02*	83.0	1.10	10 μH	NA
[145]	0.13 μm	10M	4.0	8.0	0.8	80.0	5.00	1 ind	1 cap
[146]	0.18 μm	10M	3.4	7.5	–	80.4	1.82	1 ind	NA
[147]	0.18 μm	10M	5.0	6.5	0.56*	75.3	1.82	1 ind	NA
[148]	0.18 μm	10M	3.3	6.2	1.05	86.5	3.84	4.7 μH + 51 nH	NA
[149]	0.18 μm	10M	3.3	–	1.5	85.8	7.44	78 nH (×2)	NA
[68]	0.13 μm	10M	3.8	4.7	–	86.2	6.35	4.7 μH + 22 nH	0.47 μF#
[150]	0.18 μm	10M	4.7	7.8	–	81.5	0.60	1 ind	NA
[151]	0.18 μm	10M	3.3	6.0	0.85	75.2	1.55	1 ind	NA
[152]	0.18 μm	10M	3.3	–	1.0	83.6	1.50	1 ind	NA
[53]	0.18 μm	20M	3.45 - 5.0	6.5	–	75.9	1.40	1 ind	NA
[62]	0.18 μm	20M	3.5	4.6	1.1	79.6	1.15	1 ind	NA
[98]	65 nm	20M	2.4	3.9	0.8	88.7	3.42	206 nH	1 μF + 7 nF#
[110]	0.153 μm	20M	3.8	4.0	3.5	87.1	5.13	1 μH + 0.68 μH	4.7 μF
[153]	0.18 μm	20M	5.5	5.2	0.89	83.0	1.47	1 μH + 0.3 μH	NA
[155]	90 nm	20M	–	–	0.25	88.4	4.1	3 ind	1 cap
[62]	0.18 μm	40M	3.5	4.6	1.1	76.4	1.15	1 ind	NA
[65]	65 nm	40M	2.4	4.7	1.0*	93.0	2.72	538 nH	12 nF#
[110]	0.153 μm	40M	3.8	4.0	3.5	85.5	5.13	1 μH + 0.68 μH	4.7 μF
[111]	0.13 μm	40M	4.0	5.0	0.92*	83.0	4.00	2 ind	1 cap
[112]	90 nm	40M	4.0	4.7	1.8	83.0	3.00	3 ind	1 cap
[128]	0.18 μm	40M	3.6	6.7	1.2	85.0	2.25	1 μH	NA
[154]	0.18 μm	40M	3.6	4.0	1.8	85.0	2.25	4.7 μH	NA
[69]	0.25 μm	40M	5.0	–	1.5	79.1	2.89	2 ind	NA
[62]	0.18 μm	60M	3.5	4.6	1.1	74.0	1.15	1 ind	NA
[110]	0.153 μm	60M	3.8	4.0	3.5	82.3	5.13	1 μH + 0.68 μH	4.7 μF
[62]	0.18 μm	80M	3.5	4.6	1.1	72.8	1.15	1 ind	NA
[65]	65 nm	80M	2.4	4.7	1.0	91.0	2.72	538 nH	12 nF#
[110]	0.153 μm	80M	3.8	4.0	3.5	81.2	5.13	1 μH + 0.68 μH	4.7 μF
[58]	0.18 μm	100M	5.0	5.0	5.0	88.0	–	2.2 μH	NA
[70]	90 nm	100M	5.0	3.2	3.2*	77.0	5.145	3 ind	1 cap
[155]	90 nm	100M	–	–	0.55	84.0	6.9	4 ind	1 cap
[156]	90 nm	100M	5.0	–	3.5	84.0	–	2 ind	1 cap
[71]	90 nm	130M	5.8	–	3.53	84.1	6.9	2 ind	4.7 μF
[57]	40 nm	160M	3.6	5.0	1.9	88.0	2.24	1 μH	1 μF
[56]	0.18 μm	200M	5.0	5.0	4.0	88.0	–	2.2 μH	NA
[79]	90 nm	200M	–	–	4.5	93.6	13.6	4 ind	NA

* Extracted from Graph

flying Capacitor value

Chapter 5

PROPOSED HYBRID SUPPLY MODULATOR DESIGN

5.1 HSM Design Parameters and Optimization for Wideband Applications

A typical HSM design involves tradeoffs between different performance parameters, and a detailed discussion is required before the inception of its design [157]. This can be accomplished by relating the effects of the HSM to the whole ET-PA system. To meet the growing wireless bandwidth demands, HSM needs to be wideband and should maintain slew-rate large enough to track the fast changing envelopes. To maintain sufficient linearity for the spectrum mask, the HSM is required to a low output ripple. To achieve a high overall efficiency of the ET-PA system, the efficiency of the HSM has to be maintained high. Therefore, an HSM needs to be optimized to achieve overall wide bandwidth & slew-rate, small output voltage ripple, and high efficiency.

5.1.1 Controller Hysteresis Limits and Effect of Controller Delay

A hysteresis controller generally consists of a current sensing unit and a comparator. The controller controls the amount of SA's current I_{SW} flowing to the load by means of sensing LA's current I_{LINEAR} and comparing I_{LINEAR} against the hysteresis limits in the controller. Conventionally [30][158] it is assumed that the upper, I_{H_COMP} and lower threshold current limit, I_{L_COMP} of the hysteresis comparator are the actual limits, I_{H_CONT} and I_{H_CONT} of the controller, and the effect of the propagation delay, t_D, is ignored. However, this is only true for narrowband applications whose switching frequency is low (hence, the switching period is much longer than t_D) and

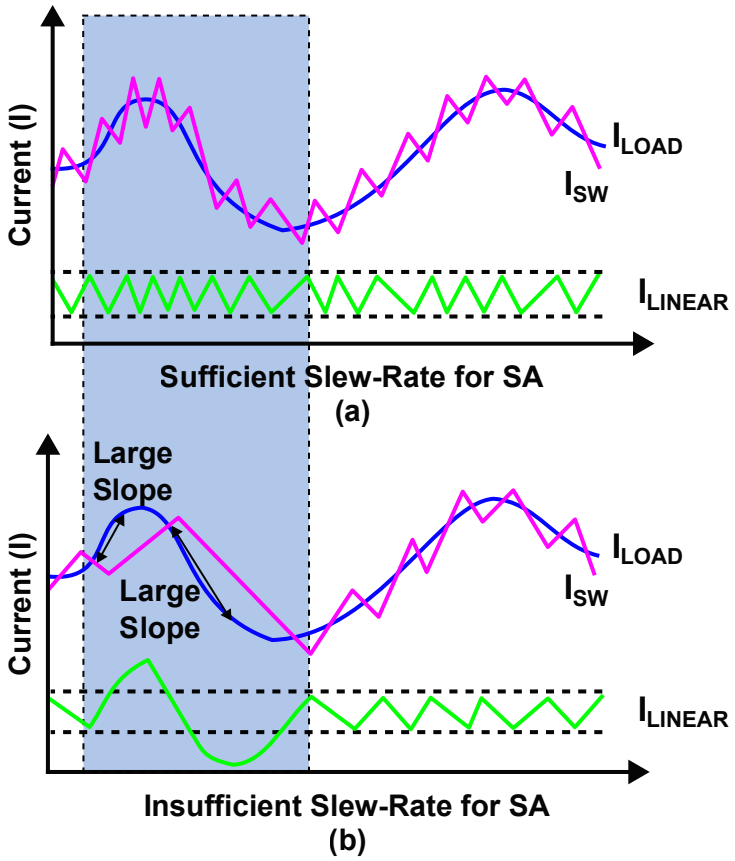


Figure 5.1: Current Waveforms of LA, SA and Load with (a) Sufficient Slew-rate and, (b) Insufficient Slew-rate

I_{SW} accounts for most of the load current I_{LOAD} as shown in Fig. 5.1(a). But this is not the case of wideband applications whose switching frequency is high (hence, the switching period is comparable to t_D). Here, the SA slews at sharp transition points and unable to provide I_{SW} to load as shown in Fig. 5.1(b). Due to this the rest of I_{LOAD} comes from I_{LINEAR}, which leads to efficiency degradation. Furthermore as shown in Fig. 5.2, increase in channel bandwidth of the envelopes for LTE protocols leads to increase in slew-rate requirements for the HSM as well. Therefore, the optimization of the HSM for wideband applications by taking t_D into consideration is needed.

From Fig. 5.3, it can be observed that V_{DD} is the supply voltage, V_{OUT} is the

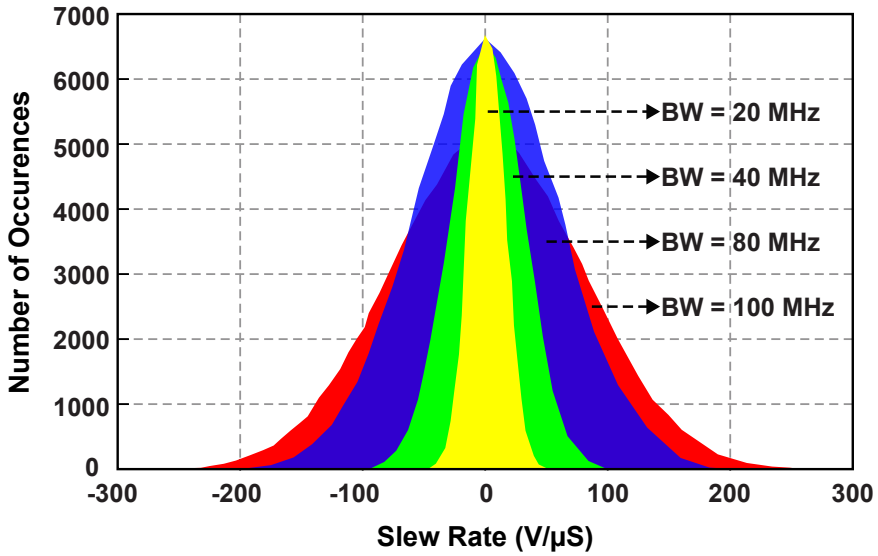


Figure 5.2: Slew-rate Trend for Different Bandwidths for LTE Protocol

output voltage and L_{ind} is the external inductor of the HSM. To include the effect of t_D, we need to observed the voltage (at switch Node) and current waveforms (for LA, SA and Load) of the HSM. Based on Fig. 5.4 (a) and (b), the controller hysteresis limits I_{H_CONT} and I_{L_CONT} for both narrowband and wideband applications can be defined as:

$$I_{H\_CONT} = I_{H\_COMP} + \left(\frac{V_{DD} - V_{out}}{L_{ind}}\right) \times t_D \tag{5.1a}$$

$$I_{L\_CONT} = I_{L\_COMP} + \left(\frac{0 - V_{out}}{L_{ind}}\right) \times t_D \tag{5.1b}$$

$$I_{HYS} = \Delta I_{HYS\_COMP} + I_{HYS\_Delay} \tag{5.2a}$$

$$\text{where, } \Delta I_{HYS\_COMP} = \left(I_{H\_COMP} - I_{L\_COMP}\right) \tag{5.2b}$$

$$\text{and, } I_{HYS\_Delay} = \left(\frac{V_{DD}}{L_{ind}}\right) \times t_D \tag{5.2c}$$

We define the controller hysteresis current I_{HYS} in eq. 5.2(a) as the difference between the upper and lower limits, i.e., $I_{HYS} = I_{H\_CONT}$ - I_{L_CONT}. The magnitude of

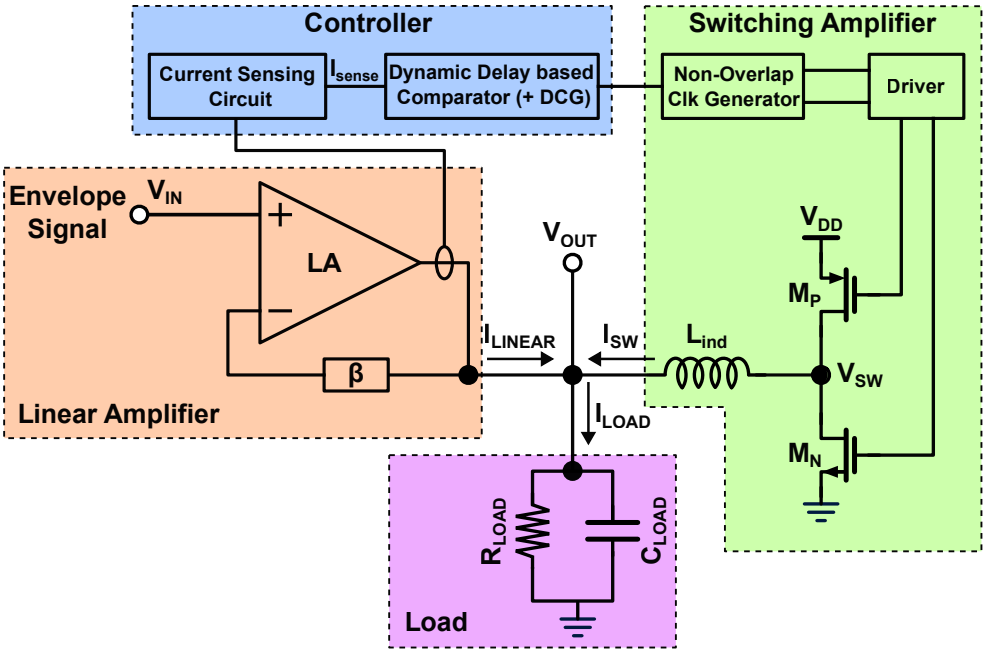


Figure 5.3: Block Diagram of the Proposed Hybrid Supply Modulator

I_{HYS} depends upon two factors i.e, extrinsic delay contributed by comparator hysteresis limits ΔI_{HYS_COMP} in eq. 5.2(b) and other is intrinsic delay, I_{HYS_Delay} in eq. 5.2(c), which depends upon parameters t_D, V_{DD} and L_{ind}. Previously in the published works [30][158], I_{HYS_Delay} is typically assumed to be negligible, i.e., $I_{HYS} = \Delta I_{HYS\_COMP}$. This is true for HSM designs with narrow bandwidth whose switching frequency is low, but it is not the case for wideband HSMs, where we need to account for the delay factor I_{HYS_Delay}.

5.1.2 Optimization of Controller Hysteresis Delay

In order to make HSM fast (or reduce hysteresis loop delay), the magnitude of I_{HYS} needs to be reduced. This can be achieved in two ways. Firstly, the magnitude of ΔI_{HYS_COMP} can be made to almost zero by moving from hysteresis to a delay-based comparator design. This helps in removing the need of generating hysteresis limits (internal/external) and leaving $I_{HYS} \approx I_{HYS\_Delay}$. Secondly, the magnitude of

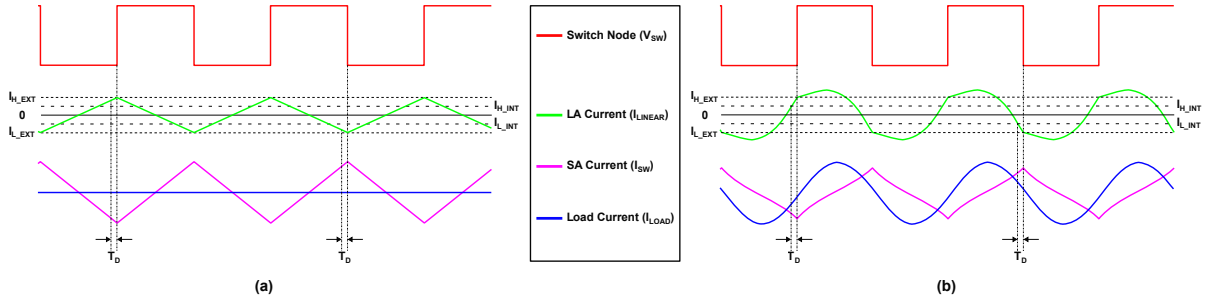


Figure 5.4: Typical Voltage (Switch Node) and Current Waveforms (for LA, SA and Load) of the HSM Tracking (a) Low-frequency Input Signals (b) High-frequency Input Signals

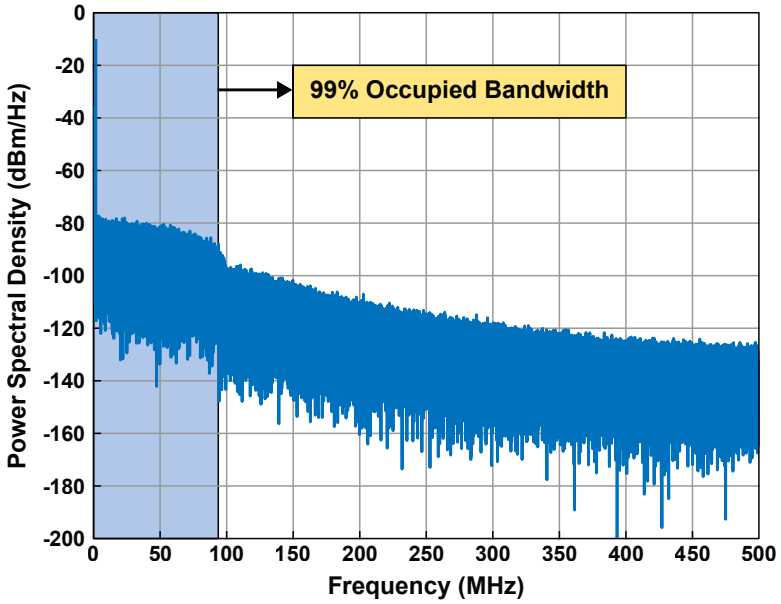


Figure 5.5: Simulated PSD Plot of LTE 100 MHz Signal

comparator delay (contributing to t_D) can be reduced by moving from voltage mode to a current mode controller design [1]. In short, for wideband HSMs, I_{HYS} is primarily bounded by the intrinsic delay hysteresis, I_{HYS_Delay}, due to the propagation delay t_D and not by the extrinsic limits of the hysteresis comparator as generally perceived. In this work, a zero threshold (hysteresis) current comparator is introduced which uses best of both the techniques (mentioned above) and explained in next Section 5.2.1 in detail.

For wideband HSMs, lower t_D leads to faster tracking but it is important to consider and optimize the losses contributed by the SA with higher switching. As shown in Fig. 5.5, the power spectrum of a modulated signal is spread from low frequency ($\sim$ DC) to high frequency. Hence, the HSM should respond slow to the low frequency input and fast to the high frequency input signals. This ultimately leads to the requirement of implementing HSM with varying t_D that can be dynamically changed with the input spectrum. To achieve this functionality, a dynamic current generator (DCG) is introduced and explained in Section 5.2.2 in detail.

5.2 Circuit Design of the Proposed HSM

We have shown in Section 5.1 that to make loop fast and obtain maximum power efficiency, ΔI_{HYS_COMP} can reduced to zero and t_D can be dynamically varied. We will now discuss the design of our HSM embodying a delay-based hysteresis controller, a dynamic current generator and a wideband LA to absorb the ripple from the SA and improve the linearity.

5.2.1 Proposed Zero Threshold High-Speed Current Comparator

The major issue of the conventional current-mode comparator embodied in the HSM designs, e.g., [23], is that the upper and low limits of I_{LINEAR}, I_{H_CONT} and I_{L_CONT}, are both positive (i.e., $I_{H\_CONT} > 0$ and $I_{L\_CONT} > 0$). Hence, the LA therein is designed to always provide positive current. This results in an undesirably larger portion of I_{LOAD} sourced from the LA, which in turn reduces the efficiency [159]. Also, we have shown in Section 5.1 that to make loop fast and obtain maximum power efficiency, ΔI_{HYS_COMP} can reduced to almost zero.

To circumvent the issue, a zero threshold high-speed current comparator is proposed as shown in Fig. 5.6. It works like in a delay-based fashion and doesn't require

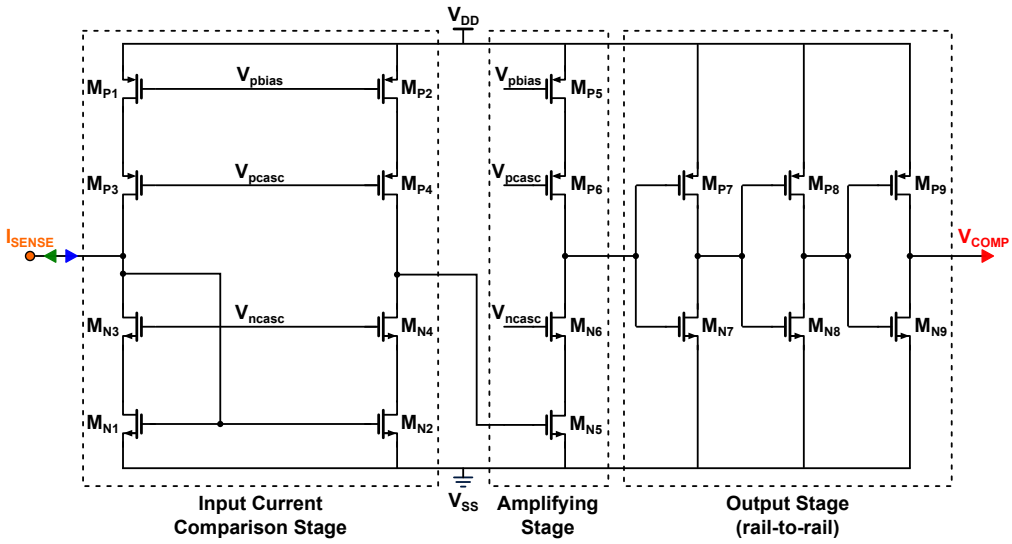


Figure 5.6: Transistor-level Implementation of the Proposed Zero Threshold High-speed Current Comparator

any external hysteresis. I_{SENSE} is the fraction of the LA's output stage current. The transistors M_{P2} and M_{P4} forms the pmos reference current and M_{N4} and M_{N2} forms the nmos reference current (via current mirror). If the LA is sourcing the current, then I_{SENSE} adds current to the nmos reference and the output of the current comparator goes low. Similarly, if the LA is sinking the current, then I_{SENSE} pulls current from the pmos reference current and the output of the current comparator goes high. Furthermore, the HSM is simulated for a dc input of $V_{DD}/2$ across a 5 Ω resistor. It can be seen from Fig. 5.7(a) and (b) that with the proposed zero threshold current comparator, the LA's current to the load goes to almost zero in the steady state (except the biasing current).

5.2.2 Proposed Dynamic Current Generator (DCG)

As discussed in Section 5.1, the magnitude of t_D needs to be varied dynamically based on the input signal's frequency content. This leads to a faster as well an efficient envelope tracking. To realize this application, a dynamic current generator

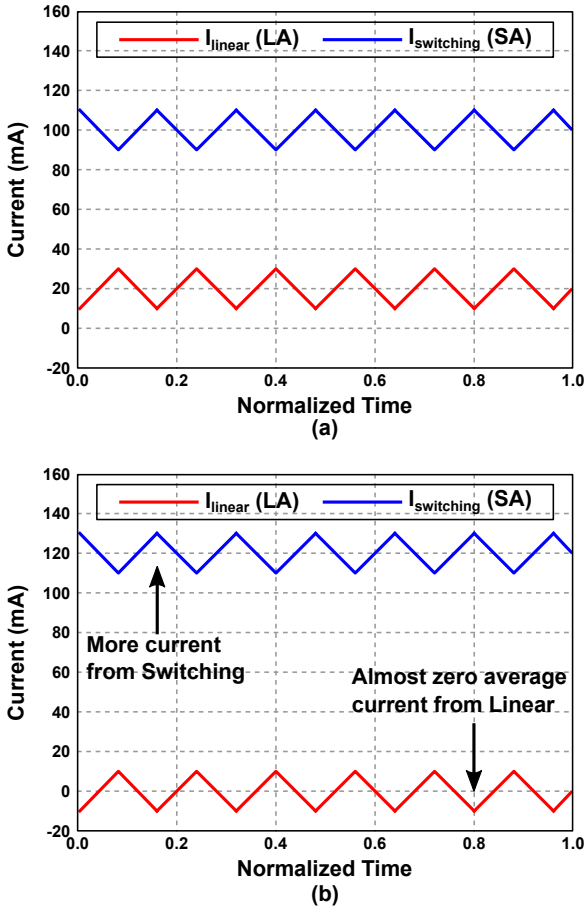


Figure 5.7: LA and SA Currents Waveforms for the (a) Conventional HSM, (b) Proposed HSM

(DCG) block is proposed which based on input signal frequency, can dynamically sink current into the comparator to change its bias current and hence, varies its delay. The dependence of bias current (I_{bias}) on 't_D' is explained from the work [160] as:

$$t_D \approx \left(\frac{C_{par} \times \Delta V_{OUT}}{I_{bias}} \right) \tag{5.3}$$

Now, as we can see that value of I_{bias} affects the magnitude of t_D from eq. 5.3, which ultimately changes the value of I_{HYS_Delay} from eq. 5.2(c). Now it is important to note that switching frequency of the loop ($f_{sw,loop}$) in HSM is given by the expression:

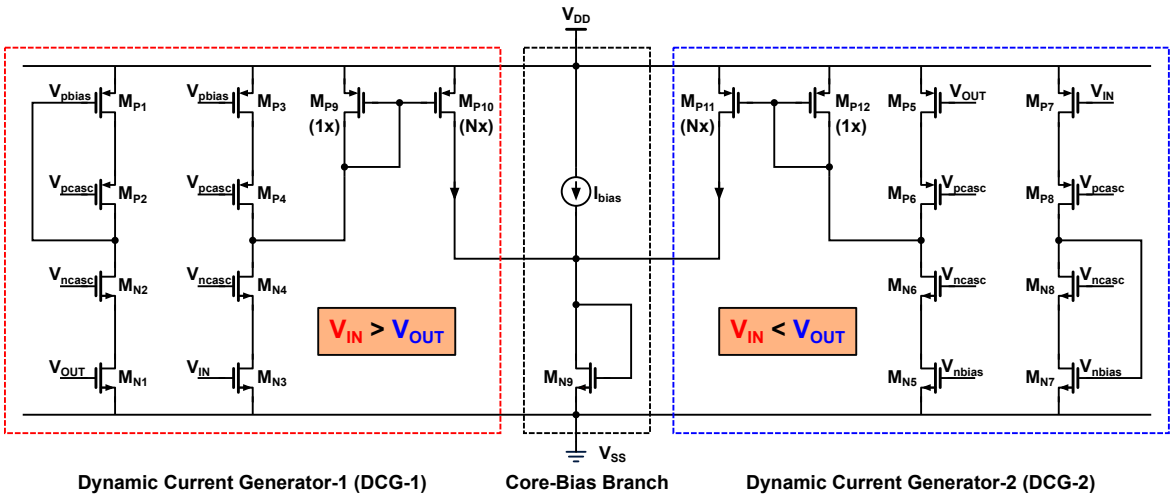


Figure 5.8: Transistor-level Implementation of the Proposed Dynamic Current Generator (DCG) Block

$$f_{sw,loop} = \frac{V_{OUT} \times (V_{DD} - V_{OUT})}{V_{DD} \times L \times N \times I_{HYS\_Delay}} \tag{5.4}$$

So, it can be deduced that by changing the I_{bias} dynamically, will vary the $f_{sw,loop}$ of the loop. This operation can be achieved through DCG block as shown in Fig. 5.8. So, in-case of rising fast transients i.e when $V_{IN} > V_{OUT}$, the DCG-1 block gets turned on. The transistors M_{N3} and M_{N4} pulls more current than M_{P3} and M_{P4}. This will eventually leads the gate voltage of transistor M_{P9} to go down and M_{P10} provides an additional bias current to I_{bias}. Similarly, in-case of falling fast transients i.e when $V_{IN} < V_{OUT}$, the DCG-2 block gets turned on. The transistors M_{N5} and M_{N6} pulls more current than M_{P5} and M_{P6}. This will eventually leads the gate voltage of transistor M_{P12} to go down and M_{P111} provides an additional bias current to I_{bias}.

To illustrate the working of the DCG in the transient, the currents from the DCG-1/2 are shown with a simulation setup. The voltage V_{IN} is ramped up from 0.2 V to 1 V and then ramped down from 1 V to 0.2 V as shown in Fig. 5.9(a). The corresponding current sourcing from DCG-1 and DCG-2 blocks into the main I_{bias} of

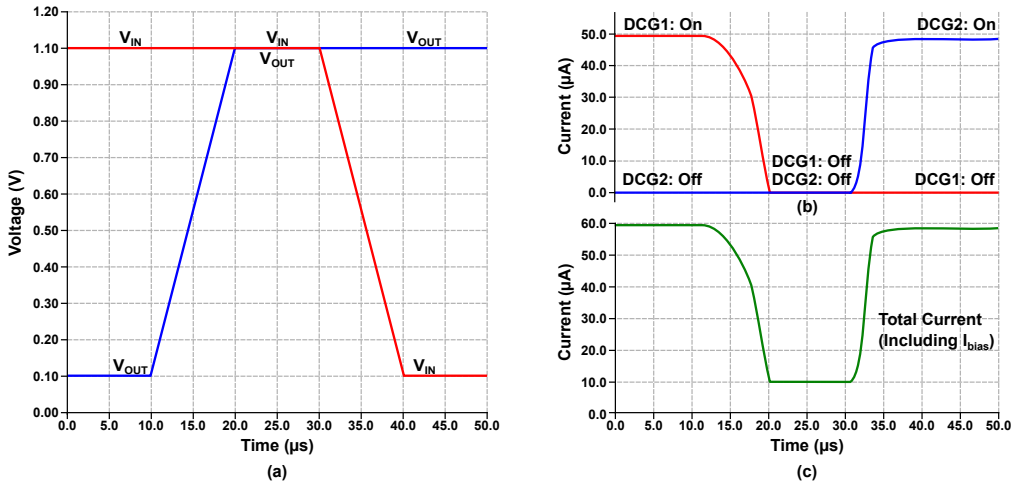


Figure 5.9: Simulated DCG's Working (a) Change in Input and Output Voltages, (b) Corresponding Currents Flow from DCG Blocks, (c) Total Current into the Comparator Core-bias Branch

the comparator are depicted in Fig. 5.9(b). It can observed that magnitude of I_{bias} changes dynamically from 12 μA $-$ 65 μA as the V_{IN} changes from 0.2 V to 1 V (and vice-versa) which is the voltage range for the LTE signal envelope. Furthermore, the change in I_{bias} magnitude leads to change in the comparator delay from 7.0 ns to 0.9 ns as shown in Fig. 5.10. This change in comparator delay varies the $f_{sw,loop}$ as per eq. 5.4. So, when the input signal frequency is low, the DCG doesn't provide current to the comparator's I_{bias} and hence, $f_{sw,loop}$ goes low. Conversely, when the input signal frequency is high, the DCG provides additional current to the comparator's I_{bias} and hence, $f_{sw,loop}$ goes high. This operation enables the HSM's loop to track the input signal frequency, which eventually helps in faster and efficient tracking of the envelope.

5.2.3 Current Sensing Circuit

In a typical HSM design, feedback from the LA to the SA is necessary to minimize the average output current from the LA to the load. A feedback signal I_{SENSE} generated from the LA output class-AB stage is used to modulate the power provided

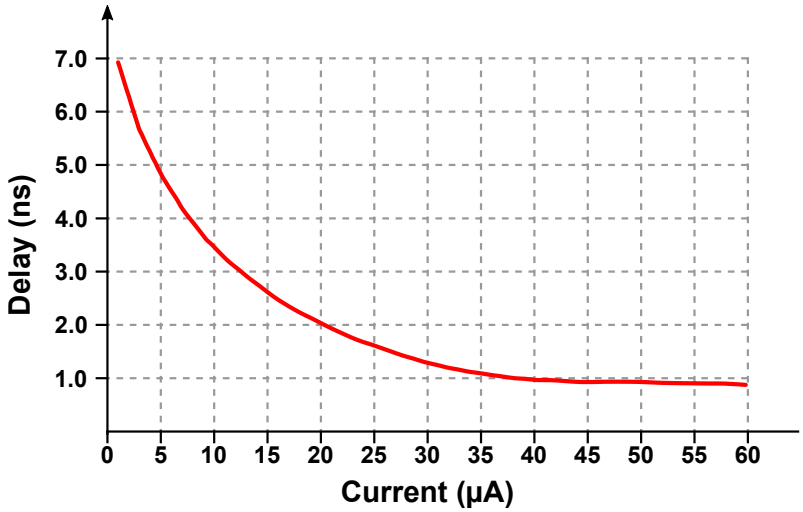


Figure 5.10: Simulated Plot of Comparator Delay with the Bias Current

by the SA. As the SA's tracking ability is limited by its low bandwidth, it is essential to accurately sense the current from the LA and an accurate current sense circuit is used in this work. This technique [161] works based on generating two references corresponding to LA's output voltage, V_{OUT} and then mirroring LA's sensed current I_{SENSE} to the comparator.

The current in the push-pull class-AB output stage of the LA is sensed through the current sense circuit formed by transistors $M_{N1}-M_{N7}$ and $M_{P1}-M_{P7}$, as shown in Fig. 5.11. Sense transistors M_{P2} and M_{N4} in paraller with the PMOS and NMOS transistors in the LA's output stage sense the current with a scaling factor of N. In order to sense the current accurately the V_{DS} of sense transistors must be same as the main class-AB transistors. To achieve this the output of LA V_{OUT} is level shifted up to V_{OH} and shifted down to V_{OL} by diode-connected transistors M_{N1} and M_{P1}. These level shifted voltages V_{OH} and V_{OL} are shifted back by M_{N5} and M_{P3} transistors to the drains of the NMOS and PMOS sense transistors respectively. This helps in achieving accurate current sensing. The current sensing action when the LA is sourcing and sinking is depicted in Fig. 5.11(a) and (b) respectively. The current

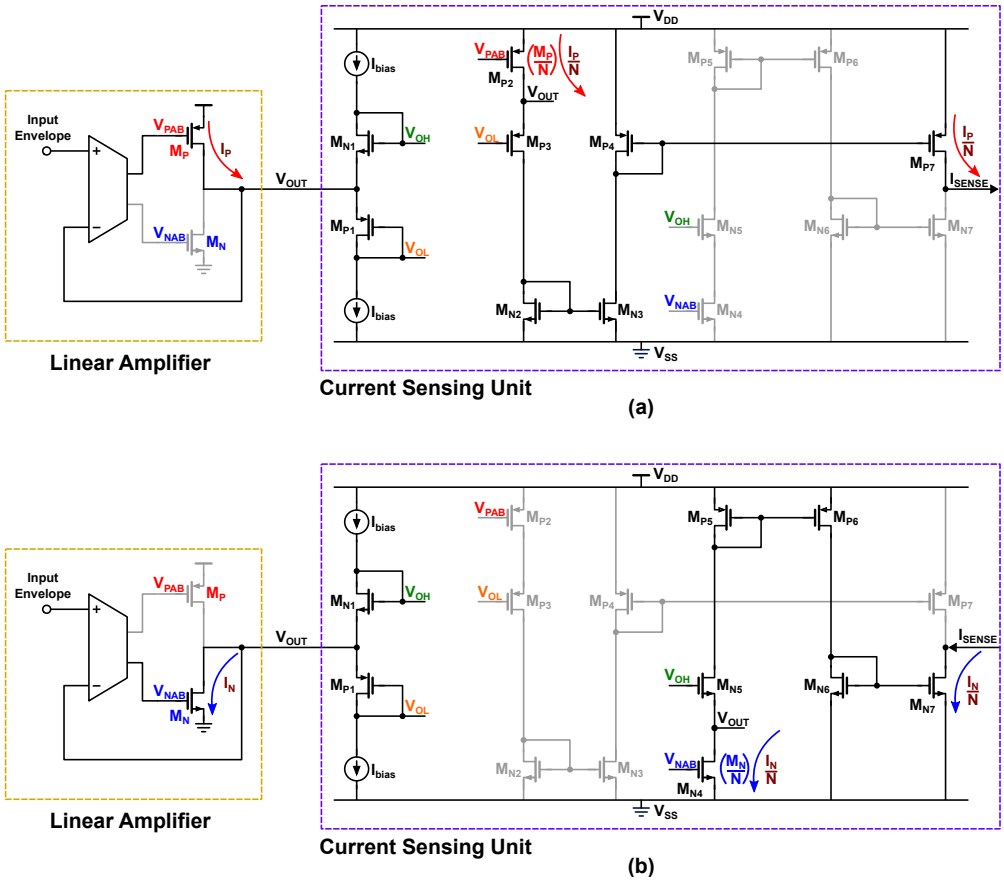


Figure 5.11: Transistor-level Working of the Current Sensing Block with the LA (a) When Class-AB High-side is Active, (b) When Class-AB Low-side is Active

sense circuit presented here offers an inherent 180 degree phase shift between the LA output current and the respective sense currents through current mirrors. Since, the current sensing is formed by current mirrors and all low impedance nodes in the circuit, the sensing is fast as compared to conventional current sensing methods [31][61].

5.2.4 Anti Shoot Through Driver

The sizing for the power stage transistors in the SA is done bigger to support majority of the load current. But a major loss of power is though the short-circuit,

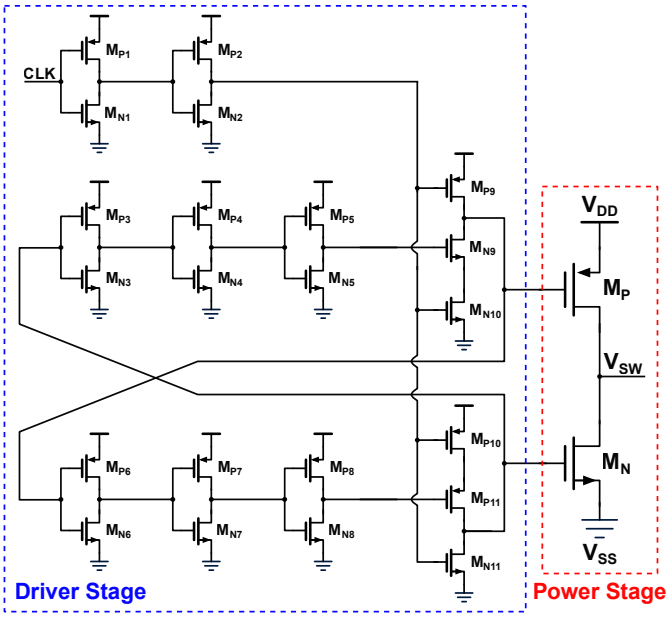


Figure 5.12: Transistor-level Implementation of the Anti Shoot Through Driver with Power Stage

when both the power transistors remain on simultaneously. Fig. 5.12 illustrates an antishoot through driver schematic [162]. The driver stage creates deadtime to prevent the power NMOS and the power PMOS turning on simultaneously. Therefore, there is minimum power loses from large shoot through current which improves the efficiency of the HSM.

5.2.5 Enhanced Class-AB Linear Amplifier

Since the amount of switching residue generated by the SA depends on the inductor and on the output impedance of LA, LA should have a low output impedance at the switching frequency to suppress the switching noise/ripple of SA which could directly affect the output PA spectrum [163]. Also, the bandwidth of the HSM should be several times higher than the signal bandwidth to avoid distortion since the input envelope bandwidth is much higher than the signal bandwidth [23]. The ripple content at the output of an HSM can be reduced by using a higher order output LC

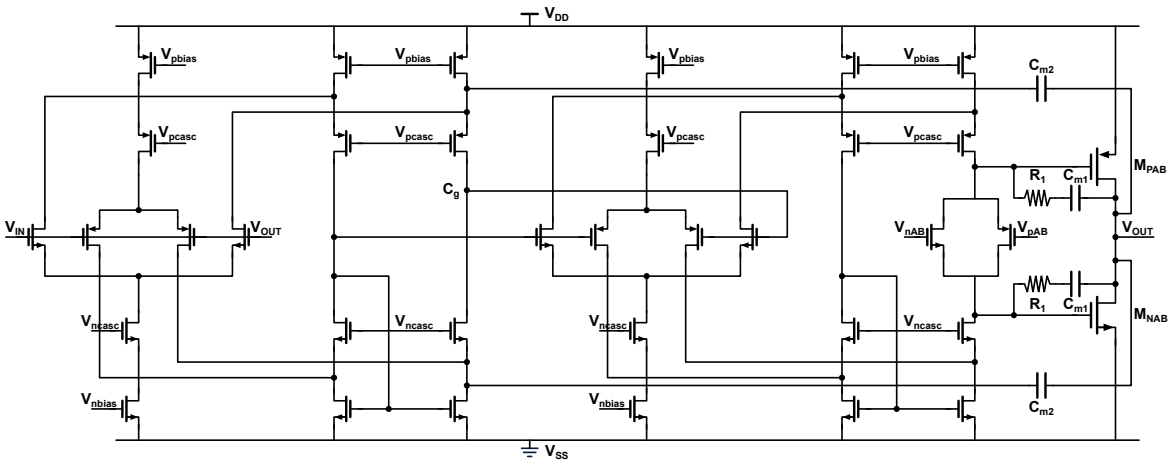


Figure 5.13: Transistor-level Implementation of the Enhanced Linear Amplifier (LA) for Wideband Tracking

filter. But the use of such filters limits the maximum HSM bandwidth of operation and is not suitable for wideband applications. The ripple voltage (V_{Ripple}) at the output node of the HSM can be expressed as follows:

$$V_{Ripple} = I_{Ripple} \times \left(Z_{OUT}(s) \;||\; R_{PA} \right) \tag{5.5a}$$

$$\text{and, } Z_{OUT}(s) = \frac{R_{OUT}}{1 + A(s) \times \beta} \tag{5.5b}$$

where I_{Ripple}, $Z_{out}(s)$, and R_{PA} represents the switching current ripple, closed-loop output impedance of the LA, and PA load resistance, respectively. Furthermore R_{OUT}, A(s) and β represents the output impedance, gain and feedback factor of the LA. It can be seen from eq. 5.5(a) and (b), that magnitude of the V_{Ripple} can be reduced by decreasing the $Z_{out}(s)$ by LA by designing a high-gain amplifier for wide bandwidth and large feedback factor.

To meet demanding requirements to track the envelopes of higher bandwidths, used a three-stage cascoded nested Miller compensated amplifier [164] with rail-to-rail input and output as a LA as shown in Fig. 5.13. The input stage was designed to

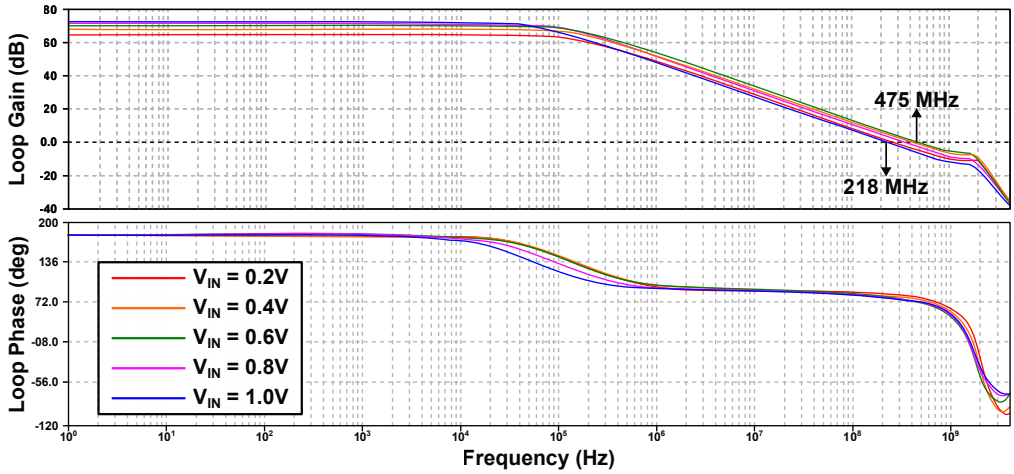


Figure 5.14: Simulated Open-loop AC (Gain and Phase) Performance of the LA Designed for Wide-band Tracking

have rail-to-rail input and output swing. A folded cascode configuration with complementary NMOS and PMOS input pairs are used such that when the input reaches to one of the supply rail, one of the pair stays active. These input pairs are loaded with folded cascode instead of current mirrors to ensure rail to rail output. When common mode of the input is at midsupply ($V_{DD}/2$), the total transconductance of the input stage is twice that of either the NMOS or the PMOS pair alone. Thus, the input transconductance is subject to 2:1 swings over the course of normal operation.

Though several techniques are proposed in the literatures to make this transconductance variation constant, for our application it is not necessary to compensate because it will just result two times variation in output resistance which is tolerable. The intermediate stage is similar to the input stage and has a rail-to-rail input/output capability. The floating current source at the output of this stage is used to set the quiescent-point for the class-AB output stage. An inverter configuration is used for the output stage in order to have rail to rail output.

The cascode configuration is obtained by connecting an outer Miller capacitor (C_{m2}) to the source of the cascode transistor of the first stage [165]. With simpler

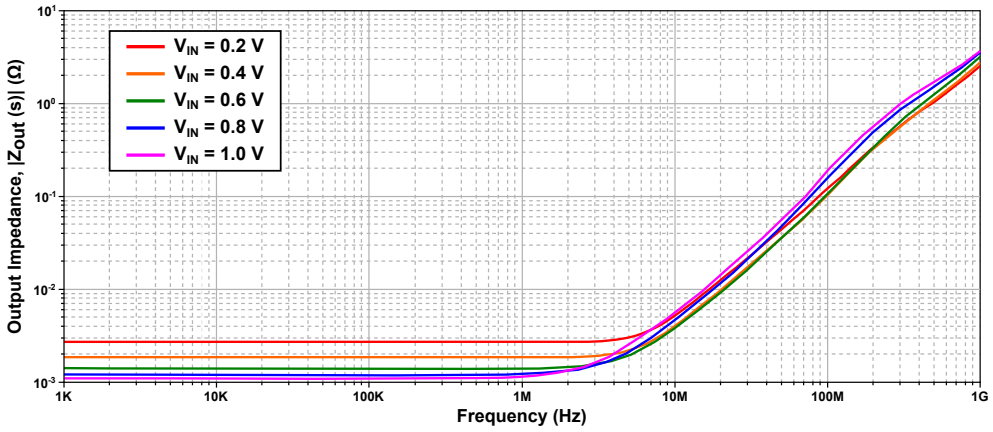


Figure 5.15: Simulated Plot of Closed-loop Output Impedance ($Z_{OUT}(s)$).

Miller, the Miller feedback to the actual gain node gives the maximum feedback factor of 1. With cascoded Miller, the cascode transistor buffers the Miller capacitor current and feeds this current into equivalent capacitor (C_g) at the gain node, which converts it back to a voltage. So when $C_{m2} > C_g$, the maximum feedback factor can be larger (than 1) by a factor C_{m2} / C_g. This in turn shifts the output pole of the cascoded Miller compensated amplifier to a frequency which is a factor C_{m2} / C_g larger than the output pole of an amplifier with simple Miller compensation. This permits a higher unity gain frequency and decreases the output impedance of the amplifier. The resulting LA has a unity gain frequency of 230−454 MHz as shown in Fig. 5.14 (across whole common-mode range) with 5 Ω ‖ 2 pF load, which is almost 3 times higher than a simple nested Miller compensated amplifier with the same power consumption. As shown in Fig. 5.15, the simulated closed-loop output impedance, $Z_{OUT}(s)$ of the LA is about 0.2 Ω at 100 MHz which is about 20−50 times lower than the PA load, R_{PA}. So it can be safely assumed that all the current ripple is absorbed by the LA and and meets our linearity requirements. The cascoded Miller loop also introduces a second non-dominant pole which occurs due to the finite source impedance of the cascode transistor. However this pole can be placed far from the

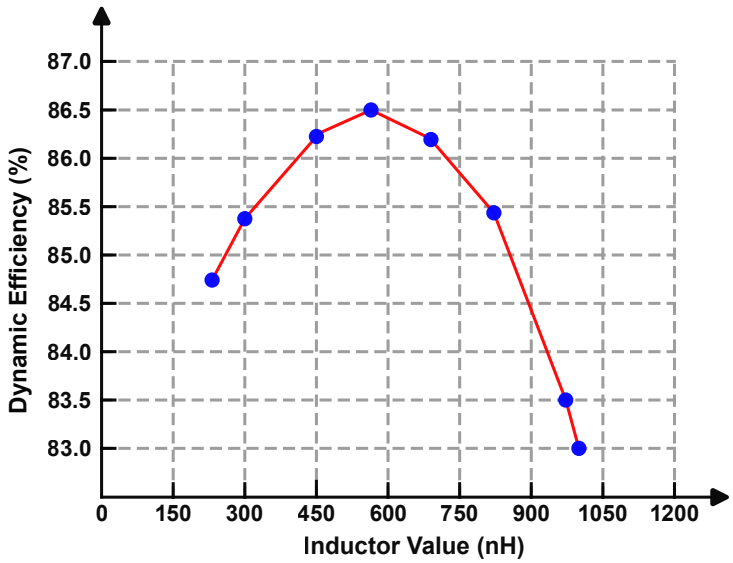


Figure 5.16: Simulated Plot of Dynamic Efficiency of the HSM Against the External Inductor Sweep for LTE 100 MHz Signal

unity gain frequency to avoid stability problems.

5.2.6 Optimization of External Inductor

The power dissipation of the HSM comprises three parts—P_{loss_AB} due to the LA, P_{loss_SA} due to the SA, and P_{loss_ind} due to the external inductor. P_{loss_ind} is due to the parasitic resistance R_{par} of the inductor. The speed-efficiency optimization of the HSM involves the tradeoffs for selecting the external inductor L_{ind}. A small L_{ind} is preferred for wide bandwidth of the SA and a large L_{ind} is preferred to reduce I_{HYS_Delay} [as expressed in eq. 5.2(c)]. In addition, for a given load current (I_{LOAD}) the parasitic resistance of L_{ind} contributes P_{loss_ind} [as expressed in eq. 5.6], and a small L_{ind} is preferred for its relatively small parasitic resistance:

$$P_{loss\_ind} = R_{par} \times I_{LOAD}^2 \tag{5.6}$$

In this paper, the HSM design is optimized for tracking wideband envelope sig-

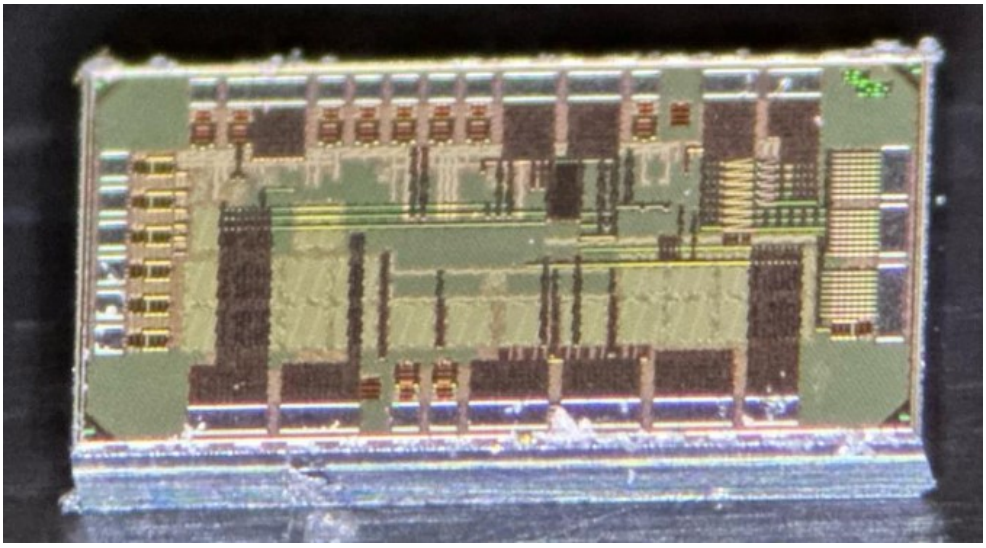


Figure 5.17: Chip Microphotograph of the Proposed HSM

nals. So, the design is simulated with particularly LTE 100MHz signal with various inductors. The parasitic resistance of the external inductor is approximated by $R_{par} \approx 0.05\Omega + 0.01\Omega/\mu H * L_{ind}$ −this is typical for commercial surface mount inductors with sufficient current rating. Based on the simulation results, the dynamic efficiency of the HSM can be plotted and it can be ascertained which inductor needs to be selected to achieve the minimum total power loss. Fig. 5.16 shows the simulated dynamic efficiency for tracking LTE 100 MHz envelope signal with various inductors. As depicted, in simulations the maximum dynamic efficiency of ≈ 85.5% is achieved with 580 nH inductor.

5.3 Measurement Results

The proposed HSM design is implemented in a TSMC 65 nm CMOS process and the die size including I/O pads was 2.05 mm × 1.0 mm. Since, many other circuits are included in die along with HSM, the actual area of HSM (along with I/O pads) is around 1.6 mm^2. The microphotograph of the chip is shown in Fig. 5.17. The HSM is packaged in a 6 mm × 6 mm QFN package and snapshot of the PCB board

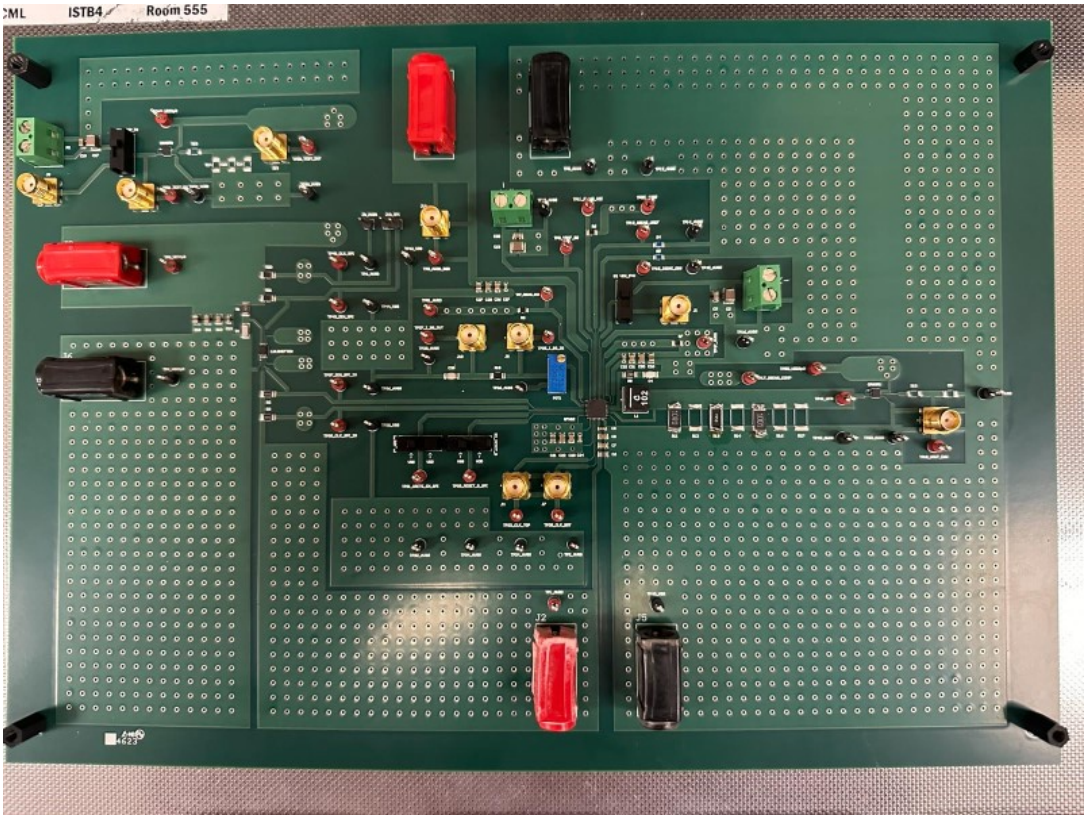


Figure 5.18: Snapshot of the PCB Testing Board

used for testing is depicted in Fig. 5.18. An external inductor of 550 nH, whose dc resistance and self-resonance frequency are 0.06 Ω and 490 MHz, respectively, is selected. The HSM operates with a maximum supply voltage option of 1.2 V and thin gate-oxide devices are used. On-chip decoupling capacitors (≈ 200 pF) are employed to suppress the noises in the supply rails due to the switching of the SA. The HSM is characterized with different resistor loads (4−10 Ω) ∥ 2 pF resembling the supply node impedance of a PA.

Fig. 5.19 depicts a plot of the measured static efficiency of the HSM when tracking different dc input voltages. Three resistive loads 4, 7, and 10 Ω, are used. The 4 Ω load serves to ascertain the driving capability of the HSM, where the HSM provides a maximum output power of 26.2 dBm with ≈ 92.2% efficiency. The performance of

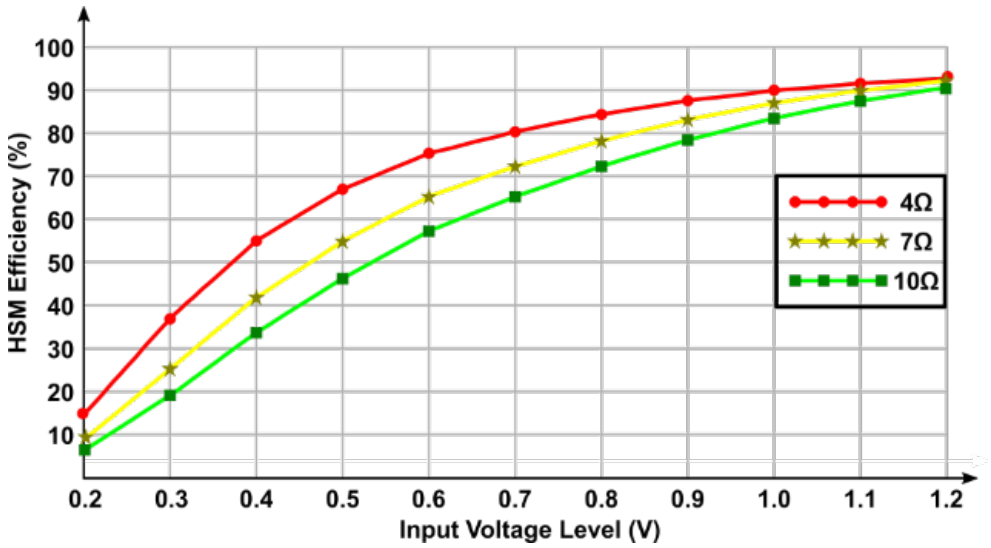


Figure 5.19: Measured HSM Static Efficiency for Different Resisitve Loads

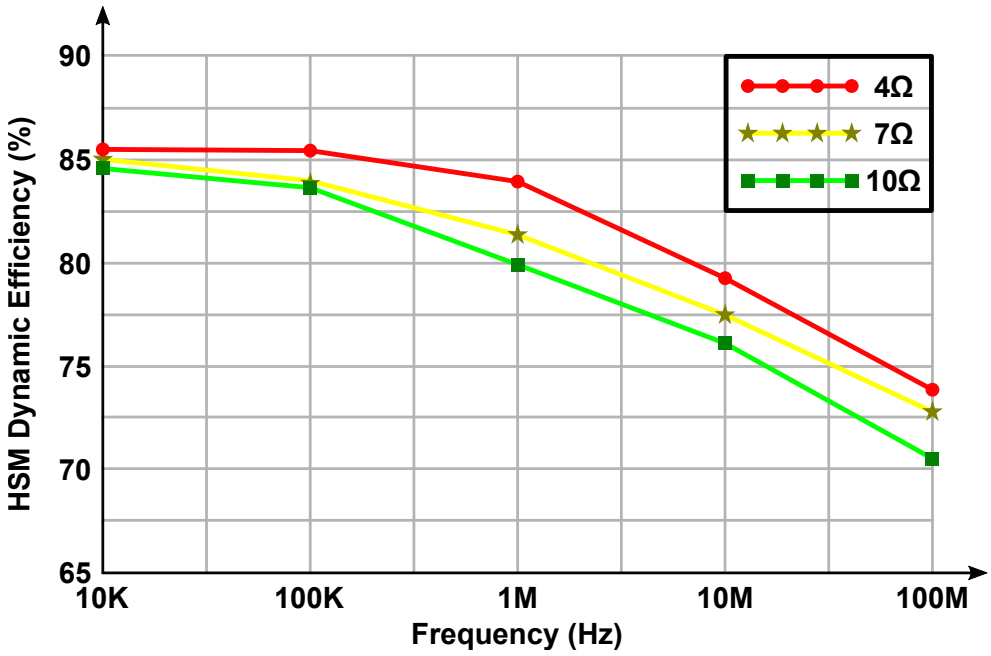
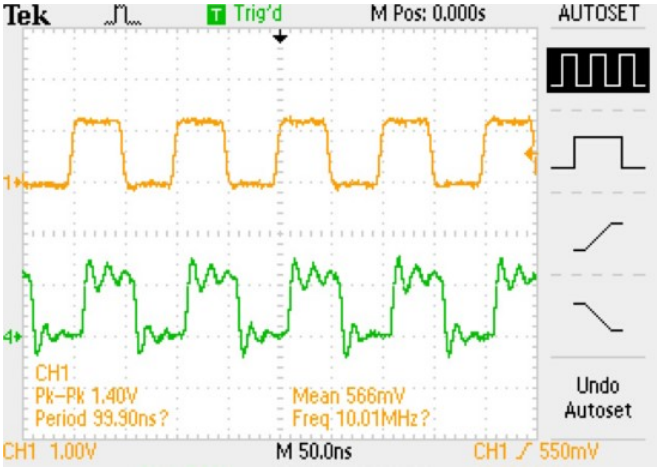
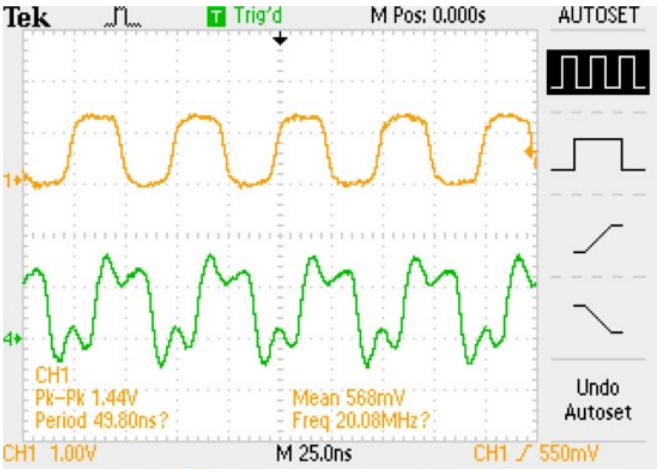


Figure 5.20: Measured HSM Dynamic Efficiency Against the Frequency Sweep

the HSM is also evaluated with single tone sinusoidal signals. Fig. 5.20 shows the measured dynamic efficiency of the HSM when tracking sinusoidal signal of 1 V_{pp} swing till 100 MHz frequency and for different resistive loads. It can easily seen that the proposed HSM maintains $\geq$ 84% at low frequency and $\geq$ 70% while tracking



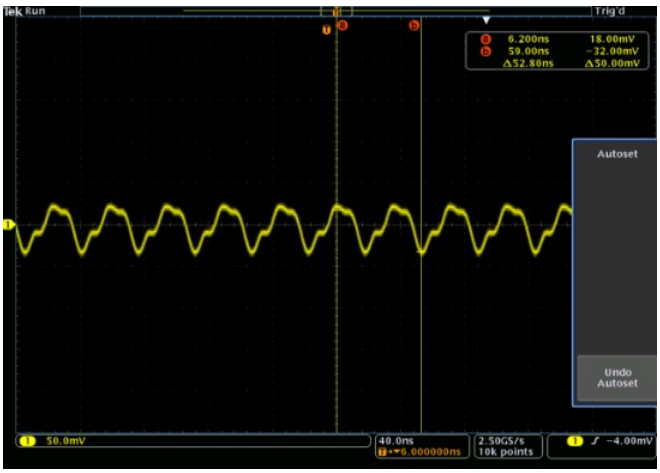
(a)



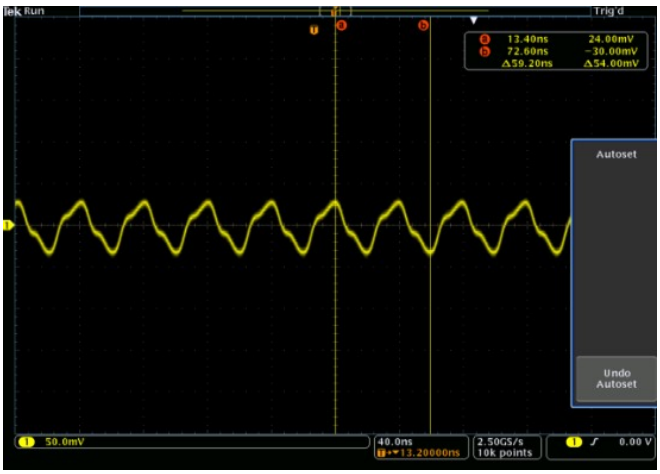
(b)

Figure 5.21: Measured Time-domain Plot of V_{IN} (Yellow) and V_{OUT} (Green) When Tracking Square Pulse of Frequency (a) 10 MHz and, (b) 20 MHz

single tone sinusoidal signal upto desired target frequency of 100 MHz. The large signal stability of the HSM is also verified as can be seen from Fig. 5.21. It can be seen that when the output responds to the input square pulse of frequency 10 MHz and 20 MHz with 1.2 V swing as shown in Fig. 5.21(a) and (b) respectively. The propagation delay between input and output is $\approx$ 7.5 ns. As expected, there is slight ringing and ground-bounce noise, i.e., voltage spikes on the otherwise clean supply rails. This is largely due to the switching operation of the SA and the inductance



(a)

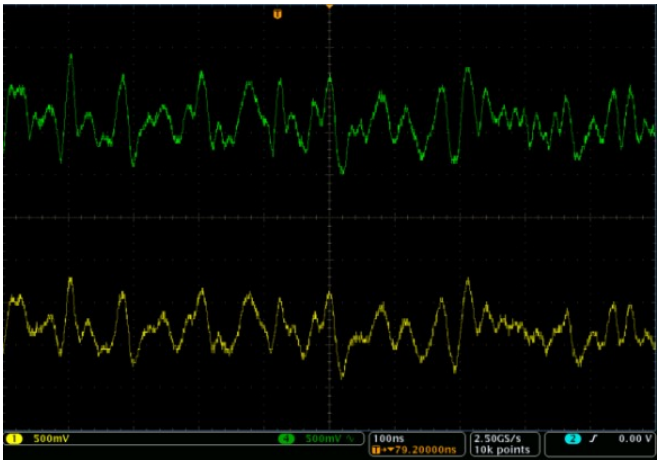


(b)

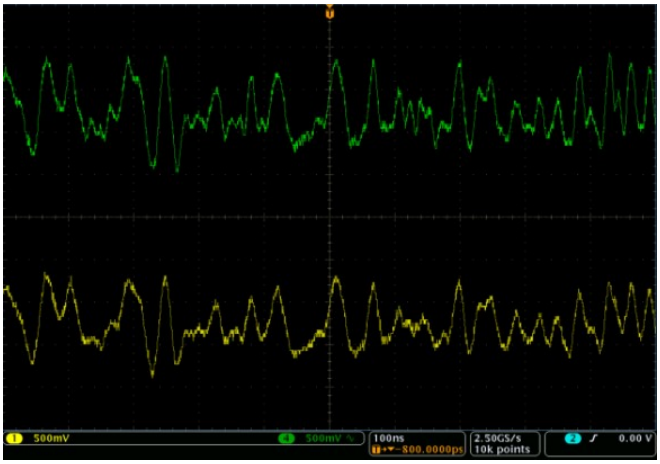
Figure 5.22: Measured Output Voltage Ripple at Different Input Voltages (a) 0.2 V and, (b) 1.0 V

of the bonding wires. In the prototype HSM, the SA is powered separately from the other analog circuits (including the LA and the controller). In the packaging of the prototype HSM, multiple power pins and multiple bonding wires were employed to reduce the bonding wire inductance (hence, reducing the supply and ground bounce).

Fig. 5.22(a) and (b) shows the output voltage ripple at different input voltages of 0.2 V and 1.0 V respectively. The maximum peak-to-peak ripple found was around 54 mV. The observed ripple is higher than the simulated values to improper modelling of the package parasitics, which cause additional ripple to appear at the PA node.



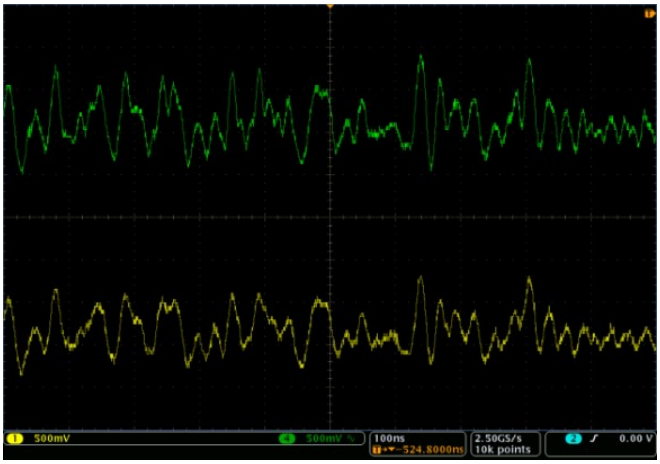
(a)



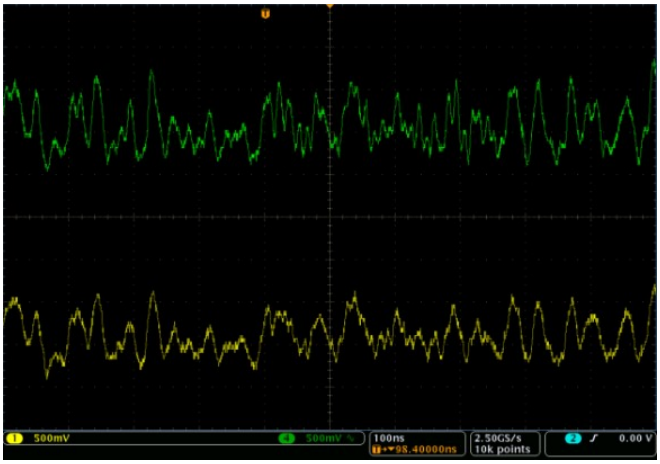
(b)

Figure 5.23: Measured Time-domain Plot of V_{IN} (Green) and V_{OUT} (Yellow) When Tracking LTE Envelope of Bandwidth (a) 20 MHz and, (B) 40 MHz

The waveforms of the input signal and the time-domain response of the HSM tracking an envelope signal extracted from 20/40 MHz 5G NR RF signal are depicted in Fig. 5.23(a) and (b) and 80/100 MHz 5G NR RF signal are depicted in Fig. 5.24(a) and (b). For the modulated signal measurements, the test signal was the envelope of a 5G NR 20/40/80 and 100 MHz 256-QAM modulated signal, whose swing was from $0 - 1.2$ V. In the measurements, the 5 Ω resistor is connected as the load to the HSM. The design is able to track the envelope signals closely and maximum difference was less



(a)



(b)

Figure 5.24: Measured Time-domain Plot of V_{IN} (Green) and V_{OUT} (Yellow) When Tracking LTE Envelope of Bandwidth (a) 80 MHz and, (B) 100 MHz

than 50 mV. The maximum efficiency achieved by the proposed HSM while tracking 100 MHz LTE signal is around 82.9%. The measurements of the prototype HSM are consolidated in Table 5.1 and are benchmarked against the pertinent state-of-the-art designs. The Figure of Merit (F.O.M) used [166] in comparing the performance is:

$$\text{F.O.M} = \frac{\text{Signal BW (MHz)} \times \text{Max Vout (V)} \times \text{Peak Eff (\%)}}{\text{Load Resistance } (\Omega) \times \text{Die Area (mm}^2) \times 100} \tag{5.7}$$

It can be seen that the prototype supply modulator features one of the highest

Table 5.1: Comparison of the Proposed HSM with Prior State-of-the-Art Works

Parameter	[43] TPEL'19	[65] JSSC'19	[70] ISSCC'19	[154] TPEL'20	[155] JSSC'22	[79] ISSCC'22	This Work
Design	Delay Based Hysteresis Control	3-Level	APT + ET	Dual Mode Sigma Delta	APT + ET (with 4^{th} order Filtering	Digital ET using Switch Cap	Dynamic Delay Hysteresis Based
Mode of Control	Current	Voltage	Voltage	Voltage	Voltage	Voltage	Current
CMOS Process	180 nm	65 nm	90 nm	190 nm	90 nm	90 nm	65 nm
Supply Voltage	3.6 V	2.4 V	5.0 V	3.6 V	4.0 V	5.0 V	1.2 V
Max. BW	40 MHz	80 MHz	100 MHz	40 MHz	100 MHz	200 MHz	100 MHz
Switching Levels	2	3	2	2	2	2	2
Peak Static Eff.	91%	–	–	91%	–	–	92.2%
Peak Dynamic Eff.	85%	91%	82%	85%	84.1%	93.6%	82.9%
Output Power	1630 mW	1000 mW	3200 mW	1800 mW	3530 mW	1500 mW	425 mW
Output Ripple	$\approx$ 16 mV	–	–	$\approx$ 18 mV	–	–	$\approx$ 54 mV
Load Resistance	6.7 Ω	4.7 Ω	3.2 Ω	4Ω	3.3 Ω	3.3 Ω	$4 - 10$ Ω
Die Area	2.25 mm^2	4 mm^2	5.145 mm^2	2.3 mm^2	6.74 mm^2	13.6 mm^2	1.6 mm^2
Off-Chip Ind.	1000 nH	538 nH	3 inductors	4700 nH	4 inductors	4 inductors	550 nH
Capacitor	100 pF (off-chip)	12 nF (on-chip)	AC Coupled + Load (off-chip)	100 pF (off-chip)	1 AC Coupled + 2 Load (off-chip)	4.7 uF (off-chip)	none
F.O.M	7.44	9.29	15.93	9.91	12.90	20.64	16.83

performance among all the published works presented in the table for three imperative parameters−high tracking 100 MHz bandwidth, high 92.2% maximum efficiency and, small die-area of 1.6 mm^2. In short, the proposed HSM design is highly competitive.

Chapter 6

CONCLUSION

Envelope tracking techniques provide a solution for improving the efficiency of a PA system under power back-off conditions. One of the major benefits of ET is its compatibility with handset applications, which makes it amongst the most popular efficiency enhancement techniques, and the most widely implemented enhancement technique to-date.

This work reviews the hybrid supply modulator, which is the most popular supply modulator architecture for implementation of ET-PA systems. This paper summarizes the HSM's theory of operation, categorizes the various HSM architectures, and details the advancements in HSM topologies for maximizing HSM performance. The state-of-the-art HSM implementations are thoroughly compared in Table 4.2 with respect to achieved performance. Finally, the challenges for ET-PA system implementation and integration of the SM with PA are also highlighted.

A hybrid supply modulator for wideband LTE applications is proposed. A dynamic hysteresis control method is developed and conventional controller design is moved to current mode. Combined operation provides a faster and efficient tracking of the input envelope. Furthermore, a enhanced LA structure is designed to track wideband signals support tracking capability of 100 MHz bandwidth for LTE signals. The circuit removes the need for any extrinsic hysteresis circuit, which circumvents the needs for hysteretic comparator and intrinsic hysteresis window of delay-based comparator is used which can be dynamically varied. A dynamic current generator block is implemented which can source/sink the current into the comparator and instantaneously varies the switching frequency of supply modulator in case of tran-

sients, to improve the slew-rate. The measurement results show the tracking of LTE 100 MHz envelope and achieving a high efficiency of 92.2%. With the power supply of 1.2 V, the HSM can provide a maximum output power of 26.2 dBm and taking a small die-area of 1.6mm^2.

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