Advanced Power Amplifier Architectures to Support 5G+ Cellular Infrastructure

by

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ABSTRACT

The world has seen a revolution in cellular communication with the advent of 5G, which enables gigabits per second data speed with low latency, massive capacity, and increased availability. Complex modulated signals are used in these modern communication systems to achieve high spectral efficiency, and these signals exhibit high peak to average power ratios (PAPR). Design of cellular infrastructure hardware to support these complex signals therefore becomes challenging, as the transmitter's radio frequency power amplifier (RF PA) needs to remain highly efficient at both peak and backed off power conditions. Additionally, these PAs should exhibit high linearity and support continually increasing bandwidths. Many advanced PA configurations exhibit high efficiency for processing legacy communications signals. Some of the most popular architectures are Envelope Elimination and Restoration (EER), Envelope Tracking (ET), Linear Amplification using Non-linear Component (LINC), Doherty Power Amplifiers (DPA), and Polar Transmitters. Among these techniques, the DPA is the most widely used architecture for base-station applications because of its simple configuration and ability to be linearized using simple digital pre-distortion (DPD) algorithms. To support the cellular infrastructure needs of 5G and beyond, RF PAs, specifically DPA architectures, must be further enhanced to support broader bandwidths as well as smaller form-factors with higher levels of integration. The following four novel works are presented in this dissertation to support RF PA requirements for future cellular infrastructure:

1. A mathematical analysis to analyze the effects of non-linear parasitic capacitance (C_{ds}) on the operation of continuous class-F (CCF) mode power amplifiers and identify their optimum operating range for high power and efficiency.

2. A methodology to incorporate a class-J harmonic trapping network inside the

PA package by considering the effect of non-linear C_{ds}, thus reducing the DPA footprint while achieving high RF performance.

3. A novel method of synthesizing the DPA's output combining network (OCN) to realize an integrated two-stage integrated LDMOS asymmetric DPA.

4. A novel extended back-off efficiency range DPA architecture that engineers the mutual interaction between combining load and peaking off-state impedance. The theory and architecture are verified through a GaN-based DPA design.

DEDICATION

To my wife, Sadiya

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INTRODUCTION

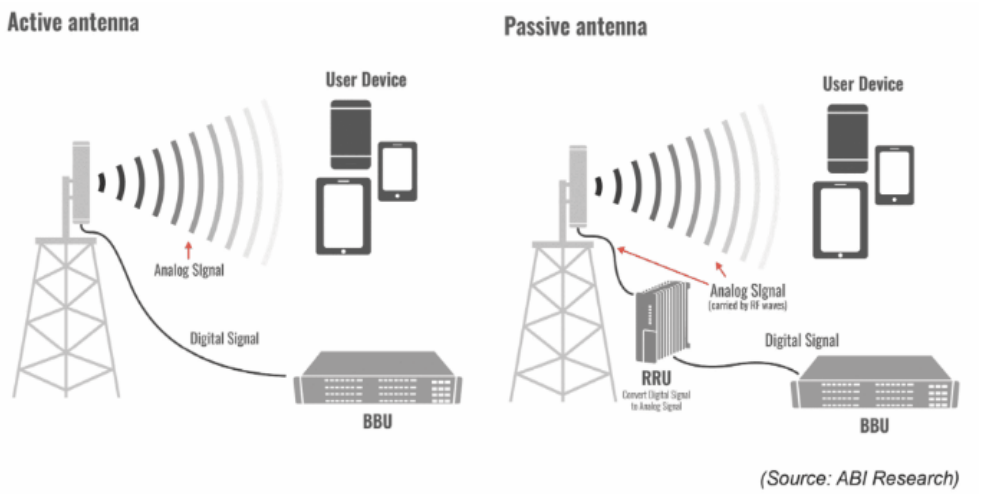

Figure 1.1: Active vs Passive Antenna

With the rapid proliferation of the modern cellular communication networks, 5G/5G+ networks are employing active antenna systems (AAS) to improve the end-user experience, capacity, and coverage. These systems use powerful techniques such as state-of-the-art beamforming and multiple-input multiple-output (MIMO) architectures. In passive antenna systems, the Remote Radio Unit (RRU) and the passive components (antenna) are independent components, whereas in AAS, the RRU and antenna elements are integrated in a single radio unit, as illustrated in Figure 1.1. By putting the antennas near to or integrated with the RF modules, the AAS improves the communication throughput and reduces power consumption as well as cable loss. There is also a growing demand to reduce the weight of these AAS-based radio units for simplified installation, reduced tower loading, and improved tower utilization. Since power amplifiers (PAs) are the most power-hungry block in a radio transceiver,

Table 1.1

Basic PA Classes

Class	I_{dq}	Conduction Angle	Efficiency %
A	$\frac{I_{max}}{2}$	2π	50 %
AB	0 to $\frac{I_{max}}{2}$	π to 2π	50% to 78.54%
B	0	π	78.54 %
C	0	0 to π	78.54 % to 100%

there is a growing need for the development of high efficiency RF power amplifiers (PAs) with compact footprint to meet these stringent AAS requirements. These PAs should be invented to enable higher level of integration and reduction in radio unit size/weight/cost, while also increasing network capacity.

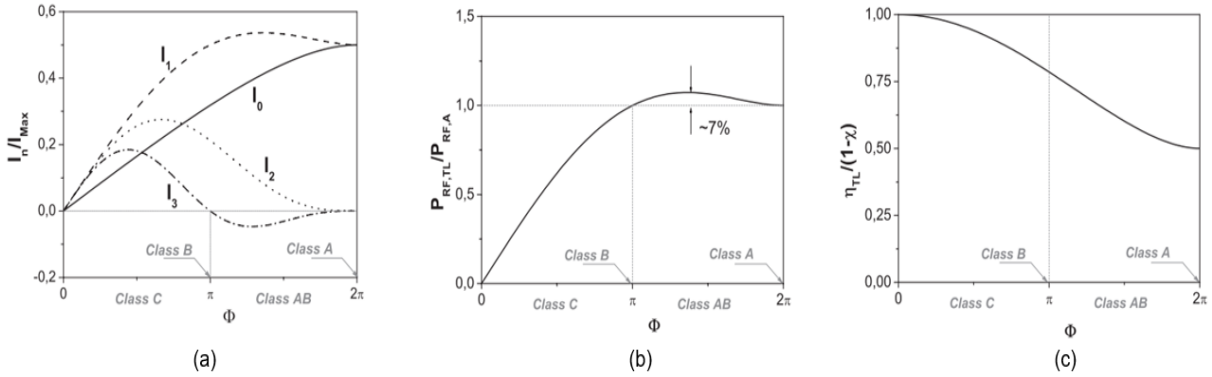

Figure 1.2: (a) Normalized fourier current components, (b) normalized power with respect to class-A, and (c) Efficiency for different classes of operation

Background

Linear RF PAs can be generally divided into four classes of operation based on the PA's bias condition. The main classes are class-A, class-B, class-AB and class-C. In

the discussion of these basic classes of operation, it's assumed that the higher order harmonics are short-circuited in the current generator plane. This short circuited harmonic condition is also dubbed as "tuned class-B" operation for simplification. Table 1.1 shows quiescent current (I_{dq}), conduction angle and efficiency for different classes of PA operation. In Figure 1.2, the normalized Fourier current, power, and efficiency are plotted with respect to conduction angle. As conduction angle decreases from class-A to class-C, efficiency goes up, while linearity degrades. Therefore, a strong trade-off between efficiency and linearity exists in these classes of operation. To improve the efficiency and to relax the efficiency-linearity trade-off, advanced PA design techniques are required.

Efficiency improvement techniques can be divided into two major categories. In the first category, the higher order harmonics are manipulated to engineer the voltage and/or current waveforms to improve the PA's performance. These kind of PAs are generally called harmonic tuned PAs. Harmonic tuned PAs were originally targeted for saturated PA operation. When a PA becomes saturated, higher order harmonics are abundantly generated and voltage /current waveforms can be significantly engineered by controlling their harmonics. However, in harmonic tuned PAs, very stringent fundamental and higher order harmonic load conditions need to be imposed, which can be a challenge for practical applications. To circumvent this limitation, the idea of continuous-mode PAs was introduced. Continuous-mode PAs can achieve the same high performance as basic harmonic tuned PAs while allowing more flexibility in impedance conditions. The second category of efficiency improvement techniques is focused on output power backoff (OBO) operation. Envelope Elimination and Restoration (EER), Envelope Tracking (ET), Linear Amplification using Non-linear Component (LINC), Doherty Power Amplifiers (DPA), Polar Transmitters, etc. are some of the techniques that fall into this category. For these techniques, a 'tuned

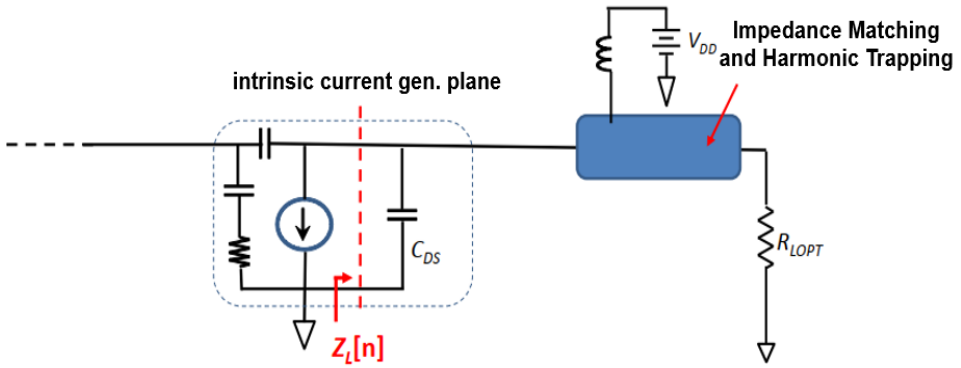

Figure 1.3: Simple PA output model

class-B" operation is generally assumed, which means that only the fundamental components are considered and higher order harmonics are short-circuited (negligible). In these architectures, one or more PAs are utilized and load impedance and/or bias voltage is modulated with respect to power level to improve the overall PA's performance. Among these architectures, DPAs are widely used in cellular infrastructure applications due to their simple configuration with high output back-off efficiency. They do not require fast switching regulators to track the envelope signal like ET amplifiers or very stringent phase accuracy required in a LINC amplifier. Moreover, these other architectures also need complicated DPD algorithms for linearization, which is typically not required for DPAs. Because of these inherent architectural advantages, DPAs have become the most popular choice for cellular infrastructure applications. As this thesis is focused on applications for cellular infrastructure, the discussion on OBO efficiency improvement will be limited to DPAs.

In the next section, the fundamental ideas behind harmonic tuned PAs and continuous-mode PAs will be discussed in detail. In the subsequent section, the DPA operating principle is introduced. In DPA operation, the carrier amplifier becomes moderately compressed/saturated at OBO at the on-set of peaking amplifier turning on. Hence, by combining harmonic tuned/continuous-mode techniques with the DPA

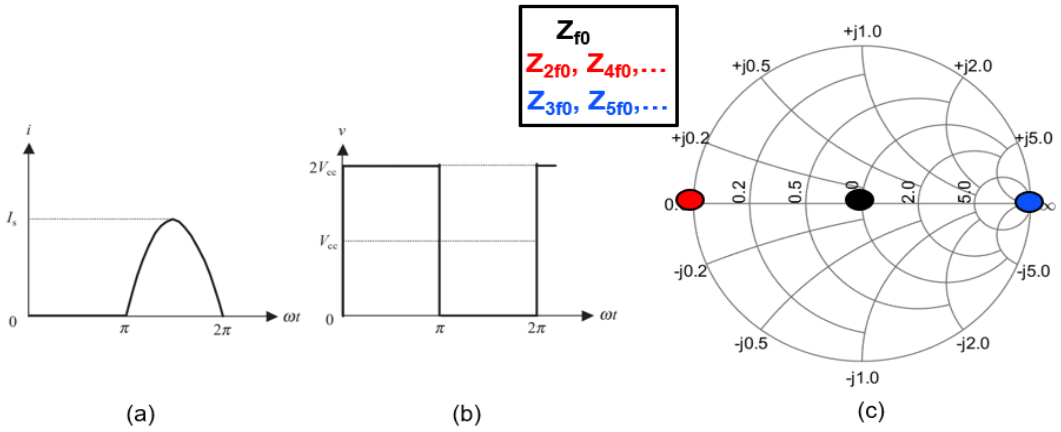

Figure 1.4: Ideal class-F (a) voltage, (b) current, and (c) impedance locations on smith chart

architecture, the OBO efficiency can be further improved. This will be demonstrated in one of the works presented in this dissertation.

1.0.1 Harmonic Tuned and Continuous-mode PA Operation

Compared to class-B/AB amplifiers, harmonic tuned PAs offer better performance (e.g. higher efficiency, power and gain). This can be achieved by providing specific impedance terminations for fundamental and higher order of harmonics to control/shape the drain-source voltage and current waveforms. Theoretically, an infinite number of harmonic terminations are required to achieve the best performance. However, in practice, only a finite number of harmonic controls are possible. Figure 1.3 illustrates a simple PA output model with fundamental impedance matching and harmonic trapping network that would realize certain chosen impedance conditions at the intrinsic current generator plane. There are three main harmonic tuned operations: class-F, class-F^{-1} and class-J. Their detailed operating principles are described below.

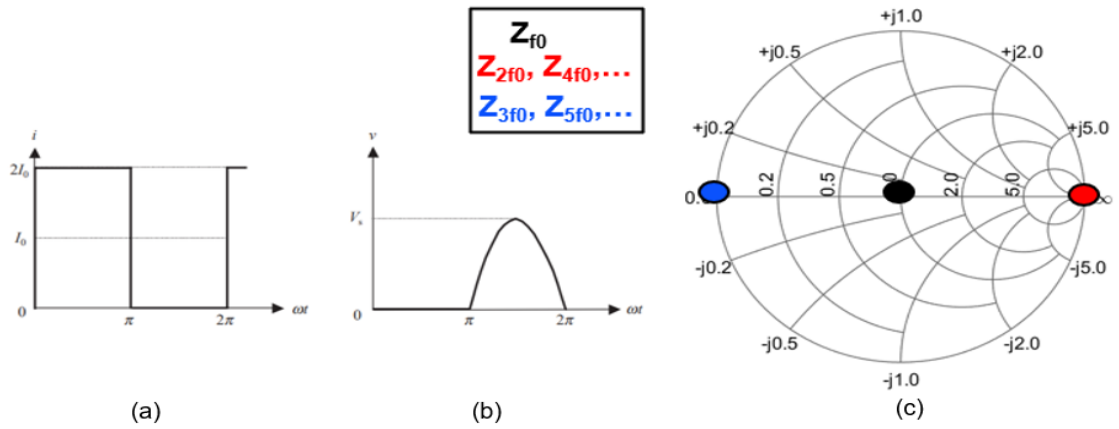

Figure 1.5: Ideal class-F^{-1} (a) current, (b) voltage, and (c) impedance locations on smith chart

Class-F

In a class-F PA, the even-order harmonics are terminated as short circuits and the odd-order harmonics are terminated as open circuits in the current generator plane. The voltage waveform is engineered and with a class-B bias condition (conduction angle of π), the PA results in a square voltage waveform and half-rectified current waveform. Voltage and current waveforms contain only odd and even order harmonics, respectively. The ideal voltage and current waveforms and the impedance locations for class-F operation are shown in Figure 1.4. Ideally, infinite number of harmonics need to be terminated for class-F operation. However, in reality, only $2f_0$ and $3f_0$ can be controlled. With $2f_0$-$3f_0$ terminated, the time-domain voltage and current for class-F operation can be expressed as (1.1) and (1.2), where $\theta = 2\pi f_0 t$. A $2f_0$-$3f_0$ class-F PA can ideally achieve 90.69 % efficiency.

$$v_{ds,classF} = V_{dd}(1 - \frac{2}{\sqrt{3}}\cos(\theta) + \frac{1}{3\sqrt{3}}\cos(3\theta)) \tag{1.1}$$

$$i_{ds,classF} = I_{max}(\frac{1}{\pi} + \frac{1}{2}\cos(\theta) + \frac{2}{3\pi}\cos(2\theta)) \tag{1.2}$$

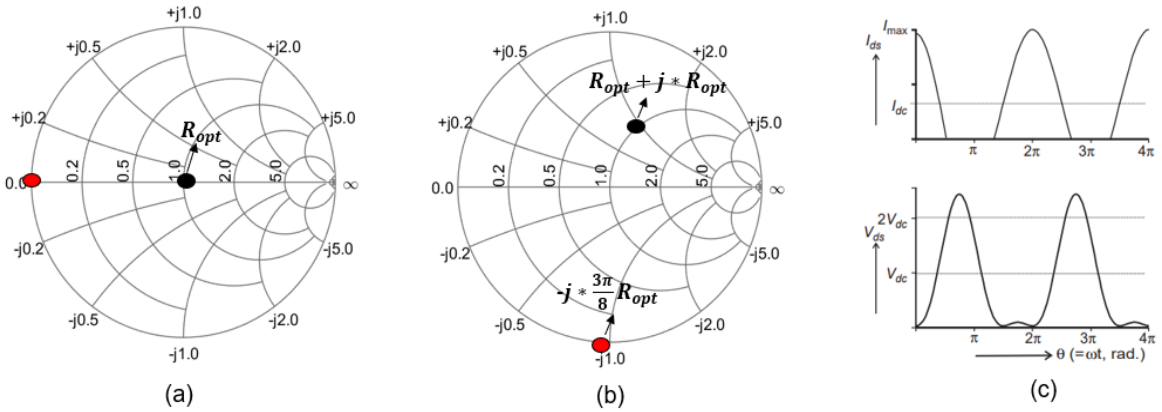

Figure 1.6: f_0 (black) and $2f_0$ (red) impedance locations on smith chart for (a) class-B, (b) class-J, and (c) voltage and current waveforms for class-J

Class-F^{-1}

A class-F^{-1} PA is the dual (often called inverse) of a class-F PA. In class-F^{-1}, the odd-order harmonics are terminated as short circuits and the even-order harmonics are terminated as open circuits in the current generator plane. Considering class-B bias condition (conduction angle of π), the PA results in a square current waveform and half-rectified voltage waveform. Voltage and current waveforms contain only even and odd order harmonic components, respectively. The ideal voltage and current waveforms and the impedance locations for class-F^{-1} operation are shown in Figure 1.5. Similar to class-F, only $2f_0$ and $3f_0$ control is feasible for class-F^{-1} PAs. With harmonic controls being limited to $2f_0$ and $3f_0$, the voltage and current waveforms for class-F^{-1} operation can be expressed as (1.3) and (1.4), where $\theta = 2\pi f_0 t$. A $2f_0$-$3f_0$ class-F^{-1} PA can ideally achieve 81.69 % efficiency.

$$v_{ds,classF^{-1}} = V_{dd}(1 + \sqrt{2}cos(\theta) + \frac{1}{2}\cos(2\theta)) \tag{1.3}$$

$$i_{ds,classF^{-1}} = I_{max}(0.3676 - 0.4246cos(\theta) + 0.0707cos(3\theta)) \tag{1.4}$$

Class-J

The idea of engineering the class-B voltage waveform and achieving the same performance as class-B with different load conditions was first introduced by Cripps [1]. This class of harmonic tuned PA operation is called class-J. Instead of a short-circuit $2f_0$ load condition as in class-B, in class-J operation, the $2f_0$ load is terminated in the inductive region. At the same time, the f_0 load is terminated in the capacitive region. This results in voltage peaking and partial overlap between voltage and current waveforms. However, the power and efficiency remain the same as class-B. Class-J produces the same 78.54 % theoretical efficiency as a class-B PA. The impedance locations on the smith chart and voltage and current waveforms are plotted in Figure 1.6. Time domain voltage and current expressions for class-J operation can be found in (1.5) and (1.6).

$$v_{ds,classJ} = V_{dd}(1 - cos(\theta))(1 - sin(\theta)) \tag{1.5}$$

$$i_{ds,classJ} = I_{max}(\frac{1}{\pi} + \frac{1}{2}\cos(\theta) + \frac{2}{3\pi}\cos(2\theta)) \tag{1.6}$$

From class-J operation, it's evident that for harmonic tuned operation, harmonics do not need to be strictly at short/open circuit regions. This finding expands the design space for PAs and allows for more PA design flexibility and maximized PA performance when designing with practical limitations of active (power) devices and passive structures. Expanding upon this idea, Cripps and other PA researchers established the continuous mode theory. There can be many solutions for fundamental and harmonic load conditions that can produce the same performance. There are three main continuous mode operations: class-BJ/continuous class-J, continuous class-F (CCF) mode and continuous class-F^{-1} (CCF^{-1}) mode.

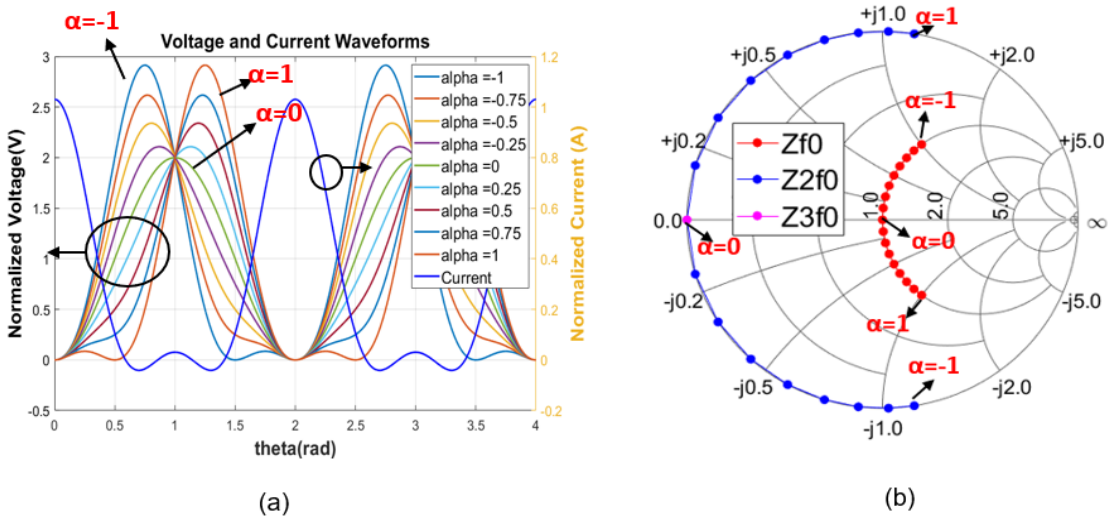

Figure 1.7: Class-BJ (a) voltage and current waveforms, (b) impedance locations on smith chart

Class-BJ/continuous class-J

In class-BJ operation, the time domain class-B voltage waveform is multiplied by $1-\alpha sin(\theta)$, where α is called the continuous mode parameter, and included in (1.7). This creates a series of voltage waveforms and the design space is expanded. The current waveform remains unchanged, as shown in (1.8). The current and voltage waveforms for class-BJ operation are plotted in Figure 1.7 (a). Each voltage waveform represents a pair of fundamental and second harmonic impedances on the smith chart, which are shown in Figure 1.7 (b).

$$v_{ds,classBJ} = V_{dd}(1-cos(\theta))(1-\alpha sin(\theta)), \quad -1 \leq \alpha \leq 1 \tag{1.7}$$

$$i_{ds,classBJ} = I_{max}(\frac{1}{\pi} + \frac{1}{2}\cos(\theta) + \frac{2}{3\pi}\cos(2\theta)) \tag{1.8}$$

Continuous class-F (CCF) mode

In CCF operation, the time domain class-F voltage waveform is multiplied by $1-\alpha sin(\theta)$, as shown in (1.9). Similar to class-BJ, this creates a series of voltage wave-

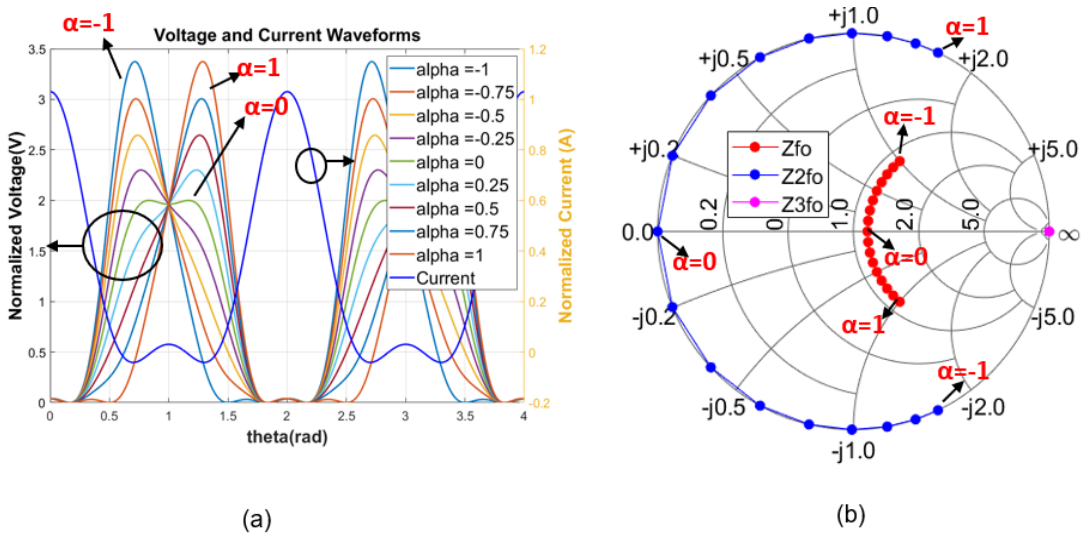

Figure 1.8: CCF (a) voltage and current waveforms, (b) impedance locations on smith chart

forms and the design space is expanded. The current waveform remains half-rectified, as presented in (1.10). The current and voltage waveforms for CCF operation are plotted in Figure 1.8 (a). Each voltage waveform represents a pair of fundamental and second harmonic impedances on the smith chart, which are shown in Figure 1.8 (b).

$$v_{ds,CCF} = V_{dd}(1 - \frac{2}{\sqrt{3}}\cos(\theta) + \frac{1}{3\sqrt{3}}\cos(3\theta))(1 - \alpha\sin\theta), \quad -1 \leq \alpha \leq 1 \tag{1.9}$$

$$i_{ds,CCF} = I_{max}(\frac{1}{\pi} + \frac{1}{2}\cos(\theta) + \frac{2}{3\pi}\cos(2\theta)) \tag{1.10}$$

Continuous class-F^{-1} (CCF^{-1}) mode

Unlike class-BJ and CCF, in CCF^{-1} operation, the time domain class-F^{-1} current waveform is multiplied by $1 - \alpha sin(\theta)$, as shown in (1.12). This creates a series of current waveforms and the design space is expanded. The voltage waveform remains half-rectified, as presented in (1.11). The current and voltage waveforms for CCF^{-1} operation are plotted in Figure 1.9 (a). Each current waveform represents a pair of fundamental and second harmonic impedances on the smith chart, which are shown

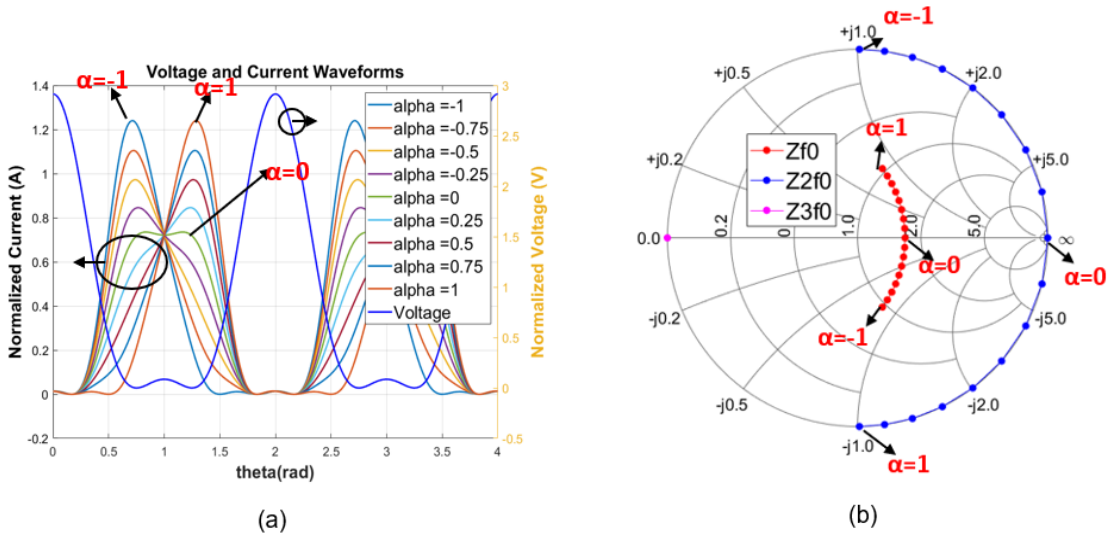

Figure 1.9: CCF^{-1} (a) voltage and current waveforms, (b) impedance locations on smith chart

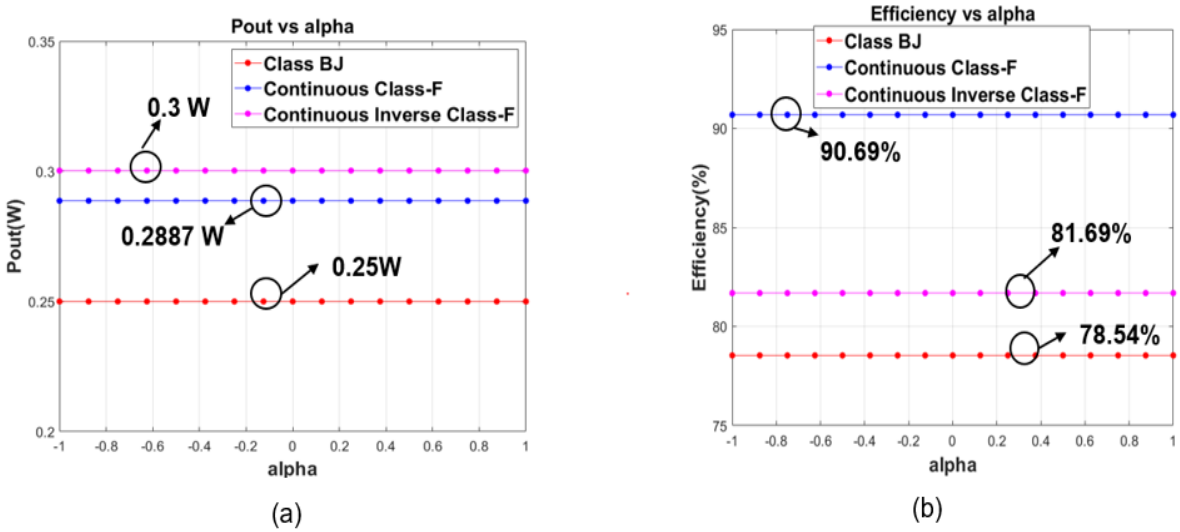

Figure 1.10: (a) Normalized output power, and (b) efficiency for all continuous mode PAs

in 1.9 (b).

$$v_{ds,CCF^{-1}} = V_{dd}(1 - cos(\theta)) \tag{1.11}$$

$$i_{ds,CCF^{-1}} = I_{max}(0.3676 - 0.4246cos(\theta) + 0.0707cos(3\theta))(1 - \alpha \sin\theta), \quad -1 \leq \alpha \leq 1 \tag{1.12}$$

Normalized output power and efficiency for different continuous mode PAs with

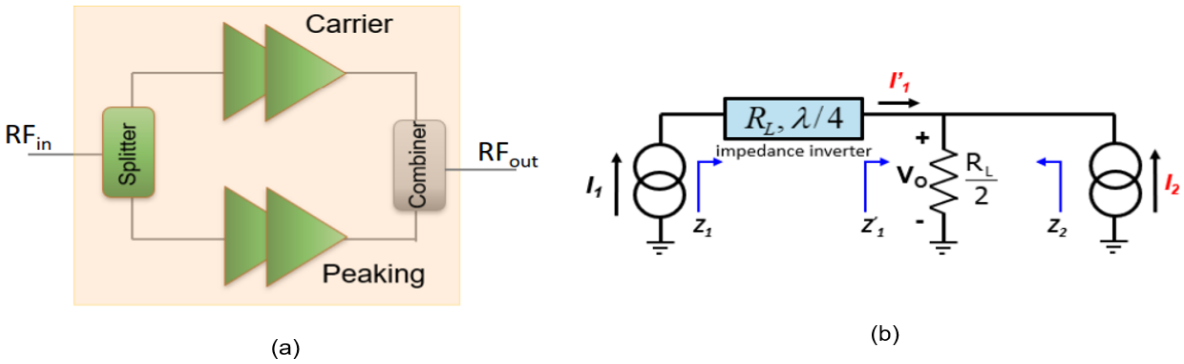

Figure 1.11: (a) A DPA block diagram, and (b) a simplified current source model of a DPA

respect to α are plotted in Figure 1.10. It's evident that ideally with the variation of α, power and efficiency remain constant in continuous mode PAs. This allows for enhanced design flexibility.

1.0.2 Fundamental Operation of the Doherty Power Amplifier

Invented in 1936 by William H. Doherty, Doherty amplifiers gained popularity in the mid-2000s as the preferred PA choice for cellular infrastructure. This choice was motivated by the DPA's higher efficiency at high power back-off level. Currently in cellular base-stations (BTS), only Doherty amplifiers are being used for power amplification. Figure 1.11 (a) depicts a block diagram of a DPA. There are two amplifiers involved: the carrier amplifier and the peaking amplifier. Generally, the carrier amplifier is biased in class-B/AB and the peaking amplifier is biased in class-C. The DPA's behavior is a function of input power and is divided into two regions: saturation when both devices are supplying their maximum power, and back-off power when the peaking device is turned off and only the carrier amplifier is producing power. For a symmetric Doherty PA in which the carrier and peaking amplifiers are of the same size, the break point between this saturation and back-off level happens at a power level 6dB before (lower) than the saturation point. For the Doherty to be ef-

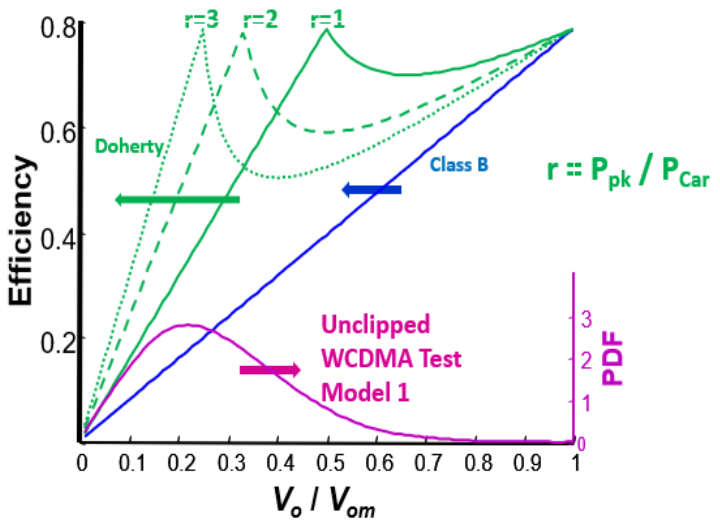

Figure 1.12: DPA efficiency with respect to normalized output voltage for different power ratio

fective, the real part of the output impedance at the intrinsic current generator plane of the carrier amplifier needs to have a high impedance before the break-point. At saturation, both amplifiers should see the optimum impedance for maximum power generation. Thus, when the input power changes from low to high power, the output combiner allows for load modulation of the output impedance of the carrier and auxiliary amplifiers. The Doherty is therefore referred to as a load-modulation technique.

Figure 1.11 (b) shows a simple current source model of the DPA with output combiner. I_1 and I_2 represent carrier and peaking amplifiers, respectively. The different impedances at the current source plane and the combiner planes, as annotated in Figure 1.11 (b), can be expressed as:

$$Z_1' = \frac{R_L}{2}\left(\frac{I_1' + I_2}{I_1'}\right) \tag{1.13}$$

$$Z_1 = \frac{R_L^2}{Z_1'} \tag{1.14}$$

$$Z_2' = \frac{R_L}{2}\left(\frac{I_1' + I_2}{I_2}\right) \tag{1.15}$$

DPA efficiency with respect to normalized output voltage (V_o/V_{om}) is plotted in

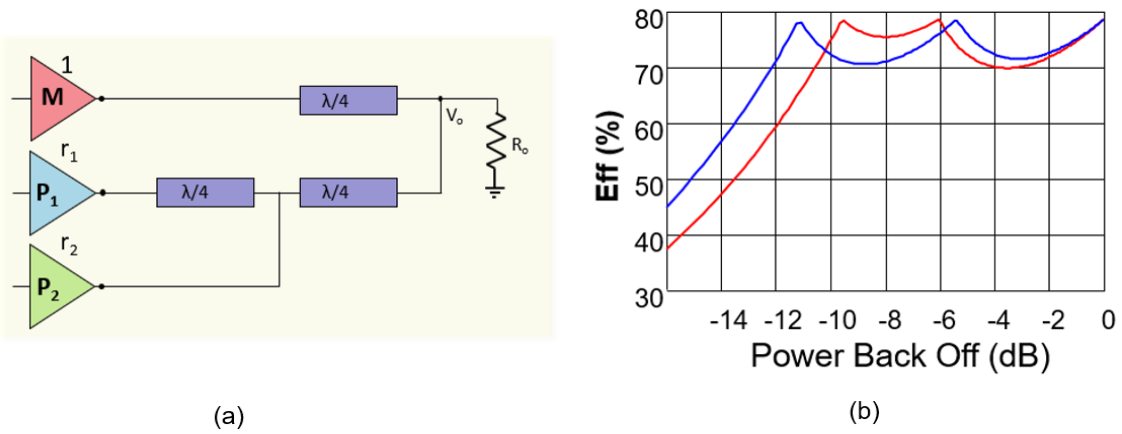

Figure 1.13: 3-way DPA, (a)block diagram, and (b) efficiency for different power ratio

Figure 1.12. Class-B amplifier efficiency is also with respect to normalized PA output power is given in the same plot. The plot demonstrates that efficiency for the class-B PA is poor at the OBO condition, which makes it unsuitable for modulated signals with variable envelope (power). By utilizing load modulation, DPAs can achieve additional efficiency peaking at OBO and thus drastically improve PA performance from a class-B configuration. For conventional DPAs, the efficiency peaking at OBO is a function of peaking to carrier power ratio (r). OBO range can be extended by increasing the asymmetry (r). The PDF of an unclipped WCDMA test model (pink) is also plotted on Figure 1.12. To get the optimum efficiency performance, the DPA architecture should be chosen such that the efficiency peaking at back-off is aligned with the maxima of the PDF of the modulated signal in use. With the symmetric configuration (r=1) efficiency peaking happens at V_o/V_{om}=0.5 or at 6 dB OBO. An asymmetric configuration (r>1) is thus generally required to get the best performance with high PAPR modulated signals that are used in cellular infrastructure.

Multi-way or multi-stage DPAs are used to further extend the DPA efficiency range. Instead of using one carrier and one peaking amplifier as in a 2-way DPA, multi-way DPAs include more than one peaking amplifier to introduce multiple peaks

at back-off powers. For example, a 3-way DPA block diagram is presented in Figure 1.13 (a). r_1 represents the power ratio between the first peaking PA and carrier PA, and r_2 represents the ratio between the second peaking PA and carrier PA. the efficiency plot of a 3-way DPA with respect to power back-off (dB) is plotted in Figure 1.13 (b). There are two efficiency peaks in the back-off region. By controlling the two power ratios (r_1 and r_2), the locations of the efficiency peaks can be controlled/chosen.

These conventional two-way and multi-way architectures suffer from some direct trade-offs between different design parameters. Moreover, the ideal harmonic tuned and continuous mode PA theories that were discussed earlier do not take into account some of the inherent non-linearities (and non-idealities) present in a real transistor. It's important to address these issues in a detailed mathematical manner to understand the nature of the limiting factors and innovate refined architectures to circumvent these pracitical implementation issues. It's also important, especially for 5G+ applications, to develop compact PA and combiner architectures that allow for a reduced overall DPA footprint.

1.1 Organization of the Work

This dissertation includes four power amplifiers (PAs) that demonstrate state-of-the art performance for wireless communication infrastructure, as they focus on the improvement of efficiency and reduction of the PA's physical footprint. The organization of the following chapters is as follows. In Chapter 2, a detailed mathematical analysis of non-linear C_{ds} effect is presented for continuous mode class-F (CCF) PAs. From mathematical analysis, it is shown that by utilizing the non-linearity of C_{ds}, the PA performance can be enhanced in certain operating conditions compared to ideal CCF operation. Chapter 3 presents a design approach used to realize a highly efficient Gallium Nitride (GaN) based class-J Doherty Power Amplifier (DPA), delivering +45

dBm peak power at 3.5 GHz, which supports 5G mMIMO small-cell infrastructure transmitters. The DPA is implemented in a compact form factor with all circuitry, excluding the output combiner and input splitter, placed in a 7 mm x 7 mm quad-flat no-leads (QFN) plastic encapsulated package. A circuit topology is presented to realize the class-J network inside the package, including the non-linearity of C_{ds} for enhanced performance.

In Chapter 4, a compact output combining network for a packaged integrated asymmetric DPA is presented. A new method is introduced for the combining network that absorbs part of the peaking amplifier's C_{ds} into the impedance transformer, thus extending the C-L-C based "C_{ds} absorption" technique to asymmetric DPAs. Based on the proposed combining network, a two-stage LDMOS integrated asymmetric DPA was designed, fabricated, and measured for a 2.6 GHz band of operation.

In Chapter 5, a novel extended back-off efficiency range Doherty power amplifier (DPA) is presented that engineers the mutual interaction between peaking off-state impedance and combining load impedance. A generic analysis to establish the theory of operation shows that unique closed form relationship can be established between peaking off-state impedance and combining load impedance. Compared to prior extended back-off Doherty works, the proposed theory introduces an expanded design space that renders flexibility to incorporate multiple frequency points to improve the bandwidth performance. Moreover, the generic analysis also covers any arbitrary combining current ratios for carrier and peaking amplifiers, thus making the proposed combining approach suitable for both symmetric and asymmetric configurations. To corroborate the theory, a proof-of-concept prototype DPA with an asymmetric configuration was designed using commercially available packaged Gallium Nitride (GaN) High-Electron-Mobility Transistors (HEMT) for 1.7-2 GHz operation.

Chapter 2

NON-LINEAR C_{DS} EFFECT ON CONTINUOUS CLASS-F MODE POWER AMPLIFIERS

2.1 Introduction

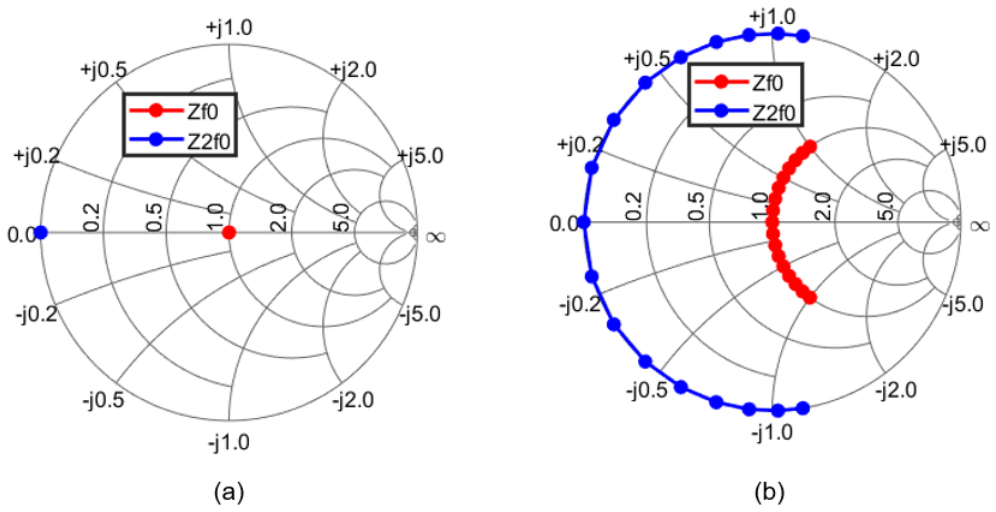

Figure 2.1: Fundamental and harmonic locations for (a) class-B PA, and (b) class-BJ PA

Parasitic capacitances such as drain-source capacitance (C_{ds}), gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}) are always present in a real transistor. Ideal PA theories targeted for harmonic tuned power amplifiers have been developed using the current-generator plane of a transistor, without taking these parasitic capacitances into account. However, if these parasitic capacitances possess linear behavior, they can be easily de-embedded to get access to the current-generator plane for establishing the ideal high performance condition, which is what is performed in most design techniques. However, for many devices, these parasitic capacitances show significant non-linearity that cannot be ignored. This is especially prominent with the

effect of C_{ds} non-linearity on continuous mode power amplifiers, and with the high nonlinearity of C_{ds} in gallium nitride (GaN) and LDMOS devices. The motivation of this work is to mathematically analyze the effect of non-linear C_{ds} on the operation of continuous class-F (CCF) mode PA operation, which provides design insight and a new set of design constraints to achieve optimized CCF performance.

In a class-B amplifier, the conduction angle of the amplifier is π and the fundamental impedance is R_{opt}, where

$$R_{opt} = \frac{2V_{dd}}{I_{max}} \tag{2.1}$$

Here, V_{dd} and I_{max} are the drain supply voltage and maximum current of the amplifier, respectively. All the higher order harmonics are assumed to be short circuited in a class-B PA. Extending the design space of class-B amplifiers was first introduced in [1] through the invention of the class-BJ amplifier. Figure 2.1 shows the location of fundamental and harmonic impedances for class-B and class-BJ PAs. Following with a similar approach, continuous class-F (CCF) mode PAs were architected to extend the conventional class-F design space [2]. The CCF theory introduces the idea that a short second harmonic and an open third harmonic condition for a conventional class-F PA is not a unique solution. Rather, an extended design space exists where the same high performance (efficiency and power) of a conventional class-F PA is achieved. Conventional class-F operation is narrowband due to the requirement of short and open impedance terminations at second and third harmonics, whereas an extended design space of CCF PAs facilitates wideband operation. In [3], a wideband PA with 74% efficiency was reported to prove the theory introduced in [2].

The original theory of class-BJ PAs does not take into account the non-linearity introduced by device drain-source capacitance, C_{ds} [1]. Recently published work shows that in the presence of non-linear C_{ds}, the design space of a class-BJ PA deviates from

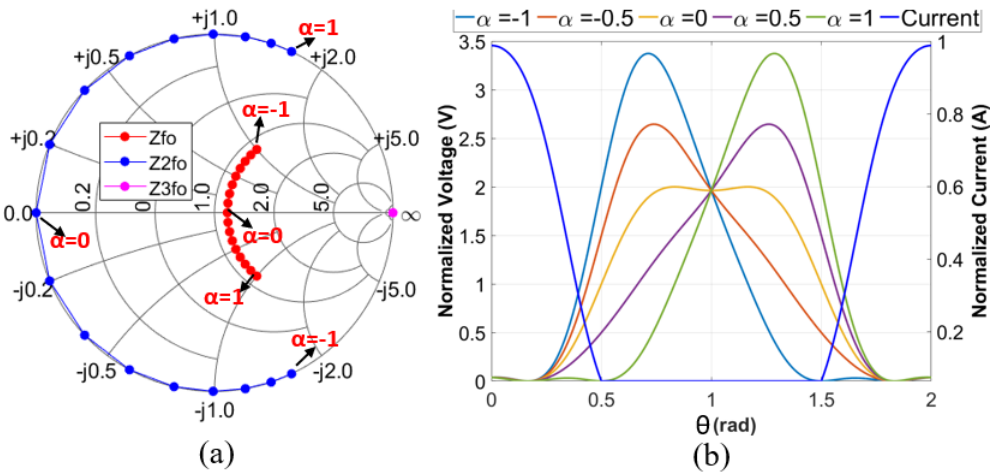

Figure 2.2: (a) Impedance locations for ideal CCF mode, and (b) CCF voltage and current waveforms

original theory, and the power and efficiency predicted by the class-BJ theory does not apply over the entire design space [4]. in this work, CCF PAs are mathematically analyzed for the first time to demonstrate the effects of non-linear C_{ds}. The analysis provides design insight and constraints to achieve optimized CCF PA performance in the presence of non-linear C_{ds}.

2.2 Theory of CCF PAs

CCF mode is an extended design space of class-F PAs first introduced in [2]. The theory suggests a single-solution open circuit third harmonic condition, whereas the second harmonic short circuit condition is but one and not the only solution to CCF operation. The voltage waveform for CCF mode can be expressed as [1]:

$$v_{ds}(\alpha) = V_{dd}(1 - \frac{2}{\sqrt{3}}\cos(\theta) + \frac{1}{3\sqrt{3}}\cos(3\theta))(1 - \alpha\sin\theta) \tag{2.2}$$

where $\theta = 2\pi f_0 t$, f_0 is the fundamental frequency, and α is the continuous mode parameter, $-1 \leq \alpha \leq 1$. If the current waveform is considered half rectified, which is the usual assumption for a tuned class-B bias condition, then the current can be

expressed as:

$$i_{ds} = I_{max}(\frac{1}{\pi} + \frac{1}{2}\cos(\theta) + \frac{2}{3\pi}\cos(2\theta)) \tag{2.3}$$

For each α value, from (2.3) and (2.3), there can be found a pair of fundamental (f_0) and second harmonic ($2f_0$) voltage components that constitute a mode for CCF operation. The third harmonic component ($3f_0$) always remains an open circuit. For narrowband applications, a designer has the freedom to choose any α value. For wideband applications, a range of α values can be chosen so that the f_0 and $2f_0$ impedances synthesized by the matching network over the target frequency band follow the impedance trajectories dictated by α. The impedance locations and the voltage and current waveforms for CCF mode are plotted in Figure 2.2.

2.3 Effect of Non-linear C_{ds} on CCF Mode PAs

The ideal CCF mode that was described in Section II is based on the assumption that C_{ds} is linear in nature, e.g., C_{ds} stays constant with drain voltage variation. However, in real devices, C_{ds} does not stay constant, but rather exhibits non-linearity with strong dependence on drain voltage. For some devices, the non-linearity is relatively weak and can be approximated with linear capacitors. But in most power devices of interest (LDMOS and GaN), the capacitive non-linearity is too strong to be ignored. In this section, a mathematical analysis is presented that illustrates the effect of non-linear C_{ds} on fundamental and second harmonic impedance trajectories for CCF operation. The analysis also shows the impact on key RF PA metrics. NXP's 50V LDMOS device is used for demonstration. In general, a non-linear C_{ds} behavior can be represented by the following expression [4]:

$$C_{ds}(v_{ds}) = C_{off} + \frac{C_0}{(1 + \frac{v_{ds}}{v_0})^m} \tag{2.4}$$

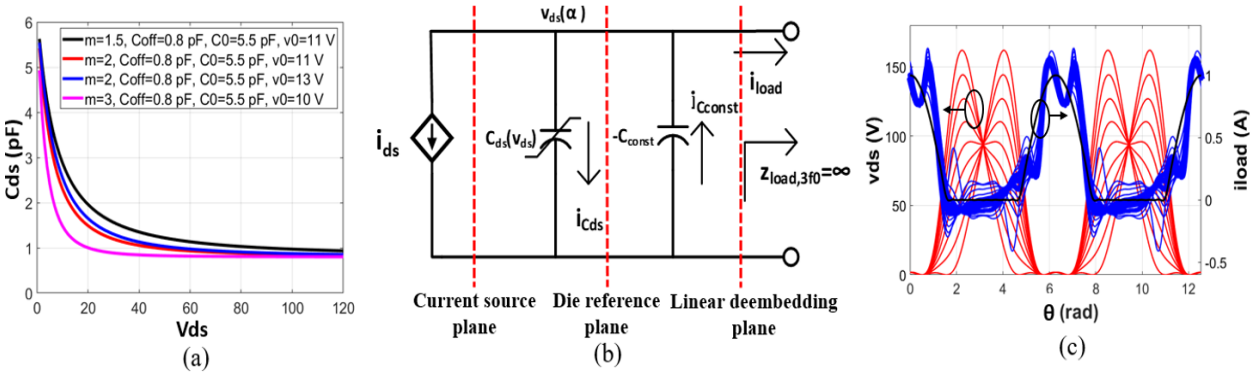

Figure 2.3: (a) Capacitance versus drain voltage for non-linear C_{ds} with various fitting parameters, (b) simplified equivalent circuit model of the PA device under operation, (c) calculated time domain voltage and current waveforms for $-1 \leq \alpha \leq 1$ at the LDP for CCF mode

where C_{off}, C_0, v_0, and m are general fitting parameters, which are extracted for a given technology. As an example, Figure 2.3(a) illustrates non-linear C_{ds} behavior for different values of fitting parameters. C_0 and C_{off} define the capacitance at low voltage and high voltage regions, respectively. Parameters v_0 and m control the slope of the capacitance curve from high to low values of V_{ds}. In this analysis, the parameter values are chosen as C_{off}=0.8 pF, C_0=5.5 pF, v_0=11 V and m=2, which are representative of the selected NXP device. The RF PA is assumed to operate with V_{dd} = 48 V, I_{max} = 1 A, and f_0 = 1 GHz. To analyze the impact of the non-linear C_{ds} on CCF operation, a simplified equivalent circuit model is presented that includes lossless non-linear C_{ds} in parallel with a current source, i_{ds} (Figure 2.3(b)). A linear de-embedding methodology is employed by placing a negative linear capacitor, C_{const}, in parallel with the non-linear C_{ds} [4]. In this example, C_{const} is 1.19 pF. The currents i_{cds} and i_{const} are not equal, as the negative capacitance does not fully cancel out non-linear C_{ds} and some residual current flows in the circuit. Applying KCL to the equivalent circuit model in Figure 2.3(b), the load current, i_{load}, can be expressed as in (2.5).

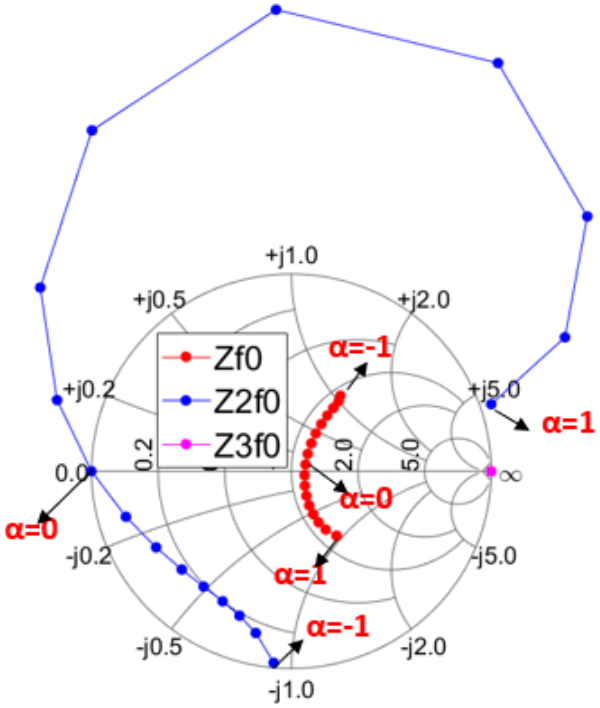

Figure 2.4: f_0, $2f_0$, and $3f_0$ impedance trajectories at the LDP

As illustrated in Figure Figure 2.3(b), an open circuit third harmonic load impedance condition is imposed at the linear de-embedding plane (LDP) per CCF theory, thus forcing the load current component, $i_{load,3f0}$, to be zero. The open circuit third harmonic is assumed to be realized by output matching circuitry. Substituting (2.4) into (2.5) for C_{ds}, the time domain load current is obtained as a function of α. The calculated time-domain load current and voltage are plotted in Figure Figure 2.3(c). Out of phase fundamental and second harmonic reactive currents are generated because of the varactor effect from non-linear C_{ds}. These out of phase components distort the ideal current waveform (see Figure 2.3(c)). By performing a Fast Fourier Transform (FFT) on the time-domain voltage and current waveforms, the fundamental and harmonic load impedances are calculated at the LDP, and Figure 2.4 portrays the newly calculated impedance trajectories. In $-1 \leq \alpha \leq 0$ range, the

$2f_0$ impedances remain inside the smith chart ($\Gamma_{2f0} < 1$). Hence, power needs to be dissipated at $2f_0$ frequency to satisfy those impedance conditions. On the other hand, for $0 < \alpha \leq 1$, the trend is opposite and $2f_0$ impedances are such that $\Gamma_{2f0} > 1$, meaning that power must be injected from an external $2f_0$ source. These overall trends for $2f_0$ impedances have similarities to that reported for a class-BJ with non-linear C_{ds} [4]. However, an important difference in the class-BJ amplifier is that $2f_0$ impedances are not impacted by non-linear C_{ds} at $\alpha = -1$ and $\alpha = 1$. In CCF mode, the $\alpha = -1$ and $\alpha = 1$ impedances are impacted, as the $2f_0$ impedances at those points remain inside and stay outside the smith chart, respectively.

The power at f_0 and $2f_0$ (P_{f0} and P_{2f0}) and the efficiency are calculated from (2.6)-(2.8) based on the fourier components of the voltage and current waveforms. In Figure 2.5(a), P_{f0} and P_{2f0} are plotted as α is varied from -1 to 1. Conventional CCF theory (linear C_{ds}) suggests that P_{f0} should remain constant and P_{2f0} should be zero for all values of α. However, the effect of non-linear C_{ds} for $-1 \leq \alpha \leq 0$ range illustrates that P_{f0} has a lower value and P_{2f0} is greater than zero. This indicates energy upconversion, as energy gets transferred from the fundamental to the second harmonic due to the non-linear capacitance. Conversely, for $0 < \alpha \leq 1$, P_{2f0} is less than zero and P_{f0} is higher than the linear C_{ds} approximation, indicating downconversion from the second harmonic to fundamental frequency. The efficiency in Figure 2.5(b) follows the same trend as P_{f0}.

$$i_{load}(\alpha) = -i_{ds} - \frac{dv_{ds}(\alpha)}{dt}(C_{ds}(v_{ds}) - C_{const}) \tag{2.5}$$

$$P_{f0} = 0.5 * Re(v_{ds,f0} * conj(i_{load,f0})) \tag{2.6}$$

$$P_{2f0} = 0.5 * Re(v_{ds,2f0} * conj(i_{load,2f0})) \tag{2.7}$$

$$Efficiency = \frac{P_{f0}}{P_{dc}} * 100\% = \frac{P_{f0}}{v_{ds,dc} i_{load,dc}} * 100\% \tag{2.8}$$

The calculated power and efficiency in Figure 2.5 provide critical insight for CCF

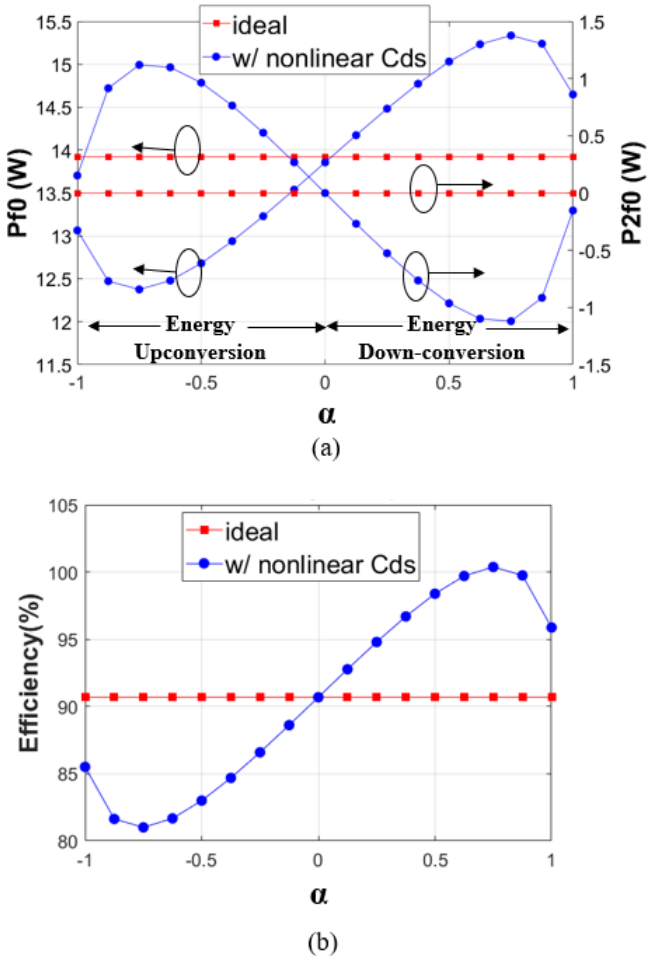

Figure 2.5: (a) Calculated f_0 and $2f_0$ power, (b) calculated efficiency

PA design. For example, to obtain higher power and efficiency, a design space of $0 < \alpha \leq 1$ leads to improvements in both power and efficiency, where the theoretical efficiency reaches as high as 100% at $\alpha = 0.75$. However, external $2f_0$ power injection is required in this range, which adds complexity and assumed dc power consumption. Another solution of interest requires that $2f_0$ impedances remain at $\Gamma_{2f0} = 1$ for values of $-1 \leq \alpha \leq 1$, thus corresponding to passive second harmonic terminations. To impose this condition at $2f_0$, a phase shift parameter ϕ needs to be introduced in the voltage expression [4]. With proper choice of ϕ, new $2f_0$ reactive voltage components are generated that counteract the effect of the $2f_0$ reactive currents generated by

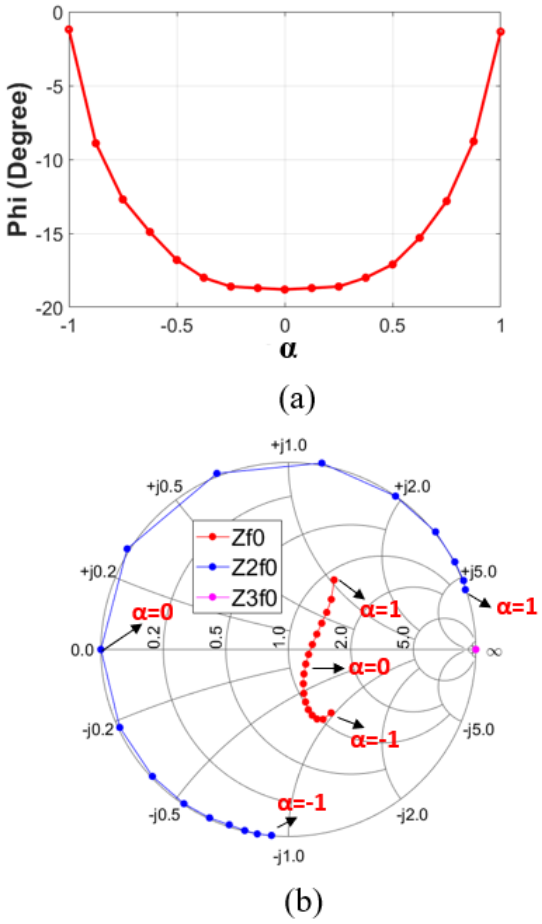

Figure 2.6: (a) Phase shift ϕ vs alpha, (b) Impedance trajectories after ϕ is applied

non-linear C_{ds}. By inserting phase shift parameter ϕ in the voltage expression, the new drain-source voltage expression become,

$$v_{ds}(\alpha) = V_{dd}(1 - \frac{2}{\sqrt{3}}\cos(\theta+\phi) + \frac{1}{3\sqrt{3}}\cos(3\theta+3\phi)).(1-\alpha\sin(\theta+\phi)) \qquad (2.9)$$

While it's a cumbersome process to identify values of ϕ that satisfies $\Gamma_{2f0} = 1$ from closed form expressions, correct ϕ values can be solved easily using an iterative method. Making an initial assumption that ϕ should always be within $\pm\pi/2$, ϕ is swept from $-\pi/2$ to $\pi/2$ as α is varied. For each value of α, the real part of Z_{2f0} is calculated using (2.4), (2.5), and (2.9) using FFT. The correct ϕ value is identified that forces $Re(Z_{2f0})$ to zero. Results for the numerical evaluation with

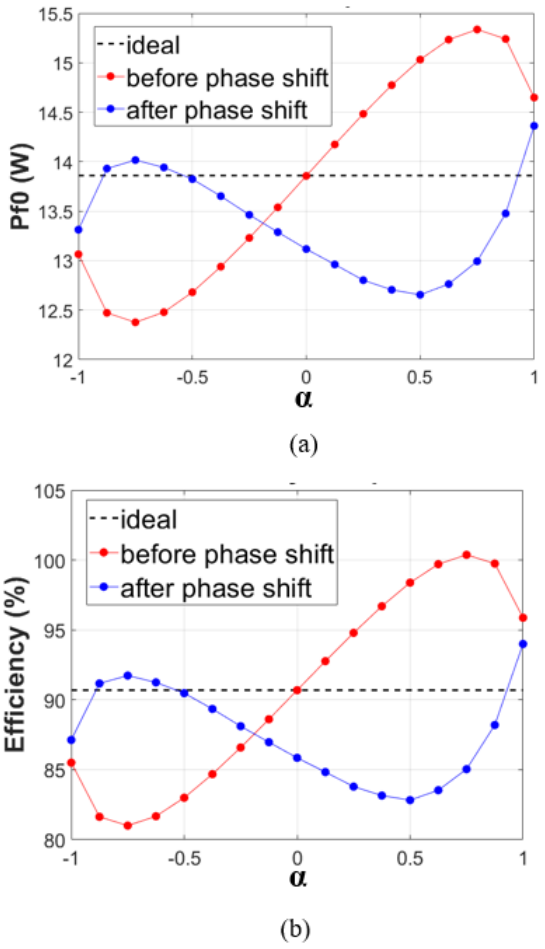

Figure 2.7: (a) Power before and after phase shift, and (b) efficiency before and after phase shift

$-1 \leq \alpha \leq 1$ calculated in 0.125 steps are given in Figure 2.6(a). Figure 2.6(b) shows the trajectory of the load impedances after the ϕ values are applied, where $2f_0$ load trajectories now stay at the edge of the smith chart for the full α range. This indicates that only passive termination can realize this solution without the need for $2f_0$ power dissipation or injection. However, the $2f_0$ load trajectory has a clockwise rotation from its original location in Figure 2.2(a) when assuming linear C_{ds}. Similarly, the f_0 load trajectory of Figure 2.6(b) diverges from its original trajectory in Figure 2.2(a). The power and efficiency after introducing phase shift are calculated from (2.6)-(2.8), once ϕ is determined and plotted in Figure 2.6(a). There is a reversal in power and

efficiency trends from the previous solution with no phase shift (see Figure 2.7). In the $-0.875 \leq \alpha \leq -0.625$ range, power and efficiency go above their nominal (ideal) values, thus suggesting a targeted operation design space. These higher power and efficiencies are not achievable in this range without applying ϕ.

2.4 Summary

The mathematical analysis presented in this work concludes that the constant power and efficiency predicted by CCF PA theory does not stay constant in the presence of a non-linear C_{ds}. From analysis, two possible CCF PA solutions are presented to optimize performance. The first solution requires external second harmonic power to be injected at the output in $0 < \alpha \leq 1$ range for high performance. The second solution with passive second harmonic termination may achieve higher than nominal (linear C_{ds}) performance by targeting the $-0.875 \leq \alpha \leq -0.625$ range. The presented methodology can be used for any device technology that possesses non-linear C_{ds}, and provides design guidance for choosing the optimal f_0 and $2f_0$ impedances in CCF PAs with the presence of non-linear C_{ds}.

Chapter 3

A HIGH PERFORMANCE CLASS-J DOHERTY POWER AMPLIFIER

3.1 Introduction

The Doherty Power Amplifier (DPA) has become widely adopted for cellular infrastructure transmitters, as it is well suited to achieve high efficiencies when amplifying multi-carrier signals with large peak to average power ratios (PAPR). DPAs have a typical operating condition at 8 dB OBO, and it is critical to maximize efficiency and linearity at this back-off level. Furthermore, the DPA must be amenable to DPD linearization, which entails careful attention to numerous design details, such as minimizing amplitude (AM-AM) and amplitude to phase (AM-PM) excursions to acceptable levels, and implementing low impedance baseband terminations, especially at the device's drain terminal. Due to the use of many transmitter pipes in a mMIMO system, package size and space are quite limited and it becomes necessary to realize the DPA in a small and cost effective form factor. This is particularly difficult in a DPA given that the architecture uses both carrier and peaking sub-amplifiers and requires matching circuity associated with each. This work utilizes integrated passive device (IPD) technology, whereby input and output pre-matching circuitry as well as harmonic termination networks are realized as lumped elements (e.g. spiral inductors, MIM caps) on a low-cost silicon (Si) integrated circuit (IC) technology. The DPA device is then realized in a small form factor QFN package consisting of wire bond interconnects between several Si ICs, GaN devices, and package leads.

A Class-J amplifier topology [8], [25] is chosen for the Doherty's carrier sub-amplifier because of its simple required drain harmonic termination and high efficiency

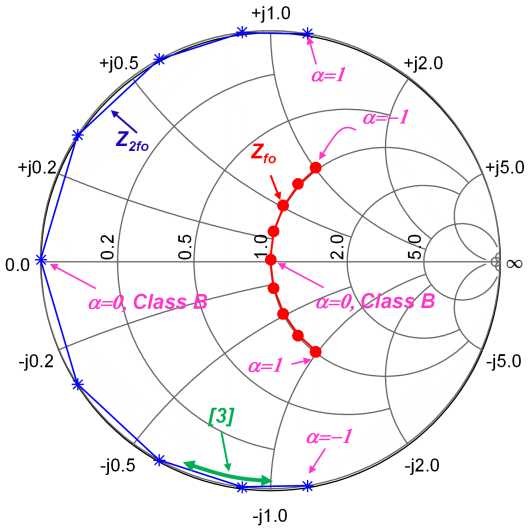

Figure 3.1: Class-B/J fundamental (red) and second harmonic (blue) load impedance at intrinsic device plane (linear C_{ds}), and (green) enhanced efficiency region of α reported in [4] for non-linear C_{ds}

under back-off conditions. Based on a more recent published work [4], the effects of transistor's non-linear output capacitance, C_{ds} on continuous class-J operation was taken into account to further improve the performance.

3.2 Class-BJ/ Continuous Class-J Amplification

The class-J power amplifier assumes a half-rectified current waveform combined with output loading/ terminations at fundamental and second harmonic frequencies to provide a phase shift of 45^o and 90^o in the drain-source voltage at these frequencies, respectively. Further work expanded the design space showing a continuum of solutions based on a half-rectified current waveform, and allowing for a more generalized drain-source voltage (3.1), where parameter α can be varied over the range of -1 to +1. Each solution results in a pair of fundamental and second harmonic terminations as illustrated in Figure 3.1, all providing the same power and efficiency as tuned Class-B operation. This design method adds a level of simplicity in PA design and

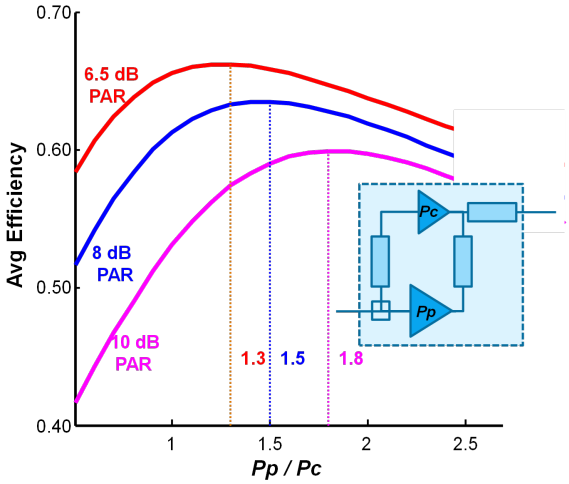

Figure 3.2: Average 2-way Doherty efficiency for 6.5, 8, and 10 dB PAPR signals as a function of peaking to carrier power (ideal Doherty operation)

circuit realization, as it gives more freedom in choosing circuit topologies that exhibit the correct loading at fundamental and second harmonic frequencies.

$$v_{ds}(\alpha) = V_{dd}(1 - \cos(\theta))(1 - \alpha \sin\theta) \tag{3.1}$$

More recently, effects of transistor non-linear output capacitance C_{ds} on continuous Class-J amplifier performance were analyzed for a Si based LDMOS transistor [4]. It was shown that C_{ds} non-linearity causes the magnitude of the second harmonic reflection coefficient at the device intrinsic drain terminal (Γ_{2fo}) to be less than 1 for certain values of α and greater than 1 for other values, leading to either enhanced or degraded power & efficiency performance as a function of α. As GaN devices exhibit similar non-linear C_{ds} characteristics, an analysis for GaN devices under Class-J operation also indicates a power and efficiency dependence with α.

3.3 Doherty Amplifier Design

In this work, we choose a two-way asymmetric DPA architecture so as to maximize efficiency performance at 8 dB OBO when driven by multi-carrier LTE signals.

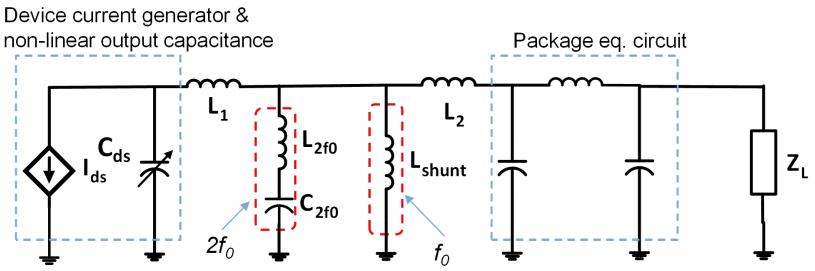

Figure 3.3: Simplified schematic of output matching circuit for Carrier sub-amplifier)

To better understand the trade-offs in choosing DPA asymmetry factor, (i.e., peaking to carrier power ratio, P_p/P_c) detailed simulations were performed for amplitude modulated signals to determine average efficiency under the assumption of ideal Doherty characteristics for various values of P_p/P_c. The results are shown in Figure 3.2 for signal PAPR values of 6.5 dB, 8.0 dB, and 10 dB. At 8 dB OBO, corresponding to 8 dB PAPR, the suggested ratio of $P_p/P_c \sim 1.5$ is optimal, and a somewhat larger asymmetric ratio is recommended as signal PAPR increases (or equivalently at higher OBO). Therefore, the presented design uses an asymmetry ratio of 1.8, leading to GaN device sizes of about 1.5 mm and 2.7 mm gate width periphery for carrier and peaking devices, respectively.

To further enhance efficiency performance at back-off, the Carrier sub-amplifier is designed for continuous mode Class-J operation, and the effects of non-linear output capacitance C_{ds} are considered in the design phase, as discussed in Section II. This leads to a circuit solution as illustrated in Figure 3.3, which implements near optimal values for the paired fundamental and second harmonic terminations. The use of a series resonant circuit formed by L_{2f0} and C_{2f0} creates a low impedance at the second harmonic frequency, while L_1 and C_{ds} provide flexibility to position the angle of Γ_{2f0} as required while maintaining the magnitude of Γ_{2f0} close to 1.0. Furthermore, inductor L_{shunt} provides an additional degree of freedom in setting the value of

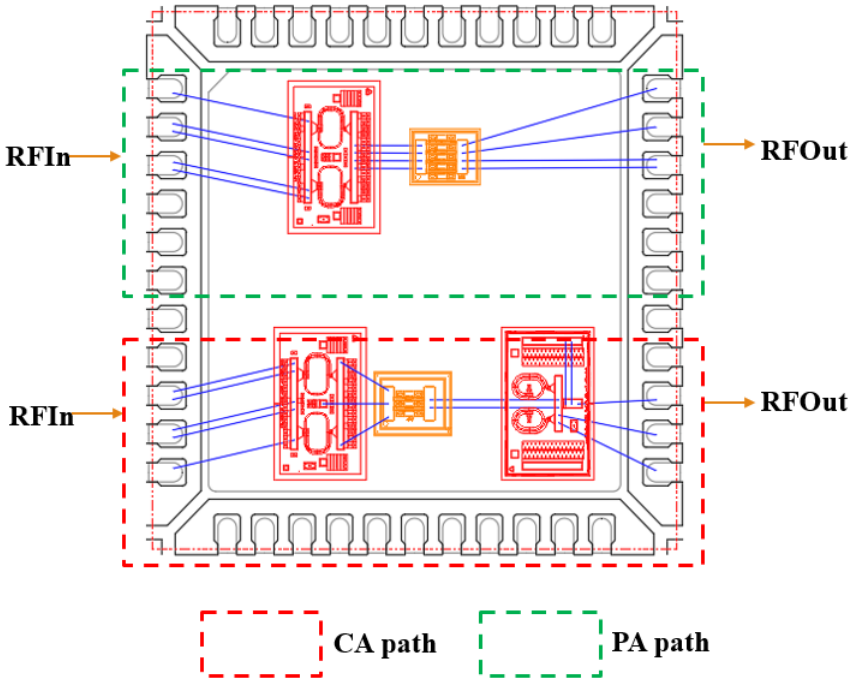

Figure 3.4: Illustration of DPA elements in a QFN package

Γ_{f0} (fundamental frequency) independent of Γ_{2f0}. For the Peaking sub-amplifier, a simple tuned Class-B output configuration is chosen, since the Peaking sub-amplifier contribution to efficiency at back-off is small in Doherty operation.

An illustration of the DPA elements within the QFN package is given in Figure 3.4. Si-based IPDs are utilized to implement RF impedance pre-matching circuits at the inputs to both Carrier and Peaking GaN devices. The pre-matching circuits make input impedances at the package reference plane amicable for realizing the input matching networks (IMNs) in the printed circuit board (PCB). Use is made of the IPD process to implement both capacitors and inductors on Si die blocks, and use of thick metallization is helpful in reducing insertion losses, especially those associated with spiral inductors. Wirebond interconnections are used between various die blocks and package pins. Similarly, the Class-J output network is realized as a combination of bond-wires and L/C components printed on a separate IPD structure. All of the

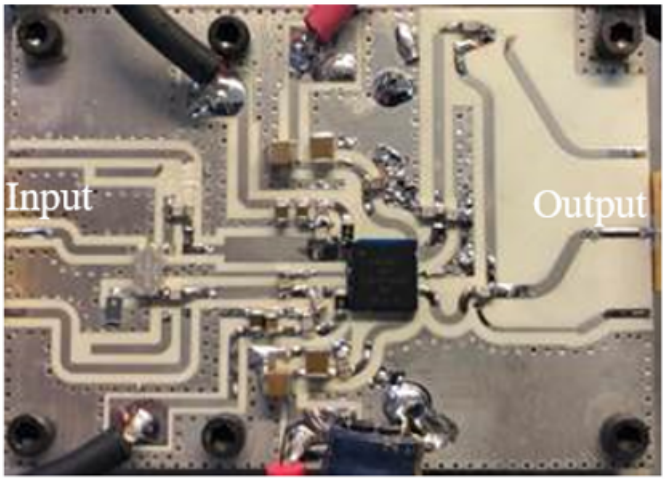

Figure 3.5: Full Doherty amplifier including QFN package, and external input coupler and output combiner

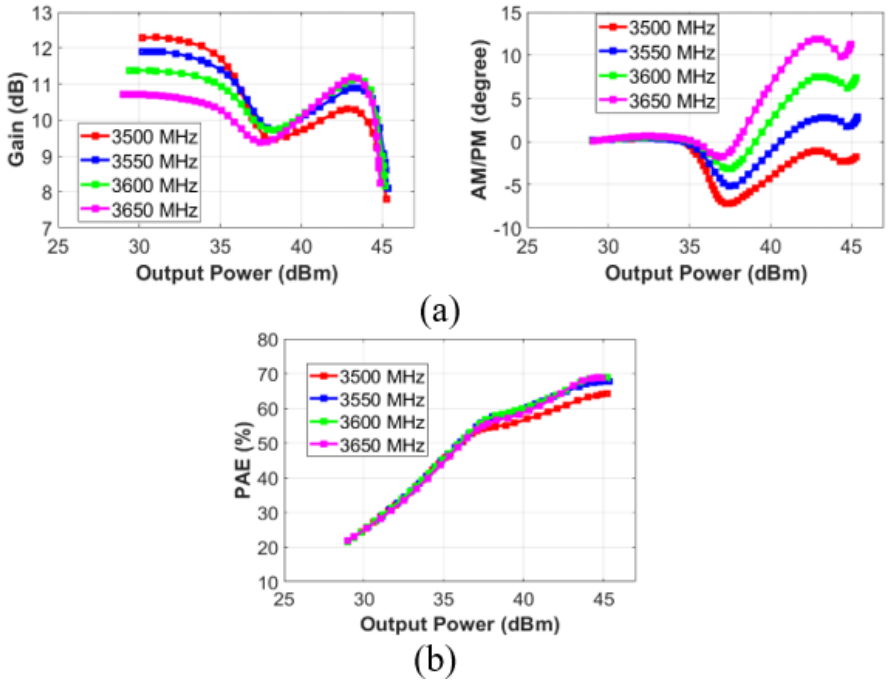

Figure 3.6: Measured DPA performance under CW drive-up stimulus, (a) gain and am/pm response, and (b) PAE

circuitry easily fits within the 7mm x 7mm QFN package.

3.4 Measured DPA Performance

The DPA was implemented in a Rogers R04350 PCB (ϵ_r=3.66) substrate with 20 mils thickness, as illustrated in Figure 3.5. The drain (supply) voltage of both carrier and peaking devices were set at 48 V. The carrier amplifier was biased at class-AB with quiescent drain current of 16 mA. The peaking amplifier was biased at class-C with gate voltage of -5.5 V. An uneven-split hybrid coupler from Anaren was used as the input coupler. The DPA was initially characterized with a CW stimulus to obtain AM-AM and AM-PM behavior. The test set up ramped the power level quickly to minimize device heating/thermal affects from significantly influencing the measurement. Drive up data is illustrated in Figure 3.6. Small signal gain is in the range of 11 to 12 dB, and saturated power of approximately +45 dBm. It can be observed that the Peaking amplifier transitions to from an off- to on-state around +37 dBm output power, resulting in some compression of the carrier amplifier and roughly a 1 dB dip in the AM-AM response. The deviation in AM-PM is kept within about 10 degrees, and PAE about 54% is recorded at +37 dBm output power.

Table 3.1

DPA Performance Under Multi-Carrier LTE Stimulus

P_{out} (dBm)	LTE Signal BW (MHz)	PAR (dB)	Efficiency (%)	ACLR-Adj(dBc)		ACLR-Alt(dBc)	
				After DPD		After DPD	
				L	U	L	U
37.04	1x20	7.0	48.79	-54.07	-53.55	-56.76	-55.84
37.04	2x20	7.0	48.79	-55.32	-55.11	-55.50	-55.76
37.01	3x20	7.5	48.68	-53.20	-52.23	-53.46	-53.05
37.04	5x20	7.5	48.79	-50.43	-50.67	-50.73	-50.72

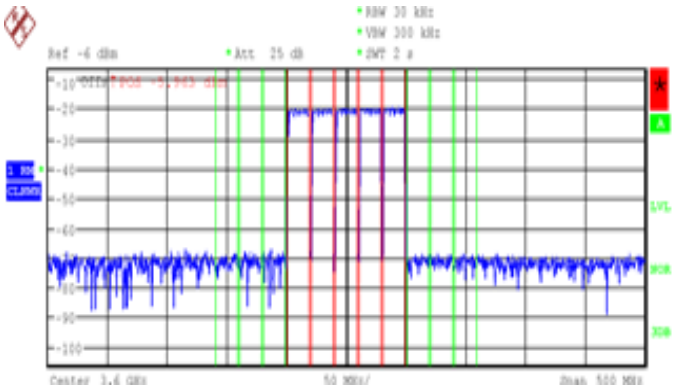

Figure 3.7: Doherty output spectral response under a 5 carrier LTE signal at 20 MHz / carrier, after DPD correction

The DPA performance when driven by multi-carrier LTE signals is tabulated in Table 3.1 for several signal bandwidths and PAPR. Excellent DPD correction is obtained for multi-carrier bandwidth signals of 100 MHz. The excellent DPD linearizability can be attributed in large part to minimizing AM-AM and AM-PM fluctuations over power drive up. Spectral performance at the PA output for a 100 MHz bandwidth LTE signal after DPD correction is shown in Figure 3.7. Excellent DPD amplifier corrected performance is shown across 500 MHz of bandwidth. Table 3.2 summarizes the performance of the proposed DPA with other state-of-the art 3.5 GHz GaN DPA designs. While maintaining a compact form factor, this work demonstrates comparable performance with excellent DPD corrected linearity compared with other DPAs. The presented solution is the only GaN DPA solution that offers the integration of harmonic trapping using a Si-based IPD with carrier and peaking amplifiers housed in a single package, thus enabling a compact solution.

Table 3.2

Comparison with Other 3.5 GHz DPAs

Ref.	Freq. (GHz)	PAE @ 8dB OBO (%)	PAE @ Sat (%)	Tech.	P_{sat}	Inst. Band-width(MHz)	ACLR after DPD (dBc)
[26]	3.5	59*	69	GaN	42.9	20	-43
[48]	3.5	55	65	GaN	45	20	-52
[27]	3.5	47	44	GaN	45	N/A	N/A
This Work	3.5-3.65	54-55	64-70	GaN	45	20	-53.55

*Estimated from CW plots

3.5 Summary

This work describes an approach used to implement a highly efficient GaN-based Class-J Doherty power amplifier in a small footprint. Active GaN devices with their input pre-matching and class-J output circuitry are placed in a 7 mm x 7 mm quad-flat no-leads (QFN) plastic encapsulated package. Under CW excitation, the DPA delivers +45 dBm peak power from 3.5 GHz to 3.65 GHz. At 8 dB OBO, the efficiency reaches 54%, and 70% at peak power. The DPA demonstrates excellent DPD linearized performance of better than 50 dB ACLR with multi-carrier LTE signaling.

Chapter 4

2.6-GHZ INTEGRATED LDMOS DOHERTY POWER AMPLIFIER FOR 5G BASESTATION APPLICATIONS

4.1 Introduction

As it was previously discussed in Chapters 1 and 3, DPAs are the most widely used PA architecture in basestation applications because of their simple configuration and high output power back-off (OBO) efficiency [5]-[10]. Traditionally, DPAs have been implemented in discrete fashion with packaged power transistors and distributed matching structures for base stations applications. With the roll-out of 5G, the DPA footprint is becoming more restricted, thus requiring higher levels of DPA integration and miniaturization. Many recently published works have explored fully integrated or partially integrated DPA architectures [11]-[22]. Among them are some promising solutions, such as the integrated Doherty [11]-[14], Doherty PA module [15],[16], and Doherty MMIC [17]-[22].

Traditionally, the DPA output combiner includes quarter-wave transmission-lines (TLs) for proper load modulation. To reduce the size of the output combining network (OCN), these TLs are in-part or entirely replaced by lumped components for miniaturization of Doherty footprints in designs below 6 GHz. *C*-*L*-*C* based "C_{ds}-absorption" is one simple and effective method to replace a quarter wave impedance inverter with lumped components for integrated Doherty architectures[11]-[13]. However, to-date, this combining topology has only been implemented in symmetric Doherty [12] and multi-way Doherty [11], [13] PA designs. This combining has not been well-adopted in the two-way asymmetric Doherty architecture because of the asymmetry presented

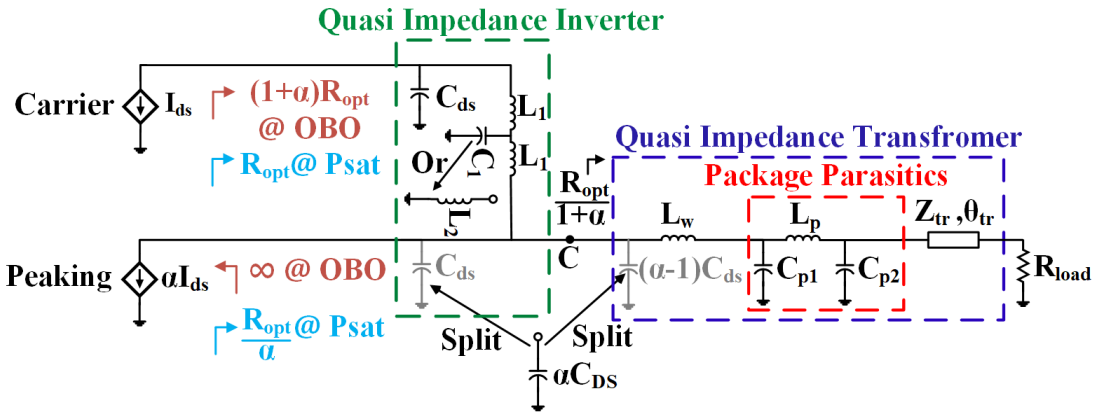

Figure 4.1: Proposed integrated Doherty output combining network (OCN)

by the carrier and the peaking amplifiers' C_{ds}. Additionally, prior analyses have not provided a generalized case for any two-way DPA architecture and they have not accounted for the effects of bondwire and package parasitic components. In this work, we present for the first time a generalized "C_{ds}-absorption" based Doherty OCN that is applicable for two-way symmetric/asymmetric DPA architectures and considers the effects of bondwire and package parasitic components. The proposed network presents a novel method of absorbing part of the peaking amplifier's C_{ds} into the impedance transformer network for an asymmetric Doherty, and the OCN offers enhanced flexibility for impedance inverter design. Based on the presented combiner, an asymmetric two-way, two-stage integrated Doherty was designed and fabricated at 2.6 GHz using NXP's AF3 LDMOS process [23]. The experimental results of the fabricated DPA and its performance comparison with other state-of-the-art works are presented in this letter.

4.2 Theory of Operation

An integrated Doherty with carrier to peaking power ratio of 1:α is selected for the proposed OCN, as shown in Figure 4.1 (α=1 for the symmetric case).

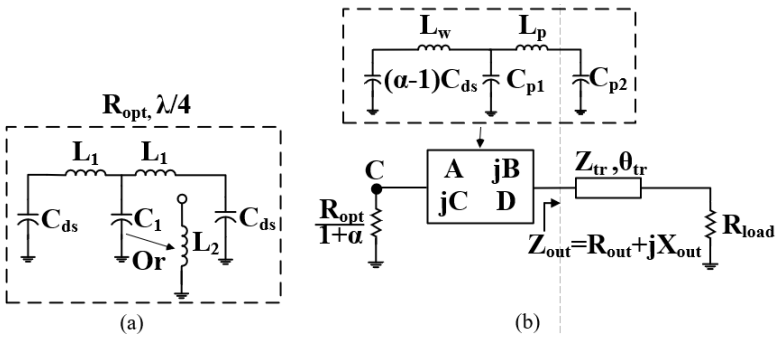

Figure 4.2: (a) Quasi impedance inverter, and (b) Parasitic components of the quasi impedance transformer replaced by ABCD network

Following the parallel equivalence of capacitors from circuit theory, the peaking amplifier's drain-source capacitance, αC_{ds}, is assumed to be split into C_{ds} and $(\alpha - 1)C_{ds}$ across the combining node (C in Figure 4.1). A π-network is formed by C_{ds}(carrier)-L_1-(C_1 or L_2)-L_1-C_{ds} (split from the peaking PA's αC_{ds}), and this network comprises the quasi impedance inverter. Bondwire (L_w) is required to connect the combining node to the package lead. The quasi impedance transformer is composed of $(\alpha - 1)C_{ds}$, bondwire (L_w), package parasitics (C_{p1}-L_p-C_{p2}), and a printed circuit board (PCB) microstrip TL (Z_{tr}, θ_{tr}). For a symmetric DPA (α=1), $(\alpha-1)C_{ds}$ does not exist and the peaking PA's C_{ds} is entirely absorbed by the quasi-inverter.

Load modulation is the key for Doherty operation, as the OCN presents different impedances to the output of the carrier and peaking PAs at OBO and saturated power conditions, as shown in Figure 4.1. For successful load modulation, the quasi-inverter should have a characteristic impedance of R_{opt} (class-B optimal load resistance) and an electrical length of $\lambda/4$, as illustrated in Figure 4.2(a). These two conditions can be satisfied simultaneously when L_1, C_1, and L_2 are calculated from the following:

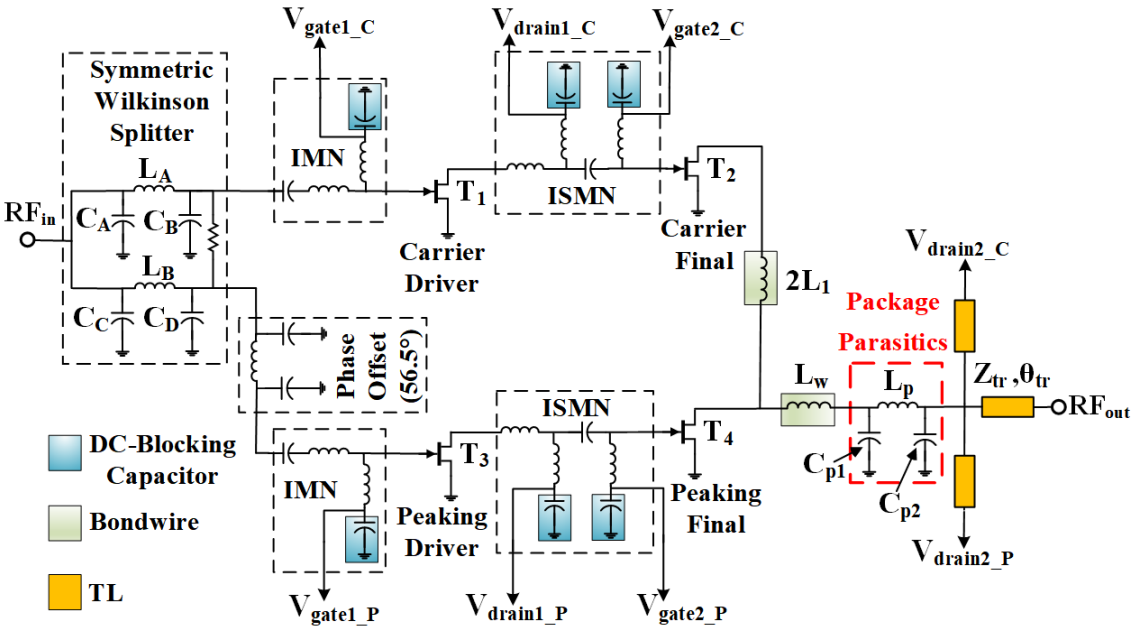

Figure 4.3: Schematic of proposed two-stage integrated Doherty

$$L_1 = \frac{R_{opt}}{\omega(1+Q_{dev})}, \tag{4.1}$$

$$C_1 = \frac{1-Q_{dev}^2}{\omega R_{opt}}, \qquad \text{if } Q_{dev} \leq 1 \tag{4.2}$$

$$L_2 = \frac{R_{opt}}{\omega(Q_{dev}^2-1)}, \qquad \text{if } Q_{dev} \geq 1 \tag{4.3}$$

Where $\omega = 2\pi f_0$ is the angular frequency, and $Q_{dev} = \omega R_{opt} C_{ds}$ is the intrinsic device quality factor. R_{opt} and C_{ds} can be extracted from class-B load-line analysis and C-V characteristics to determine Q_{dev}. If Q_{dev} approaches unity, then both C_1 and L_2 present open-circuit conditions following (4.2) and (4.3), and the quasi-inverter reduces to C_{ds}-$2L_1$-C_{ds}, which is the same solution as the well-known C-L-C inverter. If Q_{dev} is less than or greater than unity, a shunt capacitor, C_1, or a shunt inductor, L_2, is required for an optimum quasi-inverter design. Hence, the proposed quasi-inverter offers additional solutions and more design flexibility when Q_{dev} is not unity.

A quarter-wave TL of characteristic impedance $((R_{load}R_{opt})/(1+\alpha))^{1/2}$ can ideally establish a single-section match between the load impedance, R_{load}, and the combining

Table 4.1

ABCD Parameters for Figure 4.2(b)

$\boldsymbol{A}$	$1-\omega^2(C_{p2}L_p - L_w(C_{p2}+C_{p1}\delta_2))$
$\boldsymbol{B}$	$\omega(L_p + L_w\delta_1)$
$\boldsymbol{C}$	$(\alpha-1)\omega C_{ds}\delta_2 + (C_{p2}+C_{p1}\delta_2)\omega\delta_3$
$\boldsymbol{D}$	$(1-\alpha)\omega^2 C_{ds}L_p + \delta_1\delta_3$

$\delta_1 : 1-\omega^2 C_{p1}L_p$, $\delta_2 : 1-\omega^2 C_{p2}L_p$, $\delta_3 : 1-(\alpha-1)\omega^2 C_{ds}L_w$

node impedance, $R_{opt}/(1+\alpha)$. However, the parasitic network formed by $(\alpha-1)C_{ds}$, bondwire L_w, and package parasitics (C_{p1}-L_p-C_{p2}) alters the characteristic impedance and the electrical length of the required TL. Therefore, the TL is presented by an arbitrary characteristic impedance and electrical length of Z_{tr}, θ_{tr}. As a first step to finding Z_{tr} and θ_{tr}, the π network formed by $(\alpha-1)C_{ds}$, L_w, and (C_{p1}-L_p-C_{p2}) is replaced by a corresponding 2-port ABCD network in the quasi transformer, as shown in Figure 4.2(b). The ABCD parameter values can be calculated from the derived expressions listed in Table 4.1.

The output impedance of the ABCD network is assumed to be Z_{out}. Next, the real and imaginary parts of Z_{out} (R_{out} and X_{out}) are calculated based on the ABCD parameters as:

$$R_{out} = \frac{R_{opt}(1+\alpha)(\boldsymbol{AD}+\boldsymbol{BC})}{\boldsymbol{A}^2(1+\alpha)^2 + \boldsymbol{C}^2 R_{opt}^2}, \tag{4.4}$$

$$X_{out} = \frac{\boldsymbol{D}R_{opt} - \boldsymbol{A}(1+\alpha)R_{out}}{R_{opt}\boldsymbol{C}}, \tag{4.5}$$

Once R_{out} and X_{out} are known, the required characteristic impedance, Z_{tr}, and electrical length, θ_{tr}, are finally calculated from the following derived expressions:

$$Z_{tr} = \sqrt{\frac{R_{load}(R_{out}^2 + X_{out}^2 - R_{load}R_{out})}{\Delta_r}}, \tag{4.6}$$

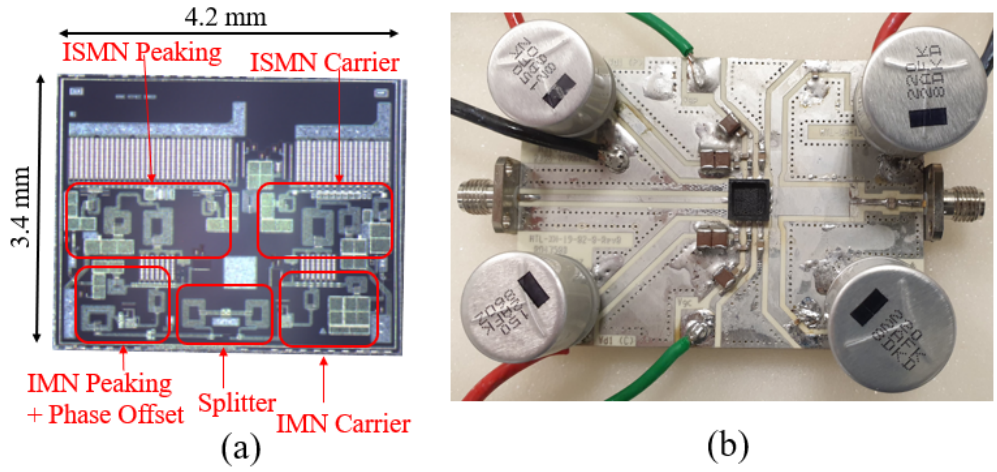

Figure 4.4: (a) Chip micrograph of the Doherty RFIC, and (b) Evaluation board

$$\theta_{tr} = \begin{cases} -\tan^{-1}\dfrac{\sqrt{\Delta_r R_{load}(R_{out}\Delta_r + X_{out}^2)}}{X_{out}R_{load}}, & \text{if } X_{out} \leq 0 \\ \pi - \tan^{-1}\dfrac{\sqrt{\Delta_r R_{load}(R_{out}\Delta_r + X_{out}^2)}}{X_{out}R_{load}}, & \text{if } X_{out} > 0 \end{cases} \tag{4.7}$$

Where $\Delta_r = R_{out} - R_{load}$. For a packaged integrated Doherty design, whether symmetric or asymmetric, all of the OCN's design parameters can be obtained using (4.1)-(4.7).

4.3 DPA Design and Measurement Results

A schematic block diagram of the designed two-stage integrated Doherty PA is depicted in Figure 4.3. There are two amplifiers in both carrier and peaking paths. The 1^{st} stage PAs (T_1 and T_3) and the 2^{nd} stage PAs (T_2 and T_4) are called driver and final PAs, respectively. For OBO efficiency enhancement, an asymmetric Doherty architecture of carrier final to peaking final ratio of 1:2 was chosen with actual device sizes as 14 mm and 28 mm. The sizes consider the insertion losses incurred by the OCN for a target peak power of 46 dBm at 2.6 GHz. The OCN was designed based on the methodology described in the previous section. The drain-source capacitance (C_{ds}), including the bondpad metallization, and the optimum load resistance (R_{opt})

values for the carrier final PA were estimated as 3.22 pF and 19 Ω. For these values of C_{ds} and R_{opt}, Q_{dev} approaches unity at 2.6 GHz. Following the theory described in Section II, only a series inductor of $2L_1$ is required for optimum quasi-inverter design. From (4.1), $2L_1$ was calculated as 1.16 nH. This inductor was implemented entirely by bondwire, as portrayed in Figure 4.3, to achieve high Q (Q> 50) and thus minimize the insertion losses incurred by the OCN. Through 3-D EM simulations, the bondwire inductors were optimized and the package parasitics were captured. For α=2, L_w=0.21 nH, C_{p1}=C_{p2}=0.32 pF, and L_p=0.15 nH, R_{out} and X_{out} were calculated as 5.57 Ω and -3.63 Ω from (4.4) and (4.5) using the calculated ABCD parameters from Table 4.1. For, R_{load} of 50 Ω, Z_{tr} and θ_{tr} were calculated as 16.2 Ω and 75.9° from (4.6) and (4.7).

The driver PAs were optimized such that they were not too large to degrade DPA PAE, but not undersized where they could degrade peak power and linearity by becoming overly compressed at the high power condition. Their device sizes are 1.8 mm for the carrier driver and 3 mm for the peaking driver. To design the inter-stage matching networks (ISMNs), load-pull and source-pull simulations were run to find the optimum target load impedances for the driver PAs and source impedances for the final PAs. The input matching networks (IMNs) were designed to conjugately match the input of the driver PAs to 50 Ω. The IMNs and the ISMNs were optimized to achieve good input return loss (IRL) and flat transmission gain across the target frequency band of 2.5-2.7 GHz.

Common practice uses an asymmetric/uneven input splitter for an asymmetric DPA. However, in this design, a symmetric lumped-component based Wilkinson splitter (C_A=C_B=C_C=C_D and L_A=L_B) is used to split the input power evenly between the carrier and the peaking paths. There are some advantages in making this choice. Firstly, the OBO gain can be improved by transmitting more power to the carrier

PA. Secondly, the gate voltage of the class-C biased peaking PA is increased to make up for the reduced transmitted power to the peaking path, which results in improved Doherty linearity. The input phase offset that is located at the input of the peaking path plays a substantial role in proper power combining of the DPA, as this phase offset compensates for the phase difference introduced by the quasi inverter and also the bias dependent phase differences between the two paths. The phase offset circuit was optimized (56.5°) for flat peak power performance and optimum AM/PM variation across the band. An NDF simulation was run to confirm the stability of carrier and peaking paths. Except for the PCB microstrip TL of the quasi transformer (Z_{tr}, θ_{tr}), all of the matching circuits were integrated on a single Si LDMOS substrate.

The Doherty's RF integrated circuit (RFIC) was designed and fabricated using NXP's latest generation of LDMOS technology. The chip micrograph and the evaluation PCB are portrayed in Figure 4.4. The overall IC size is 4.2 mm x 3.4 mm. The IC was mounted in a QFN 7 mm x 7 mm package using a high thermal conductivity die-attach material. The PCB substrate is a Rogers R04350B with 20 mils thickness. The carrier driver and the carrier final stages are biased in class-AB with a quiescent drain current of 11 mA and 52 mA, respectively. The peaking driver and the peaking final stages are biased in class-C (V_{gate1_P}=1.45V and V_{gate2_P}=1.29V). All of the drain (supply) voltages (V_{drain1_C}, V_{drain2_C}, V_{drain1_P} and V_{drain2_P}) are set at 28V. To minimize the PCB footprint, the driver stages' gate and drain biases and the final stages' gate biases are fed through the RF-cold points to eliminate the need for long TLs on the PCB, as illustrated in Figure 4.3. The DPA performance with CW signal excitation is plotted in Figure 4.5(a). The DPA exhibits a 3-dB compressed peak power of 46 dBm, 31.7 dB of gain, and 45-48% PAE at an average output power of 38 dBm (8 dB OBO) from 2.5-2.7 GHz. The AM/PM at peak power reaches only -25°, which helps to enhance the digital predistortion (DPD) linearization capability.

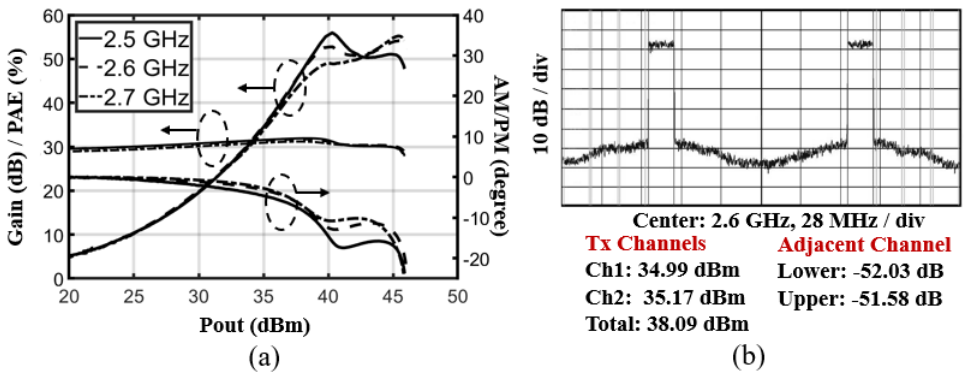

Figure 4.5: (a) Measured Gain, PAE, and AM/PM performance of the DPA under CW signal, and (b) DPD performance with two-carrier 160 MHz LTE

The DPA was linearized with NXP's AFD4400 Digital Frontend DPD system. When driven by a two-carrier 160 MHz LTE signal, the DPA achieves linearized ACPR better than -51 dBc (Figure 4.5(b)) at 38 dBm output power. The DPA performance is compared with other state-of-the-art Doherty designs in Table 4.2, and the presented DPA shows competitive performance, as it demonstrates one of the best combinations of gain and efficiency.

Table 4.2

DPA Performance Summary and Comparison with State-of-the-Art

Ref	[7]	[10]	[11]	[13]	[15]	This Work
Tech	LDMOS	GaN	LDMOS	GaN	GaN	LDMOS
freq (GHz)	1.8-2.2	3.4-3.6	2.5-2.7	2.655	2.1-2.7	2.5-2.7
Psat (dBm)	47	43	42	42.2	41	46
Gain (dB)@Pavg.	16	26	32	30.9	12-14	31.7
PAE (%)@Pavg.	45-49	43	42	46.8	46-53	45-48
Pavg. (dBm)	39	35	34	35.1	33.8	38
Type	Int. Doherty	Int. Doherty	Module	MMIC	MMIC	Int. Doherty

4.4 Summary

This works presents an improved "C_{ds} absorption" based Doherty combiner that may be used in asymmetric DPAs. Based on the proposed combiner, a packaged integrated asymmetric DPA was designed and fabricated, and the DPA demonstrates state-of-the-art performance in a small form factor, with less than 1/3 the size compared to discrete implementations of similar performance [24]. The DPA achieves 45-48% PAE and 31.7 dB gain at 8 dB OBO, with good DPD linearizability.

Chapter 5

A NOVEL EXTENDED BACK-OFF EFFICIENCY RANGE DOHERTY POWER AMPLIFIER

5.1 Introduction

As previously mentioned, with the rapid proliferation of modern telecommunication systems, spectrally efficient digital modulation is essential to enhance the data throughput. This results in complex modulated signal such as orthogonal frequency division multiplexing (OFDM) with high peak-to-average power ratio (PAPR). Being the most power hungry block in a radio transceiver, power amplifiers (PA) often dictate the overall transceiver chain's power dissipation. Therefore, it is critically important for PAs to exhibit high efficiency at large output power back-off (OBO) to facilitate spectrum efficiency under high PAPR (8 to 12 dB) OFDM signals.

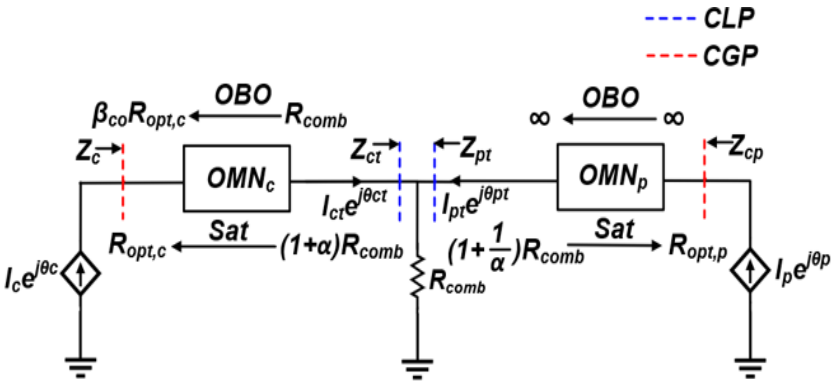

Figure 5.1: Generalized combiner network for conventional Doherty

The symmetric DPA architecture with two amplifiers (carrier and peaking) of same power capability or die periphery is the most common and simplest DPA configuration. However, a symmetric DPA can only achieve high efficiency up to 6 dB

OBO which is largely insufficient to meet these modern communication standards. To improve the efficiency range of DPAs, many excellent works have been conducted over the years. Some of the most popular techniques that are prevalent include multi-path DPA([28]-[33]) and asymmetric DPA architectures ([34]-[44]). In multi-path DPA configuration, more than one peaking amplifiers are utilized to introduce multiple load modulation at different OBO levels. This causes multiple efficiency peaking and therefore, extends the DPA efficiency range. However, the combiner configuration and input drive in these DPAs may become quite complex since multiple peaking amplifiers need to be turned on at specific power levels. Moreover, due to the split of input power in multiple paths, the DPA gain can also become severely limited. In an asymmetric DPA architecture, the peaking amplifier has higher power capability through device sizing ([38]-[44]) or asymmetric drain biasing between the two amplifiers ([34]-[37]). To push the efficiency range as high as 9-10 dB OBO, an asymmetric DPA may require large asymmetry between the carrier and peaking amplifier peripheries, which can also limit the DPA gain ([45],[46]). In the case of asymmetric drain biasing, multiple supply voltage sources are required, which may burden the system with added complexity.

Apart from the techniques that are discussed above, in recent years a different approach has emerged in which the DPA combiner architecture is engineered by introducing new design parameters and thereby gaining more degree of freedom to extend the DPA efficiency range ([47]-[55]). Among these techniques are: non-infinity peaking off-state impedance ([47]-[50]), complex combining load ([51], [52], [54]), and current combining out-of-phase ([53]). In the "non-infinity peaking off-state impedance" approach, the peaking amplifier's off-state impedance presented to the combiner, which is generally assumed as infinity in conventional combiner design, is intentionally designed as non-infinity impedance. In the "complex combining load"

Table 5.1

Comparison Among Different Doherty Configurations

Doherty Configuration	No. of Amplifiers	Peaking to Carrier Combining Current Ratio	Combining Load	Peaking off-state Impedance	Two Combining Currents' Phase Relation
Symmetric (conventional)	2	1	Real	Infinity	In-phase
Asymmetric	2	>1	Real	Infinity	In-phase
Multi-path	>2	1 or >1	Real	Infinity	In-phase
Complex Load	2	1	Complex	Infinity	In-phase
Non-infinity Peaking Off-state	2	1	Real	Non-Infinity	In-phase
Out-of-phase Current Combining	2	1	Real	Infinity	Out-of-phase

approach, the combining load impedance, which is generally a real-value, is designed as a complex-value impedance. In the "current combining out-of-phase" approach, the phases of the two combining currents, which are generally in-phase at saturated power, are engineered to be out-of-phase. These methods were predominantly targeted for symmetric DPA architectures to extend their back-off level beyond 6 dB. However, these techniques primarily suffer from limited design space and hence not enough flexibility to improve other design metrics such as RF operating bandwidth. Very recently, the "complex combining load" method ([54]) and a combination of "non-infinity peaking off-state" impedance and "current combining in out-of-phase" methods ([55]) were introduced in DPA architectures using unequal carrier and peaking cells. Even though unequal cells were used in these works, the DPA was treated as a symmetric configuration by intentionally designing the combining current ratio

to be equal to one. In [54], a smith chart-based complex combining load DPA design approach was introduced that could operate at a single frequency. Notably in [55], it was shown that combining multiple methods provides design flexibility and by finding a design space using a numerical solution, a DPA of $> 8\%$ fractional RF bandwidth was designed. Table 5.1 presents a comparative summary that summarizes the different design characteristics of existing Doherty architectures.

In this work, a novel extended efficiency range DPA combiner for arbitrary combining current ratio is presented that establishes a correlated relationship between peaking off-state and combining load impedances. Starting from a discussion of the fundamental limitation of a conventional output combiner to extend the back-off efficiency range, it is shown that the interaction between peaking off-state impedance and combining load impedances can be engineered to extend the efficiency range with enhanced design flexibility. A compact closed form relationship between the two parameters is established, which gives a PA designer a set of closed form equations to design their amplifier for their desired requirements. Regardless of infinity or non-infinity off-state impedance and real or complex valued combining load impedance, the presented method is developed to work as long as the presented closed form relationship between the two parameters are maintained. A step-by-step DPA design for packaged transistors based on the ABCD parameters are presented, and a proof-of-concept prototype DPA is designed with an asymmetric configuration to validate the presented theory. Unlike the previous works, the full power capability of the two active devices (PAs) will be utilized and the mild asymmetry between the two devices will be shown as a design advantage. The organization of this chapter is as follows. In section 5.2, the theory and fundamental operation and formulation of the necessary parameters of the proposed combiner is detailed. Section 5.3 covers the design methodology and simulated performance of the prototype DPA based on the theory

presented in section 5.2. Section 5.4 presents the fabrication details of the prototype DPA and its measured performance compared with state-of-the art DPAs. Section 5.5 makes conclusions about this work.

5.2 Theory

The fundamentals of dynamic load modulation in DPAs are well explained in literature ([8], [45], [46]). In Doherty operation, the carrier amplifier is generally biased in class-B or class-AB, and the peaking amplifier in class-C. At low power conditions, the peaking amplifier remains off and an increased load condition is enforced at the carrier's output to increase the effective output voltage swing. As the power goes up, the output voltage swing gets maximized with the saturation of the carrier amplifier and the first efficiency peak of the Doherty is obtained. At this point, the peaking amplifier turns on and the current injected by the peaking amplifier at the combining load causes active load modulation of the carrier amplifier. As the power goes up further, the carrier amplifier continues to get load modulated. In this high power region, both carrier and peaking amplifiers contribute to output power. The second Doherty efficiency peak is produced when the Doherty output power is saturated with the saturation of both amplifiers.

5.2.1 Conventional Doherty Combiner and Its Limitations

A generalized combiner network for a conventional Doherty is presented in Figure 5.1. Carrier and peaking amplifiers are represented as voltage controlled current sources ($I_c e^{j\theta_c}$ and $I_p e^{j\theta_p}$). In a conventional combiner, the combining load impedance is a real impedance (R_{comb}), and the impedance presented to the combining load by the peaking amplifier is maintained (and assumed) at infinity to completely isolate the peaking PA's effect on the combining load at OBO ([8], [45], [46]). The combin-

ing currents are expressed as $I_{ct}e^{j\theta_{ct}}$ and $I_{pt}e^{j\theta_{pt}}$ in Figure 5.1. The two currents are combined in-phase in a conventional combiner, and hence $\theta_{ct} = \theta_{pt}$. If the matching networks are assumed to be reciprocal and lossless, then the ratio of the power generated by both amplifiers at the current generator plane (CGP) and the combining current ratio at the (CLP) should be the same. If that ratio is defined as α and the load modulation ratio (LMR) is represented as β, then α and β can be expressed as:

$$\alpha = \frac{P_{sat,p}}{P_{sat,c}} = \frac{I_{pt}e^{j\theta_{pt}}}{I_{ct}e^{j\theta_{ct}}} = \frac{I_{pt}}{I_{ct}} \tag{5.1}$$

$$\beta = \frac{P_{sat,c}}{P_{break}} \tag{5.2}$$

Here, P_{break} represents the power at break-point when the first efficiency peak comes out with the onset of peaking amplifier's turning on. If β_{co} represents the LMR for conventional combiner, following analysis explicitly derives the relationship between α and β_{co}.

In Figure 5.1, the combining load impedance is represented as R_{comb}. In terms of α and R_{comb}, following expressions summarize the impedances at the combining load plane (CLP) at OBO and saturated power conditions,

$$Z_{ct,obo} = R_{comb} \tag{5.3}$$

$$Z_{ct,sat} = (1+\alpha)R_{comb} \tag{5.4}$$

$$Z^{*}_{pt,obo} = \infty \tag{5.5}$$

$$Z_{pt,sat} = (1+\frac{1}{\alpha})R_{comb} \tag{5.6}$$

For the above load conditions at CLP, OMN_c and OMN_p ensures that by impedance transformation, proper load conditions are presented at the current generator plane (CGP). Generally, an odd multiple of quarter wavelength ($n\lambda/4, n = 1, 3, ..$) impedance inverter with characteristic impedance of $(\beta_{co} \cdot R_{opt,c} \cdot R_{comb})^{1/2}$ is used as OMN_c. Here, $R_{opt,c}$ represents the optimum load impedance for the carrier PA. The OMN_p is de-

signed to match between $Z_{pt,sat}$ at CLP and $R_{opt,p}$ at CGP, where $R_{opt,p}$ is the optimum load impedance for the peaking PA. The insertion phase of OMN_p is maintained as $m\pi$, where $m = 0, 1, 2...$ so that the infinite off-state impedance of class-C biased peaking PA at CGP is transferred to CLP at OBO condition. All the impedances at CGP for conventional Doherty operation are expressed in the following,

$$Z_{c,obo} = \beta_{co} R_{opt,c} \tag{5.7}$$

$$Z_{c,sat} = R_{opt,c} \tag{5.8}$$

$$Z^*_{p,obo} = \infty \tag{5.9}$$

$$Z_{p,sat} = R_{opt,p} \tag{5.10}$$

$$|\theta_p - \theta_c| = \frac{n\pi}{2}, n=1,3,... \tag{5.11}$$

If the load and source reflection coefficients for conventional DPA are presented as $\Gamma_{L,co}$ and $\Gamma_{S,co}$, then they can be expressed in terms of CLP and CGP impedances as follows-

$$\begin{aligned} \Gamma_{L,co} &= \frac{Z_{ct,obo} - Z_{ct,sat}}{Z_{ct,obo} + Z^*_{ct,sat}} = \frac{R_{comb} - (1+\alpha)R_{comb}}{R_{comb} + (1+\alpha)R_{comb}} \\ &= \frac{-\alpha}{2+\alpha} \end{aligned} \tag{5.12}$$

$$\begin{aligned} \Gamma_{S,co} &= \frac{Z_{c,co,obo} - Z_{c,co,sat}}{Z_{c,co,obo} + Z^*_{c,co,sat}} = \frac{\beta_{co} R_{opt,c} - R_{opt,c}}{\beta_{co} R_{opt,c} + R_{opt,c}} \\ &= \frac{\beta_{co} - 1}{\beta_{co} + 1} \end{aligned} \tag{5.13}$$

$\Gamma_{L,co}$ and $\Gamma_{S,co}$ are related to each other in terms of the s-parameters of OMN, by following expression,

$$\Gamma_{S,co} = S_{11} + \frac{S_{12} S_{21} \Gamma_{L,co}}{1 - S_{22} \Gamma_{L,co}} \tag{5.14}$$

From power wave theory, s-parameters of a reciprocal and lossless OMN can be

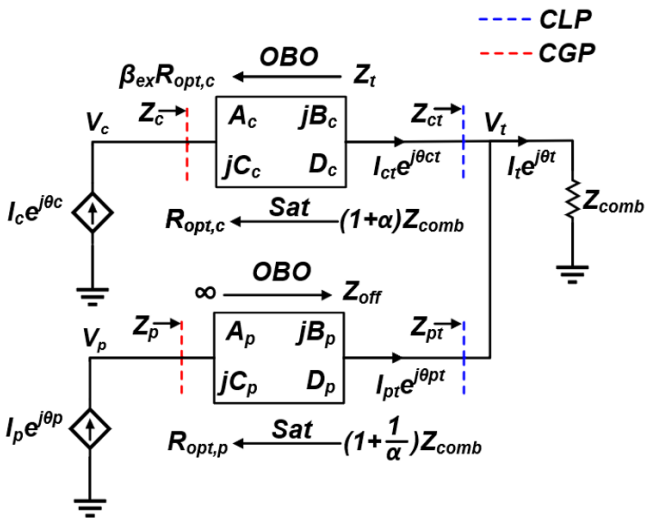

Figure 5.2: Generalized combiner network for the proposed COCL Doherty

defined as,

$$[S] = \begin{bmatrix} 0 & e^{j\theta} \\ e^{j\theta} & 0 \end{bmatrix} \tag{5.15}$$

Using the s-parameters from (5.15) to (5.14),

$$\begin{aligned} \Gamma_{S,co} &= \Gamma_{L,co} e^{j2\theta} \\ \Rightarrow |\Gamma_{S,co}| &= |\Gamma_{L,co}| \end{aligned} \tag{5.16}$$

From (5.16), when OMNs are reciprocal and lossless the magnitude of load and source reflection coefficients should be equal. Using the expressions of $\Gamma_{L,co}$ and $\Gamma_{S,co}$ from (5.12) and (5.13) to (5.16), following relationship between β_{co} and α can be found,

$$\beta_{co} = 1 + \alpha \tag{5.17}$$

The OBO of a DPA is defined as the ratio between the saturated power of DPA, $P_{sat,DPA}$ and power at break-point, P_{break}. The OBO in dB can thus be expressed as

following-

$$OBO = 10\log(\frac{P_{sat,DPA}}{P_{break}}) = 10\log(\frac{P_{sat,c}}{P_{break}}\frac{P_{sat,DPA}}{P_{sat,c}}) \tag{5.18}$$

$$\text{Here, } \frac{P_{sat,DPA}}{P_{sat,c}} = \frac{P_{sat,c} + P_{sat,p}}{P_{sat,c}} = (1+\alpha) \tag{5.19}$$

Using (5.2) and (5.19) in (5.18), OBO in dB can be re-written as,

$$OBO = 10\log(\beta(1+\alpha)) \tag{5.20}$$

(5.20) is the most general expression of OBO in dB for any Doherty configuration. Considering the relation between LMR and α for a conventional combiner from (5.17), one can find the OBO in dB for a conventional combiner (OBO_{co}) from (5.20) as,

$$OBO_{co} = 20\log(1+\alpha) \tag{5.21}$$

From (5.21), OBO_{co} is a function of saturated power or combining current ratio, α only. This makes OBO_{co} to be dependent of entirely the saturated power capabilities of the two devices. Since, unity power utilization factor (PUF) by harnessing maximum voltage and current capabilities of two amplifiers is desirable in DPA operation, this puts more stringent constraint on OBO_{co}. In some prior works, the ratio α for a pair of carrier and peaking PAs is increased by either using different drain supply voltages ([34]-[37]) or by sacrificing PUF ([38]) e.g. harnessing less power from the carrier PA from what it is maximally capable of. Both approaches may be undesirable for practical application. Using same drain supply voltage reduces the complexity by eradicating the need for one additional power supply and unity PUF condition guarantees the reduction of cost by minimizing the die sizes. The other more practical option to increase α while using same drain supply voltage and maintaining unity PUF is to increase the peaking amplifier size with respect to carrier amplifier ([39]-[43]). However, to achieve high extended back-off range such as 9.5-10 dB OBO, α of

1.98-2.16 would be required from (5.21) and this kind of high asymmetry can start limiting the gain of the DPA because of highly uneven input power splitting ([45],[46]). Therefore, to attain more flexibility in combiner architecture could become beneficial to improve DPA performance while achieving high extended back-off range.

To increase the flexibility of DPA combiner, several methods were published in the past ([47]-[55]) to extend the OBO of DPA by introducing new design parameters in the combiner architecture. In this work, a new method is proposed to extend the OBO of DPA of any arbitrary power ratio, by engineering the interaction between combining load and peaking off-state impedances. The unique close form relationship that will be established between these two parameters will show that correlated variation of combining load impedance with peaking off-sate impedance expands the design space. For simplicity, the proposed combining method is named as COCL (Correlated Off-state and Combining Load) method. Since the proposed COCL method offers more degree of freedom than conventional combiner, enhanced design flexibility to optimize the DPA performance is possible. It will also be shown that some of the previously published works are subsets of the proposed COCL architecture. The theory behind the new combiner's operation is presented in the next section.

5.2.2 Proposed COCL Doherty Operating Principle

A generalized Doherty combiner network based on ABCD transmission parameter is depicted in Figure 5.2 to describe the operating principle of the proposed combiner. To simplify the analysis few assumptions are made as following-

1. Piece-wise linear current generator model is assumed with zero knee voltage condition thus optimum voltage swing at full power and OBO condition should be same.

2. Carrier amplifier is class-B biased and peaking amplifier is class-C biased. Optimum impedances are presented to the amplifiers at OBO and saturated power conditions.

3. The same drain bias voltage is used for both amplifiers and target PUF is unity.

4. All the higher order harmonics are short-circuited. Only fundamental component is considered for efficiency calculation.

In addition to above assumptions, it's also assumed that the matching networks are lossless and reciprocal and the combining is coherent ($\theta_{ct} = \theta_{pt}$). 'obo' and 'sat' subscripts will represent in the subsequent analysis the OBO and saturated power conditions respectively. 'co' and 'ex' subscripts will represent conventional and extended back-off parameters respectively. First and foremost, for extended back-off operation, the general expectation is to achieve higher LMR and OBO than a conventional combiner. Therefore, following boundary conditions are set at first for LMR and OBO parameters of the extended back-off combiner,

$$\begin{cases} OBO_{ex} > OBO_{co} \\ \beta_{ex} = \dfrac{10^{(OBO_{ex}/10)}}{1+\alpha} \end{cases} \tag{5.22}$$

To satisfy (5.22), additional parameters need to be introduced in the combiner architecture so that load reflection coefficient can be controlled by the new parameters, in addition to α. At the same time, the OMNs of the proposed combiner should be designed with the new parameters in such a way so that they can translate the load modulation at the CLP from low to high power transition to CGP without incurring any losses-same as it was the case for conventional combiner.

In a conventional combiner, it's assumed that the peaking off-state impedance (Z_{off}) is infinity and does not interact with the combining load at back-off when

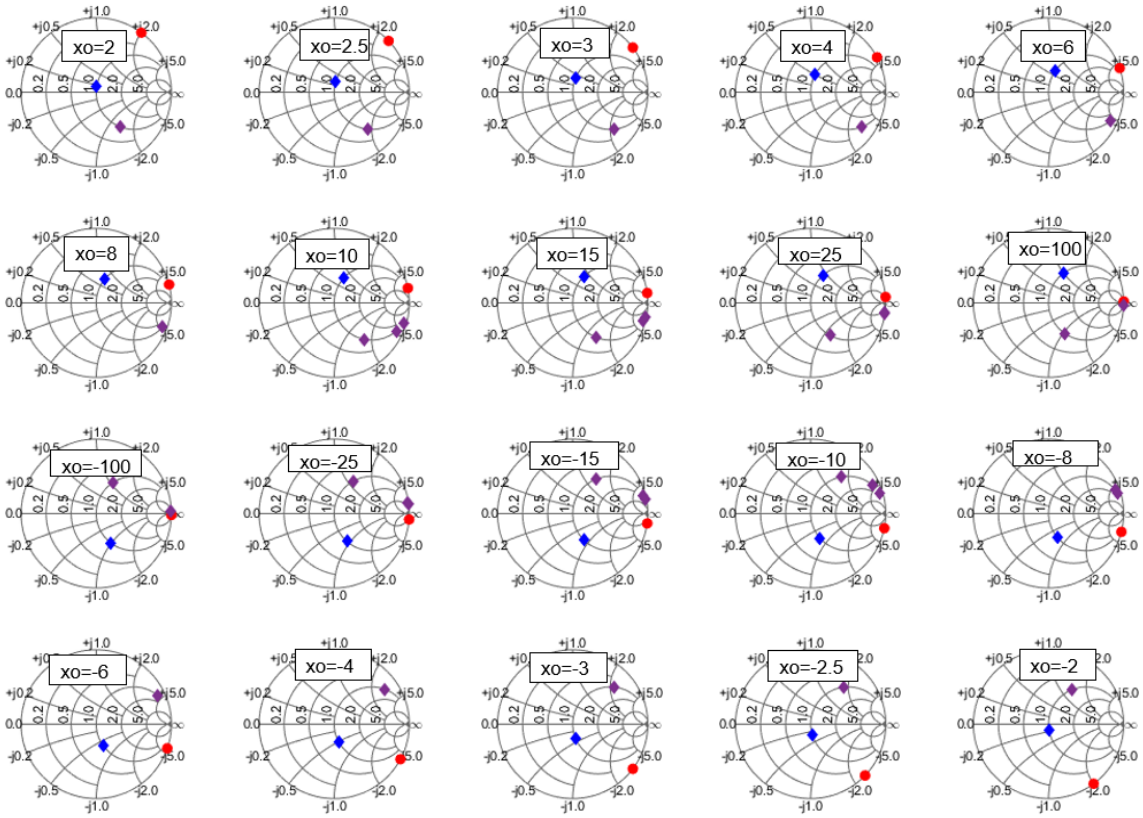

Figure 5.3: Location of $Z_c = R_c(1 + jx_c)$ (blue and purple) for different values $Z_{off} = jR_c x_o$ (red) when $\alpha = 1.5$, $OBO_{ex} = 9.5$ dB and $R_c = 15\Omega$ on smith charts. Charts are normalized to R_c.

peaking amplifier is tuned off. However, it's impossible to achieve infinite peaking off-state condition in a wideband application for all the frequencies involved. In that case, when Z_{off} becomes non-infinity, it interacts with the combining load impedance (Z_{comb}) at OBO and the impedance looking from the carrier at CLP (Z_t) does not remain the desired real impedance anymore. In the proposed combiner, this interaction between Z_{off} and Z_{comb} is taken into consideration to extend the OBO range. To do that, mathematically, Z_{comb} and Z_{off} should be considered as complex and non-infinity so that they can assume any arbitrary value and in the limiting case, can approach infinity and real impedance if necessary. Hence, defining these two impedances as non-infinity and complex is the most generic representation to engi-

neer their interaction for extending the OBO range. In light of this conviction, Z_{comb} and Z_{off} can be expressed as,

$$Z_{comb} = R_c(1 + jx_c) \tag{5.23}$$

$$Z_{off} = jR_c x_o \tag{5.24}$$

Here, R_c represents the real part of combining load and x_c and x_o represent normalized imaginary part of the combining load and off-state impedances with respect to R_c. The off-state impedance is assumed to be located at the high impedance region at the right edge of the smith chart and therefore, the real part of the off-state impedance can be ignored. from (5.23) and (5.24), two new parameters x_o and x_c appeared in the proposed combiner which can now be engineered to satisfy the boundary condition (5.22). In the subsequent analysis, a closed form relationship between x_o and x_c will be established. For a target OBO_{ex}, it will be shown that this relationship can be maintained for a large design space which provides additional design flexibility.

If, Z_t represents the impedance looking into the CLP from carrier side at OBO, then Z_t can be defined as,

$$Z_{comb,obo} = Z_t = R_t(1 + jx_t) \tag{5.25}$$

Here, R_t is the real part of Z_t and x_t is the normalized imaginary part of Z_t with respect to R_t. From Figure 5.2, Z_t is also a parallel combination of Z_{comb} and Z_{off}. Hence, the following relationship can be established between Z_t, Z_{comb} and Z_{off},

$$\begin{aligned} Z_t &= Z_{comb}//Z_{off} \\ \Rightarrow R_t(1 + jx_t) &= \frac{R_c(1 + jx_c) \cdot (jR_c x_o)}{R_c(1 + jx_c) + jR_c x_o} \end{aligned} \tag{5.26}$$

Z_{comb} and Z_{off} expressions from (5.23) and (5.24) and Z_t expression from (5.25) are utilized in (5.26). Equating the real and imaginary parts on both sides, following

relationships between R_t, x_t, R_c and x_c are found.

$$R_t = \frac{R_c x_o^2}{1 + (x_c + x_o)^2} \tag{5.27}$$

$$x_t = x_c + \frac{1 + x_c^2}{x_o} \tag{5.28}$$

The lossless OMN at the carrier output must be designed to accomplish load modulation as such that at OBO it matches Z_t at the CLP to $\beta_{ex} R_{opt,c}$ at CGP and at saturation, it matches $(1+\alpha)Z_{comb}$ at CLP to $R_{opt,c}$ at CGP. If the load reflection coefficient and source reflection coefficient for proposed combiner are denoted as $\Gamma_{L,ex}$ and $\Gamma_{s,ex}$, then from above description they can be expressed as,

$$\begin{aligned} \Gamma_{L,ex} &= \frac{Z_{ct,obo} - Z_{ct,sat}}{Z_{ct,obo} + Z^*_{ct,sat}} = \frac{Z_t - (1+\alpha)Z_{comb}}{Z_t + (1+\alpha)Z^*_{comb}} \\ &= \frac{R_t(1 + jx_t) - (1+\alpha)R_c(1 + jx_c)}{R_t(1 + jx_t) + (1+\alpha)R_c(1 - jx_c)} \end{aligned} \tag{5.29}$$

$$\Gamma_{S,ex} = \frac{Z_{c,obo} - Z_{c,sat}}{Z_{c,obo} + Z^*_{c,sat}} = \frac{\beta_{ex} R_{opt} - R_{opt}}{\beta_{ex} R_{opt} + R_{opt}} = \frac{\beta_{ex} - 1}{\beta_{ex} + 1} \tag{5.30}$$

Using the same s-parameter relation in terms of reciprocal and lossless OMN as described for conventional combiner in the previous section (see (13)-(15)), the relation between the magnitude of the two reflection coefficients can be expressed as,

$$|\Gamma_{S,ex}| = |\Gamma_{L,ex}| \tag{5.31}$$

Using R_t and x_t from (5.27) and (5.28) in (5.31) and by simple mathematical manipulation $|\Gamma_{L,ex}|$ can be expressed as,

$$|\Gamma_{L,ex}| = \sqrt{\frac{(1 + x_c^2)(\beta_{co}^2 + (\beta_{co} x_c + \alpha x_o)^2)}{(1 + x_c^2)(\beta_{co}^2 + (\beta_{co} x_c + \alpha x_o)^2) + 4\beta_{co} x_o^2}} \tag{5.32}$$

For simplicity, $\beta_{co} = 1 + \alpha$ relation from (5.17) is utilized in (5.32) and same will be followed in rest of the analysis. By inserting $|\Gamma_{L,ex}|$ from (5.32) to (5.31) and

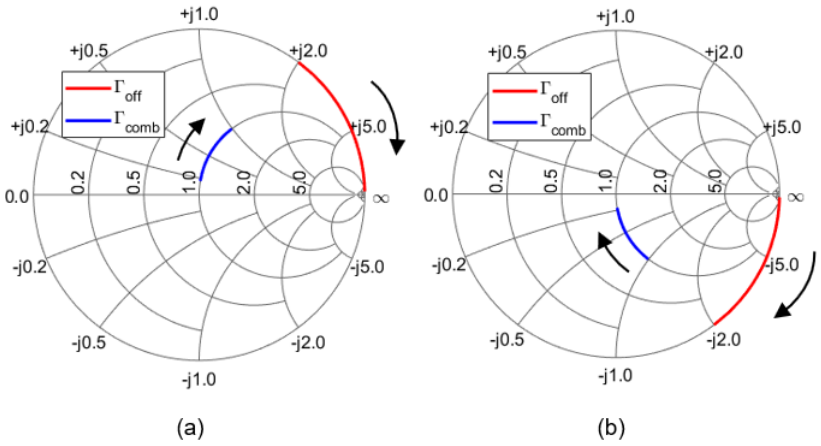

Figure 5.4: Locus of Γ_{off} and Γ_{comb} in the (a) inductive design space and (b) capacitive design space

$\Gamma_{S,ex}$ from (5.30) to (5.31) and by some mathematical manipulation, one can obtain a quartic equation for x_c. Solving that equation for x_c, results in following expressions,

$$x_c = \frac{-\alpha\sqrt{\beta_{ex}}x_o \pm \sqrt{x_p}}{2\beta_{co}\sqrt{\beta_{ex}}} \tag{5.33}$$

$$x_p = \alpha^2 x_o^2 \beta_{ex} - 4\beta_{co}(\beta_{ex}\beta_{co} \pm \sqrt{\beta_{ex}x_o^2(\beta_{ex}-\beta_{co})(\beta_{ex}\beta_{co}-1)}) \tag{5.34}$$

From (5.33) and (5.34) , one can find that x_c is a function of α, β_{co}, β_{ex} and x_o. For a given carrier and peaking amplifier pair, α and β_{co} are known parameters. If OBO_{co} is calculated from (5.21), then the target OBO_{ex} can be set from and β_{ex} can be calculated from boundary conditions in (5.22). Therefore, x_o becomes the only unknown to find x_c.

Though it appears that x_o is a free variable, a valid operating range can be determined by carefully evaluating (5.33) and (5.34). From (5.33), a valid solution for x_c can only be achieved if, $x_p \geq 0$. Using this condition on (5.34), boundary condition for x_o can be found as-

$$\{x_o | x_o \leq -x_{o,lim} \text{ or } x_o \geq x_{o,lim}\} \tag{5.35}$$

Table 5.2

x_c for Different Values of x_o and α When, $OBO_{ex} = 8.5$ and 9.5 dB

	$OBO_{ex} = 8.5\ dB$			$OBO_{ex} = 9.5\ dB$		
x_o	$\alpha = 1$	$\alpha = 1.25$	$\alpha = 1.5$	$\alpha = 1$	$\alpha = 1.25$	$\alpha = 1.5$
± 2	± 0.436	± 0.136	∓ 0.412	± 0.657	± 0.420	± 0.168
± 2.5	± 0.568	± 0.277	∓ 0.112	± 0.790	± 0.545	± 0.299
± 3	± 0.665	± 0.371	± 0.007	± 0.892	± 0.636	± 0.386
± 4	± 0.803	± 0.493	± 0.138	± 1.044	± 0.765	± 0.503
± 6	± 0.976	± 0.633	± 0.265	± 1.241	± 0.923	± 0.635
± 8	± 1.083	± 0.713	± 0.331	± 1.370	± 1.020	± 0.711
± 10	± 1.158	± 0.767	± 0.373	± 1.461	± 1.086	± 0.762
± 15	± 1.276	± 0.847	± 0.431	± 1.610	± 1.189	± 0.836
± 25	± 1.391	± 0.920	± 0.481	± 1.760	± 1.288	± 0.904
± 50	± 1.497	± 0.982	± 0.520	± 1.904	± 1.375	± 0.961
± 100	± 1.558	± 1.016	± 0.541	± 1.989	± 1.424	± 0.992

The expression for $x_{o,lim}$ can be found in (5.36). As long as, x_o is within the range as expressed in (5.35), at least one solution for x_c is guaranteed. (5.33)-(5.35) along with (5.36), establishes the fundamental relationship between x_o and x_c to achieve extended OBO efficiency range for a DPA.

$$x_{o,lim} = \sqrt{\frac{A - 8\sqrt{B}}{\alpha^4 \beta_{ex}}} \tag{5.36}$$

Where, $A = 4\beta_{co}^2((\alpha^2-2)\beta_{ex}+2\beta_{co}(1-\beta_{co}\beta_{ex}+\beta_{ex}^2))$ and $B = \beta_{co}^4(\beta_{co}-\beta_{ex})(\beta_{co}\beta_{ex}-1)(\beta_{co}((\beta_{co}-\beta_{ex})\beta_{ex}-1)-(\alpha^2-1)\beta_{ex})$.

In x_c expression of (5.33) there are two $\pm$ signs including the $\pm$ embedded into x_p from (5.34). Therefore, there can be as many as four possible solutions. To demonstrate the x_c solutions that are produced for a given value of x_o to achieve extended OBO, α is chosen as 1.50, which would make β_{co} and OBO_{co} to be 2.5 and 7.96 dB respectively from (5.17) and (5.21). If the target OBO_{ex}, which can be any value greater than OBO_{co} according to (5.22), is chosen as 9.5 dB, then β_{ex} can be

calculated from (5.22) as 3.565. With these values of α, β_{co} and β_{ex}, $x_{o,lim}$ is calculated from (5.36) as 1.3567. Hence, according to (5.35), any x_o value greater than -1.3567 or less than 1.3567 should be avoided to get valid combining load impedance for the target OBO_{ex}. Let's choose 2 to 100 in the +ve range and -100 to -2 in the -ve range as two safe ranges for x_o to achieve at least one valid solution for x_c. For different values of x_o, in these two ranges, x_c is calculated at first from (5.33)-(5.34) and then off-state impedance, Z_{off} and combining load impedance, Z_{comb} are calculated from (5.23) and (5.24) for each case when, R_c is 15Ω. Please note, R_c is a free parameter and can be optimized in a real design. For each case, calculated Z_{off} and Z_{comb} are then plotted on smith chart (see Figure 5.3). It can be observed that, Z_{comb} solutions are symmetric with respect to Z_{off}- two sets of Z_{comb} solutions that are produced from two conjugate Z_{off} values, are also complex conjugate to each other. This is true for any value of α and target OBO_{ex}. In each solution set, Z_{comb} with minimum magnitude of x_c (blue diamond marker in Figure 5.3) is considered as the primary solution whilst others are considered as secondary solutions. In rest of the work, all the discussions are limited to primary solution only. The reasons for preferring the primary solution over the others are twofold. Firstly, it has the minimum magnitude among all x_c, which minimizes the Q of the combining load. Secondly, this is the only solution, that maintains the correlated relationship with x_o for the widest possible x_o range. The significance of these two features will be elaborated shortly.

Table 5.2 summarizes calculated primary x_c for 8.5 and 9.5 dB OBO_{ex} while varying x_o from $\pm$2 to $\pm$100 and α from 1 to 1.5. It's noticeable that, for same x_o values, as α goes up, magnitude of x_c goes down. In practical design, a post-matching network is designed to match 50Ω load impedance to combining load impedance, Z_{comb}. As, x_c is the normalized reactive part of Z_{comb}, it's magnitude simply determines the quality factor (Q) of the impedance transformer network. From Bode-Fano criteria

([56], [57]), bandwidth (BW), in-band reflection co-efficient (Γ_{avg}) and the Q of complex load are related to each other by (5.37). As Q goes down, BW improves and vice versa. Therefore, for a target OBO_{ex}, higher α value is beneficial to lower the Q of the combining load impedance and thus, improving the bandwidth. This also validates why primary solution for x_c is chosen as the one with minimum Q value.

$$\frac{BW}{\omega_0}\ln(\frac{1}{\Gamma_{avg}}) \leq \frac{\pi}{Q} \tag{5.37}$$

Special case I: infinite peaking off-state impedance

A special case of the proposed combining topology is when peaking off-state impedance approaches infinity. By imposing that condition in (5.31) and solving for x_c, would result in following expression,

$$\lim_{x_o \to \infty} |\Gamma_{L,ex}| = |\Gamma_{s,ex}|$$

$$\Rightarrow x_c = \pm\sqrt{\frac{(\beta_{ex} - \beta_{co})(\beta_{ex}\beta_{co} - 1)}{\alpha^2 \beta_{ex}}} \tag{5.38}$$

The solution of x_c in (5.38) is what was proposed in original "complex combining load" theory ([30],[31],[33]) to utilize only complex combining load for extending the BO efficiency range for symmetric DPA ($\alpha = 1$, $\beta_{co} = 2$). The "complex combining load" theory lacks the more generic case when off-state impedance is arbitrary non-infinity value and also combining current ratio is any arbitrary value. Therefore, the x_c solutions achieved in "complex combining load" theory only limited to two and does not offer the proposed expanded design space that will be discussed shortly.

Special case II: real combining load impedance

Another special case might be of interest is what the off-state peaking impedance value would be when the combining load impedance approaches real value for extended

OBO range. That can be derived easily by imposing limiting condition for x_c to be zero in (5.31) and solving for x_o. That results in following expression,

$$\lim_{x_c \to 0} |\Gamma_{L,ex}| = |\Gamma_{s,ex}|$$

$$\Rightarrow x_o = \pm\sqrt{\frac{\beta_{co}^2 \beta_{ex}}{(\beta_{ex} - \beta_{co})(\beta_{ex}\beta_{co} - 1)}} \tag{5.39}$$

The earlier works on two-way extended-OBO efficiency range DPA utilizing only "non-infinity peaking off-state impedance" approach is based on the x_o solution in (5.39) ([25]-[29]). It's interesting to see that the extended-OBO efficiency range DPA combiner based on "complex combining load" method (special case I) and "non-infinity peaking off-state impedance" method (special case II) are part of a same generic system and are two special cases of the proposed COCL combiner. There exists many extended-OBO efficiency modes in between these two solutions (see Figure 5.4 and Table 5.2) that can only be discovered by the proposed theory. These new modes are enormously beneficial for designing extended-OBO efficiency range combiner with enhanced design flexibility such as to improve bandwidth, linearity etc.. To enlighten this point, in Figure 5.4, Γ_{off} and Γ_{comb} are plotted on smith-chart when $OBO_{ex} = 9.5\ dB$ and $\alpha = 1.5$ based on the values presented in Table 5.2. Based on the sign of x_o and x_c, two separate continuum of design spaces at inductive (Figure 5.4(a)) and capacitive (Figure 5.4(b)) regions are produced. Each combining load impedance, Z_{comb} on Γ_{comb} locus corresponds to an off-state impedance, Z_{off} on Γ_{off} locus and these two impedances change their values in correlated fashion. The arrows show the relative direction of Z_{off} and Z_{comb} as their values change along Γ_{off} and Γ_{comb} loci. It can also be observed that the direction of the arrows follow foster or clockwise rotation. To associate this with off-state impedances of peaking amplifier variation with frequency, they normally rotate in clockwise direction while

transitioning from low to high-frequency. At the same time, the clockwise variation of the combining load impedances for multiple frequencies can be supported by judicial design of the post-matching network (PMN). Therefore, COCL combiner provides the flexibility to accommodate multiple frequencies to follow these two trajectories in correlated manner, which can be beneficial to improve the bandwidth performance. The similar design space can be produced for any arbitrary α value and target OBO_{ex}.

5.2.3 Derivation of the ABCD Parameters

The theory and fundamental operating principle of the proposed combiner was discussed in details in the previous section. More specifically, the unique closed-form relationship between x_o and x_c or Z_{off} and Z_{comb} was established to achieve extended BO operation. It's equally important to derive a general formulation for the output matching networks (OMNs) of carrier and peaking PAs in order to achieve correct operation of the proposed combiner. With that aim, the OMNs of the carrier and peaking PAs are represented as generalized two-port ABCD networks (see Figure 5.2) and in this section closed-form formulation of these ABCD parameters will be deduced. Following boundary conditions are set for the derivation of ABCD parameters-

1. The combining currents magnitude ratio ($|I_{pt}|/|I_{ct}|$) is α and the combining currents are in phase (θ_{ct}=θ_{pt}).

2. At OBO, the carrier OMN must present a match between Z_t at the combining plane to $\beta_{ex}R_{opt,c}$ at carrier CGP.

3. At saturated power, the carrier OMN must present a match between $(1 + \alpha)Z_{comb} = \beta_{co}Z_{comb}$ at the combining load to $R_{opt,c}$ at carrier CGP.

4. At OBO, the peaking OMN must present non-infinite off-state impedance Z_{off}

to the combining load. This allows Z_{off} to approach infinity in a special case (special case I).

5. At saturated power, the peaking OMN must present a match between $(1 + 1/\alpha)Z_{comb} = (\beta_{co}Z_{comb})/\alpha$ at the combining load to $R_{opt,p}$ at peaking CGP.

In order to meet the carrier OMN requirements at OBO and saturated power conditions, following relations can be obtained between CGP and CLP impedances in terms of carrier ABCD parameters-

$$\beta_{ex}R_{opt,c} = \frac{A_cR_t(1 + jx_t) + jB_c}{jC_cR_t(1 + jx_t) + D_c} \tag{5.40}$$

$$R_{opt,c} = \frac{A_c\beta_{co}R_c(1 + jx_c) + jB_c}{jC_c\beta_{co}R_c(1 + jx_c) + D_c} \tag{5.41}$$

Similarly, imposing the peaking matching requirements at OBO and saturated power conditions, following relationships can be established between CGP and CLP impedances in terms of peaking ABCD parameters-

$$\infty = \frac{-jA_pR_cx_o + jB_p}{jC_pR_cx_o + D_p} \tag{5.42}$$

$$R_{opt,p} = \frac{A_p\beta_{co}R_c(1 + jx_c) + j\alpha B_p}{jC_p\beta_{co}R_c(1 + jx_c) + \alpha D_p} \tag{5.43}$$

From (5.40), (5.41) and (5.43) and using lossless and reciprocal condition for the

OMNs, following expressions can be deducted-

$$A_c R_t x_t + B_c = C_c \beta_{ex} R_{opt,c} R_t \tag{5.44}$$

$$D_c R_{opt,c} - C_c \beta_{co} R_{opt,c} R_c x_c = A_c \beta_{co} R_c \tag{5.45}$$

$$A_c \beta_{co} R_c x_c + B_c = C_c \beta_{co} R_{opt,c} R_c \tag{5.46}$$

$$A_c D_c + B_c C_c = 1 \tag{5.47}$$

$$D_p \alpha R_{opt,p} - C_p R_{opt,p} \beta_{co} R_c x_c = A_p \beta_{co} R_c \tag{5.48}$$

$$A_p \beta_{co} R_c x_c + \alpha B_p = C_p R_{opt,p} \beta_{co} R_c \tag{5.49}$$

$$A_p D_p + B_p C_p = 1 \tag{5.50}$$

Carrier ABCD parameters (A_c, B_c, C_c, and D_c) can be derived from (5.44)-(5.47). After deriving C_p from (5.42), remaining peaking ABCD parameters (A_p, B_p, and D_p) can be easily derived from (5.48)-(5.50). All the derived ABCD parameters are summarized below-

$$A_c = \frac{C_c(\beta_{co} R_c - \beta_{ex} R_t) R_{opt,c}}{M} \tag{5.51}$$

$$B_c = \frac{\beta_{co} C_c R_c R_t R_{opt,c} (\beta_{ex} x_c - x_t)}{M} \tag{5.52}$$

$$C_c = \pm \sqrt{\frac{M}{\beta_{co} R_c R_{opt,c} ((\beta_{co} R_c - R_t \beta_{ex})^2 + M^2)}} \tag{5.53}$$

$$D_c = \frac{\beta_{co} C_c R_c (\beta_{co} R_c (1 + x_c^2) - R_t (\beta_{ex} + x_c x_t))}{M} \tag{5.54}$$

$$M = \beta_{co} R_c x_c - R_t x_t \tag{5.55}$$

$$A_p = \frac{D_p R_{opt,p} (\alpha x_o + \beta_{co} x_c)}{x_o \beta_{co} R_c} \tag{5.56}$$

$$B_p = -\frac{D_p R_{opt,p} (\beta_{co} (1 + x_c^2) + \alpha x_c x_o)}{\alpha x_o} \tag{5.57}$$

$$C_p = \frac{-D_p}{R_c x_o} \tag{5.58}$$

$$D_p = \pm \sqrt{\frac{\alpha \beta_{co} R_c x_o^2}{R_{opt,p} (\beta_{co}^2 + (\beta_{co} x_c + \alpha x_o)^2)}} \tag{5.59}$$

Once, all the ABCD parameters are obtained from (5.51)-(5.59), the intrinsic voltages (V_c, V_p) and currents (I_c, I_p) can be expressed in the matrix form as,

$$\begin{bmatrix} V_c \\ I_c \end{bmatrix} = \begin{bmatrix} A_c & jB_c \\ jC_c & D_c \end{bmatrix} \begin{bmatrix} Z_{comb}(I_{ct} + I_{pt}) \\ I_{ct} \end{bmatrix} \tag{5.60}$$

$$\begin{bmatrix} V_p \\ I_p \end{bmatrix} = \begin{bmatrix} A_p & jB_p \\ jC_p & D_p \end{bmatrix} \begin{bmatrix} Z_{comb}(I_{ct} + I_{pt}) \\ I_{pt} \end{bmatrix} \tag{5.61}$$

From (5.60) and (5.61), the combining currents (I_{ct}, I_{pt}) can be derived and expressed as follows-

$$I_{ct} = \frac{I_c(D_p + jC_pZ_{comb}) - jI_pC_cZ_{comb}}{D_cD_p + jZ_{comb}(C_cD_p + C_pD_c)} \tag{5.62}$$

$$I_{pt} = \frac{I_p(D_c + jC_cZ_{comb}) - jI_cC_pZ_{comb}}{D_cD_p + jZ_{comb}(C_cD_p + C_pD_c)} \tag{5.63}$$

The intrinsic voltages can be found from below expressions after calculating I_{ct} and I_{pt} from (5.62) and (5.63)-

$$V_c = A_cZ_{comb}(I_{ct} + I_{pt}) + jB_cI_{ct} \tag{5.64}$$

$$V_p = A_pZ_{comb}(I_{ct} + I_{pt}) + jB_pI_{pt} \tag{5.65}$$

Please note that, C_c and D_p can either have +ve or -ve root from (5.53) and (5.59), and depending on that, four different combination of carrier and peaking OMNs possible. Also, the roots of C_c and D_p dictate whether the OMN will be low pass (LP) type (-ve insertion phase) or high pass (HP) type (+ve insertion phase) networks. In order to make sure that the currents are combined in phase at the combining load, it's important to know the phase difference between the current generator currents ($\Delta\theta = \theta_p - \theta_c$) and that can be evaluated from ABCD parameters from (5.66). For proper output combining, this phase difference needs to be counteracted by introducing additional phase to either of the amplifier's input. The required phase adjustment

Table 5.3

Types of OMN Combination and Required Adjustment of Phase from the Input

Type	Root of C_c	Root of D_p	Adjusted phase when, $x_c \geq 0$	Adjusted Phase when, $x_c < 0$	Applied to
I	+ve (LP)	+ve (HP)	$\|\Delta\theta\| - \pi$	$-\|\Delta\theta\|$	Peaking IN
II	+ve (LP)	-ve (LP)	$-\|\Delta\theta\|$	$\|\Delta\theta\| - \pi$	Carrier IN
III	-ve (HP)	-ve (LP)	-$\|\Delta\theta\| - \pi$	$\|\Delta\theta\| - 2\pi$	Carrier IN
IV	-ve (HP)	+ve (HP)	$-\|\Delta\theta\|$	$\|\Delta\theta\| - \pi$	Carrier IN

depends on the combination of the matching networks and the sign of x_c (see (5.66)). Considering the fact that, most often an input offset transmission line is utilized for phase adjustment which has a -ve insertion phase, the correct phase for each combination of matching networks is summarized in Table 5.3. It can be noticed that only for type I combination, phase adjustment is expected from the peaking input. For remaining three type of OMNs, the adjustment is expected from the carrier input. In an ideal scenario, any of the combination of OMN networks should produce the same results for a target OBO_{ex} as long as the relationship between x_o and x_c is maintained as established in section 5.2. However, in practical matching circuit design, PA designer may prefer one solution or the other depending on the ease of implementation and losses incurred by the matching networks.

$$\Delta\theta = tan^{-1}\left(\frac{\beta_{co}R_c(D_cC_p - \alpha D_pC_c)}{\alpha D_pC_c - \beta_{co}R_c(x_c(\alpha D_pC_c + D_cC_p) - \beta_{co}R_cC_pC_c(1 + x_c^2))}\right) \tag{5.66}$$

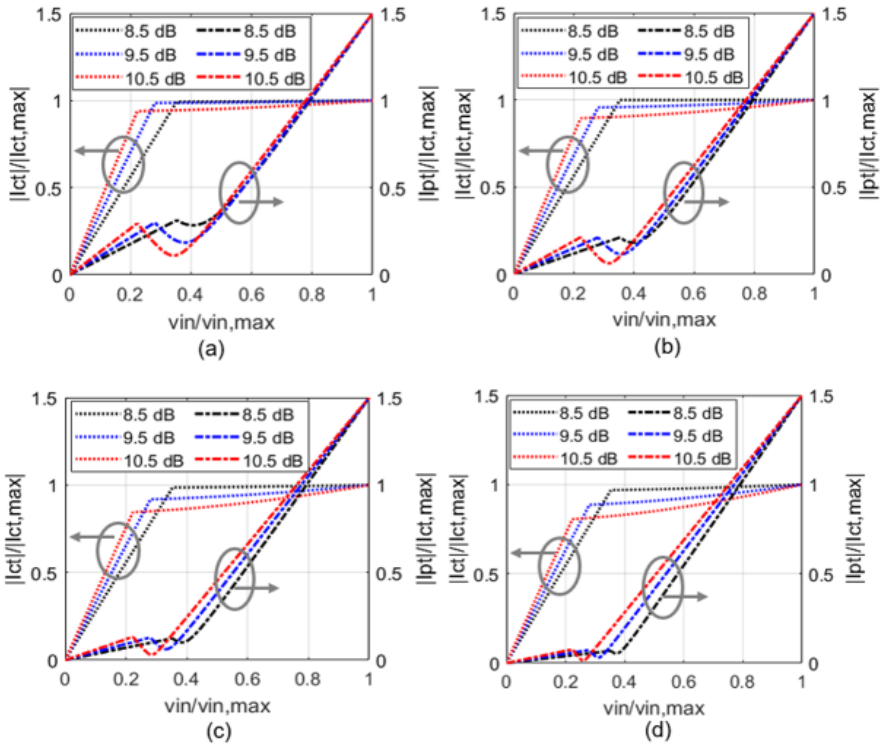

Figure 5.5: Combining currents (I_{ct} and I_{pt}) plots obtained from analysis for (a) $|x_o| = 3$, (b) $|x_o| = 4.5$, (c) $|x_o| = 8$, and (d) $|x_o| = 15$ when, for each cases $OBO_{ex} = 8.5, 9.5$ and $10.5\ dB$.

$$I_c = \frac{I_{c,max}}{2v_{in}} e^{j\theta_c} \tag{5.67}$$

$$I_p = \begin{cases} 0, & \text{if } v_{in} \leq \dfrac{1}{\beta_{ex}} \\ \dfrac{\alpha I_{c,max}(v_{in} - \frac{1}{\beta_{ex}})}{2(1 - \frac{1}{\beta_{ex}})} e^{j\theta_p}, & \text{if } v_{in} > \dfrac{1}{\beta_{ex}} \end{cases} \tag{5.68}$$

All the required combiner parameters to evaluate the performance of COCL Doherty from theoretical analysis have been determined by now. Assuming class-B operation, the current generator (I_c and I_p) can be expressed as linearly varying currents with normalized input voltage, v_{in} in (5.67) and (5.68). Utilizing these expressions, combining currents are calculated for different values of $|x_o|$ ($|x_o|$=3, 4.5, 8 and 15) when $\alpha = 1.5$ and OBO_{ex} is 8.5, 9.5 and 10.5 dB. Calculated currents are plotted in Figure 5.5. Difference in peaking combining current ($|I_{pt}|$) off-state

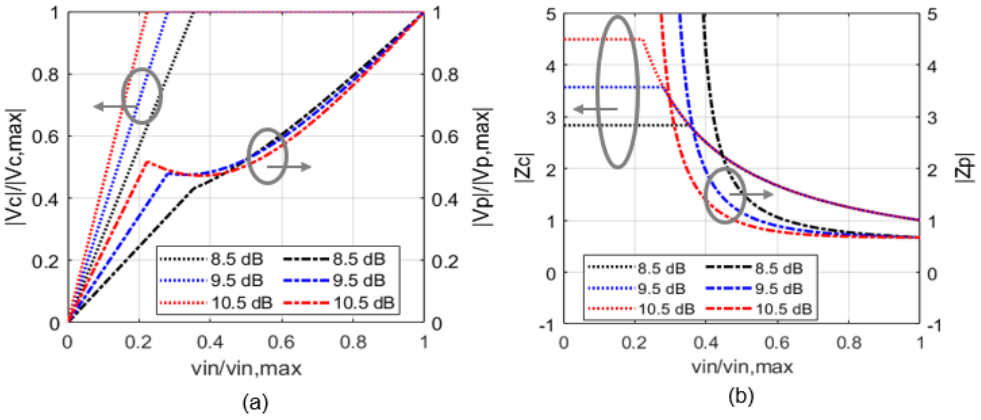

Figure 5.6: (a) Intrinsic voltage (V_c and V_p) and (b) load impedances (Z_c and Z_p) plots obtained from analysis when $OBO_{ex} = 8.5, 9.5$ and $10.5\ dB$.

behavior can be observed from Figure 5.5 for different values of $|x_o|$. As $|x_o|$ goes up, peaking PA introduces less loading effect on the combining load resulting in smaller current at off-state condition and vice versa. Moreover, one can notice from Figure 5.5 that peaking PA turns on sooner as OBO_{ex} goes up. At full power condition, $|I_{pt}|$ is ($\alpha = 1.5$) times $|I_{ct}|$, regardless of $|x_o|$ and OBO_{ex} combination.For different values of $|x_o|$ ($|x_o|$=3, 4.5, 8 and 15), $|V_c|$ and $|V_p|$ are calculated from (5.64) and (5.65) and $|Z_c|$ and $Z_p|$ are calculated using (5.67) and (5.68). Normalized $|V_c|$, and $|V_p|$ are plotted in Figure 5.6(a) and $|Z_c|$ and $|Z_p|$ are plotted in Figure 5.6 (b). Regardless of the $|x_o|$ values, same voltage and load impedance characteristics are obtained from calculation. Carrier PA reaches full voltage swing at OBO when peaking PA starts turning on and stays at maximum voltage till saturation ($v_{in}/v_{in,max} = 1$). Since, I_{ct} and I_{pt} are known, load voltage V_t and output power can be easily calculated for different OBO conditions.

Assuming, class-B DC power consumption, efficiency is calculated and plotted in Figure 5.7. It can be noticed that without sacrificing any peak power, proposed COCL DPA can extend the efficiency range beyond 7.96 dB OBO produced by the

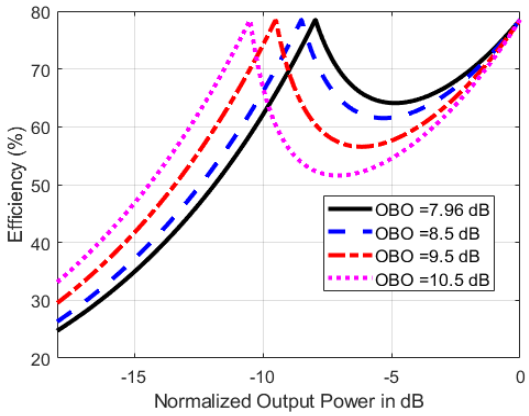

Figure 5.7: Calculated efficiency plot for proposed COCL DPA when $\alpha = 1.5$

conventional approach.

5.3 Design and Simulation Results

To validate the COCL theory and to provide useful design guideline, an asymmetric two-way DPA with commercially available GaN devices was designed. For the carrier device, CGH40006S and for the peaking device, CGH40010F were selected. All the simulations for this design were run in Keysight ADS. Load-pull simulations were carried out on vendor provided large signal model to determine the power capabilities of the two devices. For simulation, carrier amplifier (CGH40006S) is biased at class-AB with gate voltage of -3.2 V and peaking amplifier (CGH40010F) is biased at class C with gate voltage of -5.8 V. The drain supply voltages for both the devices were set at 28 V. With the aforementioned bias conditions, the saturated power of CGH40006S and CGH40010F were found as 10.6 W and 15.85 W respectively-which translates to a peak power ratio, α of about 1.5. The optimal load resistance values $R_{opt,c}$ and $R_{opt,p}$ were estimated from load-pull data as 50Ω and 33Ω respectively. With a conventional combining approach, this carrier and peaking pair can only achieve 7.96 dB of OBO. To extend the OBO range using the proposed approach, a target

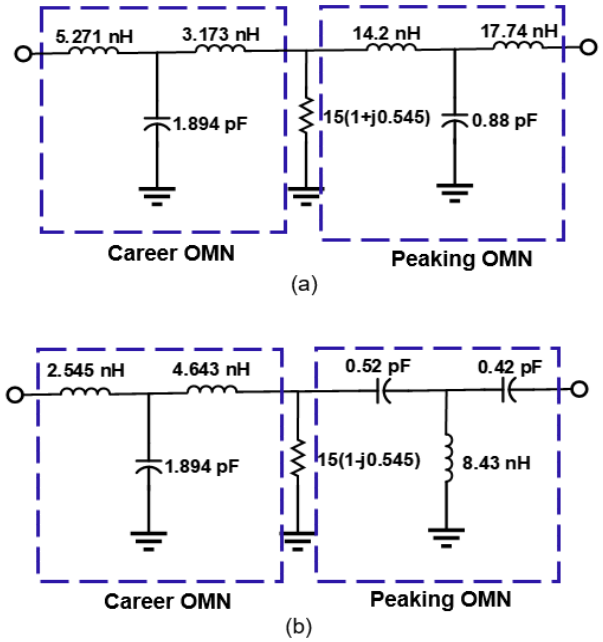

Figure 5.8: Example lumped component based ideal COCL Doherty combiner, when (a) $x_o = 4.5$, and (b) $x_o = -4.5$

OBO_{ex} of 9.5 dB is selected. In order to demonstrate the flexibility of the proposed COCL theory to accommodate multiple frequencies, 1.7-2 GHz was selected as the target frequency range with a fractional bandwidth (FBW) target of $> 15\%$. All the discussions in the prior theory section related to $\alpha = 1.5$ and $OBO_{ex} = 9.5$ dB are relevant for this proof-of-concept Doherty design.

To simplify the design process, a methodology to design lumped component based ideal COCL DPA combiner for two design spaces at center frequency 1.85 GHz is presented in the following. Followed by that, carrier and peaking devices' package parasitics are introduced and lumped matching components are recalculated based on the modified ABCD parameters. The modified networks should provide useful guidelines for the prototype distributed element based Doherty circuit design.

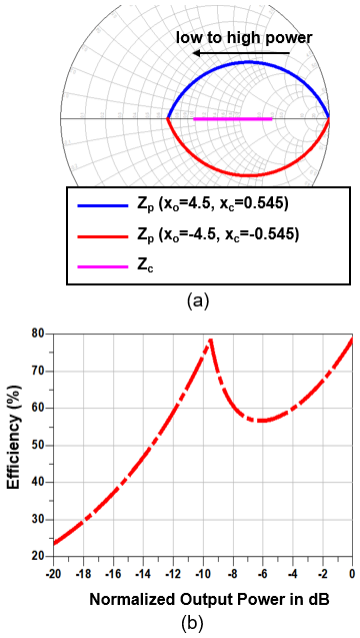

Figure 5.9: Simulation results of ideal COCL combiners of Figure 5.8. Simulated (a) impedance trajectories, and (b) efficiency

Table 5.4

Calculated ABCD Parameters for Ideal COCL DPA Combiner

$x_o = 4.5,\ x_c = 0.545$							
A_c	B_c	C_c	D_c	A_p	B_p	C_p	D_p
-0.35	48.40	0.022	0.188	-1.10	23.53	0.01	-0.69
$x_o = -4.5,\ x_c = -0.545$							
A_c	B_c	C_c	D_c	A_p	B_p	C_p	D_p
0.35	48.40	0.022	-0.188	-1.10	-23.53	-0.01	-0.69

Ideal COCL DPA combiner design

In this section, an ideal COCL combiner design procedure based on the ABCD parameters will be discussed. For, $\alpha = 1.5$ and target OBO_{ex} of 9.5 dB, it was shown in Figure 5.4 from section 5.2 that there exists two COCL design spaces in the inductive and capacitive regions of the smith chart. Either of those spaces can be targeted for combiner design. In addition, as it was discussed in section 5.2, four different combi-

nations of OMNs possible depending on the roots of C_c and D_p. Moreover, matching networks can be synthesized either in T type or π type formations from calculated ABCD parameters [29]. This makes the total options for OMN combination to be sixteen for a pair of x_o and x_c values. Since LP type topologies are predominantly used for matching network designs in practical application, Type II combination is selected for this design. x_o is chosen as ± 4.5 from around the center of Γ_{off} from Figure 5.4 (a) and (b). When, $x_o = \pm 4.5$ the primary solutions for x_c can be found from (5.33)-(5.34) as ± 0.5447. For, $R_c = 15\ \Omega$, $R_{opt,c} = 50\ \Omega$, and $R_{opt,p} = 33\ \Omega$, R_t and x_t are calculated at first from (5.27) and (5.28) and next all the ABCD parameters are calculated from (5.51)-(5.59). Table 5.4 summarizes the calculated ABCD parameters for these two design spaces. Based on the calculated ABCD parameters, lumped component based T-type matching networks were synthesized at 1.85 GHz for both carrier and peaking amplifiers. The resulting lumped-component based realizations can be found in Figure 5.8. For the simulations, ideal voltage controlled current source is utilized from Keysight ADS and for phase compensation, calculated phase adjustments from table II for type II combination ($-55.29°$ for Figure 5.8(a) and $-124.711°$ for Figure 5.8(b)) are applied to carrier inputs.

The simulation results of the ideal combiners are presented in Figure 5.9. The peaking amplifier's impedance trajectory (Z_p) follows the inductive path (blue line in Figure 5.9(a)) for the combiner with inductive load. This trend is opposite (red line in Figure 5.8(a)) for the combiner with capacitive load. However, in both cases, carrier amplifier's trajectory stays the same (pink line in Figure 5.9 (a)) and always stays on the resistance axis of the smith chart from low power to high power transition. The simulated efficiency results are plotted in Figure 5.9(b). Irrespective of the combiner topologies, the simulated efficiency performance remains the same. Two efficiency peaks at peak power and 9.5 dB OBO is achieved with peak efficiency value 78.4%.

Table 5.5

Modified ABCD Parameters after Incorporating Carrier and Peaking Parasitic Networks

$x_o = 4.5$, $x_c = 0.545$							
A_c	B_c	C_c	D_c	A_p	B_p	C_p	D_p
-0.16	43.32	0.0256	0.7	-0.94	25.508	0.0312	-0.22
$x_o = -4.5$, $x_c = -0.545$							
A_c	B_c	C_c	D_c	A_p	B_p	C_p	D_p
0.4865	46.126	0.018	0.325	-1.065	-17.35	0.0114	-1.12

These results are exactly similar to the results achieved from direct mathematical analysis in Figure 5.7 and hence validates the proposed theory.

Incorporating parasitics and modified combiner

Since the carrier and peaking devices for this design are both packaged devices, package parasitic components introduced by the wire and package itself influences the matching network designs [39]. In addition, device drain-source capacitances are always present at the output of the transistors. For better estimation of real matching networks, incorporating the network formed by these parasitic components in the combiner is essential. After they are incorporated, ABCD parameters are re-calculated and based on them the lumped OMN components are re-synthesized. If the ABCD parameters of the modified OMN is defined as, $[ABCD]_{mod}$ and the ABCD parameters of the package parasitic networks and the ideal case ABCD parameters without any parasitics-calculated above are defined as $[ABCD]_{par}$ and $[ABCD]_{ideal}$ respectively, then they are related to each other by following expression-

$$[ABCD]_{mod} = [ABCD]_{par}^{-1}[ABCD]_{ideal} \tag{5.69}$$

Figure 5.10 shows the parasitic network of both carrier and peaking devices. Af-

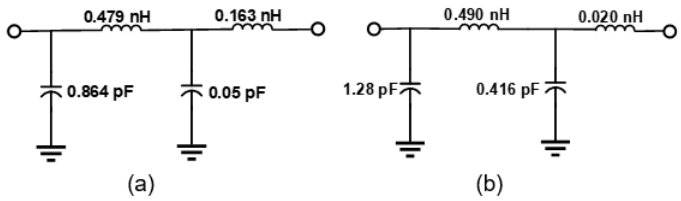

Figure 5.10: (a) Carrier (CGH40006S) parasitic network (b) Peaking (CGH40010F) parasitic network

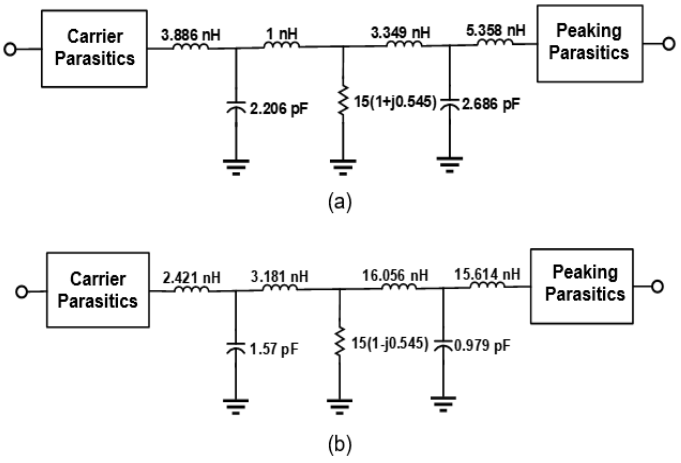

Figure 5.11: Modified combiner of (a) Figure 5.8 (a), and (b) Figure 5.8(b) after incorporating the parasitic networks from Figure 5.10

ter finding the $[ABCD]_{par}$ matrix of both the carrier and peaking devices, modified network parameters ($[ABCD]_{mod}$) can be calculated from (5.69). Table 5.5 summarizes the calculated modified ABCD parameters after the parasitics are incorporated. Based on the modified ABCD parameters, lumped component based T-match networks for both carrier and peaking amplifiers were re-synthesized. The new OMNs along with the parasitic components are presented in Figure 5.11.

For distributed network transformation, lumped series elements are replaced by series transmission lines. It can be observed that the combiner with capacitive load (Figure 5.11(b)) has very high series inductance values on the peaking side. In distributed network transfer, very high series inductance values would translate to transmission lines that have very high characteristic impedance e.g. too narrow and/or are

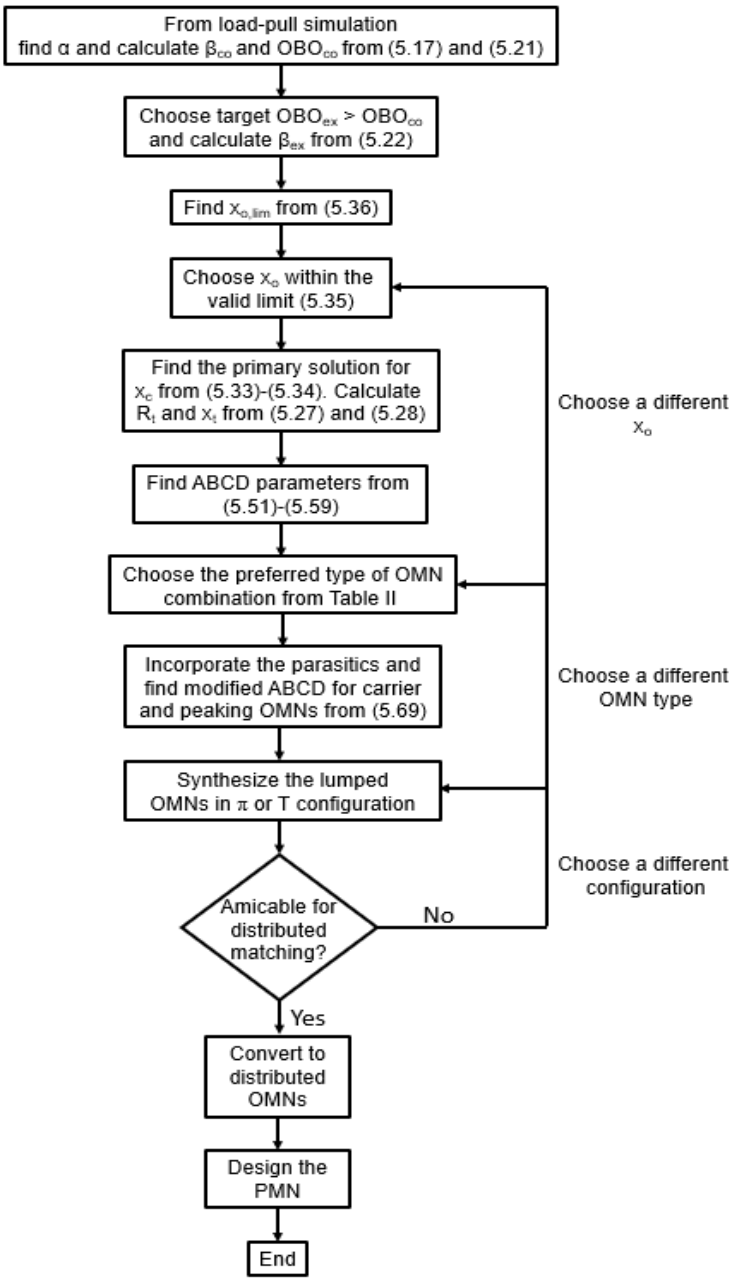

Figure 5.12: Design flow chart

very long ([50], [58]). Practically both of these conditions are challenging to realize in printed circuit boards (PCBs). Thus the first combiner solution (Figure 5.11(a)) with inductive load or in more general terms, inductive COCL design space should be a preferred choice for this prototype Doherty implementation. The summary of

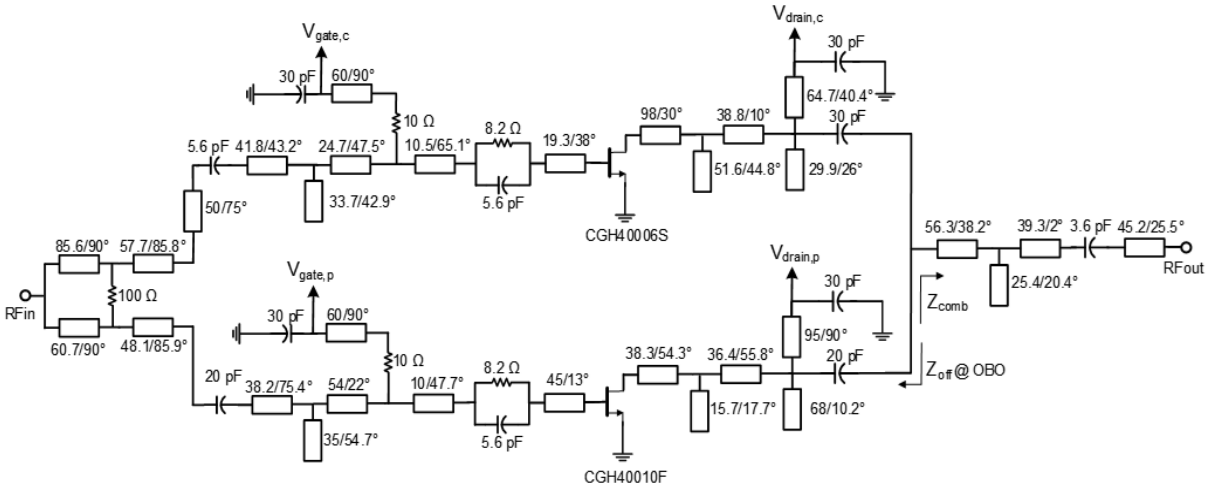

Figure 5.13: Full schematic of the prototype COCL Doherty

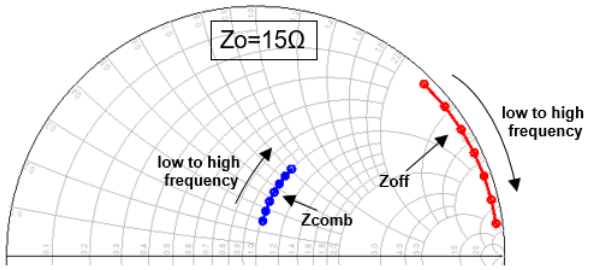

Figure 5.14: Simulated Z_{off} and Z_{comb} trajectories on smith chart for 1.7-2 GHz

COCL Doherty combiner design procedure is illustrated by a design flow chart in Figure 5.12.

Prototype Doherty design

The full schematic of the designed prototype Doherty circuit is portrayed in Figure 5.13. Source-pull simulations were run at first for class-AB biased carrier amplifier and class-C biased peaking amplifiers, to find their optimum source impedances. Then the input matching networks (IMNs) were designed for both amplifiers. Unlike symmetric DPAs, as the carrier and peaking amplifiers are different and so do their input impedances, two different IMN designs were required to achieve optimum per-

formance. Multi-section matching networks with a hybrid of stepped-impedance and single stub topology was adopted for both IMNs. This ensured that good matching was obtained across the target frequency band. In order to attain good stability, parallel RC networks along with series resistors on DC bias lines were incorporated into both IMNs.

To split the input power between carrier and peaking amplifiers, an uneven-split Wilkinson splitter was designed. The split ratio for the power delivered from RF input to the peaking path and to the carrier path was chosen as 1.41:1. Following the theory, phase adjustment would have been needed for type II combiner at the carrier input, hence an input offset-line was added between splitter and carrier IMN. In addition to the phase difference between two amplifiers' OMNs, phase offset line was also adjusted to account for the phase difference between two amplifiers' IMNs.

Based on the guidelines achieved from the lumped component based synthesis, the inductive design space is selected for the prototype combiner design. One of the advantages of the COCL combiners-as it was discussed in section 5.2, it provides continuum of off-state and combining load impedances for extended OBO range and therefore, flexibility to accommodate multiple frequency points. From section 5.3, $x_o = 4.5$ was chosen as the normalized off-state impedance at 1.85 GHz. Additional x_o are assigned from Γ_{off} (Figure 5.4 (a)), to other frequencies in 50 MHz steps to cover 1.7-2 GHz range. For the target x_o values, primary solution for x_c is found from (5.33)-(5.34). Z_{comb} and Z_{off} are then calculated from (5.23) and (5.24) with $R_c = 15\Omega$. Lumped component based OMNs from Figure 5.11(a) are then converted to distributed elements based on the procedure discussed in [50]. As there can be numerous choices for making these transformations, some tuning and optimizations were adopted to get the best performance. A post matching network is designed to match 50Ω load impedance to Z_{comb} impedances.

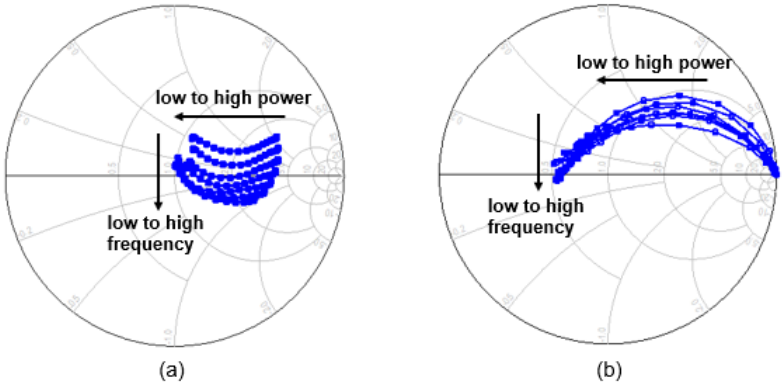

Figure 5.15: Simulated (a) Z_c and (b) Z_p trajectories on prototype Doherty for 1.7-2 GHz

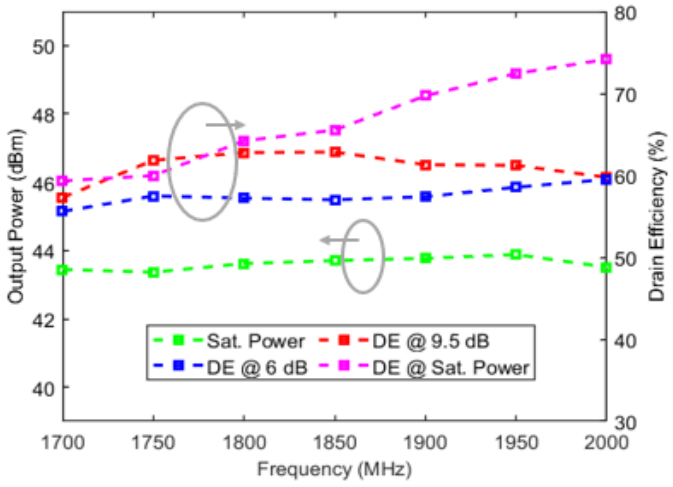

Figure 5.16: Simulated saturated power and efficiency at different power levels versus frequency for the prototype Doherty

Figure 5.14 shows the Z_{off} and Z_{comb} locations on smith chart obtained from simulation. They closely follow the calculations from analysis. In addition to the fundamental matching for proper COCL load modulation, both devices were characterized for optimum second harmonic ($2f_o$) termination at the package plane to achieve best performance. By running second harmonic load-pull simulation, the optimum $2f_o$ loads at the package reference plane for carrier and peaking devices were found as $j100\Omega$ and $j70\Omega$ respectively. Bias lines for both amplifiers were utilized

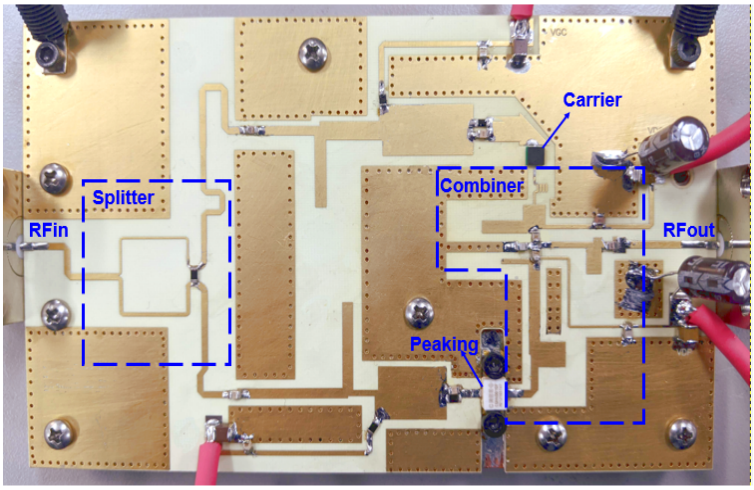

Figure 5.17: Snapshot of fabricated Doherty PCB

to terminate the $2f_o$ impedances at their optimum locations. Carrier and peaking amplifiers' Z_c and Z_p trajectories were monitored during the design process and Figure 5.15 presents their simulated trajectories. Expected load modulation behavior is apparent from these results. Simulated power and drain efficiency (DE) of the COCL Doherty are plotted in Figure 5.16 as a function of frequency. In simulation, the COCL Doherty achieves saturated power from 43.4 to 43.9 dBm, efficiency at 9.5 dB OBO from 57 to 63% and at 6 dB OBO from 55.6 to 59.5 % in 1.7-2 GHz frequency range. The peak efficiency reaches as high as 74 % at 2 GHz.

5.4 Measurement Results

The COCL Doherty prototype was fabricated in a Rogers R04350B ($\epsilon_r = 3.66$) substrate with 20 mils thickness. Before taping out the PCB, input and output networks were EM (Electromagnetic) simulated using Momentum from Keysight ADS. Modelithics cap models were incorporated as well to get good agreement between simulation and measurement results. The overall PCB size was 5 inch in width and 3 inch in height. After manufacturing, the Doherty PCB was mounted on a copper

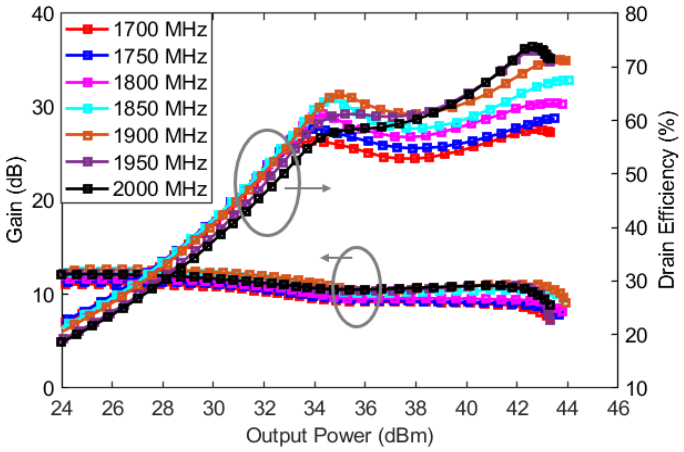

Figure 5.18: Measured efficiency and gain versus output power for CW signal

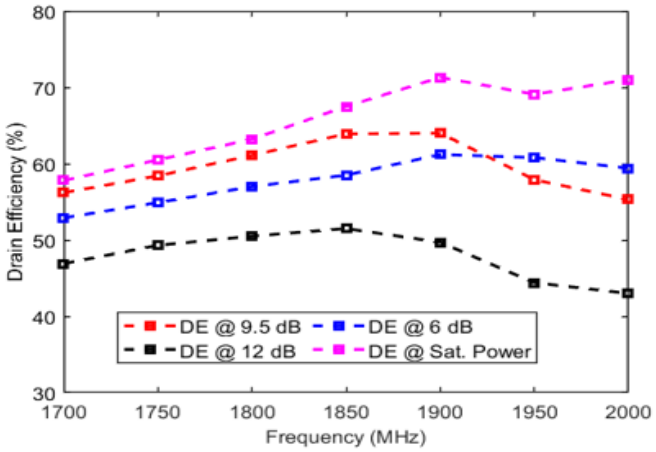

Figure 5.19: Measured drain efficiency for different power levels versus frequency for CW signal

fixture to evaluate it's performance. Figure 5.17 shows the photograph of the prototype Doherty board. For measurement, carrier was biased at class-AB with fixed quiescent current (I_{dq}) of 11 mA while peaking was biased at class-C with bias voltage optimized within ±0.3 V. Both amplifiers' drain supply was set at 28V.

At first, the DPA was measured under continuous-wave (CW) signal from 1.7-2 GHz. Measured efficiency and gain across frequency rage 1.7-2 GHz as a function of output power for CW excitation is plotted in Figure 5.18. Distinguishable extended back-off efficiency range Doherty characteristics with efficiency peaking at output

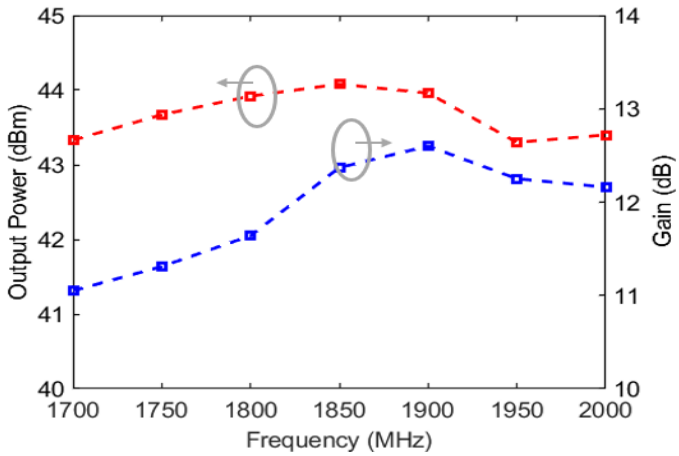

Figure 5.20: Measured saturated power and small signal gain versus frequency for CW signal

back-off of 9.5-10 dB is noticeable from these plots. Efficiency for different output power back-off levels as a function of frequency is plotted in Figure 5.19. For back-off operation, the DPA exhibits efficiency from 53.1% to 61.2% at 6 dB OBO, while at 9.5 dB OBO efficiency is from 55% to 64%. For 100 MHz of center bandwidth (1.8-1.9 GHz) DPA achieves better than 60 % efficiency at 9.5 dB OBO. Up to 12 dB OBO, better than 43% efficiency was achieved by the DPA. With these efficiency performance, the prototype DPA validates the proposed theory for extending the back-off range with good bandwidth performance. At saturated operation, the prototype Doherty achieves 58% to 71% efficiency. These performances are aligned with the results obtained from simulation.

The saturated power and small signal gain performance versus frequency under CW excitation is plotted in Figure 5.20. The saturated power is 43.3 to 44 dBm and the small signal gain is better than 11 dB with gain reaching it's maximum value of 12.6 dB at 1.9 GHz. From these plots, one can deduce that the DPA achieves very consistent saturated power and gain performance across the band with minimal variation.

To evaluate the COCL DPA performance with modulated waveform, it was char-

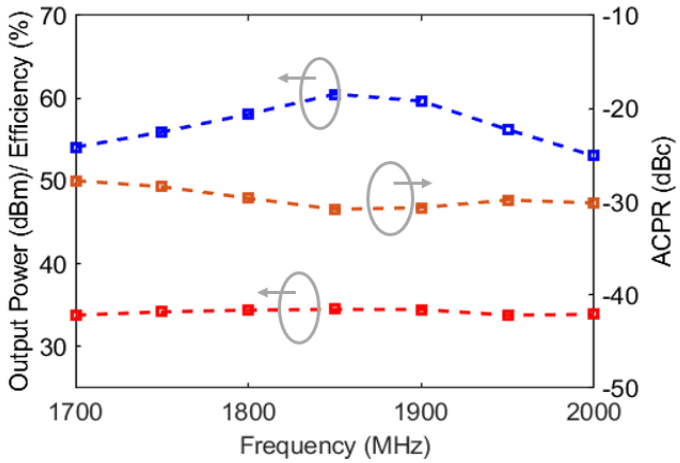

Figure 5.21: Measured average power, efficiency and ACPR for modulated signal

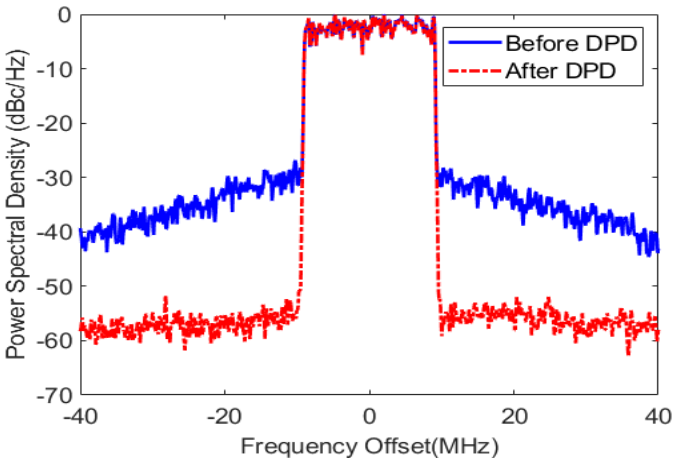

Figure 5.22: Measured power spectral density with modulated signal before and after DPD

acterized under long-term evolution (LTE) 20 MHz signal with 9.6 dB peak-to-average power ratio (PAPR). Measured average efficiency, power and adjacent channel power ratio (ACPR) as a fuction of frequency are plotted in Figure 5.21. The DPA exhibits average power of 33.7-34.4 dBm with average efficiency lies in between 53 to 60% and ACPR of -30.8 to -27.9 dBc. Digital pre-distortion (DPD) technique was employed to assess the linearizability of the DPA. The DPD transceiver has a sampling rate of 737 mega sample per second (MSPS) and the DPD uses generalized memory polynomial based scheme with a relatively low complexity algorithm (polynomial order of 9, 3

Table 5.6

Performance Comparison with State-of-the-Art Extended Back-off Range DPAs

			CW Performance				Modulated Signal Performance				
Ref.	Architecture/ Method	Freq. (GHz)	P_{sat} (dBm)	Gain (dB)	OBO (dB)	DE (%) @ OBO	Signal /BW (MHz)	PAPR (dB)	P_{avg} (dBm)	DE (%) @P_{avg}	ACPR (dBc)
[26]	Symm./NPOI	2.2-2.3	45	11.6-13.5	9	45.1-49.6	LTE/20	8.7	36.3	47.2	-30/-50.3
[27]	Symm./NPOI	3.5	44.9*	13	9	58*	LTE/20	9	35.9	58	NA/-52
[28]	Symm./NPOI	1.9-2.1	42	14	9.5	51-61	WCDMA/5	9.6	32.4	58	-27.4/-46.7
[29]	Symm./NPOI	1.9-2.2	43.8-44.5*	7.5-10.5*	9	47-58*	LTE/20	9	35	55	-24.4/-49
[31]	Symm./CCL	1.4-1.7	41.3-42.5*	12-14	9	50-56	LTE/20	8.5	33.5	51-55	-30/-50
[32]	Symm./CCOP	2.1-2.3	42.5-43.6*	9.8-11.8*	9	40-55*	LTE/20	9	34.6	50.7	-24.8/-50.3
[33]	Symm.(unequal cell)/CCL	1.68	43.5	13.4	9.5	54.7	LTE/10	9.6	34	56.4	-27/-48
[34]	Symm.(unequal cell)/ NPOI+CCOP	3.45-3.75	41.8-43.5	9.5-11.8	8.5	33.3-54.1	LTE/20	8	34.4-36.8	38.9-56.8	-25/-45
This Work	Asymm./ COCL	1.7-2	43.3-44	11-12.6	9.5	55-64	LTE/20	9.6	33.7-34.4	53-60	-30.8/-53.9

*Estimated from plots, NA=Not Available, NPOI=Non-infinity Peaking Off-state Impedance, CCL= Complex Combining Load, CCOP=Current Combining in Out-of-phase

memory taps and total number of DPD coefficients less than 80). The power spectral density of the DPA at 1.85 GHz before and after the DPD correction is presented in Figure 5.22. An ACPR of -53.9 dBc is obtained after DPD correction from the original uncorrected ACPR of -30.8 dBc.

The measured prototype COCL DPA performance was compared with other state-of-the-art extended OBO range DPAs in Table 5.6. The proposed DPA stands out in terms of OBO efficiency, bandwidth and linearity performance. The proposed DPA demonstrates highest efficiency for $\geq$ 8.5 dB OBO level with excellent DPD corrected linearity. Moreover, the DPA shows very consistent and less dispersive power (<1 dB) and back-off efficiency (<10%) variation across the frequency of operation. In addition, even though asymmetric configuration is used with uneven input splitting,

the gain is in par with many of the symmetric configuration.

5.5 Summary

This work presents a novel extended OBO range DPA combining technique that engineers the interaction between peaking off-state impedance and combining load impedance. Based on a closed form relationship established between the off-state impedance and combining load impedance, it is shown that the proposed combiner offers enhanced design flexibility compared to most of the previously published and implemented methods. A step-by-step prototype design approach starting from ABCD parameter calculation to distributed combiner design was detailed in this work. Finally, a prototype asymmetric Doherty for 1.7 GHz to 2 GHz frequency range was designed to validate the theory in measurement. The prototype DPA with CW excitation achieves a saturated output power of 43.3 to 44 dBm with efficiency of 58-71%. The DPA demonstrates excellent extended OBO efficiency of 55-64% at 9.5 dB OBO and $>$ 43% efficiency up to 12 dB OBO under CW signal. With an LTE 20 MHz modulated signal, the prototype DPA achieves 53-60% average efficiency and excellent DPD corrected ACPR of -53.9 dBc.

Chapter 6

CONCLUSION

In this dissertation, four state-of-the-art, high performance RF PAs targeted for future 5G/5G+ base-station applications are presented. In Chapter 2, a detailed mathematical analysis shows that the constant power and efficiency predicted by the ideal CCF operation is not guaranteed in the presence of non-linear C_{ds}. Higher PA performance compared to ideal CCF operation can be achieved through two distinct mechanisms: 1) by active second harmonic injection in $0 < \alpha \leq 1$ range, and 2) by passive second harmonic termination in $-0.875 \leq \alpha \leq -0.625$ range. Overall, the analysis broadens the CCF design space and enables a PA designer to discover high performance ranges for a CCF PA when the C_{ds} does not behave linearly, as typically assumed in an ideal operation.

In Chapter 3, a methodology to realize class-J termination conditions inside a small form-factor 7 mm x 7 mm quad-flat no-leads (QFN) plastic encapsulated package is presented. By utilizing the presented methodology, the GaN-based DPA footprint could be reduced from a typical combiner realization in which the output harmonic trapping network is outside the package and implemented in a PCB. At the same time, the DPA achieves state-of-the-art performance (efficiency of 54%, and 70% at 8 dB OBO and peak power) with excellent linearizability for 3.5 GHz massive MIMO application. In Chapter 4, a novel methodology to realize a C_{ds} absorption based integrated Doherty combiner for any arbitrary carrier and peaking amplifier power ratio is presented. The novel combining approach also takes into account the package parasitic effects for an integrated Doherty implementation in a package. Utilizing the proposed methodology, a 2-stage integrated LDMOS DPA was designed

and fabricated. The fabricated DPA demonstrated superior performance by achieving best-in-class gain and efficiency combination (45-48% PAE and 31.7 dB at 8dB OBO) with good DPD linearizability (<-51.5 dBc). In chapter 5, a novel methodology to extend the OBO efficiency range taking the combined effect of combining load and peaking off-state impedance is presented. Proposed COCL theory, offers wider design space and more flexibility in extended back-off efficiency DPA design compared to previously published methodologies. The added flexibility is proven to be beneficial for extending the operating bandwidth of the DPA. From 1.7-2 GHz, the designed extended-OBO DPA achieves efficiency 55-64 % efficiency under CW excitation and 53-60 % efficiency with LTE signal at 9.5 dB OBO with DPD corrected linearizability of -53.9 dBc.

The conventional DPA architecture is narrowband and requires large area for implementation. In this dissertation, some elegant DPA architectures are proposed that offer improved performance by extending the design space and innovating design techniques to reduce the footprint by in-package integration of harmonic trapping and combiner networks. The detailed mathematical analysis and model presented for non-linearity analysis and extended OBO range architectures with enhanced design flexibility can be instrumental to realizing future PAs for 5G+ wireless infrastructure. Combining continuous mode PA theory, while considering the non-linear parasitic capacitance, with extended OBO range architectures can further improve the DPA performance for future cellular communication networks.

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