Modeling and Simulation of Ionizing Radiation Effects

In

Pipeline Analog to Digital Converters

By

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A Thesis Presented in Partial Fulfillment
Of the Requirements for the Degree
Master of Science

Approved April 2013 by the
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ARIZONA STATE UNIVERSITY

August 2013

ABSTRACT

Low Power, High Speed Analog to Digital Converters continues to remain one of the major building blocks for modern communication systems. Due to continuing trend of the aggressive scaling of the MOS devices, the susceptibility of most of the deep-sub micron CMOS technologies to the ionizing radiation has decreased over the period of time. When electronic circuits fabricated in these CMOS technologies are exposed to ionizing radiations, considerable change in the performance of circuits can be seen over a period of time. The change in the performance can be quantified in terms of decreasing linearity of the circuit which directly relates to the resolution of the circuit. Analog to Digital Converter is one of the most critical blocks of any electronic circuitry sent to space. The degradation in the performance of an Analog to Digital Converter due to radiation effects can jeopardize many research programs related to space. These radiation effects can completely hamper the working of a circuit. This thesis discusses the effects of Ionizing radiation on an 11 bit 325 MSPS pipeline ADC. The ADC is exposed to different doses of radiation and performance is compared.

DEDICATION

To my Family and Friends

ACKNOWLEDGMENTS

I would like to take this opportunity to acknowledge the enthusiastic supervision of Dr. Hugh Barnaby for his constant support and guidance throughout the whole course of research and giving me this opportunity of working on a novel and challenging problem for my thesis. I would also like to extend my sincere gratitude to Garrett Schlenvogt, for helping in creating leakage models for the transistors.

I would also like to thank my committee member, Dr. Bertan Bakkaloglu for his time and effort that helped me fulfill my degree requirements. I express my gratitude to Dr. Esko Mikkola for his immense help and guidance that helped me understand the basics of Ionizing radiation effects on CMOS devices. I am especially grateful to the staff at Ridgetop Group, John Bush, Andrew Levy and Doug Goodman for their support.

I am thankful to all my friends here at Arizona State University - these are those people who made the time worthwhile. I would take this opportunity to thank the design team - Ali Naziri, Sampath Venkatesan at Ridgetop Group for making this tape. The work wouldn’t have been possible without their guidance on implementation and proof-reading. I also want to thank some of my real close friends - Avinash, Jassi, Hiten, Rakesh. They are those few people who share my joy in completing this thesis work. This list cannot be complete without mentioning Shruti Kaushik, I owe her for all the good times and million other things!

Finally I am indebted to my family for their constant encouragement and belief in me and my dreams. Thanking my parents, and brothers, Vasu and Rishab wouldn't do justice to the amount of faith they have shown in me. All I have done in my life, or would do; will be for the sole purpose of making them proud.

TABLE OF CONTENTS

CHAPTER Page

LIST OF TABLES

LIST OF FIGURES

Figure Page

Figure Page

Preface

This thesis aims to explore the effects of ionizing radiation on the performance of a pipeline analog to digital converter (ADC). Chapter 1 describes the basic architecture used for the pipeline. It also includes an explanation of the various blocks used.

Chapter 2 provides an overview of ionizing radiation effects in CMOS devices. Different processes that occur when a CMOS device is exposed to ionizing radiation have been explained. For example, the characteristics of a transistor when it is exposed to different doses of radiation and how this changed characteristic deteriorates the performance of a circuit at macro-level are explained.

Chapter 3 describes the modeling of ionizing radiation effects on a single NMOS transistor. A new model of an NMOS transistor is created when it is subjected to different doses of radiation. Ionizing radiation leads to off state leakage. For transistors used as a switch in a switched capacitor network; this leakage may decrease the accuracy of a circuit.

Chapter 4 presents the radiation-enabled modeling results along with a conclusion for a pipeline ADC. The model captures the circuit response characteristics by incorporating a unique methodology for simulating radiation effects at the transistor level.

Chapter 5 gives the conclusion.

Chapter 1

INTRODUCTION TO PIPELINE ANALOG TO DIGITAL CONVERTERS

Pipeline Analog to Digital Converters are widely used and popular architectures for sampling rates varying from a few mega samples up to 500-600 mega samples. Resolution ranging from eight bits up to sixteen bits can be achieved with this architecture with some amount of initial latency. These features and advantages make this architecture useful for a wide range of applications including digital receivers, CCD imaging, modems, and communication systems, which need high throughput along with high resolution [1, 2].

1.1 Brief Explanation

As the name suggests, the pipeline architecture consists of many ADC's in series. The input signal is processed by the first stage of the pipeline. A coarse ADC is used to quantize the input signal, giving out digital bits hence generating residue voltages. The generated residue voltage of the first stage is given as an input to second ADC in the pipeline. This second ADC quantizes the signal producing more digital bits along with the residue voltage which is given as an input to the next ADC in the pipeline. Hence the signal is propagated in a pipeline [1, 2].

1.2 Architecture of Pipeline Analog to Digital Converter.

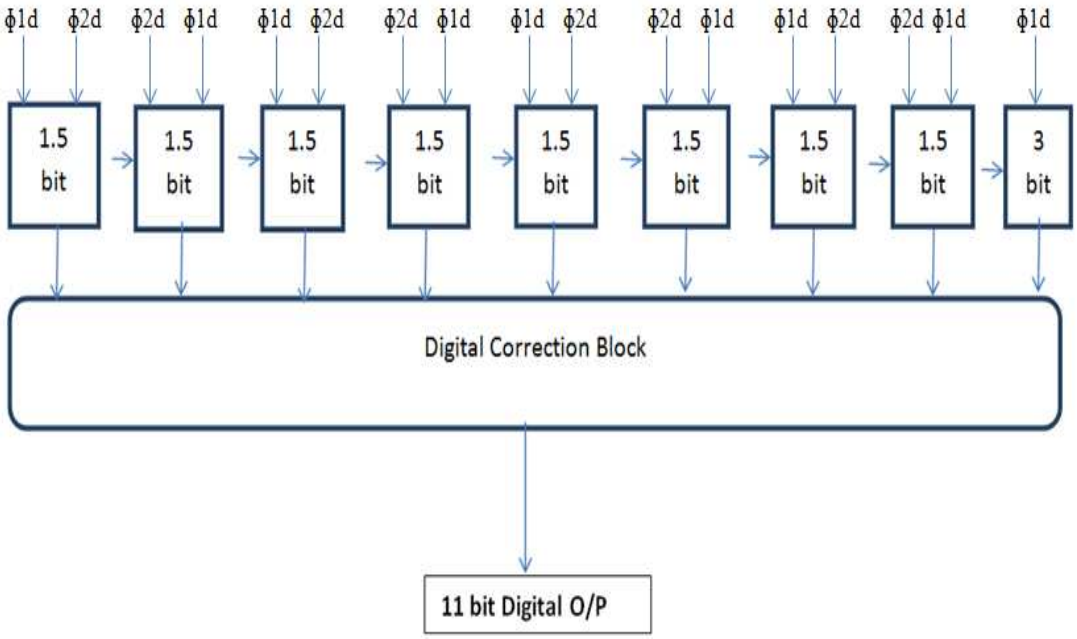

Figure1: ADC Architecture

Figure 1 shows the architecture used for the pipeline ADC. Eight 1.5 bit double sampled gain stages along with a three bit flash stage are used to obtain an eleven bit digital output code. There is some amount of initial latency until the time pipeline is filled up. Once the pipeline is filled, digital codes are obtained on every clock edge hence increasing the throughput.

1.3 System level design considerations and specifications for the ADC

Many factors have to be considered in the system level design of an 11 bit 325 MSPS pipeline ADC. Table 1 shows the specifications for the ADC.

Parameter	Specification
Sampling Speed	162.5 MSPS
Effective Sampling Speed	325 MSPS
Resolution	11 Bits
Input Signal Band width	61 MHZ
Input Signal Swing	1.2 V P-P
Power	140 mW

Table 1: Specifications

Some of the factors include selecting the architecture of the gain stage depending on the latency to be tolerated, power and area specifications. Other factors include choosing the correct operational amplifier (Op-Amp) topology, comparator topology, scaling of the sampling capacitors, number of channels if time interleaved structure is to be used, quantization noise, distortion and sampling frequency.

1.4 General flow of signal in pipeline ADC

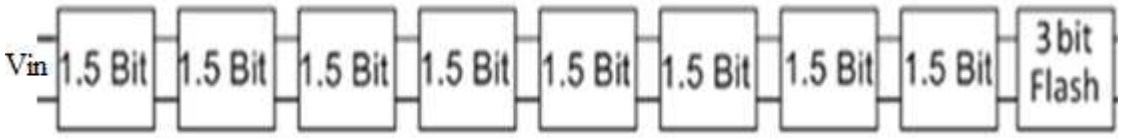

Figure 2: Pipeline architecture showing flow of signal

As the front end sample and hold amplifier is not used for this radiation effects study, an analog input signal is given directly to the first 1.5 bit gain stage. Figure 2 shows the general flow of the signal in the pipeline. The input signal is sampled directly by the sampling network of the first gain stage and at the same time sampled by the comparators. Based on the decision of the comparator, the residue voltage for the next stage is generated by the MDAC (multiplying analog to digital converter) of the first gain stage. The residue voltage (error voltage) generated by the first stage is very small. The second ADC needs to have higher resolution than the previous stage to resolve the input. In order to avoid this problem, we make use of the gain stage to keep the signal level for the second ADC the same. Since we have gained up the residue voltage of the first stage ADC, the second ADC will make the comparison with the same set of reference voltages, eliminating the need of a new set of reference voltage values for each stage. Once we have filled the pipeline, we will have new set of digital codes on every clock cycle. Once, the first ADC in the pipeline quantizes the input signal and generates the residue voltage for the next stage, the previous stage becomes available to process the input signal, hence increasing the throughput. Delay registers have to be used in order to store the data. First 1.5 bit gain stage gives the output code in the first clock cycle whereas last stage of the pipeline gives the digital code after some latency as the signal is propagated through the pipeline. In order to make digital correction logic work, all the digital bits are to be added at the same time, hence delay registers are used before the digital correction logic so that all the digital codes are received at the correction logic at the same time.

1.5 Clocks structure used for the gain stages

A non-overlapping clock structure is used for the gain stages. There needs to be some amount of non-overlapping period in between the sample and hold phase for the switched capacitor network to work. Figure 3 shows the clock waveforms used in the design.

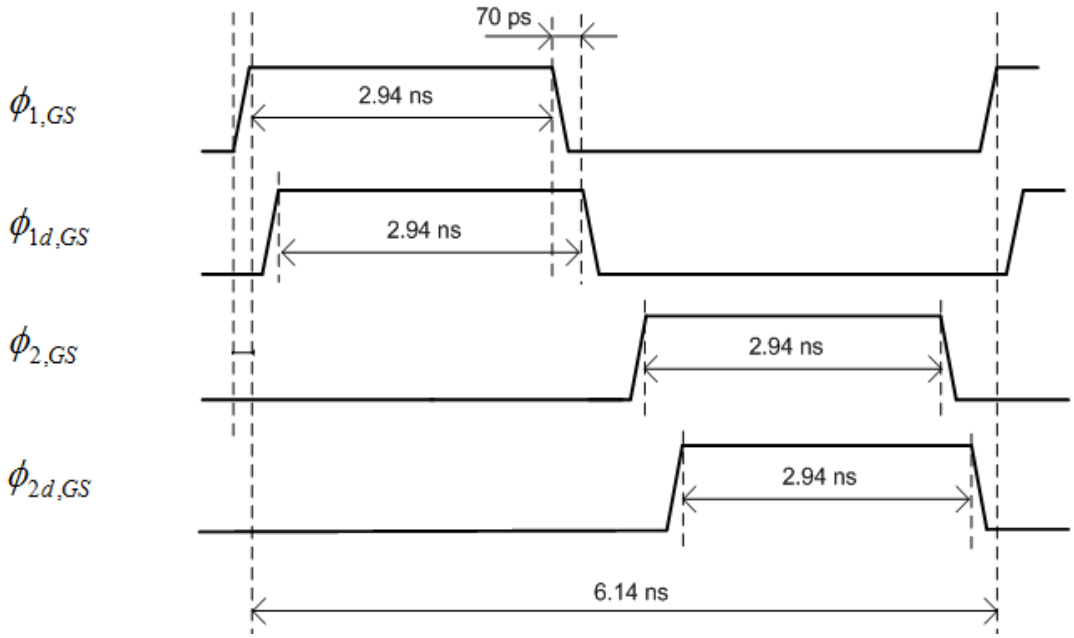

Figure 3: Clock waveforms [5]

Delayed version of Φ1 and Φ2 clocks which are Φ1d and Φ2d are used to make use of bottom plate sampling technique. This technique prevents any charge dumping onto the sampling capacitor when the sampling switch is turned off in the switched capacitor network. Both the phases of the clock are utilized in order to double the sampling frequency.

1.6 Explanation of a Double Sampled 1.5 bit gain stage

The 1.5 bit gain stage is an important block in pipeline analog to digital converter. The double sampling architecture, which makes use of the Op-Amp sharing technique [1], is used in order to effectively double the sampling rate with not much addition in area and power. With a single sampling architecture, the Op-Amp is idle in one phase of the clock. Twice the speed can be achieved by making use of the phase during which an Op-Amp is idle. Table 2 shows the specifications required for a 1.5 bit gain stage.

Parameter	Specification
Power	16 mW
Linearity	11 Bits
Peak – Peak Swing	1.2 V P-P
Switches Used	Transmission Gate
On resistance (T.G)	< 1000 Ohms

Table 2: Specification for the 1.5 bit gain stage

In the case of a single sampling architecture, the op-amp can be reset to remove any parasitic capacitance; whereas in double sampling, we cannot reset the op-amp as it is operating in both clock phases. Double sampling leads to an increase in the number of switches since an additional sampling network must be added. The schematic shown on

Figure 4 is an example of double sampling network. The circuit consists of a differential input and differential output. In the Φ1d phase of the clock, sampling network 1 samples the input signal and holds it. In the same phase (Φ1d) one set of flash ADCs quantizes the input signal into two bits. The two bit digital output with the help of digital logic in Φ2d phase is then used to control the switches of the MDAC stage of sampling network 1 and generates the residue voltage in the Φ2d phase.

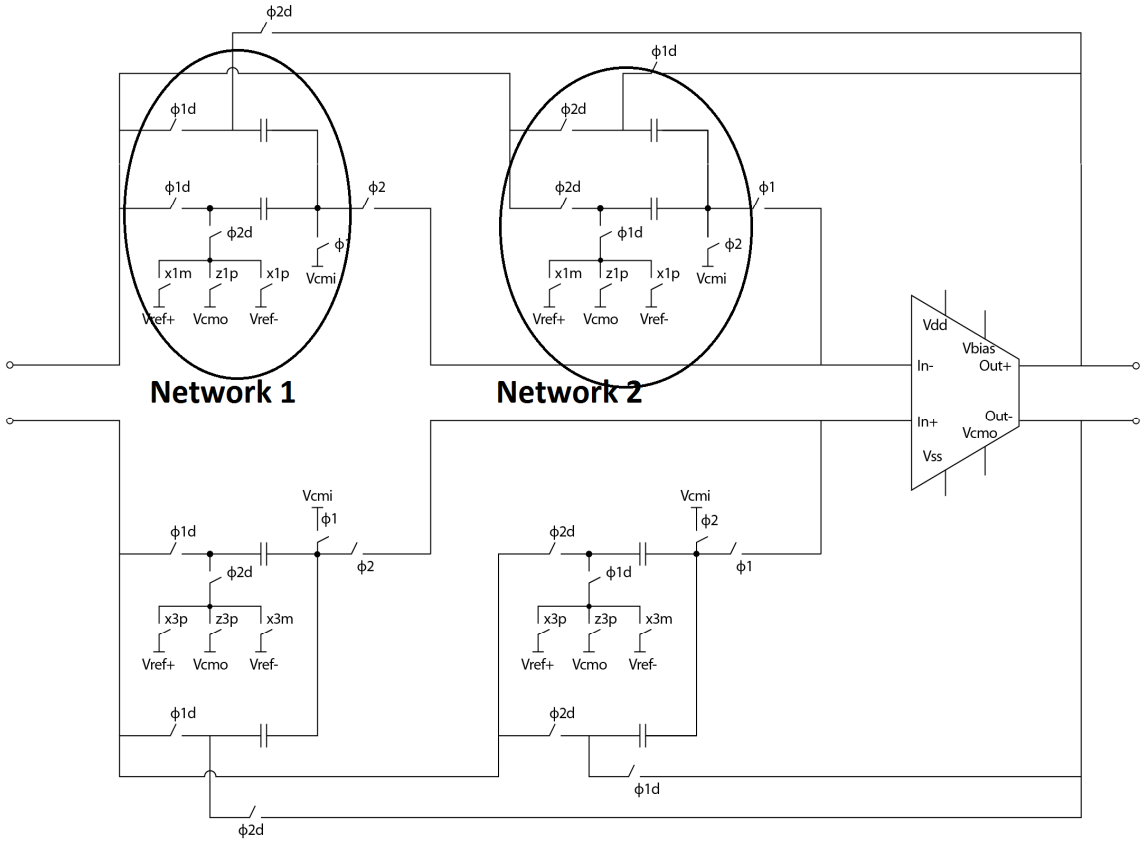

Figure 4 Double Sampled 1.5 Bit Gain Stage [1, 5]

Since we are making use of a double sampling technique, the sampling network 2 samples the input signal in the Φ2d phase and in the same phase the second set of flash ADCs quantizes the signal to two bits. The two bit digital output with the help of digital

logic in Φ1d phase is then used to control the switches of the MDAC stage of sampling network 2 and generates the residue voltage in Φ1d phase. In this way we are getting the residue voltages in both the phases of the clock, which are then sampled by the next double sampled 1.5 bit gain stage. A 1.5 bit gain stage needs an inter-stage gain of two. A switched capacitor circuit making use of two capacitors is an excellent circuit to realize a gain of two.

In one phase of the clock, Vin (input voltage) is sampled onto the sampling capacitors (C1 and C2). The charge stored on to the capacitors is Vin (C1 + C2). In the other phase of the clock, all of the stored charge is transferred on to the feedback capacitor C1. The resulting voltage on C1 in phase □1d forms the output voltage as shown Figure 4.

$$\text{Vin } (C1 + C2) = \text{Vout } (C1) \qquad (1.1)$$

$$\text{Vout/Vin} = (1 + C2/C1) \qquad (1.2)$$

If the value of both the capacitors is kept the same, a gain of two is realized with the help of simple switched capacitor network. The network is used in conjunction with the op-amp in a negative feedback configuration. In order to achieve the required gain, the op-amp has to provide equal and opposite charge to the bottom plate of the feedback capacitor C1. This ”flip around” architecture has many advantages when compared with a charge redistribution network in terms of gain and bandwidth of the op-amp.

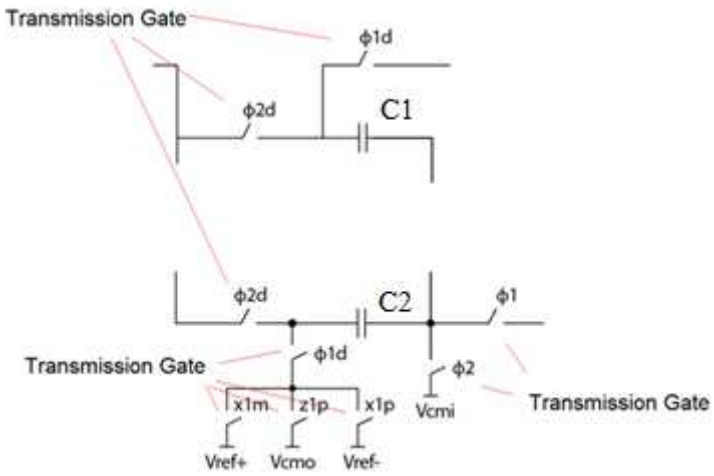

Figure 5: Switched Capacitor network [1]

The linearity of a gain stage depends on many factors. One of the factors is the accuracy of the sample and hold inside each sampling network which in turn depends on the linearity of the switch inside that sample and hold. Other factors are offset of comparators, as well as gain and bandwidth of the amplifiers.

The linearity of the switch in the sample and hold as shown in Figure 5 may be adversely affected by ionizing radiation. It has been observed that with increased ionizing radiation, the standby current (off-state current) of an NMOS transistor (nFET) can increase several orders of magnitude. This effect not only tends to increase the static power consumption but also may degrade the functionality of the circuit. Figure 5 shows the switched capacitor network which uses transmission gate switch. The switch is not able to hold the value at the sampling capacitors due to off-state leakage which comes into effect after ionizing radiation exposure. This leads to the generation of incorrect residue voltages. These errors may be propagated in the whole pipeline hence decreasing the linearity of the ADC. Various mechanisms may be responsible for increased off state

leakage including: 1) leakage between source and drain terminals of an nFET (edge leakage) and 2) leakage underneath the isolation oxides between the drains and/or sources of adjacent nFETs.

1.7 Redundant Signed Digit (RSD) architecture for the 1.5 bit gain stage.

In order to avoid errors due to comparator offset, an RSD architecture [1] is used. In this architecture, the offset requirements of a comparator are relaxed to a great extent. Figure 6 shows the block diagram of the RSD architecurture. This architecture generates two digital bits based on the comparison of the input voltage with a reference voltage. One bit forms the most significant bit (MSB) and the redundant bit is added with a redundant bit of previous stage in the digital error correction logic. In the RSD scheme, the input value is compared with a set of comparators where trip points (VH and VL as shown in the figure) are set at –Vref/4 (VL) and +Vref/4 (VH), where Vref corresponds to the reference voltage used for ADC.

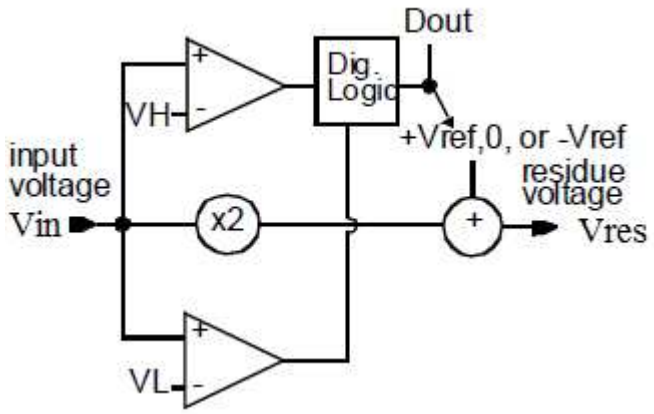

Figure 6: Redundant Signed Digit ADC [4]

The following residue voltages (Vres) are obtained with the help of different operations performed by switched capacitor network based on the comparator decision.

Vres = 2(Vin) + Vref for Vin < -Vref/4 [Digital code obtained - 00] (1.3)

Vres = 2(Vin) for (–Vref/4 < Vin < +Vref/4) [Digital code obtained - 01] (1.4)

Vres = 2(Vin) - Vref for Vin > Vref/4 [Digital code obtained – 10] (1.5)

Figure 6 shows a typical transfer curve for the RSD applicaton.

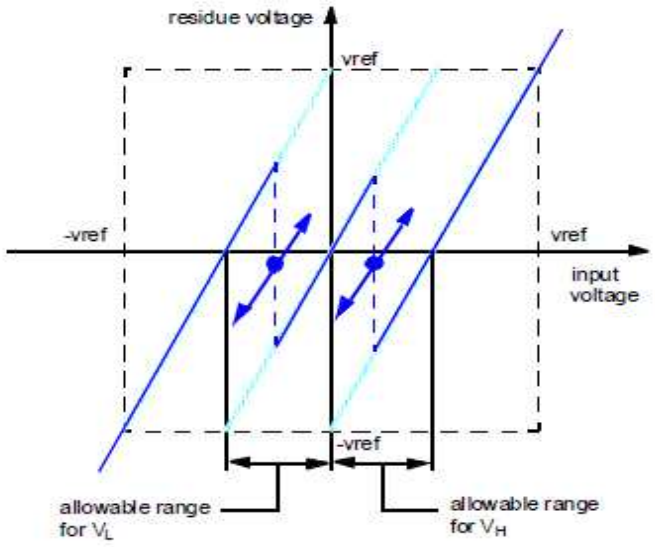

Figure 7: RSD Architecture transfer function [4]

Consider a case where we have small amount of comparator offset, due to comparator offset the trip point of the comparator will change. As long as the comparator offset is within Vref/4 range, the transfer curve would not go outside the range (denoted by the box in Figure 7), hence producing residue voltages within range.

1.8 Operational Amplifier (Op-Amp)

The Op-Amp is an important block in the working of a 1.5 bit gain stage. Figure 8 shows the telescopic cascode topology which is implemented in the gain stage. This topology is chosen as it has a large bandwidth.

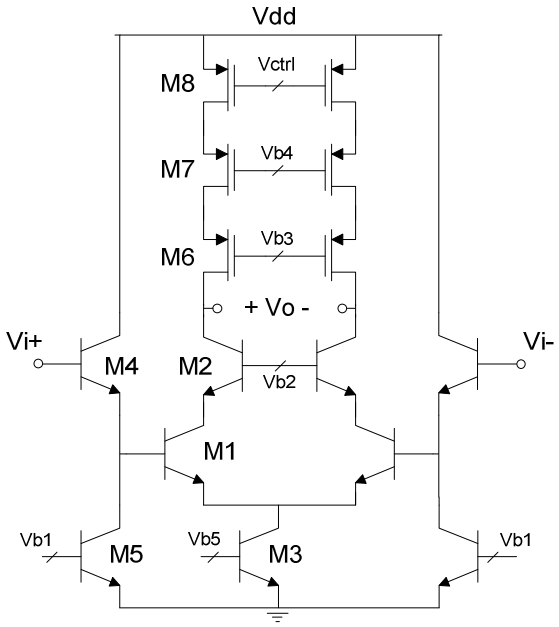

Figure 8: Telescopic cascade Op-amp [3, 5]

High gain of the order of 80 dB is achieved by making use of the cascode structure of PMOS transistors. A pair of Bipolar Junction Transistors (BJTs) is used as an input transistor differential pair because BJTs have higher transconductance and lower noise compared to MOSFETs.

1.9 Three bit flash

A three-bit flash is one of the most popular architectures, which gives a digital output in one clock cycle [1, 2]. It is one of the fastest architecture but the resolution is limited to the maximum of six bits.

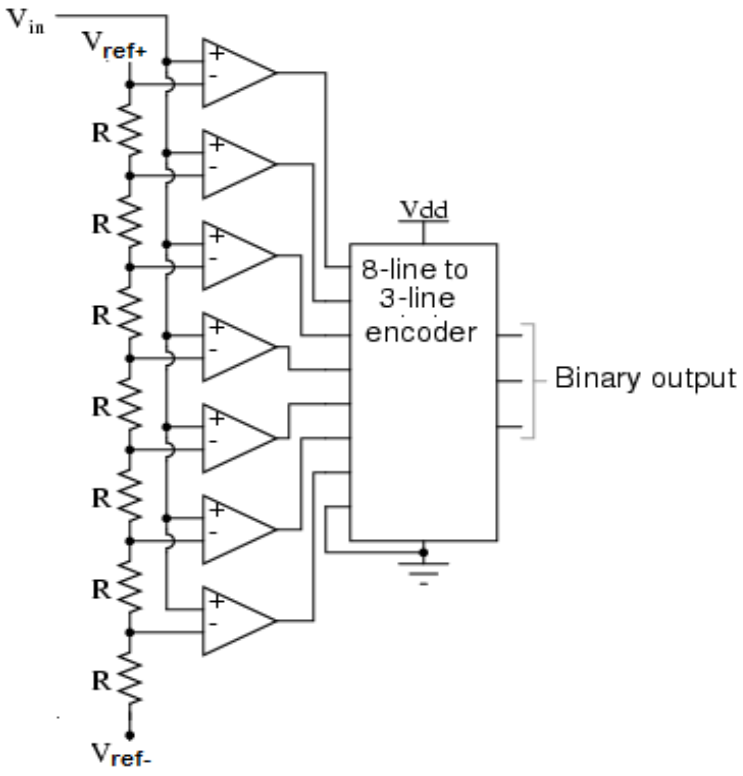

Figure 9: Three bit Flash Architecture [1, 2]

Figure 9 shows a block level diagram of a three bit flash which consists of series network of comparators. It also consists of a resistive ladder network which provides different reference levels to each of the comparator. The input signal is fed to the comparators, comparison is done with different comparison points and the thermometer code is obtained. Eight line to three line encoder is used to obtain three bit digital output code.

This chapter explains the architecture of pipeline ADC used for the simulation of ionizing radiation effects. The effects of the ionizing radiation will be simulated on this pipeline architecture. The ADC will be exposed to different doses of ionizing radiation and degradation (if any) in the performance will be seen.

Chapter 2

Ionizing Radiation Effects in MOS Devices.

2.1 Introduction

Due to the continuing trend of aggressive semi-conductor scaling, the susceptibility of most deep sub-micron technologies to ionizing radiation has reduced. The primary reason for less susceptibility is extreme sensitivity of n-channel and p-channel transistors to ionizing radiation. Several studies conducted at Naval Research Laboratory in 1964 showed that the primary mechanisms responsible for MOSFET performance degradation were the buildup of positive oxide charge [N_{ot}] in the gate oxide region along with the creation of interface traps at Si-SiO_2 interface [6,7,8]. Reduction in gate oxide thickness (t_{ox}) and increase in channel and body doping has played an important role in improving the inherent radiation hardness of most deep sub–micron technologies. As the oxide thickness is scaled, it leads to the reduction of oxide charge trapping in the gate oxides, thus improving the radiation hardness [9]. Increased doping reduces the effect of oxide trapped charge on the channel surface potential, which also increases resistance to ionizing radiation damage.

The degrading effects of ionizing radiation on electronic circuits can be mitigated by using specializing techniques such as Radiation Hardening by Process (RHBP) and Radiation Hardening by Design (RHBD). RHBP has its disadvantages such as low yield, higher manufacturing costs, process instability [10]. Due to these disadvantages RHBD is typically preferred over RHBP. RHBD includes special layout techniques and design

approaches which enables the desired radiation hardness of an electronic circuit to be achieved in some technologies.

2.2 Radiation Effects on MOS devices and Circuits

This chapter primarily discusses Total Ionizing Dose (TID) effects on MOS devices and circuits. It discusses how and increase in the ionizing radiation dose level changes the characteristic of a transistor which may eventually alter the performance of a circuit at macro-level.

2.2.1 Total Ionizing Dose:

Electron-hole pair (ehp) generation through ionizing radiation is the major cause of radiation damage in CMOS devices. The quantity of electron-hole pairs generated is directly proportional to the amount of energy transferred to target material [11]. The energy per unit mass which leads to the generation of electron-hole pairs is defined total ionizing dose. The RAD and GRAY are units which quantify TID. They denote the total amount of energy absorbed per unit mass of the target material. Some minimum amount of energy is required for the process of ionization to occur. Experiments revealed that amount of energy required to create electron hole pairs in SiO_2 is around 17eV +- 3eV [12].

After the generation of the electron- hole pairs, the transport mechanism of these ehps starts within the oxide. A fraction of the ehps generated recombine initially reducing the initial density of the total carriers. As the mobility of electrons is much more than that

of the holes, they are rapidly swept out of the oxide. The mobility of the holes in the oxide is generally of the order of 10^{-4} to 10^{-11} $cm^2 V^{-1}S^{-1}$ whereas the mobility of electrons is of the order of 20 $cm^2V^{-1}s^{-1}$ [13]. Some of the holes that do not recombine slowly travel towards the Si-SiO_2 interface causing long term TID effects.

The processes that occur after the interaction of ionizing radiation with the target material shown in Figure 10 are as follows

- Electron-hole pair (ehps) generation
- Recombination of ehps
- Hole transport
- Hole trapping (oxide trapped charge)

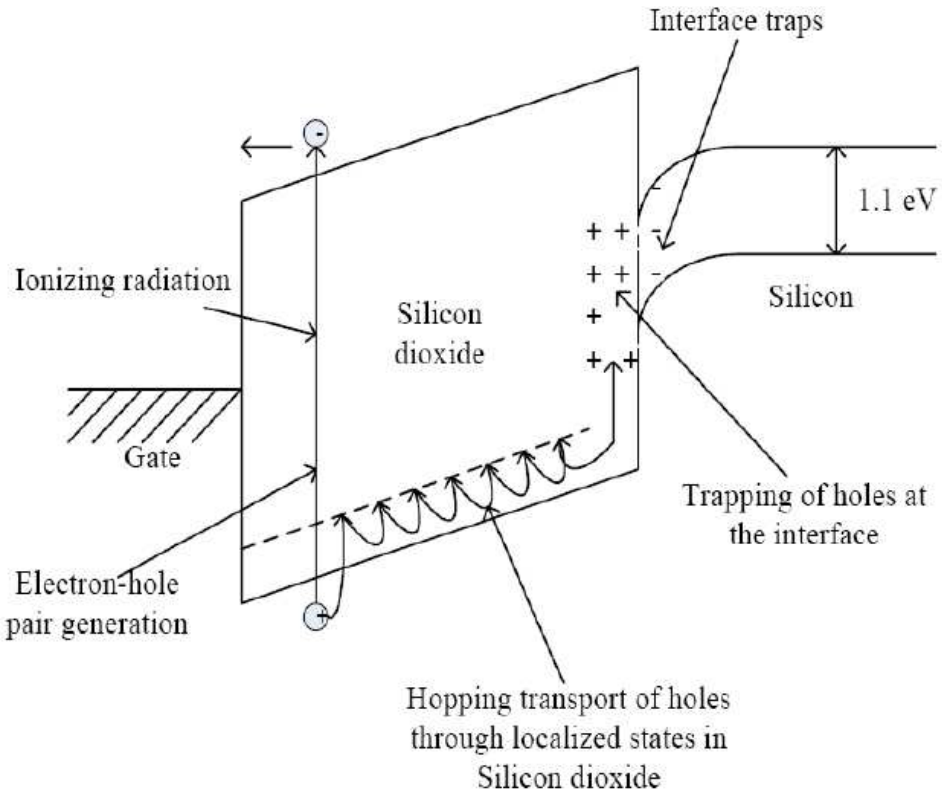

Figure 10 Processes related to the damage of CMOS devices due to TID [14]

2.3.1 Generation of electron-hole pairs:

As mentioned above, the generation of electron hole pairs occurs when ionizing radiation interacts with the solid material. For CMOS device, the most sensitive materials are the dielectrics (e.g., SiO_2) that are in close proximity to an underlying semiconductor. The process of ionization generates ehps as photons or particles pass through dielectric. The amount of the ehp generated is typically expressed in terms linear energy transfer (LET). The unit of LET is MeV-cm^2/g. It is function of particle's mass, energy and density of the target solid. Total ionizing does is proportional to the LET of an ionizing particle.

Total Ionizing Dose (TID) affects lead to the generation of ehps in the target solid material. TID gives the total amount of energy deposited on a target material when it is placed under the effect of ionizing radiation. The SI unit of TID is Gray (Gy). Rad (radiation absorbed dose) is another common unit to quantify TID. One Rad is equal to 100 ergs of ionizing energy deposited per gram of the target material.

$$1 \text{ Rad} = 100 \text{ ergs/gm} = 6.24 * 10^{13} \text{ eV/g [15]} \quad (2.1)$$

2.3.2 Recombination:

Recombination is the process that follows the generation of ehps. After the generation of ehps, some fraction of the pairs recombines. The time available for this recombination process is very small as the electrons which are having very high mobility are very rapidly swept out of the oxide (or other dilectric). Hole yield is the term which is used to denote the density of the holes that escape the initial recombination. Hole yield is

dependent on the type of particle and the applied electric field. Hole yield is different for different types and energies of the incident radiation.

2.3.3 Hole Transport

A fraction of the holes that do not recombine can travel towards the interface of Si-SiO_2 by two major mechanisms. Polaron hopping and multiple trapping are the two processes by which holes can transport to Si-SiO_2 [16, 17]. The positively charged hole can distort the local potential as it moves through the oxide. Polaron hopping is a process that occurs between shallow traps states separated by a very small distance, i.e., less than 1 nm. Figure 11 shows the polaron hopping process that takes place in the oxide.

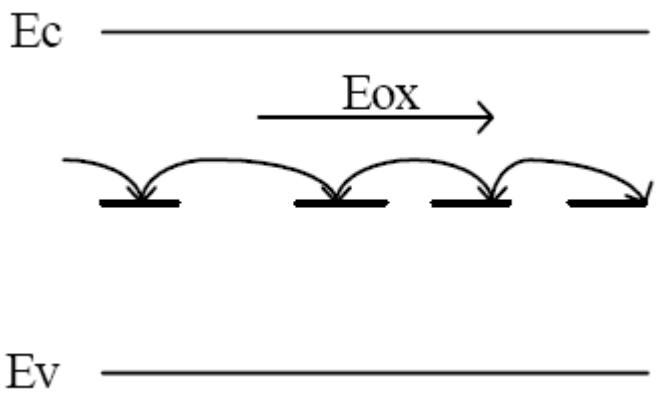

Figure 11 Polaron hopping process due to applied field [18]

In the phenomenon of multiple trapping, the transport of holes is mediated by traps. These processes are found to be highly dispersive in time.

2.3.4 Oxide trapped charge:

Vacancies of oxygen that exist in a SiO_2 layer can trap holes. However it is process and field dependent phenomenon. The total amount of oxide charge formed in the oxide due to hole trapping can be approximated by the equation [19, 20, 21]

$$\Delta N_{ot} = D * K_g * f_y * f_{ot} * t \quad (2.2)$$

where D is the total ionizing dose, K_g is the electron hole pair density for 1 rad of energy deposited in Sio_2, f_y is the hole yield, f_{ot} is the hole trapping efficiency, t_{ox} is the thickness of the oxide. Oxide trapped charge (N_{ot}) can alter the threshold voltage, V_t of a CMOS transistors. Threshold voltage shifts created by N_{ot} is often denoted at ΔV_t and can be approximated as [22]

$$\Delta V_t = (-t_{ox} / \varepsilon_{ox}\, \varepsilon_0) * q * \Delta N_{ot} \quad (2.3)$$

where q is the magnitude of electronic charge, and the product $\varepsilon_{ox}\varepsilon_0$ is the permittivity of SiO_2. As shown in the above equation, positive trapped charge leads to a negative shift in the threshold voltage of both the NMOS and PMOS transistors. For the NMOS transistor the buildup of positive charge increases its off state current. This increase in the off state current affects the functioning of the circuit at macro level. The switched capacitor circuit which makes use of a transmission gate switch (having NMOS and PMOS transistors) forms an integral part of the 1.5 bit gain stages. If the switch starts leaking in the hold phase of the clock due to the buildup of positive charge, we will eventually be sampling wrong value on the sampling capacitor which may lead to wrong generation of residue voltages which will propagate in the whole pipeline, hence deteriorating the performance.

The effect of N_{ot} on the threshold voltage of a PMOS transistor is also a negative shift, which means it leads to an increase in the absolute value of V_t. This leads to less off state current in a PMOS transistor. Figure 12 shows an increase in the off state leakage current of NMOS transistor due to the trapping of positive charge in the gate oxide of a transistor. After irradiation, there is a negative shift (green color) in the characteristics of an NMOS transistor (Figure 12) showing increase in the leakage current for the same gate to source bias

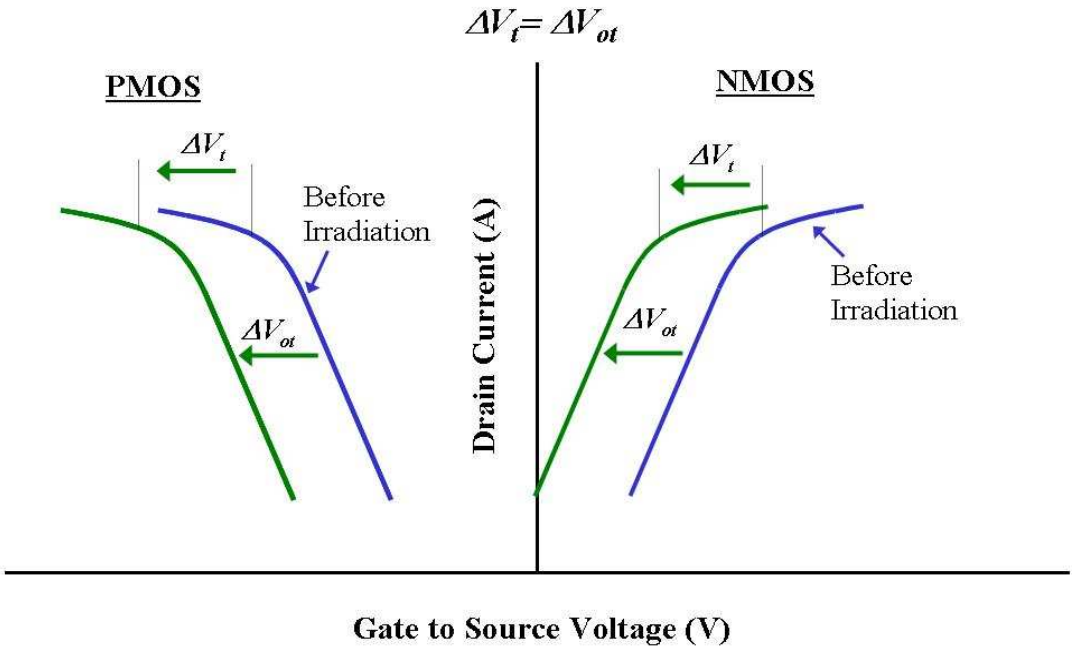

Figure 12: Oxide trapping leading to a change in Id vs Vgs characteristics [22]

From the equations given above, one may observe that the shift in the threshold voltage is directly proportional to the square of the oxide thickness. Thus, as the thickness

of the oxide is reduced, there is a less possibility for the formation of charge at the interface, thus the amount of the V_t shift will be reduced.

2.3.5 Interface traps

The other process that occurs upon exposure to ionizing radiation is the generation of interface traps (N_{it}). These states are formed by the creation of dangling bonds at the interface and this state act as a trap for the free carriers in the underlying semiconductor. Interface traps lead to an increase in the sub-threshold swing of a transistor. The holes generated by the ionizing radiation interact with hydrogen containing defects in the oxide and generate H+ ions [23]. The generated H+ ions can drift to the Si-SiO_2 interface. These protons react and form dangling bonds which are also known as Pb centers. Figure 13 shows an effect on the characteristic of a NMOS and a PMOS transistor due to interface charge trapping. For both NMOS and PMOS transistor, the buildup of Nit typically leads to a decrease in the off-state current of a transistor.

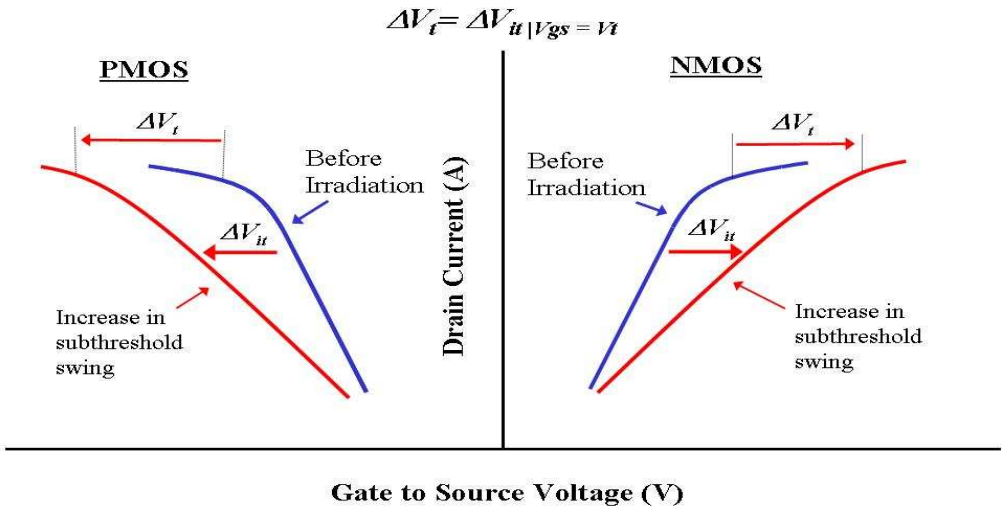

Figure 13 Interface trapping leading to a change in transfer characteristics [22]

2.3.6 Field oxide effects

It has been shown that generation of N_{ot} and N_{it} leads to a change in the characteristics of a transistor. One important change is in the form of V_t-shifts. It has also been found that on thinner oxides, these problems are not as significant as V_t-shifts are proportional to the square of oxide thickness. The thinner the oxide the smaller the V_t-shift. In most of the modern CMOS technologies, the gate oxide thickness scales. Hence the problem of charge trapping in the gate oxides is no longer a matter of great concern in most modern CMOS technologies.

Generally, the isolation field oxides in modern CMOS technologies are much thicker than the gate oxides and majority of the problems associated with the TID effects exist in these thick isolation oxides.

Local oxidation of silicon (LOCOS) and Shallow Trench Isolation (STI) are the commonly used isolation oxide techniques in modern CMOS technologies. STI is the isolation technique used for technologies below 0.3 um.

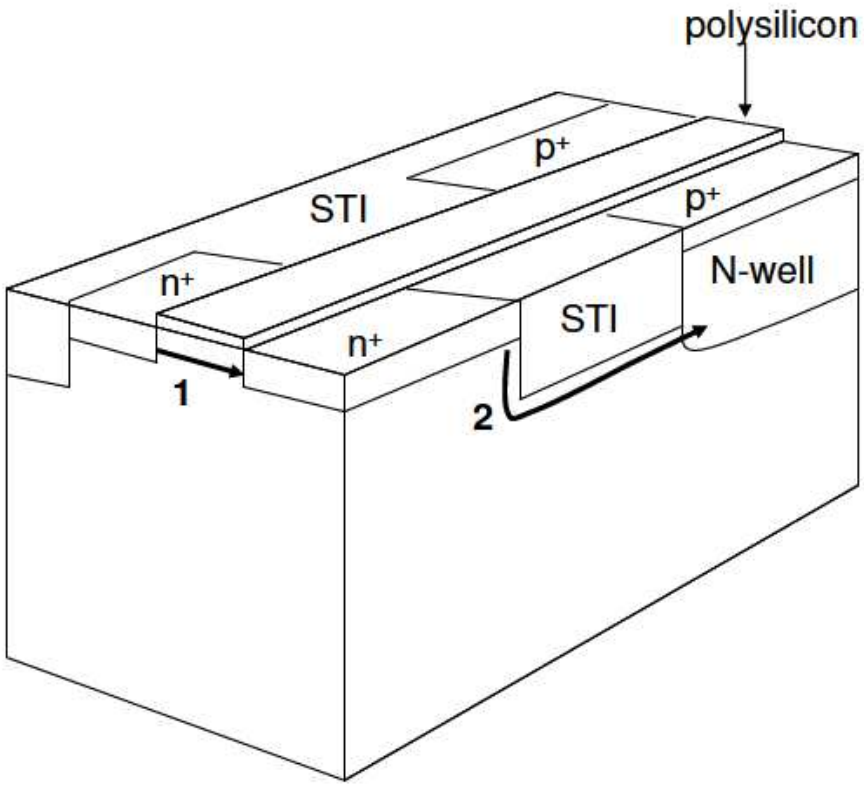

Figure 14 Two leakage paths in STI oxides due to TID effects [24]

Figure 14 shows the two leakage paths formed due to TID effects. Intra device leakage is the leakage which exists between the source and drain terminals of a device (Path 1). It is due to the formation of positive charge at the Si-SiO_2 interface which forms the minor channel for the flow of current between the source and drain of a transistor. The effects due to intra device leakage is observed in NMOS transistors as PMOS transistors do not undergo any change as there edges do not turn on when positive

charge is trapped. The off state leakage becomes severe for TID doses of 300 krad and above.

Device to device leakage also referred to as Inter device leakage is another type of off- leakage caused by the charge trapped in the STI. The leakage paths arise between the source or drain terminal of a NMOS transistor to an adjacent n-well of a PMOS transistor or another NMOS source or drain. Figure 15 shows the different leakage paths formed. It is caused by the formation of positive charge in the bottom of the STI.

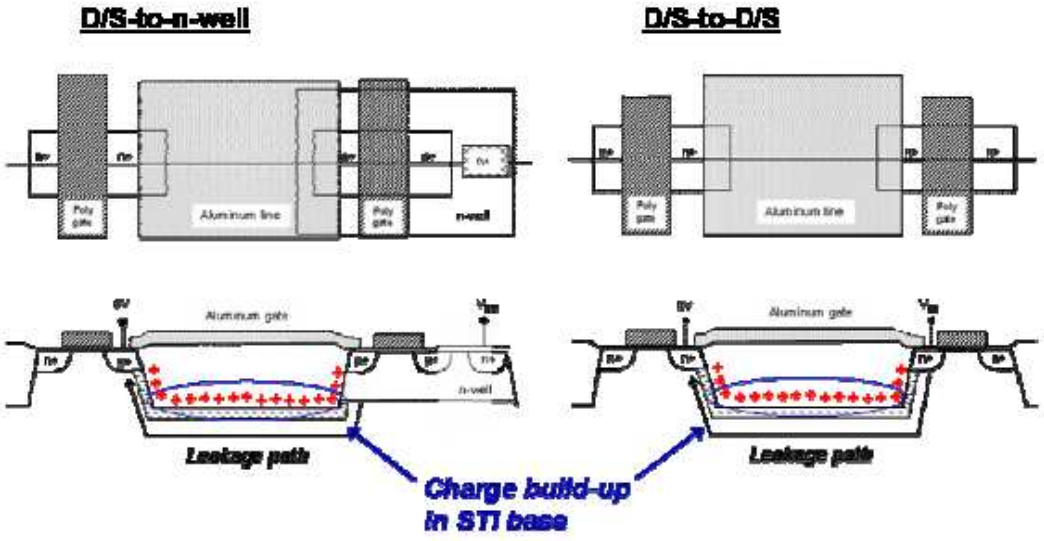

Figure 15 Different leakage paths due to charge trapping in STI [27]

Since we know ionizing radiation affects leads to the trapping of positive charge along the STI sidewall which decreases the V_t of the transistor and increases the off state current. Now we have to model this trapping of positive charge along the sidewall in Cadence so that we can simulate its effects on the performance of the ADC.

Chapter 3

Leakage Modeling in NFET Switches

This chapter explains the steps that are used to model leakage in a NMOS transistor caused by ionizing radiation exposure. When an NMOS transistor in a transmission gate switch is in the on state, it tracks the input. A sampling switch needs to hold the sampled value in the hold phase for correct operation. Due to positive charge build-up in the field oxide due to ionizing radiation, current leakage between drain and source terminals can affect the hold value of the voltage on the capacitor, hence decreasing the linearity of the switch.

3.1 Total Dose Modeling Methodology

In lieu of experimental irradiation characterization data, a combination of TCAD modeling, analytical methods and circuit simulations were used to assess post-irradiation degradation of NFET switches and the ADC architecture discussed previously. In this chapter we focus specifically on the modeling of degradation in NMOS transistors.

3.2 Device Modeling

To model the NMOS transistor from the IBM 8HP process, which is the process used in the ADC design, two TCAD structures were constructed using the Silvaco tool, ATLAS. The first structure shown in Figure 16 represents a 2-D cross-section of the NMOS transistor, cut from drain to source along the transistor channel. The second

structure is also a 2-D cross section of the NMOS transistor, except the cutline is taken perpendicularly to the channel. This structure is used to estimate impact of total dose effects along the STI sidewalls in NMOS devices.

The structures were constructed using all available process information (device geometry, t_{ox} and doping). Then, utilizing ATLAS device simulation, structures were optimized to match the I_{DS} vs. V_{GS} characteristics of a Cadence AMS I-V simulation of the IBM 8HP transistors. Once I_{DS} vs. V_{GS} characteristics of the NMOS transistor agree with Cadence simulation, the optimized doping profile is used to create the NMOS STI sidewall structure. Once the two structures are calibrated, the radiation effects module (REM) was employed. REM is a self-consistent field/charge-trapping module, which models ionizing radiation-induced transport and non-uniform trapping of charge in the oxide. REM simulates the trapped charge build-up in the STI at user-defined dose stress step points and bias conditions. Using REM inside of ATLAS allows for a calculation of the effect total ionizing dose will have on the gate oxides and the NMOS STI sidewall.

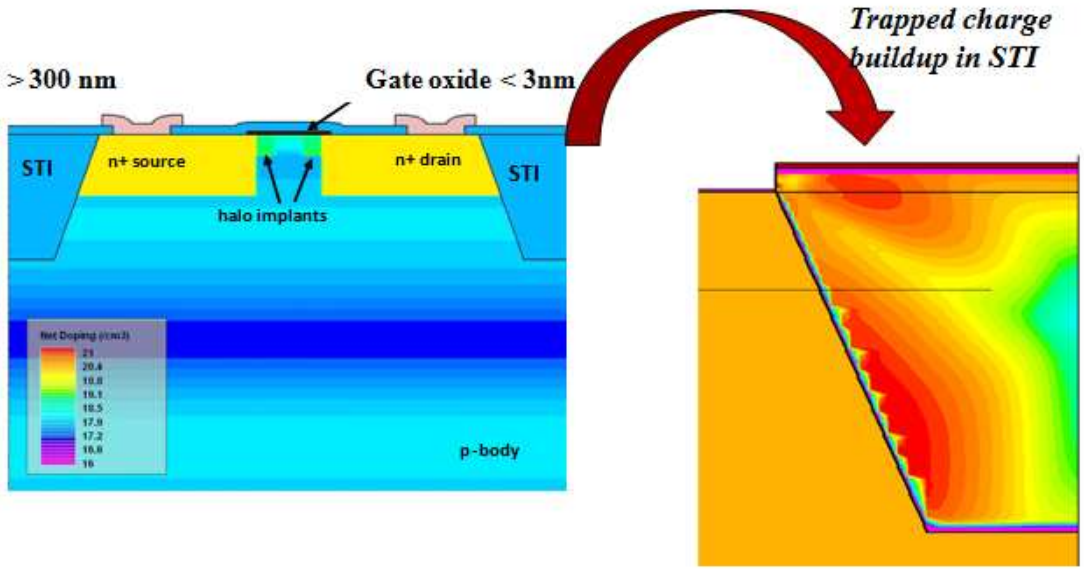

Figure 16: Charge trapping along STI sidewall [26]

It has been discussed in the previous chapter that as the thickness of the gate oxide scales in modern CMOS technologies, charge trapping in gate oxide is no longer a big problem, and the majority of positive charge gets trapped along the STI sidewall. Figure 16 shows the buildup of charge along the sidewall.

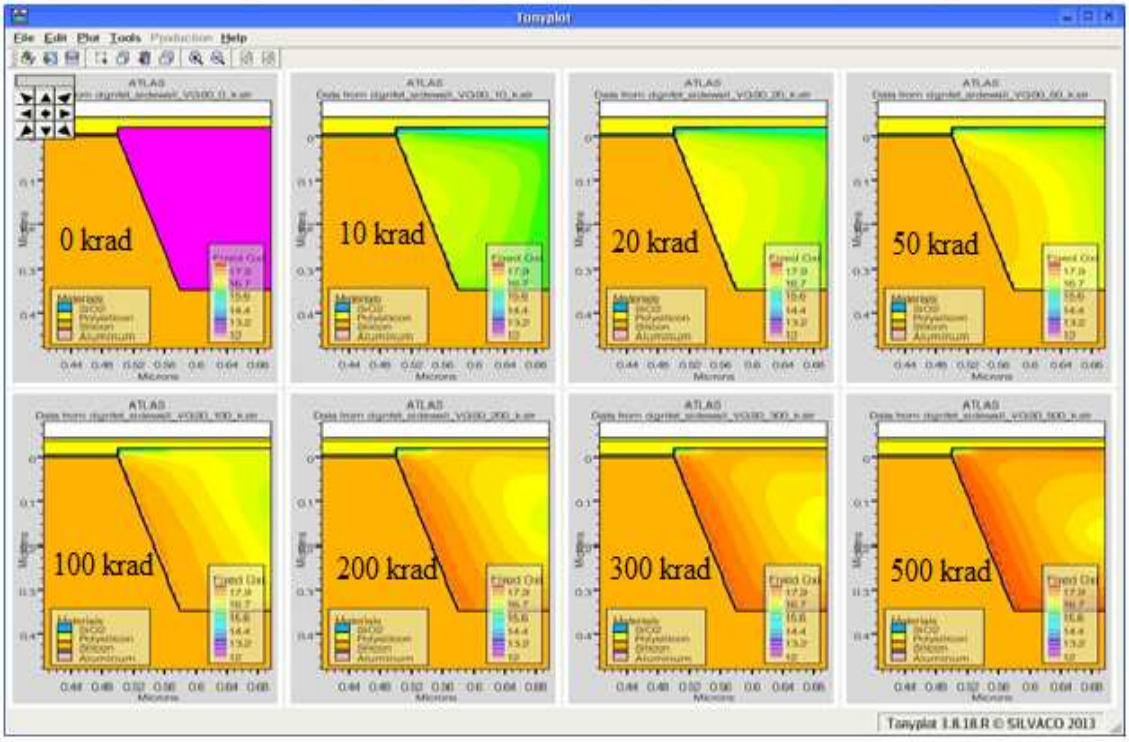

Figure 17: REM simulations showing build up of charge along STI sidewall

ATLAS allows structure files to be saved during simulation, containing position-dependent electrical information. Structure files were saved prior to REM simulated irradiation and after each total dose stress step level. The results of TID modeling of the NMOS structures following REM simulation reveals no significant shift from pre-irradiation threshold voltage for as drawn NMOS device. This is expected, as the device scaling has nearly-eliminated charge trapping in thin gate oxide [27]. However, charge trapping along STI sidewalls, resulting in activation of a “parasitic edge” transistor is an on-going concern for NMOS transistors [27]. Figure 17 shows build-up of positive fixed oxide charge along the STI sidewall for different radiation doses. Simulations of the structure, utilizing ATLAS with REM, reveal significant oxide trapped charge buildup along the STI sidewall. Moreover, the density increases monotonically as the dose level

is increased (see Figure 17). From these structure files, a cut-line was obtained adjacent to the STI sidewall, in the silicon bulk, allowing extraction of the position-dependent ψ_s at each total dose level. Additionally, position-dependent doping bulk (N_A) profile is obtained. As we increase simulated total dose and trap significant positive oxide charge, the surface potential (ψ_s) at the Si/SiO_2 interface along the sidewall will increase. This effect is shown in Figure 18.

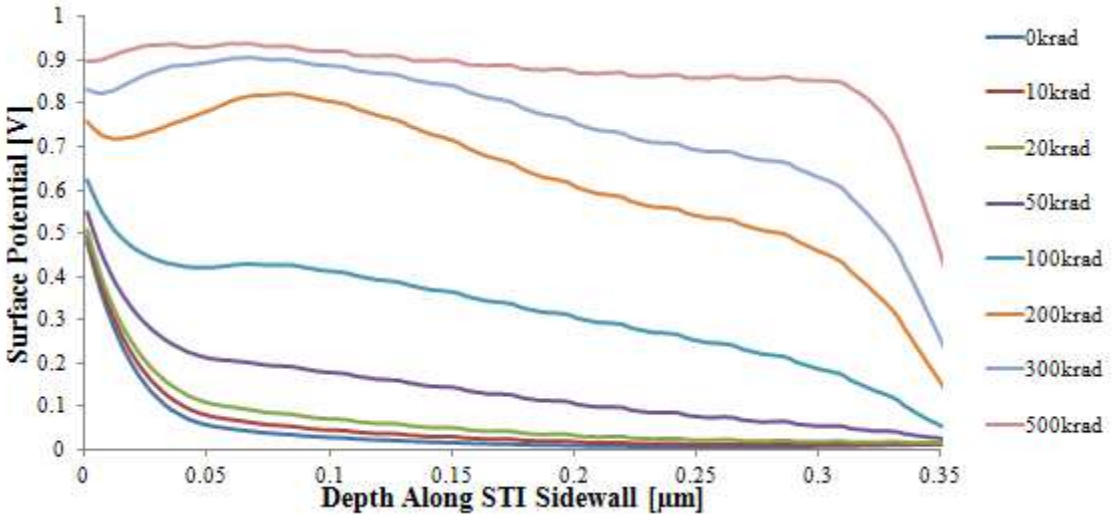

Figure 18: Simulated surface potential along STI sidewalls

From the surface potential at the interface, position dependent fixed oxide sheet charge densities along the STI sidewall can be calculated.

The increased off-state current is modeled as a collection of "parasitic edge" transistors that conduct current in parallel with the "as drawn" NMOS devices after irradiation. As it is a 2-D structure, we must correlate the results of oxide-trapped charge buildup in the STI to a corresponding current conduction along the STI sidewall. This

was accomplished by: 1) extracting structural electrical information from TCAD simulation structures 2) utilizing that information in analytical calculations resulting in 3) parameterization of the "parasitic edge" transistor for use in Cadence simulation.

The extracted total dose (D) and position (z) dependent ψ_s (Figure 26) is used to calculate the flatband voltage (V_{FB}) using the following equation, valid when no gate bias is applied (i.e. V_{GB}=0V) [28]

$$V_{FB}(D,z) = \psi_s(D,z) + \gamma(z)\sqrt{\psi_s(D,z) + \phi_t e^{(\psi_s(D,z) - 2\phi_f(z))/\phi_t}} \quad (3.1)$$

where ϕ_t is the thermal voltage, $\phi_F(z)$ is the Fermi potential, $\gamma(z) = \sqrt{2q\varepsilon_{Si}}\sqrt{N_A(z)}/C_{ox}(z)$ and $C_{ox}(z) = \varepsilon_{ox}/t_{ox}(z) = \varepsilon_{ox}/2\pi z\frac{\theta}{360}$. Theta (θ) is defined as the STI sidewall angle. Furthermore, position-dependent threshold voltage (V_T) can be calculated using the equation:

$$V_T(D,z) = V_{FB}(D,z) + 2\phi_f(z) + \gamma(z)\sqrt{2\phi_f(z)} \quad (3.2)$$

Utilizing the equations and the TCAD structures three parameters are now known: position-dependent t_{OX} and N_A as well as position and total dose dependent V_T.

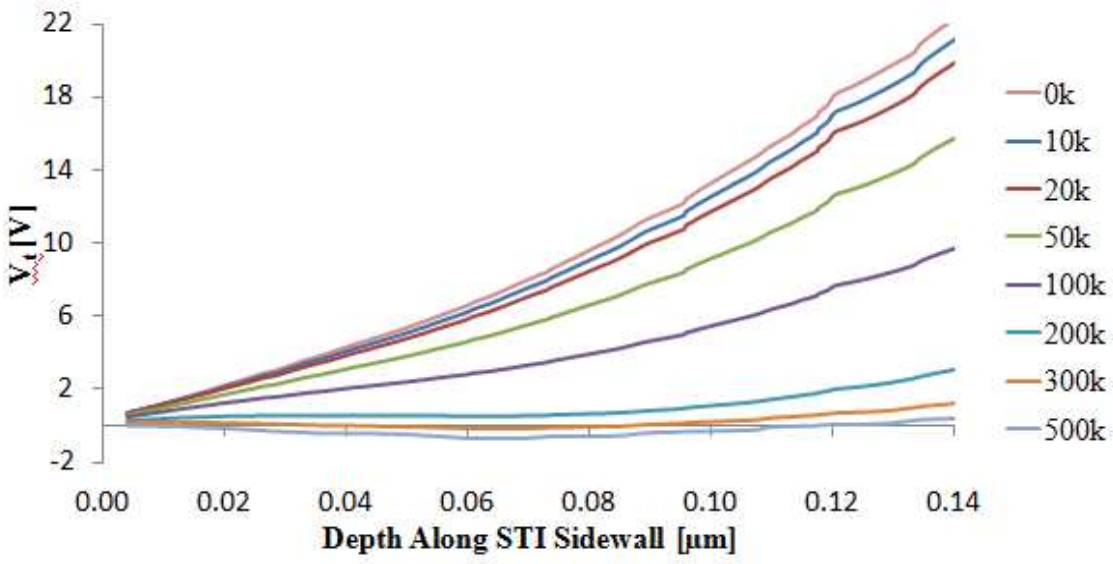

Figure 19: Changing V_t along STI sidewall

Figure 19 shows decreasing V_T with increasing TID. The primary reason for the decrease in V_T is the generation of positive charge along the STI sidewall. This decrease in V_T with increasing TID is the primary the reason for leakage in the NMOS transistor which hampers the performance of the circuit at the macro-level.

3.3 Radiation Enabled Circuit Simulation

For BSIM4 compact transistor models, $V_{T,}$ N_A and t_{OX} can be directly defined for a MOSFET. However, all three parameters change along the depth, z. along the STI sidewall. Using a similar methodology as previously published, the parasitic edge transistor which is formed along the STI sidewall due to ionizing radiation is divided into seven incremental "parasitic edge" transistors of nominal gate width W_i=20nm [29, 30]. Now, for each of the seven incremental transistors N_{Ai}, t_{OXi} and V_{Ti} can be determined

where V_{Ti} is total dose dependent parameter for each incremental transistor.

Incremental Sidewall Transistor	Incremental t_{ox}
SW1	15.3 nm
SW2	41.8 nm
SW3	68.7 nm
SW4	96.7 nm
SW5	127.2 nm
SW6	153.3 nm
SW7	178.1 nm

Incremental Sidewall Transistor	Incremental N_A
SW1	4.62×10^{17} cm^{-3}
SW2	3.58×10^{17} cm^{-3}
SW3	3.29×10^{17} cm^{-3}
SW4	3.74×10^{17} cm^{-3}
SW5	4.56×10^{17} cm^{-3}
SW6	5.50×10^{17} cm^{-3}
SW7	6.28×10^{17} cm^{-3}

Table 3: Incremental t_{ox} and N_a with increasing sidewall width

Table 3 shows the different t_{ox} and N_A values taken for the seven parasitic edge transistors. As we move along the sidewall t_{ox} increases and the doping profile N_A changes along the STI sidewall. In Cadence, a new NMOS device sub-cell is constructed that contains the "as-drawn" devices with seven incremental "parasitic edge" transistors placed in parallel. Figure 20 shows the transistor level modeling of the seven parasitic edge transistors. Voltage controlled voltage sources (VCVS) are used to provide the same biasing conditions to parasitic edge transistors as that of the 'as drawn' transistor. The minimum width required for the parasitic edge transistors is 20 nm and length remaining the same as that of 'as drawn' transistor. In order to overcome the effects due to narrow channel, the minimum width taken for each parasitic edge transistor is 1um. Thus the total amount of leakage current due to parasitic edge transistors is divided by the factor

(1um / 20nm) of 50 so that we could have the leakage current solely due to the presence of parasitic transistors original width. The leakage current obtained as a result of ionizing radiation is added to the main 'as drawn' NMOS transistor with the help of current controlled current source (CCCS).

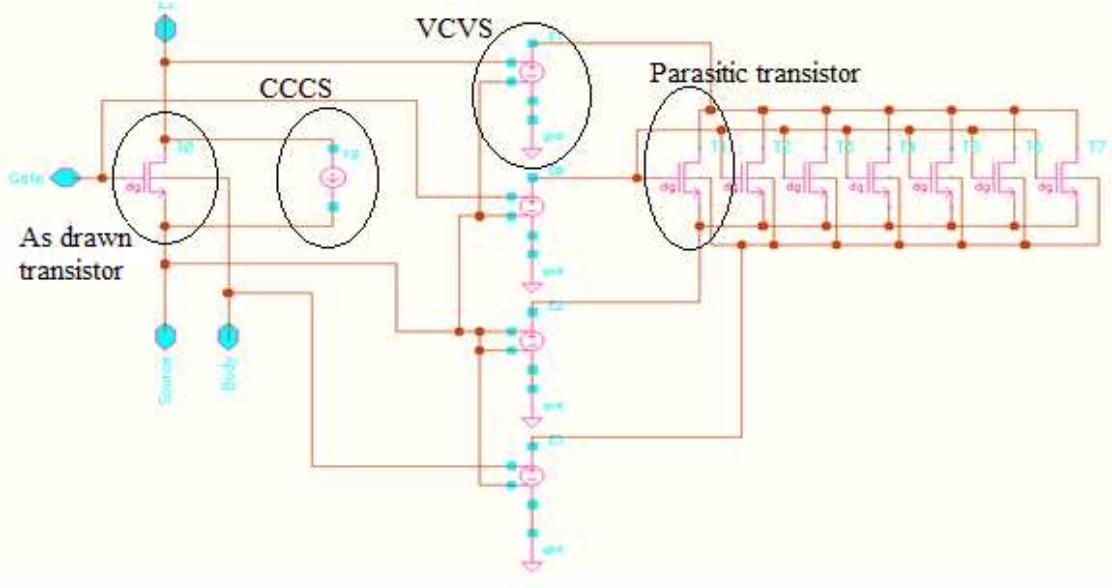

Figure 20: DGNFET with TID enabled Sub-Circuit

A new BSIM4 model is defined for the "parasitic edge" transistor, with the ability to instance $N_{A,}$ t_{OX} and V_T parameters for substitution of N_{Ai} , t_{OXi} and V_{Ti}. Successive Cadence AMS simulations that use V_{Ti} values at a known total dose stress step level effectively simulates radiation damage and leakage in the sub-cell for a given TID level. As higher stress steps are reached, many of the incremental transistors conduct significant I_{DS} current, as V_{Ti} becomes less than the "as-drawn" $V_{T.}$

Figure 21 shows the characteristics of newly modified NMOS devices when subjected to 500 Krad of TID with different biasing across V_{ds}.

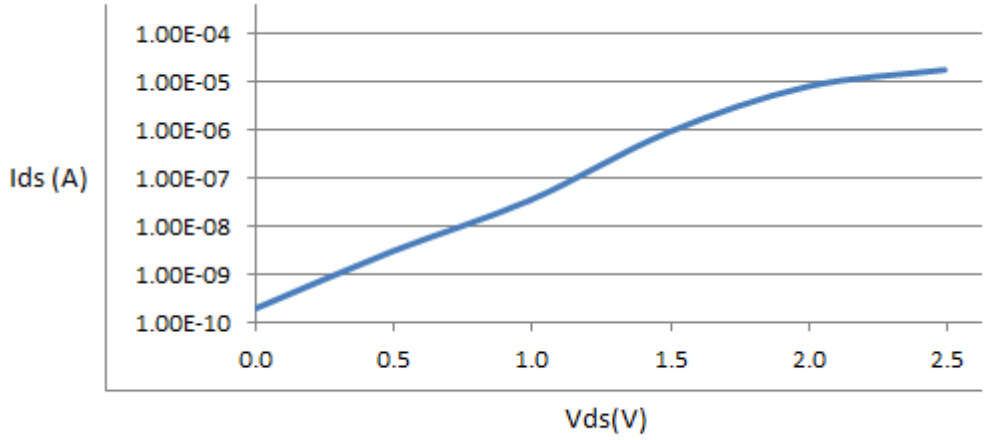

Figure 21: Increase in the off-state current for 500 Krad for different V_{ds}

The simulation results show the there is a tremendous increase in the off-state current depending on the voltage between the drain and source terminals. If Vds is high, off-state current is quite large whereas if the voltage between drain and source terminals goes down to 100mV, off-state current is fairly low.

For the purpose of this thesis, the maximum peak to peak swing tolerable by the ADC is 1.2 V P-P differentials. Single ended swing will be 600 mV P-P. Hence the drain and source terminals maximum voltage difference in the worst case scenario is 600 mV which accounts for a leakage current of around 10 nA between the two terminals. Chapter 4 gives us the simulation specifications and the circuit level modeling results obtained as a result of leakage introduced due to ionizing radiation effects in the NMOS devices.

Chapter 4

Simulation of ionizing radiation effects in an eleven bit pipeline ADC

A pipeline ADC is composed of several 1.5 bit gain stages in series. The accuracy of the pipeline ADC depends on the performance of individual 1.5 bit gain stage. If the performance of 1.5 bit gains stage deteriorates it will affect the accuracy of the complete pipeline.

4.1 Switched Capacitor Network

The switched capacitor network in 1.5 bit gain stage is a very important block which determines the linearity of the gain stage. Switches used in the sample and hold network of the gain stage needs to be ‘N’ bit linear if the required accuracy of the gain stage is ‘N’ bits. If the switches in the sample and hold network of the gain stage are not ‘N’ bit linear, the gain stage linearity will decrease which in turn will decrease the linearity of the whole pipeline.

A leaky switch in the front end sample and hold is a threat to the accuracy of the ADC. Leakage in a switch is tolerable when we move down the pipeline as the required linearity decreases by 6 dB for every stage. Linearity of a switch can directly be related to the leakage levels in a transistor. High leakage levels correspond to more degradation in linearity.

As discussed in the previous chapter ionizing radiation leads to the formation of positive charge along the STI sidewall. This trapped charge increases the off state current might lead to the wrong voltage values at the sampling capacitors. Modeling different amount of leakages in a switch due to different doses of radiation and comparing the performance of a gain stage and hence on an eleven bit pipeline analog to digital converter with and without leakage is the objective of this thesis.

The gain stage with and without leaky switch is implemented in the pipeline structure and the performance is quantified based on different doses of radiation for the given operating specifications. Figure 22 shows the switched capacitor network of the 1.5 bit gain stage.

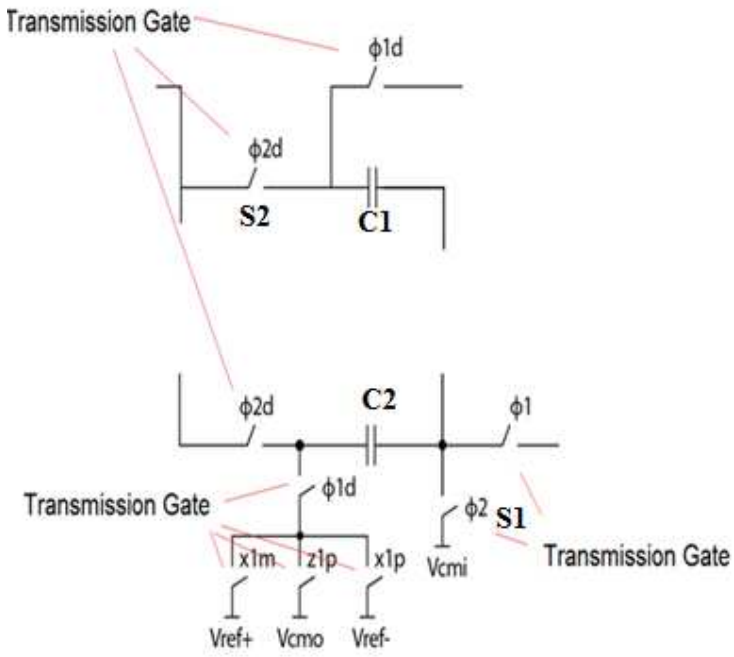

Figure 22: Switched capacitor network

The amount of leakage current due to ionizing radiation between the two terminals in the switch is largely dependent on the difference between drain and source voltage of the NMOS transistor when it is in the off state.

As discussed in the previous chapter, leakage current increases exponentially in the off state when drain to source voltage is increased from 0 to 2.5 volts. Simulations were performed on the circuit shown in Figure 22. Differential input is applied to the circuit in Figure 22. In order to see the drooping effects in the off state of a switch in the open loop configuration, a special test condition is created which is not from the required specifications. To be able to see maximum amount of degradation, a single ended input swing of the magnitude 2.5 volts at a sampling frequency of 5 MHz is applied to switched capacitor network. This test condition provides the worst case biasing to the switched capacitor network so that maximum leakage can occur through the switch.

In the sampling phase of the clock (when clock is high and switch is on), the switch is tracking the input signal in a perfect manner as shown in Figure 23. When the switch is transformed from on state to off state, a test condition which is created increases the voltage difference between drain and source terminal in the off state to 2.5 volts so that we can have leakage current of the order of 18 uA between the source and drain terminals of the NMOS transistor. Sampling frequency is also reduced to 5 MHz so that we can have more amount of time for the switch to leak. This large amount of leakage

through the switch causes a lot of degradation in the hold phase. The switch is not able to hold the value on to the sampling capacitor in the open loop configuration and leaks.

Figure 23 shows a major droop in the off state of a switched capacitor network when used in the open loop configuration.

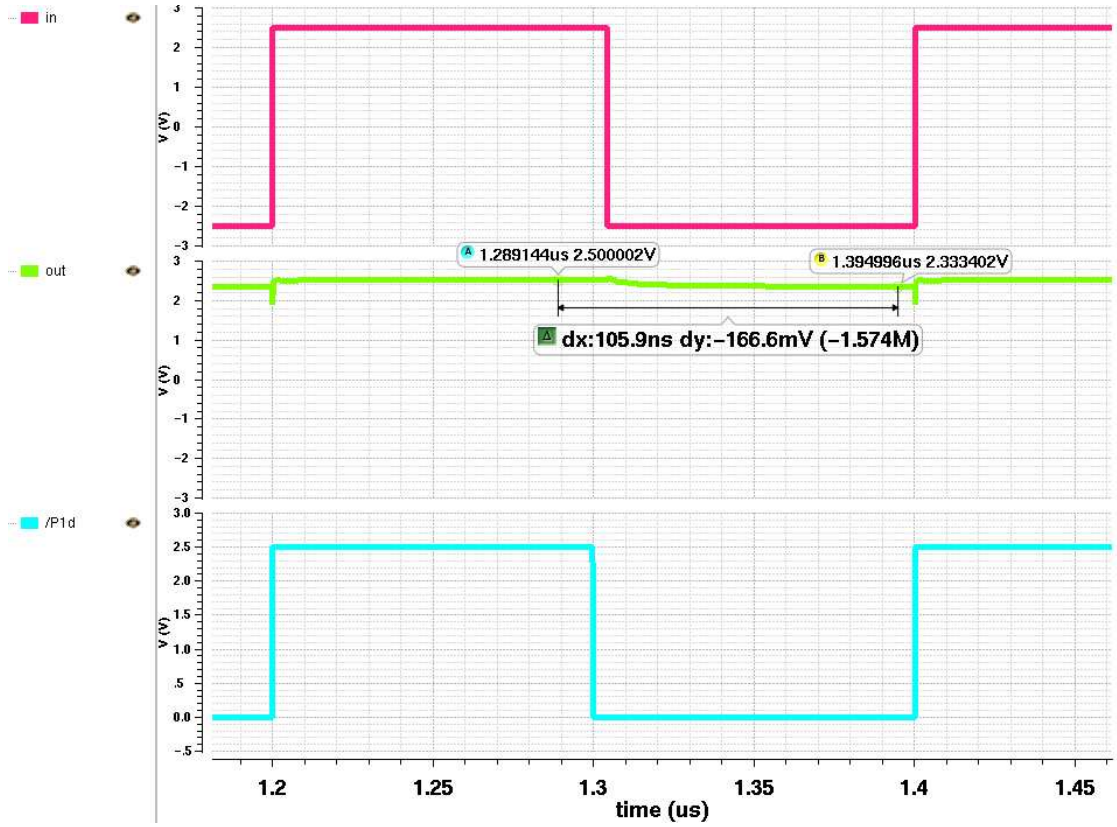

Figure 23: Test results for a special condition

As we always make use of the circuit in the differential manner, the output voltage when taken differentially in the hold phase of the clock is degraded by an amount of 166.6 mV which is a very big degradation.

When the same circuit shown in Figure 22 is tested in an open loop configuration with a sampling frequency of 162.5 MHz (which is the original specification) and with a single ended swing of 600 mV volts, we would not be seeing a big amount of droop in the hold phase as the amount of leakage between the two terminals is of the order of 10 nA and also leakage time available for the switch is also less which will keep the output voltage intact in the hold phase of the clock.

4.2 Different sub-blocks affecting performance

The 1.5 bit gain stage is an integral part of pipeline ADC. If some degradation is observed in the working of a switched capacitor network which is an integral part of the single 1.5 bit gain stage, it is likely there would be some degradation seen at the whole pipeline ADC level as the same 1.5 bit gain stage is repeated in the pipeline ADC.

The three bit flash which is being used in the backend pipeline do not have any switched capacitor network as the input is given directly to the comparators, hence three bit flash will behave as expected without any degradation.

The op-amp, which is an integral part of the 1.5 bit gain stage do not play any role in degrading the performance of the circuit. As we have discussed in the previous chapters ionizing radiation effects introduces leakage in the NFETs only. There is no leakage introduced in the PFETs because their edges do not turn on when exposed to

ionizing radiation as their body material is N-type. From the topology of the op-amp as already discussed in chapter 1, there is no NFET used in the design. BJT (NPN's) and PFETs are used.

The digital blocks used in the digital correction logic of the ADC (registers, full adders) used in the design do not play any major role in degrading the performance as such small amount of leakage due to ionizing radiation do not have any effect on the performance of the digital circuits at macro level.

The comparator is also an important block which could affect the performance of the circuit at macro level by giving out the wrong decisions which could hamper the complete functionality of the circuit. Ionizing radiation simulations on comparator are beyond the scope of this thesis.

4.3 Simulation results for the given specifications

For the specifications of the ADC as mentioned in chapter 1, the worst case V_{ds} is of the order of 600 mV single ended as peak to peak swing for the ADC is 1.2 Volts. Also the sampling frequency is 325 MHz. The leakage current for this V_{ds} is only of the order of 9-10 nAmps for the maximum TID of 500 krads.

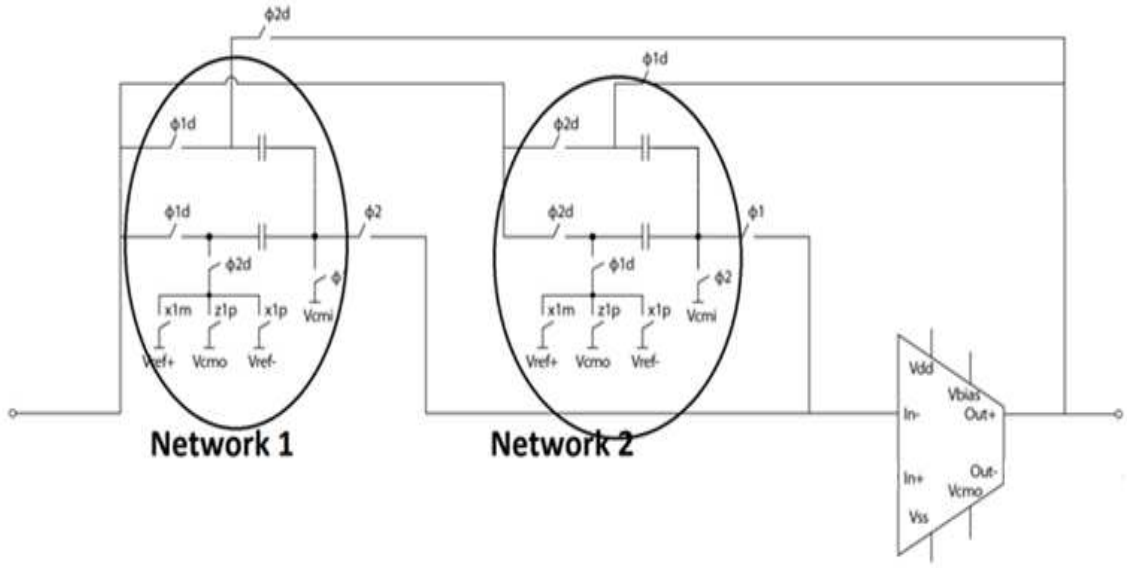

Figure 24: Switched capacitor network implementation in closed loop

The switched capacitor network is implemented in the closed loop configuration along with op-amp in negative feedback as shown in Figure 24. The simulations are performed for the given specifications of the ADC. As we know from the structure of the clocks as discussed in chapter 1, the non-overlapping period between Φ1d and Φ2d which are sampling and hold clocks respectively is 60 ps which is extremely small to see any major drooping. In the hold phase (Φ2d) for the network 1 as shown in Figure 24, the op-amp is in a closed loop configuration and supplies current of very a high magnitude which makes the closed loop system stable. Even if leakage of the order of few nA occurs in the switches due to radiation effects, the op-amp high output current nullifies the leakage and keeps the output voltage intact.

The same simulations are also performed with the much lower sampling frequency of the order of 5 MHz along with doubling the signal swing so that more leakage could occur. It was observed that the simulation results with and without leaky switches are almost same. The reason being, even if we have very large amount of off time for the droop to happen if the frequency is lowered, the non-overlapping period between the two clocks is only 60 ps. In the off state, switched capacitor network comes in the closed loop configuration as it will happen in all the cases and op-amp will provide large amount of current nullifying any degrading affects due to small amount of leakage in the switches. Figure 25 shows the simulation results of a single 1.5 bit gain stage with the usage of radiation models. We are getting an SFDR of around 64db with the usage of radiation models. SFDR number almost remains same even if the leaky switches are removed.

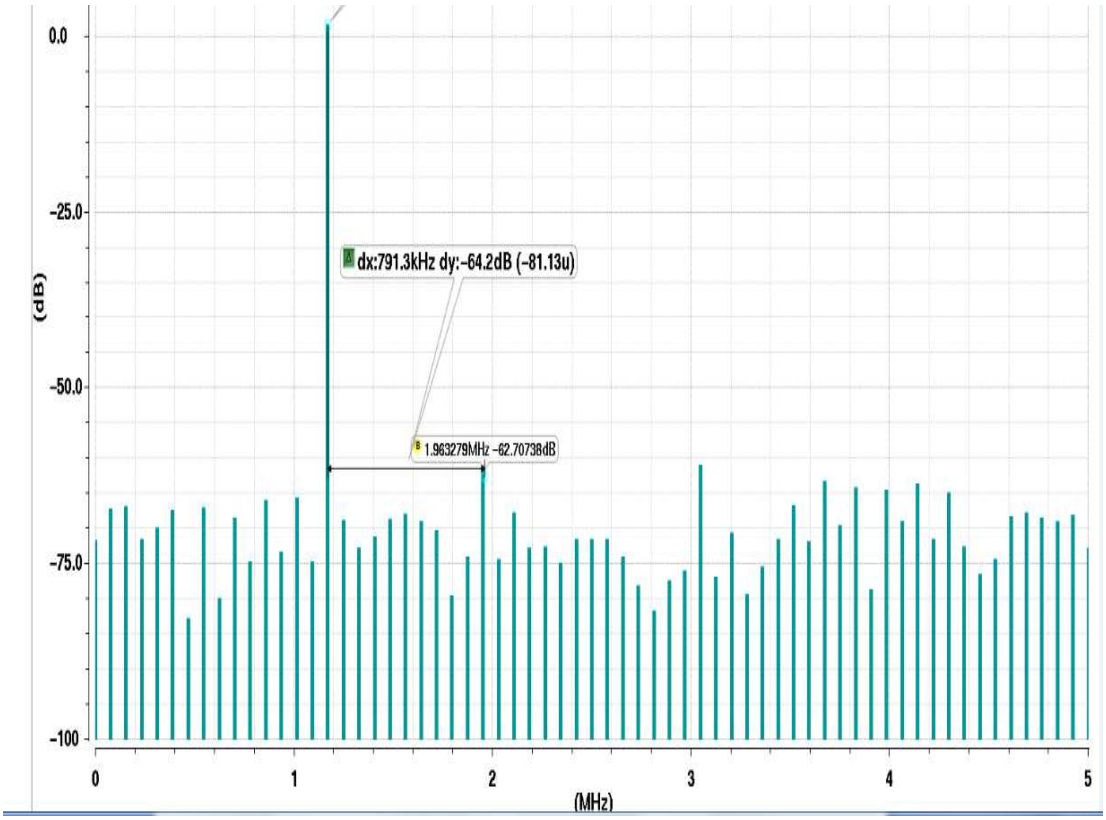

Figure 25: SFDR plots for special test condition of 1.5 bit gain stage

When simulations are performed to calculate the SNDR (Signal to noise and distortion ratio) of the 1.5 bit gain stage for different doses of radiation for the actual specifications of the ADC as described in chapter 1, no difference in the performance is seen for different doses of ionizing radiation as the leakage current is too small to cause any major degradation. We will have maximum amount of leakage for the worst case Vds of 600 mV which would not be the input pattern always for given sampling frequency and for given input bandwidth. Also due to the fact that the RSD algorithm performs many different operations of adding and subtracting the reference voltages from the input

voltage as explained in chapter 1, we would be passing out the residue voltages to the next stage in series which will be much lesser in swing, hence less amount of leakage and the integrity of the signal is maintained in the pipeline.

Figure 26 shows the simulation results of the complete eleven bit pipeline ADC. The effective number of bits (ENOB) value is constant for different doses of radiation.

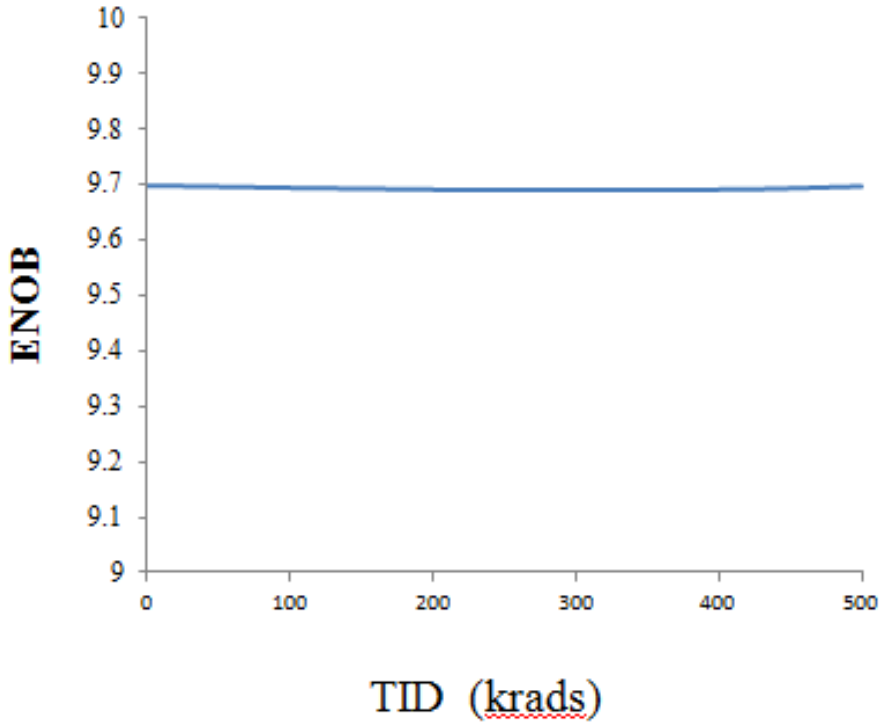

Figure 26: TID vs ENOB plot

This figure clearly shows that the ADC designed in IBM 8HP 130nm process for the given specifications is not prone to performance degradation under the ionizing radiation effects.

Chapter 5

Conclusion

A eleven bit pipeline ADC for given specifications is designed in an IBM 8HP 130nm process for NASA. It is simulated with and without the effects of ionizing radiation. A unique methodology is incorporated for simulating ionizing radiation effects at transistor level.

When the ADC is simulated without any ionizing radiation effects, an ENOB of 9.7 is obtained. Simulations were performed for different doses of radiation. When an ADC is exposed to different doses of radiations ranging from 0 krads to 500 krads, it was observed that the increased level of TID doses leads to an increase in the off state leakage current of an NFET (which is an integral part of switch) from few nA to 18 uA. The high amount of leakage in the switch could be a deteriorating factor in the performance of a circuit. It was found that the primary reason for an exponential increase in the leakage current is the trapping of positive charge along the STI sidewall region. It was also observed that the amount of charge trapped in the gate oxide is very less. Charge trapping in gate oxides did not cause any threshold voltage shifts in the gate oxide region. Threshold voltage shifts were only observed along STI sidewall which was primarily the reason for leakage in the NFET.

When the complete ADC is simulated with the radiation models against the given specifications, it was observed that the leakage in the switches of the gain stages were of the order of only few nano-amperes. The sampling speed of the ADC was very fast, because of which there was no difference in the value of voltage at the sampling capacitors with and without leaky switches. Due to the fact that we are sampling the correct voltage at the sampling capacitors for all levels of doses, we did not see any degradation in the performance of the whole ADC at macro level.

There are many other sub-blocks of the ADC like op-amp, different digital blocks which are also not susceptible to any performance degradation due of the ionizing radiation affects. Simulation results showed almost same ENOB number of 9.7 when an ADC is simulated for different doses of radiation

Hence, we arrive at a conclusion that the eleven bit 325 MSPS ADC fabricated in an IBM 8HP process for NASA is a radiation hard design up to a TID level of 500 Krads for the given specifications.

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