Distributed Photovoltaic Generation in Residential Distribution Systems: Impacts on Power Quality and Anti-islanding

by

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ABSTRACT

The past few decades have seen a consistent growth of distributed PV sources. Distributed PV, like other DG sources, can be located at or near load centers and provide benefits which traditional generation may lack. However, distribution systems were not designed to accommodate such power generation sources as these sources might lead to operational as well as power quality issues. A high penetration of distributed PV resources may lead to bi-directional power flow resulting in voltage swells, increased losses and overloading of conductors. Voltage unbalance is a concern in distribution systems and the effect of single-phase residential PV systems on voltage unbalance needs to be explored. Furthermore, the islanding of DGs presents a technical hurdle towards the seamless integration of DG sources with the electricity grid.

The work done in this thesis explores two important aspects of grid integration of distributed PV generation, namely, the impact on power quality and anti-islanding. A test distribution system, representing a realistic distribution feeder in Arizona is modeled to study both the aforementioned aspects. The impact of distributed PV on voltage profile, voltage unbalance and distribution system primary losses are studied using CYMDIST. Furthermore, a PSCAD model of the inverter with anti-island controls is developed and the efficacy of the anti-islanding techniques is studied. Based on the simulations, generalized conclusions are drawn and the problems/benefits are elucidated.

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NOMENCLATURE

ac	Alternating current
ANSI	American National Standards Institute
ASD	Adjustable speed drive
C	Capacitance
CAP 1	Shunt capacitor 1
CAP 2	Shunt capacitor 2
CAP 3	Shunt capacitor 3
CSP	Concentrating Solar Power
dc	Direct current
DDSRF	Double decoupled synchronous rotating frame
d-	Direct axis
dq	Direct-quadrature synchronously rotating axis
DG	Distributed generation
EMTP	Electromagnetic Transients Program
EMTDC	Electromagnetic Transients including DC
f_{sys}	Frequency in Hz
f_{lower}	Lower frequency threshold
f_{upper}	Upper frequency threshold
FORTRAN	The IBM Mathematical Formula Translating system
GIS	Geographic Information Systems

I_d	Direct axis current
I_{dp}	Direct axis component of positive sequence current
I_{dn}	Direct axis component of negative sequence current
I_q	Quadrature axis current
I_{qp}	Quadrature axis component of positive sequence current
I_{qn}	Quadrature axis component of negative sequence current
IEEE	Institute of Electrical and Electronics Engineer
INV 1	PV inverter 1
INV 2	PV inverter 2
L	Inductance
L	Inductor
LC	Inductor-capacitor
LCL	Inductor-capacitor-inductor
LTC	Load Tap Changer
LVUR	Line Voltage Unbalance Ratio
NDZ	Non-Detection Zone
NEMA	National Electrical Manufacturers Association
NREL	National Renewable Energy Laboratory
P	Proportional

P	Real power
PCC	Point of Common Coupling
PI	Proportional Integral
PLCC	Power Line Carrier Communication
PLL	Phase Locked Loop
PSCAD	Power System Computer Aided Design
PV	Photovoltaic
PVUR	Phase voltage Unbalance Ratio
PWM	Pulse Width Modulation
Q	Reactive power
q-	Quadrature axis
R	Resistance
REC	Recloser
SPICE	Simulation Program with Integrated Circuit Emphasis
SVR	Step Type Voltage Regulator
[T]	Park's transformation matrix
T1	Transformer 1
T2	Transformer 2
US	United States
V	Voltage

V_a	Phase A voltage
V_b	Phase B voltage
V_c	Phase C voltage
V_{cd}	Direct axis control voltage
V_d	Direct axis voltage
V_{cq}	Quadrature axis control voltage
V_q	Quadrature axis voltage
V_{lower}	Lower voltage threshold
V_{upper}	Upper Voltage threshold
VUF	Voltage Unbalance Factor
X	Reactance
$\alpha\beta$	Alpha-beta stationary axis
ω	Angular frequency in radians/s
Θ	Transformation angle in radians

Chapter 1. A background on solar photovoltaic generation and grid integration

1.1 Renewable energy in the United States

Concerns about energy independence and environmental impacts of burning fossil fuel, in recent years, have promoted large investments in development of renewable energy. Despite sluggish (or negative) load growth in the United States due to an economic slowdown, ambitious renewable portfolio standards, federal tax incentives, emerging power conversion technologies, and a general acceptance of renewable energy resources have contributed to the rapid proliferation of renewable energy markets in the United States [1]. In 2009, 11% of the net electric energy generation (in MWh) in the U.S, constituted of renewable energy resources. Conventional hydropower constitutes 7% of the net electric energy generation (in MWh), but has limited growth potential. Other renewable sources like wind, solar, geothermal and biomass constitute 4% of the net electric energy generation (in MWh). Although these sources form a modest share of the nation's renewable generation portfolio mix, they have been growing more rapidly in the recent years [2], [3].

1.2 Growth and development of solar photovoltaic generation

By the end of 2009, solar energy resources, consisting of concentrating solar power (CSP) and solar photovoltaic (PV) together constituted 0.02% of the domestic electricity generation (in MWh) in the U.S [3], [4]. The advent of large - scale merchant projects that sell their power directly to electricity utilities has significantly aided the deployment of solar PV technologies and has attracted

considerable financial capital. With about 900 MW of new installed capacity (by nameplate rating), the cumulative installed PV capacity in the US has reached 2.5 GW, at the end of 2010 [3], [4]. According to NREL, there is approximately 16 GW (by nameplate rating) of utility scale solar resources under development, as of January 2012. Solar PV constitutes an overwhelming 72% of these ongoing projects [4].

About a decade ago, solar photovoltaic generation was mostly used for off – grid applications such as telecommunications and water pumping for irrigation. However, in recent years, to attain required renewable portfolio standard levels, the majority of the new PV installations are connected to the grid both at the distribution and transmission level. At the transmission level, PV generation facilities are central-station photovoltaic systems, consisting of several individual PV inverters connected to a medium voltage collector system, which is further connected to the grid via a station transformer. Central-station PV systems are typically utility owned and range between 10 kW to 25 MW. At the distribution level, PV generation sources include both central-station PV systems and smaller rooftop units. Residential rooftop PVs, typically ranging between 2-10 kW constitute a major share of the PV installations at the distribution systems. Due to the ease of installation, modularity and pollution free operation, PV generators are highly suitable for integration in a residential environment. Although an expensive technology, several financial incentives in the form of tax rebates, government subsidies and special metering rates, in recent years, have encouraged

homeowners to install rooftop PVs leading to a rapid proliferation of distributed PV in the distribution systems.

1.3 Research motivation and objectives

Distribution grids have been typically designed assuming the primary substation to be the single generating source in the system. High penetration of distributed PV sources at the distribution level needs close examination as distribution grids were not intended to accommodate active generation sources at the downstream end of the feeders. The presence of multiple distributed generation (DG) sources in distribution grids might cause bidirectional power flow leading to potential problems like overvoltages, increased fault levels and misoperation of devices sensitive to the direction of current flow like, relays, fuses, reclosers and voltage regulators. Furthermore, of the issue of islanding presents new challenges to the safe and reliable operation of the distribution grids. Sections 1.4 through 1.7 provide a more detailed discussion of these topics. The aim of this research is to investigate the impact of various levels of PV generation on a test distribution feeder and study the islanding conditions that may be encountered during the operation of the system.

This research focuses on an actual distribution feeder in the United States. A deployment of large-scale PV generation is studied. The distribution feeder has been modeled in a commercially available distribution system analysis software package, CYMDIST, to investigate the impact of three different levels of PV pen-

etration on voltage regulation, voltage unbalance factor, and line losses. To study the islanding conditions and the operation of inverters upon islanding, the same distribution feeder has been modeled in a commercially available analysis package, PSCAD / EMTDC. Several cases have been discussed and the findings of the study have been presented.

1.4 Distributed generation and its impacts on distribution systems

Distributed generation refers to power generation sources that can be located at or near load points. These sources of electric power are not connected directly to the bulk power transmission system (100 kV and above) and range from a few kilowatts up to 50 MW [5], [6]. Power production technologies that are integrated within distribution systems fit under this definition. The distributed generation technologies can be further classified as renewable and non – renewable types. Popular renewable technologies include wind and solar whereas non – renewable DG sources comprise of internal combustion engines, combustion turbines, microturbines and fuel cells [7]. Distributed PV being a commonly used DG source, has a similar impact on the distribution grid as other DG sources have. The benefits and potential problems reported with presence of DGs in distribution systems are discussed in the following sections.

Benefits of DGs in distribution systems

Distributed generation, being located at or near load centers provide benefits which traditional generation may not. In studies conducted, it was found that

presence of DG sources have a significant effect on the reliability and power quality of distribution systems [8-13]. Some of the important benefits derived from DG sources are shown in Table 1.1.

Table 1.1 Matrix of distributed generation services and benefits [13]

		Benefit categories				
		Energy cost savings	Savings in T&D losses and congestion costs	Deferred generation capacity	System reliability benefits	Power quality benefits
DG Services	Reduction in Peak power requirements	✓	✓	✓	✓	✓
	Ancillary service capability: Operating reserve Regulation Black start Reactive power	✓	✓	✓	✓	✓
	Emergency Power supply	✓	✓		✓	✓

Problems associated with DGs in distribution systems

Transmission systems (69 kV and above) often have a meshed architecture, where the buses are interconnected and the system protection and controls are designed for bi-directional power flow in transmission lines. In contrast to transmission systems, residential distribution primary systems (35 kV and below) are typically radial and have been designed for unidirectional power flow considering the primary substation as the sole generating source in the network. The

presence of DG sources in distribution systems violates this assumption and new operating situations might arise which are not encountered in conventional systems. Initial studies conducted to assess the impact of DG sources have pointed out the possible power quality, reliability and operational issues that might be of concern [14-19]. Some of the prominent problems associated with grid connected DGs are as follows:

- Connecting DG sources may lead to faulty operation of switching capacitors and voltage regulators [14]. Reverse power flow in the feeder during excess generation at DG locations causes step – type voltage regulators (SVR) to misoperate as the direction of voltage regulation is determined by the direction of real power flow. If DG sources are operated in a voltage regulating mode, it gives rise to "voltage hunting" between DGs and voltage controlled capacitor banks [14].
- Although, in practice, DG sources are not allowed to actively regulate voltage, they may lead to voltage swells due to reversal of real power through the feeder resistances for networks with low *X/R* ratios [14], [15], and [16].
- DG sources under certain operating conditions may worsen voltage unbalance in distribution primary feeders, which are often unbalanced due to the presence of single-phase loads [15], [16].
- Presence of DG sources poses a problem for the feeder protection system, which are primarily reclosers and fuses for radial distribution networks. DG sources cause problem with fuse coordination, as fuses are incapable of direc-

tional comparison. DGs may also lead to desensitization of relays and reclosers when located upstream with respect to the fault location [17], [18].

- Although power electronics based DG sources like PV generators contribute only twice the rated current for a small duration of time and do not necessitate use of higher rated fault interrupting devices, increasing penetration levels of such sources may warrant a thorough examination of circuit breaker and fuse ratings [17], [18].
- Another important issue reported with grid integration of DG is that of operation during loss of grid, also referred to as an islanding condition. Islanded operation of DGs may lead to equipment damage, problems with reclosing and shock hazard for operation and maintenance personnel [19].

1.5 Power quality issues in distribution systems

The term power quality in distribution systems has widely been used to define the ability of the load bus voltage to maintain a sinusoidal waveform at rated voltage and frequency [20]. A more generalized definition of power quality problem could be any abnormality in voltage, current or frequency, which may lead to damage of equipment or utility assets. A brief discussion of the power quality indices studied in this work and their implications is provided in this section.

Voltage regulation

Voltage regulation is defined as the difference between the voltage magnitude at the load terminals at full load and no load in % of full load voltage with input voltage held constant [21].

Load current flowing through line impedances and distribution transformers cause voltage drops along the feeder resulting in poor voltage regulation under heavy load conditions. The recommended service and utilization voltage as per ANSI C84.1 [22] is given in Table 2.1, where, range A refers to the normal operating conditions and range B refers to the emergency operating conditions for short periods. As a standard practice, utilities in USA maintain service voltages within a limit of ± 5 % under normal operating condition. Short-term overvoltages lead to overheating and permanent damage, primarily to electronic components like circuit boards, which are sensitive to high voltages. Long-term undervoltages on the other hand, lead to overheating of motors due to increased currents. Prolonged abnormal voltage conditions cause severe damage to both residential and commercial loads, which are primarily a combination of motor, and electronic loads.

Table 1.2 ANSI C84.1 voltage range for 120 V voltage level

Range	Service		Utilization	
	Min	Max	Min	Max
A (Normal)	-5%	+5%	-8.3%	+4.2
B (Emergency)	-8.3%	+5.8%	-11.7%	+5.8%

Voltage unbalance

Voltage unbalance is referred to as a condition where in the three phase voltages differ in amplitude or are displaced from their normal 120 degree phase relationship or both [20]. There are various definitions of voltage unbalance in literature [23]. The National Electrical Manufacturers Association (NEMA) definition [24] of voltage unbalance factor, also known as the line voltage unbalance ratio (LVUR) is given by

$$\text{LVUR} = \frac{\text{Maximum deviation from average line voltage}}{\text{Average line voltage}} \tag{1.1}$$

The IEEE definition of voltage unbalance [25], also known as the phase voltage unbalance ratio (PVUR) is given by

$$\text{PVUR} = \frac{\text{Maximum deviation from average phase voltage}}{\text{Average phase voltage}} \tag{1.2}$$

The voltage unbalance factor (VUF in %) [25], [26] is defined as the ratio of the magnitude of negative sequence voltage to the magnitude of the positive sequence voltage. The VUF (%) is given by

$$\text{VUF}(\%) = \frac{|\text{Negative sequence voltage}|}{|\text{Positve sequence voltage}|} \times 100 \tag{1.3}$$

Tripping of adjustable speed drives (ASD) and damage to three-phase induction motors are the most common problems reported with supply voltage unbalance [27-30]. A brief description of the two phenomena is provided in the following paragraphs.

Steady state voltage unbalance has a deteriorating effect on current unbalance and harmonics of pulse width modulated (PWM) voltage source inverter (VSI) based ASDs. A high level of unbalance can lead to tripping of overload protection in ASDs thus stalling critical processes. High unbalance also increases the harmonics injected into the system by the ASDs [27], [28].

Voltage unbalance at the motor stator terminals cause current unbalances which are disproportionately higher. Unbalanced current leads to torque pulsations, mechanical stresses, increased losses and shorter winding insulation life due to overheating [29], [30]. NEMA MG-1-1998 requires motor to give rated output only for unbalance less than 1 % [24]. It is a common practice among most utilities to maintain the voltage unbalance factor within 2 % at the point of common coupling (PCC).

Distribution system primary losses

Distribution system primary losses refer to the active power losses that occur due to current flowing through transmission line, transformer resistance, and transformer core losses. The distribution system losses can be partly reduced by either reducing the resistance of the conductors or by reducing the load current flowing through them. High losses in distribution feeder not only cause overheating of conductors, they also translate directly into dollar losses.

1.6 Islanding of distributed generation

An important technical issue with integration of DGs is that of islanding. The IEEE 1547 standard [31], defines an island as a condition in which an area is solely energized by local generation sources when it is electrically separated from rest of the electric grid. An island can be formed due to a number of reasons some of which are as follows [32]:

- Opening of utility breaker due to a fault, which the DG protection system fails to detect.
- Opening of utility breaker due to nuisance tripping.
- Switching of distribution loads.
- Intentional disconnection of utility supply for feeder or equipment maintenance.
- Disruption of feeder conductors due to natural calamities or human acts.

Although DGs can operate in an islanded condition and still supply power to the connected loads, operating under such conditions may lead to degradation of power quality. Some of the drawbacks of operating DGs in islanded condition are as follows [19], [32]:

- A DG source supplying power after disconnection of the main grid keeps the distribution feeders energized and jeopardizes safety of line workers.
- The voltage and frequency of the grid may go out of permissible limits during islanded operation causing damage to sensitive equipment.

- If DG sources are not adequately grounded, they may lead to overvoltage conditions in the islanded portion of the system.
- High speed reclosing could result in out of phase reclosing of DG, which leads to large mechanical torque and high currents that damage generators and prime movers.

An intentional islanding or anti-islanding scheme is a control mechanism that detects islanding conditions without misoperating during grid disturbances. The anti-islanding schemes developed so far can be broadly divided into three different categories: passive inverter - resident methods, active inverter - resident methods and methods not resident in the inverter including the use of communication between utility and PV inverter [32], [33], [34]. These methods are further described as follows:

Passive inverter - resident methods

These methods of anti- islanding depend on detection of an abnormality in the voltage magnitude or frequency at the point of common coupling (PCC) between the inverter and the utility supply occurring due to disconnection of the grid [32], [33]. The commonly used passive methods discussed in literature are:

- Over/under voltage
- Over/under frequency
- Voltage phase jump
- Detection of voltage harmonics
- Detection of current harmonics.

Passive methods of anti-islanding are relatively inexpensive options as they are easy to implement using over/under voltage and frequency detection. Although inexpensive and straightforward, these methods have relatively large non detection zones (NDZ), a load condition when the islanding method fails to detect an island. In addition, having stiff limits on voltage and frequency may lead to nuisance tripping of inverters during disturbances, which are transitory in nature, like starting of motors.

Active inverter - resident methods

This group of anti-islanding techniques uses a variety of methods to cause an abnormal condition at the PCC by worsening the frequency drift or voltage drift occurring due to the loss of utility supply [32], [34]. The commonly used active methods discussed in the literature are:

- Impedance measurement
- Slip-mode frequency shift
- Frequency bias
- Sandia frequency shift
- Sandia voltage shift
- Frequency jump.

Active methods of anti-islanding are superior to passive methods of island detection in a sense that they have relatively small NDZs as compared to passive methods. Although these methods have smaller NDZs, they may not be able to detect an islanding condition when the generation within the island matches the

load closely. Some active methods like impedance measurement and frequency jump may lose effectiveness during multi-inverter conditions. Active methods, which include harmonic injection or frequency drift, may lead to power quality degradation as they work on the principle of disturbance injection. Implementing active methods need additional controllers, which can selectively detect islanding condition from transient disturbances.

Communication based methods

Communication based methods involve transmission of data between the utility and the inverter [34]. In this method, the utility sends out a transfer trip to the inverter, in case the utility side breaker trips, causing the inverter to stop energizing the island. Some commonly used communication based methods are

- Power line carrier communication (PLCC)
- Signal produced by disconnect
- Supervisory control and data acquisition.

Communication based methods are superior techniques of islanding detection and prevention as they are effective over all ranges of loads and do not cause any power quality degradation. These methods are highly effective when the DGs have connectivity with the utility through communication channels. However, these methods are expensive requiring additional communication equipment and advanced monitoring infrastructure at the utility substation, DG locations and switchgear. Moreover, implementation of the communication-based methods

may not be effective in distribution systems where large parts of the feeders are protected using fuses.

1.7 Recent trends in distribution system modeling

Distribution systems, though an important part of the power delivery network has been long neglected in terms of modernization and analysis. Limited availability of data on distribution systems has hindered detailed modeling of loads as well has secondary distribution networks. Rising penetration levels of distributed generation and evolution of smart grid technologies has ameliorated this problem largely. Most utilities nowadays have complete geographic information system (GIS) data of feeders and transmission and distribution assets [35], [36]. A high-resolution data of loads and generation is also available to the utilities through advanced metering infrastructure and modern data acquisition systems. New techniques have been developed, using which both the temporal and spatial nature of load and generation distribution can be captured [36], [37]. Such detailed modeling of distribution systems, which is granular enough to identify individual residential or commercial load locations, has enabled the further investigation of the impact of high penetration of distributed generation in these systems.

Chapter 2. Impact of distributed PV on power quality: power flow analysis

2.1 Introduction

Advancements in metering infrastructure and data acquisition systems have enabled the development of detailed distribution system models. With such detailed models available, the impacts of integrating DG sources in distribution grids can be studied intensively. The impact of integrating distributed PV on a realistic test distribution feeder has been studied in this chapter. An overview of the test distribution feeder modeled in CYMDIST, the analysis approach used and the findings of the power flow analysis have been provided in the following sections.

2.2 Distribution system modeling in CYMDIST

CYMDIST is a commercially available distribution system analysis software package, which performs several types of analysis on balanced or unbalanced, three phase, two phase and single phase systems being operated in meshed, looped or radial architecture [38]. The capabilities of CYMDIST include

- Balanced and unbalanced power flow
- Fault Analysis
- Load balancing
- Load allocation/estimation
- Optimal capacitor placement.

To study the effect of distributed PV on a radial distribution system, a test distribution feeder is modeled in CYMDIST. The test feeder is modeled based on

- GIS data containing the location of the lines equipments and loads.
- Equipment data, which includes line parameters, transformer parameters, inverter parameters and source parameters.
- Load data, and generation data of the distributed PV.

Modeling of a distribution system in CYMDIST involves combining the geographic location of the equipments, loads and generators obtained from GIS data with the load and generation data, typically available from energy management system databases. The model thus created, captures both the spatial distribution of the load and its variation at fixed time intervals. A detailed description of the modeling procedure can be found in [36], [37].

2.3 Test distribution feeder

The test distribution feeder modeled for this study, represents a typical urban distribution feeder located in Arizona. The load data used as input consists of the total feeder load sampled at one hour averages. The equipment data and the line parameters used for modeling the system were provided by the utility. The test distribution feeder, modeled using CYMDIST, is shown in Figure 2.1. The test feeder consists of a 12.47 kV, 9 mile long, three-phase overhead line with single-phase cable feeders emanating from the main feeder along its length (not shown in Figure 2.1). The sequence impedances of the cable and overhead line used are given in Table 2.1.

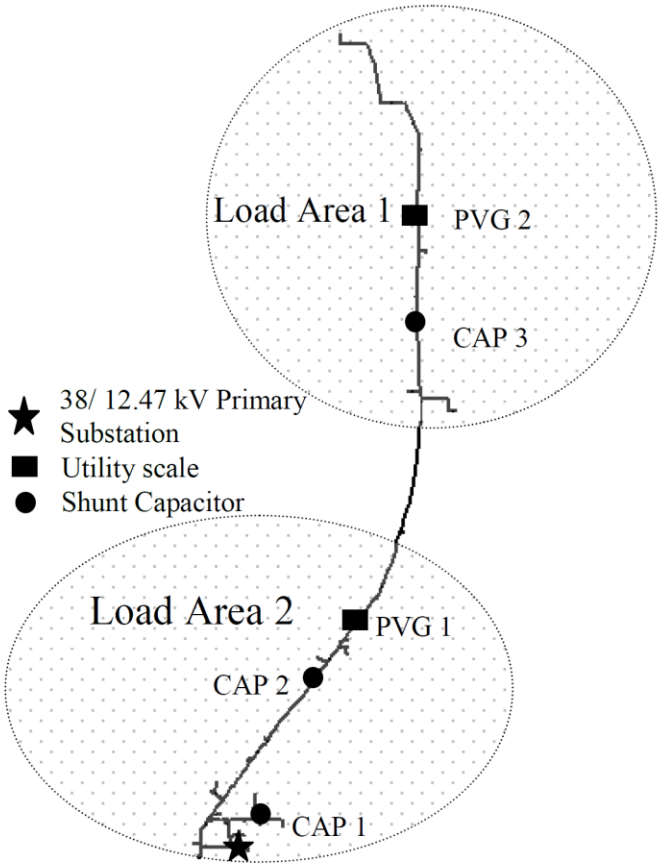

Figure 2.1 Test distribution feeder modeled in CYMDIST

Table 2.1 Feeder data (R, X in Ω/mile and B in μS/mile)

Feeder Type	R1	R0	X1	X0	B1	B0
Overhead Line (3Φ)	1.65	2.31	0.87	2.49	5.45	3.03
Cable (1Φ)	1.66	1.66	0.86	0.86	93.18	93.18

The three phase overhead line has been modeled as a balanced overhead line, assuming it is transposed. The key features of the system are as follows:

- The feeder serves two load areas, load area 1 and load area 2 as shown in Fig. 2.1. The residential loads as well as the single phase PVs are concentrated in these two areas.
- The residential loads are located on the radial feeders and some of them have single-phase PV generators installed on rooftops. The residential load model along with the installed PV source is shown in Figure 2.2.
- The residential loads are modeled as constant power loads operating at a power factor of 0.89 lagging.
- The PV generators are modeled as electronically coupled generators operating at unity power factor. These sources can be thought of as negative power drawing loads.
- The rooftops PVs have a generating capacity in the range of 3 - 4 kW.
- There are two large, utility scale, three phase PV installations at about 3 miles (PVG 1) and 7 miles (PVG 2) from the substation.
- PVG 1 generates 400 kW, PVG 2 generates 500 kW and the total generation from rooftop PV installations is 400 kW. The distribution of the single phase PV on each phase is 174 kW on phase A, 109 kW on phase B and 117 kW on phase C. The total distributed PV in the system is 1.2 MW.
- There are three shunt capacitor banks located at CAP 1, CAP 2, and CAP 3, which have a capacity of 800 kVAr, 1200 kVAr and 800 kVAr respectively.

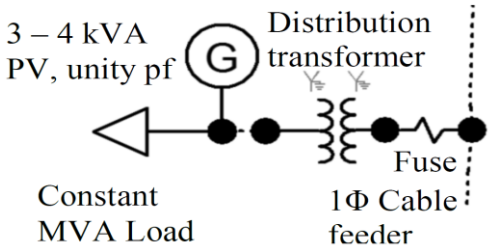

Figure 2.2 Typical residential load model with rooftop PV source

The hourly load variation of the system for the year 2012 is shown in Figure 2.3. The system loading conditions that have been chosen for the study are marked in the load curve.

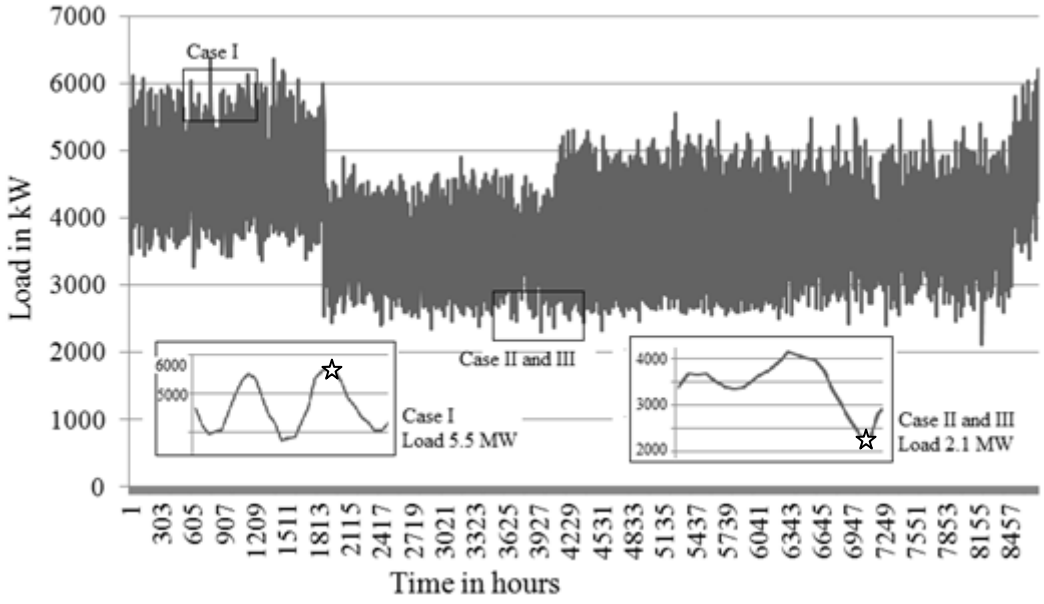

Figure 2.3 Load of the test distribution system over one year

2.4 Analysis approach

As a part of this study, the effect of distributed PV on the voltage profile, voltage unbalance and primary losses of a distribution system are investigated. To assess the impact of distributed PV, three different cases are considered. A summary of the cases have been provided in Table 2.2.

Table 2.2 Summary of loads and PV generation

Case	Load on phase A	Load on phase B	Load on phase C	Loading condition	Generation form PV	PV penetration (% by MW)
I	1895 kW	1855 kW	1750 kW	Heavy	1.2 MW	21.81
II	620 kW	755 kW	725 kW	Light	1.2 MW	57.14
III	620 kW	755 kW	725 kW	Light	2 MW	95.2

Case I represents a scenario when the distribution system is heavily loaded and the PV generation constitutes 21.81 % of the total load. In this case, the total load in the system is 5.5 MW and the total generation from PV is 1.2 MW. Case II represents a scenario when the system is lightly loaded and the PV generation constitutes 57.14 % of the load. The total load in the system is 2.1 MW and the total PV generation is 1.2 MW. Case III has a similar loading condition as Case II, however in this case the PV generation is 2 MW, which is 95.2 % of the load. Cases I and II are actual load and generation scenarios that can be encountered in this system. For simulating Case III, where the PV penetration level is maximum, the lightly loaded system of Case II is taken and the PV penetration level is in-

creased to 2 MW by including an additional 0.8 MW of residential rooftop PV. The additional PV has been distributed in load area 1 and load area 2. The three cases chosen represent two distinct operating conditions, heavily loaded system with a low PV penetration and lightly loaded system with a moderate to high PV penetration. The cases chosen are expected to elucidate the impact of PV during heavy load conditions and the possible concerns when the PV generation levels are comparable to the load in the system

To analyze the system, a three phase unbalanced power flow is conducted and the parameters examined are plotted. As per the IEEE 1547 standard, distributed PV generators are not allowed to perform active voltage regulation [31]. In compliance with the IEEE 1547, the PV generators are set to operate at unity power factor. In the following sections, the simulation results and a discussion of the results are presented.

2.5 Effect of distributed PV on voltage profile

In this section, the impact of distributed PV generation on the voltage profile of the test distribution feeder has been studied. While performing the simulations, the shunt capacitors are kept in service to examine their impact on all the cases.

Figure 2.4 shows the plot of line-to-neutral voltages along the main feeder for Case I. As the system is heavily loaded, the voltage drop along the feeder is high. To maintain the service voltage within acceptable limits, the supply voltage at the substation is set to 1.03 p.u. by raising the load tap changer (LTC). From

Figure 2.4, it can be seen that the minimum feeder voltage, without any PV on the system, is 0.955 p.u. The introduction of 1.2 MW of PV in the system improves the voltage profile and the minimum voltage on the feeder rises to 0.975 p.u. During heavy load conditions, the distributed PV generation is less than load demand and there is no reversal of power flow in the lateral feeders. The distributed PV serves a part of the load locally, reducing the load current in various sections of the main feeder. A reduction of load current in the main feeder results in less voltage drop at the downstream end of the feeder.

Figure 2.5 shows the plot of line-to-neutral voltages along the main feeder for Case II. As the system is lightly loaded, in the absence any PV generation the receiving end voltages of the feeder are close to 1 p.u. The voltage swell at the middle of the feeder without the inclusion of PV, as seen in Figure 2.5, is due to the reactive power injection by the shunt capacitors. It can be seen that inclusion of 1.2 MW of distributed PV generation leads to a voltage rise at the receiving end of the feeder. As the PV penetration level is higher than in Case I, a reversal of power flow occurs at the distributed PV locations where generation is more than the load. This effect, compounded with the reactive power injection by the shunt capacitors gives rise to a voltage swell at the receiving end of the feeder. However, it should be noted that at this level of PV penetration the feeder voltages remain within the ± 5 % limit.

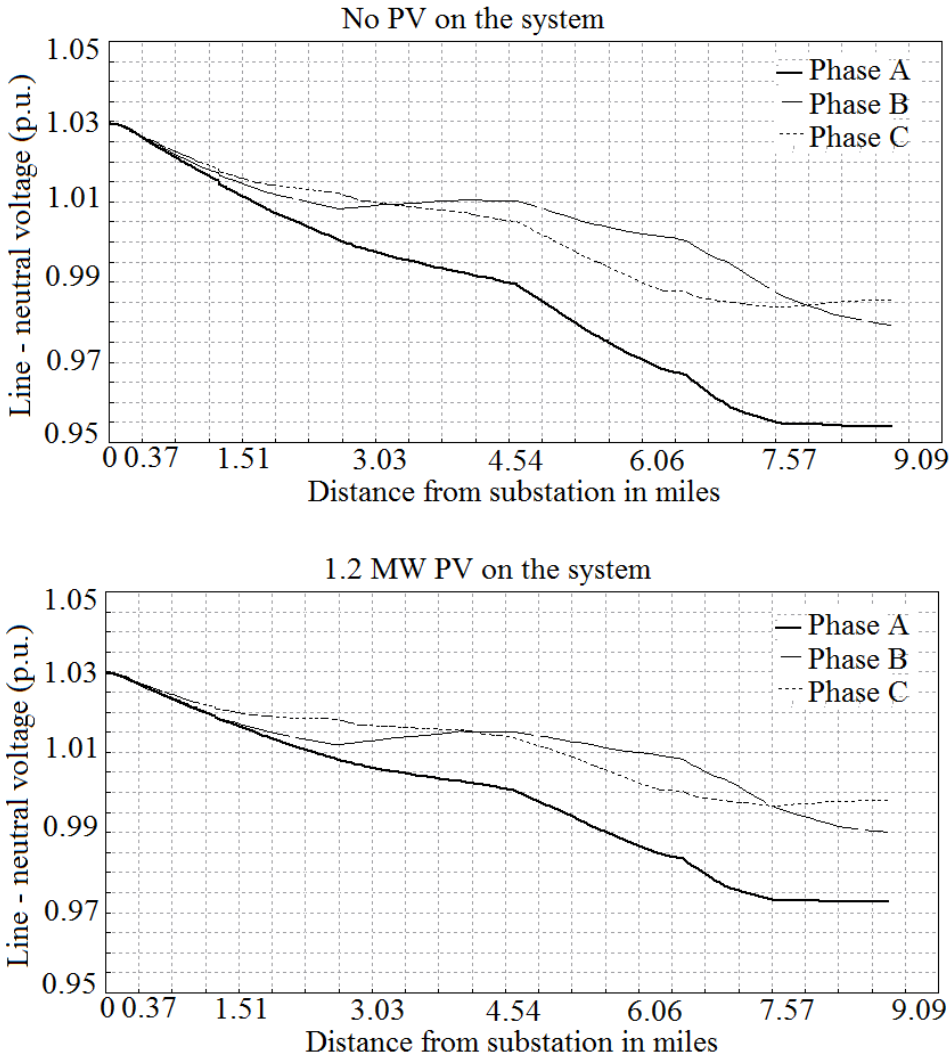

Figure 2.4 Voltage profile along the main feeder for Case I

Figure 2.6 shows the line-to-neutral voltages along the main feeder for Case III. As the PV penetration level increases compared to Case II, there is an increase in the line-to-neutral voltages along the main feeder. Although the feeder voltages remain within 1.05 p.u., a close study of the lateral feeders show marked overvoltages at certain feeder locations in load area 1, which is lightly loaded as compared to load area 2. Figure 2.7 shows portions of feeder at resi-

dential locations in load area 1 where overvoltages occur. The voltage rise at these locations is due to the reversal of power flow as the residential load is less than the rooftop PV generation. It should be noted that the voltage correcting shunt capacitors connected to the system also contribute to this rise.

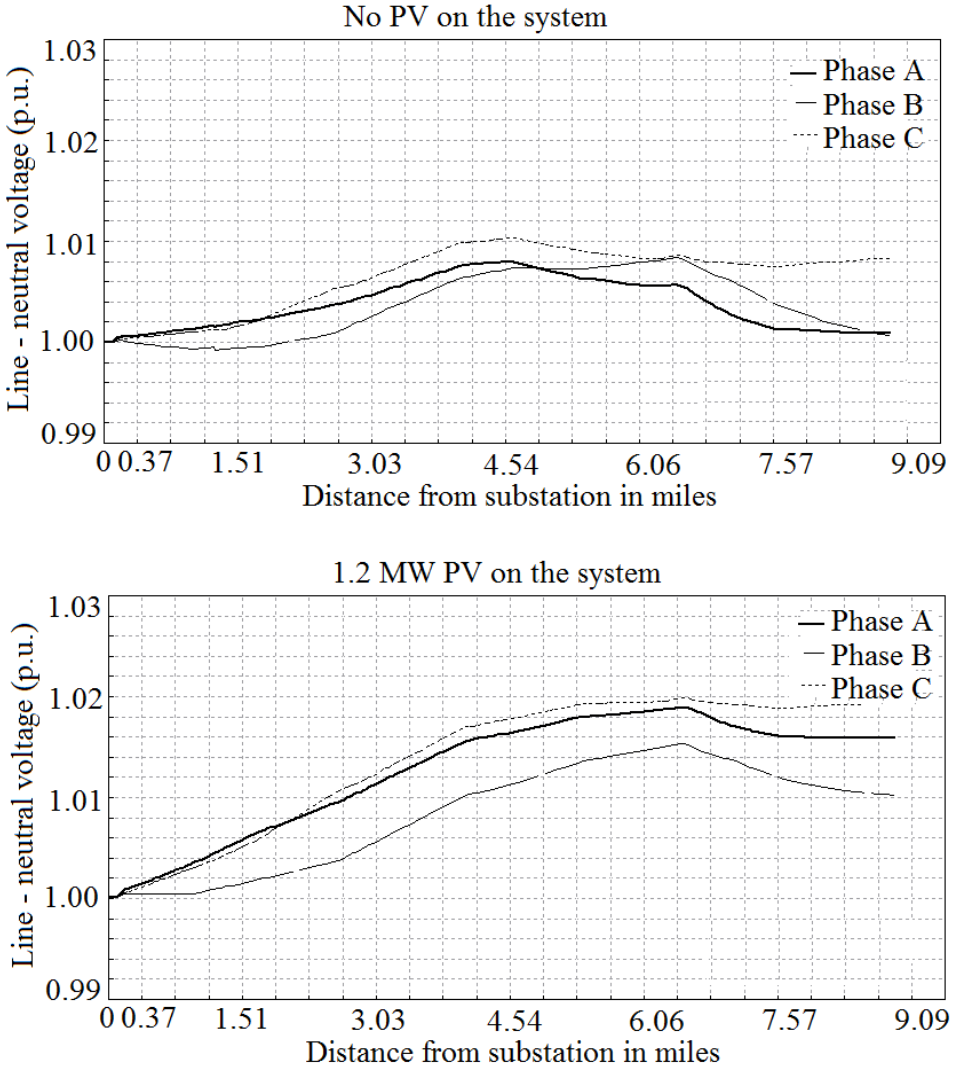

Figure 2.5 Voltage profile along the main feeder for Case II

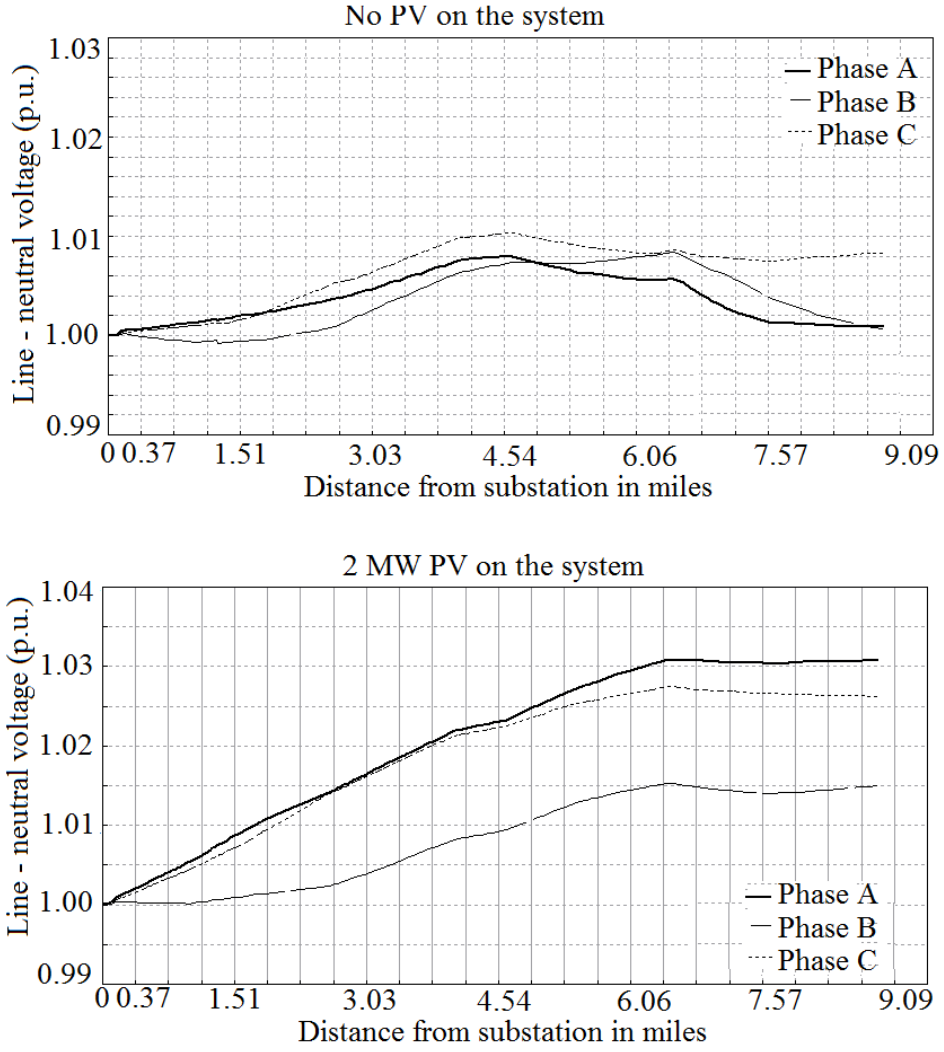

Figure 2.6 Voltage profile along main feeder for Case III

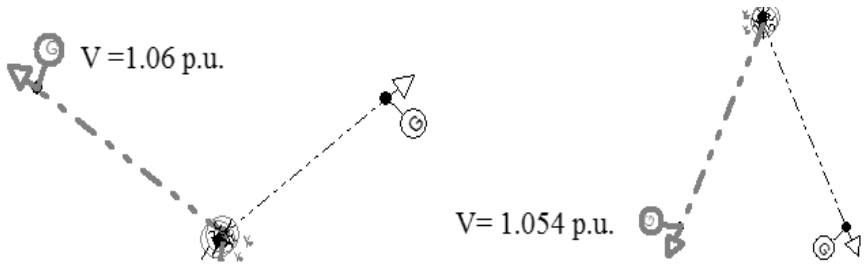

Figure 2.7 Overvoltages at a few residential locations in load area 1.

2.6 Effect of distributed PV on voltage unbalance

In this section, the effect of distributed PV generation on the voltage unbalance of the test distribution feeder has been studied. As discussed in Chapter 1, there are three commonly used definitions of voltage unbalance. In this study, the index VUF (%) has been used as a measure of the unbalance of the supply voltage. It is assumed that the substation is a balanced three-phase source and as the distance from the substation increases, the unbalanced load currents cause unequal voltage drops on the feeder leading to unbalanced phase voltages. In general, the voltage unbalance factor increases with the distance from the substation.

Figure 2.8 shows the plot of voltage unbalance factor along the main feeder for Case I. For a heavily loaded system, inclusion of distributed PV has a notable effect on the VUF (%). It can be seen from Figure 2.8 that the voltage unbalance factor decreases significantly, from 0.7 % to 0.45 % at the feeder end, when 1.2 MW of distributed PV generation is included in the system. With the presence of distributed PV, the loads are supplied locally. This, in effect, decreases the unbalanced current in the supply feeder resulting in reduced unbalanced voltage drop and improvement of the VUF (%) at the PCC.

Figure 2.9 shows the plot of voltage unbalance factor along the main feeder for Case II. As the system is lightly loaded, the voltage unbalance factor is low and reaches a maximum value of 0.22 %. This is a consequence of there being no appreciable voltage drop along the feeder and as a result, the phase voltages remain nearly balanced at the PCC. A comparison of the VUF (%) in Case II shows

that for a lightly loaded system, a moderate penetration level of distributed PV has no significant effect on the voltage unbalance factor and the maximum value of VUF (%) is close to 0.22 % with or without the inclusion of any distributed PV in the system. However, it should be noted that there is an increase in the voltage unbalance with the inclusion of distributed PV in the middle of the main feeder. This increase is due to the fact that different amounts of penetration of PV in different phases causes unequal voltage rise in the middle of the feeder.

Figure 2.10 shows the plot of voltage unbalance factor along the main feeder for Case III. A high penetration level of PV in this lightly loaded system causes the maximum voltage unbalance to rise from 0.22% to 0.48%. Although in this case the VUF (%) increases, it is still within the acceptable 2% range and is not a concern for utility operators. The rise in voltage unbalance factor in this case is due to the unbalanced increase in PV generation on the three phases. For the test distribution system, increased PV generation results in higher voltage rise in phase A and phase C as compared to phase B (see Figure 2.6), resulting in an increased VUF (%). As the residential PV systems are single-phase units, their effect on the voltage unbalance depends on their distribution in the system and distribution of the loads as well.

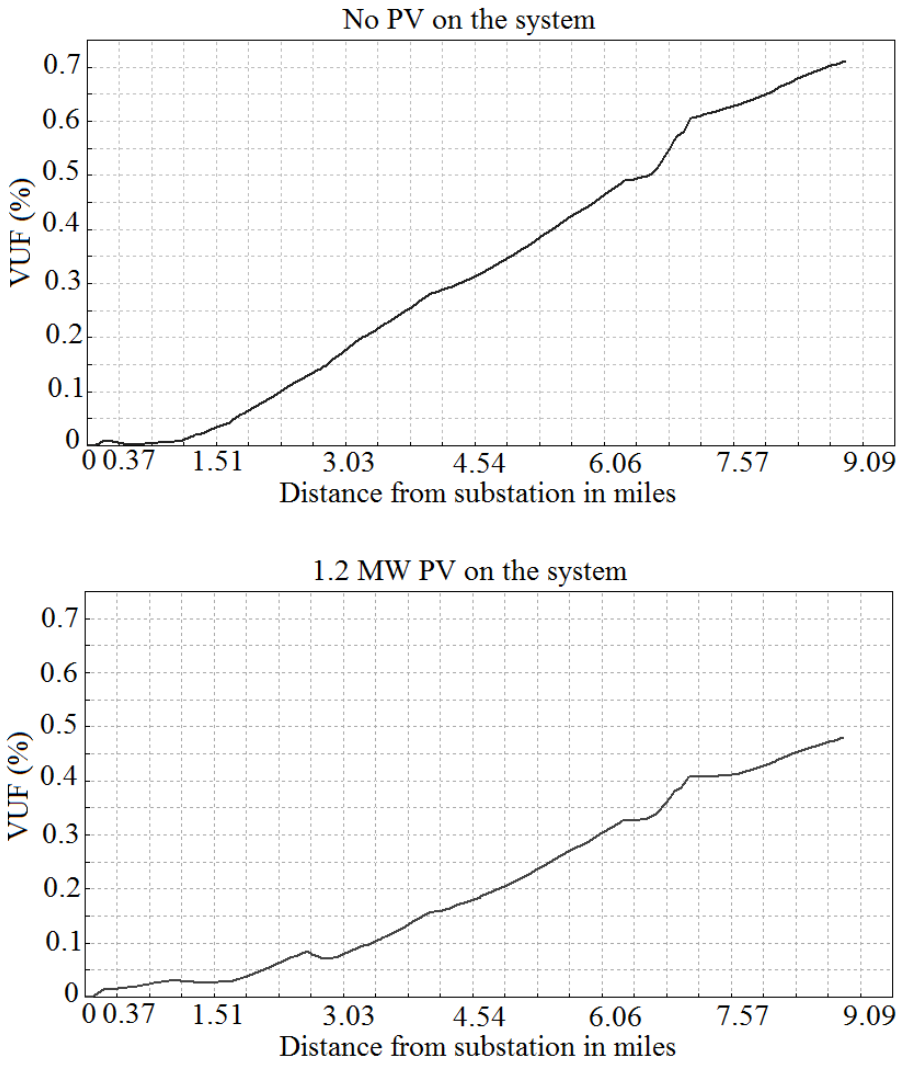

Figure 2.8 VUF (%) along the main feeder for Case I

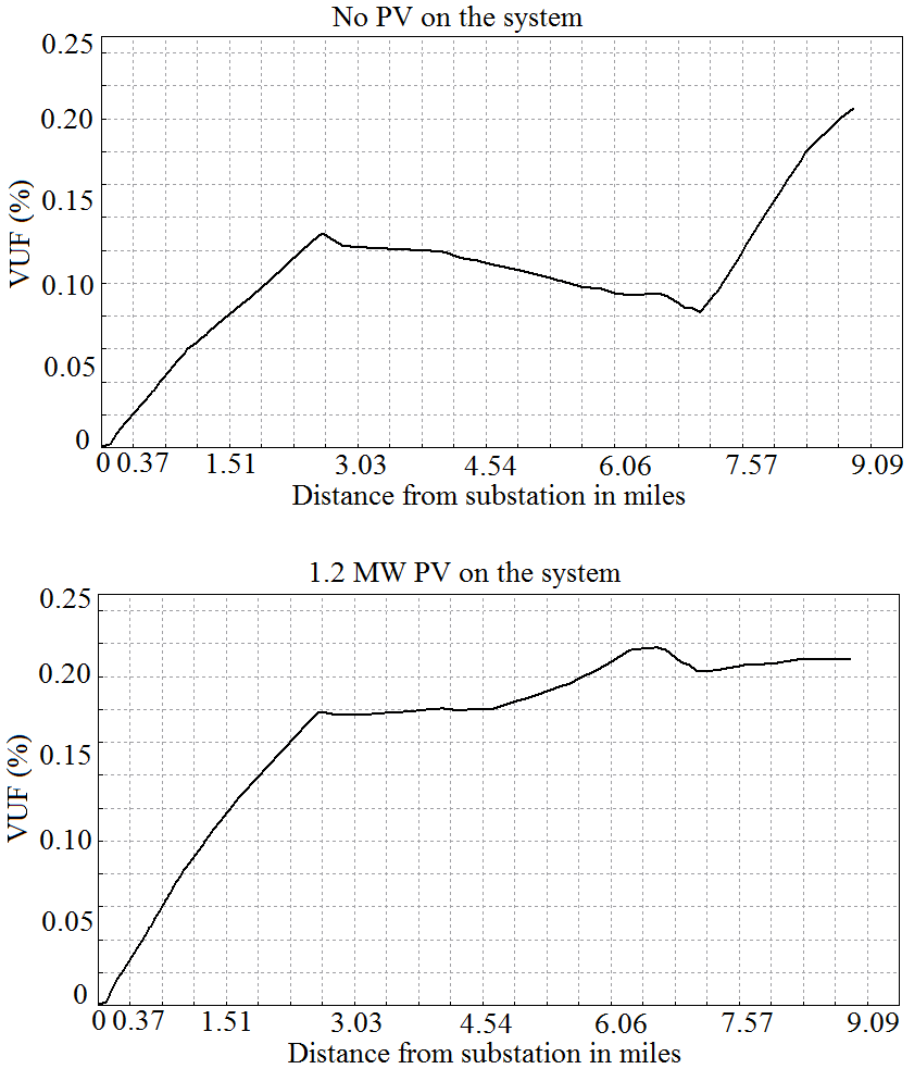

Figure 2.9 VUF (%) along the main feeder for Case II

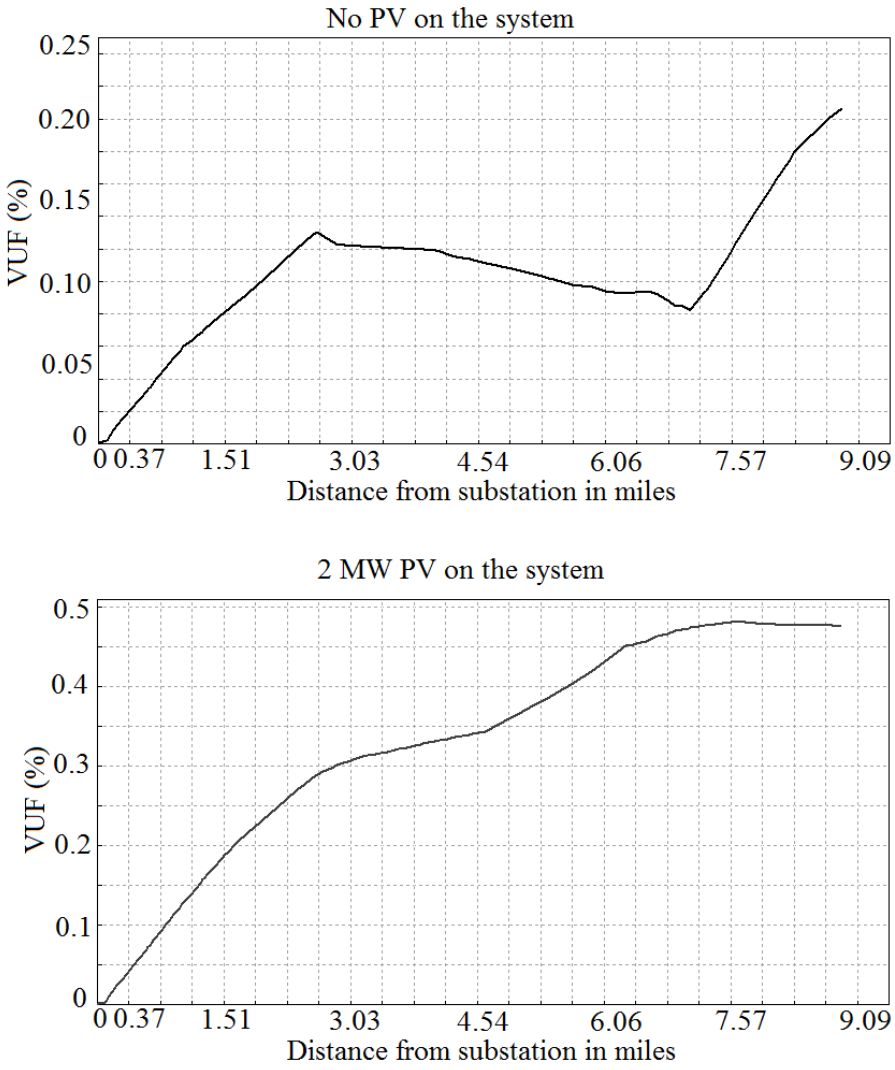

Figure 2.10 VUF (%) along the main feeder for Case III

2.7 Effect of distributed PV on distribution system primary losses

In this section, the effect of distributed PV generation on the primary losses of the test distribution system is studied. Although the no-load losses of the transformers are a part of the distribution system primary losses, these are not included in this study as the actual values were not available during this time. The

comparison results would remain unaffected by the exclusion of transformer no-load losses as these values do not change with the variation in the PV penetration or the loading of the system. For calculating the losses, CYMDIST divides the line into a number of sections and the tip of the spikes, as shown in the plots, gives the losses in kW on the particular section. The total loss on the main feeder can be estimated by summing the losses on each section.

Figure 2.11 shows the plot of line losses on the different sections of the main feeder for Case I. During heavy load conditions, as seen from Figure 2.11, there is a significant effect on line losses as distributed PV generation is included in the system. A comparison of the plots in Figure 2.11 shows that the maximum reduction in line loss for a section in the main feeder is about 3 kW. The total loss in the distribution grid without the inclusion of PV is 176 kW in this scenario. Integrating 1.2 MW of PV in the system reduces the losses by 59 kW and the total loss with PV in the system is 117 kW.

Figure 2.12 shows the plot of line losses on the different sections of the main feeder for Case II. From Figure 2.12, it can be observed that, for a lightly loaded condition, the line losses decrease on the feeder sections as 1.2 MW of distributed PV generation is included in the system. From a comparison of the plots in Figure 2.12, it can be seen that the reduction in line losses is not significant as the lines are lightly loaded to begin with and the feeder losses are less. The total line loss in the entire distribution system including the lateral feeders is 24.6 kW

without the inclusion of PV, including 1.2 MW of distributed PV reduces the total losses to 15.9 kW.

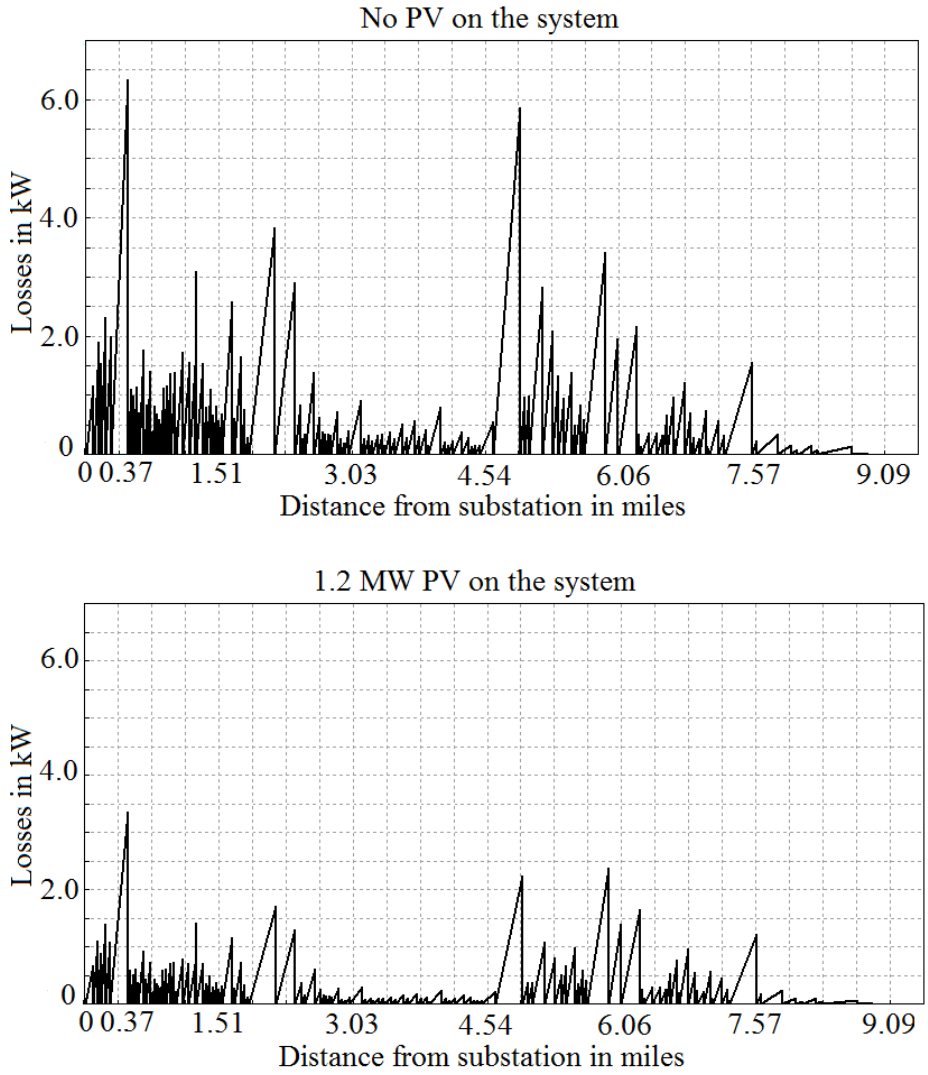

Figure 2.11 Distribution system primary losses along the main feeder sections for Case I

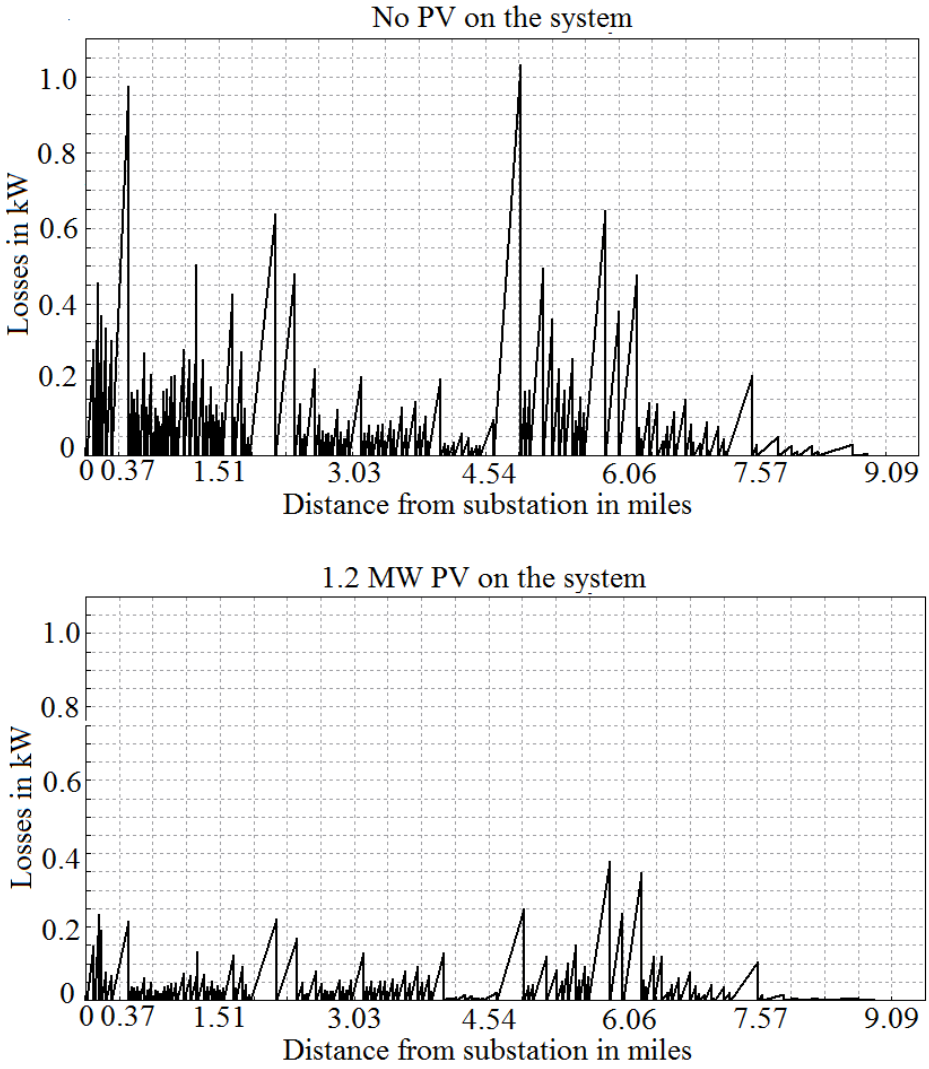

Figure 2.12 Distribution system primary losses along the main feeder sections for Case II

Figure 2.13 shows the line losses on the different sections of the main feeder for Case III. From a comparison with figure 2.12, it is seen that as the PV generation increases from 1.2 MW to 2 MW there is an increase in the kW loss on various feeder sections of the main feeder. The total kW loss increases from 15.9 kW to 23.9 kW when an additional 0.8 MW PV generation is added to the system.

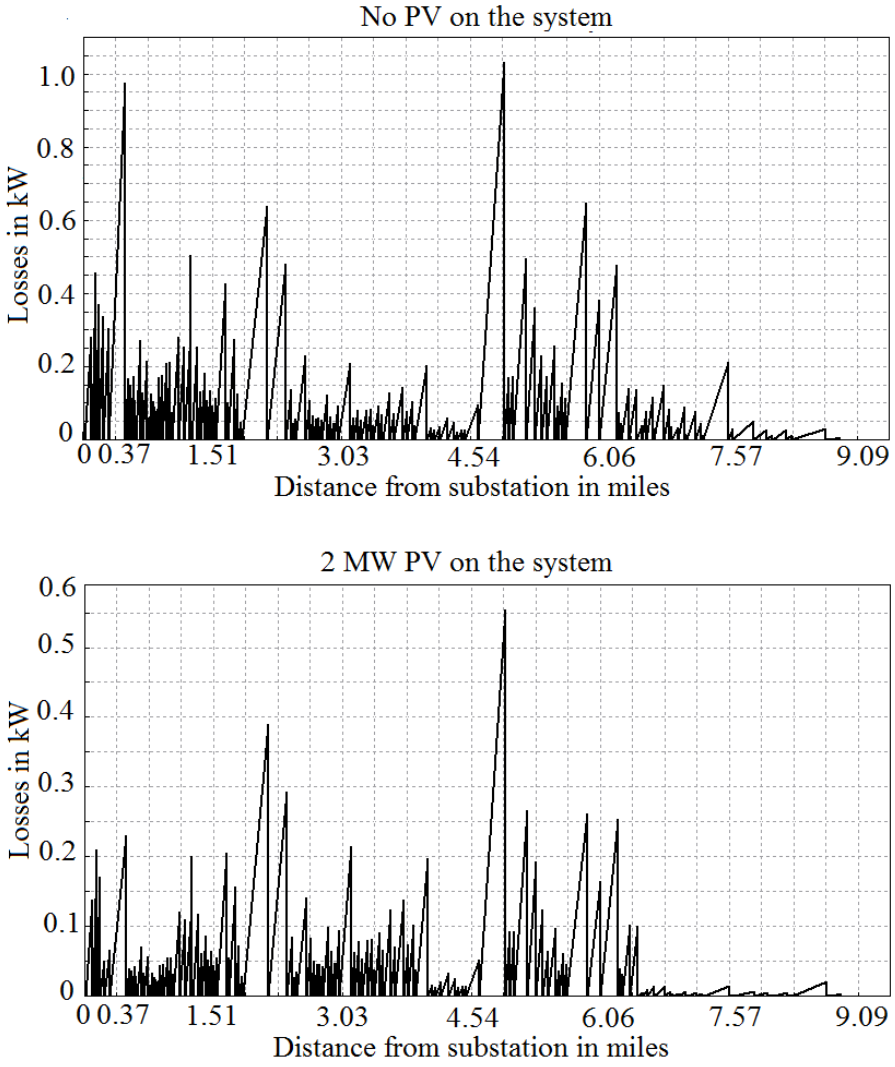

Figure 2.13 Distribution system primary losses along the main feeder sections for Case III

With the inclusion of distributed PV, the generation exists closer to the load resulting in reduced active power flow on the main distribution feeder. The decrease in the active power flow in the line causes a substantial reduction in line losses. However, in Case III, when the system is lightly loaded increasing the PV

penetration level causes reversal of power flow in the system, the reverse power flowing in some sections of the feeder results in increased losses in the system.

2.8 Brief summary of the results

The power flow analysis results indicate that introduction of distributed PV generation up to a moderate level result in better voltage regulation and reduced primary losses in the test distribution system. The effect of distributed PV on voltage unbalance is somewhat different. At low penetration levels, the distributed PV generation reduces the line voltage drop and improves the voltage unbalance. However, as the penetration level increases, due to the unequal distribution of single-phase PV units, the voltage unbalance is seen to increase in the middle section of the test distribution feeder.

A high penetration level of distributed PV has some adverse impacts on the test system. The reversal of power flow due to surplus generation result in overvoltages at some distributed PV locations and increased primary losses in some sections of the feeder, as compared to the cases with low to moderate level of PV penetration. The voltage unbalance is found to increase, with the addition of single-phase PV units, as these units are distributed unequally on different phases and subsequently cause unequal voltage rise.

Chapter 3. Modeling of three phase grid-tied PV inverter

3.1 Introduction

Photovoltaic panels upon insolation produce a dc current output. The dc output is converted to ac for further connection to the transmission and distribution system using an inverter. The inverter may be single-phase or three-phase depending on the size of the PV generation unit. The advent and growth of large-scale PV systems in the range of 10 kW to a few MW has increased the importance three-phase, grid-tied inverters. The grid-tied inverters have additional controllers like anti-islanding controls and maximum power point tracking (MPPT) control to comply with the grid interconnection standards and to account for the electrical characteristics of the PV panels. References [31], [39] and [40] provide the necessary compliance conditions for grid-tied inverters connection with the grid. These inverters may or may not be capable of operating as standalone units based on the type of control implemented.

With an increased proliferation of PV generation sources in transmission and distribution systems, it has become important to develop models of these devices for computer simulation studies. Power electronic devices due to the presence of solid-state switches, which have non-linear characteristics, present a considerable challenge to modeling and simulation. Although a complete switching model of an inverter captures the behavior of the solid-state switches and the ripple in current and voltage waveforms, the simulation time may be very long, with large amounts of output data. This may obscure the given phenomena of interest

[41]. At frequencies significantly lower than the switching frequency, the network can be modeled by an average model [42], [43]. At the grid interconnection level, representing the switching devices by their average characteristics is adequate. This is the case for studies involving the operation of inverters in response to grid events such as faults, voltage sags, voltage swells and islanding. Presently, many software packages are available for modeling power electronic devices. As examples, SPICE [44] and EMTP [45] are the most widely used simulators in the industry. While SPICE is highly effective for analysis of power electronic devices at the circuit level, EMTP is better suited for simulating high power electronics in power systems. At the higher power levels for power systems (e.g., P > 1 MW), the switching devices can be represented by ideal switches and the controllers by transfer functions and logical expressions [41]. In addition, the availability of detailed transmission line models, transformer models and load models make EMTP a suitable choice for simulating grid-tied inverters while analyzing them as power sources in a grid. In the work presented in this thesis, the anti-islanding study of a three-phase grid-tied inverter is performed in PSCAD / EMTDC, which is an EMTP type simulator [45]. The individual components of the inverter are modeled in PSCAD / EMTDC using FORTRAN programming language. The basis of the approach is given in the guidelines provided by the PSCAD / EMTDC manual [46]. The FORTRAN codes for several typical components can be found in Appendix A. In the following sections, a brief descrip-

tion of the grid-tied inverter and the different components modeled for anti-islanding analysis are presented.

3.2 Switching model and average model of an inverter

The input to a PV inverter is ideally a regulated dc voltage source and the output filters could be L, LCL, or LC filter and a transformer, with or without harmonic filters. In the model used for this study, the input to the inverter is considered as an ideal dc voltage source and the output filter is an L (only) filter. Figure 3.1 shows the switching model of a grid-tied inverter. Though a switching model enables accurate representation of the discrete switching behavior, it takes a long time to simulate and is not suitable for small signal analysis. The corresponding cycle-by-cycle average model, also referred to as the average model of the inverter is shown in Figure 3.2.

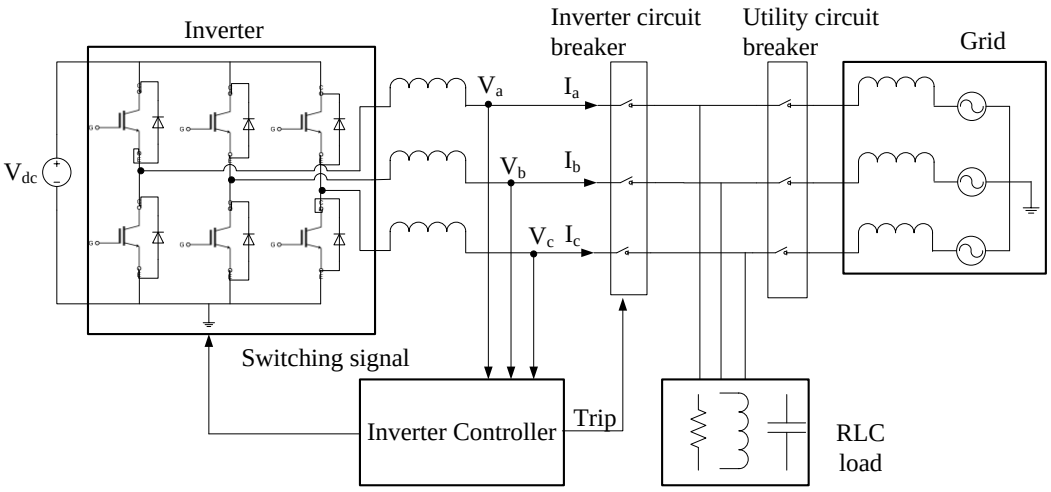

Figure 3.1 Switching model of a grid-tied three-phase inverter [47]

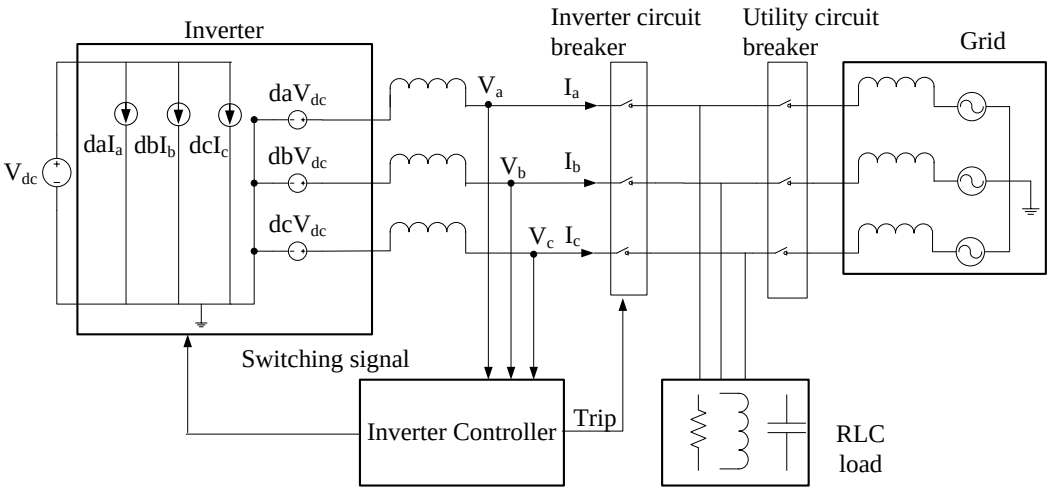

Figure 3.2 Average model of a grid-tied three-phase inverter [47]

In a cycle-by-cycle average model, the switching network is represented by controlled voltage and current sources with averaged switching duty cycle and the controller action is represented by continuous functions like proportional (P) or proportional integral (PI), instead of actual discrete functions. The average model, due to its simplified representation of switching devices and controllers takes lesser time to simulate and is suitable for small signal analysis [47].

3.3 Control block design

Grid-tied inverters operate in two basic control modes: constant current control and constant power control. In this study, a constant current controlled inverter has been considered and the results of the study can be easily extended to constant power controlled inverters. The constant current control could be im-

plemented in an ABC (stationary) frame, $\alpha\beta$ (stationary) frame [48], or a *dq* (synchronously rotating) frame [49], [50]. In this work, a *dq* implementation is used, which is more popular in modern digitally controlled inverters [47]. Figure 3.3 shows a block diagram of the current control block developed for the study. The key functional components of the current controller are the ABC/*dq* to *dq*/ABC co-ordinate transformation block, the phase locked loop (PLL), and the type II controller.

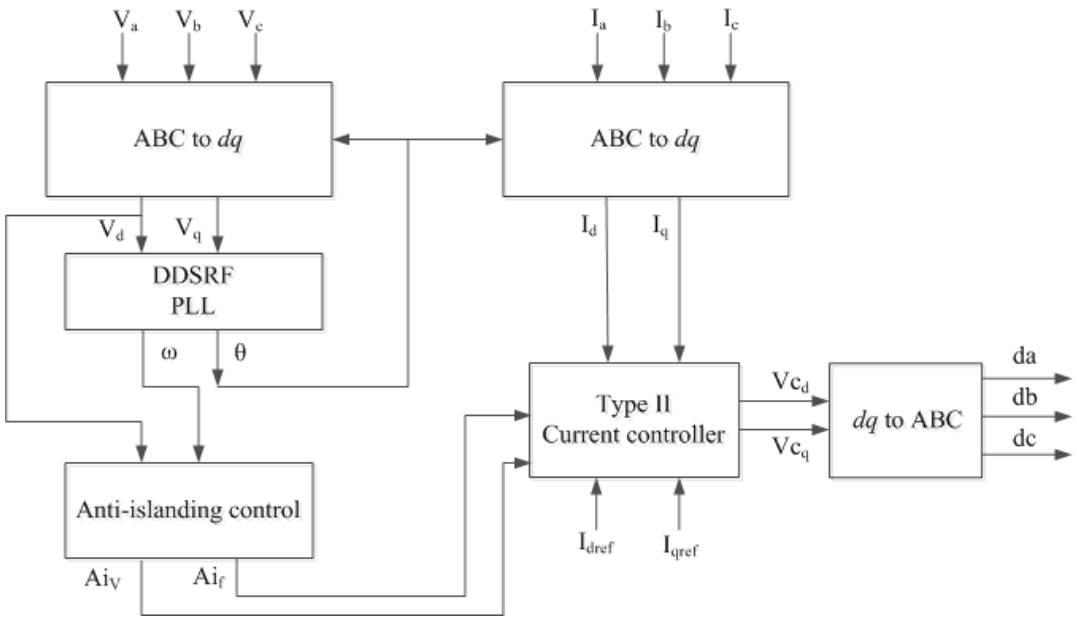

Figure 3.3 Block diagram of the current control block

Coordinate transformation block

The coordinate transformation block is used to implement the inverter control in the *dq* reference frame. The Park's transformation [49],[50], given by (3.1) is used in this block to convert the inverter terminal voltage and current from the ABC (stationary) frame of reference to the *dq* (synchronously rotating) frame. The inverse of Park's transformation is used to generate the duty cycles for phases A, B and C from the output of the controller, which are in the *dq* frame.

$$[T] = \frac{2}{3}\begin{bmatrix} cos\,\theta & cos(\theta - \frac{2\pi}{3}) & cos(\theta + \frac{2\pi}{3}) \\ sin\,\theta & sin(\theta - \frac{2\pi}{3}) & sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{3.1}$$

Phase locked loop

A PLL is a closed loop controller, which detects the phase of an input periodic signal and generates an output signal whose phase is related to the input signal [51]. A PLL is used in grid-tied inverters to synchronize the inverter with the grid when they are brought online. In the controller used, the phase locked loop takes the grid voltage as an input and gives the frequency and phase angle of the grid voltage as the output. A variety of techniques can be used to design a PLL [51], but irrespective of the algorithm, a PLL should be able to detect the phase correctly even with distortion in the grid voltage. In this work, a decoupled double synchronous rotating frame (DDSRF) PLL is used. A DDSRF based PLL uses an unbalanced voltage vector, with both positive and negative sequence

components and expresses it on a double synchronous rotating frame, to detect the phase of the positive sequence component of the input voltage vector [51], [52]. A DDSRF PLL is chosen for this work, as the distribution system voltages are often unbalanced due to the presence of single-phase loads or single pole operation of reclosers. A block diagram of the DDSRF PLL is shown in Figure 3.4.

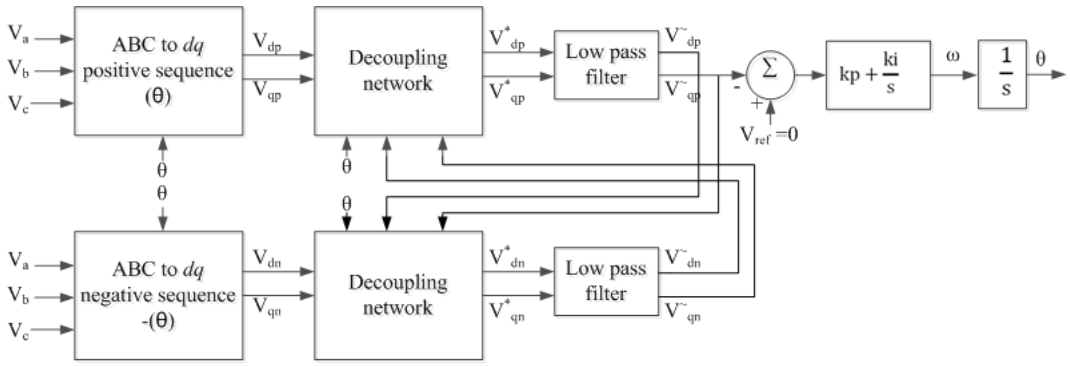

Figure 3.4 Block diagram of DDSRF PLL [52]

Current controller

The current controller is designed using the K-factor approach [41] and is modeled in a *dq* frame of reference. A detailed discussion of the controller design and implementation can be found in [53]. The current controller modeled has a bandwidth of 1 kHz and a phase margin of the 60°. As the phase boost needed for the controller transfer function is less than 90°, a type II controller is used. Figure 3.5 shows the type II controller structure implemented in a *dq* reference frame. The *d*-axis current reference controls the active power and the *q*-axis current reference controls the reactive power injected or absorbed by the inverter.

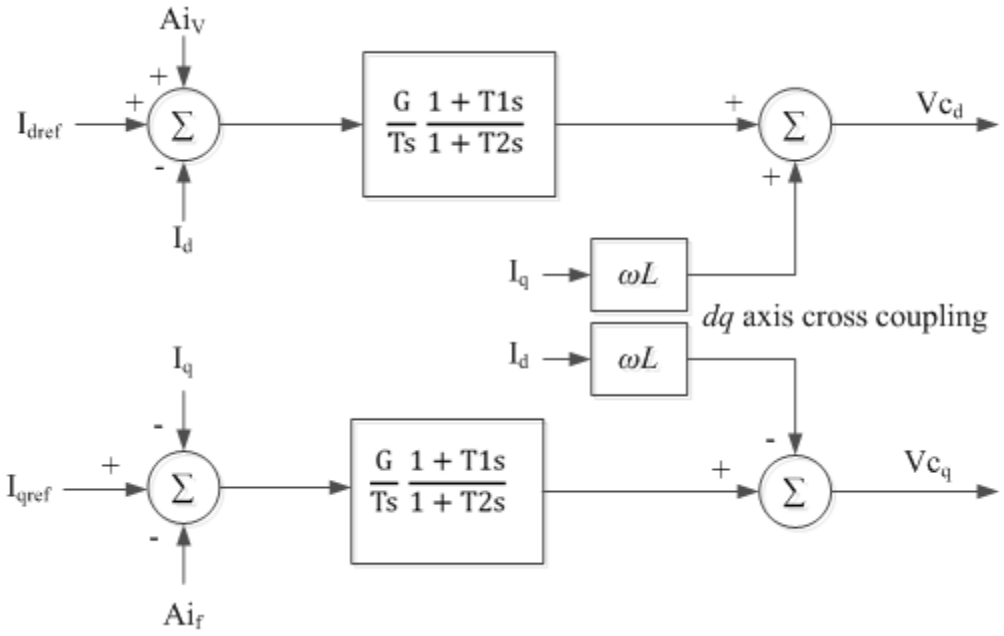

Figure 3.5 Block diagram of the current controller

3.4 Anti-islanding control

As discussed in Chapter 1, active anti-islanding methods have relatively narrow non-detection zones (NDZs), and are superior to the passive methods. The active anti-islanding schemes discussed in this paper are based on positive feedback and *dq* implementation.

For an anti-islanding study, it is a standard practice to represent the local load by a parallel combination of resistance (*R*), inductance (*L*) and capacitance (*C*) connected at the inverter terminals, as shown in Figure 3.1 and Figure 3.2 [31], [39]. The relationships between active/reactive power and voltage/frequency for a parallel-connected *RLC* load, is given by (3.2) and (3.3) respectively,

$$P = \frac{V^2}{R} \tag{3.2}$$

$$Q = V^2(\omega C - (\omega L)^{-1}) \tag{3.3}$$

where, P is the active power supplied by the inverter, Q represents the reactive power flowing into the inverter, V is the voltage across the *RLC* load and ω is the system angular frequency in rad/s. Based on this load representation, the two anti-islanding algorithms are briefly discussed as follows.

Voltage based positive feedback

Figure 3.6 shows the *dq* implementation of the voltage based positive feedback scheme [47]. When a voltage rise is sensed at the inverter terminals, a positive feedback signal is generated which increases the inverter active power output. For a constant impedance load, due to the load characteristic given by (3.2), an increase in active power injected causes the voltage across the load to increase. The positive feedback eventually drives the voltage beyond the nominal range, leading to island detection. A similar phenomenon occurs in the opposite direction if an initial voltage dip is detected. In a *dq* control frame, for a VSI operating in a current control mode, the positive feedback signal is fed to the *d*-axis current, which controls the active power output.

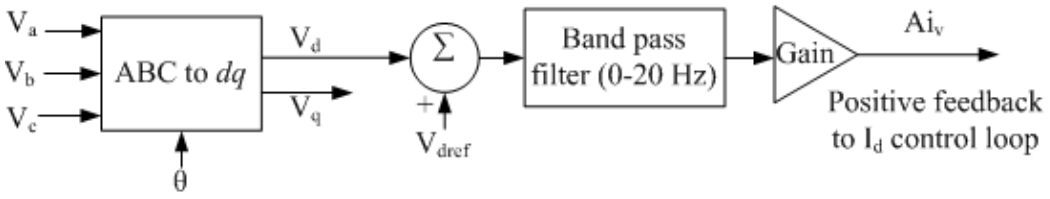

Figure 3.6 Voltage based positive feedback in *dq* reference frame

Frequency based positive feedback

Figure 3.7 shows the *dq* implementation of a frequency based positive feedback scheme [47]. When the inverter controls senses an increase in frequency at its terminals, a positive feedback is generated which increases the reactive power absorbed by the inverter. For a constant impedance load, due to the load characteristics given by (3.3), an increase in reactive power absorbed, causes the frequency to increase further. The positive feedback eventually drives the frequency out of the nominal limits resulting in island detection. An initial frequency dip would result in a similar destabilization in an opposite direction. In the *dq* control frame, for a VSI operating in a current control mode, the positive feedback is fed to the *q*-axis current, which controls the reactive power output.

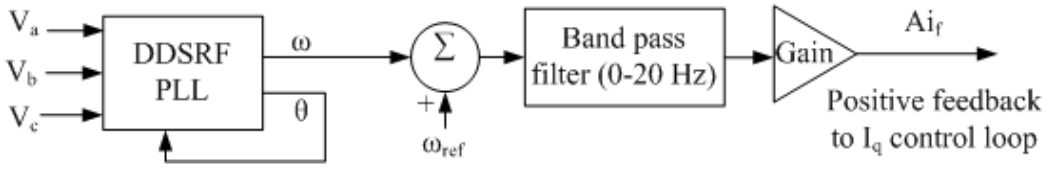

Figure 3.7 Frequency based positive feedback in *dq* reference frame

3.5 Voltage and frequency excursion detection

The overvoltage / undervoltage and the overfrequency / underfrequency relay for inverter anti-islanding detection are simulated using simple comparators and logical gates. Figure 3.8 shows the block diagram of the overvoltage / undervoltage and the overfrequency / underfrequency relay. The voltage and fre-

quency comparator sends a trip signal when the measured value of the peak line-neutral voltage (which is the direct axis voltage in the *dq* reference fame) or the frequency is beyond the threshold limits. The trip signal sets the inverter duty ratio to zero and simultaneously opens the inverter circuit breaker as shown in Figure 3.1 and Figure 3.2. The threshold values of frequency and voltage are set according to [31], [39]. Table 3.1 provides the voltage and frequency threshold values used to generate the trip signal.

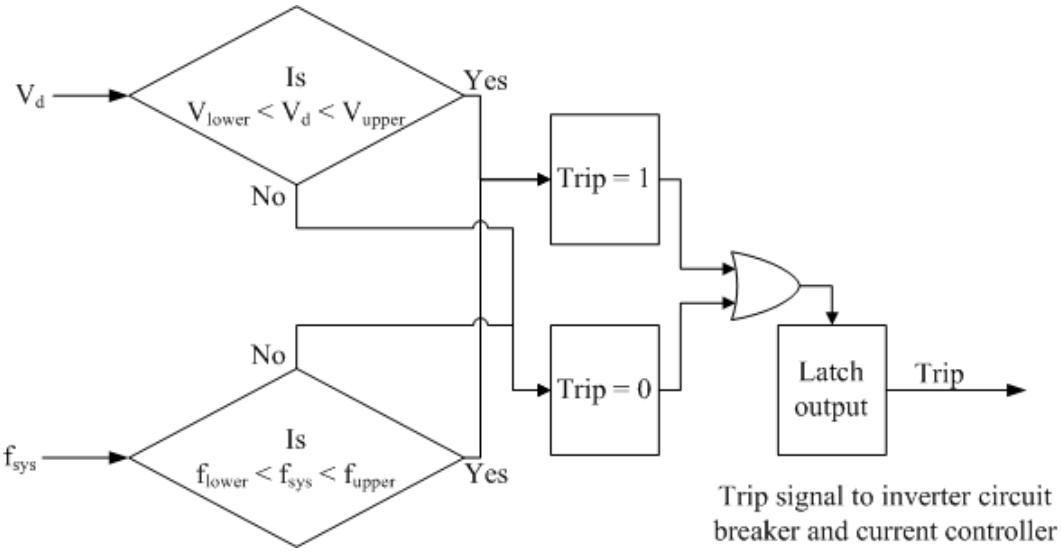

Figure 3.8 Block diagram of overvoltage / undervoltage and overfrequency / underfrequency relay

Table 3.1 Voltage and frequency thresholds

Voltage threshold	Upper limit	±431.11 V (Line-neutral peak)
	Lower limit	±344.8 V (Line-neutral peak)
Frequency threshold	Upper limit	60.5 Hz
	Lower limit	59.3 Hz

As the active islanding method works on the principle of forcible destabilization of voltage and frequency at the inverter terminals, the voltage and frequency may return to normal values after the inverter is disconnected. To prevent the resetting of the trip signal a lockout function or latch is simulated, which prevents the trip signal from resetting if the voltage and frequency values return to normal after disconnection of the inverter.

3.6 Summary

This chapter presents a brief discussion of the key components of a three-phase grid-tied inverter that were modeled for the present study. A brief description of the island detection methods and their implementation in the *dq* frame are also provided in this chapter. The models of the individual components were created using the FORTRAN script in PSCAD/EMTDC. The inverter model described herein is used in the following chapter to study the performance of the anti-islanding controls under three envisaged operating scenarios.

Chapter 4. Anti-islanding study: time domain simulation

4.1 Islanding in power distribution systems

One of the prominent technical issues associated with grid interconnection of distributed photovoltaic (PV) generation is that of islanding. Islanding refers to off-grid operation of the distributed generation plus its nearby load(s), often following a disturbance. Figure 4.1 shows an islanded distribution system, disconnected from the grid and being supplied by local DG sources. Although PV generators can continue to supply loads in an island, operating under such conditions may lead to degradation of power quality and safety hazards [19], [31], [39], and [40]. The IEEE 1547 [31] standard requires a distributed generator (DG) to detect and disconnect from the system within 2 seconds of island formation. The IEEE 929 standard further documents islanding, as applied to PV systems [39]. References [39], [40] provide the minimum test procedure for non-islanding PV inverters. To comply with the present standards, most grid connected PV inverters are equipped with anti-islanding controls.

In this chapter, the effectiveness of two active anti-islanding methods, voltage based positive feedback [47] and frequency based positive feedback [47], are studied. A test system, representing an actual distribution system with two utility scale inverters is simulated. A brief description of the system, the cases considered and the simulation results are presented in the following sections.

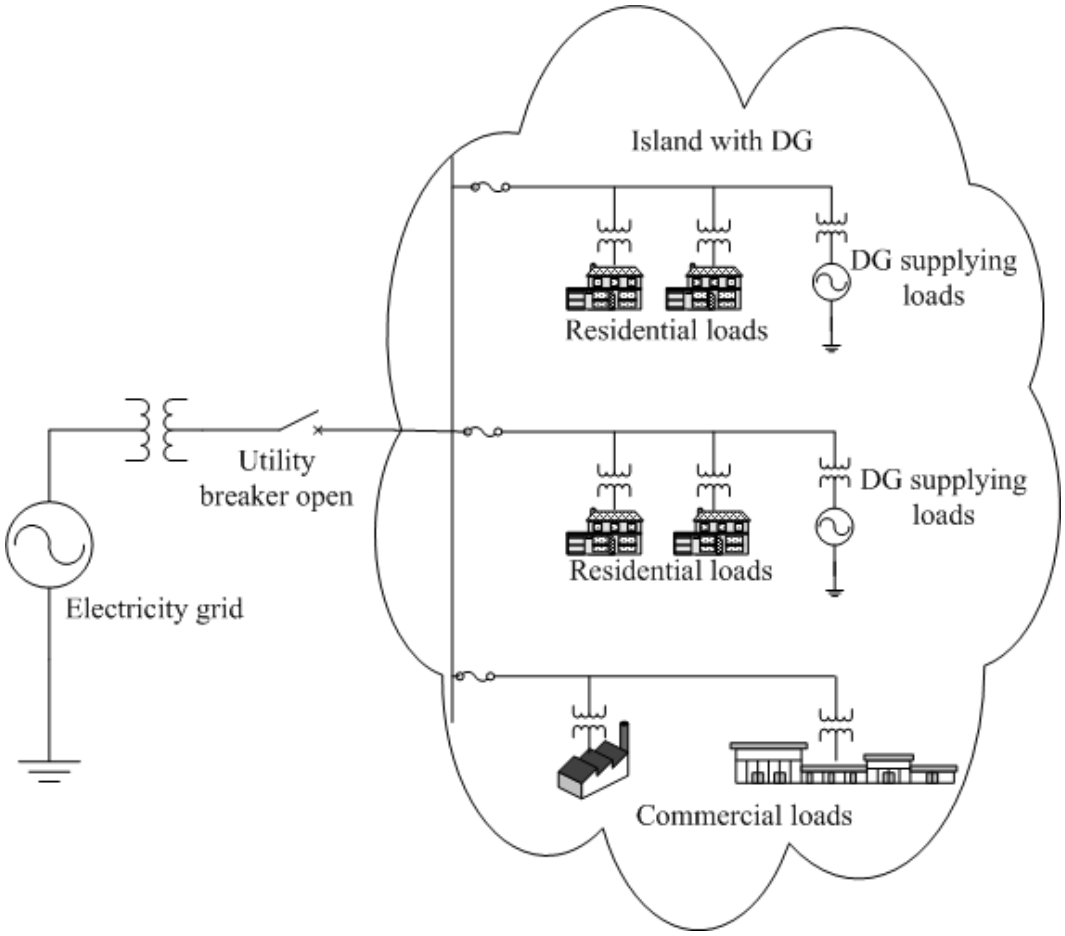

Figure 4.1 An islanded distribution system with DG sources supplying local loads

4.2 System description

Figure 4.2 shows the test distribution system modeled in PSCAD, used for this study. The test system modeled here is the same test distribution feeder that was previously introduced in Chapter 2. For an anti-islanding study, it is adequate to represent the local loads and shunt capacitors as aggregated parallel connected *R*, *L* and *C* [31], [39]. In accordance with this assumption, the loads in the system are represented as groups of parallel-connected *R*, *L* and *C*. The utility grid is represented by a voltage source supplying a line-to-line voltage of 12.47 kV at 60 Hz. Opening the recloser REC leads to the formation of an island as shown in Figure 4.2. PV inverters, INV 1 and INV 2 are connected to the test system through 0.48 kV/ 12.47 kV transformers, T1 and T2 respectively. The inverter INV1 is rated at 500 kW and INV 2 is rated at 400 kW. As per the IEEE 1547 standard [31], the inverters are operated at unity power factor and supply only active power.

4.3 Analysis approach

With a high penetration of PV generation in this system, a worst-case operating condition for islanding detection is encountered when the local generation and the load match closely. In this condition, the active and reactive power flow through the recloser REC is close to zero. In the absence of any active anti-islanding mechanism, opening the recloser REC does not cause any appreciable change in the voltage or frequency at the PCC, thus inhibiting island detection by passive methods

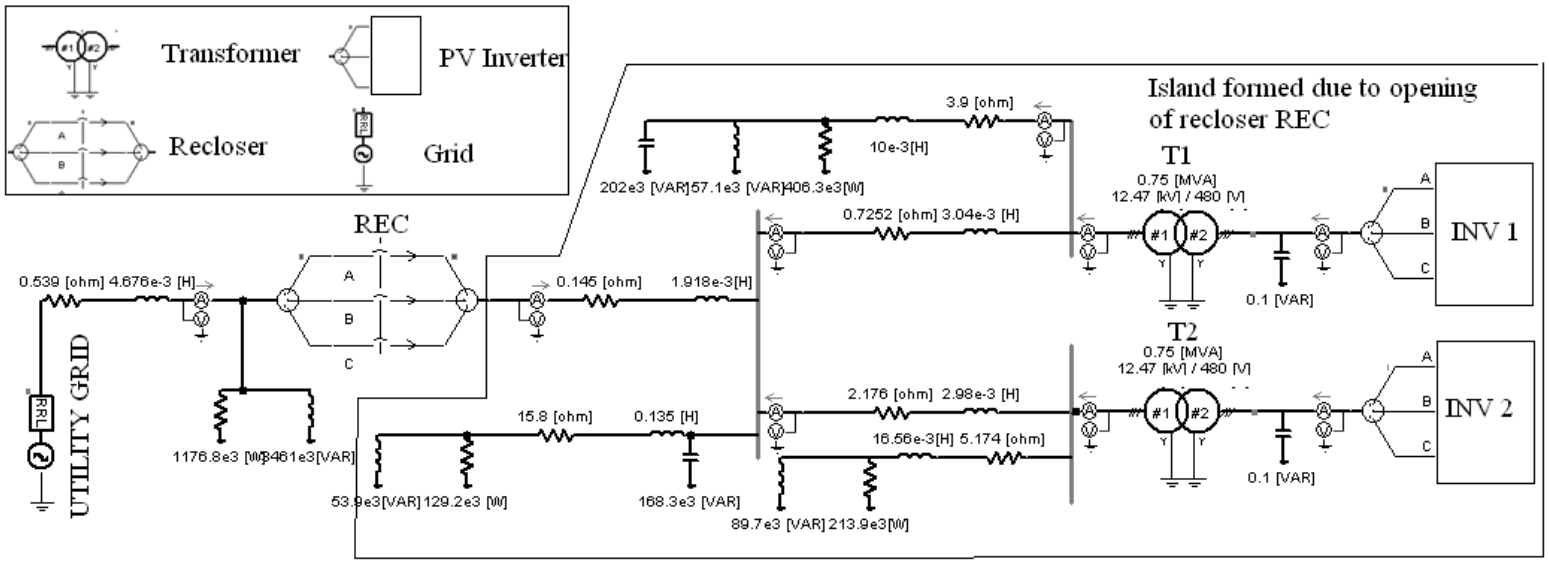

Figure 4.2 Test distribution system modeled in PSCAD

. To simulate a similar operating condition, the inverter active power outputs and the shunt capacitor reactive power outputs are adjusted to match the active and reactive power consumption within the island. A summary of the load and generation in the island is given in Table 4.1. The active and reactive power losses in the network account for the difference in load and generation values.

Table 4.1 Load and generation summary within the island

Active power consumed	Reactive power consumed	Reactive power generated	Active power generated	
			INV1	INV 2
750 kW	306 kVAr	370 kVAr	460 kW	355 kW

In the test distribution system, from an island detection perspective, two distinct scenarios may be encountered based on the operation of the recloser REC. The first scenario is a normal operation of the recloser REC, when all three phases open. The second scenario is a faulty operation of the recloser REC, when one or two of the three phases fail to open. Operating a grid tied inverter in either scenario may damage any sensitive equipment connected to the system or the inverter itself. It is desirable that the inverter anti-islanding controls detects all such situations and disconnects the inverter from the grid. To study the effectiveness of the discussed anti-islanding schemes three different cases have been considered. These three cases encompass the discussed possible scenarios that could be encountered. The cases considered are as follows:

- Case I: All three phases of the recloser REC opens

- Case II: Two phases of the recloser REC opens and one phase fails to open
- Case III: One phase of the recloser REC opens and two phases fail to open

4.4 Case I: All three phases of the recloser REC opens

Consider the case where all three phases of the recloser REC opens. To simulate this case, after the initial transients settle down and a steady state is reached, the recloser REC is opened at time 10 seconds.

Active feedback scheme disabled at both inverters

Figure 4.3 and Figure 4.4 show the line-to-neutral voltages at the terminals of inverter INV1 and the system frequency, respectively, after the recloser REC operates. With active island detection scheme disabled, the inverter fails to detect this condition as the voltage and frequency measured at the inverter terminals remain within the acceptable limits. The inverters thus continue to energize the island in this case.

Active feedback scheme enabled at both inverters

Figure 4.5 shows the system frequency after the recloser REC operates, when frequency based positive feedback is enabled at both inverters. The positive feedback signal drives the system frequency beyond the upper threshold of 60.5 Hz [31]. This over frequency condition is detected by the over/under frequency relay, which disconnects the inverter from the system. As shown in Figure 4.6, the islanding condition is detected in 35 ms and the inverter disconnects from the grid.

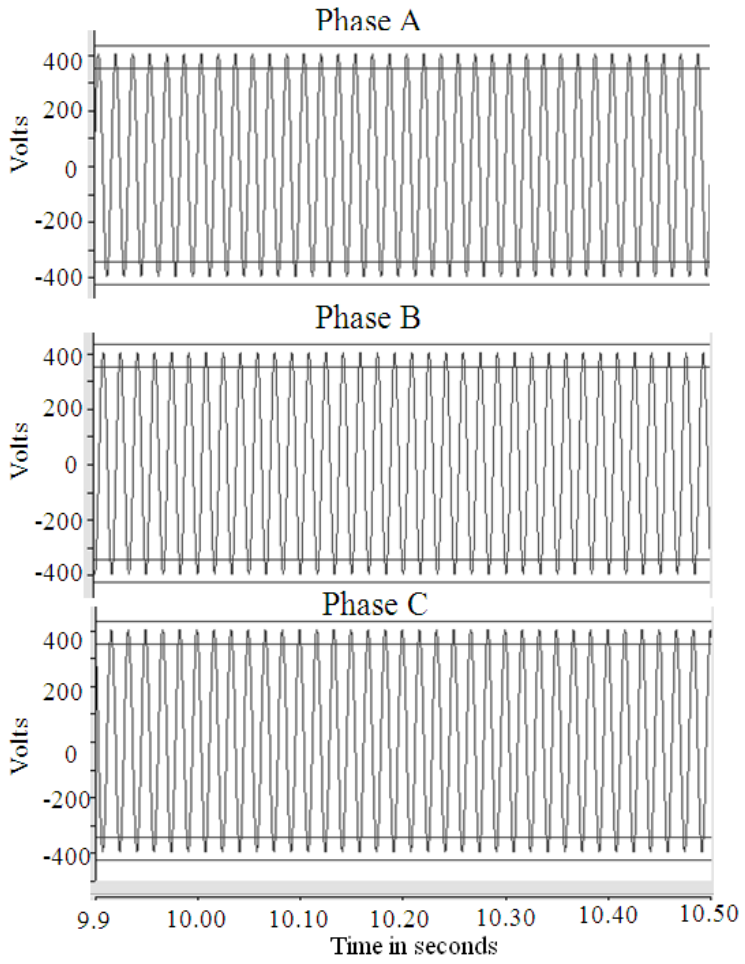

Figure 4.3 Line-to-neutral voltages at the terminals of inverter INV 1 with active island detection disabled

Figure 4.7 shows the line-to-neutral voltages at the terminals of inverter INV 1, after the recloser REC operates, when voltage based positive feedback is enabled at both inverters. The positive feedback signal pushes the terminal voltage of the inverter beyond the upper threshold of 1.1 p.u. or 431.1 V (peak line-to-neutral) [31]. The overvoltage condition is detected by an over/under voltage relay, which disconnects the inverter from the system. As shown in Figure 4.8,

this scheme detects the islanding condition in 35 ms and disconnects the inverter from the grid.

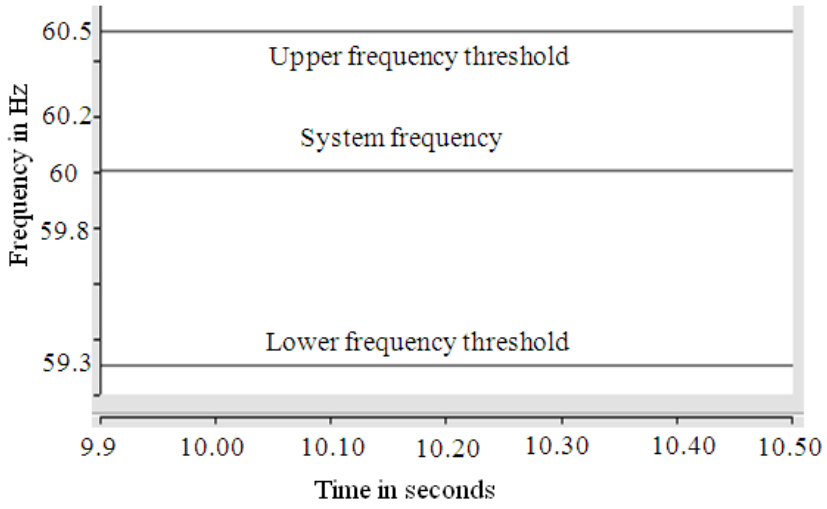

Figure 4.4 System frequency with active island detection disabled

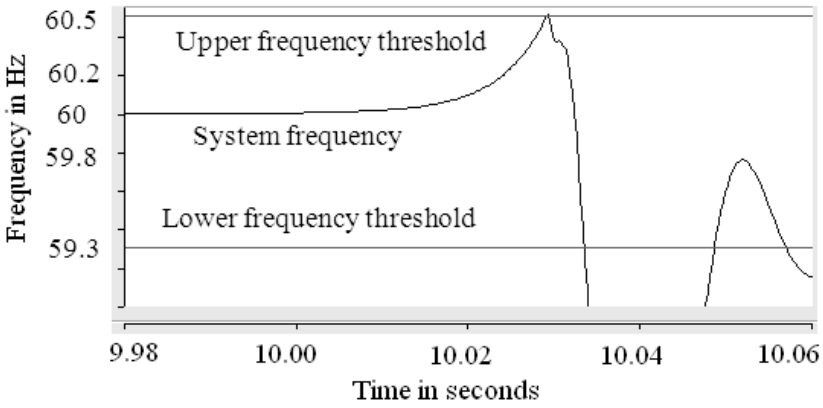

Figure 4.5 System frequency with frequency based positive feedback enabled for Case I

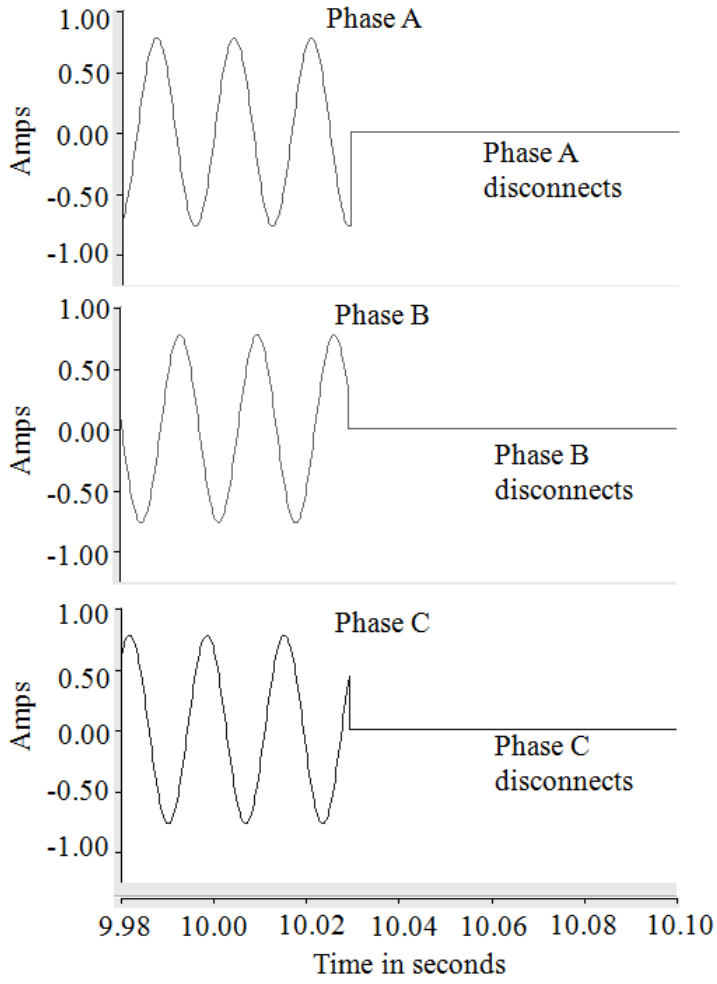

Figure 4.6 Line currents at the terminals of inverter INV 1 with frequency based positive feedback enabled for Case I

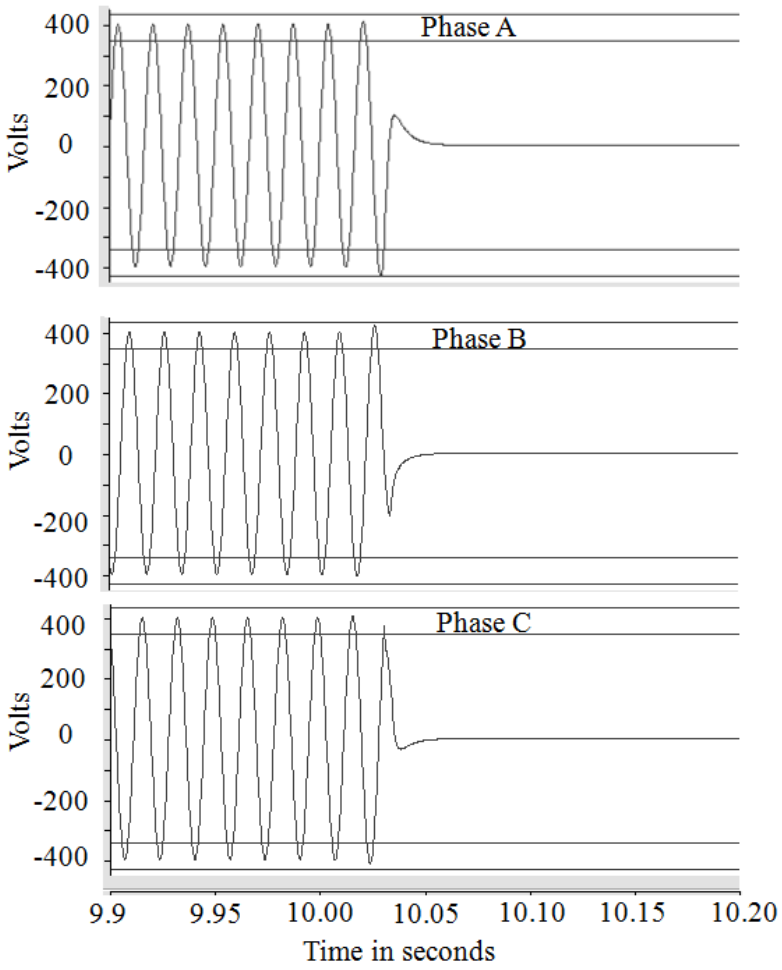

Figure 4.7 Line-to-neutral voltages at the terminals of inverter INV 1 with voltage based positive feedback enabled for Case I

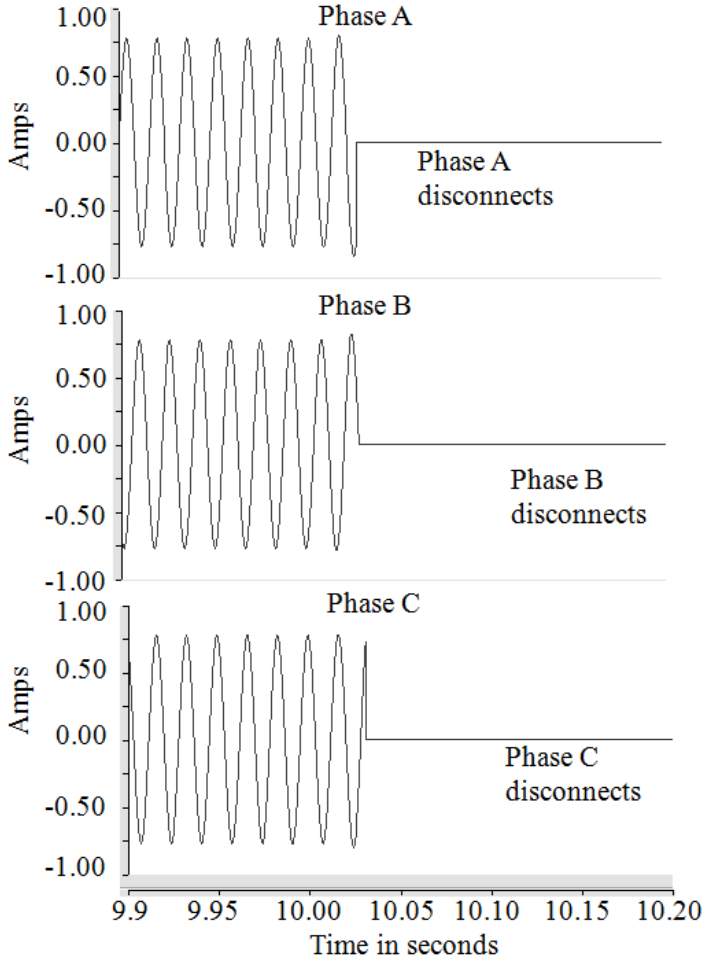

Figure 4.8 Line currents at the terminals of inverter INV 1 with voltage based positive feedback enabled for Case I

4.5 Case II: Two phases of the recloser REC opens and one phase fails to open

Consider the case where two phases of a recloser open but one phase fails to open. To simulate this case, after the initial transients settle down and a steady state is reached, Phases A and B of the recloser REC are opened at time 10 seconds, and phase C is deliberately kept closed.

Active feedback scheme disabled at both inverters

In the absence of any anti-islanding scheme, the inverters fail to detect this condition as the voltage and frequency measured at the inverter terminals, remains within acceptable limits. The inverters do not disconnect from the system and continue to energize the island. The line-to-neutral voltages at the terminals of inverter INV 1 and system frequency, in this case, are identical to those shown in Figure 4.3 and Figure 4.4 respectively.

Active feedback scheme enabled at both inverters

Figure 4.9 shows the system frequency, following a misoperation of recloser REC, when frequency based positive feedback is enabled at both inverters. The positive feedback signal drives the system frequency beyond the upper threshold of 60.5 Hz [31]. This over frequency condition is detected by an over/under frequency relay, which disconnects the inverter from the system. As shown in Figure 4.10, this scheme detects the islanding condition in 60 ms and disconnects the inverter from the grid.

Figure 4.11 shows the line-to-neutral voltages at the terminals of inverter INV 1, following a misoperation of recloser REC, when voltage based positive feedback is enabled at both inverters. The positive feedback signal pushes the terminal voltage of the inverter beyond the upper threshold of 1.1 p.u. or 431.1 V (peak line-to-neutral) [31]. The overvoltage condition is detected by an over/under voltage relay, which disconnects the inverter from the system. As shown in Figure 4.12, this scheme detects the islanding condition in 110 ms and disconnects the inverter from the grid.

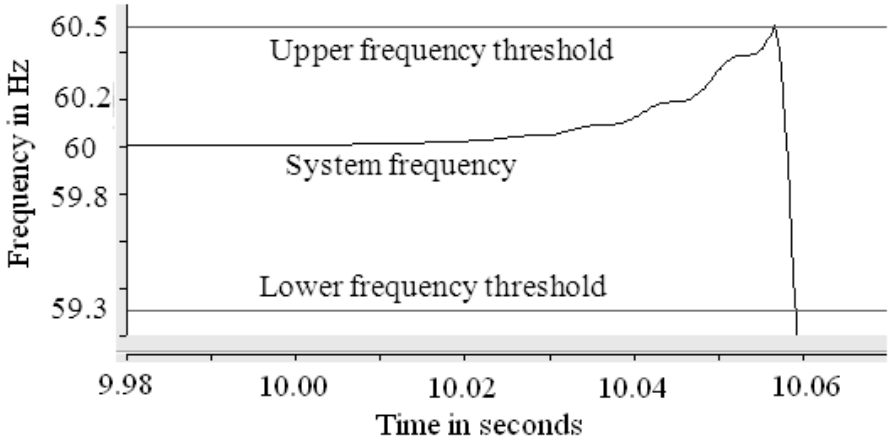

Figure 4.9 System frequency with frequency based positive feedback enabled for Case II

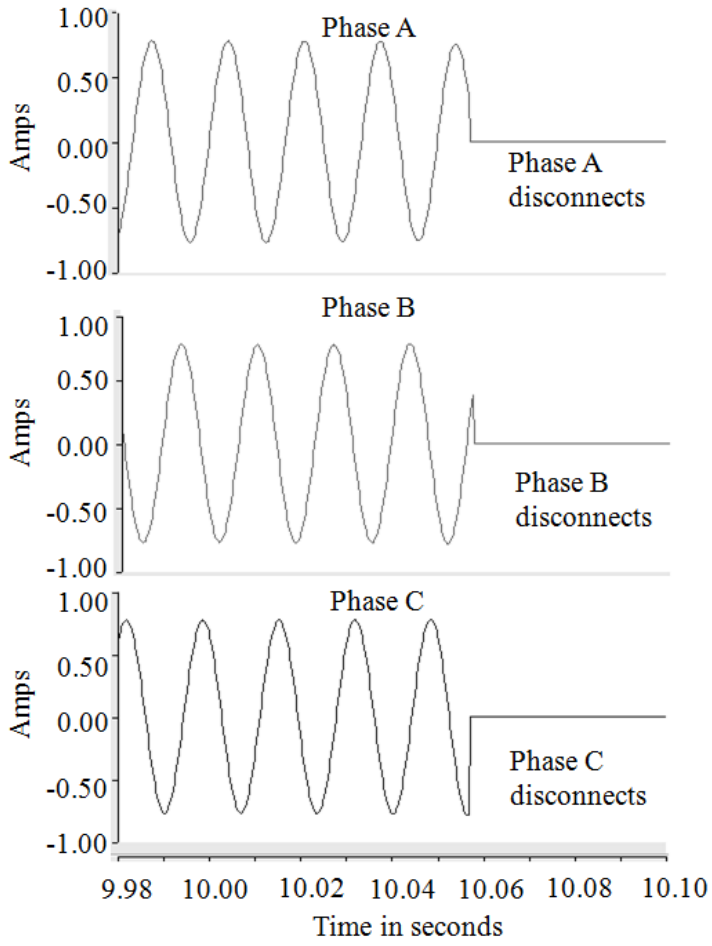

Figure 4.10 Line currents at the terminals of inverter INV 1 with frequency based positive feedback enabled for Case II

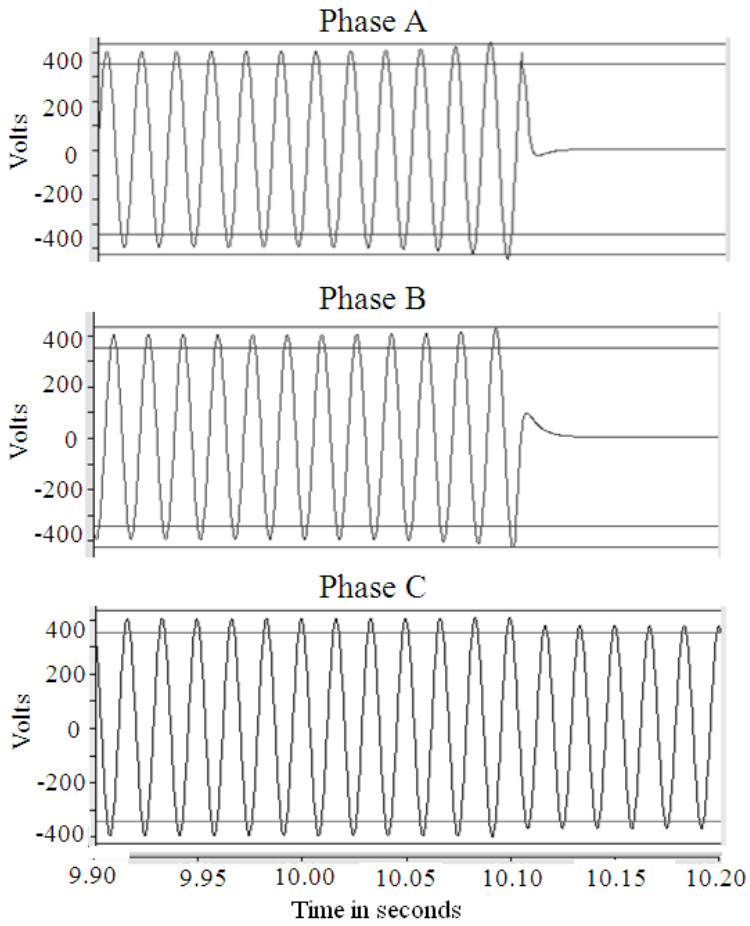

Figure 4.11 Line-to-neutral voltages at the terminals of inverter INV 1 with voltage based positive feedback enabled for Case II

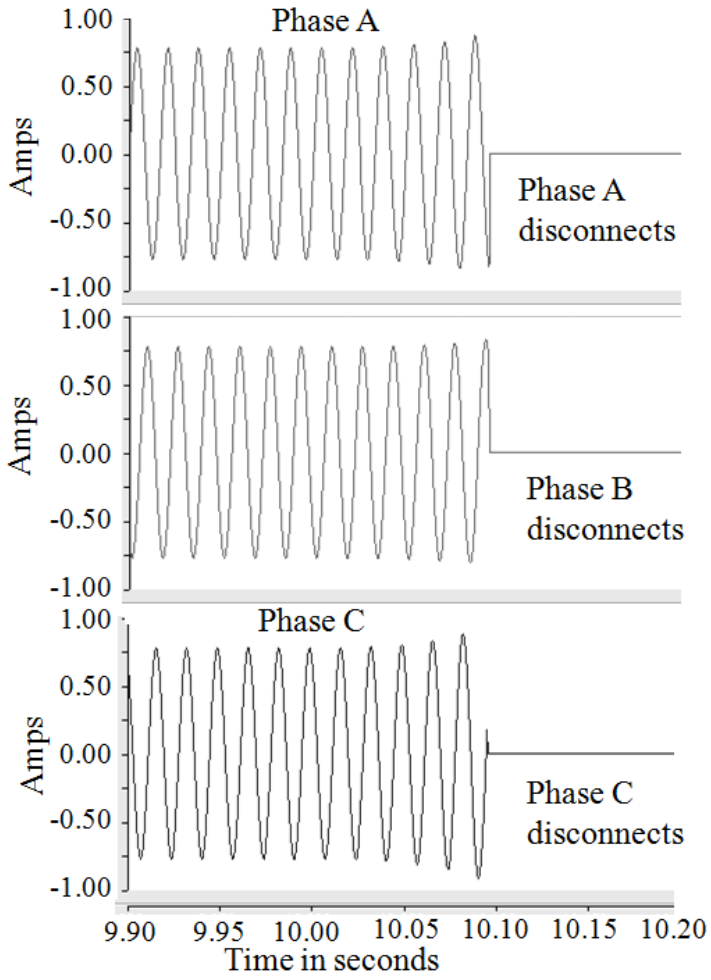

Figure 4.12 Line currents at the terminals of inverter INV 1 with frequency based positive feedback enabled for Case II

4.6 Case III: One phase of the recloser REC opens and two phases fail to open

Consider the case that one phase of a recloser REC opens but the remaining two phases do not open. To simulate this case, after the initial transients settle down and a steady state is reached, Phase A of the recloser REC is opened at time 10 seconds and phases B and C are deliberately kept closed.

Active feedback scheme disabled at both inverters

Without any anti-islanding scheme activated, the inverters fail to detect the recloser operation, as the voltage and frequency measured at the inverter terminals, remains within acceptable limits. The inverters remain connected and continue to energize the island. The line-to-neutral voltages at the terminals of inverter INV 1 and system frequency, in this case, are identical to those shown in Figure 4.3 and Figure 4.4 respectively.

Active feedback scheme enabled at both inverters

Figure 4.13 shows the system frequency following a misoperation of recloser REC, when frequency based positive feedback is enabled at both inverters. The positive feedback signal destabilizes the system frequency causing it to oscillate with increasing amplitude. As the frequency moves beyond the upper limit of 60.5 Hz [31], this condition is detected by an under/over frequency relay, which disconnects the inverter from the system. As shown in Figure 4.14, this scheme detects the islanding condition in 450 ms and disconnects the inverter from the grid.

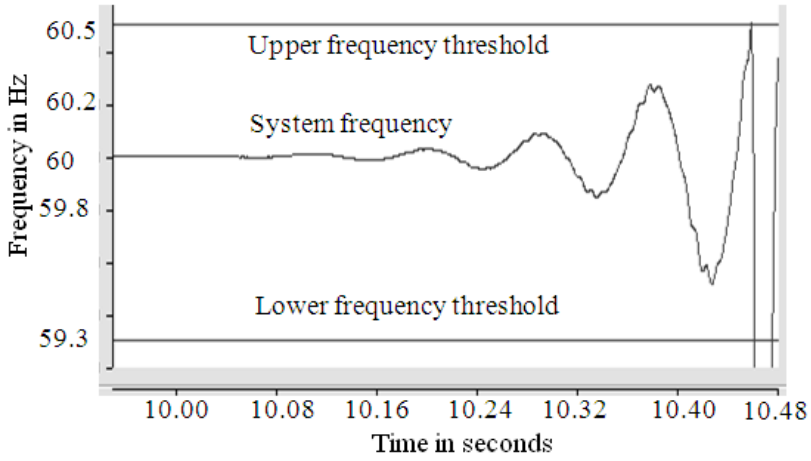

Figure 4.13 System frequency with frequency based positive feedback enabled for Case III

The voltage based positive feedback scheme, however, fails to detect the island formation in this case. The line-to–neutral voltages are identical to those shown in Figure 4.2, following a recloser misoperation, with the voltage based positive feedback activated in both inverters. The inverters remain connected to the system and continue to energize the island in this case.

4.7 Summary of the results of Cases I, II, and III

A brief summary of the results and some conclusions drawn from the simulations in Cases I, II, and III are as follows:

- The frequency based feedback scheme works effectively for all the cases and disconnects the inverter upon island formation within 2 seconds, which is in compliance with the IEEE 1547 [30] standard.

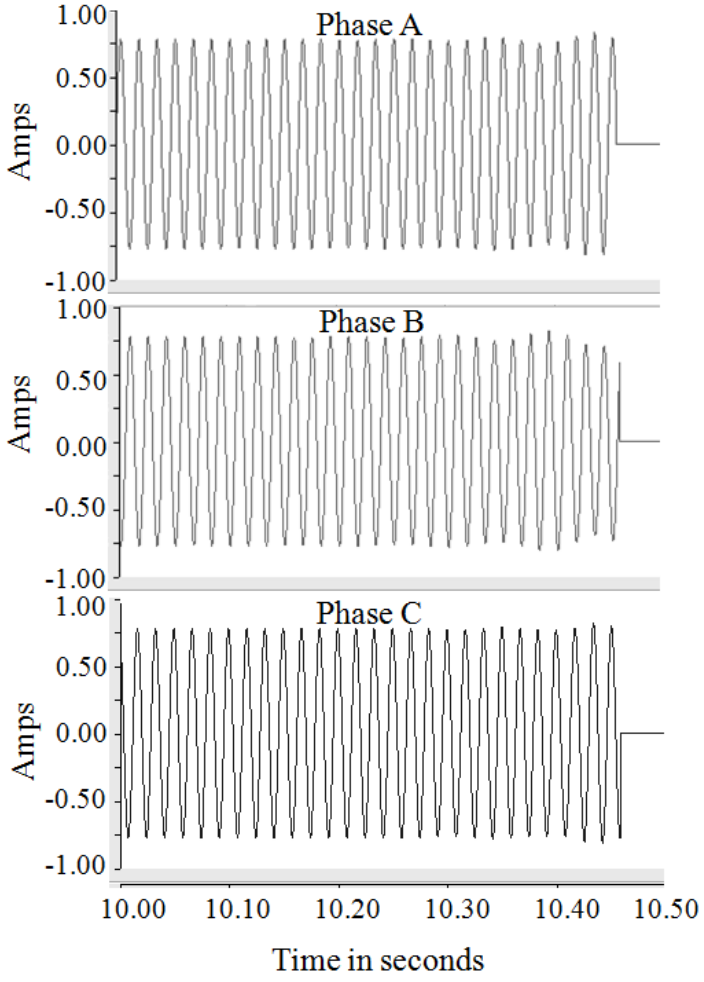

Figure 4.14 Line currents at the terminals of inverter INV 1 with frequency based positive feedback enabled for Case III

- The voltage based positive feedback fails to detect an island formation in Case III when only one phase opens and two phases fail to open. For all other cases, the voltage based scheme works effectively. The close load and generation match within the island is responsible for the failure of the voltage-based scheme in this case.
- The time needed to detect an island formation during recloser misoperation is more than the time needed to detect such an occurrence during a normal recloser operation. The detection time increases progressively as the number of phases failing to open increases. The increased in time is due to the fact the connected phases energizes the island and holds the frequency and voltage within the threshold.
- Contrary to the case when the recloser operates normally, during a recloser misoperation, the detected frequency and voltage at the inverter terminals does not drift in any direction. During a partial disconnection, the grid behaves like unbalanced voltage source operating at 60 Hz with a single phase voltage or two phase voltages set to zero.
- When disconnected partially, the frequency of the island does not drift towards the resonating frequency as the connected phase or phases maintain the frequency at 60 Hz. However, if the frequency based anti-islanding is kept operative, the feed forward signal due to the overshoot of the PLL at the onset of the partial islanding, destabilizes the inverter causing it to disconnect. Figure 4.15 shows the overshoot in system frequency tracked by the PLL.

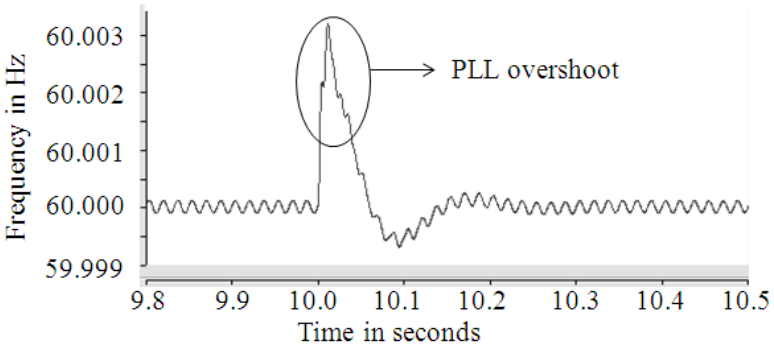

Figure 4.15 PLL overshoot in frequency tracking due to opening of two phases

When only two phases are disconnected, the *d* - axis voltage does not drift but oscillates at 120 Hz around the positive sequence *d* -axis value, and the amplitude of this oscillation is given by the magnitude of the negative sequence component present in the voltage. These oscillations generate a feed-forward signal that drives the voltage out of bounds thus disconnecting the inverter. Figure 4.16 shows the 120 Hz oscillations in the direct axis voltage at the inverter terminal before and after the recloser operation.

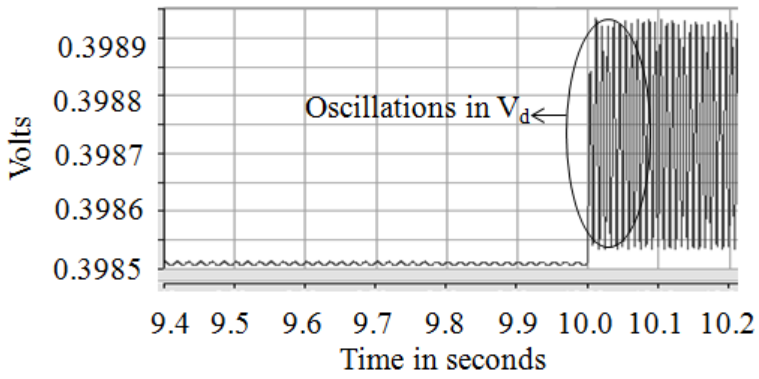

Figure 4.16 Oscillation at 120 Hz in *d*- axis voltage V_d due to presence of negative sequence when two phases of recloser opens.

Chapter 5. Conclusions and future work

5.1 General conclusions

The work presented in this thesis covers two important aspects of grid integration of distributed PV generation. The issues addressed in this work are the effects of distributed PV generation on the power quality of a distribution grid and the anti-islanding of grid-tied PV inverters. The impact of different PV penetration levels on the voltage profile, voltage unbalance and distribution system primary losses were discussed in Chapter 2 of the thesis. Chapter 3 provided the details of the inverter model developed for the anti-islanding study and the results of the study were presented in Chapter 4. Based on the simulations performed and the results presented in the previous chapters the following general conclusions can be drawn:

- A low to moderate penetration level of distributed PV generation is beneficial for distribution grids. Moving the generation closer to the load reduces the line current in different sections of the system. A reduction in line currents leads to better voltage profile at the consumer locations. In addition, decreasing line current reduces the resistive losses in the network. An overall reduction in the distribution system primary losses is achieved.
- A higher penetration level of distributed PV generation can have an adverse effect on the distribution grid. A reversal in power flow, due to sur-

plus in generation, may lead to voltage swells at DG locations beyond the acceptable limits. An increase in line flows due to the reversal in power flow may lead to increased losses in the system. Inadequate sizing of line conductors may cause overloading of lines at high penetration levels of PV generation.

- A large number of single-phase generators have a potential to worsen the voltage unbalance at various locations in the system. Distribution systems are often unbalanced due to the presence of single-phase loads, adding single-phase generation in an arbitrary manner may lead to increase in voltage unbalance. However, a planned addition of distributed PV can benefit an unbalanced system by reducing the voltage drop in stressed phases and thus balancing the phase voltages.
- The active anti-islanding techniques studied have narrow non-detection zones and are capable of detecting an island formation under conditions of power matching in a multi-inverter case. The anti-islanding techniques are capable of detecting an islanding condition even during a recloser misoperation. A misoperation may occur due to a mechanical failure in the recloser.
- It is possible that a voltage based positive feedback scheme will fail to disconnect inverters from the grid after a faulty recloser operation. Although increasing the gain of the positive feedback loop may result in island detection, this reduces the selectivity of the scheme and may lead to

nuisance tripping of inverters during normal grid operation (e.g., a voltage sag or swell). A frequency based positive feedback scheme, however, operates satisfactorily under conditions of active power matching and a combination of both the voltage and frequency based schemes could be a better solution for island detection. Both the schemes can be implemented independently and this approach could reduce the non-detection zone of the anti-islanding schemes.

5.2 Proposed future work

The work done in this thesis covers some important issues concerning the grid interconnection of distributed PV generation. However, many issues still need to be addressed. The new research avenues that could be explored based on the present work are as follows:

- Throughout this study, the power output of the PV inverters is considered constant with the variability in solar insolation neglected. The variation in insolation can be included in future works to identify its impact on the grid at high penetration levels of PV generation. That is, the dynamics of the voltage and current in the distribution primaries should be studied under realistic dynamic conditions.
- The switching of shunt capacitors and operation of SVRs with a high penetration PV may be problematic. The impact of increasing PV penetration on the

operation of these devices needs to be explored. This study would include dynamic (i.e., nonsinusoidal) conditions.

- In the present study, the PV inverters are set to operate at unity power factor supplying only active power. It is possible to operate the inverters at variable power factor by means of suitable control. The controller would then detect the line voltage and set the power factor of the inverter automatically for corrective action. The possibility of the inverters to actively regulate voltage and their interaction with other voltage regulating devices needs to be studied.
- In this study, the load is modeled as constant power load for the power flow analysis and as constant impedance load for the anti-islanding study. The load models could be refined in the future to include the generalized constant impedance-current-power (ZIP) load model.
- Detailed models of air conditioners have been developed in PSCAD [54]. As air conditioners form a majority of loads in states like Arizona and California, the air conditioner load model could be used in future to perform anti-islanding studies and fault analysis.
- The inverter model used in the present study is designed based on controller details as provided in published literature. A validation of the developed model needs to be done with field test results, and further refinement of the controllers could be done in future to have a more accurate representation of the inverter.

- The present study is performed with two inverters having identical anti-islanding mechanism. In a high penetration PV case, inverters with distinctly different anti-islanding mechanisms may be operating in parallel. Such a scenario needs to be studied to evaluate the interaction of the different anti-islanding methods and their efficacy when used in parallel.
- With an increasing PV penetration level, it becomes imperative to analyze the impact of PV generation on the sub-transmission system. During a power export scenario the distribution system behaves like a generating source, which has both single phase, and three phase generation with a power electronic interface. Developing suitable models of these sources and studying their impact on the sub-transmission system could be an interesting research avenue.
- With a proliferation of power electronics interfaced sources with dc-ac conversion, the electromagnetic compatibility of such sources needs to be explored in future [55], [56].

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APPENDIX A

FORTRAN CODE FOR SIMULATION OF AN INVERTER

A.1 Fortran code for simulation of a DDSRF PLL

```
SUBROUTINE DDSRF(Ea,Eb,Ec,theta,Kp,Ki,fc,fr,Klp,Edpf)

!---------------------------------------
! Standard includes
!---------------------------------------

      INCLUDE 'nd.h'
      INCLUDE 'emtconst.h'
      INCLUDE 'emtstor.h'
      INCLUDE 's0.h'
      INCLUDE 's1.h'
      INCLUDE 's2.h'
      INCLUDE 's4.h'
      INCLUDE 'branches.h'
      INCLUDE 'pscadv3.h'
      INCLUDE 'fnames.h'
      INCLUDE 'radiolinks.h'
      INCLUDE 'matlab.h'
      INCLUDE 'rtconfig.h'
!-----------------------------------------------------------------
-----------
!-----------------------------------------------------------------
-----------
! Variable Declaration
! Input variables
      REAL Ea,Eb,Ec,Kp,Ki,fc, Klp
! Output variables
      REAL fr, theta
! Internal variables
      REAL Eqp, Edp, Eqpf, Edpf, Eqn, Edn, Eqnf, Ednf, Eq_int, w
!-----------------------------------------------------------------
------------

! Copy and increment pointers
      MY_STORF=NSTORF
      NSTORF=NSTORF+11
!
!-----------------------------------------------------------------
------------
! Main part of the subroutine
!-----------------------------------------------------------------
------------

! calculating w and fr
!---------------------------------------

      Eq_int = 0.5*(STORF(MY_STORF + 2) +
STORF(MY_STORF+2))*DELT*Ki + STORF(MY_STORF + 8)
      w= Kp*STORF(MY_STORF + 2) + Eq_int + TWO_PI*fc
      fr=w/TWO_PI
```

```
!---------------------------------------
!calculating theta
!---------------------------------------

      theta= 0.5*(w + STORF(MY_STORF+9))*DELT + STORF(MY_STORF +
10)
      theta_i = mod(theta,TWO_PI)

!-----------------------------------------------------------------
-------------
! ABC to DQ transformation in positive sequence frame
!
      Edp =2*(Ea*cos(theta_i) + Eb*cos(theta_i-PI2_BY3) +
Ec*cos(theta_i+PI2_BY3))/3
      Eqp =2*(Ea*sin(theta_i) + Eb*sin(theta_i-PI2_BY3) +
Ec*sin(theta_i+PI2_BY3))/3
!-----------------------------------------------------------------
------------
! ABC to DQ transformation in negative sequence frame
!
      Edn = 2*(Ea*cos(-theta_i) + Eb*cos(-theta_i-PI2_BY3) +
Ec*cos(-theta_i+PI2_BY3))/3
      Eqn = 2*(Ea*sin(-theta_i) + Eb*sin(-theta_i-PI2_BY3) +
Ec*sin(-theta_i+PI2_BY3))/3
!-----------------------------------------------------------------
------------
! Double frequency component cancellation
!
      Edp_i=Edp-STORF(MY_STORF+4)*cos(2*theta_i)-
STORF(MY_STORF+6)*sin(2*theta_i)
      Eqp_i=-Eqp-
STORF(MY_STORF+6)*cos(2*theta_i)+STORF(MY_STORF+4)*sin(2*theta_i)

      Edn_i=Edn-
STORF(MY_STORF)*cos(2*theta_i)+STORF(MY_STORF+2)*sin(2*theta_i)
      Eqn_i=-Eqn-STORF(MY_STORF+2)*cos(2*theta_i)-
STORF(MY_STORF)*sin(2*theta_i)
!-----------------------------------------------------------------
------------
! Filtered positive sequence dq-axis elements
!
      Edpf = (STORF(MY_STORF)*(1-Klp*DELT*0.5)
+0.5*Klp*DELT*(Edp_i+STORF(MY_STORF+1)))/(1+Klp*DELT*0.5)
      Eqpf = (STORF(MY_STORF+2)*(1-Klp*DELT*0.5)
+0.5*Klp*DELT*(Eqp_i+STORF(MY_STORF+3)))/(1+Klp*DELT*0.5)
!-----------------------------------------------------------------
------------
! Filtered negative sequence dq-axis elements
!
      Ednf = (STORF(MY_STORF+4)*(1-Klp*DELT*0.5)
+0.5*Klp*DELT*(Edn_i+STORF(MY_STORF+5)))/(1+Klp*DELT*0.5)
      Eqnf = (STORF(MY_STORF+6)*(1-Klp*DELT*0.5)
+0.5*Klp*DELT*(Eqn_i+STORF(MY_STORF+7)))/(1+Klp*DELT*0.5)
```

```
!-------------------------------------------------------------------
------------


!---------------------------------------
! Output at time zero
! ---------------------------------------
      IF ( TIMEZERO ) THEN
      Edpf= 0
      Eqpf = 0
      Ednf = 0
      Eqnf = 0
      Edp_i= 0
      Eqp_i= 0
      Edn_i= 0
      Eqn_i= 0
      Eq_int= 0
      w= 0
      theta= 0
      ENDIF
!
!---------------------------------------
! Save the data for next time step
! ---------------------------------------
      STORF(MY_STORF) = Edpf
      STORF(MY_STORF + 1) = Edp_i
      STORF(MY_STORF + 2) = Eqpf
      STORF(MY_STORF + 3) = Eqp_i
      STORF(MY_STORF + 4) = Ednf
      STORF(MY_STORF + 5) = Edn_i
      STORF(MY_STORF + 6) = Eqnf
      STORF(MY_STORF + 7) = Eqn_i
      STORF(MY_STORF + 8) = Eq_int
      STORF(MY_STORF + 9) = w
      STORF(MY_STORF + 10) = theta
!
RETURN
END
```

A.2 Fortran code for simulation of a current controller

```
SUBROUTINE DQcontrol(Id,Iq,tht,T,T1,T2,G,Idmd,
Iqmd,Aif,Aiv,cut,da,db,dc)

!---------------------------------------
! Standard includes
!---------------------------------------

      INCLUDE 'nd.h'
      INCLUDE 'emtconst.h'
      INCLUDE 'emtstor.h'
      INCLUDE 's0.h'
      INCLUDE 's1.h'
      INCLUDE 's2.h'
      INCLUDE 's4.h'
      INCLUDE 'branches.h'
      INCLUDE 'pscadv3.h'
      INCLUDE 'fnames.h'
      INCLUDE 'radiolinks.h'
      INCLUDE 'matlab.h'
      INCLUDE 'rtconfig.h'
!-----------------------------------------------------------------
-----------
!-----------------------------------------------------------------
-----------
! Variable Declaration
! Input variables
      REAL Id,Iq,tht,T,T1,T2,G,Aif,Aiv,cut,Idmd, Iqmd
! Output variables
      REAL da,db,dc
! Internal variables
      REAL Iderr,Iqerr,Iderr1, VcdT,Iqerr1,VcqT,
m,a,b,c,Iderr2,Iqerr2, Vcd, Vcq

!-----------------------------------------------------------------
------------

! Copy and increment pointers
      MY_STORF=NSTORF
      NSTORF=NSTORF+6
!
! Compute the internal constants
      m=G*T1/T2
      a=1/T1
      b=1/T2
      c=a-b

!-----------------------------------------------------------------
------------
! Main part of the subroutine
!-----------------------------------------------------------------
------------
```

```
! calculating Iderr and Iqerr
!---------------------------------------

      Iderr=Idmd+Aiv-Id
      Iqerr=Iqmd-Aif-Iq

!---------------------------------------
!calculating Vcd
!---------------------------------------

      Iderr1 = STORF(MY_STORF+1)+
0.5*DELT*(Iderr+STORF(MY_STORF))

      IF (Iderr1>100) THEN
      Iderr1 = 100
      ELSE IF (Iderr1<-100) THEN
      Iderr1 = 100
      ENDIF


      Iderr2 = (STORF(MY_STORF+2)*(1-
b*DELT*0.5)+0.5*c*m*DELT*(Iderr1+STORF(MY_STORF+1)))/(1+b*DELT*0.
5)
      VcdT= m*Iderr1+Iderr2

      IF (VcdT>1) THEN
      VcdT = 1
      ELSE IF (VcdT<-1) THEN
      VcdT = -1
      ENDIF

      Vcd= VcdT+0.1319*Iq

!---------------------------------------
!calculating Vcq
!---------------------------------------

      Iqerr1 = STORF(MY_STORF+4)+
0.5*DELT*(Iqerr+STORF(MY_STORF+3))

      IF (Iqerr1>100) THEN
      Iqerr1 = 100
      ELSE IF (Iqerr1<-100) THEN
      Iqerr1 = 100
      ENDIF


      Iqerr2 = (STORF(MY_STORF+5)*(1-
b*DELT*0.5)+0.5*c*m*DELT*(Iqerr1+STORF(MY_STORF+4)))/(1+b*DELT*0.
5)
      VcqT= m*Iqerr1+Iqerr2
```

```
      IF (VcqT>1) THEN
      VcqT = 1
      ELSE IF (VcqT<-1) THEN
      VcqT = -1
      ENDIF


      Vcq=VcqT-0.1319*Id

!----------------------------------------
!Relay input
!----------------------------------------
      IF (cut==1) THEN
      Vcd = 0
      Vcq = 0
      ENDIF

!-----------------------------------------------------------------
-------------
! DQ to ABC transformation
!
      da =Vcd*cos(tht) + Vcq*sin(tht)
      db =Vcd*cos(tht-PI2_BY3) + Vcq*sin(tht-PI2_BY3)
      dc =Vcd*cos(tht+PI2_BY3) + Vcq*sin(tht+PI2_BY3)

!----------------------------------------
! Output at time zero
! ---------------------------------------
      IF ( TIMEZERO ) THEN
      Iderr1 = 0
      Iderr2 = 0
      Iqerr1 = 0
      Iqerr2 = 0
      ENDIF
!
!----------------------------------------
! Save the data for next time step
! ---------------------------------------
      STORF(MY_STORF) = Iderr
      STORF(MY_STORF + 1) = Iderr1
      STORF(MY_STORF + 2) = Iderr2
      STORF(MY_STORF + 3) = Iqerr
      STORF(MY_STORF + 4) = Iqerr1
      STORF(MY_STORF + 5) = Iqerr2
!
RETURN
END
```

A.3 Fortran code for simulation of an overvoltage / undervoltage and overfrequency / underfrequency relay

```
SUBROUTINE VFRelay(V,f, Vup,Vlow, fup, flow,Trip)

!---------------------------------------
! Standard includes
!---------------------------------------

      INCLUDE 'nd.h'
      INCLUDE 'emtconst.h'
      INCLUDE 'emtstor.h'
      INCLUDE 's0.h'
      INCLUDE 's1.h'
      INCLUDE 's2.h'
      INCLUDE 's4.h'
      INCLUDE 'branches.h'
      INCLUDE 'pscadv3.h'
      INCLUDE 'fnames.h'
      INCLUDE 'radiolinks.h'
      INCLUDE 'matlab.h'
      INCLUDE 'rtconfig.h'
!-----------------------------------------------------------------
-----------
!-----------------------------------------------------------------
-----------
! Variable Declaration
! Input variables
      REAL V, f
! Output variables
      INTEGER Trip
! Internal variables
      REAL Vup, Vlow, fup, flow
           INTEGER trip1, trip2

!-----------------------------------------------------------------
------------

! Copy and increment pointers
      MY_STORI=NSTORI
      NSTORI=NSTORI+1
!
!-----------------------------------------------------------------
------------
! Main part of the subroutine
!-----------------------------------------------------------------
------------
! Detecting over voltage or under voltage
!---------------------------------------

      IF (V>Vup .OR. V<Vlow) THEN
      trip1=1
           ELSE
```

```
        trip1=0
         ENDIF
      IF (f>fup .OR. f<flow) THEN
      trip2=1
           ELSE
        trip2=0
         ENDIF

! Final trip signal
!---------------------------------------
         IF (trip1==1 .OR. trip2==1) THEN
         Trip=1
           ELSE
           Trip=0
           ENDIF
! Latch the trip signal
!---------------------------------------
         IF (STORI(MY_STORI) > Trip) THEN
         Trip=STORI(MY_STORI)
           ENDIF
! Block trip signal till steady state is reached
!---------------------------------------
           IF (TIME<2) THEN
           Trip = 0
           ENDIF
!---------------------------------------
! Output at time zero
! ---------------------------------------
      IF ( TIMEZERO ) THEN
      Trip= 0
      ENDIF
!
!---------------------------------------
! Save the data for next time step
! ---------------------------------------
      STORI(MY_STORI) = Trip

!
RETURN
END
```

A.4 Fortran code for simulation of an anti-islanding controller

```
SUBROUTINE Antiisland(V,f,Vset,fset,gainV,gainf,Aiv,Aif,wc1,wc2,
Aivc,Aifc, ferrG,Aiv1)

!---------------------------------------
! Standard includes
!---------------------------------------

      INCLUDE 'nd.h'
      INCLUDE 'emtconst.h'
      INCLUDE 'emtstor.h'
      INCLUDE 's0.h'
      INCLUDE 's1.h'
      INCLUDE 's2.h'
      INCLUDE 's4.h'
      INCLUDE 'branches.h'
      INCLUDE 'pscadv3.h'
      INCLUDE 'fnames.h'
      INCLUDE 'radiolinks.h'
      INCLUDE 'matlab.h'
      INCLUDE 'rtconfig.h'
!-----------------------------------------------------------------
-----------
!-----------------------------------------------------------------
-----------
! Variable Declaration
! Input variables
      REAL V,f,Vset,fset,gainV,gainf
! Internal Variables
      REAL ferr,Verr,ferrG,VerrG,Aiv1,Aiv2,Aiv3,Aif1,Aif2,Aif3
        INTEGER Aifc, Aivc
! Output Variables
      REAL Aiv, Aif
!-----------------------------------------------------------------
-----------
! Copy and increment pointers
      MY_STORF=NSTORF
      NSTORF=NSTORF+8

!-----------------------------------------------------------------
-----------
      ferr=f-fset
        Verr=V-Vset
!-----------------------------------------------------------------
-----------
! Gain of the loop
      ferrG=ferr*gainf
        VerrG=Verr*gainV
!-----------------------------------------------------------------
-----------
! Band pass filter
```

```
      Aiv1= ((1-
wc1*DELT*0.5)*STORF(MY_STORF)+wc1*DELT*0.5*(VerrG+STORF(MY_STORF+
1)))/(1+wc1*DELT*0.5)
        Aiv3= -Aiv1+VerrG
        Aiv2= ((1-
wc2*DELT*0.5)*STORF(MY_STORF+2)+wc2*DELT*0.5*(Aiv3+STORF(MY_STORF
+6)))/(1+wc2*DELT*0.5)

        Aif1= ((1-
wc1*DELT*0.5)*STORF(MY_STORF+3)+wc1*DELT*0.5*(ferrG+STORF(MY_STOR
F+4)))/(1+wc1*DELT*0.5)
        Aif3= -Aif1+ferrG
        Aif2= ((1-
wc2*DELT*0.5)*STORF(MY_STORF+5)+wc2*DELT*0.5*(Aif3+STORF(MY_STORF
+7)))/(1+wc2*DELT*0.5)
!-------------------------------------------------------------------
-----------
! Hard limiter
      IF (Aiv2>0.1) THEN
           Aiv2 =0.1
           ELSEIF(Aiv2<-0.1) THEN
             Aiv2=-0.1
             ENDIF
           IF (Aif2>0.1) THEN
           Aif2 =0.1
           ELSEIF(Aif2<-0.1) THEN
             Aif2=-0.1
                ENDIF
!-------------------------------------------------------------------
-----------
! Antiislanding control
           IF (Aivc==1) THEN
           Aiv =Aiv2
           ELSE
             Aiv=0
             ENDIF
           IF (Aifc==1) THEN
           Aif =Aif2
           ELSE
             Aif=0
             ENDIF
!-------------------------------------------------------------------
-----------
! Timezero values
        IF (TIMEZERO) THEN
            Aiv1=0
            Aiv3=0
            VerrG=0
            Aiv2=0
            Aif1=0
            ferrG=0
            Aif2=0
            Aif3=0
```

```
            ENDIF
!---------------------------------------
! Save the data for next time step
! ---------------------------------------
      STORF(MY_STORF) = Aiv1
      STORF(MY_STORF+1) = VerrG
        STORF(MY_STORF+2) = Aiv2
        STORF(MY_STORF+3) = Aif1
      STORF(MY_STORF+4) = ferrG
        STORF(MY_STORF+5) = Aif2
        STORF(MY_STORF+6) = Aiv3
        STORF(MY_STORF+7) = Aif3
! ---------------------------------------
      RETURN
        END
```