Energy Efficient RF Transmitter Design using Enhanced Breakdown Voltage SOI-CMOS Compatible MESFETs

by

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ABSTRACT

The high cut-off frequency of deep sub-micron CMOS technologies has enabled the integration of radio frequency (RF) transceivers with digital circuits. However, the challenging point is the integration of RF power amplifiers, mainly due to the low breakdown voltage of CMOS transistors. Silicon-on-insulator (SOI) metal semiconductor field effect transistors (MESFETs) have been introduced to remedy the limited headroom concern in CMOS technologies. The MESFETs presented in this thesis have been fabricated on different SOI-CMOS processes without making any change to the standard fabrication steps and offer 2-30 times higher breakdown voltage than the MOSFETs on the same process.

This thesis explains the design steps of high efficiency and wideband RF transmitters using the proposed SOI-CMOS compatible MESFETs. This task involves DC and RF characterization of MESFET devices, along with providing a compact Spice model for simulation purposes. This thesis presents the design of several SOI-MESFET RF power amplifiers operating at 433, 900 and 1800 MHz with ~40% bandwidth. Measurement results show a peak power added efficiency (PAE) of 55% and a peak output power of 22.5 dBm. The RF-PAs were designed to operate in Class-AB mode to minimize the linearity degradation.

Class-AB power amplifiers lead to poor power added efficiency, especially when fed with signals with high peak to average power ratio (PAPR) such as wideband code division multiple access (W-CDMA). Polar transmitters have been introduced to improve the efficiency of RF-PAs at backed-off powers. A MESFET based envelope tracking (ET) polar transmitter was designed and

measured. A low drop-out voltage regulator (LDO) was used as the supply modulator of this polar transmitter. MESFETs are depletion mode devices; therefore, they can be configured in a source follower configuration to have better stability and higher bandwidth that MOSFET based LDOs. Measurement results show 350 MHz bandwidth while driving a 10 pF capacitive load.

A novel polar transmitter is introduced in this thesis to alleviate some of the limitations associated with polar transmitters. The proposed architecture uses the backgate terminal of a partially depleted transistor on SOI process, which relaxes the bandwidth and efficiency requirements of the envelope amplifier in a polar transmitter. The measurement results of the proposed transmitter demonstrate more than three times PAE improvement at 6-dB backed-off output power, compared to the traditional RF transmitters.

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CHAPTER 1

INTRODUCTION

Modern digital communication systems have rapidly expanded in capability which has required significant advancements of both digital CMOS and RF front-end performance. The expectations of more features and extended battery lifetime has made bandwidth, power and system efficiency even more critical. The standard platform for system integration at relatively low cost has traditionally been silicon CMOS. The high cut-off frequency (f_T) of deep sub-micron CMOS technologies now makes it possible to integrate RF and digital CMOS circuits. This has led to a trend of building single chip CMOS transceivers [1], [2], [3]. Yet, the advancement and scaling of CMOS has also led to reduced operating voltages which makes analog and RF design more difficult due to limited voltage headroom. The nominal supply voltage and cut-off frequency of CMOS transistors for various technology nodes are shown in Figure 1 [4], [5].

The high cut-off frequency of deep sub-micron CMOS transistors benefits both digital and analog/RF circuits. This trend has enabled the RF front ends to operate at several GHz. The reduction in supply voltage has also helped to minimize the power dissipation in digital circuitries. However, due to aggressive signal-to-noise ratio, output power, dynamic range and linearity requirements of modern communication standards, analog and RF circuits suffer intensely from this supply reduction. The sticking point is the integration of front end stages, specifically power amplifiers, since inductive elements used in their design lead to high voltage swings around the drain terminal.

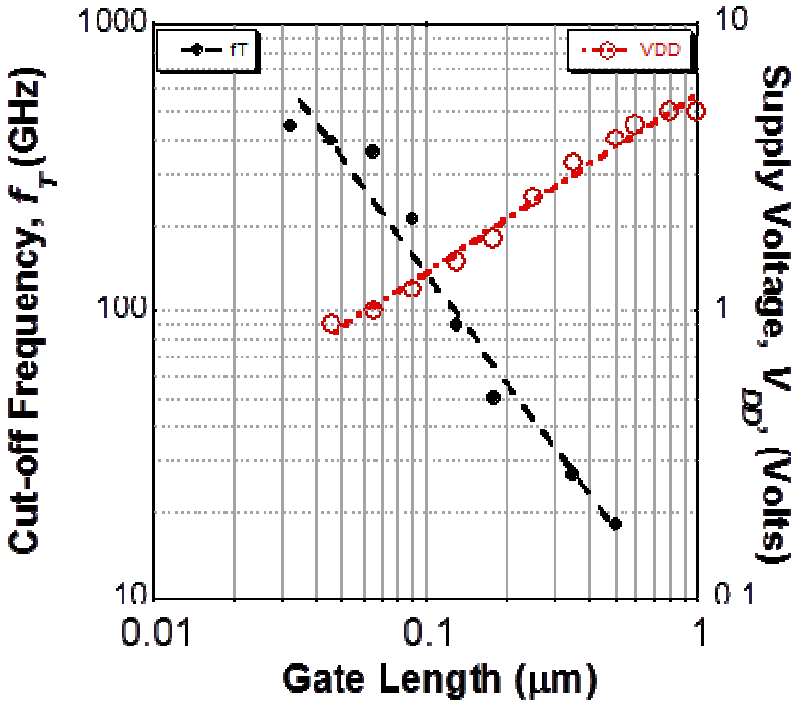


Figure 1. CMOS scaling trend.

RF PAs are power hungry blocks that need to handle large voltage and current swings on the output node to achieve a desired transmitted power. Based upon the application, the output stage should be capable of delivering a fixed amount of maximum power. As we will see in the following sections, the supply voltage of a technology limits either the output power, efficiency, or adds design complexities.

A very simplified form of a Class-A RF amplifier is shown in Figure 2. The operational behavior of the Class-A amplifier will be discussed more in detail in the subsequent sections of this thesis. However the basic output power calculation is shown here.

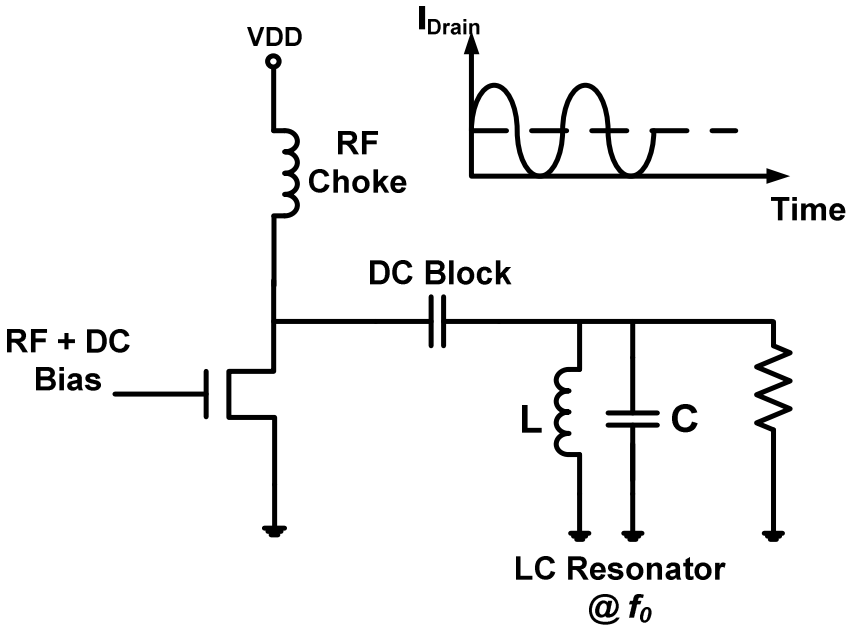


Figure 2. Class A RF power amplifier

The output power is shown in Equation 1 for a Class-A amplifier with an ideal transistor. For a fixed supply voltage, V_{DD}, reducing R_L increases the output power, P_{OUT}. As will be shown later, in practice there are some limitations on lowering the R_L value [6]. In this example it is assumed to have R_L=5 Ω.

$$P_{OUT} = \frac{{V_{DD}}^2}{2 \times R_L} \qquad \text{Equation 1}$$

Substituting the collected data shown in Figure 1 into Equation 1, the maximum output power for different single device PA on CMOS technologies, for the case of a Class A output stage, was calculated and shown in Figure 3. As it can be seen, the maximum P_{OUT} for a standard 45nm CMOS technology is less than 60-mW. This amount of power is much lower than what is required for most handset device applications. For example, the GSM 900/1800 [7] standards require a P_{OUT} of 1-4 Watt. This is less of an issue for other higher voltage

technologies such as GaN, GaAs or LDMOS which can encompass power ranges of 1-10 Watt [8], [9], [10].

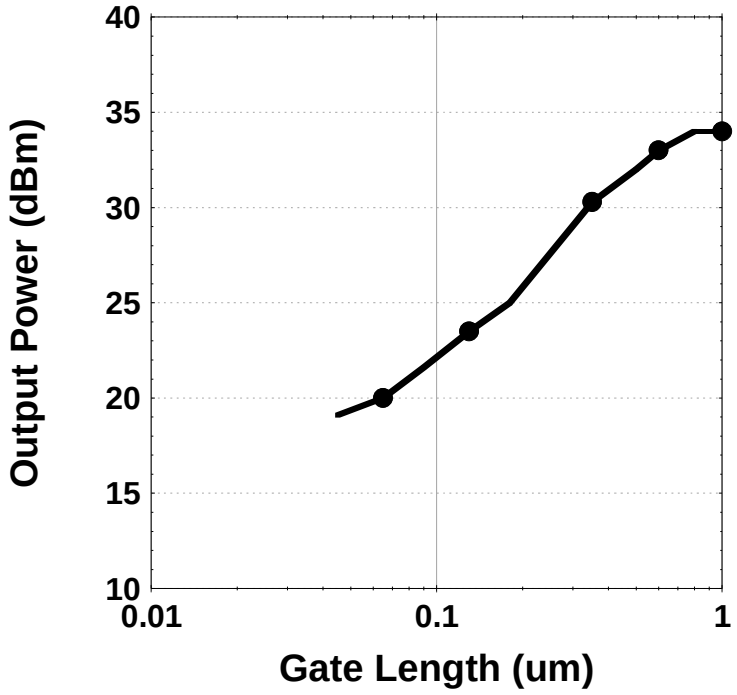


Figure 3. Maximum output power of a Class-A amplifier versus gate length under 5 Ohm loadline condition.

As a result of the reduced output power capability for deep-submicron CMOS devices, high power and expensive discrete units like SiGe and GaAs are often employed. Nevertheless, many efforts have been made to employ CMOS transistors in PA modules [11], [12]. The main motivation is the low fabrication cost of CMOS compared to all the other PA technologies. Moreover, almost all the other transceiver circuit blocks can currently be designed and integrated on the same CMOS chip. Thus, the CMOS power amplifier is the last challenge towards a single chip transceiver solution.

Many techniques have been studied to overcome the headroom limitation of CMOS transistors. One such solution is higher impedance transformation [13] which is often used to reduce the voltage swing on the transistor nodes. Unfortunately this adds additional losses to the matching network [6]. Another option is the cascode architecture [14], [15]. The cascode allows for a higher supply voltage since the voltage is divided between two or more transistors. This method can slightly increase output power. Some more specialized processes also include bipolar transistors; however, these processes are typically much more expensive than standard bulk CMOS processes [16]. A low cost solution which is possible on many of today's processes is using thick gate oxide MOSFETs [17]. These transistors can typically handle voltages that are 1.5-2 times higher than standard MOSFETs. Parallel amplification is another approach that uses a power combiner that adds up output power from parallel PAs. This method requires extra passive components, which results in larger die area and worse efficiency.

In summary, there are tricks and architectures that can enhance the output power for a class-A amplifier, but each of them has their own drawbacks. Designing high efficiency amplifiers, such as class–E, are even more challenging since the voltage swing is 2-3.5 times larger than the supply voltage [18]. All these issues together, have led to a vital need for high breakdown voltage, low cost, RF transistors on CMOS processes.

The idea of a high voltage, silicon on insulator (SOI)-CMOS compatible MESFET was proposed and patented by T.J. Thornton, *et al.* [19]. The patented MESFET has some outstanding characteristics that make it one of the best device

solutions towards fabrication of low cost, fully integrated transceivers. The main advantage of MESFETs over MOSFETs is their enhanced breakdown voltage. These MESFETs have supply voltage capabilities that are several times higher than the MOSFETs on the same processes. On certain technologies, breakdown voltages that are 20-30 times higher than the MOSFETs have been achieved. This greatly relaxes the design constraints on CMOS PAs and can significantly increase the peak output power.

The remaining portion of this thesis will focus mainly on demonstrating the feasibility of high power, high speed and linear RF output stage design using the proposed SOI-MESFET devices. This task would not be possible without having a good understanding of both RF power amplifier theory and SOI-MESFET device operation. Hence, the first chapter is focused on understanding these two concepts.

1.1. SOI-MESFET Device Operation

Metal-semiconductor field-effect-transistors (MESFETs) can be integrated on any SOI or SOS (Silicon on Sapphire) CMOS processes without altering the process or adding any additional fabrication steps [20], [21], [22], [23]. Other reports [24], [25], [26] have considered silicon MESFETs on SOI, SOS, and bulk CMOS processes but in each case, none of them used a standard CMOS process flow.

A cross section view of the proposed SOI-MESFET is shown in Figure 4. Unlike most MOSFETs, MESFETs are depletion mode devices. They are also a majority carrier device. This means that a channel exists between drain and

source, even when the gate is floating. In order to reduce the drain current and eventually “pinch-it off” a negative gate bias voltage is needed to invert the channel under the gate. Spacers regions are added between the drain and gate, L_{aD}, and the source and gate, L_{aS}, to avoid shorting the device terminals. Depending on the channel thickness, the MESFET can operate as a fully or partially depleted transistor. MESFETs used in this work are partially depleted (PD), which means that the silicon channel below the gate is sufficiently thick to control the conduction of the device.

Like a CMOS transistor, the RF performance and current drive capability of a MESFET is highly dependent on the minimum gate length that can be achieved. The PD-MESFET drain current (I_D) equations are also fairly similar to standard MOSFETs. Current and parasitic capacitance calculations are discussed in the modeling chapter. The rest of this section talks about structural differences between the MOSFET and MESFET and the benefits of MESFETs in certain applications such as PAs.

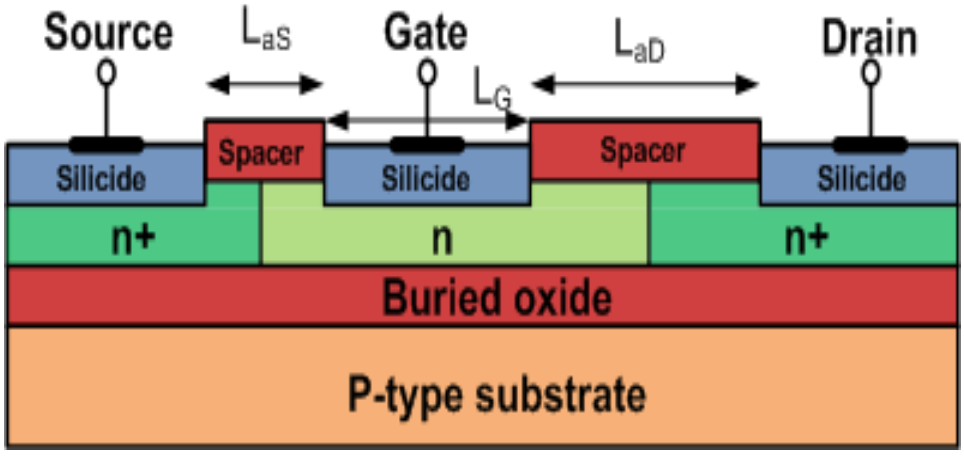


Figure 4. Cross section view of a partially depleted MESFET structure.

A cross sectional view of an N-channel MOSFET on a bulk CMOS technology is shown in Figure 5. One of the dissimilarities between MESFETs and MOSFETs is the gate contact. The MOSFET's high impedance gate oxide layer does not exist in MESFETs. Instead a MESFET gate is formed by a metal-silicide contact on a lightly doped silicon region. This introduces much higher quiescent gate current (I_G) in MESFETs, which increases off-mode power dissipation. However, it benefits the MESFET in terms of breakdown voltage behavior. Oxide breakdown is one of the key CMOS breakdown mechanisms and it continues to get worse as the oxide thickness, t_{ox}, scales with technology nodes.

$$Electric\ Field\ (E) = \frac{V_{OX}}{t_{OX}}, so\ t_{OX} \downarrow \Rightarrow E \uparrow \qquad \text{Equation 2}$$

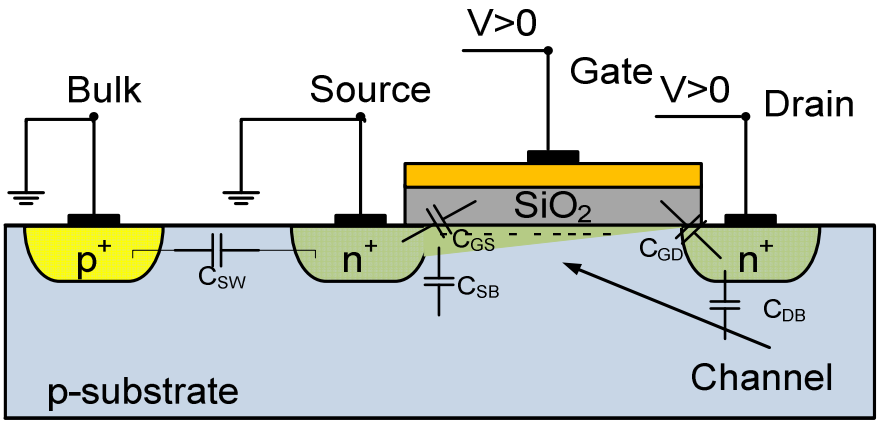


Figure 5. Cross section view of a standard N-channel MOSFET.

The drain to source electric field is another source of breakdown in MOSFETs. The L_{aS} and L_{aD} regions added in the MESFET structure, increase the distance between drain to source and thus lower the electric field at this critical junction. Therefore, the spacers can also be used to improve the breakdown voltage. This is a similar concept to that used in LDMOS.

The MESFET breakdown is thought to be caused mostly by avalanche ionization and tunneling mechanisms. As the MESFET approaches soft breakdown, which is reversible, the surface electric field can become large enough to lower the barrier height at the gate and allow electrons to tunnel into the channel from the gate metal. Consequently this leads to an exponential increase in drain-to-gate current. If the drain voltage is further increased and/or the gate becomes more negatively biased, the electric field will become even larger and avalanche ionization will begin to occur. Eventually this will lead to a non-reversible hard breakdown for the MESFET [27].

The cost of enlarging the spacer regions includes added parasitic resistance for the MESFET and additional die area needed to lay the devices out. Source resistance degrades both DC gain and RF performance. Thus there is a tradeoff between enhancing the breakdown voltage and RF performance. Although the RF performance degrades as V_{BD} increases, the overall MESFET performance has evident advantages over MOSFETs for up to 5GHz PA design applications. Measured characteristics of fabricated MESFETs are discussed in Chapter II of this thesis. The following subsection is an overview of how device parameters can affect the PA performance.

1.2. RF Power Amplifier Theory and Figure of Merit

RF power amplifier design methodology is somewhat different and more challenging than low power or low noise amplifiers. Specific figures of merit (FoMs) have been defined for characterization and comparison purpose of power amplifiers. Among them power added efficiency (PAE), drain efficiency (DE), 1-

dB compression point, harmonic suppression, bandwidth, gain, AM/AM and AM/PM characteristics, are the most widely used. In the next section, the FoMs and different classes of operations will be presented.

1.2.1. Figures of Merit

A large portion of the total energy consumed in any radio transmitter is devoted to the output stages. Therefore, the efficiency is a critical factor when evaluating different PAs. It characterizes the effectiveness of the DC-to-RF power conversion of an amplifier. It is also a measure of dissipated power as heat in percent. Low efficiency can be seen in high electricity cost, low battery life and heating effects. Heating can significantly compromise the reliability and lifetime of the whole transmitter; hence, in some cases, special cooling systems are required [28].

Figure 6 shows a general block diagram of a power amplifier. The ratio of the fundamental RF power delivered to the load, R_L, (P_{LOAD}) to the DC power handled from the V_{DD}, supply voltage, (P_{DC}) is called drain efficiency (DE) and is calculated in Equation 3.

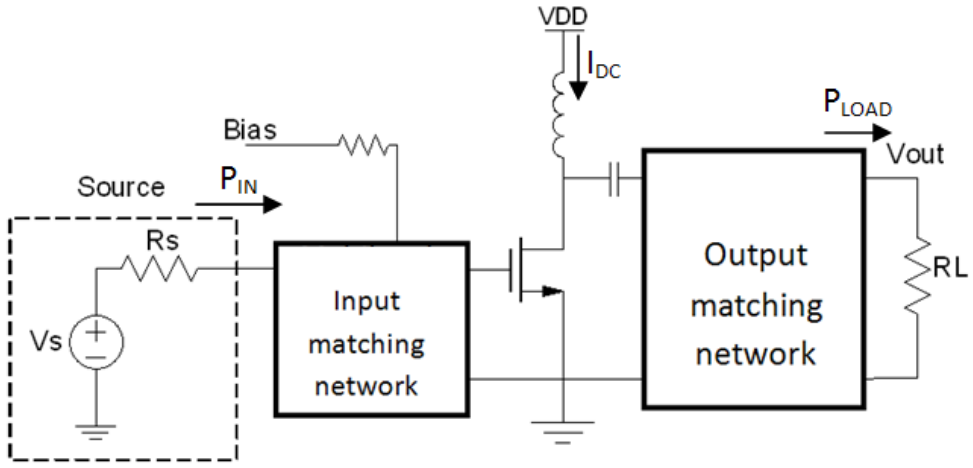


Figure 6: Power Amplifier block diagram

$$DE = \frac{P_{LOAD}}{P_{DC}} = \frac{P_{LOAD}}{I_{DC} \times V_{DD}} \qquad \text{Equation 3}$$

Transistor power gain (G_T or G) is finite and drops as frequency increases. Therefore a more inclusive definition for power efficiency should also include the effect of input power (P_{IN}). Power added efficiency (PAE) is defined in Equation 4 [28].

$$PAE = \frac{P_{LOAD} - P_{IN}}{P_{DC}} = \frac{P_{LOAD} - P_{IN}}{I_{DC} \times V_{DD}} = \frac{P_{LOAD}}{I_{DC} \times V_{DD}}\left(1 - \frac{1}{G}\right) = DE\left(1 - \frac{1}{G}\right) \qquad \text{Equation 4}$$

Transistor gain is highly dependent on bias conditions, and it drops quickly at higher output powers. This behavior contributes to the main part of nonlinearities. Power amplifiers directly affect the signal integrity. Therefore, the RF PA nonlinearity should be low enough in order to satisfy the modulation scheme specifications. Figure 7 shows the generic nonlinear behavior of a power

amplifier. The 1-dB compression point is noted on the plot. It is defined as the point where the gain drops by 1 dB compared to the small signal gain [28].

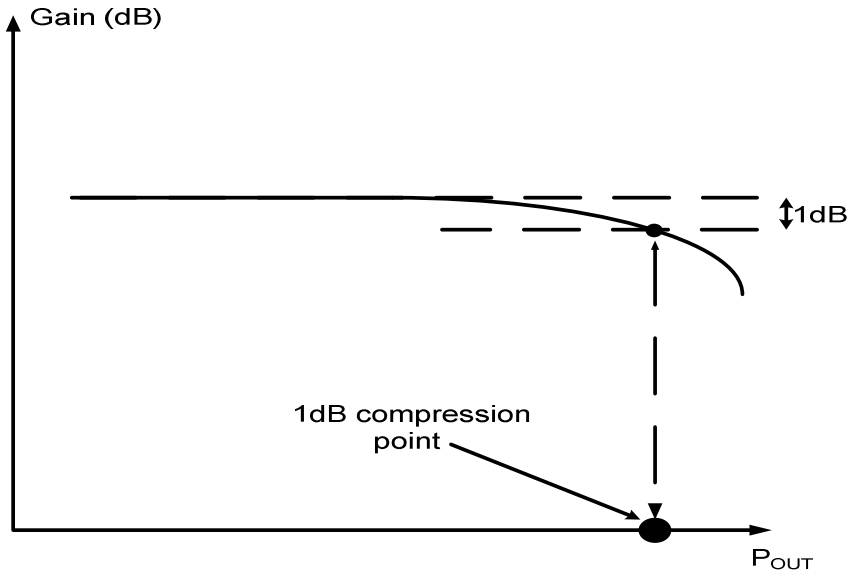


Figure 7. Power Gain vs Output Power

Communication standards put some requirements on both the in-band signal quality and out of band harmonic emission of the transmitted RF signal. Second and third harmonic suppression characterizes nonlinearities and out of band emission behavior of a power amplifier. Harmonic suppression is defined as the ratio of power delivered to load at the second or third harmonic to the amount of power located at the fundamental frequency, while applying a single tone sinewave to the PA's input. Figure 8 shows an example of a PA output spectrum. Second and third harmonic suppression levels are also marked on the plot [28].

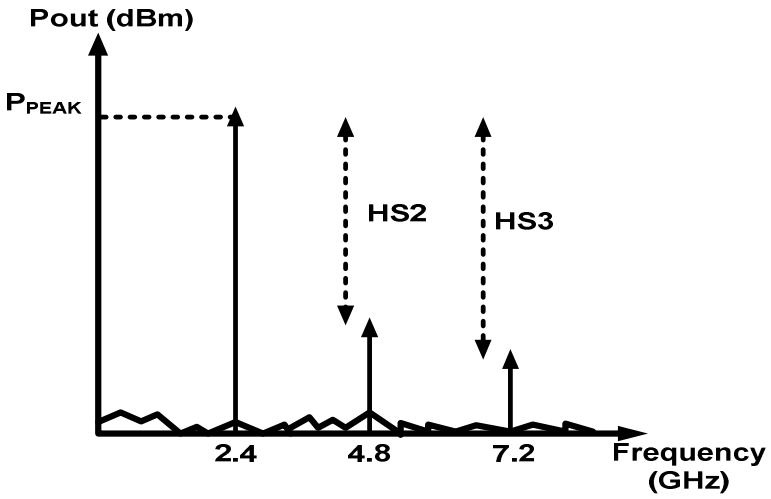


Figure 8. An example of power amplifier output spectrum

Inter-modulation distortion is another consequence of the PA nonlinearity. In many applications, the modulated signal has a wide bandwidth and PA nonlinearity introduces new distortion products which fall inside the signal bandwidth. A conventional approach for in-band distortion characterization is a two-tone test. If two sinusoidal signals, with frequencies equal to f_1 and f_2, are injected at the input of a nonlinear amplifier, the output signal contains additional frequency components called inter-modulation products.

Figure 9 shows the generation of third-order inter-modulation products [29], [30]. Besides the input signal harmonics, the amplifier generates new frequencies located at nf_2-mf_1 where m and n are integers. Among these products, $2f_2$-f_1 and $2f_1$-f_2, third order inter-modulation products, are the most critical as they may fall within the channel bandwidth and interfere with the desired signal [29], [30]. The inter-modulation distortion to carrier signal power ratio is usually measured and used to characterize the PA nonlinearity.

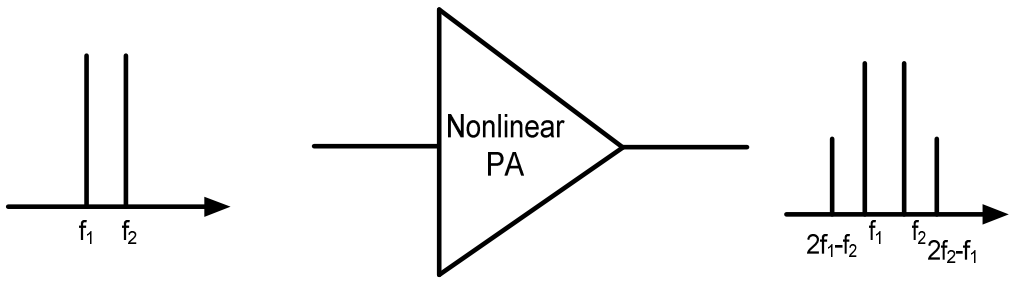


Figure 9. Third Order Inter-modulation products

A great deal of effort has been employed to design high efficiency power amplifiers satisfying the required linearity on the transmitter side. Different classes of operation and more advanced transmitter architecture have been developed [28].

1.2.2. RF Power Amplifier Classes of Operation

1.2.2.1. Linear Power Amplifiers

Depending on biasing and matching network conditions, the RF PA can operate at different classes. Each class of operation has its own tradeoff between linearity and efficiency. Among all the different classes, class-A is known as the simplest and most linear PA, but the least efficient class of operation.

Figure 10 shows the schematic of a class-A amplifier. I_{DC} is the transistor quiescent current.

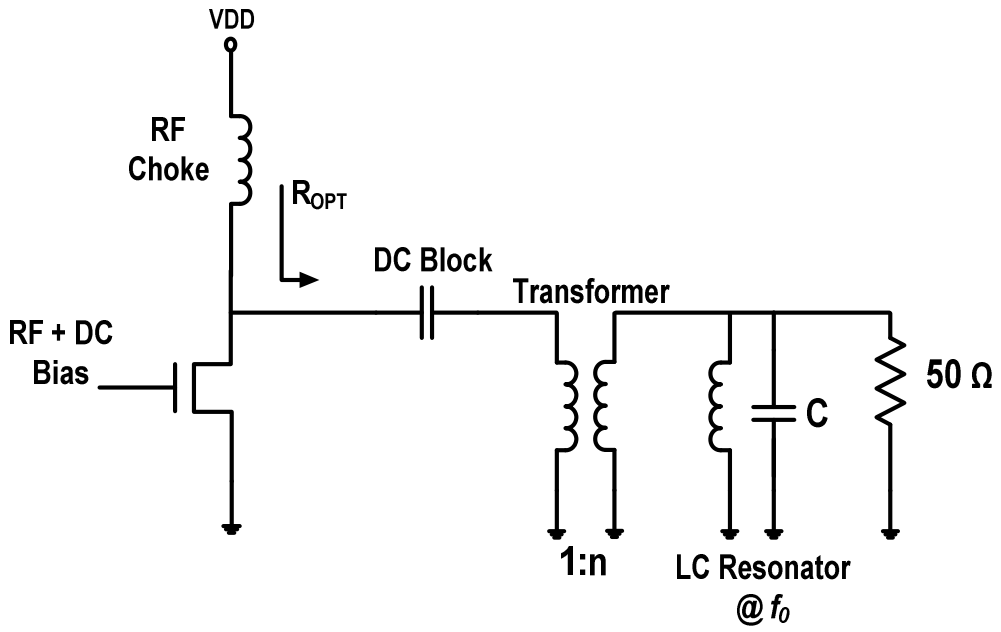


Figure 10. Class A amplifier

The main assumption in a class-A design is that the bias levels are chosen so that the transistor operates in the linear region and has 360 conduction angles [32]. This condition implies that the transistor passes the entire waveform at the input. In theory, class A does not add any distortion to the signal, but in practice the amplifier gain is a function of input power. So large signal swing at the gate causes gain variation which is a source of distortion.

The matching network between the FET drain and load has an inherent filtering effect which improves the out of band harmonics suppression. It also transforms the load impedance; 50 Ohm is used in most of the cases, to the desired impedance seen from the drain at the fundamental frequency. Maximum output power (Pout) of a class-A amplifier is derived in Equation 5.

$$P_{MAX} = \frac{V_{DD}^2}{2 \times R_{OPT}}$$ Equation 5

This shows that the maximum output power depends on supply voltage and the impedance presented to the transistor by the matching network. Theoretically, the peak class-A efficiency is 50%, when the DC current (I_{DC}) is equal to the RF signal amplitude (I_{RF}). Equation 6 shows class-A drain efficiency under the above conditions [28].

$$DE = \frac{P_{out}}{P_{DC}} = \frac{I_{RF}^2(R_{opt}/2)}{I_{RF}V_{DD}} = \frac{I_{RF}(R_{opt}/2)}{V_{DD}} \xrightarrow{Max\ I_{RF}R_{opt}} DE = 50\%$$ Equation 6

Based on the above formula, to improve the efficiency, the DC current has to be decreased. One method is to decrease the conduction angle of the waveform which ultimately distorts the output signal. Deviating from a 360 degree conduction angle changes the class of operation from class A to class AB, B, C, with better efficiency. Figure 11 shows different classes of operation depending on quiescent current (I_D). Vgs is DC voltage across the transistor gate. Also their efficiency versus conduction angle is plotted in Figure 12. Class C gives the highest efficiency at the cost of significant nonlinearity [28], [30], [31], [32].

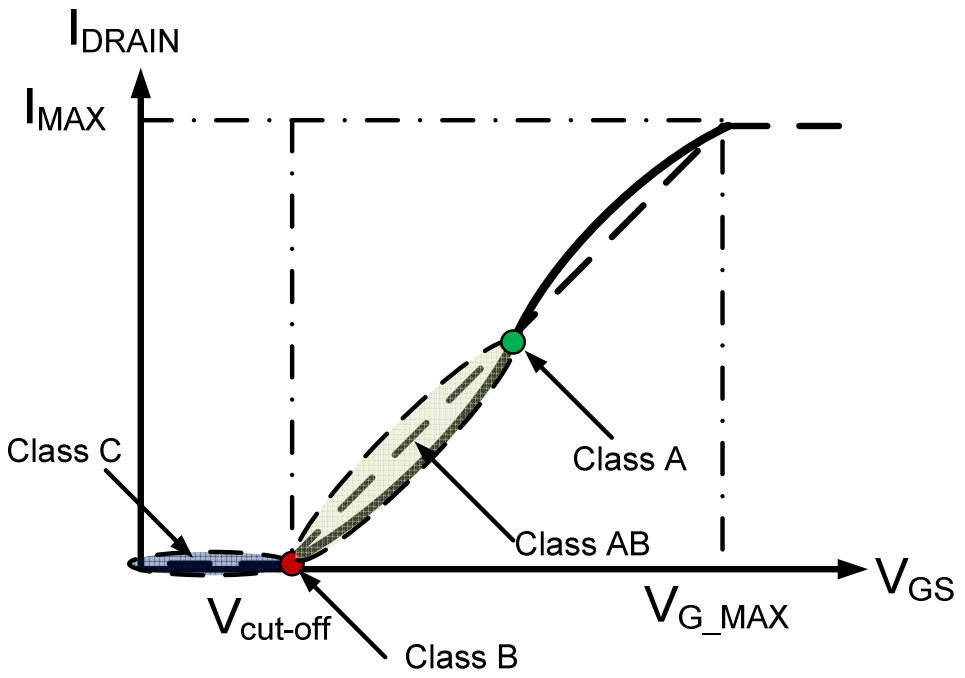


Figure 11. The quiescent bias point on the transistor transfer characteristic [28].

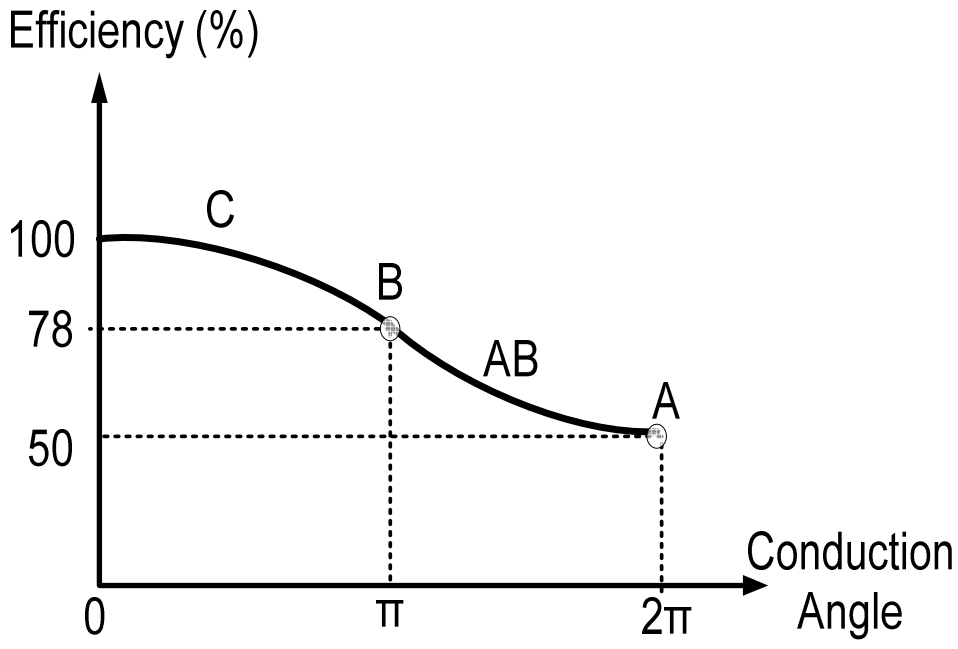


Figure 12. PA efficiency vs class of operation [28].

All the above calculations were done based on the fact that the RF transistor is ideal. However, in practice $r_{ds}=\infty$, $V_{KNEE}=0$, $G=\infty$ and maximum P_{OUT} do not happen. An example of a class-A PA design using a non-ideal transistor explained here shows how efficiency and linearity degrades based on our device choice.

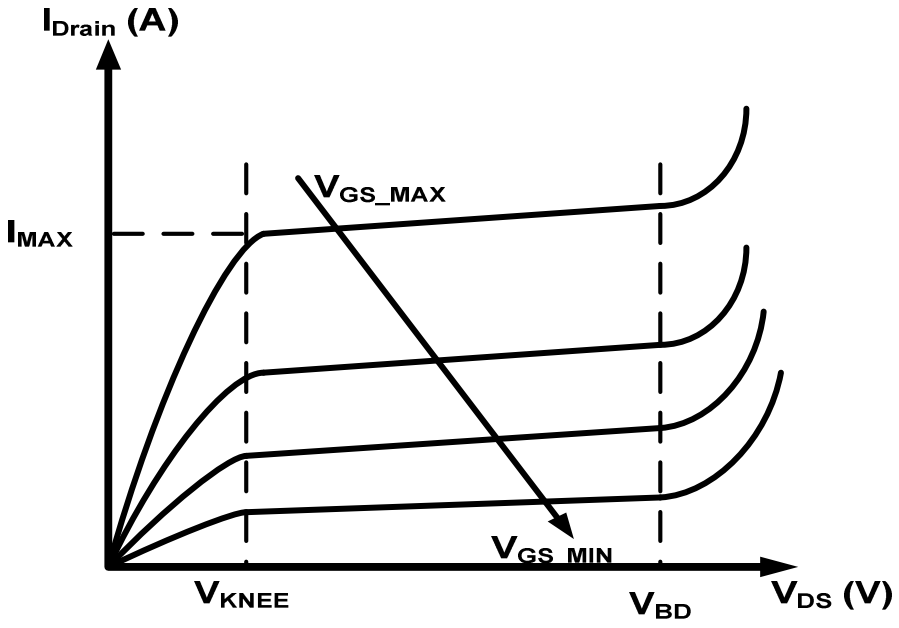


Figure 13. Transistor Family of Curves

An example of a more realistic transistor family of curves (FOC) is shown in Figure 13. The drain voltage swing is limited to V_{BD} from the top and V_{KNEE} from the bottom. For example, if $V_{KNEE}=0.5V$ the peak to peak voltage swing is reduced to 2.5V instead of 3V for the ideal case. Drain efficiency decreases as the knee voltage increases. In this example it drops by 9%:

$$DE = \frac{V_{DD}-V_{KNEE}}{V_{DD}} \xrightarrow{This\ example} DE = 41\% \qquad \text{Equation 7}$$

Another consideration is transistor gain at GHz frequencies. Figure 14 shows an example of the maximum available power gain for a transistor versus frequency. For this example, the maximum power gain at 1GHz is assumed to be 10 dB. Putting this number in the PAE equation (4), the peak PAE of class-A in this example drops to 37%, comparing to the 50% of an ideal transistor.

$$PAE = DE \times \left(1 - \frac{1}{G}\right) = 41 \times (1 - 0.1) = 37\% \qquad \text{Equation 8}$$

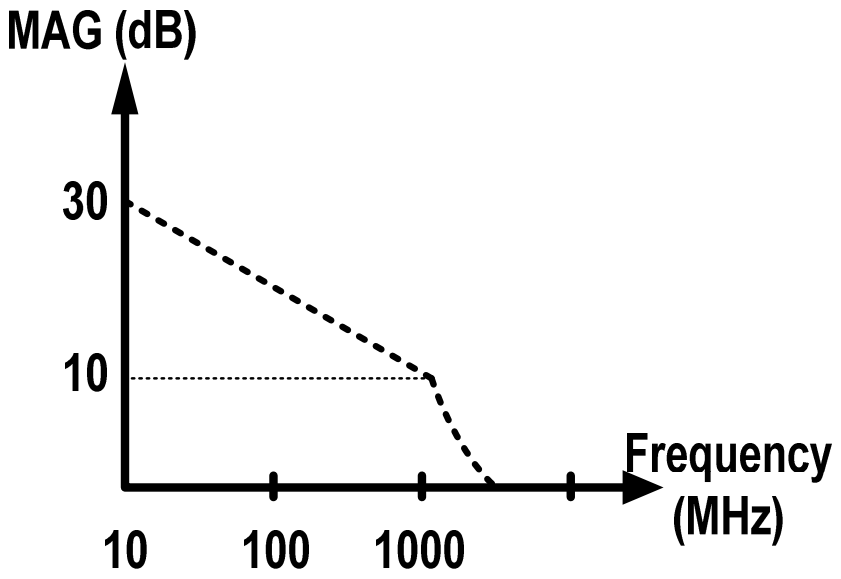


Figure 14. Transistor power gain versus frequency.

Maximum available frequency, f_{MAX}, is the point where the gain plot crosses the x-axis, corresponding to MAG=0 dB. Typically, to achieve 10dB of power gain, a device with 5-10X higher f_{MAX} than the desired operational frequency is needed. Measurement results in Chapter II shows that most of the fabricated MESFETs have a f_{MAX} greater than 10GHz, which is enough for a 2.5 GHz PA application.

Another practical design consideration is the peak output power. Based on Equation 5, for a fixed V_{DD}, the peak P_{OUT} would increase by reducing R_{OPT}. The ratio of R_{OPT} over R_L is defined as the impedance transformation ratio, r. If the supply voltage reduces by a factor of two, then r should increases by a factor of four to achieve the same power. High r values though increase matching network sensitivity, loss and reduce the PA bandwidth [30], [31], [32].

Impedance transformation can be done using different topologies. A few of the most commonly used transformers on CMOS technology, L-matched, T-matched and π-matched networks, are shown in Figure 15. The following calculations are based on an L-network, which has the minimum number of passive components.

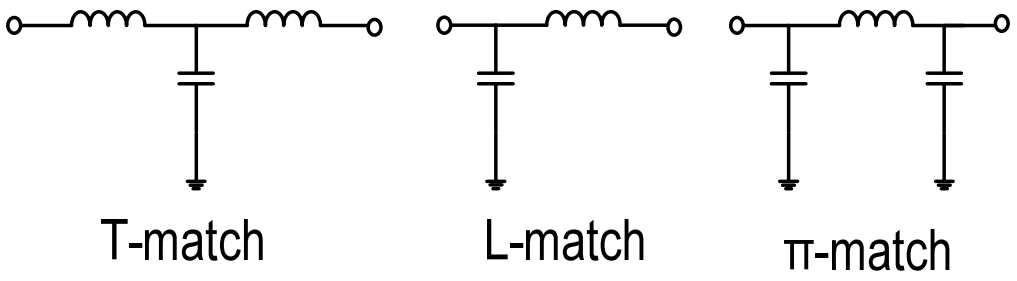


Figure 15. Different impedance transformers using lumped components.

A detailed analysis of the transformer is discussed in [31], pages 119-130. There, the quality factor, Q, of the matching network is defined as:

$$Q = \sqrt{r - 1} \qquad \text{Equation 9}$$

Knowing Q and the quality factor of inductors, Q_{IND}, the efficiency and bandwidth of the transformer can be calculated, where the f_0 is the center frequency:

$$\mathrm{BW} = \frac{f_0}{Q} \qquad \text{Equation 10}$$

$$Efficiency_{Transformer} = \frac{1}{1 + \frac{Q}{Q_{IND}}} \qquad \text{Equation 11}$$

Figure 16 shows the efficiency of the matching network versus different inductor quality factors and impedance transformation ratios. A typical Q value number for a high quality, on-chip inductor on a CMOS process is around 10-15. Therefore, the matching network of a 1W single transistor class-A PA on a 45nm CMOS technology has less than 60% efficiency, which is due to the high impedance transformation ratio and low quality inductors on CMOS processes. The previous examples in this Chapter show that peak class-A PAE, considering gain and kneevoltage non-idealities, is around 37%. Based on Figure 16, this value is much lower, 19-22 % after the matching network.

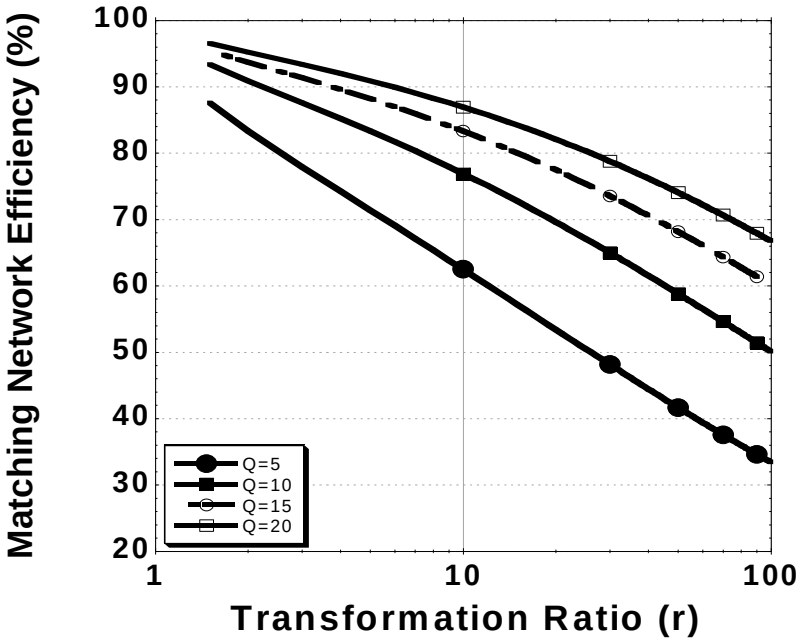


Figure 16. Matching network efficiency versus impedance transformation ratio for different inductor quality factors.

1.2.2.2. High Efficiency Power Amplifiers

All the above calculations show that a practical class A efficiency can be much lower than the 50% calculated in Equation 6. There is a tradeoff between efficiency and linearity. When the linearity constraints are somewhat relaxed, it is definitely better to aim for higher efficiency. Figure 12 shows how efficiency improves based on bias conditions. Another approach to achieve high efficiency is through a proper matching network design. Class F, F^{-1} are the examples of very energy efficient amplifiers which are designed based on waveform engineering and harmonic tuning at the load. An example of inverse class-F circuit is shown in Figure 17.

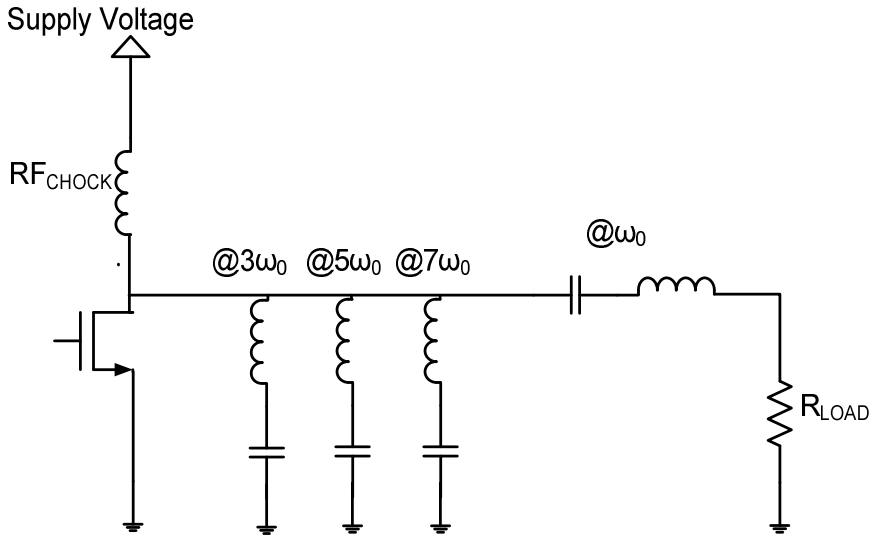


Figure 17. Inverse Class F Amplifier

The series LC resonators at the drain act as short circuit at odd harmonics of the center frequency (ω_0). For infinite number of resonators, the drain voltage waveform consequently appears ideally as a (half) sinusoid and the current waveform as a square wave [30], [31], [32]. Example of a voltage and current waveform at the drain/collector of an ideal inverse class-F amplifier is shown in Figure 18. 100% efficiency is ideally achievable. In practice, due to transistor parasitics, the finite quality factor of matching components and the finite number of resonators this value degrades more than 15%. The factor also depends on the device technology and fabrication process and materials used.

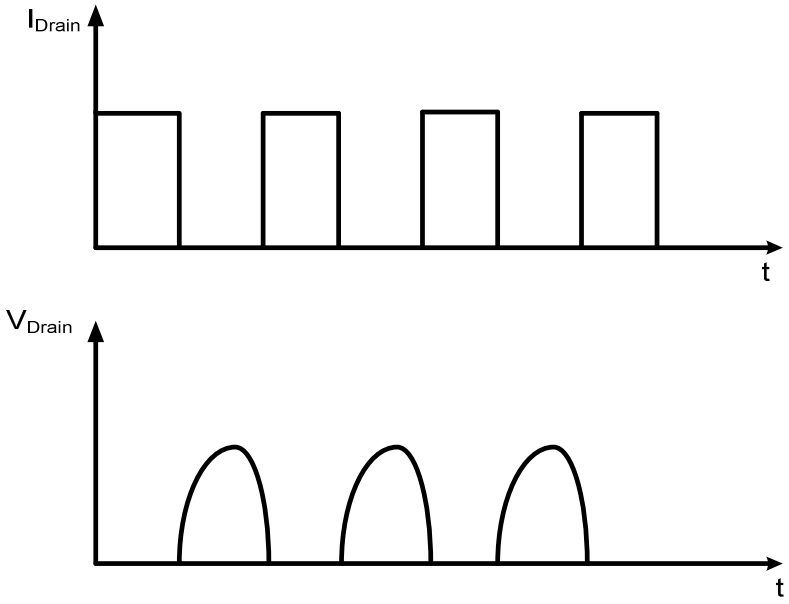


Figure 18. Class F drain waveforms

Switching amplifiers are another example of high efficiency amplifiers. Linear amplifiers like class A, AB, B or C are designed based on the transistor transconductance which is acting as voltage dependent current source. Since a pseudo class-E amplifier is designed in this work, the theory behind this class of operation is described in more detail in ensuing sections.

Unlike these classes, in switched mode PAs, the transistor is operating as a switch having two states; ON or OFF. In theory they can achieve almost 100% efficiency by satisfying the following condition; when the transistor is turned ON, the voltage across the switch is almost zero, and high current is flowing through the device [30], [31], [32]. In other words, the transistor acts as a low resistance (closed switch) during this first part of the period. When the transistor is turned OFF, current through the switch is zero, and a high voltage is applied across the device, i.e. the transistor acts as a high resistance (open switch) during the other

part of period. For this reason, SMPAs such as classes D, E are inherently nonlinear but highly efficient. All these classes ideally achieve 100% power efficiency with nonzero output power [30], [31], [32].

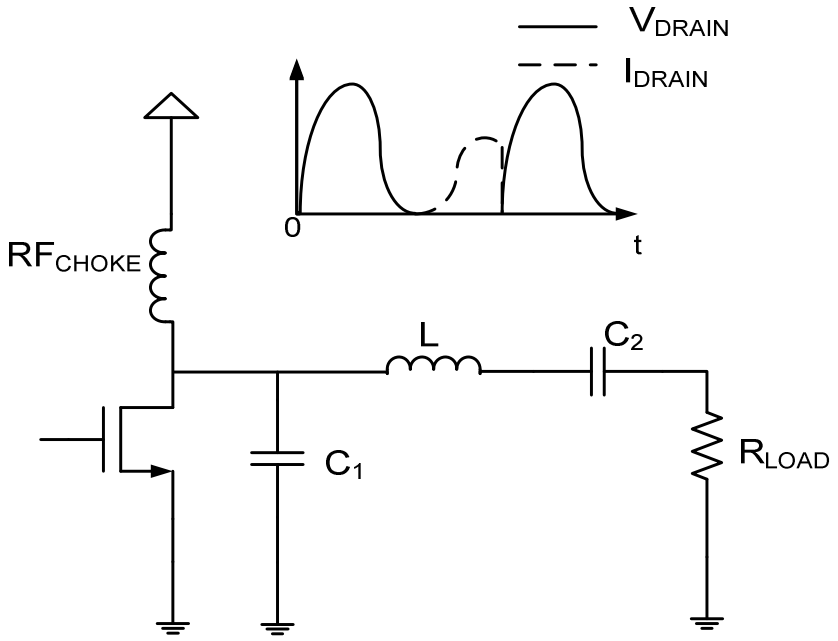


Figure 19. Class E amplifier with lumped elements matching network

The simplest form of class E topology is sketched in Figure 19 [28]. The RF choke provides a DC path to the supply voltage and has very high impedance at high frequency. High efficiency is achievable under zero voltage switching (ZVS) condition. Figure 20 shows a simplified class E. The transistor is replaced with a switch and the inductor is split into two inductors L_a and L_b. (L_a-C) resonates at desired center frequency [28].

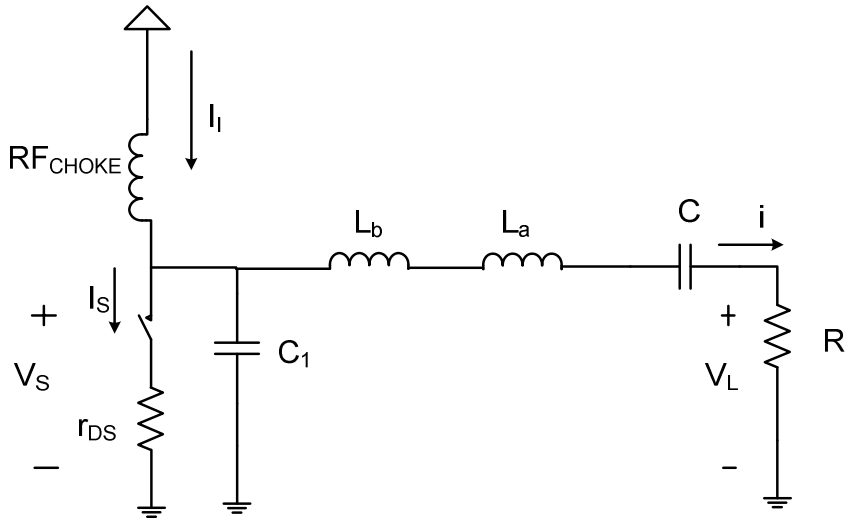


Figure 20. Simplified class E amplifier

Referring to the "RF power amplifier" book [31], section 5.6.4, satisfying the ZVS condition results in the following formulas for the inductor and capacitors.

$$C_1 = \frac{8}{\pi(\pi^2+4)\omega R} = \frac{0.1836}{\omega R} \qquad \text{Equation 12}$$

$$L_b = \frac{\pi^2-4}{2(\pi^2+4)\omega^2 C_1} \qquad \text{Equation 13}$$

$$P_o = \frac{V^2}{R}\frac{8}{(\pi^2+4)} \qquad \text{Equation 14}$$

Class E operation is not guaranteed for the whole frequency range. There is a maximum frequency (f_{max}) of operation which is:

$$f_{max} = 0.05066\frac{P_o}{V^2 C_o} \qquad \text{Equation 15}$$

As Equation 8 shows, the class E output power (P_o) depends on load resistance R. Lower resistance gives higher output power. On the other hand, efficiency goes down as the resistance decreases. Besides the analysis which is

only valid for class E operation, higher impedance transformation results in higher loss in the matching network.

Figure 21 plots the relation between class E efficiency and load resistance.

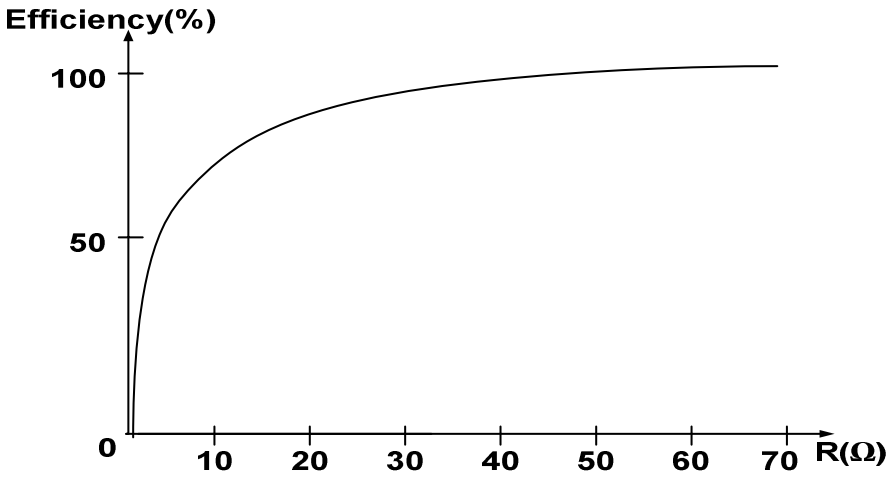


Figure 21. Class E efficiency vs load resistance [28].

As it was discussed class E, F and inverse F improves the peak efficiency, however in many applications the average power is much less than the peak output power. There are more advanced transmitter architectures, such as polar transmitter and Doherty amplifiers that improve the average efficiency. Few of these methods will be overviewed in the last chapter of this thesis. A novel high efficiency transmitter based on MESFET characteristics will also be proposed [28].

1.3. Summary and Discussion

Problems associated with RF power amplifier design on deep submicron CMOS technologies were discussed and SOI-MESFET was presented as an

alternative cheap solution. The SOI-MESFET device structure, behavior and its advantages and disadvantages comparing MOSFET devices on the same process were compared. The effect of device non-idealities on the PA performance, like PAE, gain and P_{OUT} were then overviewed.

The following chapters will talk about measured characteristics of SOI-MESFET devices and how they impact power amplifier design using this technology. To demonstrate the idea of MESFET PA, a few RF output stages have been fabricated and measured. Their results will be presented in subsequent chapters. A fast and low cost approach to design these circuits is to start with simulations. Therefore, a compact large signal model was developed for measured devices.

CHAPTER 2

CHARACTERIZATION AND MODELING

Circuit design, and more specifically RF circuit design, would not be possible without knowing accurate characteristics of active and passive devices over a wide range of frequencies. Moreover, having a compact computer aided design (CAD) model reduces the design cost and time to market. The accuracy of the model is dependent on the precision of the measurements and its capability to capture non-idealities. Thus to have a solid design based on simulations, the MESFETs need to be well characterized in advance. DC and RF characterization of SOI-MESFETs are discussed in this chapter. A scalable compact large signal model is also developed for our fabricated devices.

The MESFETs have been fabricated at different SOI-CMOS technology nodes and foundries. Two of the earlier MESFET demonstrations made use of partially depleted (PD) SOI technologies at the 600 nm [22] and 350 nm CMOS technology nodes [20], [27]. In this chapter recently taken data from PD-MESFETs fabricated on 150 nm and 45nm SOI CMOS processes will be presented. These devices represent the most aggressively scaled and highest performing Si-MESFETs to date with gate lengths as short as 150 nm. Where it is applicable, the results are compared to those from devices fabricated using the earlier 350 nm process. This comparison between different foundries provides insight into the MESFETs performance improvement from one technology node to the next.

2.1. DC Characterization

The SOI MESFETs are depletion mode devices, thus they have negative threshold voltage. An example of a MESFET drain and gate current versus gate voltage at a fixed drain voltage for four different devices is shown in the Gummel plot in Figure 22.

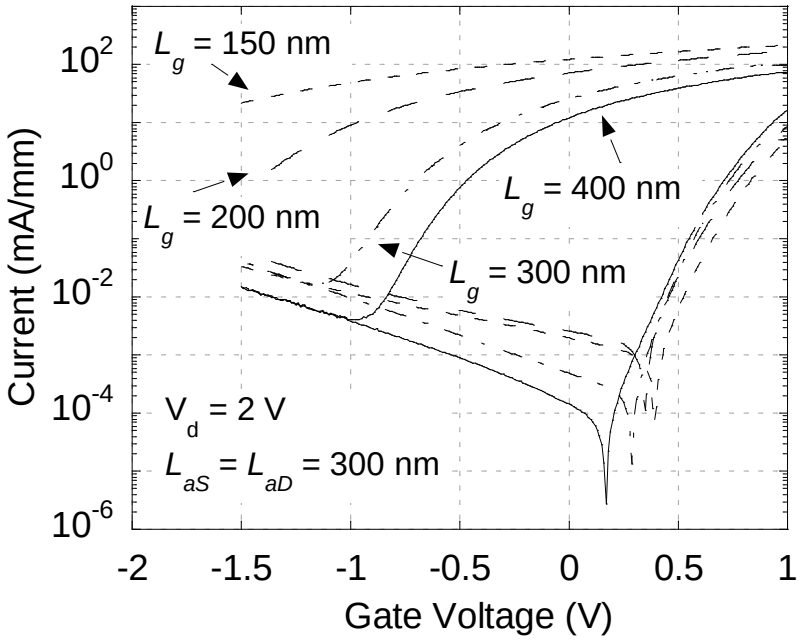


Figure 22. Gummel plots for L_G=150, 200, 300 and 400 nm on a 150 nm SOI CMOS technology.

From Figure 22 it is evident that the aggressively sized gate lengths on the 150 nm process can be affected by short channel effects (SCE). The gate length at which SCE ceases to be an issue becomes clearer in Figure 23 which extracts the threshold voltage, V_t, for various MESFETs. From the figure we conclude that gate lengths $L_g \geq 400$ nm are required to avoid SCE altogether in the 150 nm technology, while $L_g \geq 600$ nm is required for the 350 nm process. Presumably,

the SOI channel in the 150 nm technology is thinner and more heavily doped than in the older 350 nm technology which allows the MESFETs to be scaled to shorter gate lengths before SCE become significant. This observation is consistent with the threshold voltage model developed by Chiang *et al.* for short-channel SOI MESFETs [33], [27].

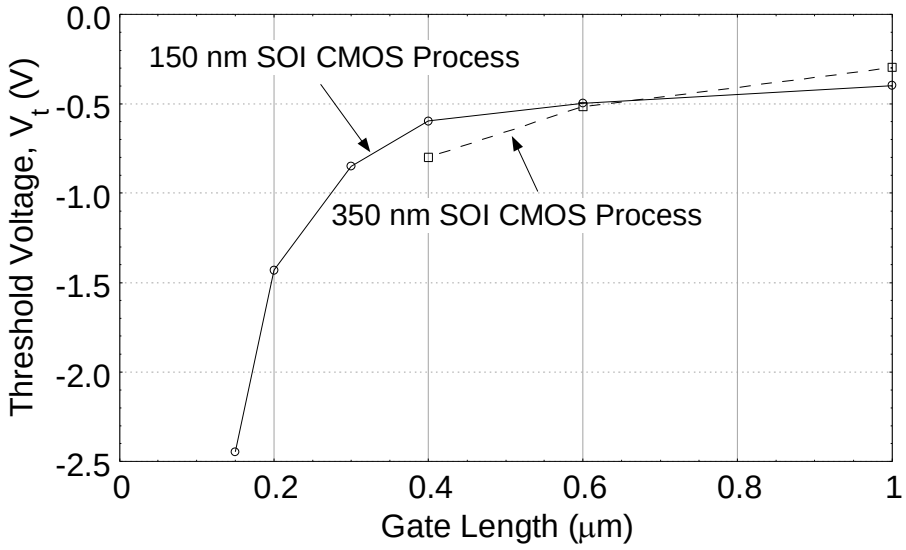
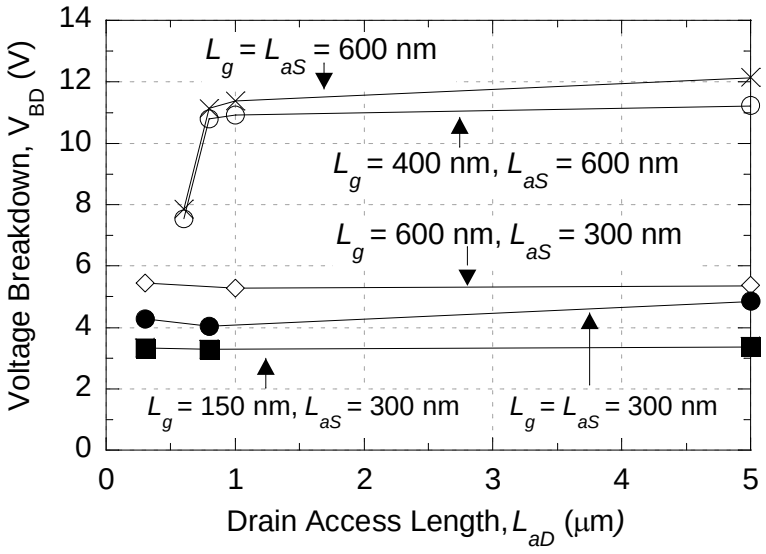
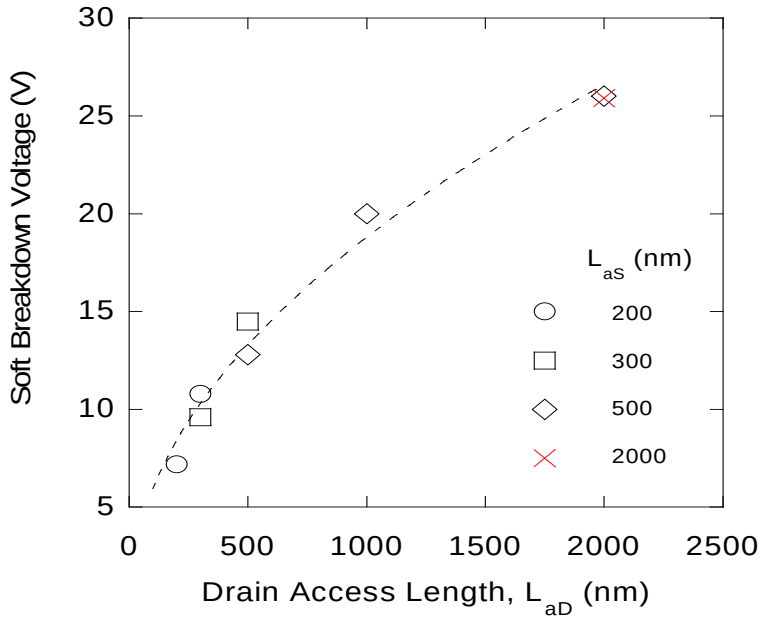


Figure 23. Threshold voltage extracted for each of the devices fabricated on 150nm and 350nm technologies.

MESFETs have a much higher breakdown voltage compared to the MOSFETs on a same process. The breakdown measurement approach used in this work is based on the drain-current injection technique [34]. The biasing metric of 1 mA/mm was used as the constant current source forced into the drain. Breakdown voltage measurements for the MESFETs on 45nm and 150nm SOI CMOS technologies are shown in Figure 24.



(a)



(b)

Figure 24. The breakdown voltage of MESFETs (a) on a 150nm SOI process. (b) on a 45nm SOI process. Dashed line shows the trend and the red cross shows to the peak measured breakdown voltage.

To date the peak measured breakdown on the 150 nm process was ~12 V and ~28 V on a 45nm process. These are considerably lower than ~55 V [22] achieved on the 350 nm process. The reason for the significant drop is likely the results of several different factors. Among them are channel doping, channel thickness, and various implants introduced on deep submicron processes that may not have been blocked during layout, but are not seen on the 350 nm process. Overall, MESFETs have shown 2-30X higher V_{BD} than standard MOSFETs. As a reference, the maximum steady-state operating voltages of the standard CMOS devices is 0.9 V, 1.95 V, and 3.5 V for the 45 nm, 150 nm and 350 nm processes respectively. V_{BD} improvement is not free of charge, and we will see in the subsequent chapters how it affects the RF performance of the proposed MESFETs.

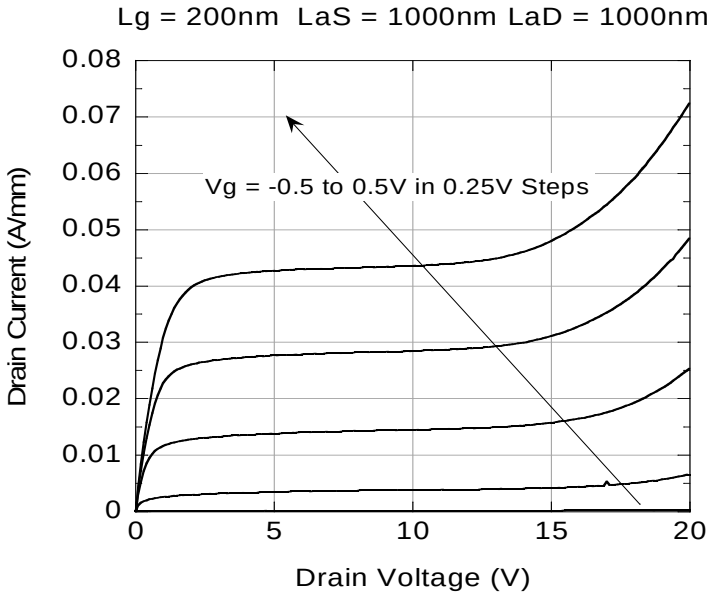


Figure 25. The family of curves for an enhanced V_{BD} MESFETs with L_G= 200nm, $L_{aS} = L_{aD}$ = 1 µm. The gate voltage is stepped from +0.5V (uppermost curve) to -0.5V in 0.25V steps.

To visualize the explained breakdown voltage improvement, FOCs, for a high V_{BD} MESFET on a 45nm technology, are plotted in Figure 25.

2.2. RF Characterization

RF characterization was performed by on-wafer probing using select devices with ground-signal-ground (GSG) pad configurations. Also included on the die was an accompanying set of open- and short-circuit test structures to de-embed the devices and remove the parasitics of the GSG pads. Measurements were taken using Agilent 8510C vector network analyzers. From the de-embedded S-parameters, WinCal [35] was used to extract the cut-off frequency, f_T, of the MESFETs which was defined as the point where current gain, $|h_{21}|^2$, equaled 0 dB [27].

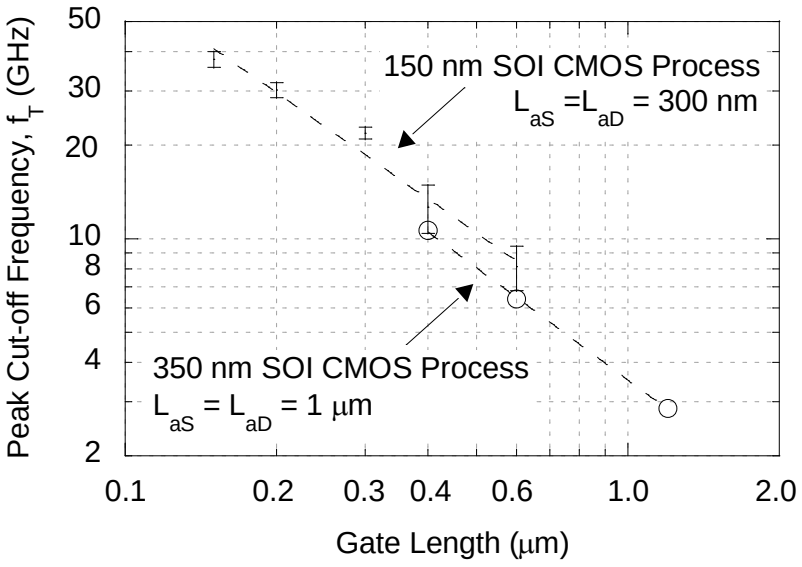


Figure 26. Shows the exponential scaling of the peak cut-off frequencies for MESFETs manufactured using different SOI CMOS processes.

Similar to a MOSFET, the cut-off frequency depends on gate length. The f_T trend is shown in Figure 26. This graph shows the measured peak f_T for various gate lengths on different SOI CMOS technologies. Cut-off frequency is a function of device transconductance and gate capacitance:

$$f_T \cong \frac{1}{2\pi}\frac{g_m}{C_{GS}} \qquad \text{Equation 16}$$

C_{GS} decreases as gate length shrinks and at the same time g_m improves as well. However, L_{aS} and L_{aD} can also significantly affect the MESFET transconductance. From a circuit perspective, L_{aS} and L_{aD} appear as parasitic resistances in series with the channel of the MESFET [36], [27]. Source resistance degenerates the device transconductance and results in lower g_m. This directly affects the f_T performance of a MESFET. Figure 27 shows the measured R_S and the peak f_T versus access length for MESFETs with the same gate length. As expected, f_T reduces by increasing L_{aS}.

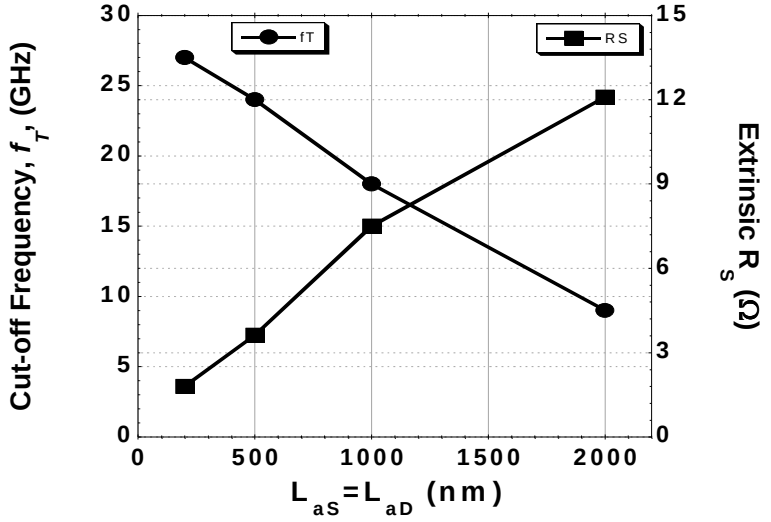


Figure 27. The peak cut-off frequency and R_S as a function of L_{aS} for MESFETs fabricated on a 45nm SOI CMOS technology.

Cut-off frequency is a widely used term in the literature for evaluating RF performance of a technology. However, maximum available gain (MAG) and f_{MAX} are more critical parameters for RF power amplifier designers. The breakdown voltage also plays an important role. As shown in Figure 24, V_{BD} depends mainly on L_{aD} for a fixed L_G, and it improves by enlarging the drain spacer, L_{aD}. The effect of L_{aD} and other parasitics on MESFET RF and breakdown voltage performance is presented below:

f_{MAX} is a function of cut-off frequency but it also depends on the gate to drain capacitance and gate resistance as well [31]:

$$f_{MAX} \approx \sqrt{\frac{f_T}{8\pi C_{GD} R_G}} \approx \frac{1}{4\pi}\sqrt{\frac{g_m}{C_{GD} C_{GS} R_G}} \qquad \text{Equation 17}$$

Based on Equation 17, f_{MAX} depends on g_m, R_G, C_{GD} and C_{GS}. R_S also appears in the MESFET source and reduces the overall transconductance by degenerating the intrinsic g_m. Hence, it is important to calculate these parasitics for different MESFET geometries. R_G, R_D and R_S can be considered extrinsic components; therefore they do not depend on the biasing conditions. A well-known method called cold-FET extraction [37] is used in this work to measure these extrinsic resistances. Measured resistances versus L_{aD} for various fabricated MESFETs are shown in Figure 28. R_S and R_G do not change with L_{aD} for a fixed L_{aS} and L_G, therefore the MESFET's f_T and f_{MAX} remain constant.

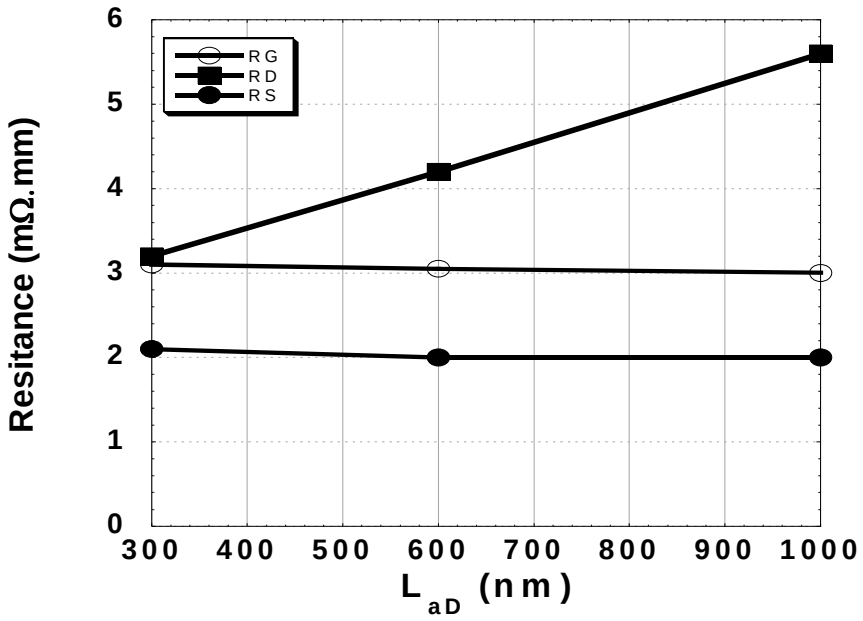


Figure 28. Measured extrinsic resistances versus L_{aD} for MESFETs with L_G=400 nm and L_{aS}=300nm on a 150 nm process.

Intrinsic capacitances also affect the MESFET f_{MAX}. Figure 29 shows that L_{aD} does not change C_{GD}, while C_{GS} and g_m scale proportionally with L_{aD}. Overall, increasing L_{aD} does not degrade the MESFET RF performance and benefits it in the form of higher breakdown voltage. It should be mentioned that there is a limit on the V_{BD} improvement by just changing L_{aD} as it is shown in Figure 24.a. Furthermore, increasing L_{aD} increases the overall layout area which can be significant in a high current device.

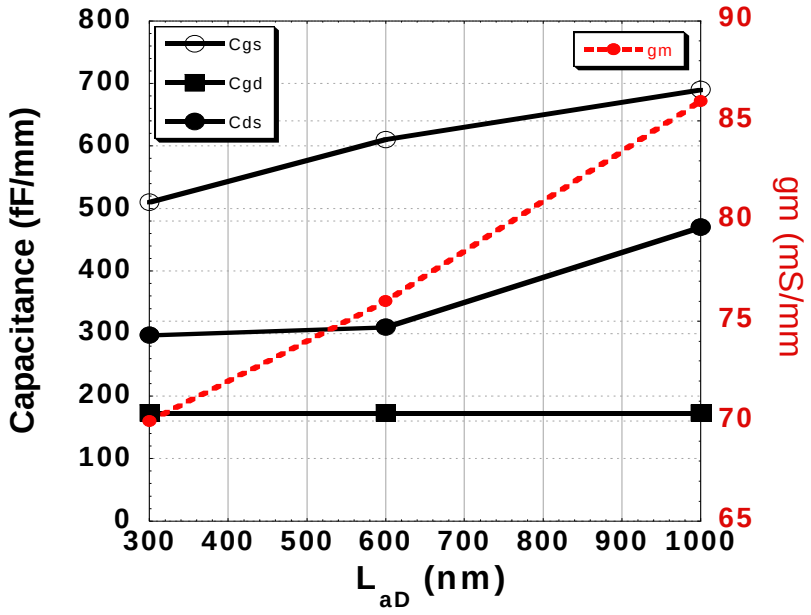


Figure 29. MESFETs intrinsic capacitances and g_m versus L_{aD} for MESFETs with L_G=400 nm and L_{aS}=300 nm on a 150nm process.

The above discussion underlines the importance of appropriately sizing L_{aS} and L_{aD} for specific applications. Measured MAG for different MESFETs is plotted in Figure 30. All the measured devices have more than 15dB available gain for frequencies less than 2.5 GHz, which is an adequate amount of gain for most RF PA applications. The peak measured f_{MAX} on the 45nm process is ~35GHz for MESFET with L_G=L_{aS}=L_{aD}=200nm.

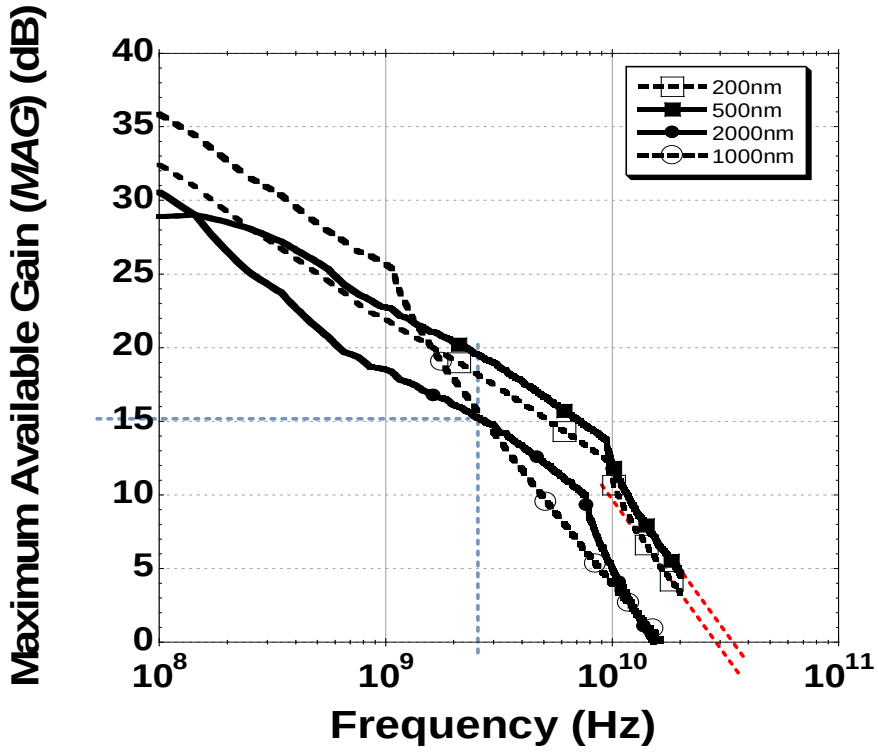
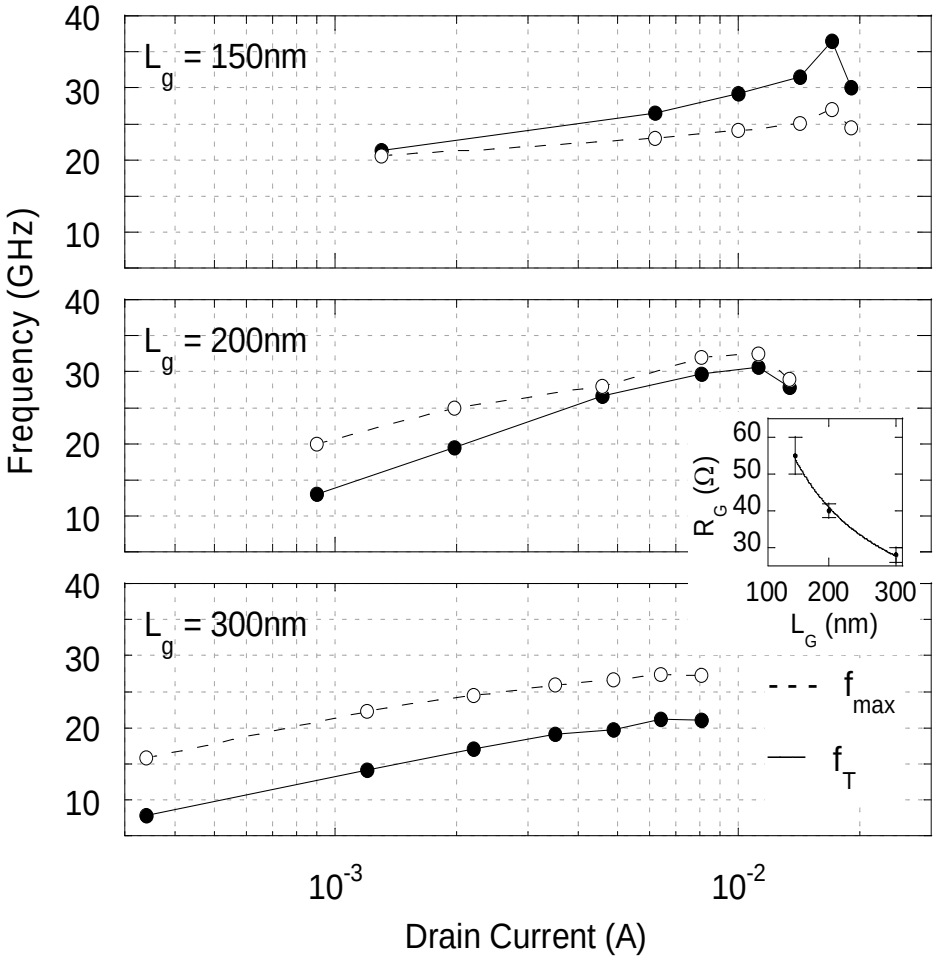
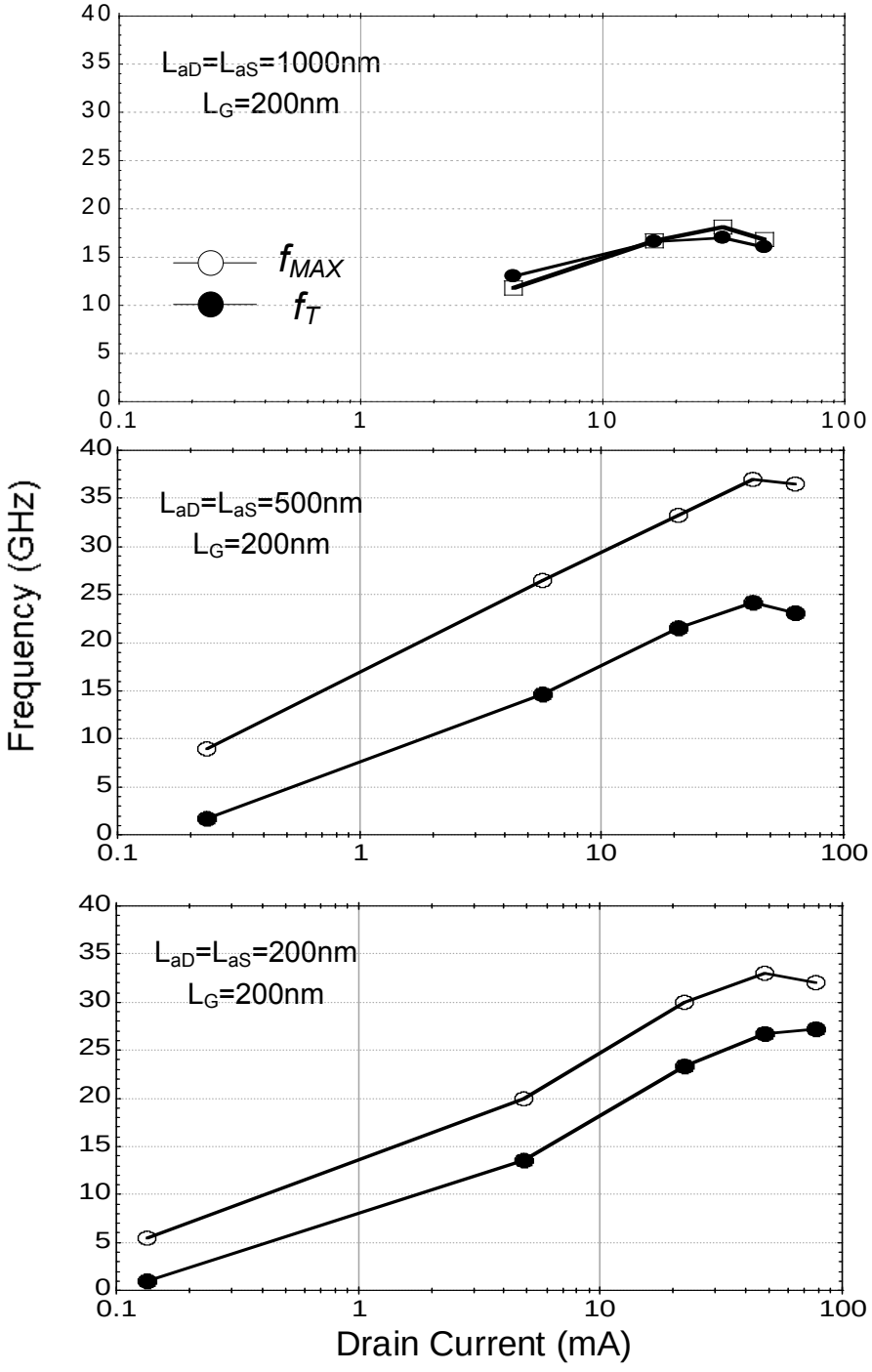


Figure 30. Measured MAG versus frequency for different MESFETs on a 45nm SOI CMOS process.

The measured cut-off frequency and f_{max} for a few selected devices on 45nm and 150nm processes is plotted in Figure 31 as a function of drain current. The results from the 150nm MESFETs show the impact of R_G on f_{max} as the gate lengths is scaled. It can also be explained using the f_{max} approximation in Equation 17. Values for R_G have been extracted for each device using the cold-FET technique and are shown in the inset to Figure 31. A power law fit shows that R_G varies proportionally with $1/L_G$ as indicated by the solid line in the inset. For the 300 nm gate length device the peak f_{max} is ~30% higher than the peak f_T. However, as R_G increases with decreasing L_G this trend is reversed, with the peak f_{max} of the 150 nm device being 30% lower than the peak f_T.


Frequency (GHz)
40
30
20
10
L_g = 150nm
L_g = 200nm
L_g = 300nm
R_G (Ω)
60
50
40
30
100 200 300
L_G (nm)
f_{max}
f_T
10^{-3}
10^{-2}
Drain Current (A)

(a)



(b)

Figure 31. shows the cut-off frequencies and f_{MAX} versus drain current for selected devices (s) on the 150 nm SOI CMOS process (b) on the 45nm SOI CMOS.

2.3. TOM3 Modeling

Simulation is an essential part of circuit design as it greatly reduces the design time and considers non-idealities of a device or technology. Device behavior and non-idealities should be accurately captured and reflected in device models for circuit simulation. Various compact models have been developed for different fabricated MESFETs. The modeling process and approach is the same for all our devices. The following describes the compact model developed for one of the SOI MESFETs fabricated on a 45nm SOI CMOS process.

Silicon MESFETs were fabricated at a commercial 45nm semiconductor foundry with L_{aS} = L_{aD} = 100nm, L_G = 184nm and gate width L_W = 300µm. Initially, twenty different devices were measured using a DC probe station and an average device was chosen to fit a model to. This device showed the most average gate, drain and source currents compared to all measured results. The TriQuint Own Model, TOM3 [38], was chosen to model the results because it is an extension of the Curtice-Statz [39] model and most importantly has a continuous expression for drain current across sub threshold, linear and saturation regions of device operation. Additionally, the model is widely available for different circuit simulators including Agilent ADS and Cadence. Figure 32 shows the circuit schematic of the complete TOM3 model [40].

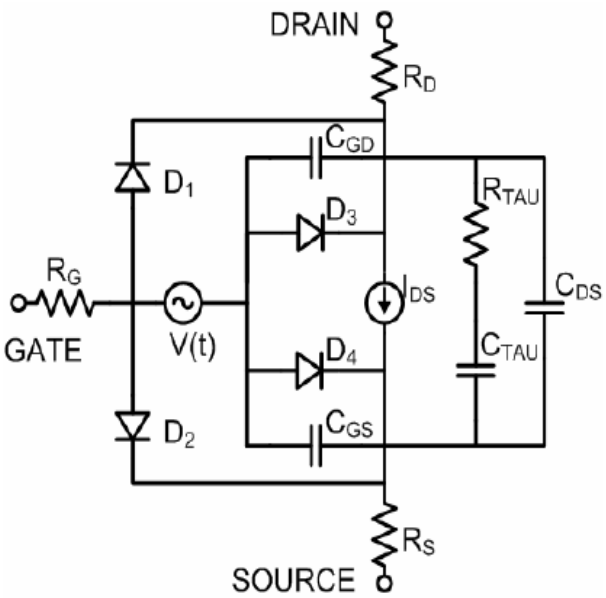


Figure 32. TOM3 model circuit schematic [38].

As the first step, extrinsic components, such as R_G, R_D and R_S, are extracted using cold-FET techniques explained in [37]. Measured extrinsic resistances versus frequency are shown in Figure 33.

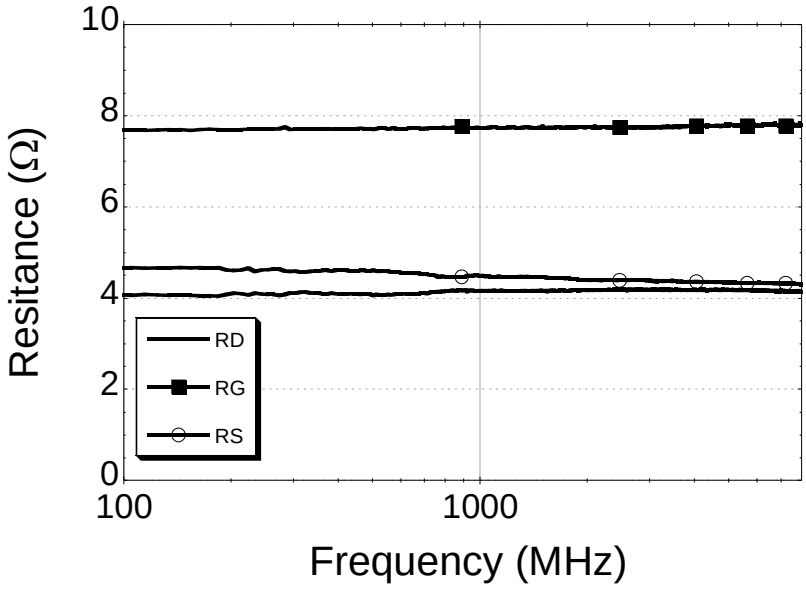


Figure 33. Measured extrinsic R_D, R_S and R_G versus frequency.

2.3.1. DC Model Characterization

First, the model was developed to describe the device operating at DC and then charge parameters were determined for RF as described in the subsection below. Initially, family of curves measurements were used to fit the model to the drain current of the MESFET, which is described in the TOM3 model equations as

$$I_{ds} = \beta \times (V_G)^Q \times f_k \times (1 + \lambda V_{ds}) \quad \text{Equation 18}$$

where β is the transconductance, V_G is a scaled nonlinear voltage as a function of region of operation, Q is the power generalizing the square-law, f_K relates the saturation parameter α approximately as

$$f_k \approx \tanh(\alpha Vds) \quad \text{Equation 19}$$

where V_{ds} is the drain to source voltage and λ is the channel length modulation parameter. V_G can initially be thought of as the gate voltage in a simple square-law, but is in fact determined nonlinearly in the model as a function of internal gate diode voltage, threshold voltage and drain voltage. Figure 34 shows the model fit (open circles) to measured data (solid line) for the fabricated MESFET with V_{ds} to 4.5V and V_{gs} from -0.5 to 0.5V. It is important to note that the nominal MOSFET device operating voltage is less than 1V for this process.

The transconductance in units of mS/mm as a function of gate voltage is plotted in Figure 35 from low (0.1V) to high (4V) drain biases [40].

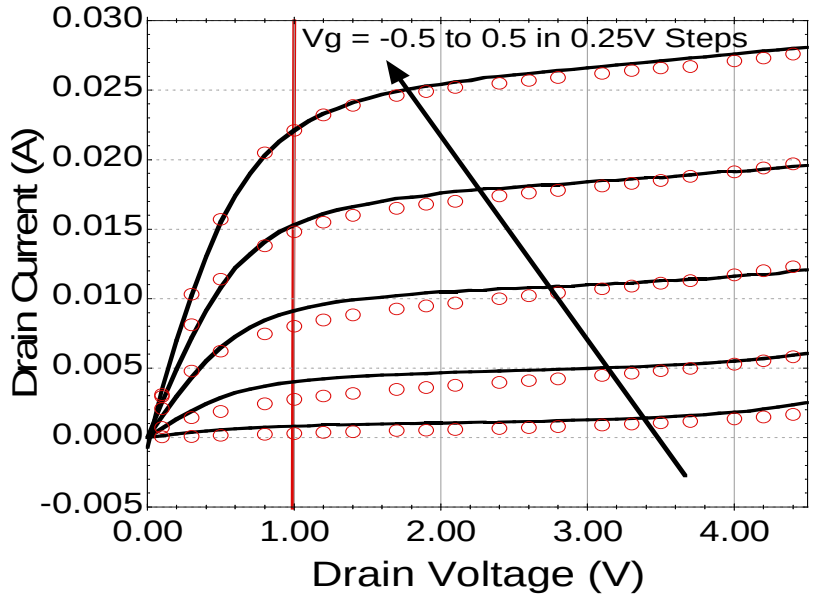


Figure 34. Measured (solid line) and simulated (open circles) results for the silicon MESFETs fabricated on the 45nm SOI process. The line at 1V represents the approximate maximum operating voltage of MOSFETs on the same process [40].

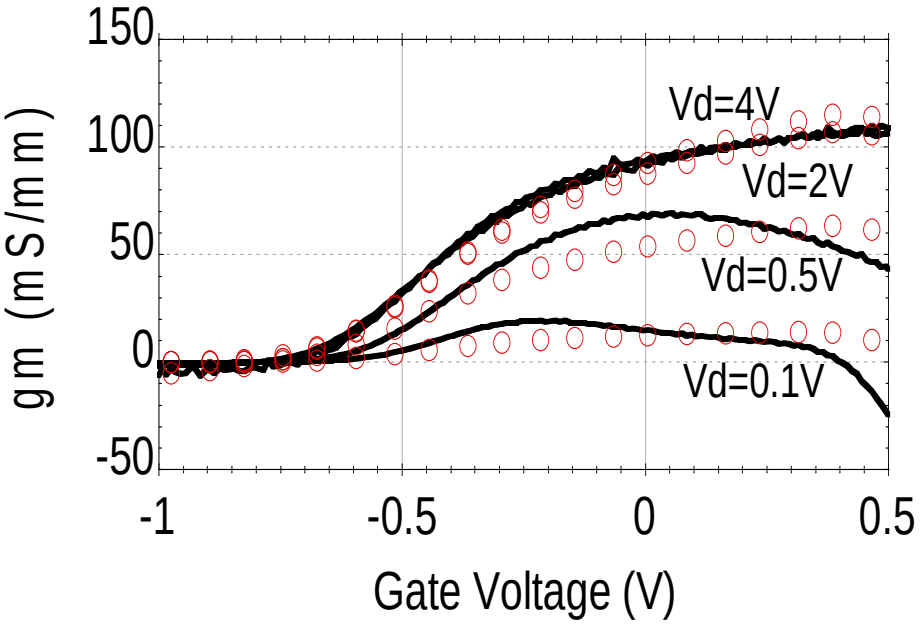


Figure 35. Measured (solid) and modeled (open circles) transconductance.

In order to get a good agreement to the measured data across drain voltages, the solution to f_k must be precise. Using measured data for I_{ds}, we can solve Equation 18 for f_k (Figure 36) to get an empirical fit for α. This enables a smooth and correct transition from linear to saturation region in the model [40].

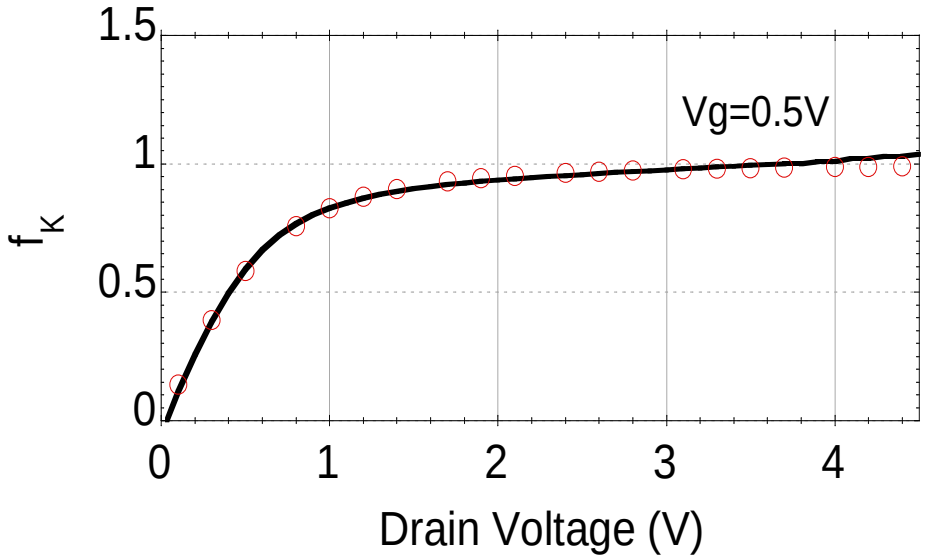


Figure 36. Model fit of the saturation current scaling f_k (circles) compared to extracted f_k from measured drain current (solid line) [40].

After matching the drain current, the next step is to model the gate current, leakage and breakdown of the MESFET which is represented by internal diodes in the TOM3 model (Figure 32 D1-D4). The MESFET gate is a Schottky diode and under forward bias can be determined by the saturation current Is and ideality factor N. Additional diodes depict the leakage current under reverse bias. However, other effects such as edge effects, device doping and DIBL are not completely captured by the model and there is a slight difference in gate current between measured and modeled results. Our current research includes additional methods to capture these effects. Figure 37 shows the measured and modeled

Gummel plots of the MESFET which depict both absolute gate and drain current. The model fits across a wide drain bias range which is critical for reliable simulations [40].

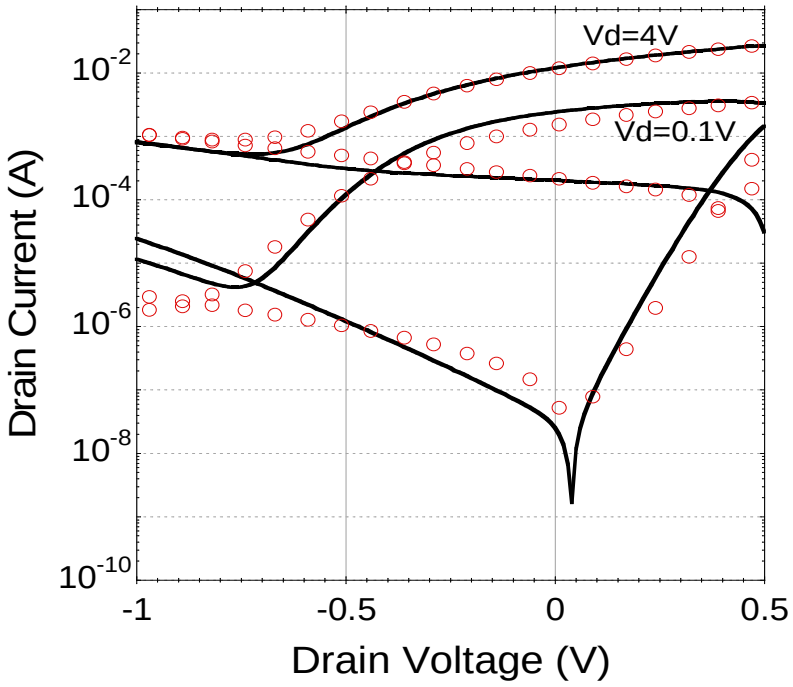


Figure 37. Gummel plots depicting drain and gate current of the MESFET across a wide drain bias range of 4V and 0.1V. Measured results are solid lines and modeled open circles. Additional drain voltages have been omitted for clarity but show a good fit to measured data from Vd = 0 to 4V [40].

2.3.2. RF Modeling

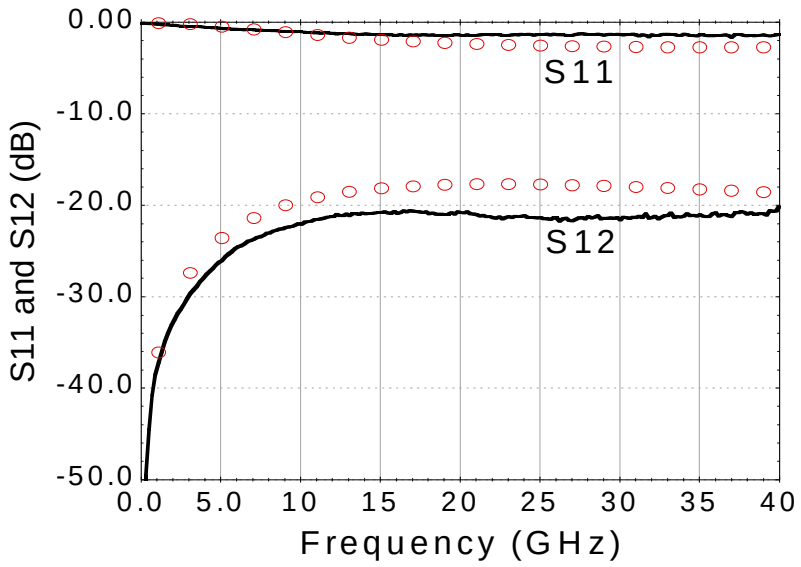
In order to use the model for microwave simulations, charge parameters must be determined to describe the parasitic capacitances of the MESFET Cgs, Cgd and Cds (Figure 32). S Parameter measurements from 100MHz to 40GHz were performed on an RF probe station on GSG MESFET structures also used for the DC model extraction. The total gate charge in the TOM3 model can be described as

$$Q_{GG} = Q_{GL} \times T + Q_{GH} \times (1 - T)$$ Equation 20

where Q_{GG} is the total charge on the gate, Q_{GL} is the low power region function, Q_{GH} is the high power region function and T describes the transition between regions as

$$T = \exp(-Q_{GGB} \times I_{ds} \times V_{ds})$$ Equation 21

with Q_{GGB} as a transition coefficient [40]. In order to get the model to agree across different power levels, Equation 20 is simultaneously fit to the measured S parameters across different gate and drain bias levels. Figure 38 shows measured and simulated S Parameters for a drain bias of 2V and gate bias of 0.25V. The maximum available gain (MAG) and H21 were calculated for both measured and simulated data and are shown in Figure 39.



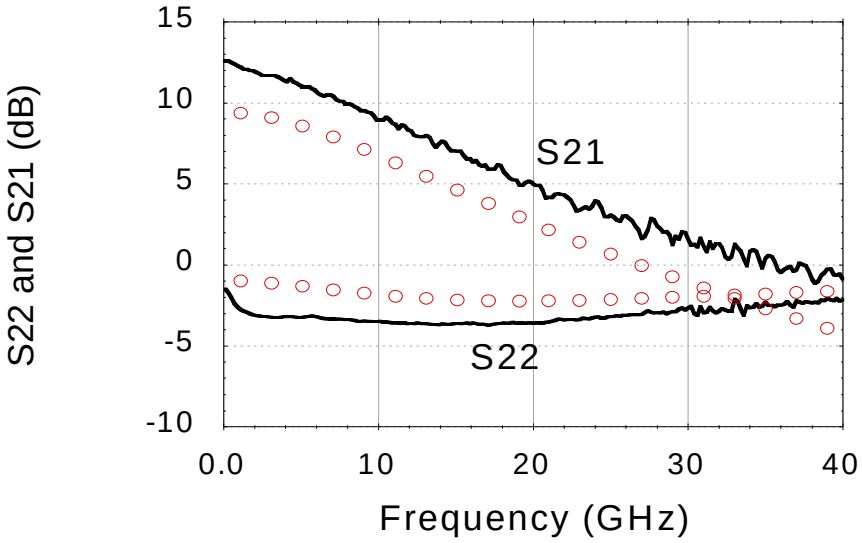


Figure 38. Measured (solid line) and modeled (Open red symbols line) S Parameters at Vd=2V and Vg=0.25V.

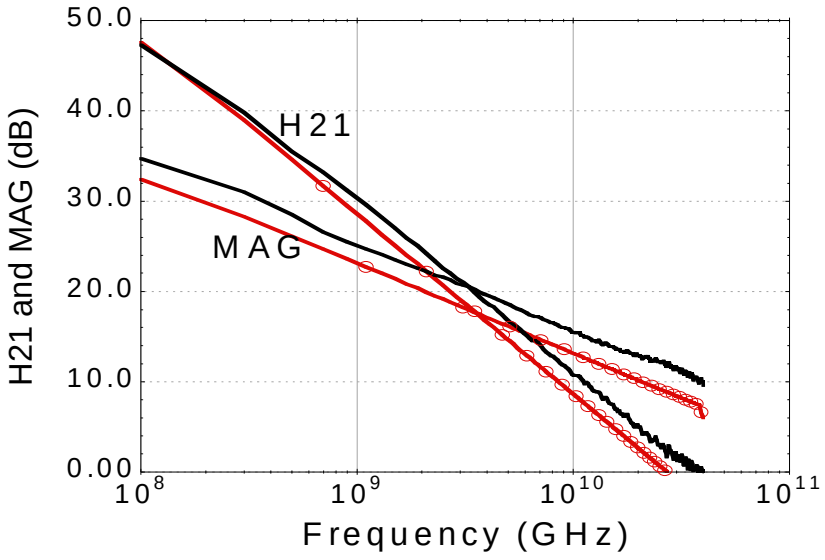


Figure 39. Measured and simulated H21 and MAG at the same bias conditions.

2.3.3. Test Power Amplifier

In order to validate the large signal behavior of our model, a test Class AB power amplifier operating at the ISM band of 433MHz was designed, simulated and then fabricated on an FR4 PCB board. A MESFET device with L_W=2.7mm

was packaged and bonded to a Kyocera A309 package utilizing multiple bondwires to reduce parasitic inductances. The MESFET was chosen so that it would be optimally matched to 50Ω and simplify matching networks for the demonstration. Figure 40 shows the schematic of the PCB board. The power amplifier was tested with a network analyzer that was used to supply varying input power at 433MHz and a power meter to measure the output power. Figure 41 shows the simulated model compared to measured amplifier results for key parameters such as output power, gain, drain efficiency (DE) and power added efficiency (PAE) [40].

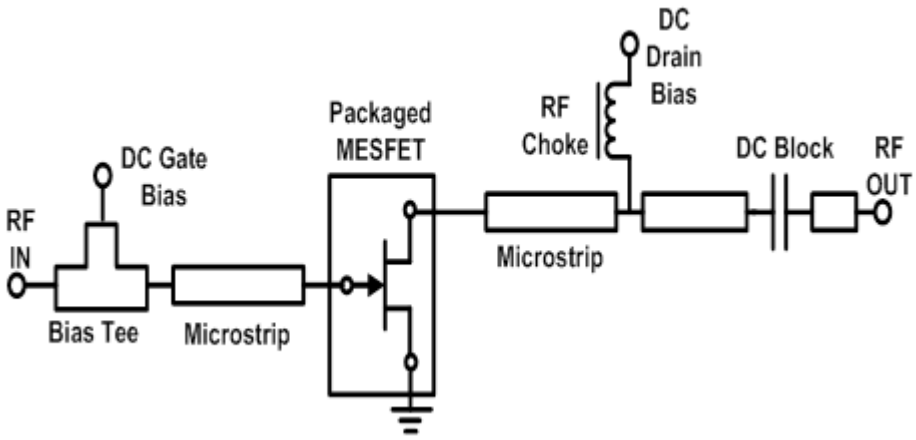


Figure 40. Class AB, 433MHz, RF Power amplifier schematic

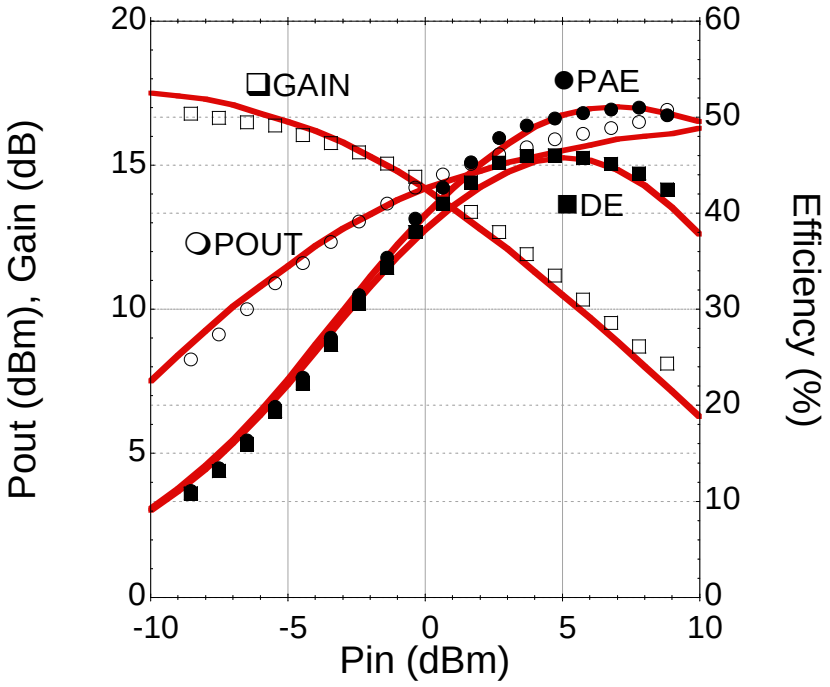


Figure 41. Measured (symbols) and simulated (solid line) of gain, output power, power added efficiency (PAE) and drain efficiency (DE).

2.4. Summary

Various MESFETs fabricated on different SOI-CMOS processes were measured. DC and RF characteristics of these devices were shown in this chapter. The first chapter discussed the need for high breakdown voltage devices on CMOS technologies for power amplifier applications. 2-30X breakdown voltage enhancement were achieved using MESFETs comparing to MOSFETs on the same SOI-CMOS process.

RF measurements proved that MESFETs can be used in power amplifiers operating in the frequency range of DC-2.5GHz. It will be shown in the next chapter that RF performance can be improved at higher frequencies. Also a TOM3 model was developed and validated for silicon MESFETs fabricated on a

45nm CMOS process through simulation of measured devices and a 433MHz Class AB power amplifier.

CHAPTER 3

SOI-MESFET POWER AMPLIFIERS

The design of RF power amplifiers are certainly a complex task. Nevertheless, this complexity, when coupled with extra limitations related to the fabrication technology, can lead to even more challenging design factors. This is particularly true in the case of CMOS power amplifiers in sub-micron technologies. Indeed, one of the main obstacles in new CMOS technologies is the low supply voltage that results in very low output power. In addition, this technology is characterized with a very low drain breakdown voltage that prevents adequate implementation of advanced power amplifier classes of operation, such as class E, due its excessive peak drain's voltage that can reach as much as $3.5\times V_{DD}$. Furthermore, passive RF components, inductors and capacitors, are another source of challenges in a fully integrated CMOS design. This manifests in low quality factor of inductors that leads to excessive losses and consequently to power efficiency degradation. In addition the large size of passive components, when compared to the RF transistors, limits the practical output matching network topologies for fully integrated implementation [28]. Chapter I discussed how the lower breakdown voltage of CMOS transistors lead to a need for more passive components and therefore lower efficiency and higher fabrication cost due to the large die area of inductors. SOI-MESFET devices were introduced as an alternative solution for the limited headroom of CMOS PAs which allows digital and RF circuit's integration on a same silicon die. The first

reported fabricated RF power amplifiers using the proposed SOI-MESFET devices are introduced in this chapter.

Agilent Advanced Design Software (ADS) was used to simulate MESFET RFPAs before fabrication. An advanced simulation tool called Load/Source Pull was used to find the optimum device size, geometry and desired matching network characteristics to achieve the best performance. Load/source pull approach is explained in the following.

A general power amplifier block diagram is shown in Figure 42. The maximum power transfer happens when Z_{OUT} is the conjugate of Z_{DRAIN}. However, the conjugate matching condition does not necessarily result in the maximum efficiency. The first chapter discussed how the efficiency can be improved by either tuning the harmonics of the load or waveform engineering approach. Few classical methodologies like class C, F, F^{-1}, … were introduced that ideally can give 100% efficiency. These RF-PAs are designed based on harmonic tuning in the matching network. The equations and load conditions given for these classes are based on an assumption that the RF transistor is an ideal unilateral device. In practice though, optimum source/load conditions for a packaged transistor, operating at giga hertz range, might be very different than what the class E and F equations suggests. Load/source pull technique helps taking into account all the non-idealities such as finite reverse isolation and gain compression of the RF transistor [28].

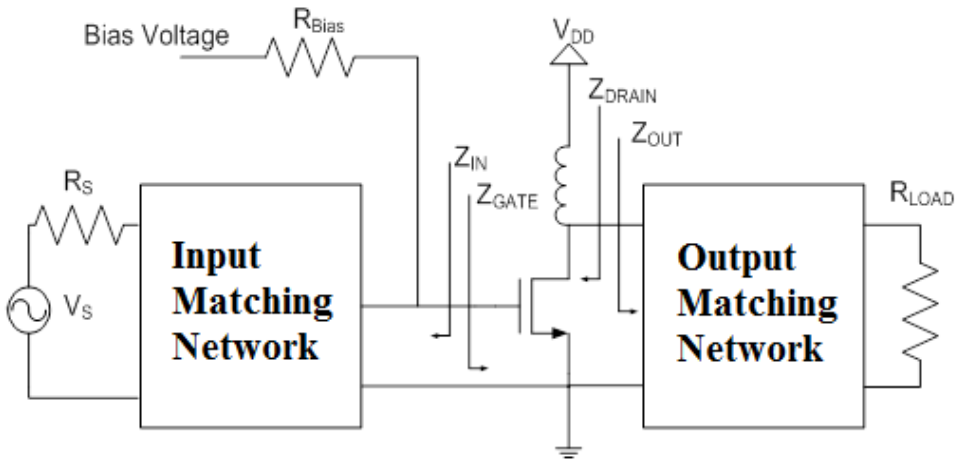


Figure 42. A general Power Amplifier block diagram.

Figure 43 shows a basic block diagram of a load/source pull setup. This technique has been widely used for many years [41] and it is based on impedance tuning at the drain and gate of the transistor to find the optimum source/load conditions. This system can be used to design for the best linearity, efficiency, bandwidth or maximum power delivery to the load. Design steps are the same for all these cases, but the goal function might be different for different applications. The optimization steps are explained below:

Step I: Set initial values for the variable load (Z_{OUT}) and source (Z_{IN}) at the fundamental frequency and its harmonics (3, 4 harmonics).

Step II: Sweep the fundamental load or source impedance all over the smith chart and find a point on the smith chart which gives the maximum PAE, linearity, etc (goal function or solving the existing tradeoffs).

Step III: Change the load/source impedances to the new point calculated in the step II.

Step IV: Sweep the other harmonics at the load and source and perform step II and III (this time for harmonic frequencies).

Step V: Repeat the step III and IV until results converge to the best possible performance.

Step VI: Repeat the step II to V until achieving best possible PAE or goal function [28].

It has to be mentioned that this is not a blind load manipulation approach, and the initial values should be calculated by knowing the RF transistor family of curves, device parasitics and design goals. Biasing conditions and initial values of load at the 2^{nd} and 3^{rd} harmonics can highly affect the final result.

Figure 43. Source/Load Pull Simulation Setup [28].

Load/source pull simulation is used to demonstrate the feasibility of the proposed MESFET power amplifiers. The TOM3 model developed for the fabricated MESFETs has been used for these simulations in ADS. The first fabricated power amplifier using SOI-MESFETs is an overdriven class AB PA operating at 433MHz.

3.1. Wideband Class AB SOI-MESFET RF PA

A MESFET transistor fabricated on a 150nm SOI-CMOS process was used to design an RF-PA operating at the center frequency of 433MHz with more than 40% bandwidth. This device has ~5V breakdown voltage and 22GHz of cut-off frequency. Due to some limitations this device had only one pad for each drain, source and gate terminals. As a result, the RF performance was significantly degraded after packaging. Figure 44 shows the MESFET RF current

and power gains versus frequency before and after packaging. Although the device has more than 15 dB power gain up to 2GHz before packaging, bond wires have extremely degraded the RF gain for frequencies above 500MHz. This problem can be eliminated by adding more bond pads, which has been included in more recently fabricated MESFETs [42].

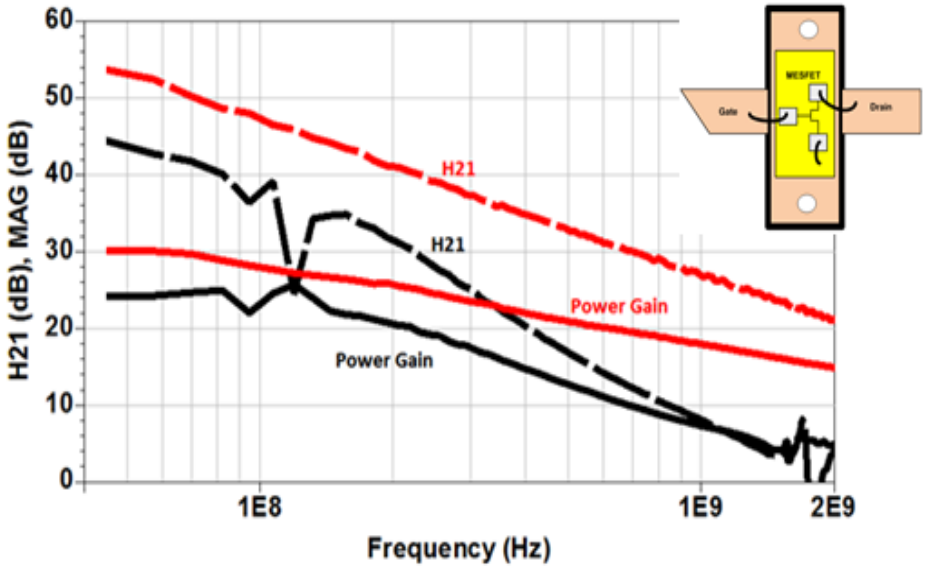


Figure 44. MESFET RF performance before and after packaging. (Red shows before packaging) (Black shows after packaging)

Chapter I discussed how the impedance transformation reduces the overall PA efficiency and limits the bandwidth. High transformation ratio is required when the transistor breakdown voltage is much less than the required voltage swings on the 50 Ω load. Therefore the main advantage of using MESFETs instead of MOSFETs in power amplifiers is relaxing the impedance transformation requisites or even eliminating it whiling meeting the standard requirements. MESFET used in this work has $L_G=L_{aS}=L_{aD}$=300nm and device

width of W=4.2mm. It has a peak drain current of 200mA and can handle up to ~5-6 V. The MESFET's family of curves is shown in Figure 45. A class AB power amplifier operating at 433MHz with peak output power of 19dBm was designed and built using this packaged SOI-MESFET.

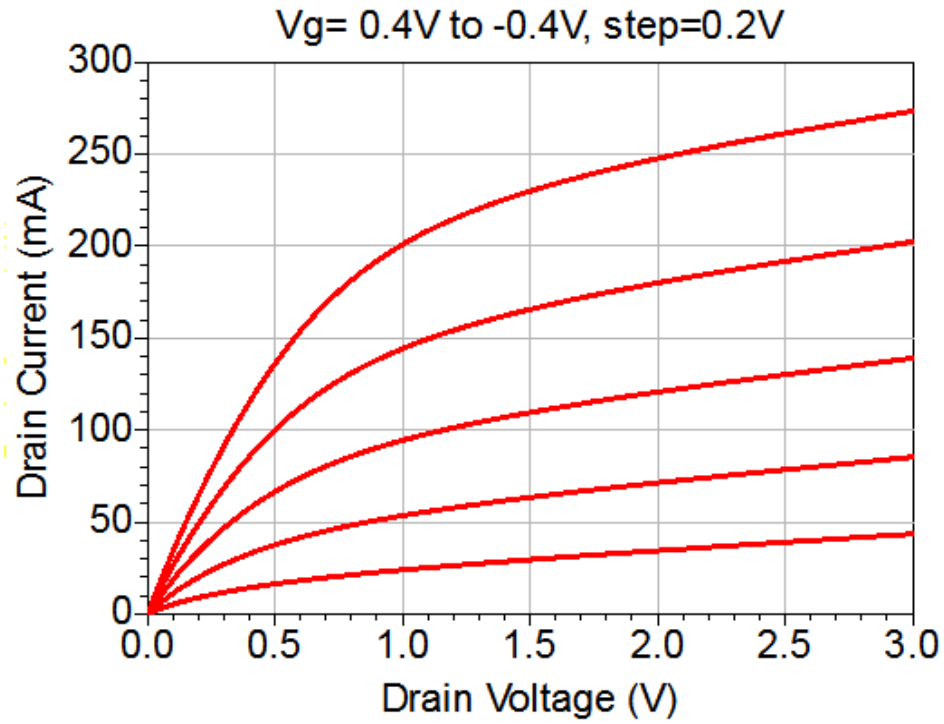


Figure 45. Family of Curves for MESFET with L_G=L_{aS}=L_{aD}=300nm and Width=4.2mm.

A load/source pull simulation has been completed in Agilent ADS using the TOM3 model to find the optimum load/source conditions that give the peak efficiency. Simulated power and PAE contours are plotted in Figure 46. Drain (load) PAE contours (Red) at the fundamental frequency show that a close to ~50 Ω load termination results in the maximum efficiency. The optimum gate impedance that gives the peak PAE and output power is around ~25 Ω. However,

PAE degrades by less than 3% if the source termination of 50 Ω is used instead of 25 Ω. Figure 46 shows the existing tradeoff between power and efficiency [42].

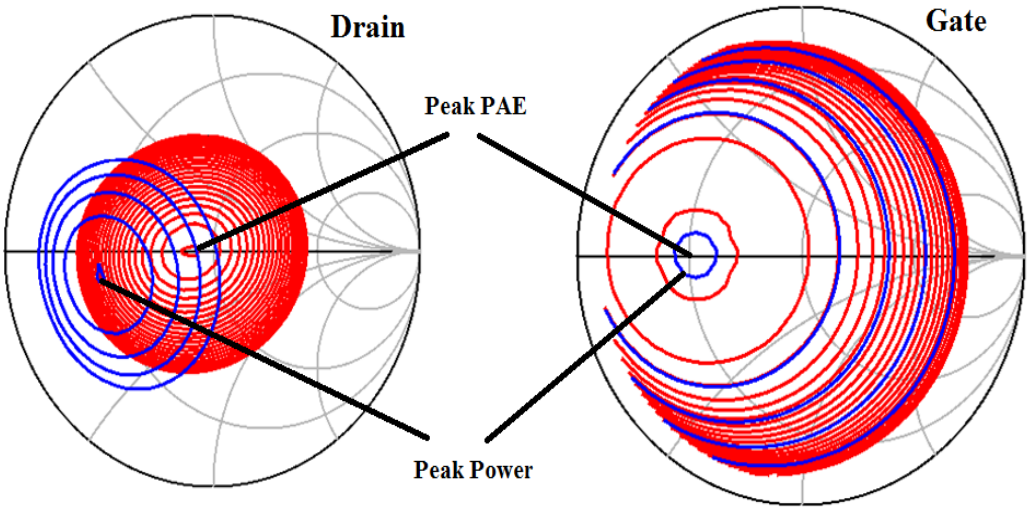


Figure 46. PAE and Power contours at drain and gate. Red shows PAE and Blue is Power contours

Load/source pull simulation results are consistent with load line calculations. A class AB PA based on the above calculations was designed and simulated in ADS. A band-pass series *LC* filter centered at 433MHz is used for harmonic suppression of the class AB PA. Packaging and bondwire effects are included in simulations.

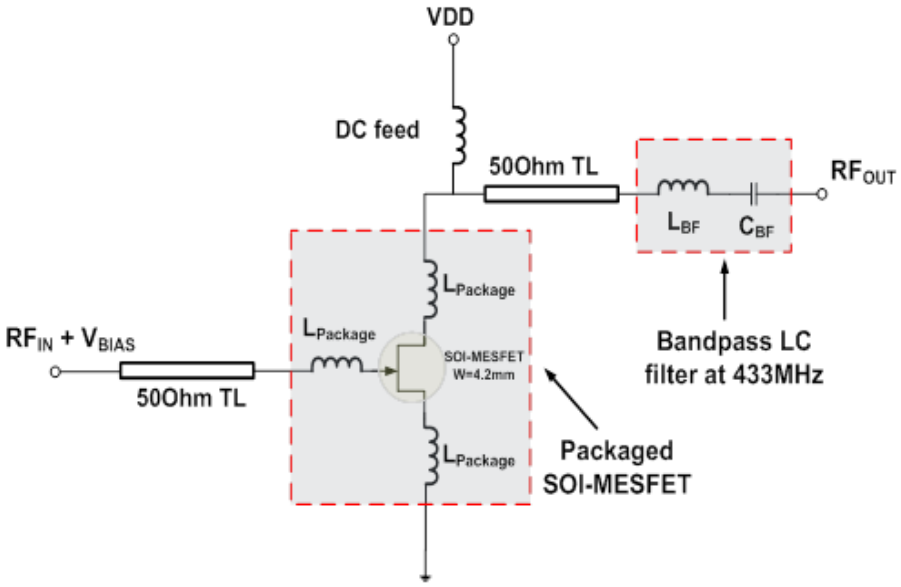


Figure 47. Schematic of the simulated class AB SOI-MESFET PA

The RF PA shown in Figure 47 was simulated in ADS. Power added efficiency (PAE), drain efficiency (DE), power gain and output power are plotted as a function of the input power in Figure 48. The maximum PAE of 58% was achieved [42].

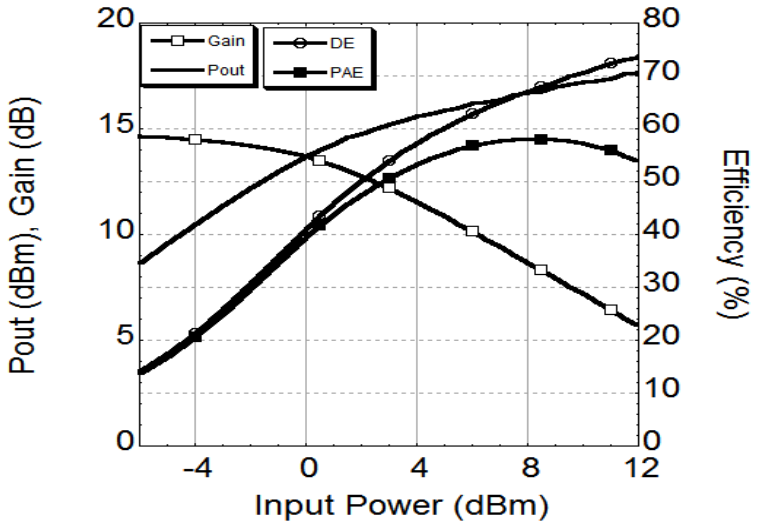


Figure 48. Simulation results of the 433MHz class AB MESFET PA.

The discussed class AB PA was fabricated using FR4 material. A photograph of the PA module is shown in Figure 49. Measurement results are shown in Figure 50. A maximum PAE of 48% was measured while delivering 17dBm to a 50Ω load. Few percent variations between measurement and simulations are due to several reasons. The TOM3 model is initially calibrated using small signal measurements at different biasing conditions, thus nonlinearities might not be captured fully in the model. Additionally, die to die variation, capacitor and inductor models along with inaccuracy in the PCB's model are the other possible sources [42].

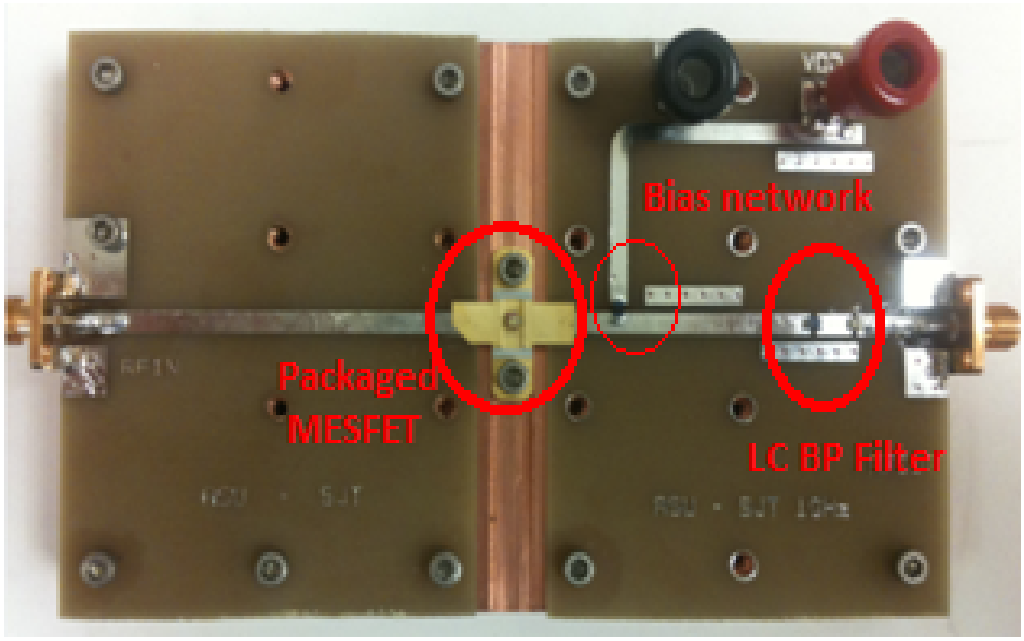


Figure 49. Photograph of fabricated class AB 433MHz SOI-MESFET PA.

The PA linearity was tested by driving it with a GSM signal at 433MHz. The input GSM signal power was increased until it reached the 1-dB compression point of the PA. As specified in the standard, adjacent channel power should be

less than -30dBc with respect to the carrier at -/+200KHz and -60dBc at -/+400KHz. The PA output spectrum was measured from 432MHz to 434MHz and the measurement resolution bandwidth is set to 10kHz. The measured output spectrum is shown in Figure 51 [42].

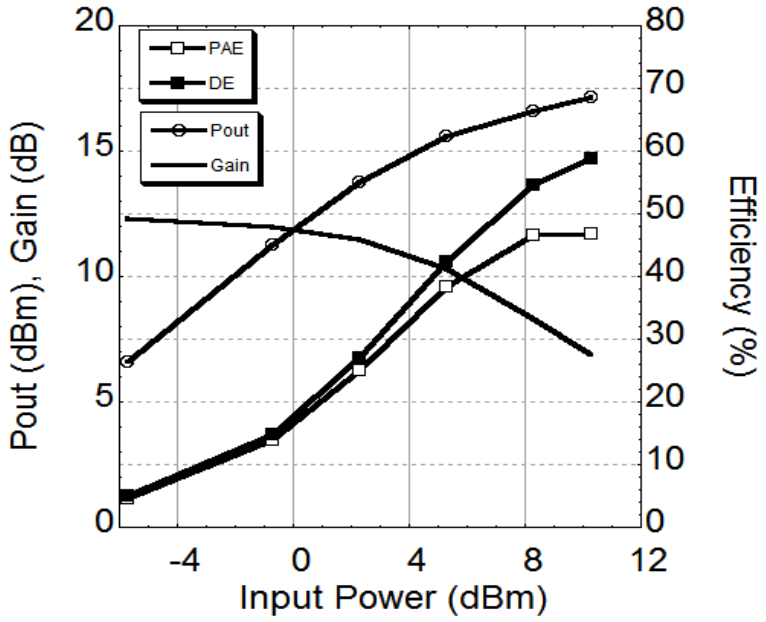


Figure 50. Measurement results of 433MHz class AB MESFET PA.

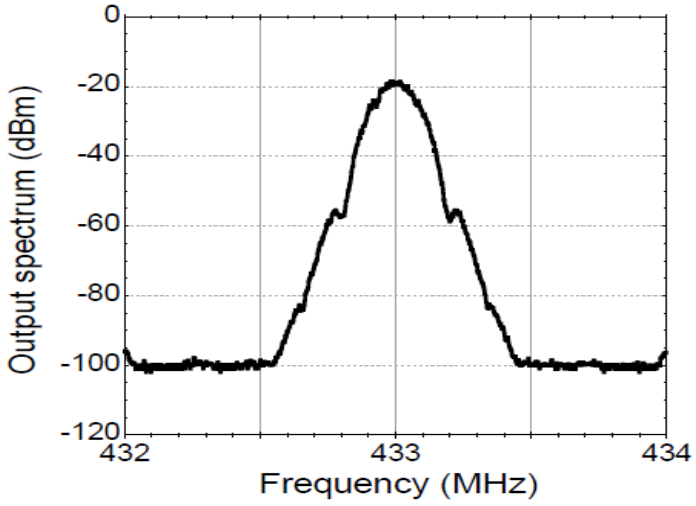


Figure 51. Output spectrum of the MESFET PA driven by a GSM signal.

The matching network bandwidth directly limits the PA frequency response. As it is mentioned before, the load/source-pull simulations show that there is no need for impedance transformation to match this SOI-MESFET device to a 50 Ohm load. As a result, this PA has a high bandwidth of 200 MHz centered on 400 MHz. In this work, the band-pass (BP) filter was designed to suppress harmonics of the RF signal at 400MHz. This limits the overall PA bandwidth, but it can be either eliminated or be replaced with another BP filter and can be used at other frequencies as well. Figure 52 shows measured PA performance versus frequency where the drain efficiency stays above 50% from 280 to 480 MHz [42].

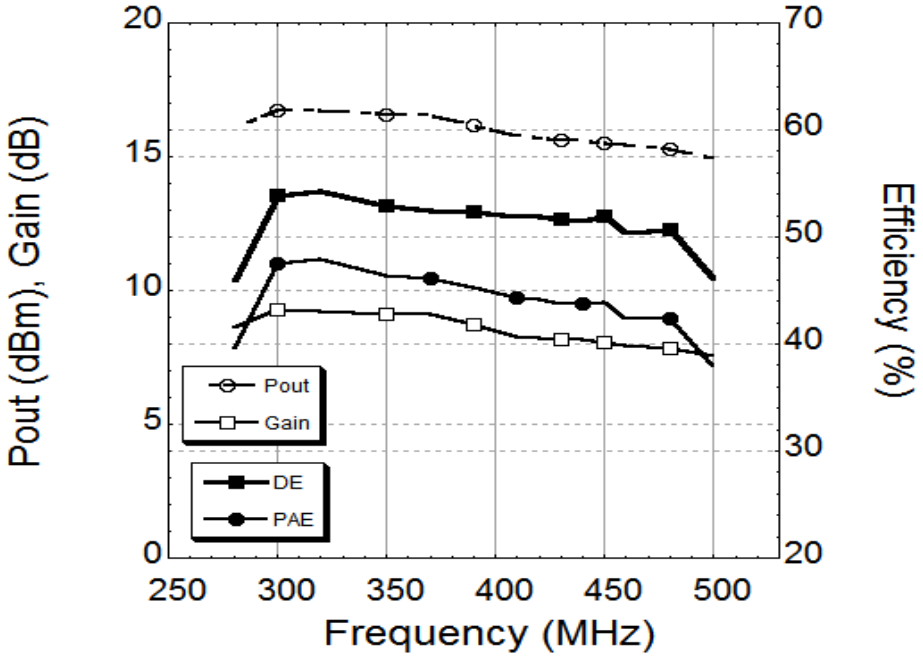


Figure 52. Class AB RF PA measurement results; PAE, DE, P_{out} and gain versus frequency.

3.2. Cascoded MOSFET-MESFET RF Power Amplifier

The previous sub section measurement results demonstrate that SOI-MESFETs can be used in power amplifier modules to relax matching network

requirements of a high power PA. RF measurements of MESFETs with V_{BD} of 28/20 V showed a good performance up to 2.5GHz. The frequency response of MESFET PAs can be further improved by using a cascode MOSFET-MESFET pair shown in Figure 53. The following explains how this technique improves the frequency response of MESFET PAs.

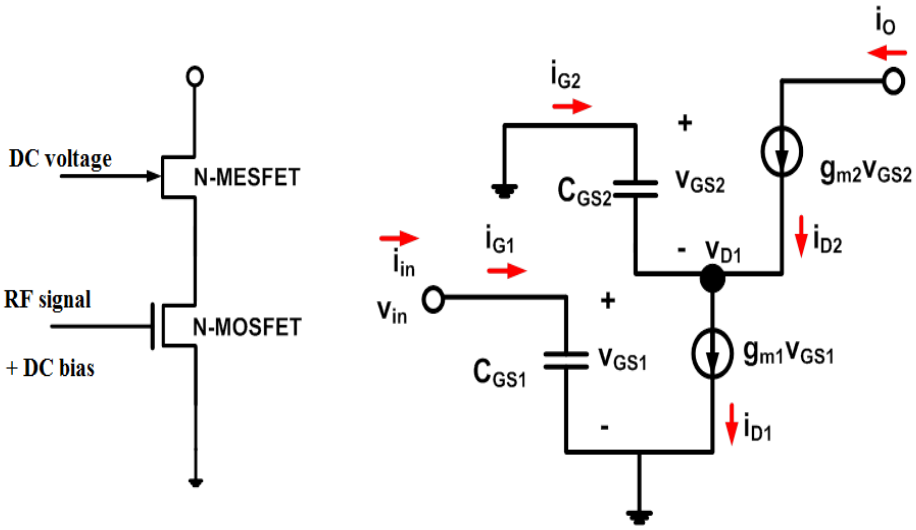


Figure 53. The proposed cascoded MOSFET-MESFET pair.

The breakdown voltage of the proposed structure is the summation of two devices breakdown voltages. The RF signal is fed to the MOSFET gate, which has few times higher cut-off frequency than MESFETs on a same process. Since the MOSFET converts the RF signal into current, the whole cascode pair has higher f_T than the MESFET's cut-off frequency. The small signal analysis of cascode pair shows that the overall f_T is approximately the geometric mean of the two devices f_T. Following are the small signal f_T analysis of the cascode structure shown in Figure 53:

$i_{in} = i_{G1} = jv_{in}\omega C_{GS1} \rightarrow v_{in} = -j\frac{i_{in}}{\omega C_{GS1}}$ and $i_{G2} = -jv_{D1}\omega C_{GS2}$ Equation 22

$i_{D1} = g_{m1}v_{in} \rightarrow i_{D1} = -j\frac{g_{m1}i_{in}}{\omega C_{GS1}}$ and $i_O = i_{D2} = -g_{m2}v_{D1}$

$\rightarrow i_{G2} = j\frac{\omega C_{GS2}i_O}{g_{m2}}$ Equation 23

KCL at drain1 node:

$i_{D1} = i_{G2} + i_O = i_O \times (1 + j\frac{\omega C_{GS2}}{g_{m2}})$ and

$$-j\frac{g_{m1}i_{in}}{\omega C_{GS1}} = i_O \times \left(1 + j\frac{\omega C_{GS2}}{g_{m2}}\right)$$ Equation 24

$$\frac{i_O}{i_{in}} = -j\frac{g_{m1}}{\omega C_{GS1}}\frac{1}{\left(1 + j\frac{\omega C_{GS2}}{g_{m2}}\right)} = -j\frac{\omega_{T1}}{\omega}\frac{1}{\left(1 + j\frac{\omega}{\omega_{T2}}\right)}$$ Equation 25

To find f_T

$|H_{21}| = |\frac{i_O}{i_{in}}(\omega = \omega_T)| = 1$, so $\omega_T = ?, \frac{\omega_{T1}^2}{\omega_T^2} = 1 + \frac{\omega_T^2}{\omega_{T2}^2}$ Equation 26

Solving the above equation:

$$\omega_T = \frac{\omega_{T2}}{\sqrt{2}} \times \sqrt{(\sqrt{1 + 4(\frac{\omega_{T1}}{\omega_{T2}})^2} - 1)} \approx \sqrt{(\omega_{T2} \times \omega_{T1})}$$ Equation 27

Equation 27 shows that cascode architecture improves the frequency performance of MESFET PAs.

Comparing cascoded MOSFET-MESFET and MOSFET-MOSFET, the first structure has much higher breakdown voltage while the RF performance is comparable with the later design for frequencies less than 10GHz. Figure 54 compares the conventional NMOS-NMOS cascode with the MOSFET-MESFET

cascode topology. The transconductance (g_m) of a cascode block is mostly determined by the input device; therefore in Figure 54.b, the MOSFET is used as the input transistor since it has higher gain and f_T.

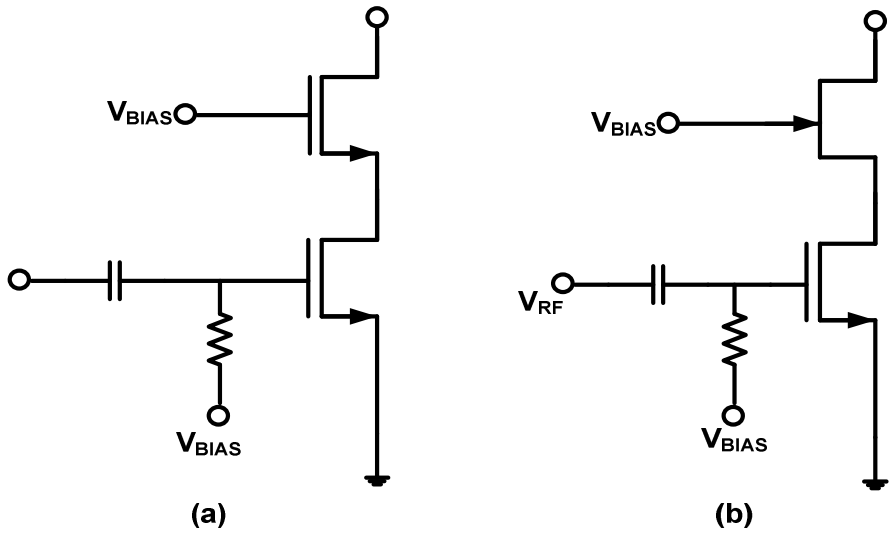


Figure 54 (a) conventional NMOS-NMOS cascode structure (b) proposed MOSFET-MESFET power amplifier

In Figure 54.a, a steady-state drain-to-source voltage of each transistor should not exceed the nominal 3V supply voltage given by the 150nm SOI CMOS technology. Therefore as a result of the cascode, the supply voltage can be theoretically increased by a factor of two. In practice however, the V_{DD} scaling will be less than two because the RF signal division ratio between the top and bottom transistors is not 1:1 with the top transistor receiving a larger share of the voltage swing. This implies that higher V_{DD} and consequently a higher output power level for the PA can be achieved if the top transistor has higher breakdown voltage. While the MESFET does have a noticeably lower f_T and g_m compared to the MOSFET, the overall performance of the PA's frequency operation and gain

should only marginally degrade since the performance of those metrics is dominated by the bottom transistor. On the 150nm SOI CMOS process the maximum voltage swing for the circuit in Figure 54.a is ~5V. Replacing the MOSFET with the MESFET in Figure 54.b, it can be increased to 8 to 12 V depending on MESFET's geometry. A cascoded MOS-MES structure was implemented in Agilent ADS as shown in Figure 54. b. The MESFET's gate length was chosen to be 300nm which allowed a 6V signal swing on the common gate transistor. In our simulations, a MOSFET with L_G=180nm transistor is used as the bottom MOSFET, it has slightly higher breakdown voltage comparing to SOI-MOSFET with gate length of 150nm [43].

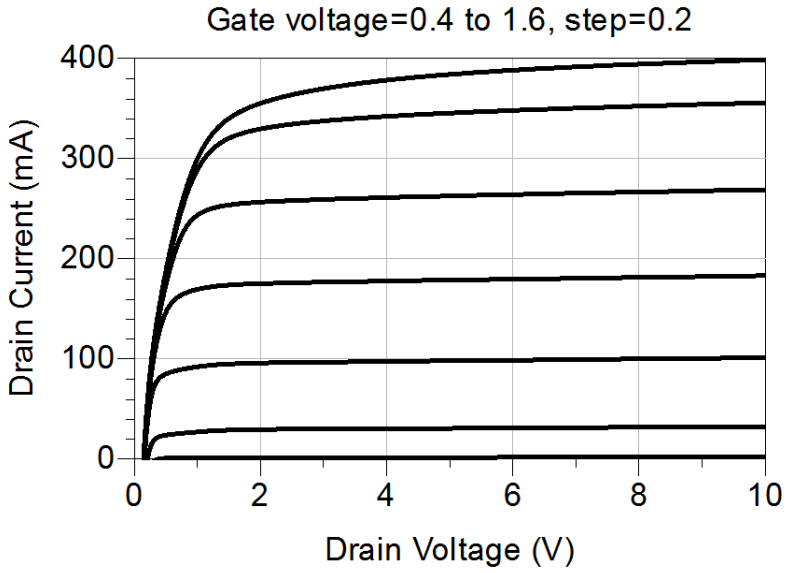


Figure 55. Cascoded MOSFET-MESFET's Family Of Curves (FOC).

Load/Source Pull simulations were performed and device widths in this simulation were chosen to deliver 24dBm power to a 50 ohms load. As the first step the family of curves for the cascoded device is plotted in Figure 55 to find

optimum biasing point. As it is shown in this plot, the drain voltage can go up to 10V without even seeing the soft breakdown effect. A high efficiency RF amplifier at 1GHz was targeted and simulation results showed a maximum PAE of 75% with around 28dB power gain. Time domain voltage and current at the top transistor drain is shown in Figure 56. Maximum voltage swing on the common gate transistor is less than 6V, which guarantees safe operation of the MESFET device. Gain, output power and PAE are plotted as a function of input power in Figure 57 [43].

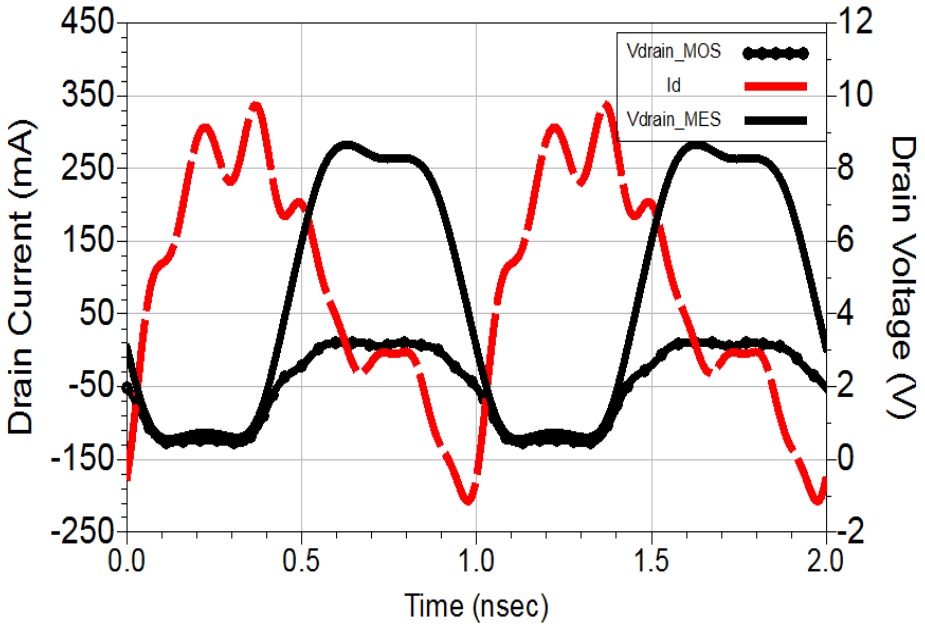


Figure 56. Time domain drain's current and voltage

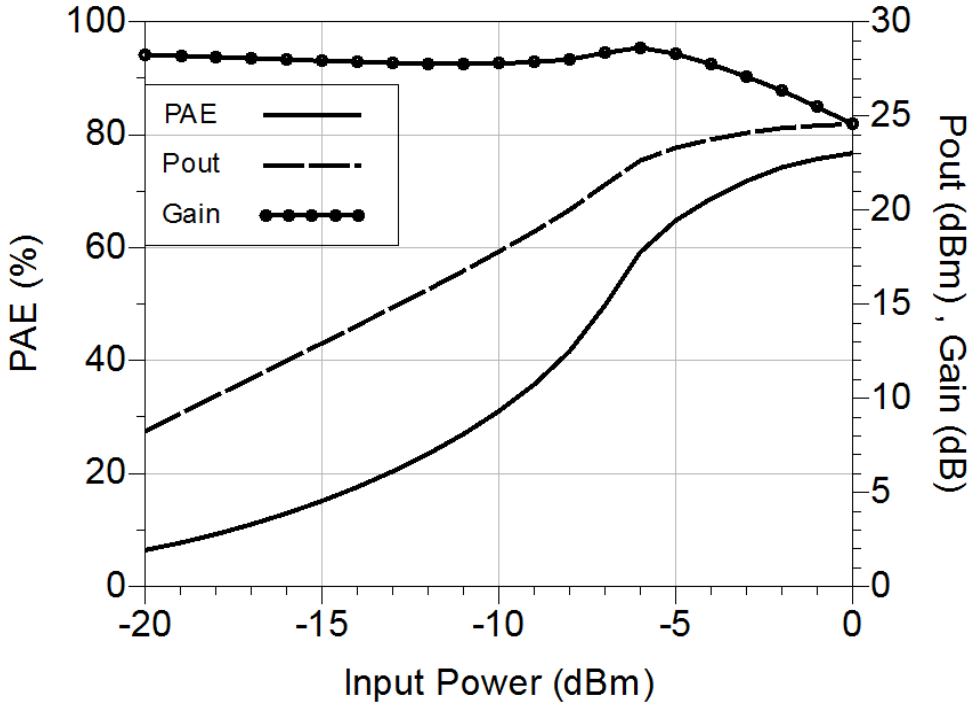


Figure 57. Pout, Gain and PAE versus Input power.

3.3. On-Die Measurements of MESFET RF-PAs

Various MESFETs breakdown voltages were measured and are plotted versus L_{aD} in Figure 58. These devices were fabricated on a 45nm SOI-CMOS process that has a nominal supply voltage of 0.9V. The peak output power of a class-A amplifier can be calculated using Equation 5 in the first chapter. The theoretical peak output powers of different MESFETs are calculated from the breakdown voltage plot of Figure 58. The theoretical maximum P_{OUT} versus drain access length (L_{aD}) for two different drain terminations of 5 Ω and 50 Ω are shown in Figure 59. Figure 59.a shows that peak output power of ~20 Watt can be achieved if a MESFET with L_{aD} = 2µm and loadline of 5 Ω is used. This is much higher than what most cellphone applications require.

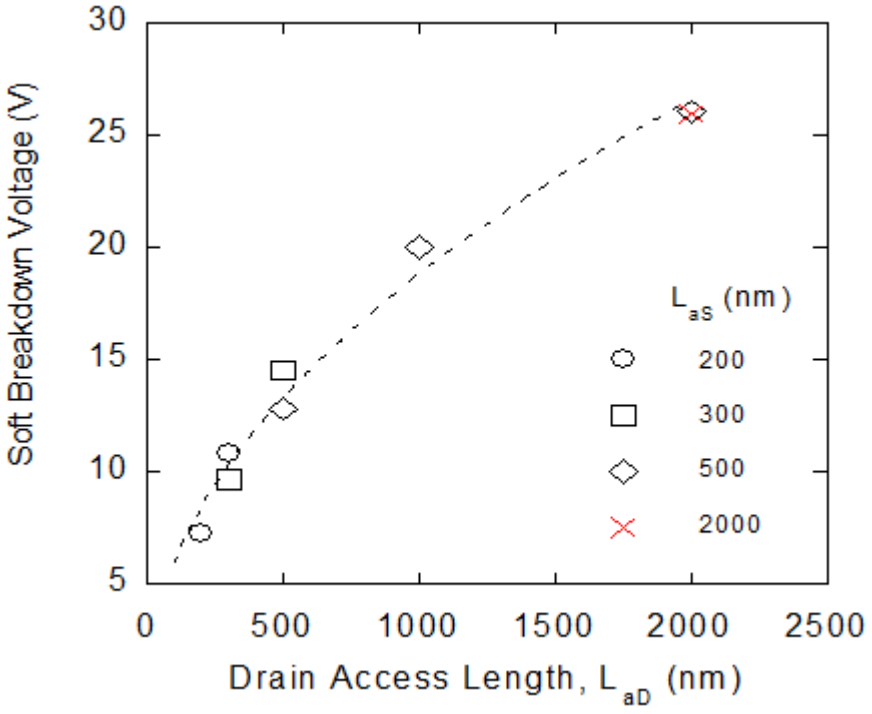


Figure 58. MESFETs breakdown voltage versus L_{aD} on a 45nm SOI-CMOS process.

Figure 59.b shows peak output powers for MESFETs with a 50 Ω loadline. The output power range is between 22dBm to 33dBm. This range of power covers many of the applications such as GSM [44] and EDGE [45]. As mentioned in the first chapter, using a 50 Ω loadline transistor can possibly result in a higher efficiency and wider bandwidth of the RF power amplifier. The term " transformer-less " will be used, in the rest of this thesis, for single ended class A/AB RF-PAs designed with 50 Ω loadline SOI-MESFETs.

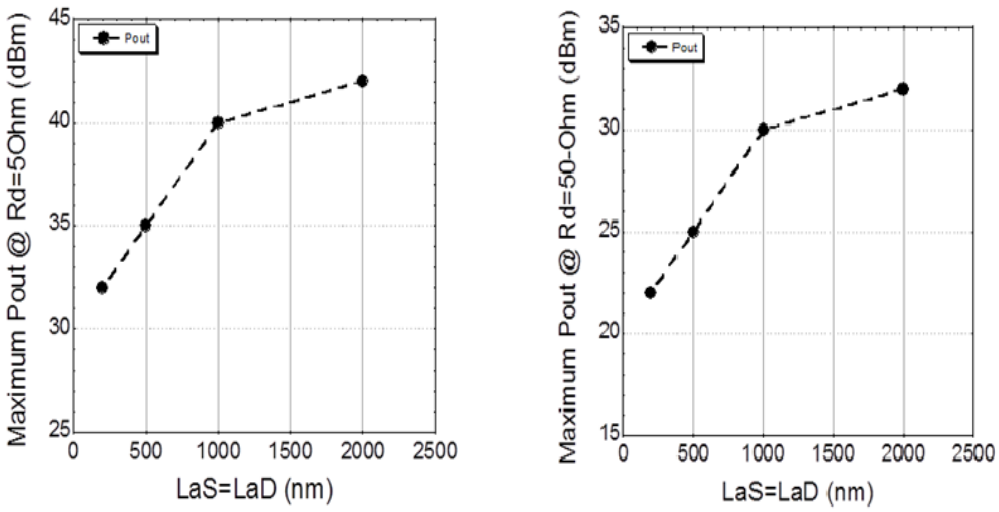


Figure 59. Theoretical peak output power of class-A amplifier versus L_{aD} (a) device loadline of 5 Ω (b) device loadline slope of 50 Ω.

MESFETs breakdown voltage can be controlled by appropriate sizing of spacer regions between drain, source and gate. Therefore, a transformer-less RF-PA can be designed for any application with the maximum output power in the range of 0.3-2 Watt. The design steps toward transformer-less MESFET PAs are explained here.

The minimum required breakdown voltage for a given peak output power is calculated in Equation 28.

$$P_{OUT} \approx \frac{\left(\frac{VBD}{2}\right)^2}{2 \times ROPT} \xrightarrow{ROPT=50 \text{ and given } POUT} V_{BD} \cong 2\sqrt{2 \times 50 \times P_{OUT}} \qquad \text{Equation 28}$$

The optimum L_{aS} and L_{aD} can be extracted from Figure 58 to achieve the above breakdown voltage. Also, the device width should be correctly set to ensure

a 50 Ω loadline. Using Equation 29 and knowing the MESFET's current drive, device width can be calculated.

$$I_{MAX} = \frac{V_{BD} - V_{KNEE}}{50} \xrightarrow[current\ drive]{} MESFET\ width \qquad \text{Equation 29}$$

The explained methodology was used to design RF power amplifiers using the SOI-MESFET. The idea of transformer-less MESFET PA was initially explored by using the setup shown in Figure 60. The shown test system is similar to the load/source pull system described at the beginning of this chapter. The main difference is that here the load and source impedances are constant at all frequencies, while in the load-pull approach; a load tuner is used to search for the optimal performance. As a result, the reported efficiencies in this work are not the highest achievable performances that can be obtained by SOI-MESFETs.

On-die open, short and thru structures in a Ground-Signal-Ground (GSG) format were used to calibrate out all the losses associated with filters, bias-T, cables and pad loss.

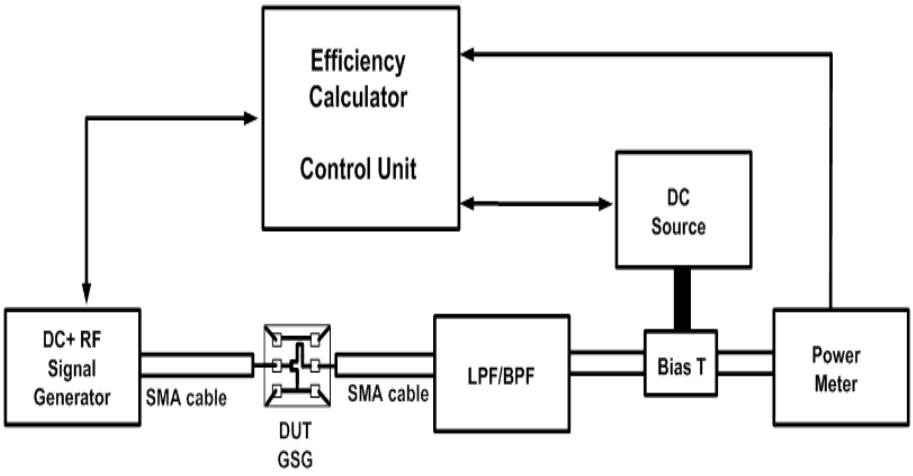


Figure 60. On-Die MESFET RF-PA measurement setup.

A low pass filter used in this work pushes the location of harmonic impedances to the edge of the smith chart. Therefore the impedance seen from the drain of MESFET is close to open at the second and third harmonics. The locations of load impedances on the smith chart are shown in Figure 61. A parallel L-C resonator is required to filter out harmonics in the traditional class A/AB amplifiers. In this work we have used a low-pass filter that represents a series L-C resonator. This technique is known as low-pass class E amplifier [MS]. Although it is not a switching amplifier, it still improves the efficiency, by influencing the time domain drain voltage and current waveforms. The drawback of this approach is the higher nonlinearity comparing to the traditional class-A RF-PAs.

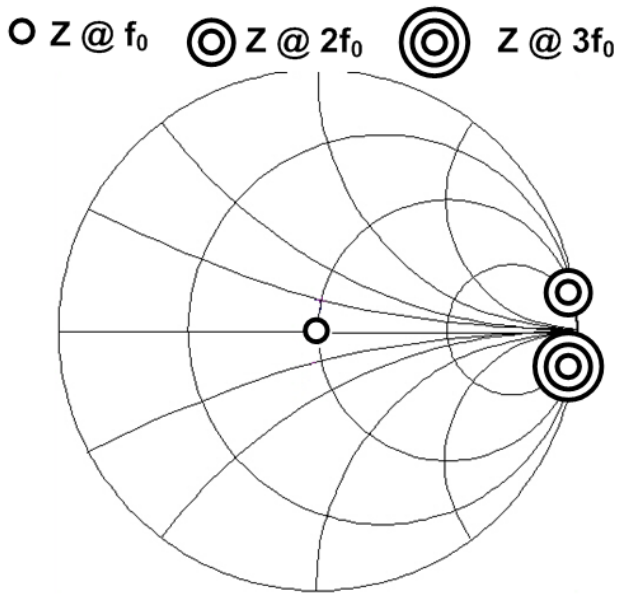


Figure 61. The presented load to the MESFET's drain at fundamental and harmonic frequencies.

MESFETs fabricated on a 45nm process were tested in this setup. MESFETs with L_G=200nm and L_{aS}=L_{aD}=500nm have breakdown voltage of ~12-13. The device used in this work has a loadline of ~80 Ω, thus it can deliver 22 dBm of power to a 50 Ω load. Measurement results at 400 MHz show peak output power of 22.5 dBm and 50 % power added efficiency. Efficiency and output power versus input power for a class-A bias condition at two different supply voltages are shown in Figure 62.

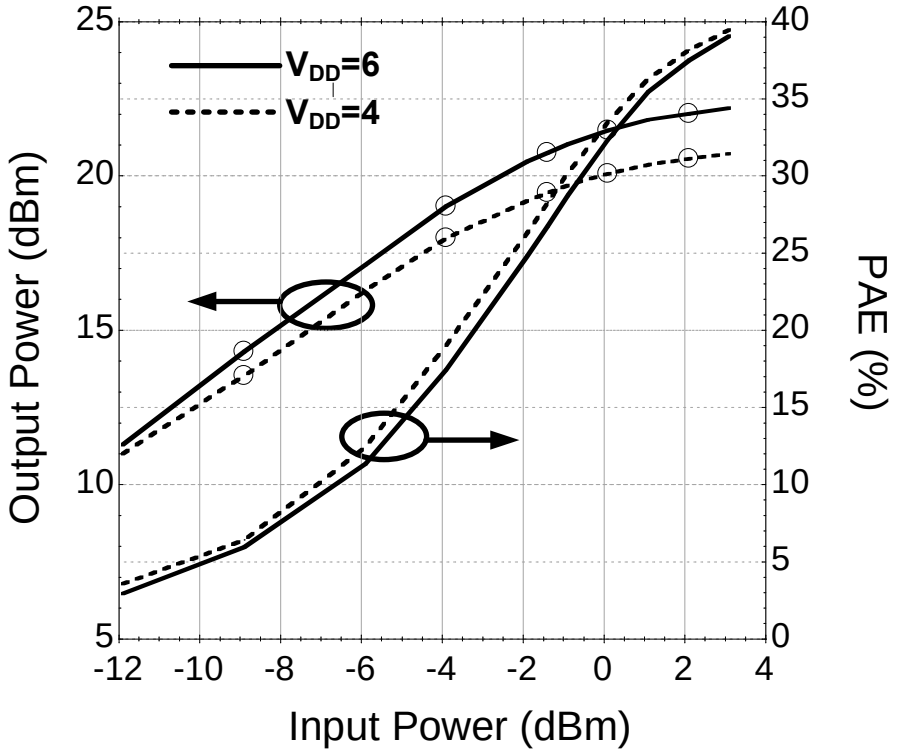


Figure 62. PAE, Pout vs Pin. Class-A 400 MHz MESFET-PA with L_G=200nm, L_{aS}=L_{aD}=500nm. V_G=0.0V

PA class of operation was changed by sweeping gate bias voltage. Figure 63 shows MESFET PA performance versus gate voltage. As the plot shows the

output power goes down for lower gate voltages (class-C), but efficiency increases to 52 %.

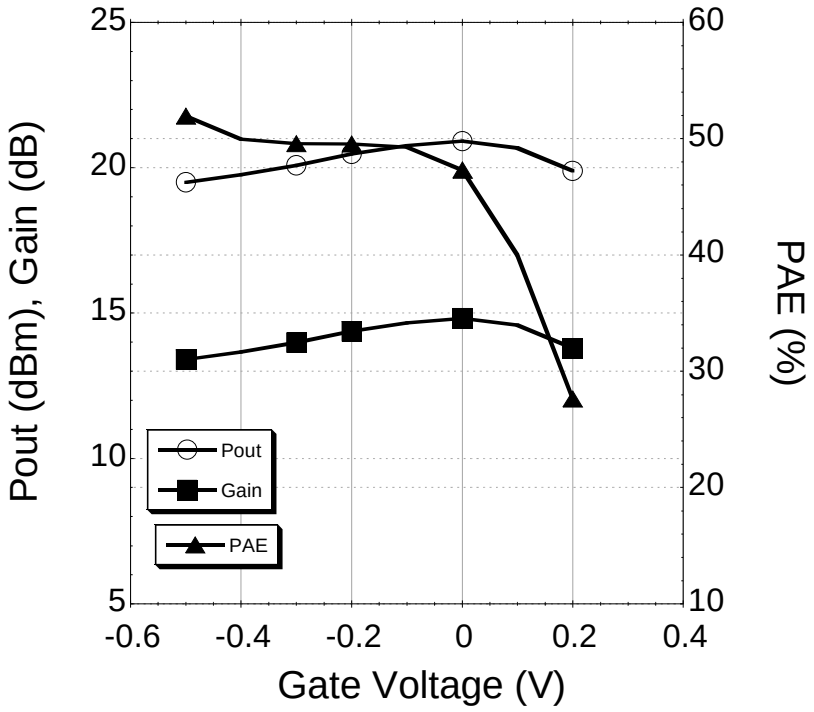


Figure 63. 400 MHz MESFET-PA performance at different classes of operation. V_{DD}=4 V, V_{SUB}=4V, Pin 6 dBm.

The next chapter discusses polar transmitters as a solution to efficiency degradation at backed-off powers. In detail operation of polar transmitters will be discussed in Chapter IV. One of the key parameters in designing these type of transmitters is RF-PA performance versus supply voltage. MESFET RF-PA PAE, gain and output power versus supply voltage were measured and plotted in Figure 64. As it is shown the peak output power increases with increasing the supply voltage. Accordingly, the 1-dB compression point increases and results in a better linearity.

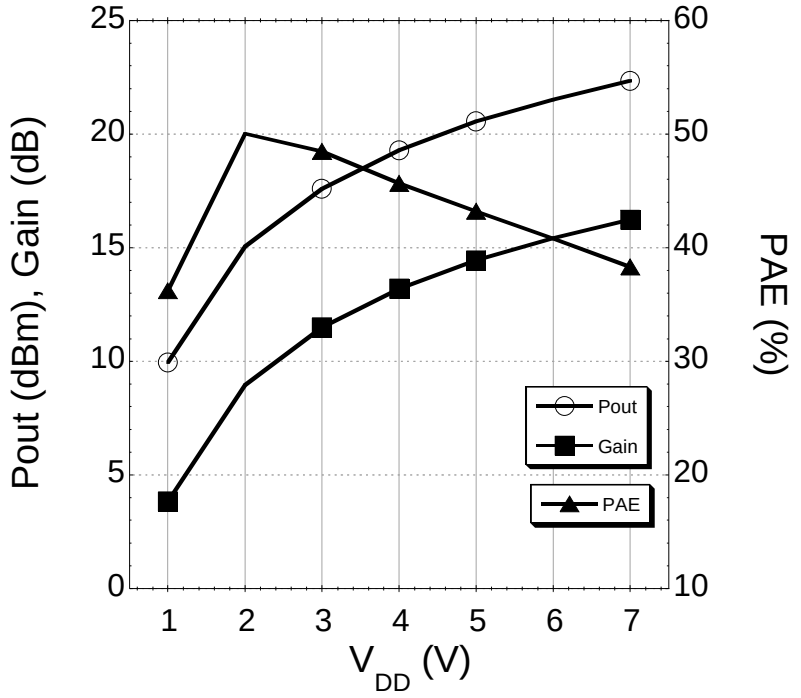


Figure 64. MESFTE RF-PA performance versus supply voltage. V_G=-0.4 V, V_{SUB}=4V, Pin=6dBm.

Similar measurements were taken for a MESFET with $L_G=L_{aS}=L_{aD}$=200nm fabricated on a 45nm Technology. Three RF power amplifiers operating at 433, 900 and 1800 MHz were measured. The peak output power of 21 dBm was measured at 433 MHz. The peak measured power added efficiency is close to 55% and MESFET PA has 15 dB of gain at 433MHz. The measured PA performances at different frequencies are shown in Table 1.

Table 1. Measurement results of transformer-less MESFET RF-PAs (MESFET has L_G=200 and L_{aS}=L_{aD}= 200nm and 500nm with Width=4mm).

Frequency (MHz)	L_G, L_{aS}, L_{aD} (μm)	V_{DD} (V)	V_G (V)	PAE (%)	P_{OUT} (dBm)	Gain(dB)
433	0.2-0.2-0.2	2	0.1	55	18.4	15
433	0.2-0.5-0.5	6	0.0	48	21.2	20
900	0.2-0.2-0.2	3	0.1	42	19	9.5
1800	0.2-0.5-0.5	3	-0.2	48	21	11
1800	0.2-0.5-0.5	7	0.0	35	24	14

3.4. Summary of SOI-MESFET RF Power Amplifiers

The first demonstration of SOI-MESFET RF power amplifiers were presented in this chapter. SOI-MESFETs on 45nm process provides enough RF gain for power amplifier applications below 2.5 GHz. The RF gain can be further increased by using a MOSFET device as the input transistor and MESFET as the cascode device. A 1 GHz RF-PA using the proposed cascode structure was designed and simulated in ADS. Simulation results show ~75 % PAE and 24dBm output power.

MESFET only RF-PAs were designed and measured at 433, 900 and 1800 MHz. Peak PAE of 55% and output power of 22.5 dBm were measured.

The following chapter discusses RF polar transmitter design using the fabricated MESFET PA at 433 MHz.

CHAPTER 4

WIDEBAND SUPPLY MODULATOR FOR POLAR TRANSMITTERS

The rapid evolution of wireless communication technologies has increased the need for handheld devices that can support high data rate communication standards. Radio Frequency (RF) front ends, especially the RF power amplifier, are the main challenges in implementation of these systems due to aggressive linearity and dynamic range requirements. Power Amplifiers (PAs) dominate the sources of distortions and power consumption in the RF-front end. They are typically operated in linear classes in order to minimize the linearity degradation. However, linear operation leads to poor average power efficiency, especially when fed by signals with high peak to average power ratio (PAPR) such as Long Term Evolution (LTE) [47] and Wideband Code Division Multiple Access (W-CDMA) signals [48]. Table 2 shows PAPR, bandwidth and power specifications of few high data rate standards [46].

Table 2. Advanced modulation schemes specifications [46].

Standards	Modulation Scheme	PAPR (dB)	Channel Bandwidth
IEEE 802.11b (WLAN)	DBPSK, DQPSK, CCK	~10	20 MHz
GSM EDGE	8-PSK	~3.2	200 KHz
WCDMA/UMTS	QPSK	~3.5-7	5 MHz
CDMA 2000	QPSK, BPSK, 8-PSK, 16QAM	~4-9	1.25 MHz

An example of MESFET class-AB RF power amplifier efficiency versus output power is shown in Figure 65. W-CDMA signal average power is 5-6 dB

below the peak power. Therefore if the PA is fed by this signal, the average efficiency drops to 10% comparing to the maximum power added efficiency of 55%. Reduced efficiency in the power amplifier is the main contributor to the significant the battery life reduction of handset devices. Low efficiency also causes high power dissipation in the device and results in severe heating effects.

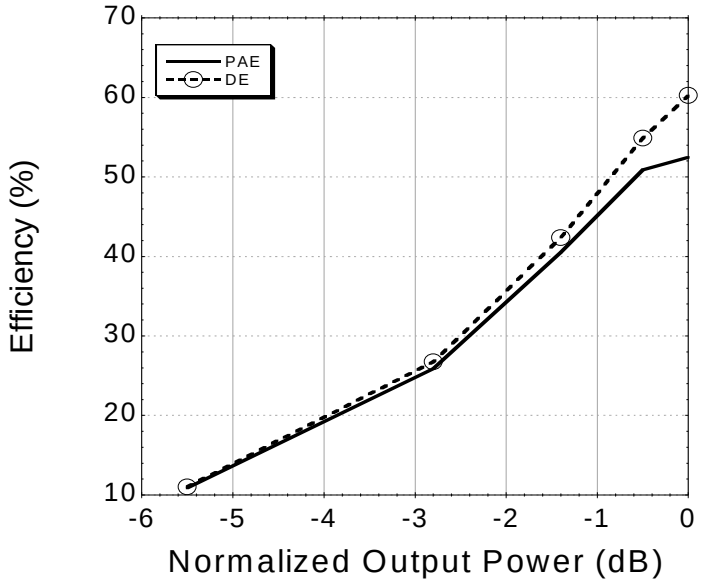


Figure 65. MESFET Class-AB amplifier efficiency versus normalized output power.

To remedy this issue, some advanced methods like Doherty amplifier and drain modulation based architectures were introduced [49], [50], [51]. Although the Doherty technique improves efficiency at backed off power, it has bandwidth limitations. Polar modulation on the other hand, can potentially have larger bandwidth and achieve close to peak PA efficiency operation over a range of input powers by tracking the envelope variation of the modulated signal at the PA supply node [28].

The main idea behind the polar architecture is to improve the drain efficiency by reducing the DC power with respect to the output power. Transient drain voltage of a class-A amplifier at different power levels are plotted in Figure 66. (a) and (b) have the same DC power consumption, while (a) has higher output power than (b), therefore it has higher drain efficiency than (b). An envelope amplifier is added to the class-A circuit of Figure 67. The envelope amplifier controls the supply voltage, V_{DD}, based on the peak-to-peak voltage swing at the drain of the PA's transistor. As a result, the DC power consumption is adaptively being changed to achieve higher efficiency at lower output powers.

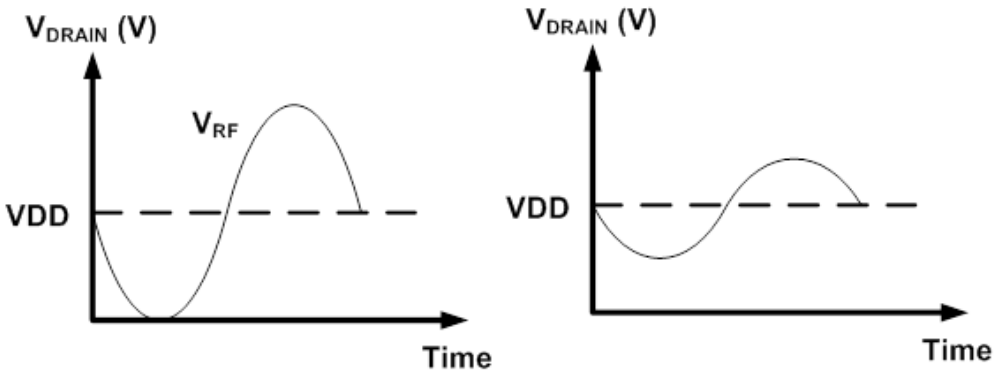


Figure 66. Class-A transient drain voltage.

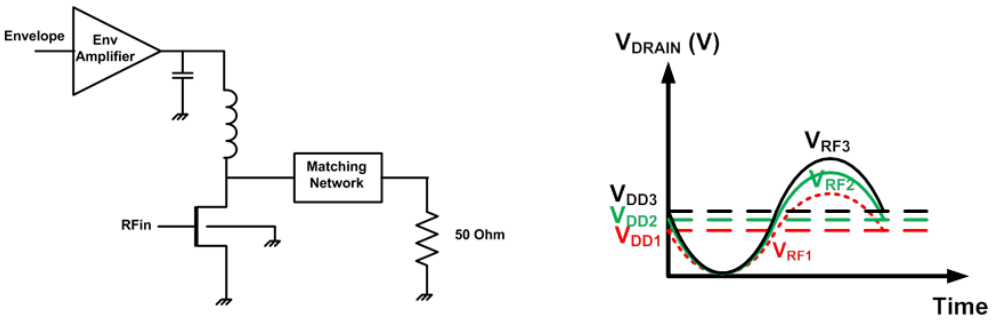


Figure 67. Efficiency improvement by reducing the DC bias point.

The idea of polar transmitter was first introduced in [52]. Figure 68 shows the proposed circuit by Kahn in [52] known as Envelope Elimination and Restoration (EER).

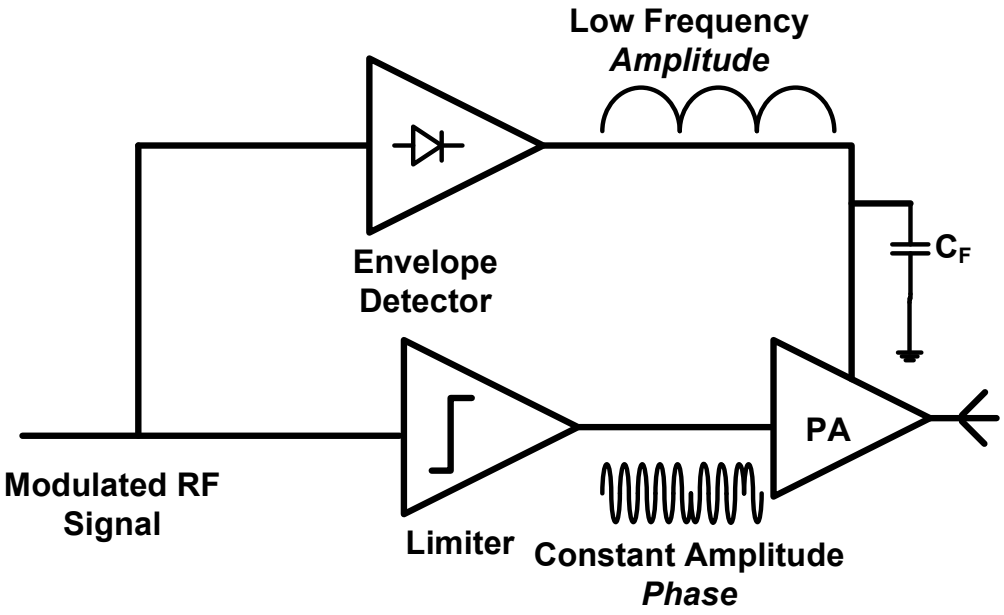


Figure 68. Kahn Envelope Elimination and Restoration (EER) Transmitter [52]

Contrary to traditional Cartesian transmitters, polar transmitters transform the in-phase and quadrature components of the input signal into amplitude (r) and phase (θ) representation.

$$r(t) = \sqrt{I(t)^2 + Q(t)^2}\ ,\ \theta(t) = tan^{-1}(\frac{I(t)}{Q(t)}) \qquad \text{Equation 30}$$

In an EER transmitter, the amplitude information is used to control the drain supply voltage and consequently the gain. The modulated phase signal is a constant amplitude signal which ensures the peak efficiency operation of the RF-PA. Since the input signal has a constant amplitude, one of the main attributes of the EER technique is to make possible the deployment of high efficiency PAs,

which are strongly nonlinear, while meeting the linearity requirements. The overall efficiency of the whole output stage is the PA efficiency multiplied by the Envelope path efficiency. Therefore, the peak efficiency reduces, but the average efficiency is improved at back off powers.

As mentioned above, a nonlinear PA can be used in EER architecture which improves the transmitter's efficiency. But this technique has two main drawbacks: (i) phase information has much more bandwidth than the original I/Q signals (ii) high input power leaks to the output and limits the dynamic range of the transmitter. To eliminate the bandwidth and dynamic range problem of EER techniques, an alternative form of polar transmitter known as Envelope Tracking (ET) has been introduced [53], [54]. In ET architecture, the PA input terminal is fed by the original modulated signal which has less BW while the supply is controlled by amplitude modulated signal. This increases the PA dynamic range and improves the backed-off power efficiency at the same time. Since the input signal has amplitude variation, a linear RF power amplifier has to be used in ET architecture. The RF PA of these architectures has to have good performance versus supply voltage variation, while the ET amplifier is linear, EER can be a nonlinear PA. Later sections discuss a new ET architecture using the proposed four terminal SOI-MESFETs.

As mentioned above, the polar transmitter needs phase (θ) and magnitude (r) information instead of Inphase (I) and Quadrature (Q) signals. I/Q to r/θ transformation are nonlinear functions, which affect signal BW. It increases the phase BW approximately by ~10-20 times and amplitude BW by ~5X comparing

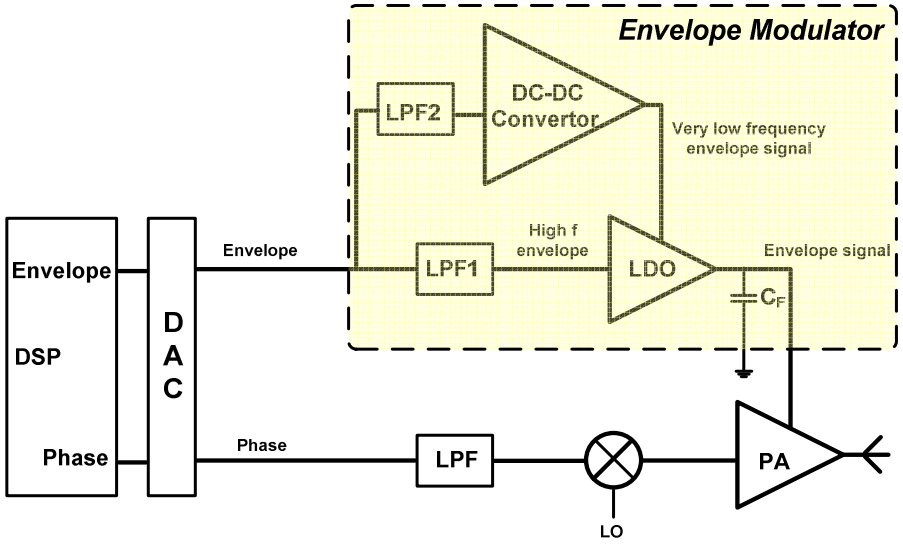
to the original I and Q signals. Therefore, the power amplifier and supply modulator must have wider bandwidth comparing to the traditional Cartesian transmitters. Previous chapters discussed how SOI-MESFETs can be used to design very wideband RF amplifiers. This chapter talks about wideband supply modulator design using the proposed SOI-MESFET device.

4.1. RF Power Amplifiers Supply Modulators

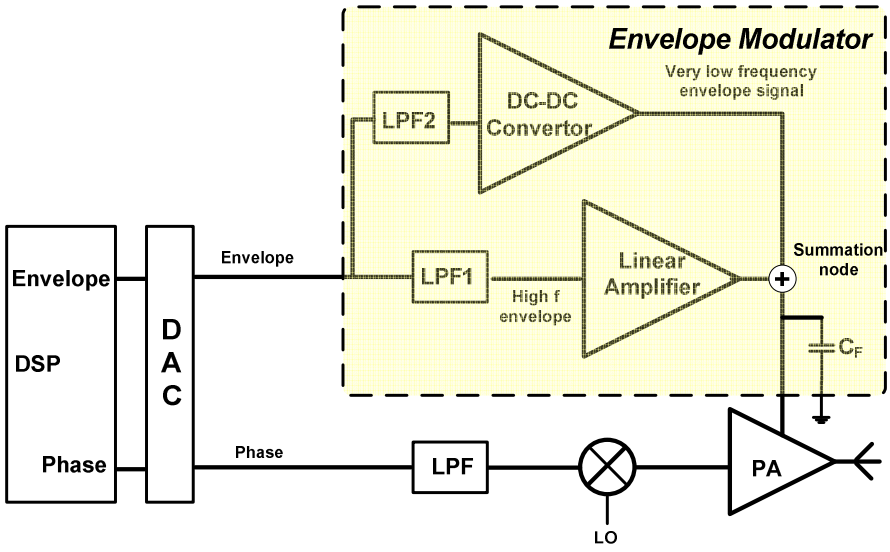
Analog amplifiers, buck convertors or mixed analog/digital circuitries are the candidates for the envelope path of polar transmitters. Buck convertors and switched mode amplifiers (SMAs) have traditionally being used to modulate the PA's supply node. Although switched mode circuits have high efficiency, they suffer from bandwidth and linearity limitations. They also generate high levels of switching noise ripple at the output terminal. SMAs are more applicable for low bandwidth (BW) signals like EDGE/GSM [55]. For large BW signals such as W-CDMA and LTE, a very fast analog amplifier is needed. Analog amplifiers can provide much more bandwidth than buck convertors, but result in low efficiency. More advanced architectures use the combination of a buck convertor for low frequencies and an analog amplifier for high frequencies [49], [55].

Various hybrid linear/SMA regulators were proposed to achieve high bandwidth and efficiency at the same time [49], [56]. In general, the linear amplifier can be in series or in parallel with the SMA. Figure 69 shows both groupings. The series combination of the switching and linear amplifiers helps remove switching noise. The drawback of this tactic is that an LDO is required to function as the linear amplifier [56]. CMOS LDOs suffer from bandwidth

limitations, stability issues and limited voltage swings [57]. The following section discusses how SOI- MESFETs can improve LDO stability and bandwidth.



(a)



(b)

Figure 69. (a) Series SMA LDO supply modulator in EER (b) Parallel Amplifier and SMA supply modulator in EER.

4.2. SOI-MESFET for PA Supply Regulation

Different LDO topologies based on P-channel or N-channel pass transistors have been introduced [57]. Both P- and N-channel LDOs are shown in Figure 70, where they each have their own advantage and disadvantages. Output impedance (Z_{OUT}) of the P-channel transistor in Figure 70.b is proportional to r_{ds} of the device. However Figure 70.a uses an N-MOSFET which has lower output impedance in an LDO circuit which gives higher bandwidth compared to P-channel LDOs or better stability. The drawback using N-channel LDOs is that a charge pump circuit is required to overcome the threshold voltage drop for enhancement mode N-channel devices [58].

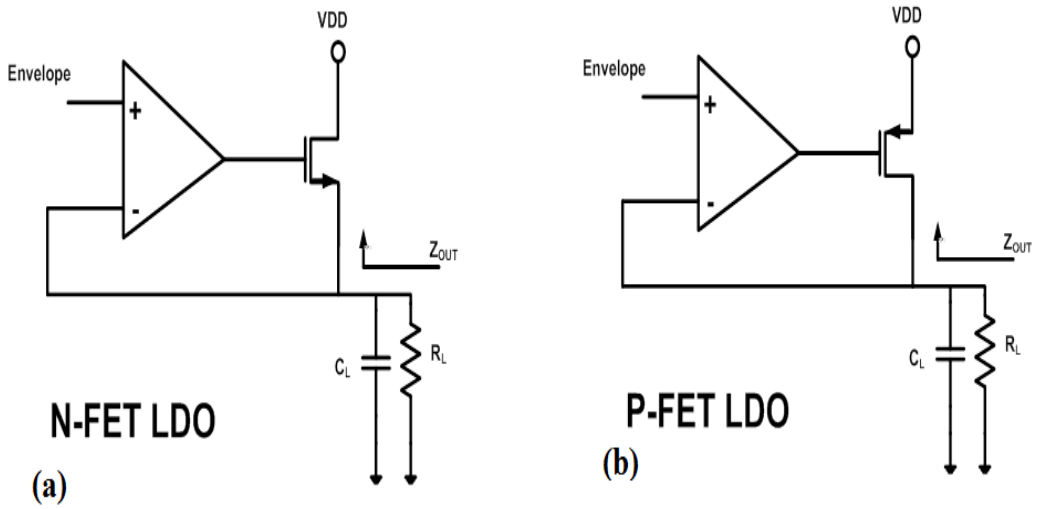


Figure 70. (a) N-MOSFET based LDO (b) P-MOSFET based LDO

In this section, we present a design methodology for a SOI-MESFET based LDO that features a depletion-mode N-type device as the pass transistor. This combines the advantages of both P and N devices allowing for low cost, design simplicity, stability, high current drive and bandwidth.

As discussed in the introduction, LDO regulators can be used to improve the overall efficiency and linearity of a RF transmitter. The proposed SOI-MESFET based LDO is shown Figure 71. An N-channel MESFET is used as the pass transistor of the LDO in a common drain configuration. The simplified equivalent small signal circuits of MESFET and PA are also shown in Figure 71. At low frequencies, the resistance seen by the LDO output node is proportional to $1/g_m$; this pushes the pole contributed by the pass transistor to higher frequencies compared to a P-FET device which has output resistance of R_{ds}. This stabilizes the LDO for larger capacitive loads.

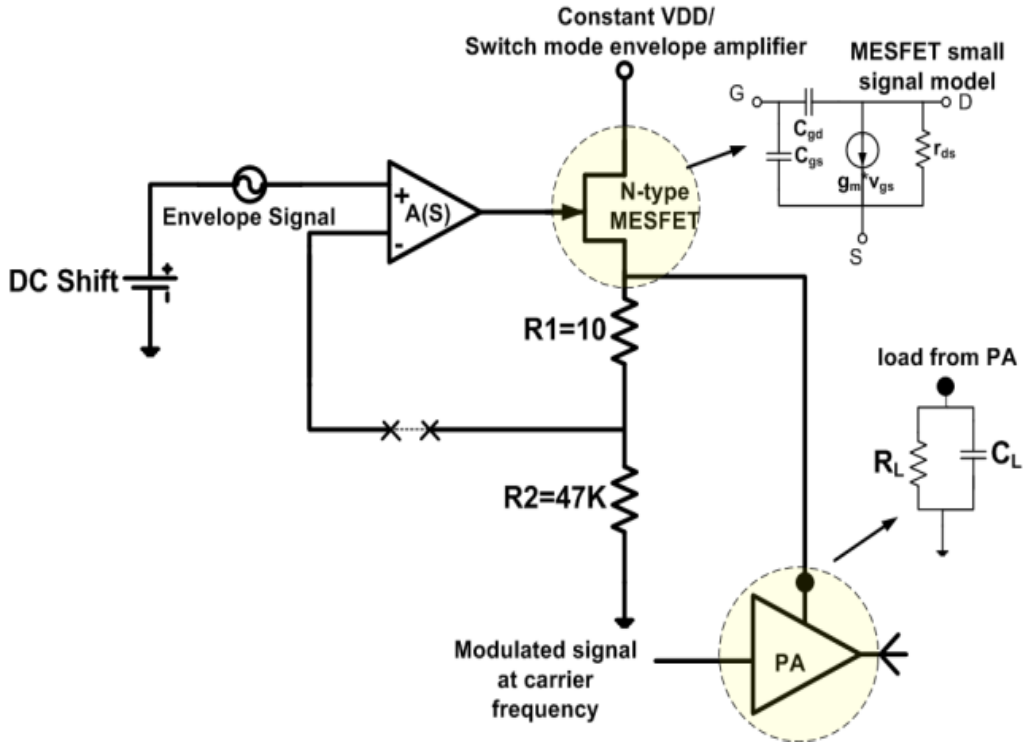


Figure 71. LDO envelope tracking regulator using the SOI-MESFET.

The loop gain transfer function of the LDO, *LG(S)*, depends on the op-amp transfer function, *A(S)*, and the common drain transistor frequency response, *M(S)*.

$$Loop\ Gain(S) = LG(S) = A(S) \times M(S) \qquad \text{Equation 31}$$

It can be shown that:

$$M(S) = \frac{g_m + C_{gs} \times S}{\frac{1}{Z_L} + \frac{1}{r_{ds}} + g_m + C_{gs} \times S} \approx \frac{g_m + C_{gs} \times S}{(\frac{1}{R_L} + g_m) + (C_{gs} + C_L) \times S} \qquad \text{Equation 32}$$

g_m is much larger than 1/RL, therefore the pole associated with M(S) is located at:

$$\omega_{PM} \approx \frac{g_m}{C_{gs} + C_L} \xrightarrow{C_L=0} \omega_{PM} = \omega_T \qquad \text{Equation 33}$$

For C_L=0, the transistor's dominant pole is located at the MESFET cut-off frequency, f_T. MESFETs used in this work have more than 10GHz cut-off frequency. The op-amp used in this work has a unity gain bandwidth of 350MHz. Its first pole is located at 35 kHz and the second pole at 500 MHz [59]. Since the pole related to the MESFET is at a much higher frequency than the op-amp's second pole, it has minimal effect on the LDO phase margin. Figure 72 shows the open loop frequency response of the LDO in the presence of low capacitive loads, less than 5pF. As it is shown in the measurements section, higher values of C_L push the MESFET pole to lower frequencies and cause instability. This issue can be resolved by using a slower op-amp with the cost of a reduced bandwidth.

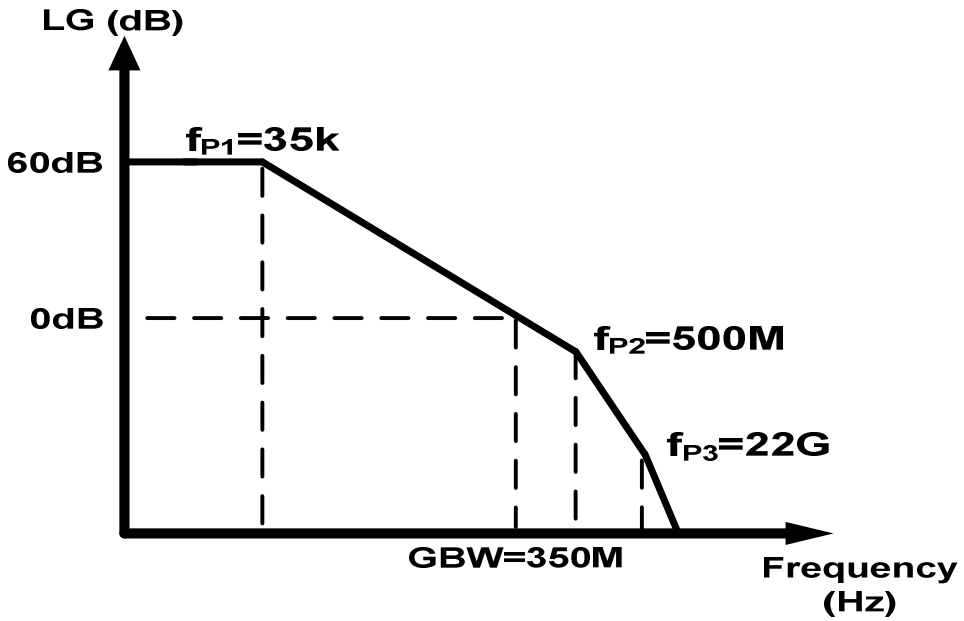


Figure 72. Frequency response of the proposed LDO.

4.3. LDO Measurement Results

An N-channel MESFET LDO for polar and envelope tracking transmitter applications is designed and built using a packaged MESFET fabricated on a 150nm SOI-CMOS process. A 350MHz bandwidth AD8061 op-amp from Analog Devices [59] was used to drive the MESFET gate. As explained in the previous section, the overall LDO bandwidth is limited mostly by the op-amp unity gain frequency. The LDO transfer function, under different load conditions has been measured and plotted in Figure 73. This plot demonstrates that a bandwidth of up to 350MHz can be achieved.

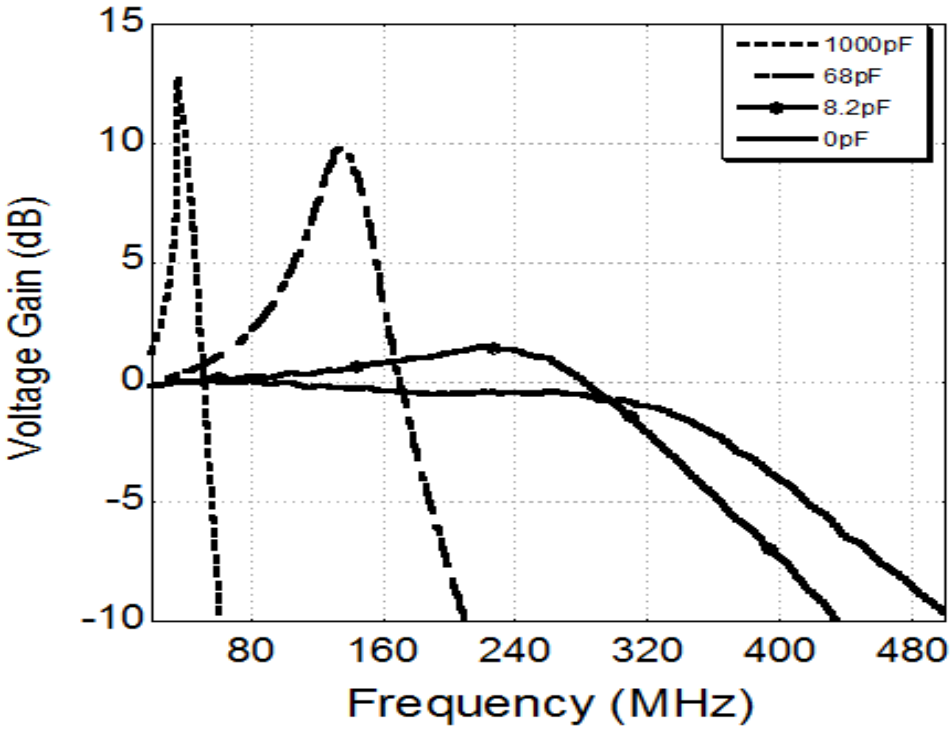


Figure 73. Measured LDO voltage gain for different capacitive loads.

The efficiency of a supply regulator directly affects the overall polar transmitter performance. Assuming the LDO voltage supply remains constant, the efficiency will drop as the output power decreases as explained in Equation 34 .

$$LDO_{Eff}(\%) = \frac{V_{OUT} \times I_{Load}}{V_{DD} \times I_{DC}} \times 100 \cong 100 \times \frac{V_{OUT}}{V_{DD}} \qquad \text{Equation 34}$$

To prevent this issue, a buck regulator can be used in series with the LDO to control the supply voltage, V_{DD}, and amplify the low frequency components of a modulated signal. The LDO efficiency with (PAE) and without (DE) the presence of an error amplifier is shown in Figure 74. Measured peak output power and efficiency are 26.2 dBm and 77% respectively when the LDO is connected to a 20Ω resistor and a 10pF capacitor.

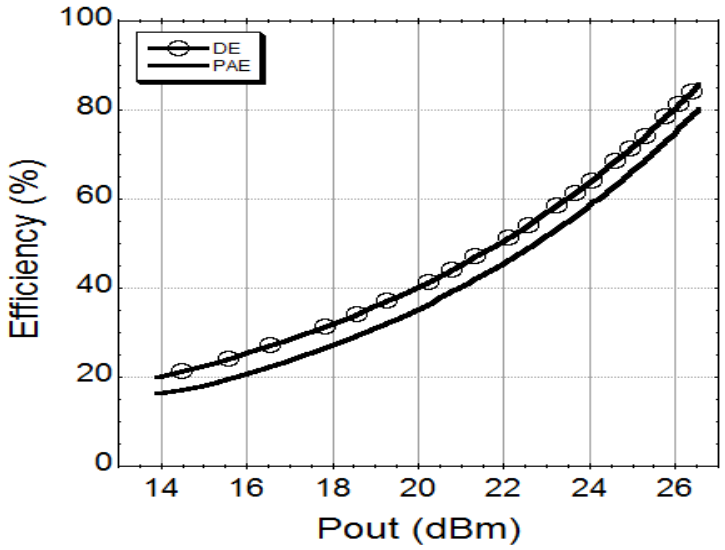


Figure 74. Measured LDO efficiency

The LDO linearity was tested by driving it with a two tone sinusoidal signal at 100MHz separated by 200 kHz. The output spectrum is shown in Figure 75. Measured IMD3 is approximately -55dBc when the input power is at -20dBc with respect to the full voltage swing.

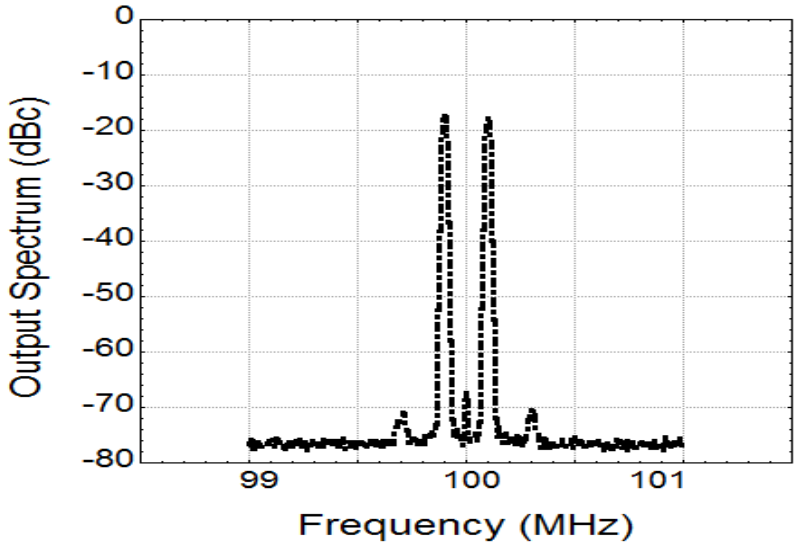


Figure 75. LDO output spectrum when it is fed with a two tone signal at 100MHz and separated by 200kHz.

Figure 76 shows the transient response of the LDO with input rectified sinusoidal. Fast slope changes at the signal edges show the broadband behavior of the LDO.

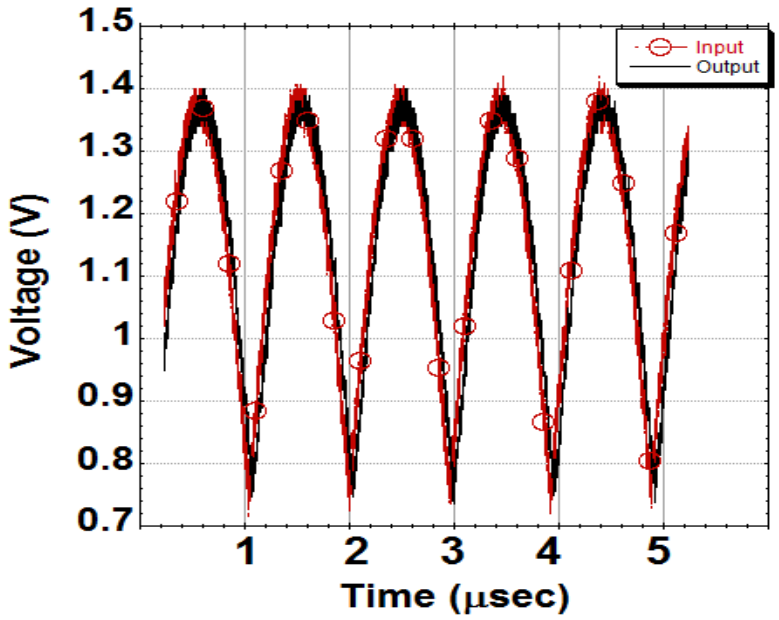


Figure 76. Transient response of the LDO to a rectified 1.2MHz sine wave applied as the envelope signal.

One of the advantages of using an LDO as the linear amplifier is to suppress the switching noise coming from the switch mode power supply. Figure 77 shows power supply noise rejection behavior of the proposed LDO. More than 50dB noise rejection has been achieved for frequencies below 300MHz.

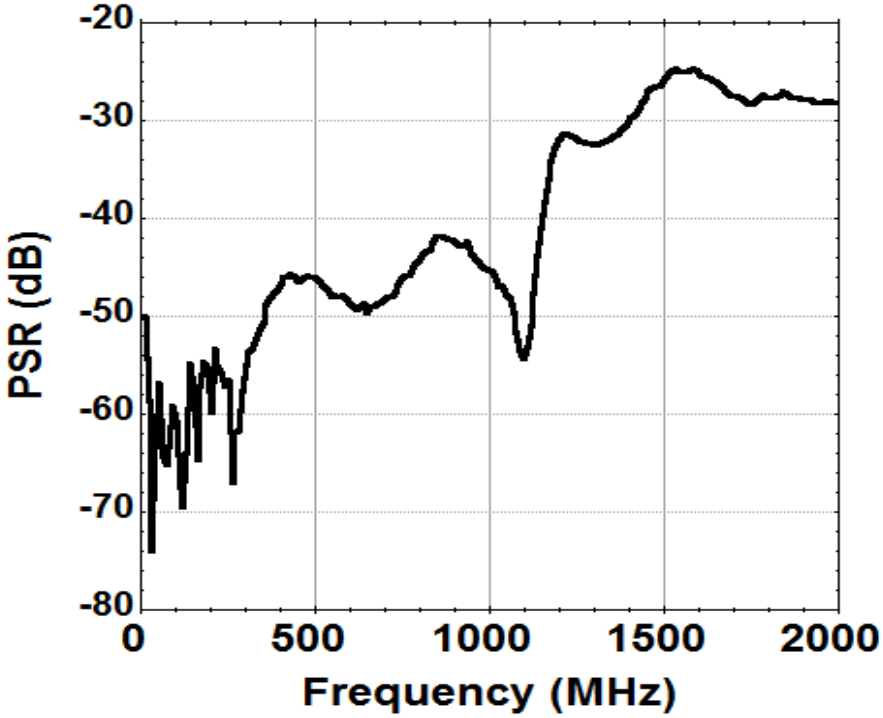


Figure 77. Measured PSR of the proposed LDO.

The linearity and transient performance of the proposed LDO was tested in an envelope tracking configuration. In this work, LDO drives the 433 MHz SOI-MESFET power amplifier discussed in the previous chapter. Figure 78 shows the test setup block diagram used in this work. Appendix-A talks about the test setup in more details. As the first step a two tone signal was applied to the PA input and the envelope was used to drive the LDO. Effect of supply voltage variation on linearity of this ET transmitter is shown in Figure 79. For a fixed PA V_{DD} of 2 V, IM3 components are 35dB lower than the fundamental tones. Measurements show that IM3 starts growing when envelope signal swing on the supply voltage is more than 0.8 V.

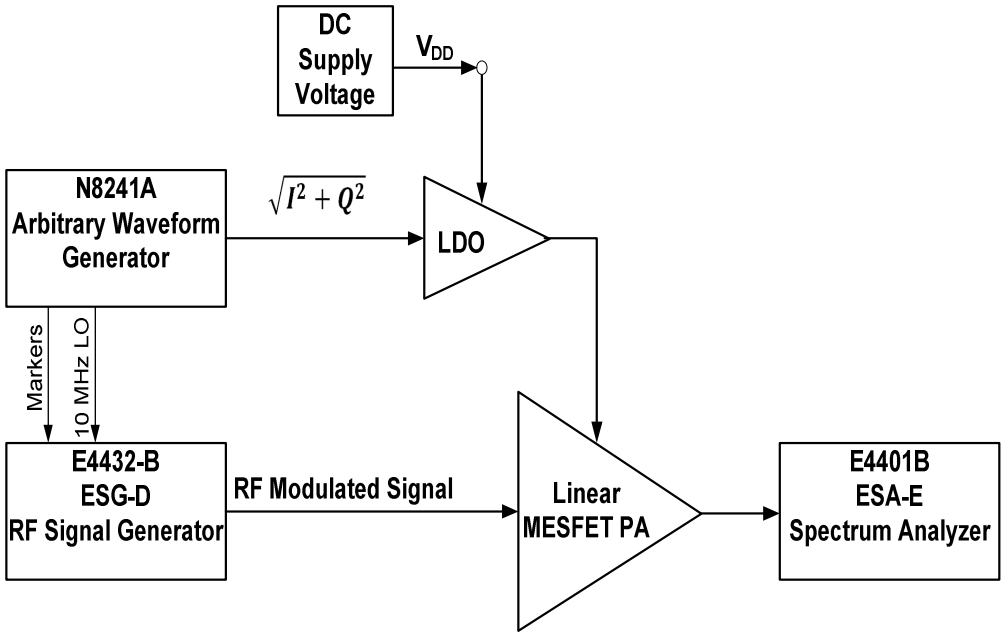


Figure 78. SOI-MESFET envelope tracking test setup.

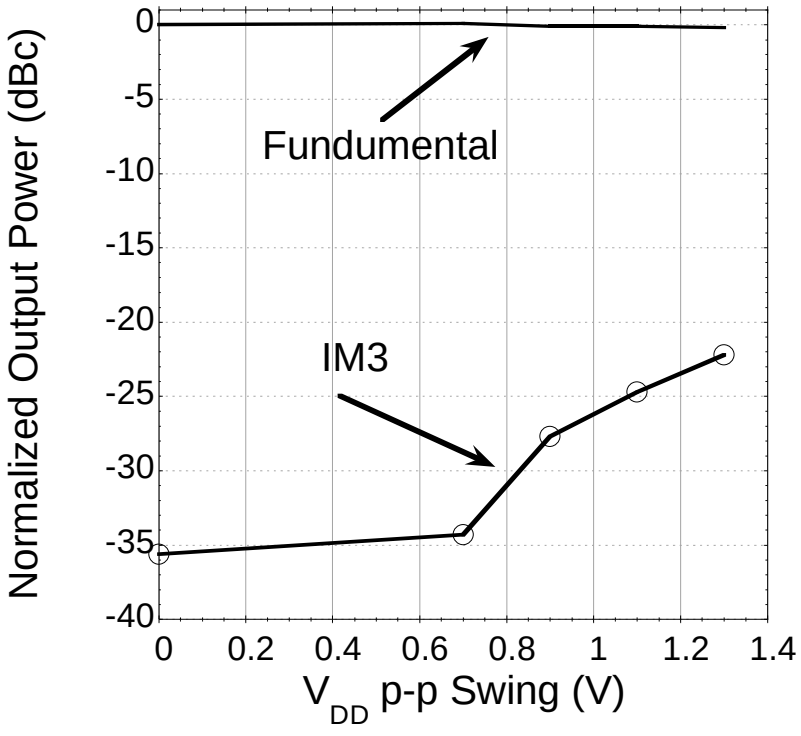


Figure 79. Effect of supply voltage swing on linearity.

An RF modulated EDGE signal was used to drive the PA input and the envelope of the EDGE signal was used to drive LDO in an ET architecture. The transient input and output voltage of LDO was captured using an Infiniium Agilent oscilloscope and is plotted in Figure 80. RMS value of weighted error signal is approximately -57 dB. Effect of envelope voltage swing on linearity of EDGE signal is shown in Figure 81. This plot shows the tradeoff between supply voltage swing (efficiency improvement) and linearity. Larger envelope swing results in better efficiency with the cost of more nonlinearity.

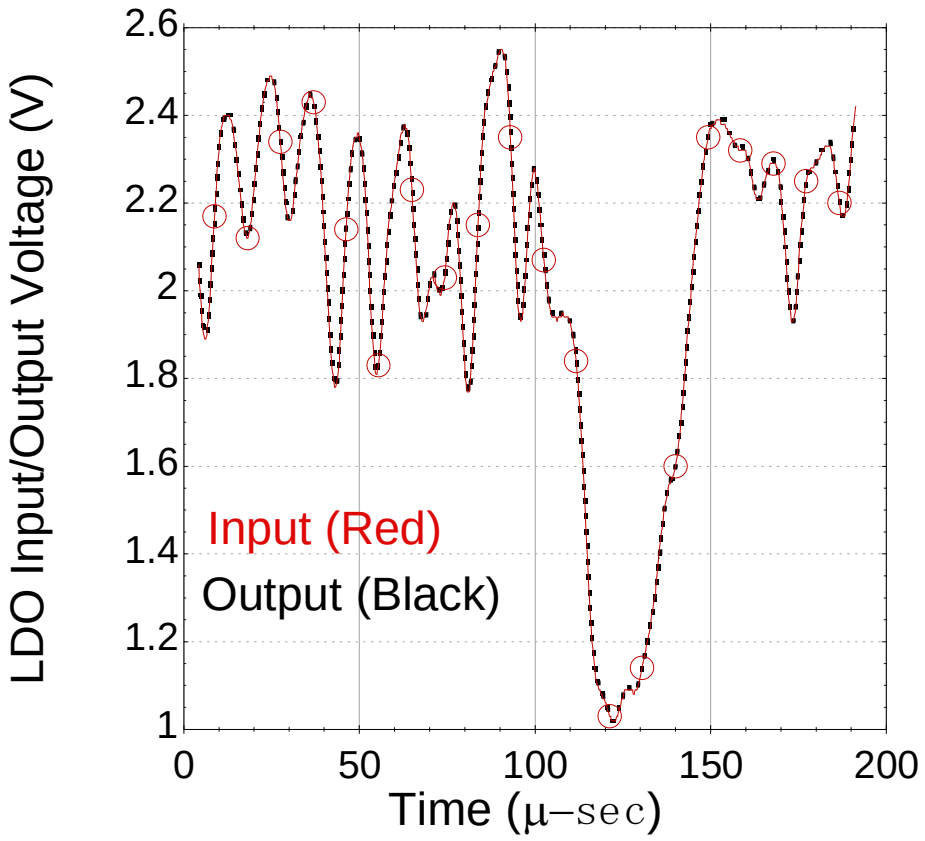


Figure 80. Transient input and output voltage of LDO for EDGE envelope signal.

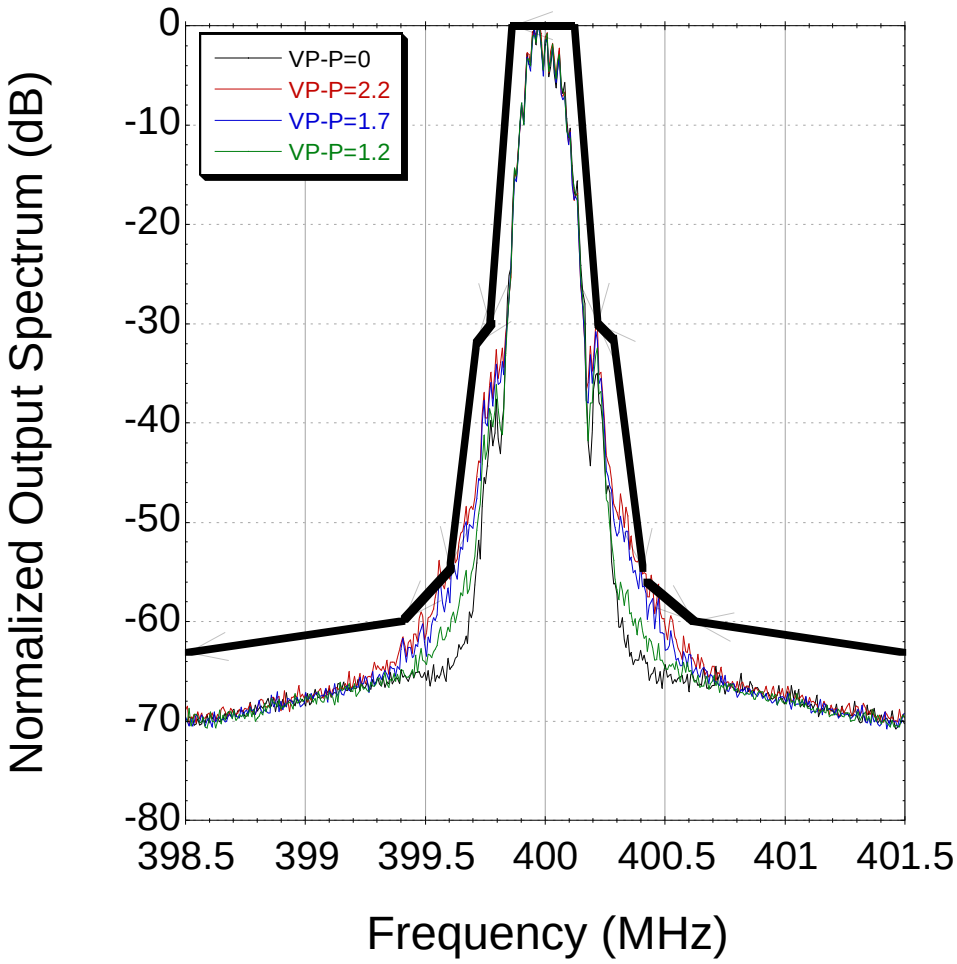


Figure 81. Normalized output spectrum of MESFET ET for EDGE signal.

LDO was fabricated on a FR4 board using a packaged SOI-MESFET and AD8061 Analog Device op-amp. The photograph of the LDO board is shown in Figure 82.

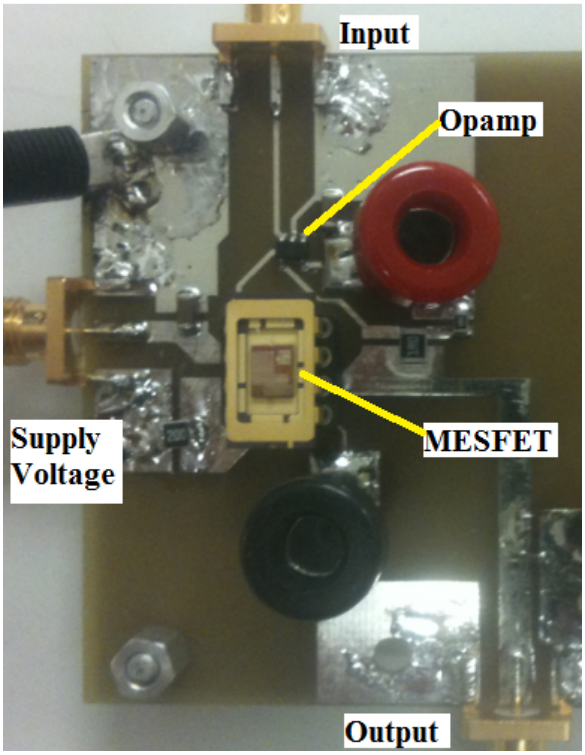


Figure 82. Photograph of the 350 MHz SOI-MESFET LDO.

4.4. Summary

This chapter discussed the need for RF transmitters which have less efficiency degradation at backed-off powers. Polar transmitter was introduced as a solution, and different polar architectures were outlined. Polar transmitter introduces switching noises on the PA supply node. To remedy this problem, a high speed and stable LDO is required. Depletion mode behavior of SOI-MESFETs makes it possible to achieve several hundred megahertz of bandwidth and decent stability at the same time. This idea was validated by designing and measuring an SOI-MESFTE LDO with 350 MHz bandwidth. LDO was tested in an ET architecture driving a MESFET PA. Measurement results show that the proposed ET transmitter satisfies EDGE requirements.

CHAPTER 5

BACKGATE MODULATED POLAR TRANSMITTER

Chapter IV explained the idea behind building polar transmitters (PTs) and described different polar architectures. All the efforts in PTs are toward improving the overall transmitter efficiency at backed-off powers, while satisfying the linearity requirements of modern communication standards. A very simplified polar transmitter block diagram is shown in Figure 83.

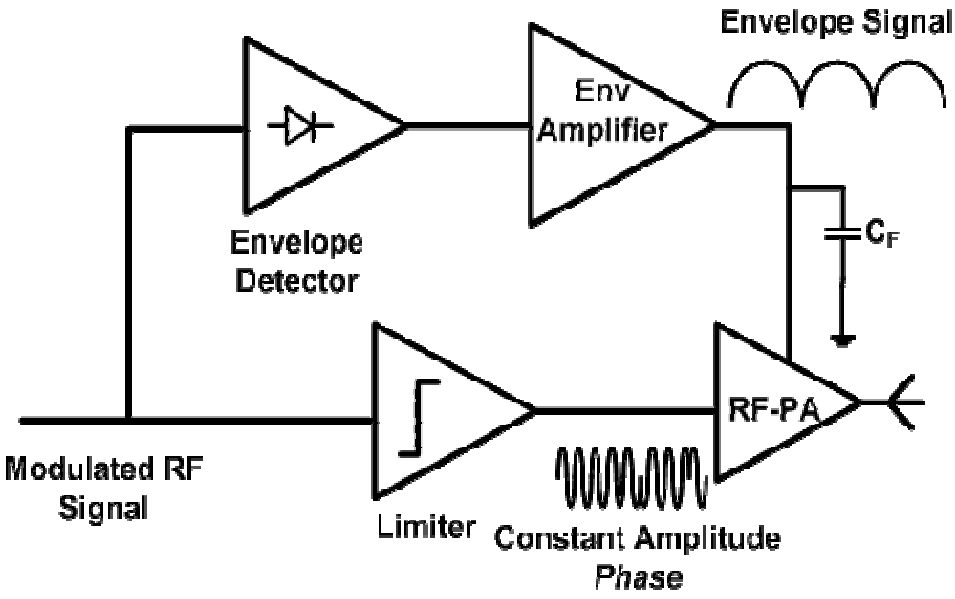


Figure 83. Simplified block diagram of a traditional polar transmitter.

At any output power level, the overall efficiency of the polar transmitter is:

Equation 35

Therefore the envelope amplifier's efficiency is as critical as the PA efficiency. Designing an efficient supply modulator that meets all the linearity specifications, can be as challenging as RF-PA design itself. Buck converters and

switching mode amplifiers are very efficient, but they suffer from bandwidth limitations and switching noises. Combinations of a linear and switched mode amplifier are introduced to regulate the PA supply voltage for wideband envelope signals. As explained in the previous chapter, the efficiency of the hybrid envelope amplifier is not constant for all signal levels and in fact decreases when the envelope signal drops. For a well-designed envelope amplifier and RF-PA, the efficiency reduction is not as significant as standalone PA efficiency degradation in backed-off powers. Thus, it is still possible to improve the average efficiency by using polar transmitters.

Another problem associated with polar transmitters is their low dynamic range due to limited supply voltage swing. Large voltage swing on the PA supply node can change the RF transistor operation mode into the linear (triode) region and causes severe AM-AM and AM-PM distortions.

Taking everything into account, although supply modulated polar transmitters can improve the average efficiency; they introduce many design challenges for meeting noise, dynamic range and linearity specifications of modern standards.

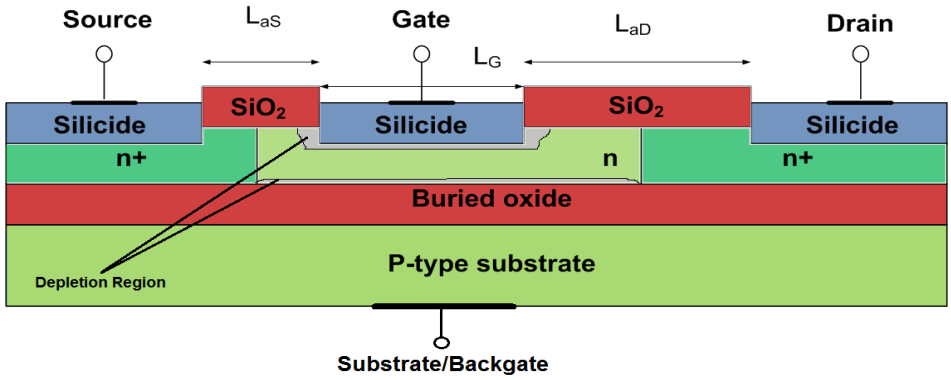
This chapter presents a novel polar architecture that can potentially mitigate some of the problems described above. The main idea behind this work is to control the RF gain and DC power by changing the substrate voltage of a partially depleted transistor on an SOI process. In principle it is the same idea as supply voltage modulation, but the advantages of the proposed technique are higher dynamic range, less design complexity and most importantly higher

efficiency. Higher efficiency can be achieved because of the low power consumption of the envelope amplifier in the proposed architecture. The buried oxide in an SOI processes is an insulator and isolates the backgate terminal from a MOSFET/MESFET device channel. Therefore, there is no DC current going through the backgate terminal.

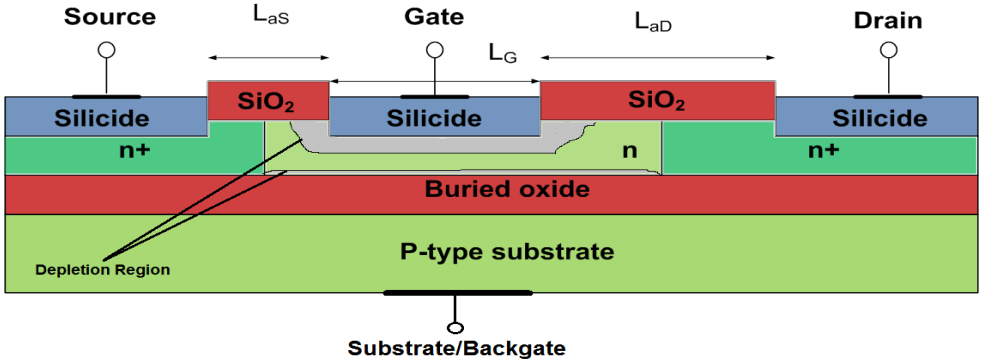
Designing a substrate modulated based transmitter requires a four terminal device model and extraction of the associated device model. Although SOI-MESFET devices are used in this work, the same technique can be applied to MOSFET devices as well. A four terminal Verilog model have been developed for SOI-MESFETs and reported in [62]. The following section talks about DC and RF characterization of SOI-MESFETs fabricated on a 45nm technology.

5.1. Substrate Voltage Effect on Device Characteristics

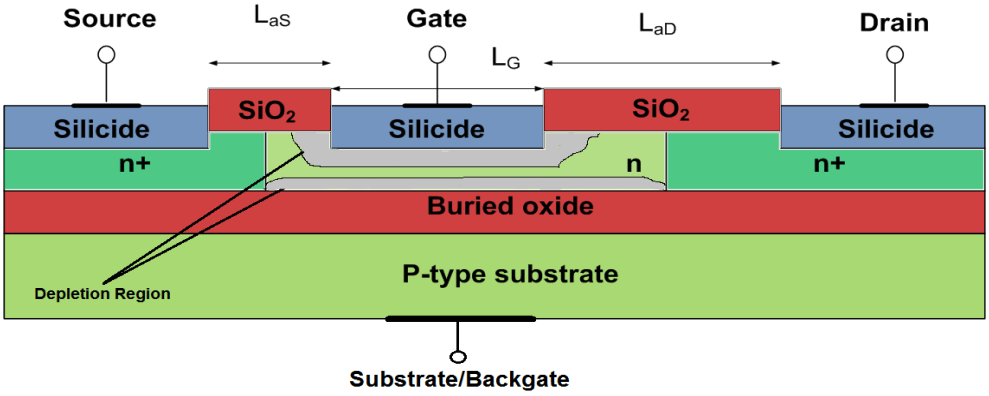
A cross section of a MESFET on a SOI process is shown in Figure 84. Figure 84 (a) shows the depletion region for V_G=0 and backgate voltage, V_{BG}=0. The depletion region grows as the gate voltage becomes more negative in Figure 84 (b) Applying a negative voltage to the substrate also depletes the channel as it is shown in Figure 84 (c). Positive V_{BG} has the opposite effect and reduces the depletion region area.



(a)



(b)



(c)

Figure 84. Cross sectional view of a partially depleted MESFET (a) $V_G=0$, $V_{BG}<0$ (b) $V_G<0$, $V_{BG}<0$ (c) $V_G<0$, $V_{BG}=-2$.

The effect of substrate voltage on the channel thickness of fully depleted transistors appears as a change in the threshold voltage, and as a result changes in DC current. This effect has been studied for SOI-MESFET devices in [62]. Measured drain current versus gate voltage at different backgate biases are plotted in Figure 85.

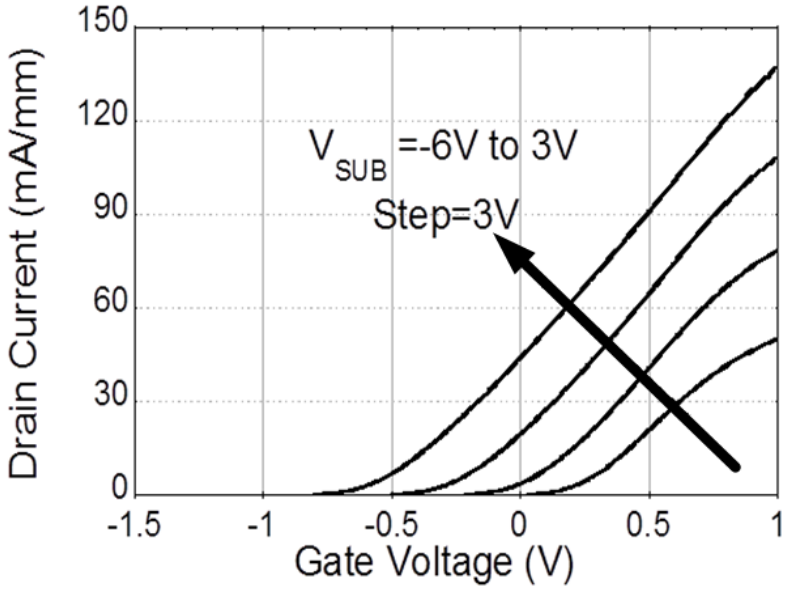


Figure 85. Effect of substrate voltage on SOI-MESFET I/V curve.

DC measurements demonstrate that the SOI-MESFET drain current can be controlled over a wide range by changing the backgate voltage. This property can be used in a polar transmitter to control the DC and RF power. The main barrier toward this task is the AC response of the substrate terminal. The following section discusses the transient and RF response of the backgate contact.

5.2. Transient Behavior of Substrate Contact

The buried oxide layer of SOI wafers is reaching ~100-200 nm in very deep submicron technologies such as the IBM 45nm SOI process used in this

work. Therefore, a smaller voltage is required to modulate the channel thickness. The input impedance of the backgate terminal was measured and is plotted in Figure 86. At low frequencies, the input impedance is a capacitive load of ~4-5pF.

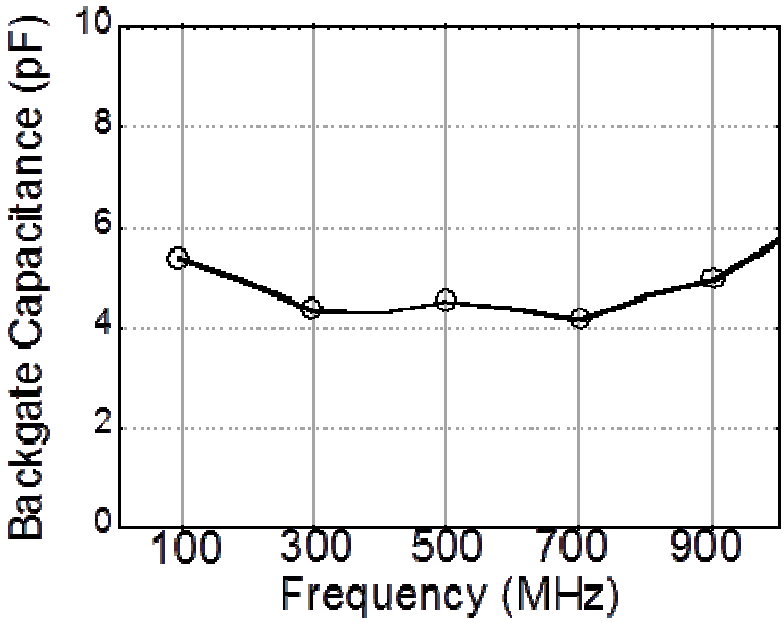


Figure 86. Measured input capacitance of the backgate terminal.

The low capacitance of the backgate terminal allows us to drive the backgate contact with a time varying signal having bandwidth of more than 100 MHz. To validate the idea, a 100 KHz square wave signal is applied to the substrate of a class-B MESFET power amplifier and the output voltage is captured with an oscilloscope. At the same time an RF signal at 433 MHz is applied to the Schottky gate. The transient output signal is shown in Figure 87. This plot demonstrates that the RF power can be modulated with a baseband signal fed to the backgate terminal.

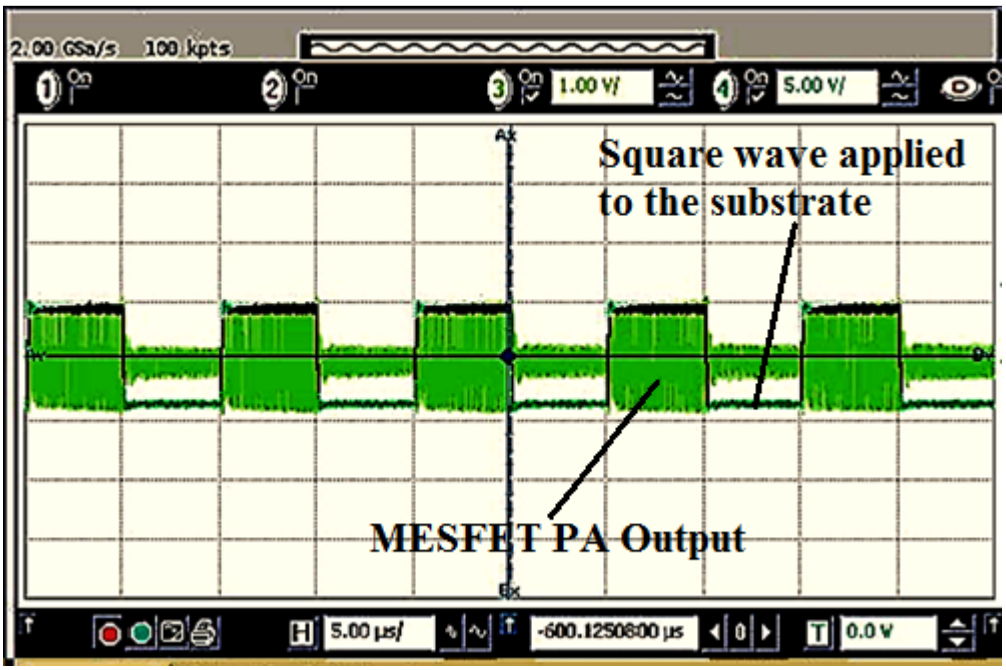


Figure 87. Transient behavior of a SOI-MESFET PA when the backgate is driven by a 100 KHz square wave.

5.3. Efficiency Enhancement Using Backgate Modulation

The previous sub-sections described how DC and RF power of SOI-MESFET/MOSFET PAs can be controlled using the backgate terminal. Measurement results of a backgate modulated SOI-MESFET polar transmitter are presented in this section. In a supply modulated EER transmitter, the output power is controlled by changing the supply voltage of the power amplifier, while the input power is constant. In the proposed polar transmitter, the supply voltage and RF input power are constant, and the output power is controlled by the substrate voltage. Figure 88 shows the block diagram of such a polar transmitter architecture. The envelope amplifier of this transmitter drives a capacitive load of ~2-pF. Therefore, a very low power (less than 5mW) baseband amplifier can be

used for this purpose. Power consumption of this envelope amplifier has a negligible effect on the overall transmitter efficiency.

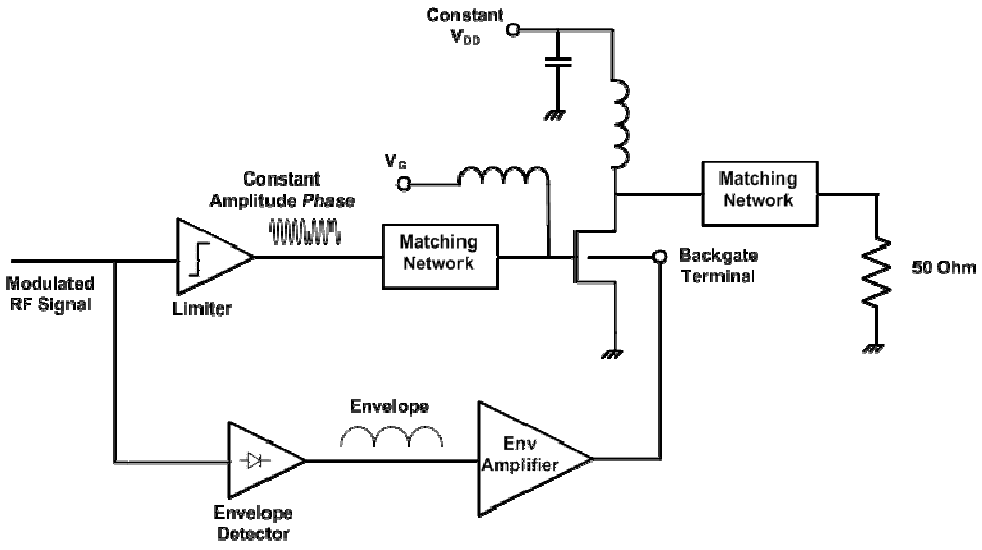


Figure 88. Block diagram of the proposed backgate modulated polar transmitter.

The static effect of the backgate voltage on the PA performance is shown in Figure 89. It shows that as the V_{BG} goes up, higher output power can be achieved. Output power and PAE are measured versus the substrate voltage and plotted in Figure 90. The peak PAE of the proposed polar transmitter is the same as the RF-PA peak efficiency. The main goal though is to improve the efficiency at backed-off output powers. PAE improvement using the proposed method in comparison to the traditional class-AB RF-PA is shown Figure 91. In the traditional approach V_{DD}, V_G and V_{BG} are constant and the RF PA is fed by a modulated RF input signal. To make a fair comparison, the same RF-PA was used in the proposed polar transmitter. Measurement results show 15% PAE improvement at 5-dB backed-off power using backgate modulation.

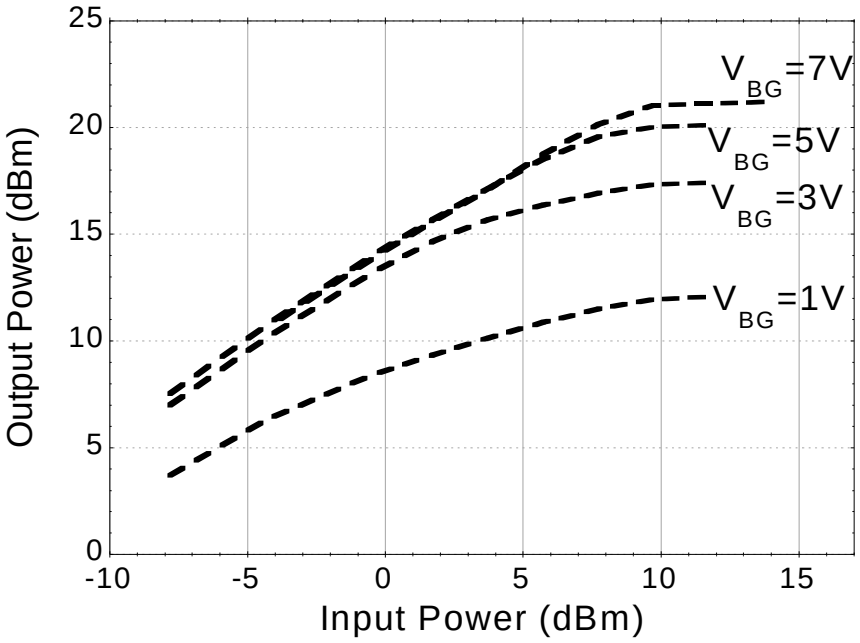


Figure 89. Effect of the backgate voltage on the MESFET RF-PA output power. VDD=3V, VG=-0.2V.

Output power and PAE are measured versus the substrate voltage and plotted in Figure 90.

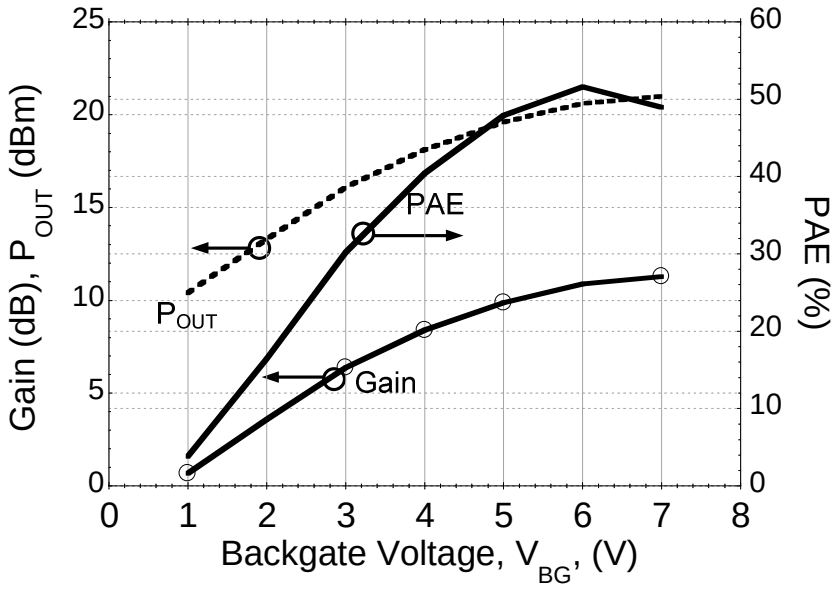


Figure 90. SOI-MESFET Power Amplifier performance versus the substrate voltage.

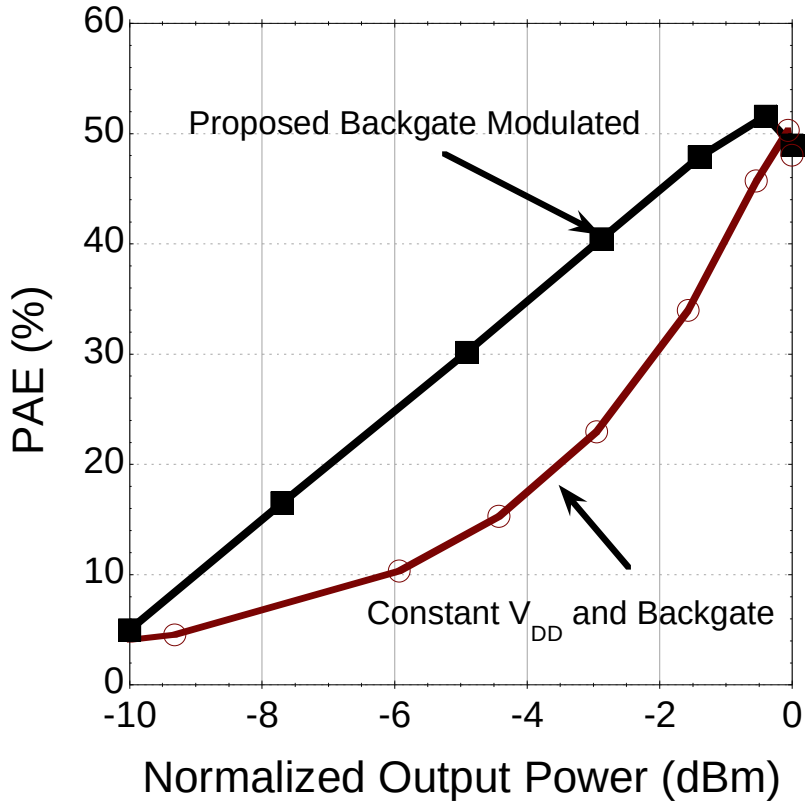


Figure 91. PAE versus output power comparison between the traditional class-AB PA and a backgate modulated polar transmitter.

One of the challenges in implementation of supply regulated polar transmitters is their low dynamic range. At low supply voltages, the RF transistor goes to the triode (linear) region and causes severe AM/AM and AM/PM distortions. A comparison between AM/PM behavior of the MESFET PA with respect to backgate terminal and supply voltage is shown in Figure 92 and Figure 93. The voltage sweep range in this measurement translates to ~13dB dynamic range for both backgate and supply modulation architectures. However, sweeping VDD changes the phase by 25 degree, where the backgate modulation only causes 6 degrees of phase change.

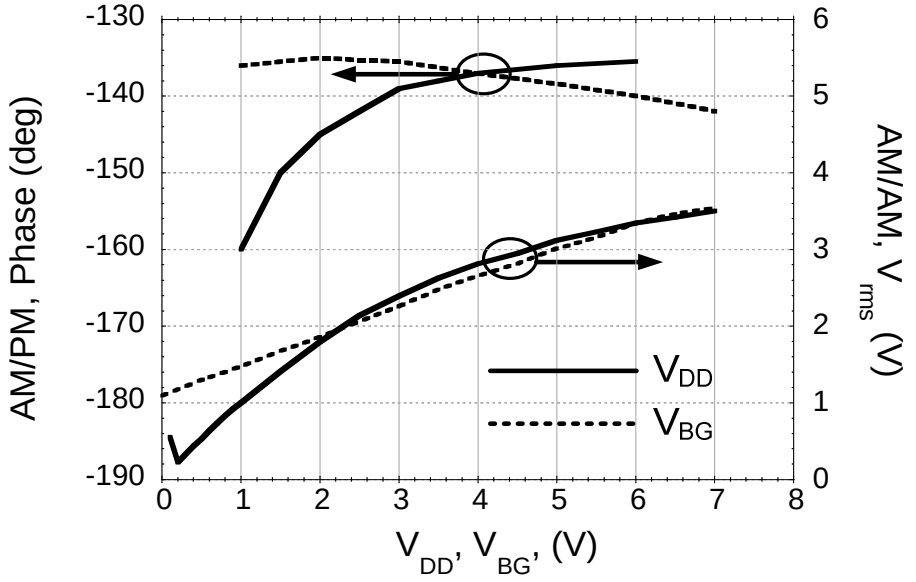


Figure 92. Measured AM/PM characteristics of SOI-MESFET 1.8GHz PA at fixed input power of 6-dBm.

The linearity performance of the proposed PT was measured in an envelope tracking structure fed by an EDGE signal. The measured normalized output spectrum is shown Figure 94. As it is specified on the graph, the backgate modulated ET output spectrum satisfies the mask requirement for EDGE signals. Efficiency improves by a factor of 1.3 for EDGE signal when the envelope signal is applied to the backgate comparing to the constant bias condition.

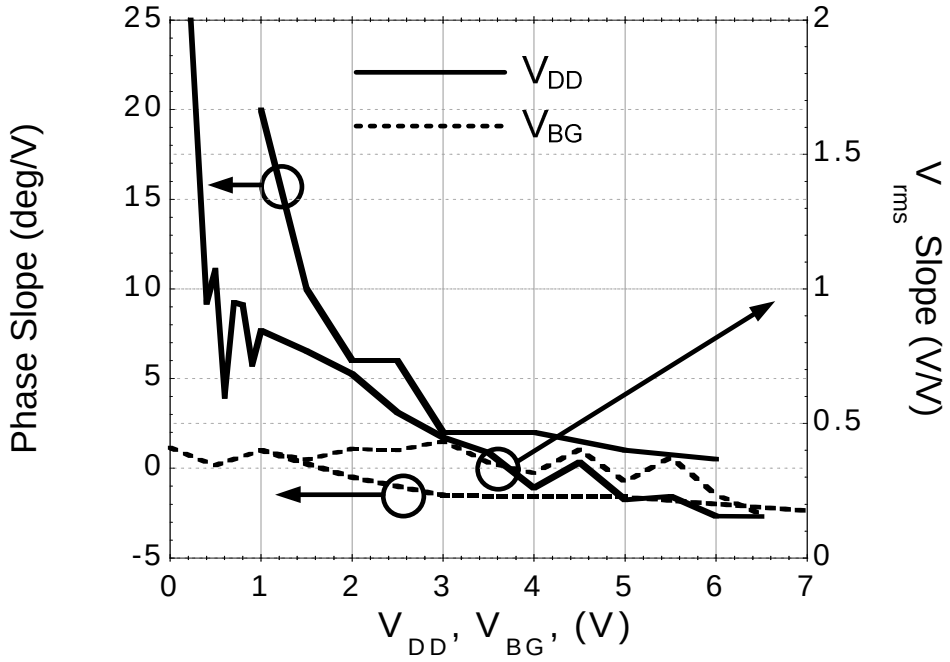


Figure 93. Measured slope of AM/PM curves for VDD and VBG sweeps.

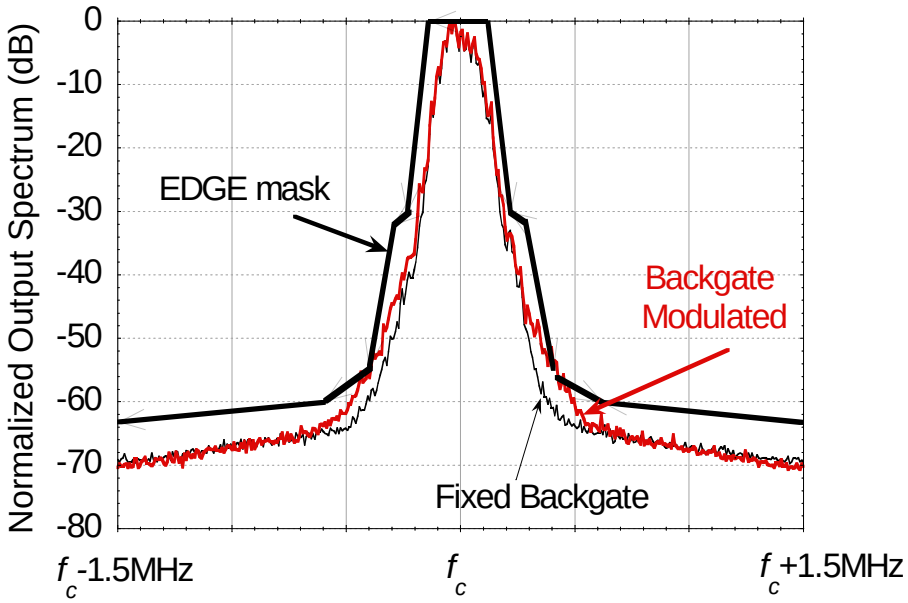


Figure 94. Output spectrum of EDGE signal for backgate modulated SOI-MESFET ET transmitter.

5.4. Backgate Modulation versus Supply Modulation

Although the peak PAE of a backgate modulated PT is the same as the RF-PA peak efficiency, PAE still drops as P_{OUT} is reduced. A similar problem is also associated with supply modulated polar transmitters. In that case the efficiency of the envelope amplifier reduces as the output power decreases. Equation 35 reflects this effect in the overall efficiency calculation of the supply modulated polar transmitter.

Efficiency drop at backed-off powers in the backgate modulated PT can be also modeled by a PAE scaling factor, ζ. ζ is not physical power dissipation in the envelope amplifier. It is simply a parameter which is defined for comparison purposes. ζ is very similar to the supply modulator efficiency and plays the same role in PAE calculation of Equation 35. Overall PAE of a backgate modulated PT can be calculated as:

$$\eta_{Total}(P_{OUT}) = \zeta(P_{OUT}) \times \eta_{PA\_MAX} \qquad \text{Equation 36}$$

ζ for a measured SOI-MESFET PA is extracted and plotted versus output power in Figure 96. To perform a fair evaluation, the supply modulator's efficiency results, presented in [63], are used as a reference in this section. Efficiencies reported in [63] are among the highest numbers reported to the date.

Figure 96 shows the comparison between the proposed technique and the traditional supply modulated PT reported in [63]. Although the proposed method has higher efficiency at high output powers, the supply modulated shows better performance for normalized P_{OUT} less than -4dBm. The quicker efficiency drop of

the backgate modulated PT is mainly due to the RF gain reduction at low output powers. RF input power is constant for backgate modulated data collected in Figure 91. This problem can be resolved by applying a lower input power at backed-off output power. Figure 95 shows efficiency versus P_{OUT} at different input powers. This graph shows that higher PAE is achievable for a fixed P_{OUT} if lower P_{IN} is used.

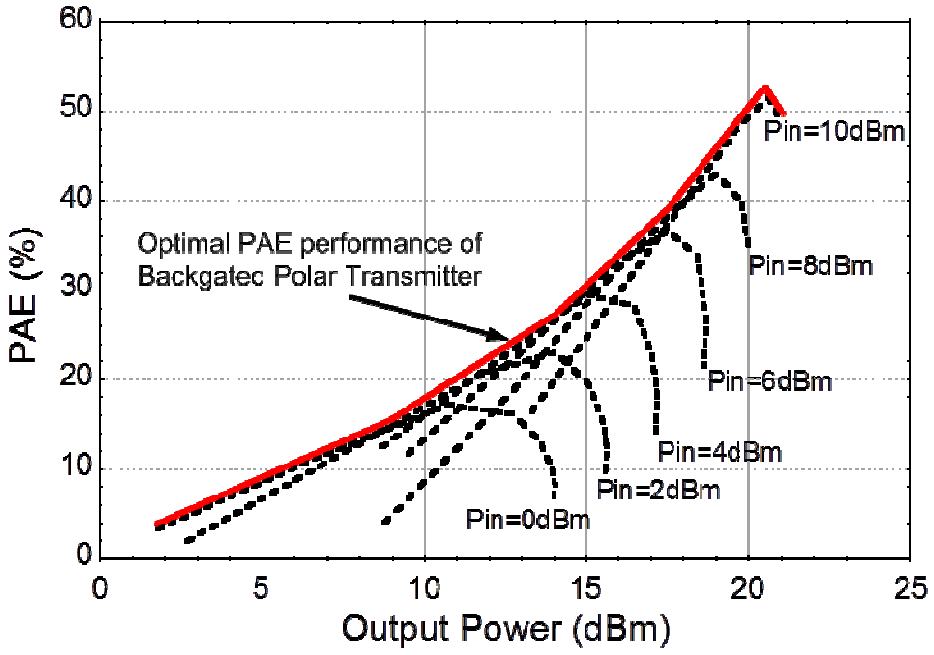


Figure 95. PAE of backgate modulated PT at different input power levels.

Efficiency of the pre-distorted backgate modulated PT is compared to the hybrid supply modulator in Figure 96. The proposed method has higher efficiency for a 6-dB range of output power. Peak efficiency is ~20% higher than the hybrid buck and LDO supply voltage modulator.

It has to be mentioned that the power amplifier efficiency drops very fast as V_{DD} approaches the knee voltage of the RF transistor. Thus, even though the

supply voltage modulator efficiency is ~40% at -12dB backed-off, the overall efficiency can be much poorer.

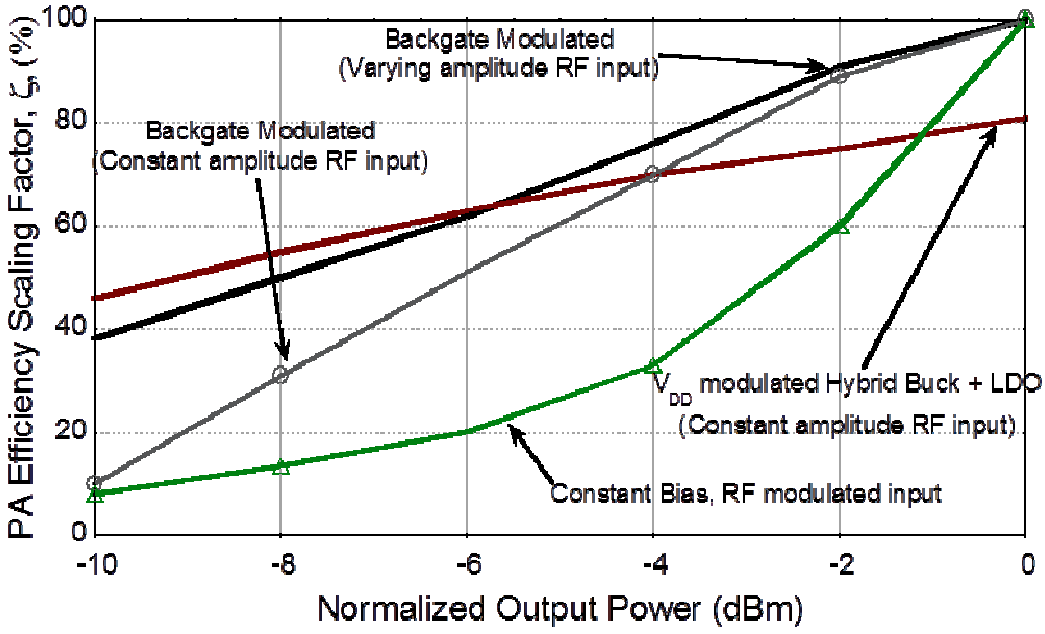


Figure 96. Efficiency comparison between the hybrid supply modulator [63], backgate PT and pre-distorted backgate PT.

5.5. Summary

A novel polar transmitter architecture was introduced in this chapter. The proposed polar transmitter uses the backgate voltage to control the output power. Efficiency performance versus output power were measured and compared to a traditional class-AB SOI-MESFET RF-PA. The proposed technique shows ~3X PAE improvement at 8-dB backed-off power.

A low power, high speed envelope amplifier can be used in this architecture. In traditional supply modulated polar transmitter, a very high power and low noise amplifier is needed. This adds design complexity and result in lower efficiency comparing to backgate modulated PT. More than 10% efficiency

improvement was achieved comparing to supply voltage modulation by using a look-up table and pre-distorting the input signal.

CHAPTER 6

CONCLUSION

The low breakdown voltage of MOSFET devices on deep sub-micron technologies limits the output power of RF transmitters and adds lots of reliability concerns to RF PAs design. The SOI-CMOS compatible MESFET was introduced as a potential solution for some of the issues associated with RF power amplifier design on silicon CMOS technologies. SOI-MESFETs can be fabricated on SOI and SOS processes with no additional cost. MESFET offers higher breakdown voltage comparing to MOSFETs fabricated on a same process. Therefore more robust high power RF-PA can be designed using these devices.

SOI-MESFETs fabricated on different SOI and SOS processes were characterized from DC to 40 GHz. DC measurements demonstrates 2-30X breakdown voltage enhancement using MESFETs compared to MOSFETs on the same SOI-CMOS process. The cost for higher breakdown voltage is lower cut-off frequency. This trade-off was studied in this thesis and the MESFET geometries were optimized to achieve enough RF gain as well as high breakdown voltage. RF measurements showed that MESFETs can be used in power amplifiers operating in the frequency range of DC-2.5GHz.

As the first step, the idea was validated using ADS simulation tool. For that purpose, a TOM3 model was developed and validated for silicon MESFETs fabricated on a 45nm and 150nm CMOS processes through simulation of measured devices. The nonlinear behavior of the model was tested by comparing

the simulation and measurement results of a 433MHz Class AB SOI-MESFET power amplifier.

The first demonstration of SOI-MESFET RF power amplifiers are presented in this thesis. SOI-MESFETs on a 45nm process provide enough RF gain for power amplifier applications below 2.5 GHz. The RF gain can be further increased by using a MOSFET device as the input transistor and MESFET as the cascode device. A 1 GHz RF-PA using the proposed cascode structure was designed and simulated in ADS. Simulation results show ~75 % PAE and 24dBm output power. Several MESFET only RF-PAs were designed and measured at 433, 900 and 1800 MHz. Peak PAE of 55% and output power of 22.5 dBm were measured. To achieve higher efficiency and better linearity, MESFETs need to be characterized using load pull tuners.

SOI-MESFETs also have some advantages over MOSFETs in low drop-out regulators. LDOs are used in polar transmitters to improve the efficiency at backed-off powers. Polar transmitter introduces switching noises on the PA supply node. To remedy this problem, a high speed and stable LDO is required. Depletion mode behavior of SOI-MESFETs makes it possible to achieve several hundred megahertz of bandwidth and decent stability at the same time. This idea was validated by designing and measuring an SOI-MESFET LDO with 350 MHz bandwidth. The LDO was tested in an ET architecture driving a MESFET PA. Measurement results show that the proposed ET transmitter satisfies EDGE requirements. As a future work, the error amplifier can be integrated on the same

die as the pass transistor. Integrating the LDO's error amplifier helps achieving better efficiency and wider bandwidth.

A novel polar transmitter architecture was also introduced in this thesis. The proposed polar transmitter uses the backgate voltage to control the output power. Efficiency performance versus output power were measured and compared to a traditional class-AB SOI-MESFET RF-PA. The proposed technique shows ~3X PAE improvement at 8-dB backed-off power. A low power, high speed envelope amplifier can be used in this architecture. In traditional supply modulated polar transmitter, a very high power and low noise amplifier is needed. This adds design complexity and result in lower efficiency comparing to backgate modulated PT. More than 10% efficiency improvement was achieved comparing to supply voltage modulation by using a look-up table and pre-distorting the input signal. This idea can be more developed by implementing an EER polar transmitter. This task requires a high voltage low frequency op-amp to be designed.

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APPENDIX A

ENVELOPE TRACKING TEST SETUP

EDGE signals are generated in ADS using EDGE signal source. Agilent N8241A arbitrary waveform generator was used to generate the envelope signal and the Agilent E4432B was used for up converting the baseband EDGE I and Q signals. Two differential, high speeds, high resolutions digital to analog converters (DACs) are placed in this signal generator. The sampling frequency of N8241A is fixed to ~625 MSPs. The EDGE signal generated in ADS has only 8X oversampling ratio. Therefore, we up-sampled the envelope signal by a factor of 300X and passed it through a low pass filter to achieve a correct analog signal for the envelope path. This task was done using interpolation command in Matlab. Data generated in ADS are taken into Matlab for scaling and formatting. An m-file was used to scale EDGE signal to signal generators DAC range. The m-file script is shown at the end of this section.

Another consideration in the test setup was synchronizing the two signal paths. N8241A have markers output and we used them to trigger the E4432B. Basically, N8241A outputs a pulse on the marker port, which shows that the frame is finished and re-triggers E4432B. The delay associated with cables should be manually tuned. N8241A Control Utility software, available on Agilent website, was used to load the data into DACs memories. E4432B was controlled by ads in software from Agilent that works on Microsoft Excel.

All the signals should be scaled to the DACs output levels. This task was done by the m-file script shown below.

```
a=EDGE_Envelope(1:16384); % import data from ADS
a=a*2-1;
```

```
NP=16384*300; % increase the number of points by 300X for upsampling
a=interp(a,300); % upsample and low pass filter the edge envelope
b=a*0+1;
%b=(abs(sin((2^6)*(samples)/(NP)*2*pi)));%*0+1;
mkr1=0;
mkr2=0;
%a=min(a,16383);
%a=max(a,0);
i=a;
q=b;
scale=1;
mx = max([max(abs(i)) max(abs(q))]); % scale data to the DACs range
scaleint = round(8192*scale)-1
i = i/mx*scaleint + 8191; % Make 14 bit unsigned integers
q = q/mx*scaleint + 8191;
i=round(i);
q=round(q);
i = min(i,16383); % Just to be safe
i = max(i,0);
q = min(q,16383);
q = max(q,0);
i=double(i);
q=double(q);
```

```
size(i)
i(1)=i(1)+mkr1*16384+mkr2*32768; % Set markers to begin segment
fk=fopen('c:\ESG\sine_AWG_q2.bin','wb'); % N8241A takes .bin format
cout=fwrite(fk,q,'int16');
fclose(fk)
fk2=fopen('c:\ESG\sine_AWG_i2.bin','wb')
cout=fwrite(fk2,i,'int16');
fclose(fk2)
plot(b)
```