A 500MSPs Bipolar SiGe Track and Hold Circuit with high SFDR

By

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ABSTRACT

The front end of almost all ADCs consists of a Sample and Hold Circuit in order to make sure a constant analog value is digitized at the end of ADC. The design of Track and Hold Circuit (THA) mainly focuses on following parameters: Input frequency, Sampling frequency, dynamic Range, hold pedestal, feed through error. This thesis will discuss the importance of these parameters of a THA to the ADCs and commonly used architectures of THA. A new architecture with SiGe HBT transistors in BiCMOS 130 nm technology is presented here. The proposed topology without complicated circuitry achieves high Spurious Free Dynamic Range(SFDR) and Total Harmonic Distortion (THD).These are important figure of merits for any THA which gives a measure of non-linearity of the circuit. The proposed topology is implemented in IBM8HP 130 nm BiCMOS process combines typical emitter follower switch in bipolar THAs and output steering technique proposed in the previous work. With these techniques and the cascode transistor in the input which is used to isolate the switch from the input during the hold mode, better results have been achieved. The THA is designed to work with maximum input frequency of 250MHz at sampling frequency of 500MHz with input currents not more than 5mA achieving an SFDR of 78.49 dB. Simulation and results are presented, illustrating the advantages and trade-offs of the proposed topology.

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Dedicated to my Parents

Mr. Ramakrishna Rao and Mrs. Jyothi Rao

ACKNOWLEDGMENTS

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PREFACE

Track and Hold Amplifiers are a part of most data conversion systems. This study explains the bipolar THA architecture for high SFDR without any complex circuitry. This architecture is designed using 130 nm BiCMOS IBM8HP process. The output steering technique combines with cascade input buffer and emitter follower switch to give better results than the work which adopt only ones of these techniques. The work is divided into five chapters. A brief introduction to the contents of each chapter is outlined below.

Chapter 2 discusses various sample and hold architectures. The figure of merits and problems for any track and hold circuits are discussed in detail. The section after that presents three new S/H techniques, all of which try to minimize the errors caused by charge injection and/or clock feed through. This chapter also gives a background to bipolar track and hold circuits.

Chapter 3 talks mainly about the design of SiGe HBT THA which mainly consists of design of the input buffer with emitter degeneration, output steering resistors, switching buffer (sampling buffer). Finally, the hold capacitor was chosen based on the kT/C noise requirement.

This THA works with an input frequency of 250 MHz and a sampling frequency of 500 MHz.THD of -74 dB and SFDR as high as 77 dB was achieved with the output dynamic range of 1 Vpp. The tradeoff between linearity and speed of a THA can be well understood from the simulations. SFDR with change in the input frequency and sampling frequency has also been discussed. The simulations and results have been described in Chapter 4.

Chapter 5 finally concludes this work with the advantages and disadvantages of this topology. Comparison of the performance of this THA topology with other current topologies has been given in this section.

1. INTRODUCTION

As Data conversion systems continue to improve in speed and resolution, increasing demands are placed on the performance of high-speed sample-and-hold circuits. The throughput of the fastest analog-to-digital converters is typically limited by the speed and precision with which the comparison function can be performed. However, the maximum input signal bandwidth that can be accommodated by a converter at a specified precision is governed by the speed at which the input can be sampled. Most of the data conversion systems use Sample and hold circuit as their front end block. The held voltage at the output of the sample and hold circuit is utilized for analog to digital conversion by the rest of the blocks in analog to digital converters. The simplest sample and hold block with NMOS as switch and hold capacitor is given in the Figure 1.
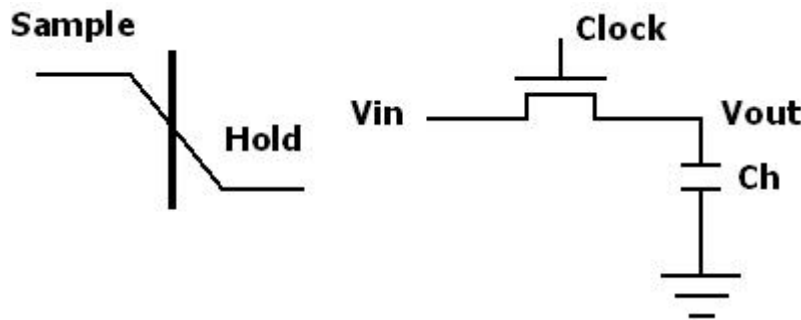
Figure 1 .Simplest Sample and Hold Circuit in MOS Technology [1], [2]

Sample-and-hold amplifier circuits also known as track and hold Circuits or track and hold Amplifiers (THAs) are key building blocks for many discrete time signal processing applications. Their basic function is to transform input continuous signals into discrete time signals and amplify them. Sample-and hold

(S/H) amplifiers track an analog signal, and when given a hold command they hold the value of the input signal at the instant when the hold command is issued, thereby serving as an analog storage device. An ideal S/H amplifier would be able to track any kind of input signal, and upon being given a hold command store at its output, without delay, the precise value of the signal, and maintain this value indefinitely.

It is often desired to take a snapshot of a signal level at a particular time, and save it for later analysis. This is particularly important in analog-to-digital conversion, where changes in the input during the conversion period may lead to erroneous results. The idea is to save the value as the voltage across a capacitor, as shown in Figure 1.In many cases, sample and hold circuits are used to minimize errors due to different delays in internal operation of the data converters. The sample and hold circuits are necessary in data conversion to sample a continuously varying signal and hold it at a constant level for a specific period of time. This value is later used by successive stages of ADCs to give out a digitized output.

Unfortunately, ideal S/H amplifiers do not yet exist, and to be able to pick a S/H amplifier to suit a particular application, one must be familiar with how S/H amplifiers are characterized, and how the S/H specifications will affect performance. Over the years, various sample and hold architectures have been used [4]. The open loop configuration with buffered input and output is fast but the accuracy achieved is less. The closed loop sample and hold offers the advantage of better resolution/accuracy but is slow because of the global

feedback. Each topology has found its own application depending on the trade-offs [4]. In addition, although CMOS transistors are widely used for the design of sample and hold circuits, the speed and noise constraints of CMOS limits its use in some high speed high performance track and hold circuits.

Hence, for ADCs with high speed (greater than 150MHz), bipolar circuits have replaced CMOS. Bipolar junction transistors (BJTs) are inherently fast because of their increased transconductance (gm) [5].The majority and the minority carriers in BJTs contribute to higher gm and hence higher speed. SiGe BJTs offer even higher speed as compared to normal homojunction bipolar transistors due to the graded Ge in the base of the bipolar resulting in higher operating frequency and thus higher speed. Therefore SiGe HBTs are used for the design of track and hold circuits in this work.

Sample and hold circuits are characterized by various parameters and figures of merit. The acquisition time, aperture error, droop rate, hold pedestal are some of the major figures of merit for THAs [1],[2]. Major types of errors, clock feed through and charge injection are associated with a S/H implementation [2]. These errors limit the operating frequency for a S/H as they introduce distortion at higher input and sampling frequency increasing the total harmonic distortion (THD) and reducing spurious free dynamic range (SFDR).Various techniques have been incorporated to overcome these sources of errors in the sampled signal.

This thesis discusses the different sample and hold architectures, the parameters and the problems in all S/H circuits. This thesis explains the background work i.e the works published in [1],[2],and [3] in detail. Finally the

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new implementation of a SiGe bipolar track and hold Circuit is presented. This high speed high SFDR sample and hold circuit was designed in IBM8HP 130nm BiCMOS process. The design mainly consists of an input buffer, emitter follower switch and a hold capacitor. The tradeoff between different parameters in the design, the advantages of this particular topology and the specifications achieved will be discussed in the following chapters.

Thesis Structure

Chapter 2 discusses the problems and ,figures of merit for any track and hold Circuit giving a complete background to the new design topology presented in the next chapter. Chapter 3 explains the new topology in detail, The design considerations involved in the design of cascaded input buffer, emitter follower switch and hold capacitor. Chapter 4 presents simulation results for the new topology. Chapter 5 concludes with results achieved and the comparison of the performance of the current design with other works.

2. BACKGROUND

Before discussing different sample and hold circuits, it is necessary to mention some performance parameters used in the characterization of S/H circuits. Later, the merits and drawbacks of each architecture and how each architecture overcomes the problems associated with S/H circuits are discussed.

The hold pedestal or hold step is a serious problem in all S/H circuits. This is an error that occurs each time a sample and hold goes from sample mode to hold mode. During this change in operation, there is always a small error in voltage being held that makes it different from the input voltage at the time of sampling. This error should not be signal dependent otherwise it can introduce nonlinear distortion.

A second important parameter is the speed at which a sample and hold can track an input signal when in sample mode. In this mode, sample and hold will have both small-signal and large signal-limitations due to its -3dB bandwidth. The -3dB bandwidth should be maximized for high speed operation. This can be done by decreasing parasitic capacitances. Having high slew rate is also an important factor which becomes critical in determining the speed of the S/H circuit. Slew rate of a circuit can be increased by increasing the quiescent current of the circuit.

The droop rate in hold mode is another limitation. This error is a drop in output voltage, when in hold mode, caused by effects such as leakage currents due to finite base currents in bipolar transistors and reverse bias junction currents. In most CMOS designs, the gate current is typically neglected. However, the junction currents in the BJT architectures may contribute significantly to leakage

resulting in hold mode droop. In the Figure 2, figure of merits for any S/H circuit and some of the errors are illustrated.
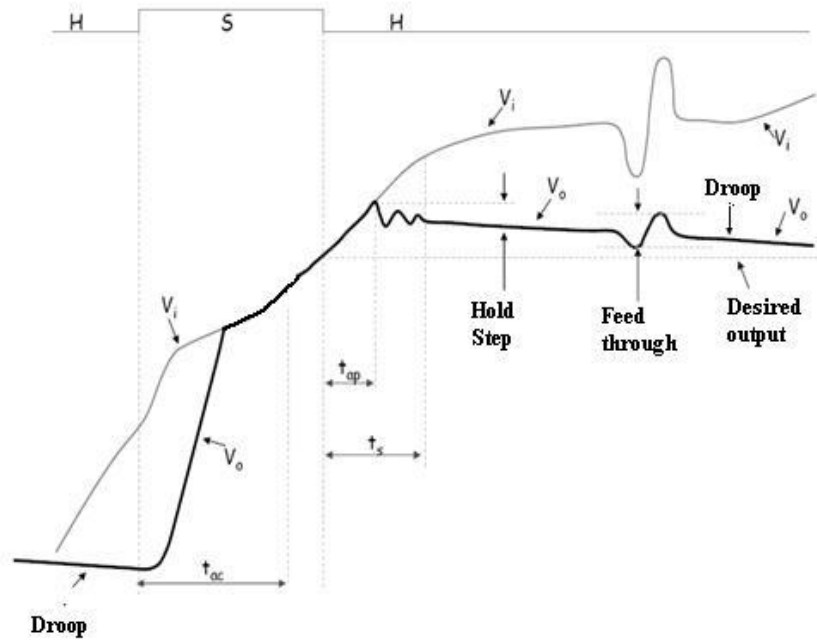
Figure 2. Performance parameters of Sample and Hold Circuit [3]

T_{ac}- Acquisition time- The time taken by the circuit to start tracking the input signal after the sample command is given is known as the acquisition time.

T_{ap}-Aperture time-The time taken by the circuit after the hold command is given to actually turn the switch off .This can also be defined as the time between the start of the hold mode and the instant when the circuit actually starts holing the voltage.

T_s-Settling time- The time required by the circuit to settle to a hold voltage within the specified error band in the hold mode.

V_i-Instantaneous Input Voltage-The input voltage at a particular instant of time

V_o-Instantaneous Output Voltage-The output voltage at a particular instant of time

The random variation of the turn-off time of the switch results in uncertain sampling time. The difference between the time when the hold command is given and when the switch actually starts holding is known aperture error. This error in the holding/sampling instant results in amplitude error of the voltage which is held. In the Figure 3, this has been illustrated as T_{ap} which is the time the circuit takes to actually sample the input voltage.
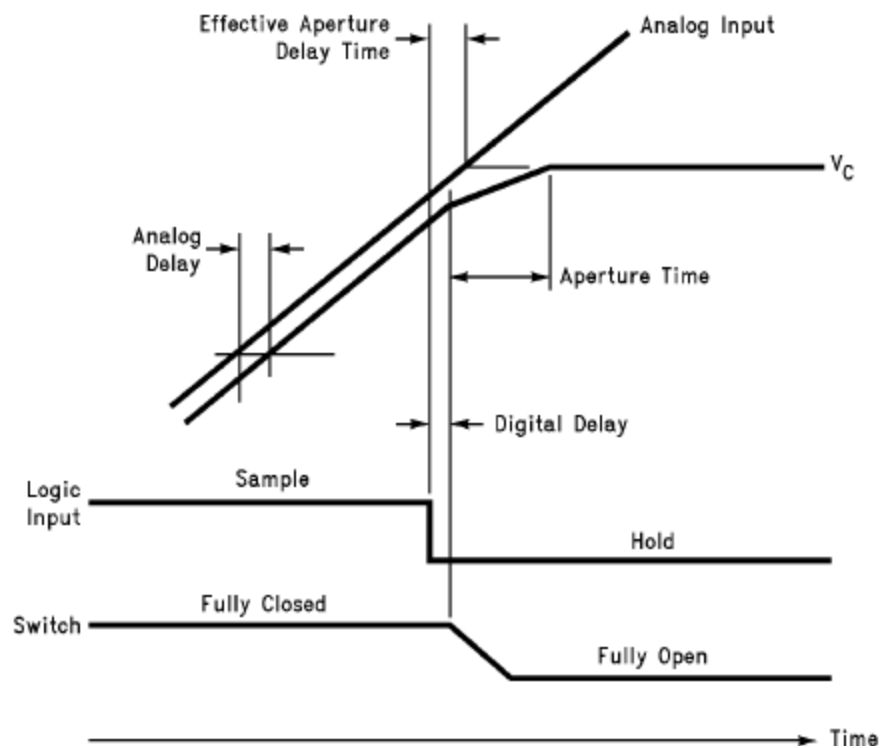
Figure 3.Diagram which shows difference between when the hold command is given when actually data is held gives the aperture time [4]

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2.1 Spurious Free Dynamic Range

In wireless telecommunication applications, large oversampling ratios are often used and the spectral purity of the A/D converter is important. For such situations, a proper specification is the ratio between the powers of the signal component and the largest spurious component within a certain frequency band, called spurious free dynamic range (SFDR). The SFDR is usually expressed in dB as in equation(1)

$$SFDR(dB) = 20 * \log * (V(fsig) / V(fspur)) \ldots \ldots \ldots \ldots \ldots \ldots (1)$$

where $V(fsig)$ is the rms value of the fundamental and $V(fspur)$ the rms value of the largest spurious signal. Spurious signals are undesired signals which could have amplitude or frequency changes. These signals may corrupt the actual desired input. The sources of spurious signals could be substrate noise, noise from the power supply or crosstalk. Normally the limiting factor of the SFDR in ADCs is harmonic distortion. In most situations, the SFDR should be larger than the signal-to-noise ratio of the converter.

2.2 Non –idealities in Track and Hold Circuits

A analog switch is the basic block in all sample and hold circuits. The on/off behavior of an analog switch is controlled by the gate voltages governing the presence of charge in the inversion channels underneath the gates in case of a CMOS switch. The dependence of the input voltages on the on/off behavior of switch is the cause of non-idealities in the sample and hold circuits. As CMOS

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switches are ubiquitous, some of problems with these switches and remedies to over come these non-idealities have been discussed below.

2.2.1 Charge injection

Charge injection is a fundamental problem in analog circuits as well as in some digital circuits like memories. The most commonly accepted charge injection mechanism (in the charge domain) occurs when the switch is turned off, dispersing the charge in the inversion channel, thereby forcing current to flow either into the substrate or the load capacitor at the MOSFET drain or source. This mechanism produces an error voltage on the load capacitor. This flow of electrons was first called charge feed through by Stafford et al. Sheu and Hu Shieh et al published analytical models of strong inversion channel injection and gate to drain overlap capacitive coupling in NMOS switches[5].Figure 4 shows an NMOS whose Clock goes from high to low. The charge is injected to left and right portion of the NMOS.
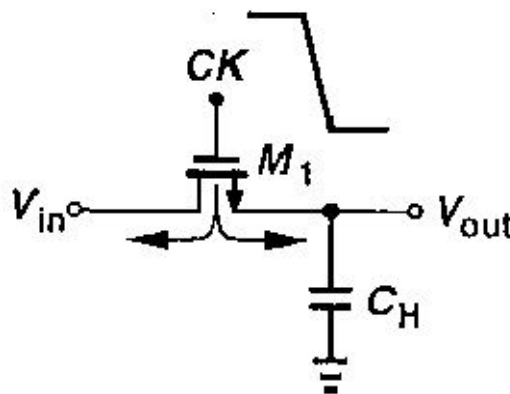
Figure 4. Charge injection in source and drain junctions in a NMOS[1]

When a MOS switch is on, it operates in the linear region (when the Ids is proportional to overdrive voltage which is the gate source voltage minus the threshold voltage) and its drain-to-source voltage, V_{DS}, is approximately zero. During the time when the transistor is on, it holds mobile charges in its channel. Once the transistor is turned off, these mobile charges must flow out from the channel region and into the drain and the source junctions. The charge injection error voltage on the S/H capacitor C_L is determined by the difference between the coupled charge and the charge injected by the transistor current. A slower gate voltage signal provides the MOSFET drain current with additional time to compensate for the coupling error. Figure 5 shows an NMOS transistor with the hold capacitor .The amount of charge injected towards the capacitor is calculated in the equations (2),(3),(4)and (5).
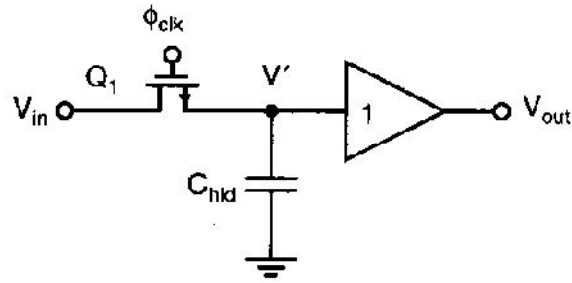
Figure 5. Sample and Hold Block with a sample switch as NMOS, a hold capacitor and an output buffer with unity gain [1]

Figure 5 shows the block diagram of a simple sample and hold architecture. When ϕ_{clk} is high, V^1 follows V_{in}. When ϕ_{clk} goes low, V^1 will ideally stay constant from then on, having a value equal to Vin at the instance ϕ_{clk} went low.

$$\Delta Q_{Chold} = Q_{CH}/2 = (C_{ox} * W * L * V_{overdrive})/2 \quad \dots\dots\dots\dots\dots \quad (2)$$

$$Voverdrive = V_{GS} - V_{tn} = V_{DD} - V_{tn} - V_{in} \quad \dots\dots\dots\dots\dots \quad (3)$$

$$\Delta V^1 = \frac{\Delta Q_{Chold}}{C_{hold}} = -\frac{C_{ox} * W * L * (V_{DD} - V_{tn} - V_{in})}{2 * C_{hold}} \quad \dots\dots\dots\dots \quad (4)$$

$$\Delta V^1 = -(C_{ox} * W * L_{ov} * (V_{DD} - V_{SS}))/C_{hold} \quad \dots\dots\dots\dots\dots \quad (5)$$

This change in voltage due to charge injection will definitely affect the held value across the capacitor. In order to avoid charge injection, many methods were developed. The one of most important ones has been mentioned below. Figure 6 shows a method to reduce the charge injection by the addition of a dummy transistor.
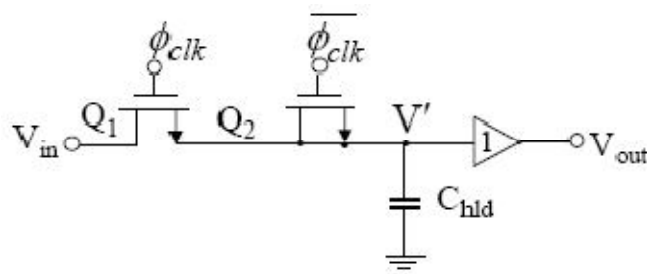
Figure 6. Addition of a dummy transistor to reduce charge injection when the

switch is off [2]

It is assumed that half of the charge is injected to the left (towards Vin) and half of it towards the hold capacitor. So in some implementations such as the circuit shown in Figure 6, a dummy transistor which operates in the inverse phase of clock with size being half of switch is inserted in the signal path. This will

cancel the charge injection from the switch when the switch is turned off and the dummy transistor is on.

2.2.2 Clock Feed through

This parameter is a measure of how isolated the sampled signal is from the input signal when the circuit enters the hold mode. Ideally, the output voltage should no longer be affected by the change in the input signal voltage. But, there is always some signal feed through, usually through parasitic capacitors from the input to the output. Clock feed through is due to the gate-to-source overlap capacitance of the MOS switch. The clock feed through error is due to capacitive path to the S/H capacitor C_L from the overlap capacitor C_{gd} and gate capacitor C_{ox}.

For the S/H circuit of Figure 1, the voltage change at V_{out} due to the clock feed through is given by the equation (6)

$$\Delta V = -C_{parasitic}(V_{DD} - V_{SS})/(C_{parasitic} + C_h) \qquad \text{...................... (6)}$$

where $C_{parasitic}$ is the parasitic capacitance . The error introduced by clock feed through is usually very small compare to charge injection. When the clock feed through is signal-independent it can be treated as signal offset that can be removed by most systems. Thus, clock feed through error is typically less important than charge injection.

2.3 Sample Hold Architectures

The symbol that is frequently used for the S/H amplifier in system block diagrams is a switch in series with a capacitor, as shown in Figure 4. Although the switch can control the mode of the device, and the capacitor can store a voltage, a S/H using just these two would have very poor performance. By studying the deficiencies of such a configuration, one can better appreciate the components that are added to this basic core to comprise a practical S/H amplifier.

First, during the sample mode, the time taken to charge the capacitor for the S/H in Figure 7 is dependent on the source impedance of the input. A large source impedance would give a large RC time constant, leading to a high acquisition time.
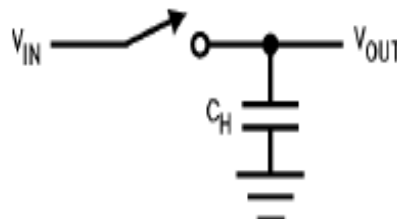
Figure 7.Sampling switch and a hold capacitor-the basic S/H block [4]

To ameliorate this effect, the input is buffered with a operational amplifier (Op-amp) as shown in Figure 8. The acquisition time will then be independent of the source impedance, and will be low due to the low output impedance of an operational amplifier.
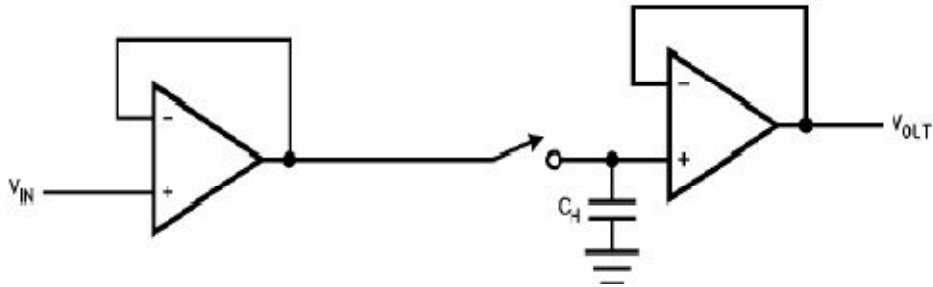
Figure 8.Sample and hold block with an input buffer and an output buffer [4]

Second, when in hold mode the hold capacitor will discharge through the load. Hence, the droop rate will be load dependent and could be very high. To ameliorate this problem, one buffers the hold capacitor from the output with an op amp. The droop rate will then be independent of the load, and will actually be rather low, due to the large input impedance of an op amp. Hence, in addition to a switch and a hold capacitor, a practical S/H amplifier must include input and output buffers. The two main variations of this structure, the open-loop and closed-loop architectures, differ in the manner of their feedback.

In the open-loop architecture shown in Figure 8, the input and output buffer amps are each configured as voltage followers. The advantage of this architecture is its speed—the acquisition time and settling time are short because there is no feedback between the buffer amps. The disadvantage of this architecture is in its accuracy, which suffers because of the lack of feedback, causing the dc errors of both amplifiers to add. For applications requiring high accuracy, one can use the closed loop-architecture, with either a follower output (Figure.9) or an integrator output (Figure.10). The feedback significantly improves the accuracy of the S/H relative to the open-loop configuration, although the speed is somewhat less.

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In both the open-loop architecture and the closed-loop architecture with follower output, the charge transfer, and hence the hold step, is a function of the input voltage. This is because the hold capacitor is connected to the input signal (through the input buffer amp). The closed-loop architecture with integrator output ameliorates this problem by connecting the hold capacitor to virtual ground instead of the input signal. Hence the charge transfer is constant.
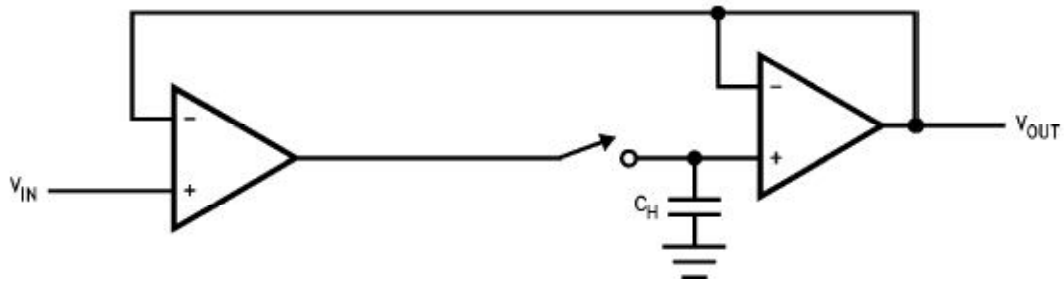

Figure 9. The closed loop architecture of sample and hold circuit[4]
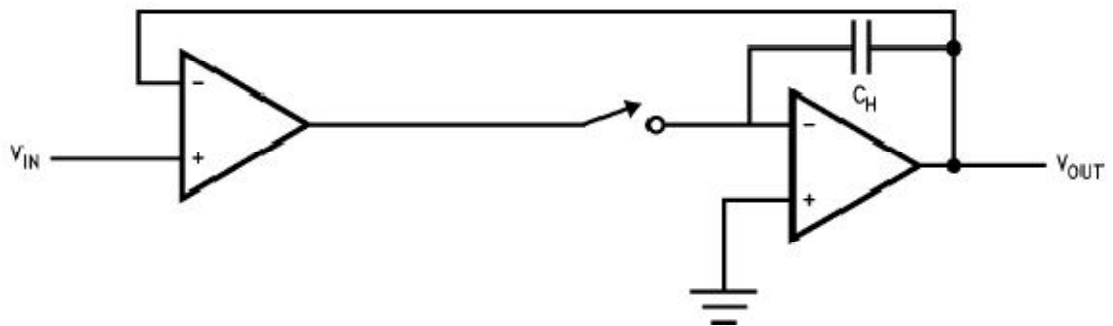
Figure 10. Closed loop architecture of Sample and Hold Circuit with integrator

output [4]

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3. BIPOLAR TRACK AND HOLD CIRCUIT DESIGN

As in the case of any bipolar track and hold circuit [7],[8],[9] and [10], the design developed for this thesis also uses the conventional architecture with an input buffer, emitter follower switch buffer, a hold capacitor and finally an output buffer. Random noise is often the performance limitation of high accuracy THAs in high-bandwidth ADC applications [1]. If the sampled noise power of a THA is to be comparable with the quantization noise of a subsequent ADC, then that places a requirement that the integrated noise on the hold capacitors be 1/4 LSB or less. The emitter-switched topology allows for large signal voltage swing, which helps to meet this demanding requirement. However, the use of a large signal swing increases linearity errors. Thus, linearity compensation techniques become essential.

The design presented here adopts the output steering technique from [8] and the switched emitter follower from [7].In addition to this, the current design a incorporates cascode transistors which connect to actual load RL during the track mode .During the hold mode, cascode transistors are connected to dummy loads and hence the output of the input buffer is isolated from the input signal. The circuit shown in Figure 11, was designed for a supply voltage of 3.3V. The input buffer and switching buffer are implemented with npn transistors only in order to achieve high speeds.

The switch is isolated from the input buffer by emitter follower transistors. This helps to reduce sampling-pedestal error. When switching from track to hold mode, i.e. when the hold signal is given, the transistors with the hold signal draws

all the current brings the emitter follower off. So, the emitter follower is off and hence holding the charge at the end of track mode in the hold capacitors. One of the main advantages of this implementation is that it does not need non-overlapping clocks.
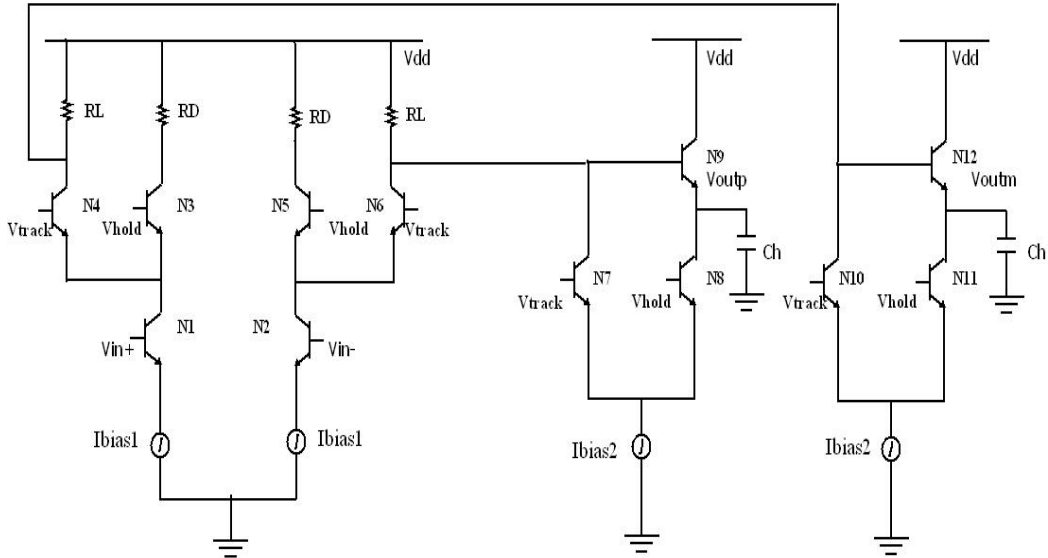
Figure 11. Schematic of Switched buffer THA with input buffer, switching buffer and hold capacitor

The differential output Voutp and Voutm drive a unity gain output buffer. The output buffer is needed in order to avoid the load from affecting the hold capacitor

3.1 Input Buffer

The input buffer consists of input transistors with one pair of cascode transistors which connect to actual loads RL during the track mode and other pair of cascode transistors which connect to dummy loads Rd during hold mode. The resistor values are chosen based on the noise requirement for 10-12bit ADC. The input transistor uses a degeneration resistor in order to improve linearity. The degeneration resistor decreases the gain of the input but increases the linearity of the track and hold circuit. By increasing the degeneration resistor value, the SFDR and THD increased but the signal swing comes down drastically. The two current sources shown in Figure 12 are ideal and biased at 600uA .The implementation of the current sources is discussed later in the chapter. The output of the input buffer goes to an emitter follower switching buffer. As the cascode transistors connected to the actual load are off, the output is isolated from the input. This is isolation is large because now the input transistors are connected to dummy loads. This brings down signal feed through and hold pedestal error by a significant amount. The figure below gives a closer schematic of the input buffer.
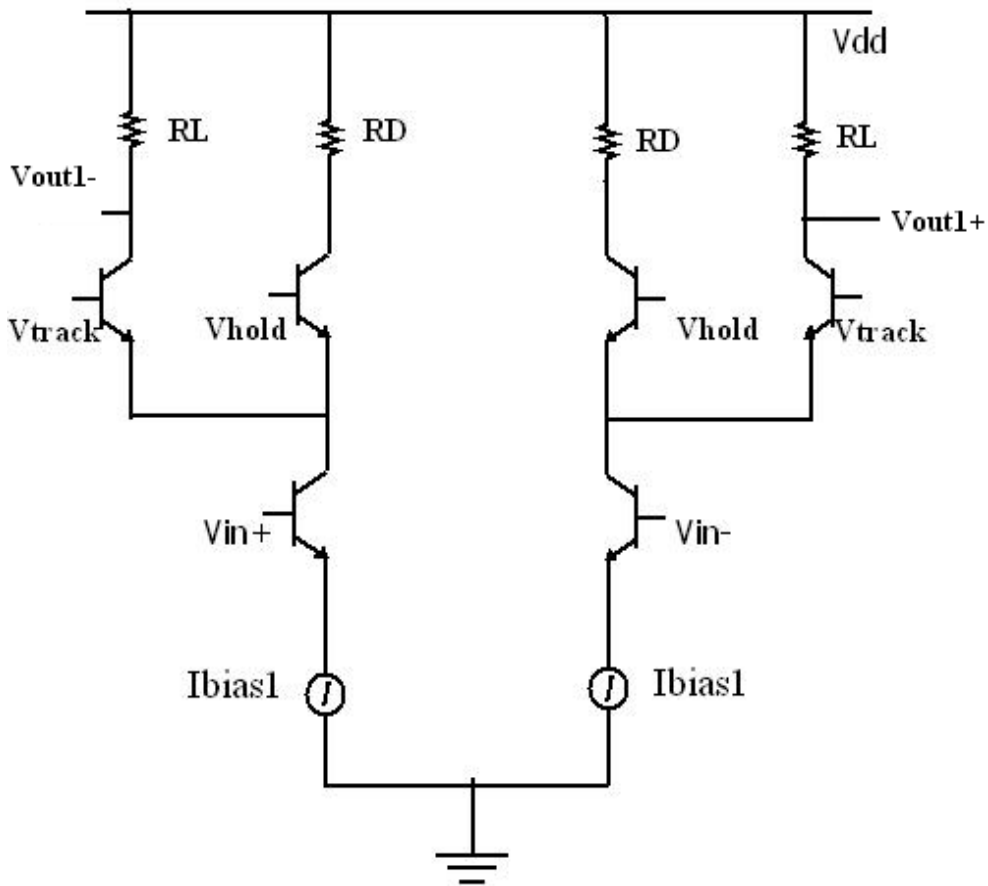
Figure 12. Schematic of the Input Buffer

3.2 Switching Buffer

The emitter follower switching buffer consists of three npn transistors. The emitter follower shields the actual switch from the input buffer. The schematic of the switching buffer is given in Figure 13.
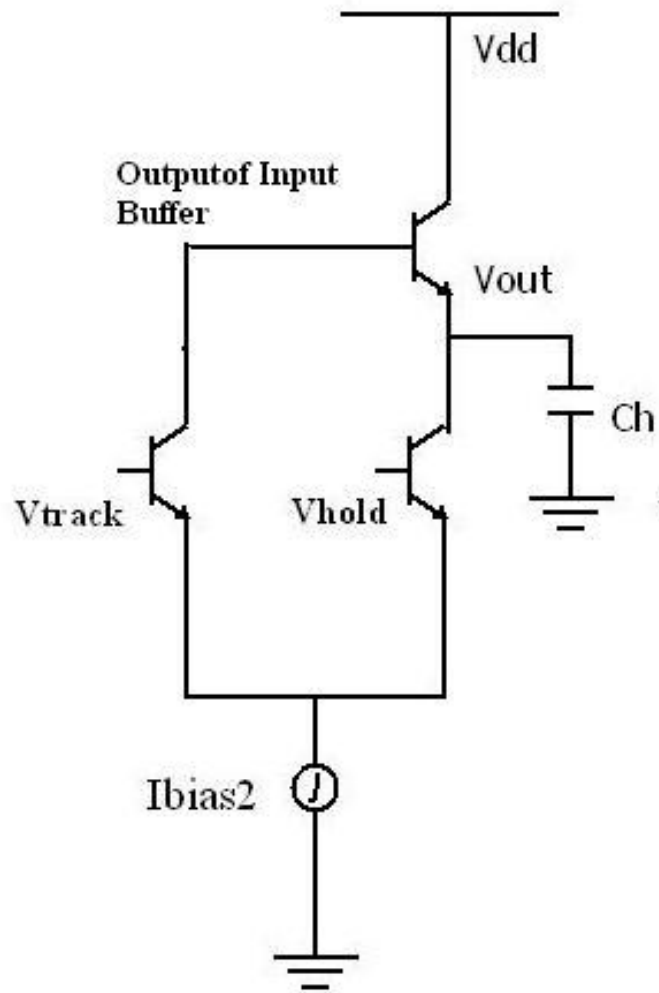
Figure 13. Schematic of the Emitter follower Switching Buffer

In the track mode, the transistor below the emitter follower is on, charging the hold capacitor. In the hold mode, the transistor connected to the base of the emitter follower is on, bringing down the voltage at the base of the emitter follower until it is off. Hence the input buffer is isolated now from the hold capacitor. So, the charge now is same the charge stored in the hold capacitor at the end of track mode. The track and hold mode transistors were sized in order to

have minimum distortion and less acquisition time. The sizes of these transistors are given in Table 1.

3.3 Constraint on the hold capacitor

The value of the hold capacitor is primarily dictated by the kT/C noise requirement [1],[2],[7]. Bigger hold capacitors are efficient as they reduce the droop and feed through. But they limit the bandwidth of the circuit. The increase in the hold capacitor also increases the current modulation at the hold node and increases the distortion. The kT/C requirement provides the following minimum value for the hold capacitor by the given equation (7)

$$kT/C < \Delta^2/12 \ [2]\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \ (7)$$

where Δ is the LSB of an n bit ADC i.e $\Delta = Vref/2^n$.

Based on the requirement for 11 bit ADC, C should be atleast 1.5pF.

The table below gives the values of sizes of all the components in the final circuit schematic Figure 11.

Components	Value
Vdd	3.3
N1,N2	12u/120n
N3,N4,N5,N6	4.8u/120n
Rl,Rd	1.05k Ohm
Ibias1,Ibias2	600u
Rdegeneration	2k Ohm
N7,N10	800u/120nm
N8,N11	10.2u/120nm
N9,N12	8u/120nm
Ch	1.62pF

Table 1. Values of the circuit components presented in the circuit design

In order to reduce the thermal noise contribution of the resistors (the integrated noise across the bandwidth of interest) in the input buffer, the current in the input buffer was increased ten times and the resistor values were scaled and accordingly the load and the dummy resistors were sized to be 100 Ohms and the degeneration resistor about 250 Ohm. Now the SNR (due to thermal noise of resistors) increased from 72 dB to 82 dB. But, this increased the power consumption of the S/H core.

3.4 Implementation of current source in the input and switching buffer

The ideal current sources were implemented as constant gm current sources. A general schematic of the constant gm current source is shown in the Figure 14 below [1]
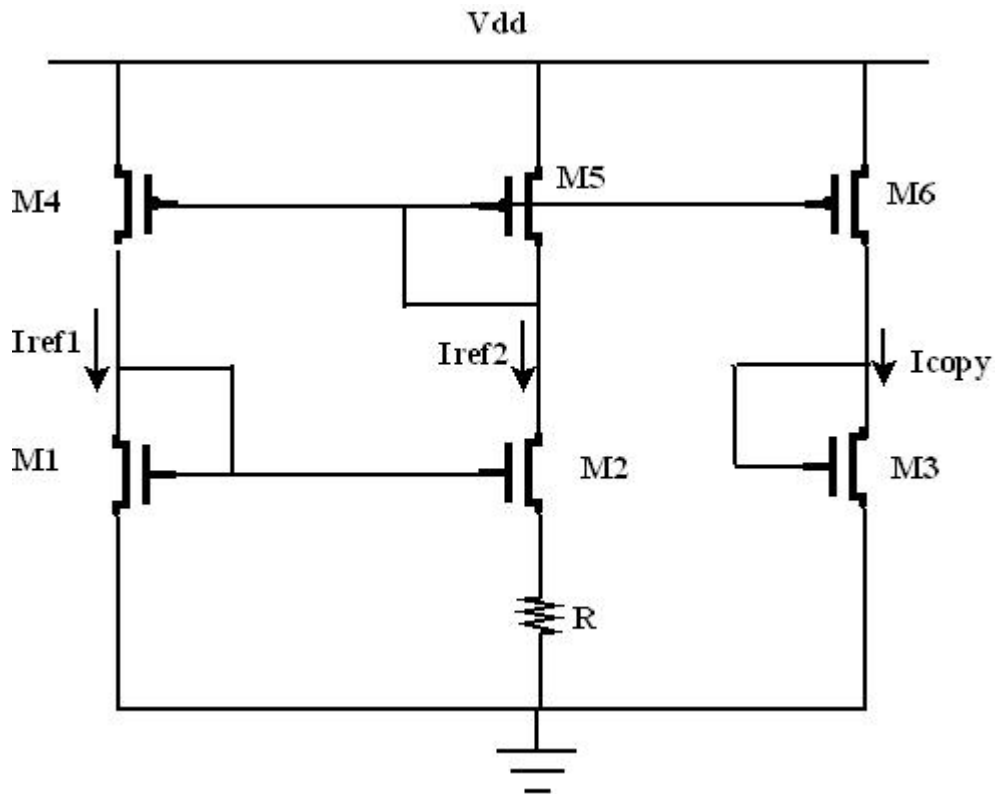
Figure 14. Schematic of a Constant gm current source [1]

This circuit was used to provide a constant current of 600uA and 1.85mA for input buffer and switching buffer respectively. This circuit provides a constant current which is independent of the supply voltage. The op-amp between the two branches reduces the V_{ds} mismatch, leading to lesser mismatch between the current branches I $_{ref1}$ and I$_{ref2}$. The higher the gain of the op-amp the better matching between the transistors.Morever,V_{gs2} should be smaller than V_{gs1} to accommodate for higher W/L with same current in both the branches .The width

of M2 is K times larger than M1 ($\beta_2 = K\beta_1$) and $L1 = L2$ so that gate source

voltage of M1 is greater than M2. Neglecting mismatch and λ effects, the current

mirror M4, M5 provides $I_{ref1} = I_{ref2}$. Equations (8)-(12) derive the expression for

transconductance (gm) in constant gm current source.

$$Vgs1 = Vgs2 + IR \quad\text{..}\quad (8)$$

$$\sqrt{\frac{2I}{\beta_1}} + V_{Thn} = \sqrt{\frac{2I}{\beta_2}} + V_{Thn} + IR \quad\text{.......................................}\quad (9)$$

$$Iref = \frac{2}{R^2\beta_1}\left(1 - \sqrt{\frac{1}{K}}\right)^2 \quad\text{...}\quad (10)$$

$$gm = \sqrt{2\beta Iref} \quad\text{..}\quad (11)$$

Substiting for I_{ref},

$$gm \approx \frac{1}{R} \quad\text{..}\quad (12)$$

This result is independent of MOSFET parameters (such as μ and V_{TH}) and

supply voltage. The variation in gm over temperature, however, is directly

affected by the temperature co-efficient of R.

4. SIMULATION AND RESULTS

The simulation results of the THA circuit are presented in this chapter. The results include the output swing, SFDR, THD, SFDR with respect to input frequency and, SFDR with respect to temperature, etc..This chapter also gives a brief overview of the importance of coherent sampling. Finally the chapter ends with a table containing all the figures of merit for the S/H circuit.

According to the Nyquist sampling theorem, the sampling frequency should atleast twice the highest frequency of the input signal. In order to meet this criteria, for a sampling frequency of 500MHz, the highest input frequency is 250MHz. Figure 15 below is the transient output of the S/H circuit with an input frequency of 244.1MHz and sampling frequency of 500MHz. Figure 16 shows that the output dynamic range of S/H circuit is 1V. Figure 17 shows closer transient output with the clock signal with maximum acquisition time which is 233.8ps.
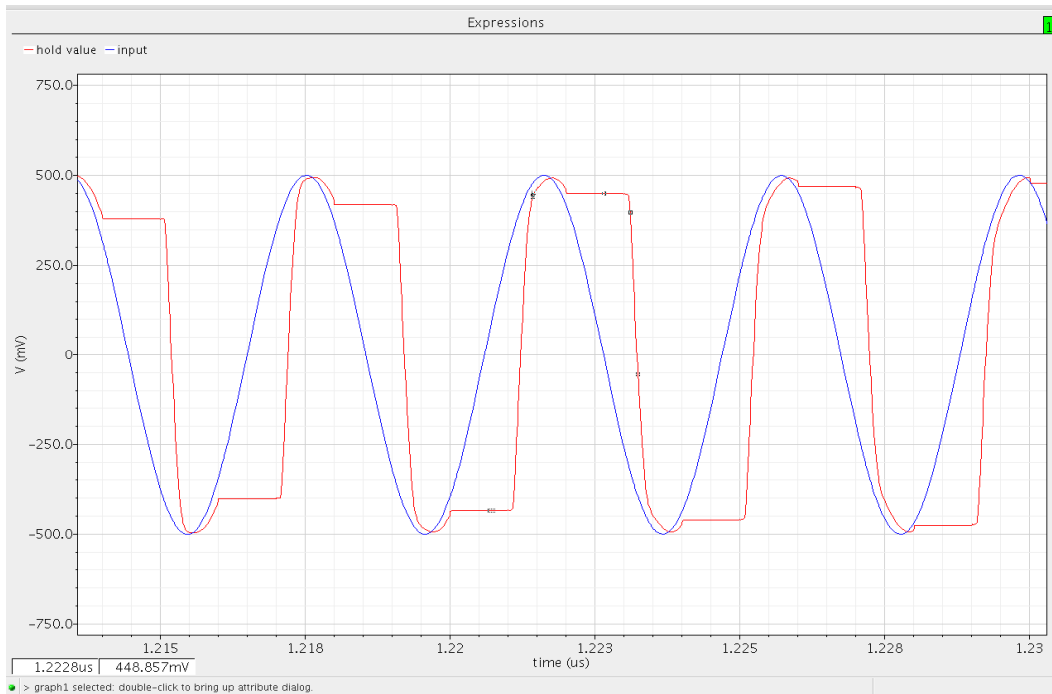
Figure 15. Output of the Track and Hold Circuit.
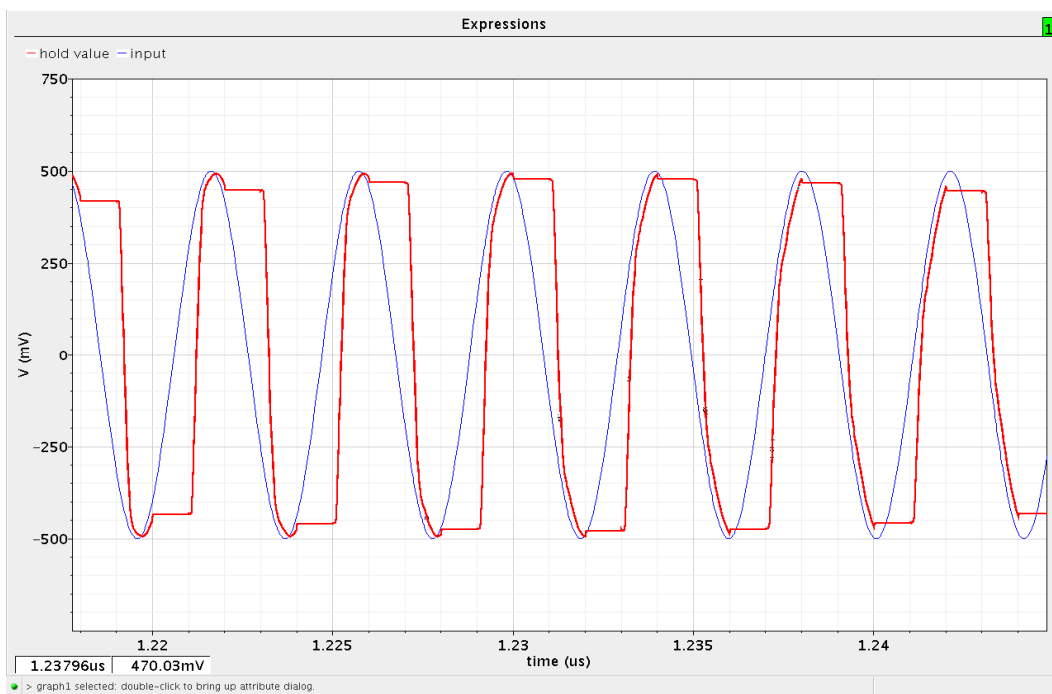
Figure 16. Output showing the total voltage swing of 1V
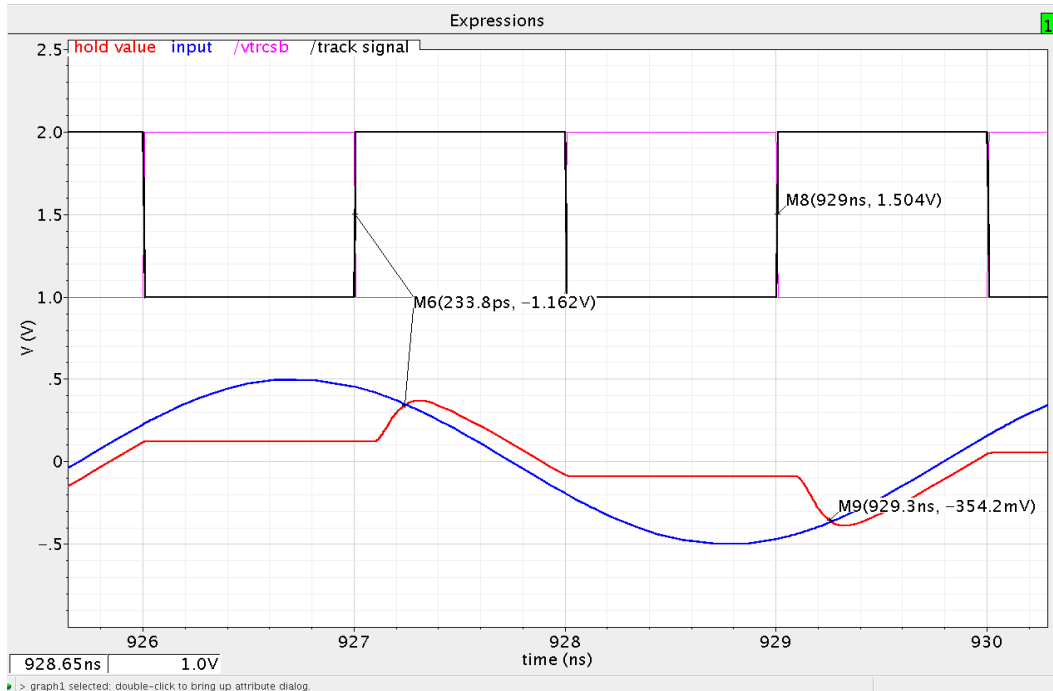
Figure 17. The output of THA showing the maximum acquisition time

4.1 Importance of Coherent Sampling and cause of spectral leakage

In order to measure the spurious free dynamic range or total harmonic distortion (THD), the transient signal has to be converted to its frequency domain counterpart. This can be done with a discrete Fourier transform or fast Fourier transform (FFT).FFT is a very useful tool to investigate the performance of S/H circuits and data converters.

Coherent sampling refers to the relation between the input frequency (fin), sampling frequency (fs), number of cycles in the sampled set (N) and the number of samples(M) which is generally chosen to be an integer with a power of two. The higher the value of M, higher the resolution of the FFT. Equation (13) gives coherent sampling condition.

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$$fin/fs=N/M\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(13)$$

where it is necessary for N to be an integer.

Due to the fact that only take finite number of samples of the time domain signal is taken, a window, generally is used to capture or rather take a snapshot of the time domain signal. If this window covers the signal in such a way that the complete cycle is not included within, then this causes discontinuity with the next sample leading to spectral leakage. Figure 18 shows the time domain and frequency spectrum of signal sampled non-coherently. Figure 19 shows an FFT of a signal sampled coherently. So, a clear distinction is seen between the case where there is no spectral leakage and one where there is spectral leakage.

Spectral leakage can be reduced following the coherent sampling formula and also by using a window with better frequency response. A window is a mathematical function which has a zero value outside a certain interval. There are various types of window functions depending on the characteristics of their main and side lobes and their application [18]. A rectangular window has high side lobes but a Hann window has moderate side lobes. It is known that the Hann window has a good frequency response as compared to rectangular window[18].
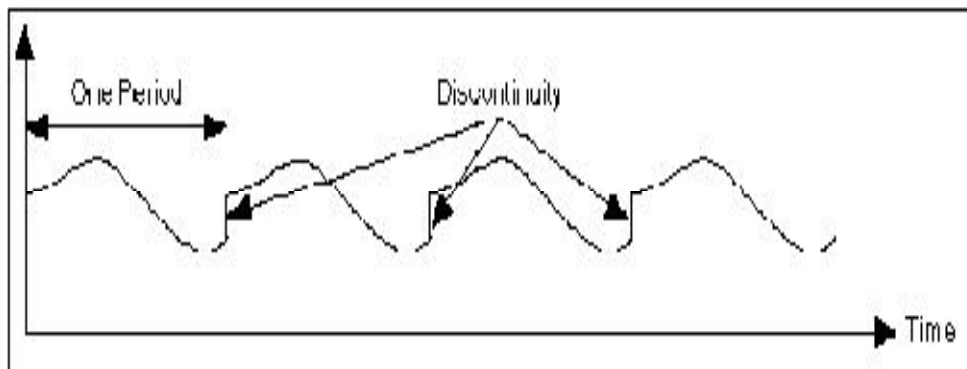
Figure 18. Time domain illustration of the signal when coherent sampling constraint is not followed [20]

dB20(abs(dft(wave_14() 1.75e-08 1.042e-06 1024 "Rectangular" 1 "default")))

244.02MHz   -9.115dB

> graph3 selected: double-click to bring up attribute dialog.
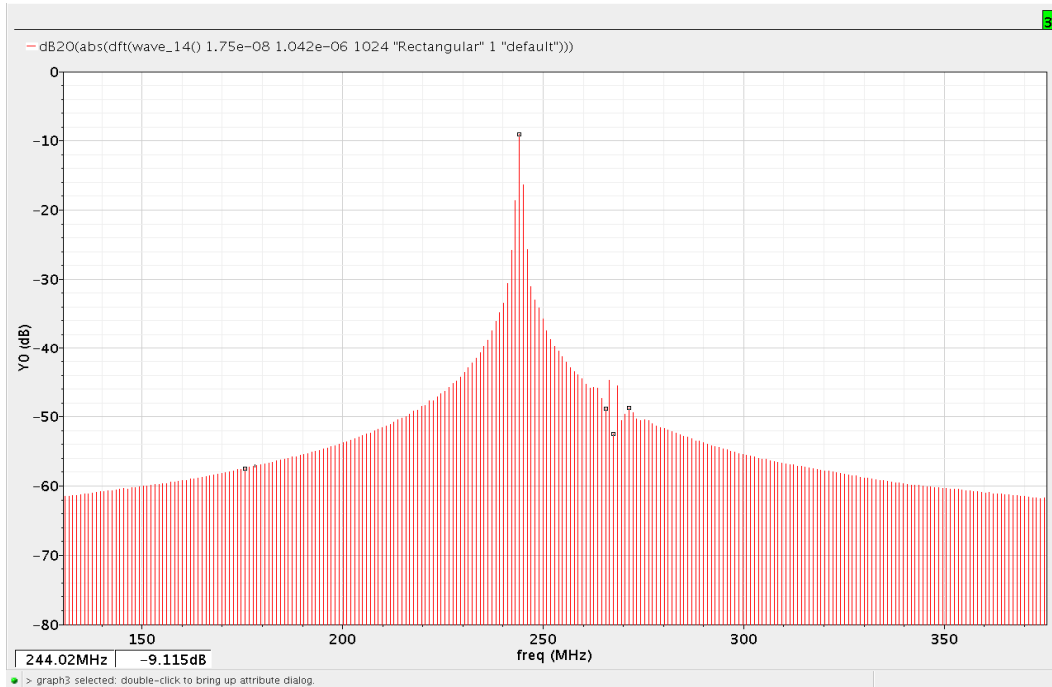
Figure 19. Spectral leakage when coherent sampling was not followed

4.2 Spurious Free Dynamic Range (SFDR)

This is one of the important measure of the fidelity of circuits in data conversion. By definition, SFDR is measure of strength of the fundamental signal to the highest spur in the output .This is used as an indicator of the amount of non-linearity present in the circuit. Therefore, SFDR signifies the lowest energy input signal level that can be distinguished from the signals that are spurious. From the definition of SFDR, any signal below the SFDR cannot be identified as a pure signal instead of a spurious one. As the spurious signal can mask the desired ones, this is very important figure of merit.

In the Figure 20, the input frequency is selected 244.1MHz in order to make sure coherent sampling constraint is satisfied with a sampling frequency of 500MHzaccording to equation(13). The FFT of the transient signal is generally between 0 to fs/2. The even order harmonics are not present in the FFT because we are using a fully differential THA. However, the third order harmonic (3*input frequency) for example would be at 732.4MHz.As the FFT gives only fs/2 frequency, the higher harmonics are aliased back into this band. The higher harmonics aliased back within fs/2 can be found by the formula |nfs$\pm$ kfn| where n is an integer and k is the harmonic. So, the third harmonic would be aliased back at |500M$\pm$3*244.1M| which would be at 232.4MHz. Similarly, the fifth harmonic is aliased back at |2*500M$\pm$5*244.1M|=220.7MHz. As the third harmonic is highest spur in the FFT between 0 to fs/2, SFDR in this case is the power in dB in the fundamental tone at 244.1MHz minus the power in dB in the third harmonic. Hence the SFDR is 78.49dB.

— dB20(abs(dft(wave_58() 1.7e-08 2.065e-06 1024 "Rectangular" 1 "default")))

M0(11.72MHz, 78.49dB)

130.37MHz | -99.782dB
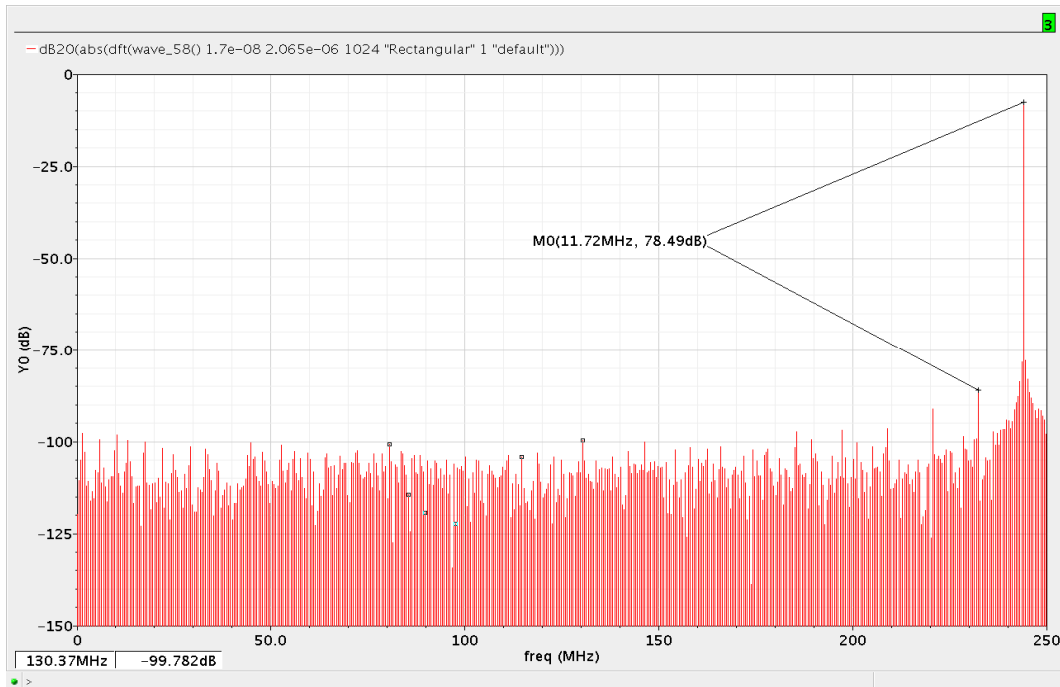
Figure 20. SFDR of the THA

4.3 Total Harmonic Distortion (THD)

Ideally, an amplifier has to provide the same gain irrespective of the input given. In other words, the gain of the amplifier should not be dependent on the input. But, large signal analysis of single and differential amplifiers circuits exhibit a nonlinear gain[1],[2]. In a differential pair, the output variation heavily nonlinear as the input level increases. The input and output characteristic of an amplifier can be approximated in the equation (14) as

$$y(t) = \alpha_1 x^1(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + ...$$ …………………….. (14)

The non linearity of a circuit can also be characterized by applying a sinusoid at the input and monitoring the output. If $y(t) = A\cos\omega t$

$$y(t) = \alpha_1 A\cos\omega t + \alpha_2 A\cos\omega t + \alpha_3 A\cos\omega t + ...$$ …………….. (15)

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$$y(t) = \alpha_1 A \cos \omega t + \frac{\alpha_2 A^2}{2}.[1 + \cos(2\omega t)] + \frac{\alpha_3 A^3}{4}[3 \cos \omega t + \cos(3\omega t)\}] + \dots \dots \quad (16)$$

From the equation (16), it can be observed that higher order terms yield higher harmonics. The even and odd order terms result in even and odd harmonics, respectively. The magnitude of the nth harmonic grows in proportion to the nth power of the input amplitude. This effect is quantified by adding the power of all the harmonics except the fundamental tone and normalizing the sum to the power of the fundamental as written in equation (17).This metric is termed as Total Harmonic Distortion. This undesirable in most signal processing systems including data converters and S/H circuits.

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots V_{\infty}^2}}{V_1} \quad \dots\dots\dots\dots\dots\dots\dots (17)$$

In S/H circuits, the input buffer and output buffer which are unity gain amplifiers contribute to non-linearity or distortion. The switches or the switching buffers add to distortion in the hold mode due to feed through and the hold pedestal problem. In the track and hold circuit, the linearity of input and output buffer is increased with the addition of degeneration resistors. As the design is fully differential, there is no contribution to non-linearity from the even order terms [1].From the Figure20, it can be seen that the THD for a up to fs/2 is < -74dB.Apart from the fundamental tone, among the higher order harmonics aliased back , third, fifth and seventh harmonics have significant power which contribute to the THD. The power of ninth and higher terms are neglected as they do not have significant power.

4.4 The effect of Temperature on SFDR

Temperature affects various device characteristics in BJTs thereby varying the performance of circuits. Mobility degrades with the increase in temperature. Initially between -20 degrees to 40 degrees there is an increase in SFDR and after 40 degrees, SFDR decreases drastically. Typically, the base transport in BJTs reduces with temperature, primarily because the mobility and recombination lifetime are reduced with increasing temperature. Occasionally the transport factor initially increases with temperature, but then reduces again [19].As the base transport factor decreases, the speed of the transistors reduce and hence SFDR decreases with increase in temperature. Figure 21 shows the behavior of SFDR with respect to temperature.
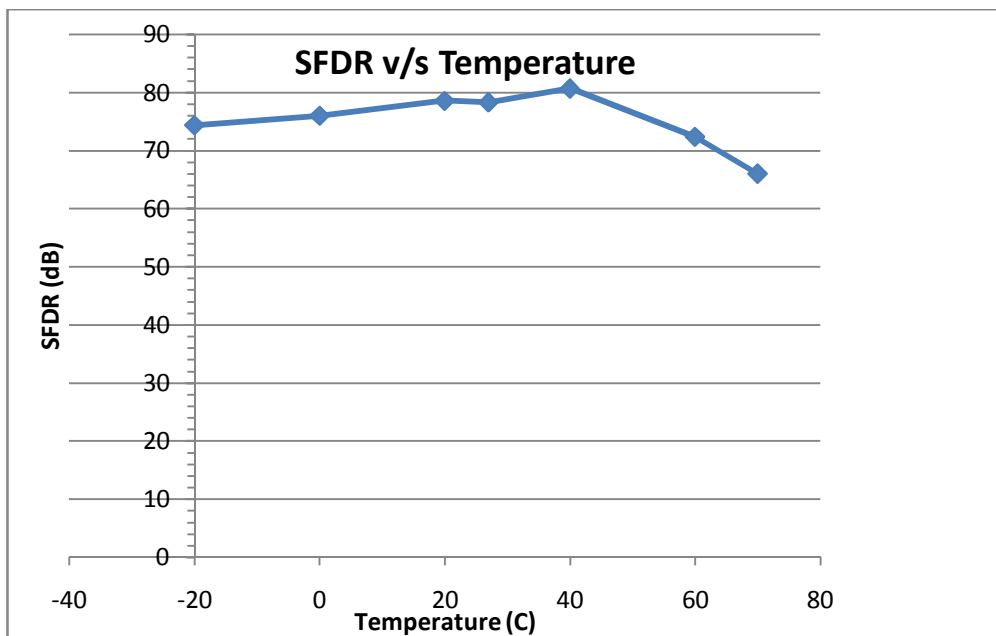

Figure 21. SFDR v/s Temperature

The temperature was varied from -20°C to 70°C, SFDR varied from 70 to 82dB.The FFT of the transient output of the THA was simulated on all process corners. The THA works on all process corners for a voltage supply change of $\pm5\%$ and temperature range of $-20\,^{o}$C to 70°C.

4.5 The effect of sampling frequency on SFDR

With the increase in sampling frequency, the behavior of the circuit degrades due to the non-idealities present. The clock feed through poses a constraint on the sampling frequency at which the circuit can operate. Higher frequency operation requires smaller hold capacitors as bigger capacitors restrict the bandwidth of the circuit. But, the noise requirement on the hold capacitor poses a constraint on the minimum value of the hold capacitor. So, this limits the operating frequency of the circuit. These problems and non-idealities lead to hold mode distortions degrading the SFDR and THD of the circuit. Using smaller hold capacitors also lead to leakage and droop problems at high frequencies hence the resolution of the Sample and Hold circuits and A/D converters decrease at high frequencies. Figure 22 shows the behavior of SFDR with change in sampling frequency.
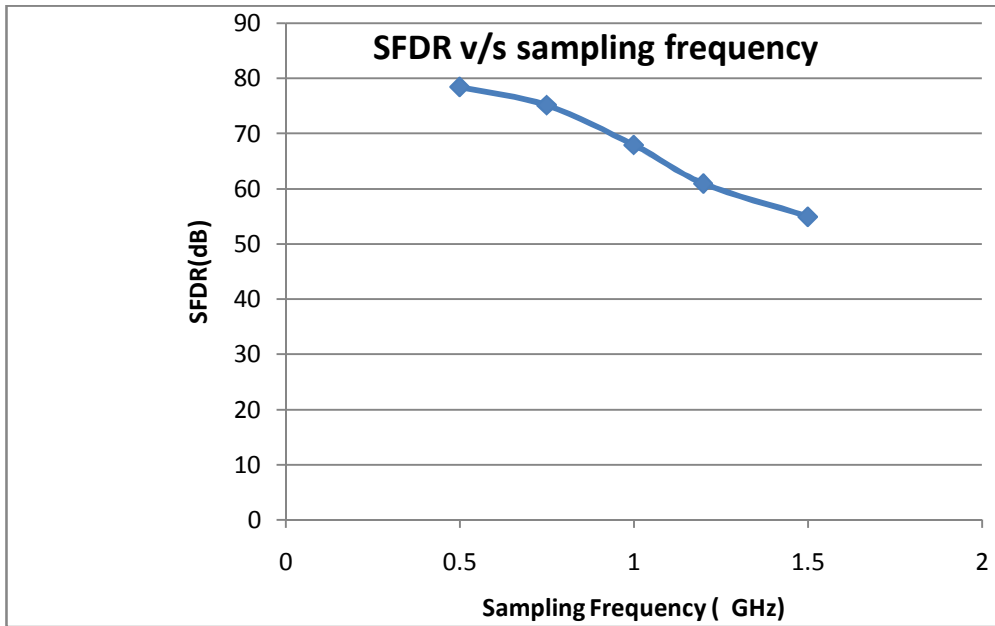
Figure 22 .SFDR v/s sampling frequency

As the sampling frequency increases from 0.5GHz to 1.5GHz, the SFDR comes down from 78.49 dB to 55dB.

The performance parameters of the current THA has been summarized in Table 2 below.

Technology	130nm
Power Consumption	50mW
Vdd	3.3V
Dynamic Range	1Vpp
SFDR	78.49dB
THD	<-74dB
Acquisition time	233ps
Droop rate	243n/838.4ps
Hold Settling Time	9.356ps

Table 2. Summary of the performance of current THA

5. CONCLUSION

This chapter gives an overview of what was achieved from the techniques in the new bipolar SiGe THA topology. This chapter also gives a comparison of the performance of the current THA with other works.

	Current design	[7]	[8]	[9]
Frequency of Operation	500Msps	1G	1G	500Msps
Acquisition time	335ps	400ps	---	----
Analog Input	1Vpp	400mVpp	1Vpp	----
SFDR	78.49dB	62dB	62dB	62dB
THD	<-74dB	< -60dB	<-62dB	<-62dB
Supply Voltage	3.3V	3.3V	5.2V	1.8V
Power Consumption of THA core	50mW	350mW	75mW	15mW*

Table 3. Comparison of the current work with other Bipolar THAs

*without the inclusion of power consumption by the current sources

This THA works for a maximum sampling frequency of 500 MHz and input frequency of 250 MHz according to Nyquist rate criterion. An output dynamic range of 1Vpp has been achieved for a supply voltage of 3.3 V. The maximum acquisition time for this THA is 233ps which is lesser than 400ps as stated in [7]. The main reason for lesser acquisition time is the use of SiGe HBTs which are faster than normal BJTs. The maximum droop rate is 243 nV/838.3 ps which is considerably less.

The current bipolar design combines the output steering technique from [8] and the emitter follower switch from [7],[9].From the Table 3,it can be clearly concluded that the SFDR and THD is higher than other THAs. The use of cascode transistors and dummy loads provide better hold mode isolation which leads high SFDR without any complex circuitry. The power consumption is 50mW including the power consumption of the constant current sources excluding the output buffer. The power consumption in [8] is clearly higher than the THA presented in this Thesis. The reason could be the use of auxiliary buffer. The power consumption given in [9] is 15mW. However, the power consumed by the current sources has not been included. If the contribution from the constant current sources is included to the power, this will be more than 50 mW. It can be concluded that the output steering technique along with the cascode transistors and emitter follower switching buffer prove to provide efficient hold mode isolation and reduce signal feed through with lesser power consumption.

The current work can be extended to higher frequencies. Operation at higher frequencies poses a challenge because the signal feed through and other non-idealities increase which would degrade the SFDR and THD. This can be overcome by adding compensation circuit to provide better hold mode isolation between the hold node and input. Addition of these compensation circuits would increase the power consumption. Hence, techniques to improve the SFDR which do not power consumption have to be developed.

REFERENCES

1. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2000.

2. Jacob Baker,CMOS Circuit Design, Layout and Simulation, IEEE *Press Series*

3. Sanchez, "Track and Hold: Architectures & Circuits", Analog and mixed Signal Center, TAMU

4. Texas Instruments, "Application Note 775 Specifications and Architectures of Sample and Hold Amplifiers", Rev No 3, 1998.

5. Weize Xu and Eby G. Friedman, "Clock Feedthrough in CMOS Analog Transmission Gate Switches", IEEE, 2002

6. R. Gabl, K. Aufinger, J. Böck, and T. F. Meister "Low-frequency Noise characteristics of Advanced Si and SiGe Bipolar Transistors",Germany.

7. Thorsten Baumheinrich, and Bernd Pregardier, "A 1-G Sample/s 10-b Nyquist Silicon Bipolar Track & Hold IC", IEEE *Journal of Solid State Circuits*,Vol. 32,No.12,December 1997

8. Hüseyin Dinç and Phillip E. Allen, "A 1.2 GSample/s Double-Switching CMOS THA with -62dB THD',IEEE *Journal of Solid State Circuits*,Vol. 44, No.3, March 2009

9. Pieter Harpe, Aton Zanikopoulos, Han Hegt, "A 62dB SFDR, 500MSPs, 15mW Open-Loop Track and Hold Circuit", IEEE *NOR chip* 2006

10. Jonathan C. Jensen, Lawrece E.Larsen, "An 8bit 3 GHz Si/SiGe HBT Sample and Hold", IEEE 2004

11. Haider S. Osmany.S.A, Gustat.H, Heinemann.B , " A 10GSamples/s 2V/sub pp/ emitter follower only track and hold amplifier in SiGe BiCMOS technology" ISCAS 2006

13. Borokhevych Y, Scheytt.J.C "10 GS/s 8-bit THA in SiGe technology",IEEE 2011

14. Christopher V. Griffith, Kosta Horaites, Joel Leja , "Spectral Leakage and Signal Sideband Mixers", April 2009

15. Sugawa N, Ikarashi T, Kuwana K, Kawakami T, Kimitsuka A, Iida T , " CMOS low distortion sample and hold circuit for audio D/A converter",

IEEE, May 1989

16. Gatti.U, Maloberti.F, Palmisano.G " An accurate CMOS Sample and Hold Circuit", ISSCC, Jan 1992

17. Harpe P, Zanikpoulos A, Hegt H, Van Roermund A., " A 62dB SFDR, 500MSPs, 15mW Open-Loop Track and Hold Circuit", Nov 2006

18. "Windowing:Optimizing FFTs using window functions",National Instruments, Dec6, 2011

19. B Van Zeghbroeck, "Principles of Semiconductor Devices",University of Colorado, Boulder, 2011

20. National Instruments, "Tutorial-Spectral Leakage", September 6, 2006

APPENDIX A

THA MEASUREMENT SETUP

A . THA MEASUREMENT SET UP

The hold voltage of the THA is very inportant as this is voltage which is processed further in A/D converters. Inorder to check the accuracy of the hold mode volatage ins a Track and Hold circuit generally two sample and hold circuits are casecaded and operated with different clocks.The idea behind this is the beat frequencies obtained by different clocks of the two sample and hold circuits. The beat frequencies obtained by the different clock signals of the two sample and hold amplifiers are used in this case.If f_{s1}/n is applied as input to the first S/H with n=2,3,4,5…, a beat frequency occurs when the second sample and hold circuit is clocked with a sampleing ferquency of f_{s1}/n.The sub-sampling gives smaller change in steps between the successive samples.The acquisition accuracy of the second circuit is increased .The final waveform can be analysed and information about the hold mode performance of the first sample and hold circuit can be determined without an A/D converter. One sine wave generator is used to generate input for the first sample and hold circuit at beat frequency. Another sine wave gerator is used which goes to a clock buffer which provides the clock signal for the first S/H circuit. Each Track and hold circuit has its own bandgap references and clock buffers.