A CMOS Sigma-Delta Digital Intermediate Frequency to Radio Frequency Transmitter

by

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ABSTRACT

During the last decades the development of the transistor and its continuous down-scaling allowed the appearance of cost effective wireless communication systems. New generation wideband wireless mobile systems demand high linearity, low power consumption and the low cost devices. Traditional RF systems are mainly analog-based circuitry. Contrary to digital circuits, the technology scaling results in reduction on the maximum voltage swing which makes RF design very challenging. Pushing the interface between the digital and analog boundary of the RF systems closer to the antenna becomes an attractive trend for modern RF devices. In order to take full advantages of the deep submicron CMOS technologies and digital signal processing (DSP), there is a strong trend towards the development of digital transmitter where the RF up-conversion is part of the digital-to-analog conversion (DAC). This thesis presents a new digital intermediate frequency (IF) to RF transmitter for 2GHz wideband code division multiple access (W-CDMA). The proposed transmitter integrates a 3-level digital IF current-steering cell, an up-conversion mixer with a tuned load and an RF variable gain amplifier (RF VGA) with an embedded finite impulse response (FIR) reconstruction filter in the up-conversion path. A 4th-order 1.5-bit IF bandpass sigma delta modulator (BP ∑ΔM) is designed to support in-band SNR while the out-of-band quantization noise due to the noise shaping is suppressed by the embedded reconstruction filter to meet spectrum emission mask and ACPR requirements. The RF VGA provides 50dB power scaling in 10-dB

steps with less than 1dB gain error. The design is fabricated in a 0.18μm CMOS technology with a total core area of 0.8 x 1.6 mm^2. The IC delivers 0dBm output power at 2GHz and it draws approximately 120mA from a 1.8V DC supply at the maximum output power. The measurement results proved that a digital-intensive digital IF to RF converter architecture can be successfully employed for W-CDMA transmitter application.

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CHAPTER 1

INTRODUCTION

1.1 Motivation and application

With the increasing demand for high linearity, power efficient and wide-bandwidth mobile devices, RF systems will benefit from moving the interface between the digital to analog domains closer to the antenna. Furthermore, in order to take advantages of the deep submicron CMOS technologies and digital signal processing (DSP), there is a strong trend towards the development of digital heterodyne architectures where the digital baseband signal is up-converted to intermediate frequency (IF) in the digital region, and RF up-conversion is part of the digital-to-analog conversion (DAC).

The digital to RF up-conversion methods included current- steering DAC cells [2-4], multi-bit ΣΔ noise shaped IF [2], and the inherently linear single-bit RFDACs [3]. The digital heterodyne transmitter has the advantages of higher integration level and power efficiency, improved I/Q matching and EVM performance, and adaptive modulation of the transmitted signal bandwidth without the need of external IF SAW filter [1]. In addition, the problems associated with conventional homodyne transmitters including DC-offset and LO leakage, are greatly reduced because there is no analog gain stage in the baseband. The RF DAC presented in [2] shows better signal-to-noise ratio (SNR), lower power consumption and reduced hardware complexity compared to the conventional DAC-Mixer architecture. In this architecture, higher SNR is achieved by using multi-bit (8-level) ΣΔM with high sampling frequency of

514MHz. However, the multi-bit DAC could require additional mismatch reduction techniques, such as dynamic element matching, which could increase the system complexity and power consumption. The architecture of RFDAC presented in [3] offers advantages in terms of high integration due to digital-intensive design and higher linearity. The impact of flicker noise up-conversion due to the DAC's current sources is reduced by alternating the operation point of the rail device from accumulation to inversion. Also jitter masking technique is employed to minimize IF jitter impact, which ensures that the current source is off during the DAC bit switching transition. However, the design shows some limitations, which make it hard to be used in the wideband transmitter applications. One limitation is inadequate filtering of the out-of-band quantization noise. In most wireless standards high adjacent channel power suppression and strict spectral emission requirements are enforced. In order to meet the spectrum emission mask and ACPR requirements, a more complex FIR filter is required to suppress the out-of-band quantization noise. Another limitation is the use of single-ended local oscillator (LO) that drives the gate of the rail device, which leads to higher LO leakage compared to that of the conventional Gilbert-cell mixer.

This objective of this work is to research a digital IF to RF transmitter (DRFTx) architecture which can be utilized in the wide-band transmitter applications with high linearity, circuit simplicity and low power consumption. The DRFTx architecture presented in this thesis is a digital heterodyne transmitter which utilizing a 3-level digital IF to RF DAC up-converter, followed by a RF

variable gain amplifier with an embedded band-pass reconstruction filter to take the advantages of RFDAC [3] while overcome its limitations so that the idea of RFDAC presented in [3] can be successfully extended to the real world W-CDMA transmitter application.

1.2 Outline of the thesis

This thesis consists of eight chapters with the introduction as the first one. Chapter 2 presents the surveys of the transmitter architectures including the conventional super-heterodyne, homodyne, and the recent digital heterodyne architecture, followed by the proposed the digital IF transmitter architecture. Chapter 3 analyzes the system requirements of the proposed architecture which provides the baseline requirements on the design of the reconstruction FIR filter, RFDAC and RF VGA. Chapter 4 shows the circuit level implementation of the major building blocks of the proposed architecture including RFDAC with embedded FIR reconstruction filter and Chapter 5 demonstrates the design of discrete-power-step RF VGA. Chapter 6 illustrates the measurement results which demonstrate that the proposed architecture is feasible for W-CDMA transmitter application. Chapter 7 presents the potential extended applications, and the conclusions are drawn in Chapter 8.

CHAPTER 2

TRANSMITTER ARCHITECTURES

The objective a radio transmitter is to up-convert the baseband signal and amplify it to the desired power level before delivering it to the transmit antenna. For a transmitter that is designed for wide-band mobile or wireless communication systems, especially for W-CDMA transmitter, high dynamic range, high linearity, low power consumption and low cost are the most important properties. W-CDMA class III mobile transmitters are targeted for a maximum power of +24dBm and a minimum of -50dBm at the antenna end which leads to a minimum of 74dB dynamic range requirement. In the W-CDMA standard, the transmitter linearity requirement can be transferred to the W-CDMA transmit waveform quality which is specified by the Adjacent Channel Leakage Ratio (ACLR) or Adjacent Channel Power Ratio (ACPR) and the RMS Error Vector Magnitude (EVM). For W-CDMA systems, ACLR is defined as the ratio of the integrated signal power in the adjacent channel to the integrated signal power in the main channel; the standard demands minimum 33dBc and 43dBc at the first channel (5MHz) and the second channel (10MHz) offset respectively [5]. EVM is a measure of how much the deviation of the transmitted constellation construction to the ideal one which is generated at the base band. W-CDMA transmitter specifies RMS EVM to be less than 17.5% at all output power levels greater than 20dBm [5]. The low power consumption property is very crucial for maximizing the battery life time which is an important factor for mobile devices. The low product cost is the most important figure from the end customers point of view,

which is determined by the technology, the integration level and the number of the external components needed to guarantee the transmit waveform quality.

To gain better insight of in the different tradeoffs, first the existing transmitter architectures will be overviewed and discussed, including super-heterodyne and homodyne transmitter architectures. Next, the digital heterodyne transmitter will be highlighted. Finally, the digital-intensive digital intermediate frequency (IF) to RF digital-to-analog (DAC) transmitter topology targeted for W-CDMA application is proposed.

2.1 Overview of transmitter architectures

The choice of transmitter architecture has a significant impact on the operation of the system. In general, there are two types of common transmitter architectures: super-heterodyne and homodyne (zero-IF or direct conversion). Each of these architectures has its own inherent advantages and disadvantages. However, many of the potential issues of the individual architecture can be solved with smart topology and / or circuit design techniques.

2.1.1 Super-heterodyne transmitter architecture

For W-CDMA transmitters, super-heterodyne architecture has been around for many decades, and still the most common architecture reported today [6]–[11]. Figure 2.1 demonstrates the traditional super-heterodyne transmitter architecture.

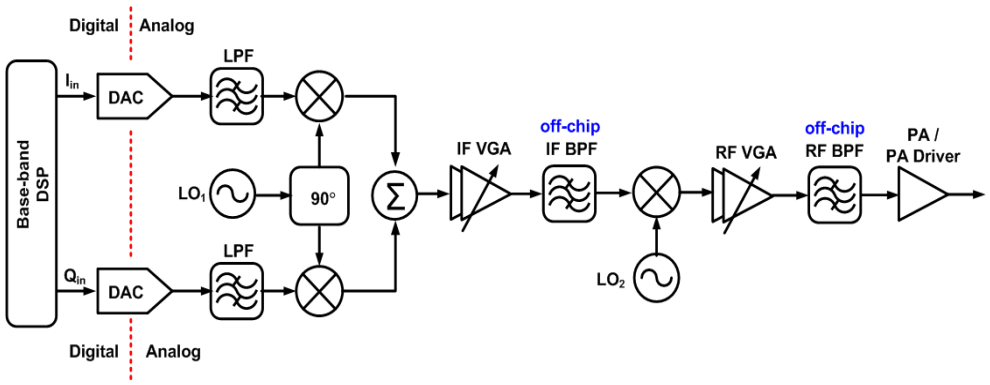


Figure 2.1: Traditional super-heterodyne transmitter architecture

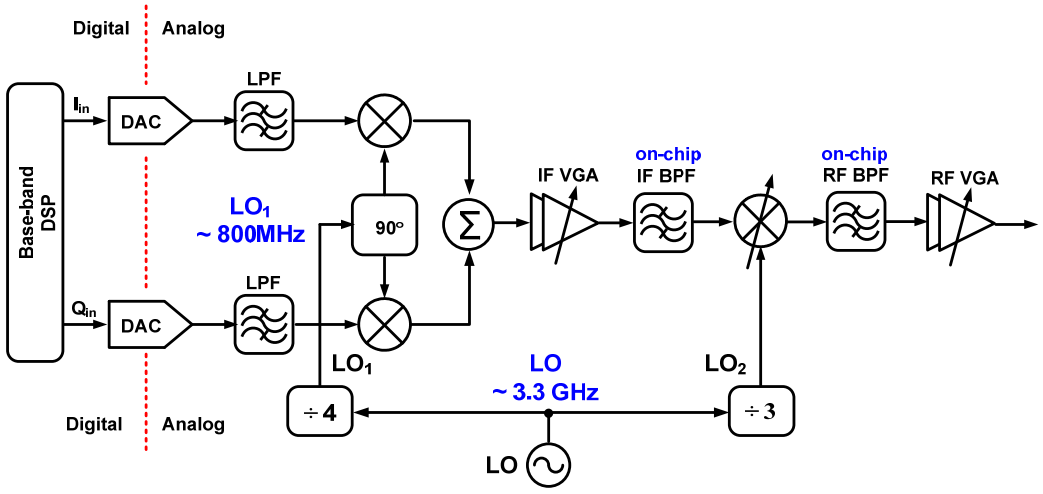
In the baseband, the in-phase and quadrature-phase (I/Q) digital bit streams are converted to the analog signals through the baseband digital-to-analog converter (DAC). After proper low-pass filtering to reject any high frequency aliasing generated during the digital-to-analog conversion process, the signals are mixed with the first local oscillator (LO) signal and up-converted to intermediate frequency (IF) and combined to generate single-sideband IF signal. Typically the combined IF signal will experience some gain variation stage and the band-pass filtering stage to reduce spurs and further reject any aliasing residues from the DAC, and then mix with the $2^{nd.}$ LO and up-converted to the radio frequency through RF mixer. Finally, the up-converted signal is sent to the RF variable gain amplifier (VGA) followed by RF band-pass filtering and then delivered to the power amplifier (PA) or PA driver. Since the base-band signal is up-converted to the radio frequency in two steps, the super-heterodyne architecture offers many advantages. First of all, the 74dB power control demanded by W-CDMA standard can easily be distributed to the IF VGA and RF VGA stages to relax the limited

substrate isolation impact on the achievable transmit dynamic range. Moreover, the waveform quality is superior mainly due to the following two reasons: 1) The LO leakage is a minor issue because the LO_1 and LO_2 are far from the transmit band, and their leakages can be suppressed at the IF BPF and RF BPF stages; 2) The quadrature modulation is performed in the intermediate frequency stages which are relative low frequencies. Therefore the transmit coupling between the in-phase and quadrature-phase paths can be minimized, and the superior matching between I/Q paths can be achieved, leading to almost ideal RMS EVM performance.

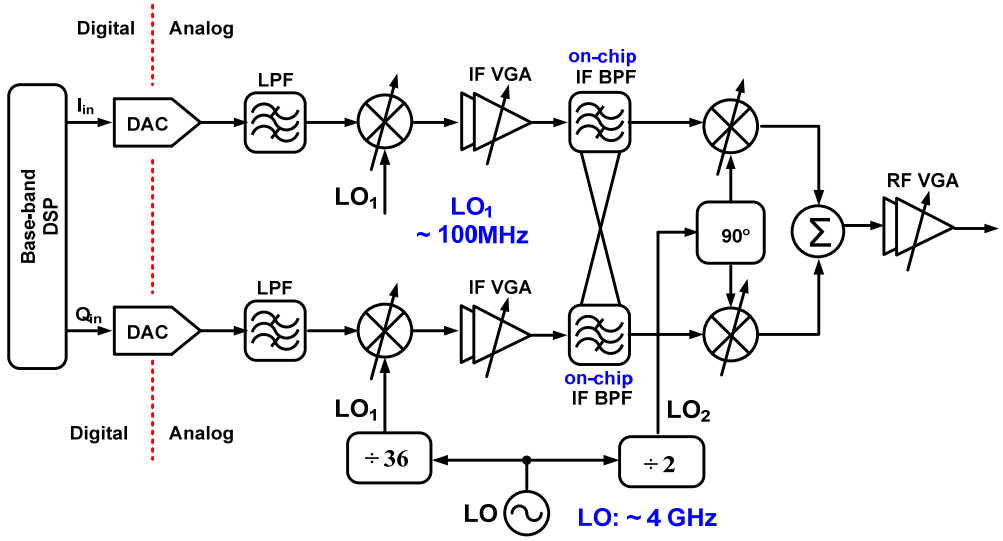
However, the good quality waveform offered by the super-heterodyne architecture does come with some high prices. First, it requires an external IF bandpass filter [6]–[9] and an external RF bandpass filter [12] to reject the unwanted spurs and the sidebands, thus driving the overall chip cost, size and power consumption up. Second, since it utilizes two-step up-conversion, two sets of synthesizes are required, leading to a complicated, area and power inefficient designs. In general, the super-heterodyne transmitter architecture is a bulky, power-hungry and high cost approach.

Recently, there are some works called variable-IF heterodyne architectures [10] [11] with the main efforts to eliminate the bulky and expensive IF BPF and insist one synthesizer as shown in Figure 2.2. Figure 2.2(a) implements the variable IF transmitter using on-chip IF and RF BPFs, while Figure 2.2(b) demonstrates alternative variable IF transmitter approach by adopting on-chip complex-IF filters. Note that none of the variable IF transmitters require an off-

chip IF band- pass filter and only one synthesizer is utilized to generate main LO



(a): Variable IF transmitter architecture with on-chip IF and RF BPF



(b): Variable IF transmitter architecture with on-chip complex-IF BPF

Figure 2.2: Variable IF transmitter architectures

signal. The IF and RF LOs are just the divided-down versions of the main LO. Therefore, the variable IF architecture offers advantages in terms of lower power

consumption and lower cost compared to the traditional super-heterodyne architecture. For the W-CDMA transmit application, since the up-conversion is still implemented in two steps (IF and RF stages), the wide power variation requirement is not an issue for the variable-IF approach. However, the variable IF arhcitectures shown in Figure 2.2 are more sensitive to I/Q mismatches compared to the traditional super-heterodyne architecture because the quadrature modulations are now implemented either at high IF frequency (~ 800M) or at RF (2GHz).

2.1.2 Homodyne transmit architecture

Apart from the two-step up-conversion transmitters described above, homodyne transmitter architectures draw a lot of attenuation these days. Figure 2.3 demonstrates a conventional homodyne transmitter. In this architecture, the baseband digital I and Q bit streams are converted to the analog signals through the baseband DACs. After baseband low-pass aliasing filtering, the filtered signals mix with the only LO and up-converted to the radio frequency, and then the RF I and Q signals are merged and drive PA or PA driver through RF variable gain amplifier and RF band-pass filter.

As shown in Figure 2.3, the homodyne transmitter up-converts the baseband signal to radio frequency in a single step, therefore it completely eliminates the IF band-pass filter and IF synthesizer. As such it offers high integration level, low power consumption and low cost compared to the heterodyne counterpart.

One big issue associated with the traditional homodyne transmitter is that

LO is operating at the exact same frequency as the PA where the strong PA output could couple to the LO and result in the degraded output waveform. This issue is known as LO pulling. One remedy is to offset LO frequency from the operating frequency of the PA as shown in Figure 2.3. By this way, the LO frequency will never overlap the desired transmit band and the LO-pulling issue can be resolved with the cost of increased power consumption due to the higher LO frequency generation.

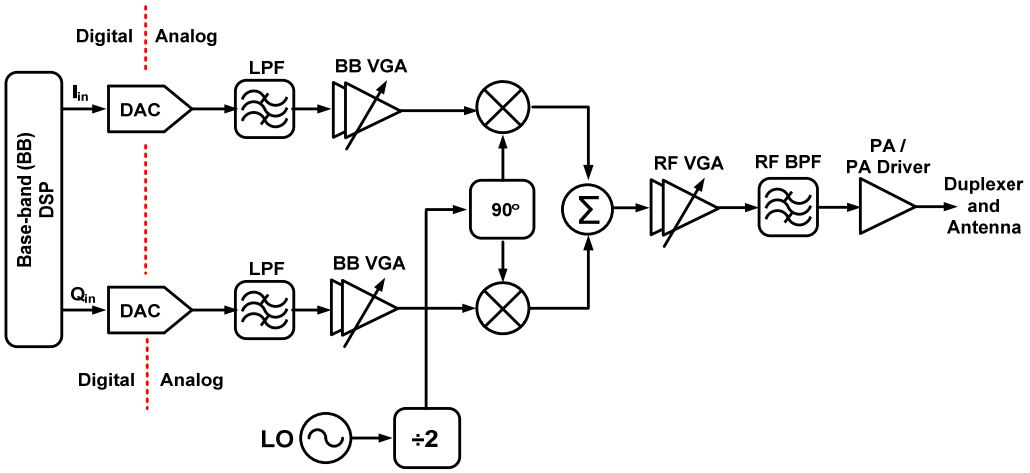


Figure 2.3: Conventional homodyne transmitter architecture

Even though the LO pulling can be removed from the problem list, another issue is hard to be solved. For W-CDMA transmitter application, the 74dB power variation is hard to implement solely at the RF stage due to the limited substrate isolation, thus the baseband variable gain amplification stage is inevitable. Since there is no ac-coupling in the baseband paths, the dc-offset due to the base-band gain variation stays in the up-conversion path and will sit in the transmit band and degrade the output waveform as shown in Figure 2.4.

Moreover, the LO/2 (LO divided down by 2) leakage signal will directly feed through to the output due to the finite substrate isolation and other non-ideality factors, and ultimately degrade the quality of the output waveform as well [13]. In addition, in the homodyne architecture, since the quadrature modulation is implemented at radio frequency, I/Q mismatches are expected to be higher compared to the heterodyne architecture.

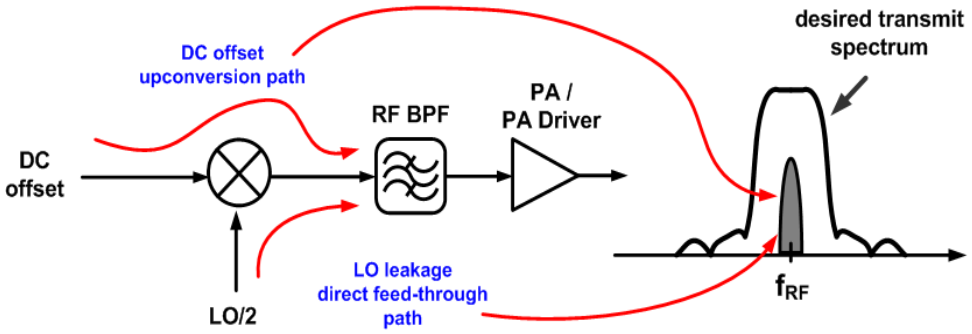


Figure 2.4: Homodyne transmitter architecture issue

2.1.3 Digital heterodyne transmitter architecture

As mentioned before, the homodyne architecture shows the advantage of the circuit simplicity, however, it is not a desired approach to transmit W-CDMA signal due to the performance issues associated with the dc-offset and the LO leakage. Super-heterodyne architectures offer performance benefits in terms of high linearity, high dynamic range and superior waveform, but they consume more power consumption, require more off-chip filters and more chip area which shortens the battery life time and drives the devices cost high, therefore it is not an attractive approach either.

Some recent works propose heterodyne transmitters using digital IF

modulator to remove the IF band-pass filter from the transmitter and keep only one synthesizer in the up-conversion path as shown in Figure 2.5 and Figure 2.6. In these transmitter systems, the first up-conversion is implemented the digital domain, hence the digital heterodyne transmitter.

In Figure 2.5, the base-band digital data (running at the chip rate of 3.84MHz) are first upsampled and interpolated, filtered by the following low-pass filter, multiplied with the first quadrature LOs, and then the IF in-phase and quadrature signals are summed together to generate the single-ended IF signal before reaching the DAC. In general, implementing digital modulator requires numerical oscillators (for example, direct digital synthesizer) and multipliers,

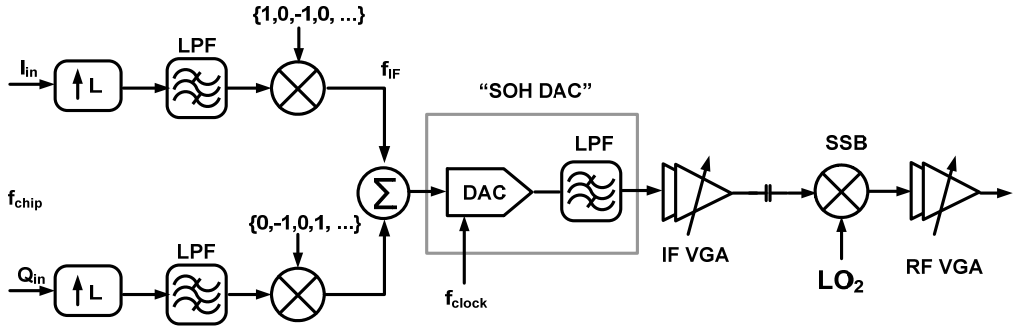


Figure 2.5: Digital heterodyne transmitter architecture proposed in [1]

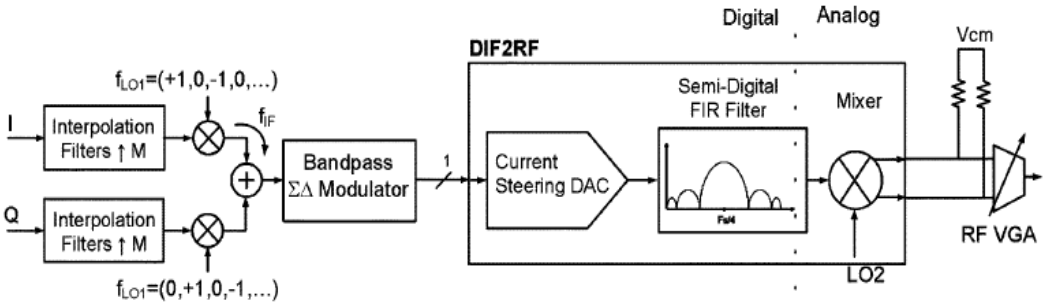


Figure 2.6: Digital IF to RF DAC transmitter architecture proposed in [14]

which could be complicated and power hungry. However, the work in [10] chooses the IF frequency (f_{IF}) to be a quarter of the DAC clock update rate (f_{clk}), thus the IF LO signals become a bit stream sequence representing values of +1, 0, or -1. Therefore, the IF digital modulation is just a simple sign-bit-flipping logic, which considerably eases the circuit complexity and reduces the power consumption.

Since the quadrature up-conversion is implemented completely in the digital domain, the perfect matching between the in-phase and quadrature-phase paths can be obtained, hence the superior EVM performance. The transmitter shown in Figure 2.6 also adopts the similar idea of digital IF modulation, therefore the excellent waveform quality can be expected as well.

The differences between the two transmitters in Figure 2.5 and Figure 2.6 are mainly demonstrated in the second up-conversion phase. Multi-bit DAC followed by a higher-order low-pass filtering method is implemented in Figure 2.5, while the single-bit DAC with embedded semi-digital reconstruction band-pass filtering topology is employed in Figure 2.6. As shown in Figure 2.5, the single-ended digital IF signal is sent to the 8-bit DAC with the clock update rate of 253.44MHz to guarantee the in-band signal-to-noise ratio (SNR), and the second-order-hold DAC attenuates the spurs and rejects the clock images to meet the W-CDMA spurious emission requirements. Since there are two variable amplifiers both in the IF and RF stages, the 74dB dynamic range demanded by the W-CDMA transmitter can easily be achieved, while the dc offset due to IF gain variation can be removed by the ac-coupling capacitor before the second up-

conversion. However, the multi-bit DAC usually requires additional matching schemes, such as dynamic element matching, to maintain good linearity. Moreover, the aggressive attenuation offered by the second-order-hold DAC could distort the in-band signal, thus the digital correction is needed to recover the transmitting waveform. The additional matching scheme and the digital correction increase the system complexity and drive the ultimate chip area and power consumption up. Different from the multi-DAC approach in [1], the digital transmitter in [14] utilize the single-bit DAC to take advantage of its inherent linearity, no matching for DAC linearity is required. A single-bit 4^{th}-order band-pass sigma-delta modulator (BP SDM) is used to generate 1-bit IF bit streams with high in-band SNR, while the out-of-band quantization noise due to the noise-shaping is suppressed by the embedded linear-phase finite impulse filter (FIR) in the second up-conversion. Thanks to the single-bit digital-to-analog conversion, the digital IF to analog RF conversion and the following reconstruction filtering are successfully merged into a single circuit block, leading to a more compact and digital-intensive transmitter design as shown in Figure 2.6. However, the transmitter in [14] shows some drawbacks which are hard for wide-band transmitter applications. One limitation is the inadequate filtering of the out-of-band quantization noise. In order to meet the spectrum emission mask and ACPR requirements, a more complex FIR filter is required to suppress the out-of-band quantization noise. Another limitation is the use of single-ended local oscillator (LO) that drives the gate of the rail device, which leads to higher LO leakage compared to that of the conventional Gilbert-cell mixer.

In general, the digital heterodyne transmitter exhibits the circuit simplicity of the homodyne architecture while inherits the superior performance of the super-heterodyne architecture with proper design.

So far, the three transmitter architectures have been overviewed and discussed. Their circuit characteristics, advantages and disadvantages are summarized in Table 2.1

2.2 Proposed digital transmitter architecture

As shown in Table 2.1, the digital heterodyne transmitter surpasses the traditional super-heterodyne and homodyne transmitters in terms of circuit simplicity and good performances. Therefore, it is more suitable for the future generation of wide-band mobile transmit terminals where size, cost and power consumption are the key factors. With the fast development on the CMOS technology, there is a strong trend to push more circuits used to be implemented in the analog region to the digital domain to take advantage of the CMOS technology scaling and the fast-and-flexible digital signal processing (DSP), thus the digital heterodyne transmitter in [14] excels the transmitter in [1] in terms of more intense digital implementation in transmit path and the low-cost CMOS technology used. However, the work in [14] shows some limitations which have already been addressed. In order to extend the idea presented in [14] to the wide-band transmitter applications, a modified digital IF to RFDAC transmitter needs to be developed.

Figure 2.7 demonstrates the proposed digital transmitter architecture

implemented in CMOS technology. It consists of 1.5-bit band-pass ΣΔ Modulator, a wideband digital IF to RF up-conversion DAC followed by a RF VGA with a reconstruction filter embedded in the up-conversion stage. The architecture performs RF up-conversion, mixing the LO signal with 3-level digital IF bit streams, while the quantization noise is suppressed by the semi-digital FIR filter. In the proposed architecture, the digital IF signal is noise-shaped via a 4^{th}-order 1.5-bit BP ΣΔM to improve in-band SNR, while the out-of-band quantization noise due to noise-shaping is suppressed by the semi-digital FIR filter and analog image reject filter. In this work, the out-of-band quantization noise suppression is designed to meet W-CDMA spectrum emission mask and ACPR requirements [5]. 74dB dynamic range demanded by the W-CDMA standard [5] is distributed to ΣΔM stage and RF VGA to overcome substrate isolation limitation.

At the baseband I/Q signals generated from the base-band DSP block are first interpolated and up-sampled from 3.84MHz (W-CDMA chip rate is 3.84Mcps) to f_s=253.44MHz, and then digitally up-converted to the intermediate frequency (IF) at $f_{IF}=f_s/4$= 63.36MHz. By choosing a sampling frequency f_s within the range from250MHz to 260MHz, digital images will be out of the W-CDMA transmitter and receiver bands [1], thereby relaxing the requirements on the reconstruction filter after the DAC. The digital band-pass IF signal is 1.5-bit noise-shaped via the 4^{th}-order band-pass (BP) ΣΔ Modulator. The 3-level IF signaling reduces the transient glitch and the quantization noise level compared to a 2-level DAC and still maintains good linearity. Also the in-band SNR can be improved by approximately 5dB due to the additional half bit with the same

Table 2.1: Summary of transmitter architectures

Architecture	No. of up-conversion	No. of synthesizers/ off-chip IF filter	Pros	Cons
Super-heterodyne	2	2 / 1	High linearity High DR Wide bandwidth Good EVM ACPR	Bulky High power High cost
Homodyne	1	1 /0	Simple Low power Low cost	DC offset LO leakage Degraded EVM
Digital heterodyne	2	1 /0	High linearity High DR Wide bandwidth Good EVM ACPR Digital intense Low power	--

oversampling ratio and the loop-filter order [15]. Moreover, the lower quantization noise level could result in a lower order of the reconstruction filter. From the system level simulations, 1.5-bit 4^{th}-order BP ΣΔM is enough to provide in-band SNR with the sampling frequency of 253.44 MHz and the 40-tap BP FIR filter is sufficient to attenuate the out-of-band quantization noise and meet the W-CDMA spectrum emission mask and ACPR requirements. Higher order FIR filter could provide more out-of-band noise suppression, however it leads to higher quiescent power consumption. Figure 2.8 shows the W-CDMA IF spectrum after

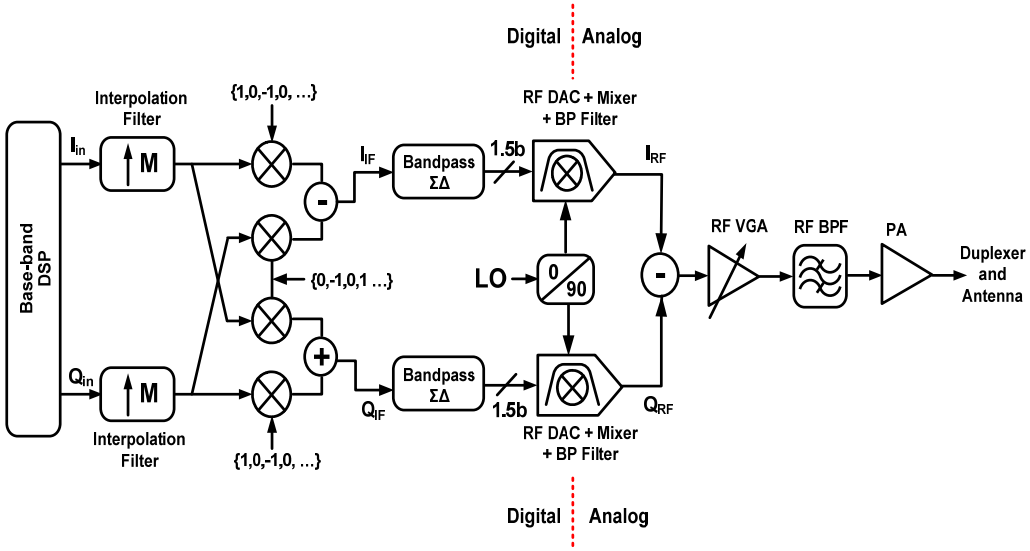


Figure 2.7: Proposed CMOS digital-IF transmitter

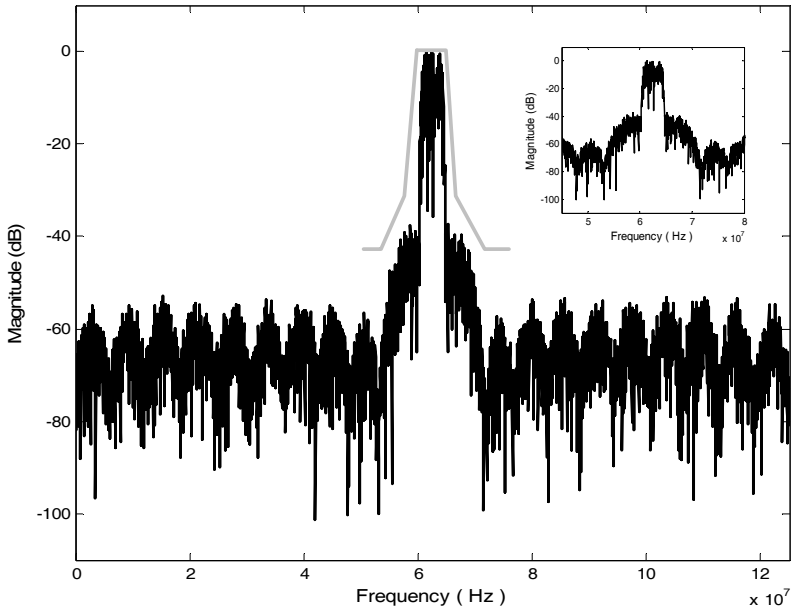


Figure 2.8: WCDMA IF spectrum after 40-tap BP FIR filtering (f_s=250 MHz)

the 40-tap FIR filtering. The zoom-in spectrum is shown on the upper-right corner of the figure. The gray line shows the W-CDMA mask.

One big advantage of the proposed architecture is that the traditional transmitter image issue is resolved by maintaining the signals in quadrature format from the baseband to the radio frequency. The accuracy of the single-sideband modulated signal is mainly determined by the first up-conversion quadrature mixers which are implemented in the digital domain in the proposed architecture.

The major building block of RFDAC+Mixer+BP filter of the proposed architecture is illustrated in Figure 2.9. The 1.5-bit noise-shaped digital IF signal generated by the BP ΣΔM feeds to the 40-tap FIR delay line, and the FIR delayed 3-level IF signals drive individual IF switch cell. The FIR coefficients (a_1 to a_{20}) due to the 40-tap BP FIR filtering are embedded in the IF switching stages and modulate the IF tail currents. The current-mode DAC outputs are summed, mixed with the LO and up-converted to radio frequency through the RF double-sideband (DSB) mixer. The mixer is loaded with an LC band-pass filter.

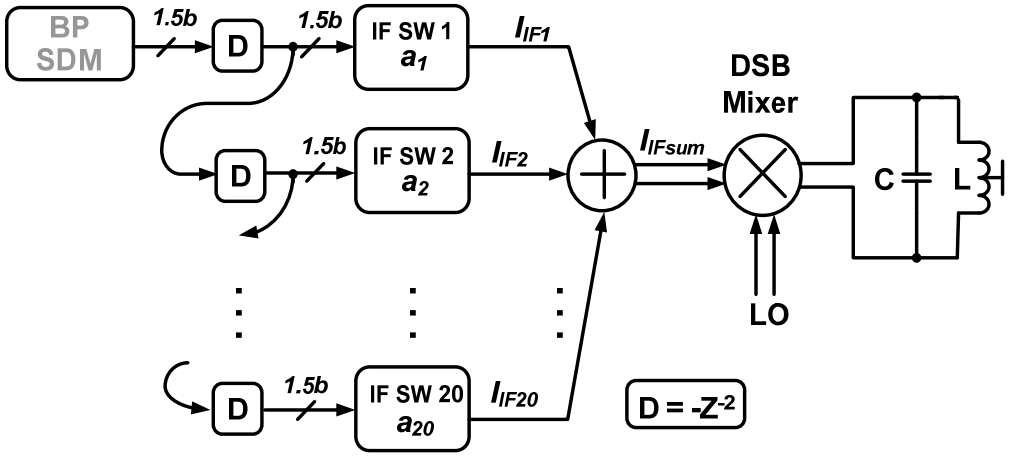


Figure 2.9: The RFDAC+Mixer+BP Filter block of the proposed RFDAC modulator

The entire block provides four functionalities: digital-to-analog conversion, frequency up-conversion, FIR reconstruction filtering, and the analog out-of-band image rejection filtering.

By adopting the proposed DRFTx architecture, the digital IF to RF converter can be extended for W-CDMA transmitter application with the benefits of circuit simplicity, high linearity and low power consumption.

CHAPTER 3

SYSTEM DESIGN OF THE PROPOSED TRANSMITTER

The design of the proposed W-CDMA transmitter is not straight-forward. First, the linearity requirement of the individual block including RFDAC and RFVGA needs to be derived based on the system level link budget analysis to avoid design randomness. Second, the IF band-pass sigma-delta modulator has to provide enough in-band signal-to-noise (SNR) while keeping the loop filter order as low as possible to ease circuit complexity and reduce power consumption. Finally, the out-of-band quantization noise generated at the BP SDM stage must be suppressed by the reconstruction filter down to the level where the adjacent channel signals are not affected. In this chapter, the system design of the proposed architecture will be presented including the transmitter linearity analysis, IF band-pass sigma-delta modulation and the FIR reconstruction filtering.

3.1 W-CDMA transmitter link budget analysis

3.1.1 System linearity requirement

In this section linearity and noise analysis of the proposed architecture based on W-CDMA transmitter link budget analysis is derived. The RFDAC non-ideality due to the finite output impedance is analyzed in order to give the lowest boundary for sizing FIR current sources.

Table 3.1 lists the major specifications of W-CDMA transmitter (class III). Table 3.2 lists the W-CDMA spectral emission mask requirements [5].

W-CDMA is a full duplex system where the transmitter and receiver

Table 3.1 W-CDMA transmitter specifications

Frequency band	1920MHz – 1980MHz
Channel spacing	5MHz
Chip rate	3.84 Mbps
Modulation	QPSK
Max. Power at antenna	24dBm (+1dB/-3dB)
Max. Power at PA output	28dBm **
RMS EVM	< 17.5%
ACPR	-33dBc @ 5MHz offset -43dBc @ 10MHz offset

Table 3.2 W-CDMA spectral emission mask requirement [5]

Δf in MHz	Relative Requirement in dBc	Measurement BW
2.5 – 3.5	-35 -15*(Δf /MHz -2.5)	30kHz
2.5 – 7.5	-35 -1*(Δf /MHz -3.5)	1MHz
7.5 – 8.5	-39 -10*(Δf /MHz -7.5)	1MHz
8.5 – 12.5 MHz	-49	1MHz

operate simultaneously at different frequencies. The nonlinear distortion generated by a mobile transmitter can spill over into the adjacent channel, or the receive band and impact received signal bit error rate (BER). Therefore digital cellular standards restrict the amount of emissions permitted in the adjacent and alternate channels. Usually, adjacent channel power arises from the spectral re-growth due to inter-modulation distortions (IMDs) from the transmitter.

In general, the ACPR at the first channel offset is dominated by the 3rd-order inter-modulation distortion (IMD3), while the ACPR at the second channel offset is mainly determined by the 5th-order inter-modulation distortion (IMD5). For the W-CDMA transmit signal which occupies a bandwidth of 5MHz, a multi-tone test [16] [17] is required to predict accurate distortion in the adjacent and alternate channels which is not an easy task in the transmitter system analysis due to long and complicated simulations required. Based on the narrow-band approximation and with a periodic modulating waveform assumption, the modulated W-CDMA signal issue can be treated as a conventional two-tone test [18]. With this approach, ACPR requirements can be translated to conventional IMD3 or OIP3 specifications.

The proposed transmitter can be modeled as a non-linear block in the transmitter analysis using the setup as shown in Figure 3.1. In this setup, an ideal W-CDMA baseband signal drives the non-linear transmitter and ACPR

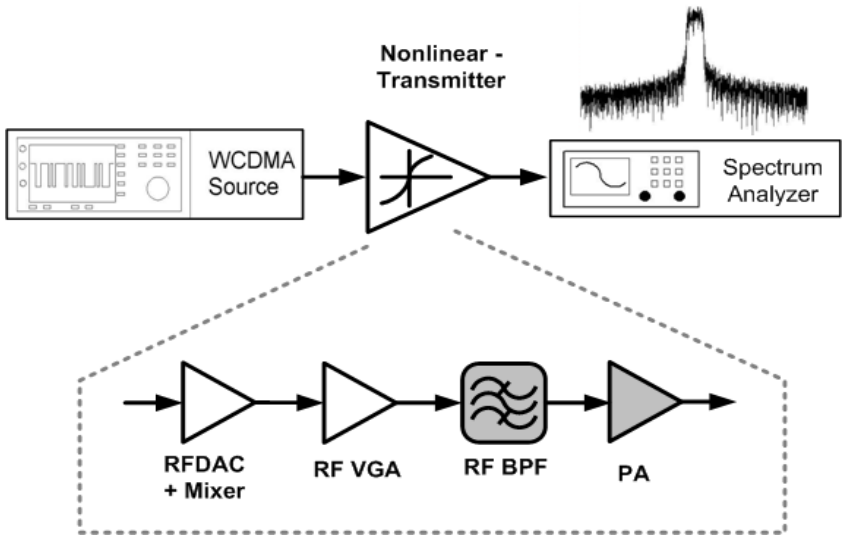


Figure 3.1: Non-linear transmitter analysis setup

performances are evaluated at the output using a spectrum analyzer. The nonlinear transmitter includes RFDAC with mixer, RF VGA, RF BPF and PA in cascade. The relationship between ACPR at the first channel offset and OIP_3 of the transmitter including PA can be approximately expressed based on the two-tone test as follows:

$$ACPR_{TX} \cong 2(P_{TX} - OIP_{3,TX}) - 9 + C_0 + 10\log_{10}\left(\frac{BW_{ACP}}{BW}\right) \quad (3.1)$$

where $C_0 \cong 0.85 * (PAR - 3)$, PAR is the peak-to-average ratio of the transmitted signal which is 3.28dB for π/4-QPSK modulated signal. $ACPR_{TX}$, P_{TX}, $OIP_{3,TX}$ are the ACPR performance, the transmitted power and OIP3 at the transmitter output respectively. BW_{ACP} represents the measuring bandwidth for the adjacent channel power which is 3.84MHz for W-CDMA signal, and BW is the desired transmitted signal bandwidth after taking the roll-off factor of 0.22 into account [19].

According to the standard, the ACPR at 5MHz and 10MHz offsets from the center of the main channel must be less than -33dBc and -43dBc, respectively [5]. Figure 3.2 shows the ACPR and OIP_3 of the transmitter based on the equation (1) with the transmitted power of 25dBm which is targeted to the W-CDMA band I class III power level (when taking additional 2dB loss due to duplexer at the antenna end). From the Fig. 3.2, to achieve better than -33dBc ACPR at 5MHz offset, the minimum transmitter OIP_3 is required to be at least +36.7dBm. In the proposed design, OIP3 of 38dBm at the PA output is chosen as a design target to leave 3 to 4dB margin for ACPR at first channel offset. Fig. 3.3 shows the output of the spectrum with different OIP3s which emphasizes how the linearity of the

transmitter impact on the ACPR performances.

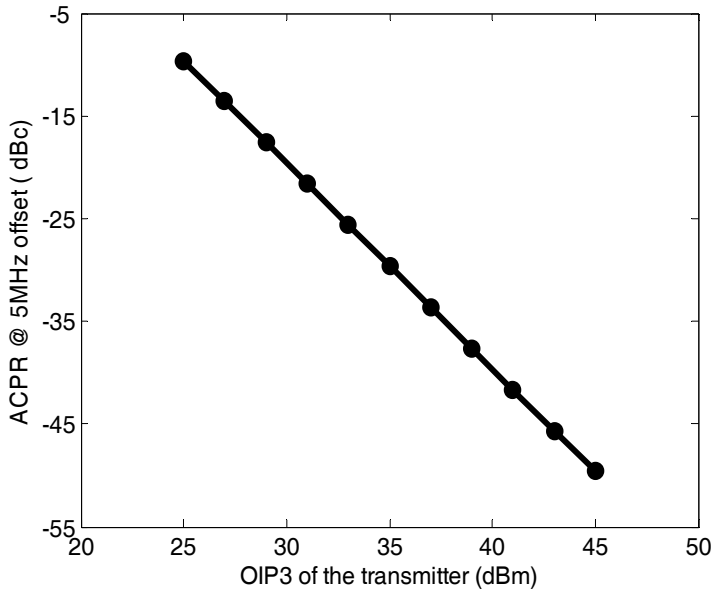


Figure 3.2: Plot of transmitter OIP3 vs. ACPR at 5MHz offset

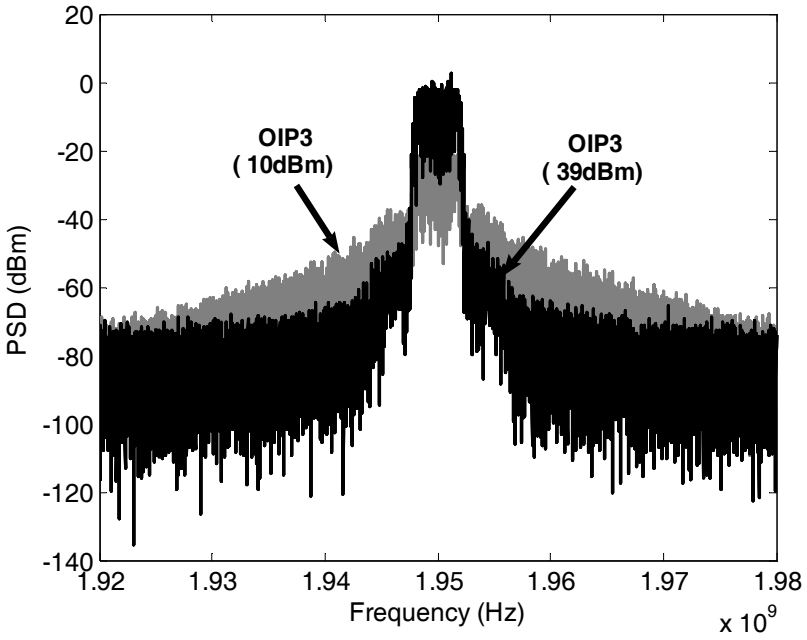


Figure 3.3: WCDMA output spectrums with two TXs' OIP3s

3.1.2. DAC +FIR linearity

In the proposed architecture, the transmitter linearity in terms of OIP3 or IMD3 is determined by the RFDAC, the VGA, RF BPF and the PA. The overall transmit linearity specification can be expressed by equation (3.2) [19]. Since the linearity of the RF BPF is usually close to ideal, the equation (3.2) can be simplified as equation (3.3). From equation (3.3), in order to relax linearity requirements on the RFVGA and PA, the FIR DAC and mixer linearity must be optimized.

$$\frac{1}{OIP3_{TX}} = \frac{1}{\frac{G_{VGA} * G_{BPF} * G_{PA}}{OIP3_{RFDAC}}} + \frac{1}{\frac{G_{BPF} * G_{PA}}{OIP3_{VGA}}} + \frac{1}{\frac{G_{PA}}{OIP3_{BPF}}} + \frac{1}{OIP3_{PA}} \tag{3.2}$$

$$\frac{1}{OIP3_{TX}} = \frac{1}{\frac{G_{VGA} * G_{BPF} * G_{PA}}{OIP3_{RFDAC}}} + \frac{1}{\frac{G_{BPF} * G_{PA}}{OIP3_{VGA}}} + \frac{1}{OIP3_{PA}} \tag{3.3}$$

where $OIP3_{TX}$, $OIP3_{RFDAC}$, $OIP3_{VGA}$, $OIP3_{PA}$ are the output 3rd order intercept points of the transmitter, RFDAC and mixer, RF VGA and PA, respectively. G_{VGA} and G_{PA} are the power gains of the RF VGA and PA. G_{BPF} is the loss of the RF BPF.

Using a commercial PA MAX2291 [11] (ACPR of -38dBc at the first channel offset with P_{out} = 28dBm which translates into $OIP3_{PA}$ = 42.2dBm, G_{PA} = 27dB) and with the designed RF VGA targeted for *OIP3* of +16dBm and the maximum power gain of 10dB, the *OIP3* of the RFDAC and mixer should be at +14.3dBm from equation (3.3) with 2dB loss due to RF BPF.

The major source of nonlinearity of current steering DACs is the finite

output impedance of DAC current sources [21]. In order to better understand how the output impedances of FIR based DACs impact on the linearity of the transmitter, the up-conversion switching quad is considered ideally linear. Therefore, nonlinear behavior of the RFDAC is analyzed using the simplified model of Figure 3.4, where a_1 to a_N are the coefficients of the FIR filter. I_1 to I_N are the FIR-scaled current sources with finite output impedances R_{o1} and R_{oN}. Moreover, S_1 to S_N are the IF switches and R_L is the equivalent mixer's output load resistance at the resonance frequency of 2GHz which is set by the LC tank in Figure 3.4. Since the mixer is ideal, the nonlinearity from the FIR DAC will directly appear at the mixer output, and mixer switches are neglected in the simplified circuit.

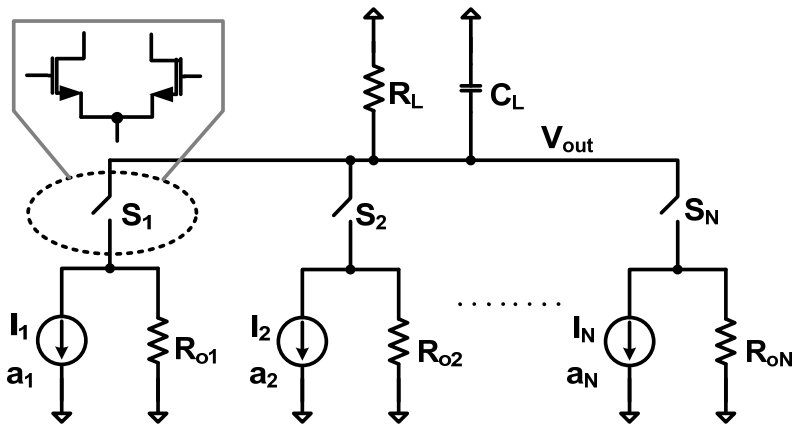


Figure 3.4: Simplified RFDAC circuit

Defining I_0 as the normalized current and g_0 as the normalized conductance related to I_0, we have

$$a_1 = I_1/I_0 = 1,\ a_1 = I_2/I_0\ ,\ \ \ldots\ ,\ a_N = I_N/I_0 \tag{3.4}$$

$$g_{o1} = 1/R_{o1},\ \ g_{o2} = 1/R_{o2},\ \ldots,\ g_{oN} = 1/R_{oN};\ \ g_L = 1/R_L \tag{3.5}$$

where $a_1, a_2, \ldots, a_N$ are the FIR coefficients. $g_{o1}, g_{o2}, \ldots, g_{oN}$ are the conductances of the current sources I_1 to I_N, respectively.

For a sinusoidal output V_{out} each of the DAC switches is either ON or OFF at a given time [20].

$$s(t)_{on} = \frac{1+\sin \omega t}{2} \ , \ \ s(t)_{off} = \frac{1-\sin \omega t}{2} \tag{3.6}$$

The total output conductance when the N switches are "on" is

$$g_{out,on} = g_L + \left((a_1 + a_2 + \ldots + a_N) \cdot g_0 \cdot s(t)_{on}\right)$$

$$= g_L + \sum_{i=1}^{N} a_i \cdot g_0 \cdot \left(\frac{1+\sin \omega t}{2}\right) \tag{3.7}$$

and the total complementary output conductance is

$$g_{out,off} = g_L + \left(\left(a_1 + a_2 + \ldots + a_N\right) \cdot g_0 \cdot \left(\frac{1-\sin \omega t}{2}\right)\right) \tag{3.8}$$

The differential output voltage is

$$V_{out,diff} = \frac{4 \cdot g_L \cdot F_N \cdot I_0 \cdot \sin \omega t}{4{g_L}^2 + 4 g_L \cdot g_0 \cdot F_N + {F_N}^2 \cdot {g_0}^2 \cdot \left(1 - \sin^2 \omega t\right)} \tag{3.9}$$

where $F_N = \sum_{i=1}^{N} a_i$ is the sum of the normalized FIR coefficients.

Assigning $x = \sin \omega t$ (a single-tone excitation)

yields

$$V_{out,diff} = \frac{4 \cdot g_L \cdot F_N \cdot I_0 \cdot x}{4{g_L}^2 + 4 g_L \cdot g_0 \cdot F_N + {F_N}^2 \cdot {g_0}^2 \cdot \left(1 - x^2\right)}$$

$$= \frac{H \cdot x}{1 + Q \cdot (1 - x^2)} \tag{3.10}$$

where

$$H = \frac{4 \cdot g_L \cdot F_N \cdot I_o}{4{g_L}^2 + 4 g_L \cdot g_o \cdot F_N}$$

$$Q = \frac{{F_N}^2 \cdot {g_o}^2}{4{g_L}^2 + 4 g_L \cdot g_o \cdot F_N}$$

Using Taylor expansion,

$$V_{out,diff} = A_1 \cdot x + A_3 \cdot x^3 \tag{3.11}$$

Since the fundamental tone and the third-order components have the following relationship [12]

$$IMD3 = \frac{4}{3} \cdot \left| \frac{A_1}{A_3} \right| = \frac{\frac{14}{3} {F_N}^2 \cdot {g_0}^2 + \frac{16}{3}\left({g_L}^2 + g_L \cdot g_0 \cdot F_N\right)}{{F_N}^2 \cdot {g_0}^2} \tag{3.12}$$

The *OIP3* of the FIR DAC is

$$OIP3_{RFDAC} = G_{RFDAC} + \frac{IMD3_{RFDAC}}{2} + P_{IN,RFDAC} = \frac{IMD3}{2} + P_{OUT,RFDAC} \tag{3.13}$$

where G_{FIRDAC} is the gain of the FIR DAC in dB, $P_{IN,RFDAC}$ and $P_{OUT,RFDAC}$ are the input and output power of the RFDAC. Since the OIP3 of RFDAC is at least 14.3dBm, and the $P_{OUT,RFDAC}$ is designed to be maximum of -10dBm, the minimum IMD_3 of RFDAC is set to be about 49dB based on equation (3.13).

Figure 3.5 shows the impact of the finite output impedances of 40-tap FIR current sources on the IMD3 of the RFDAC. In order to achieve -38dBc ACPR at 5MHz offset, IMD3 of the RFDAC needs to be at least 49dB, which translates to the minimum unit current source output impedance of 600kΩ.

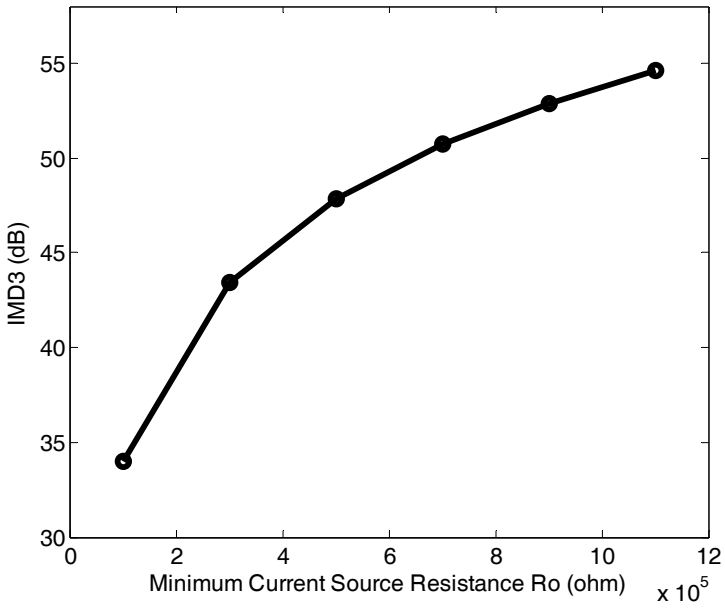


Figure 3.5: RFDAC IMD3 vs. normalized current source resistance

3.2 System design of IF band-pass sigma-delta modulator

The design of 1.5-bit IF band-pass sigma-delta modulator is mainly targeted for the high in-band SNR while keeping the loop-filter order as low as possible. In order to ease the design of the following DAC and eliminate extra matching circuitries, 1.5-bit quantizer is chosen. Compared to the inherent linear 1-bit DAC, 3-level DAC reduces the transient glitch and the quantization noise level and still maintains good linearity. Also the in-band SNR can be improved by approximately 5dB due to the additional half bit with the same oversampling ratio and the loop-filter order [21]. Moreover, the lower quantization noise level could result in lower order of the reconstruction filter.

From the wave quality requirement of W-CDMA, in-band SNR needs to be at 36dB (equivalent to 6-bit ENOB). With the quantizer bit is fixed at 1.5-bit

level, the order of the filter needs to be derived to provide minimum 36dB in-band SNR. For the sigma-delta modulator with the same quantizer bit, the higher the order the higher the SNR can be achieved based on the following equation [22]:

$$SNR_P = \frac{3\pi}{2}(2B-1)^2 * (2n+1) * (\frac{OSR}{\pi})^{2n+1} \tag{3.14}$$

where the SNR_P is the full-scale SNR, B is the quantizer bit, n is the loop-filter order, OSR is the over-sampling ratio.

However as shown in Figure 3.6, the higher loop-filter order results in higher out-of-band quantization noise level due to the more aggressive noise-shaping. In order to suppress the out-of-band noise below the required ACPR levels, the higher order reconstruction filter order is required and will ultimately

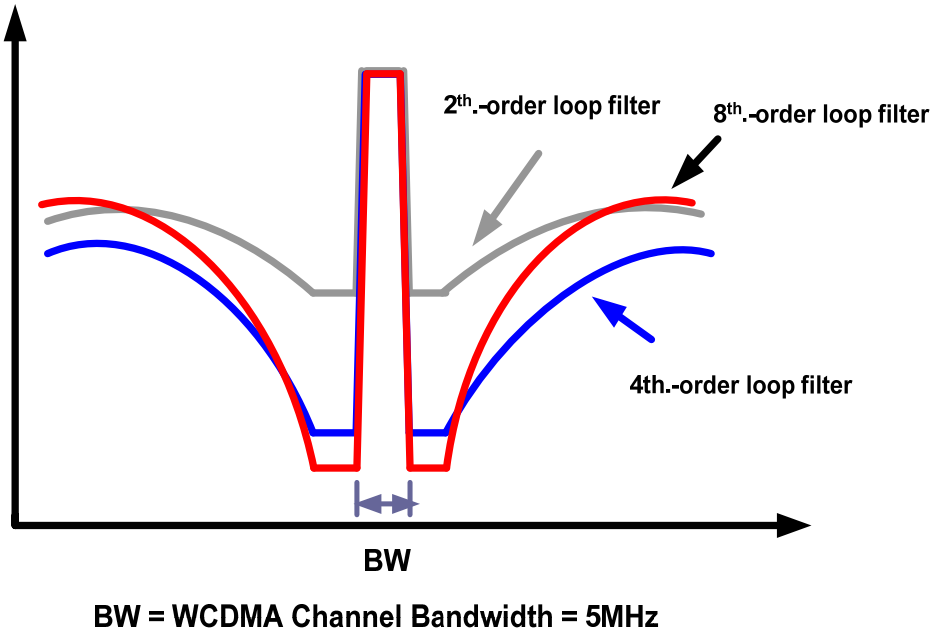


Figure 3.6: The relationship between the in-band SNR and out-of-band noise with different loop-filter orders (same quantizer bits)

complicate the design and drive the circuit power consumption high. On the other hand, if the filter order is low, even though the out-of-band quantization noise level is low compared to the higher-order ones, it might not provide enough in-band SNR and degrade the ultimate W-CDMA wave quality. Therefore there is trade-off among in-band SNR, the sigma-delta loop filter order and the following reconstruction filter order.

For the current design, the IF is fixed at 62.5MHz with the digital LO frequency at 250MHz due to the image issue explained before. Therefore, the sampling frequency *fs* is equal to 250MHz, and the signal bandwidth f_{BW} is equal to 5MHz, the OSR is about 25 using the following equation [15]:

$$OSR = \frac{f_S / 2}{f_{BW}} \tag{3.15}$$

Up to now, the minimum SNR, the quantizer bit and OSR are given, the order of the loop filter can be derived from the simulations using different loop-filter order. Table 3.3 lists the simulated SNR with OSR =25 and the signal BW of 5MHz. From the table, 2nd.-order loop filter can only provide marginal in-band SNR, when taking the degradation happening along the following upconversion path, approximately 38dB in-band SNR is absolutely not enough. From the simulation results, a 4th.-order bandpass sigma-delta modulator is chosen based on the decent in-band SNR it offers. Figure 3.7 shows the W-CDMA IF signal after the 1.5-bit 4th-order band-pass sigma-delta modulator.

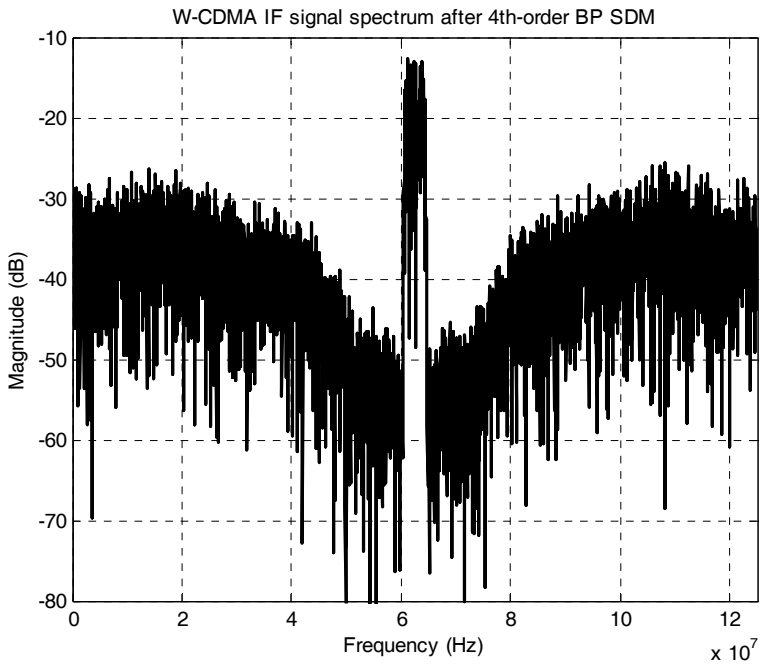


Figure 3.7: W-CDMA IF signal after 4th.-order BP sigma-delta modulator

Table 3.3: Simulated SNR with signal BW of 5MHz with OSR = 25

Loop filter order	Quantizer bits	SNR (dB)
2nd. – order (BP)	1.5	~ 38
4th – order (BP)	1.5	~ 62

3.3 System design of band-pass FIR reconstruction filter

W-CDMA transmitter demands minimum 33dBc and 43dBc ACPR at the first channel (5MHz) and the second channel (10MHz) offset, while the 3-level IF signals contain high out-of-band quantization noise due to the noise-shaping from the IF band-pass sigma-delta modulator. Without proper filtering the out-of-band noise, it is impossible for the proposed transmitter to meet the ACPR

requirements.

The main purpose of the using FIR filter as reconstruction filter is its linear-phase property which is critical to maintain linearity of the transmit signal after filtering. Moreover, the FIR coefficients can be easily programmed to fit different transmit standards, therefore, it has the potential for the reconfigurable multi-band transmitter applications.

The general structure of band-pass FIR filters is illustrated in Figure 3.8, and the equation representing the structure can be expressed as [23]

$$H_{FIR}(z) = a_0 + a_1 * (-z^{-2}) + ... + a_{n-1} * (-z^{-2})^{n-1} + a_n * (-z^{-2})^n \qquad (3.16)$$

where the a_0, a_1, a_2, …, a_{n-1}, and a_n are the FIR coefficients, and $-z^{-2}$ is the band-pass delay unit, and n is the filter order. From equation (3.16), the filter frequency response is determined by the FIR coefficients and the filter orders.

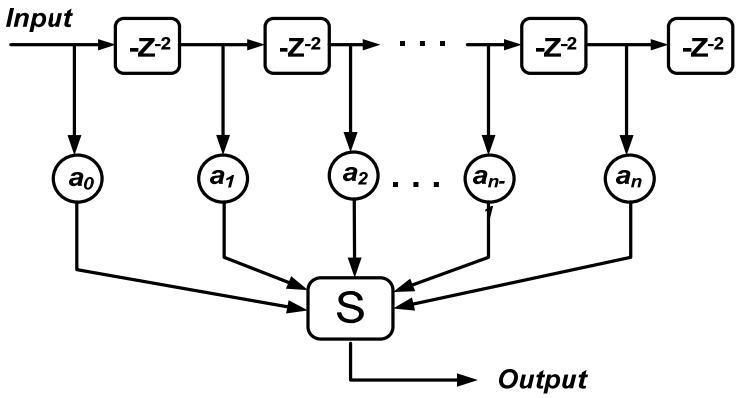


Figure 3.8: Band-pass FIR filter structure

In order to meet the W-CDMA ACPR requirement while keeping low the filter order, different types of windows are examined, including Rectangular, Kaiser, Triangler and Hann. With the multiple iterations, a 36-tap FIR filter using

Kaiser window and Beta equal to 3 is found to meet the W-CDMA emission mask requirements for the clock rate of 250MHz. For real circuit implementation, the exact coefficients are hard to achieve. Therefore, the rounded FIR coefficients are used. Taking the FIR coefficient rounding effect and the real silicon non-ideality into account, 40-tap FIR filter is more realistic to meet the target. Figure 3.9 shows the 40-tap band-pass FIR filter frequency response without rounding, and its phase frequency response is shown in Figure 3.10.

As mentioned before, one reason to pick the FIR filter for the signal reconstruction is its programmability. With the same FIR filter order and different FIR coefficients, the filter can be used as the reconstruction filter for other transmit band, for instance, the 2.4GHz WLAN 802.11g band. Figure 3.11 plots the 40-tap FIR frequency response for 2GHz WLAN transmit band, and its phase frequency response is shown in Figure 3.12. Figure 3.13 shows the magnitude frequency response for both W-CDMA and WLAN 802.11g on the same plot to have better view of 40-tap FIR filter for both transmit bands in terms of bandwidth, notches and out-of-band roll-off.

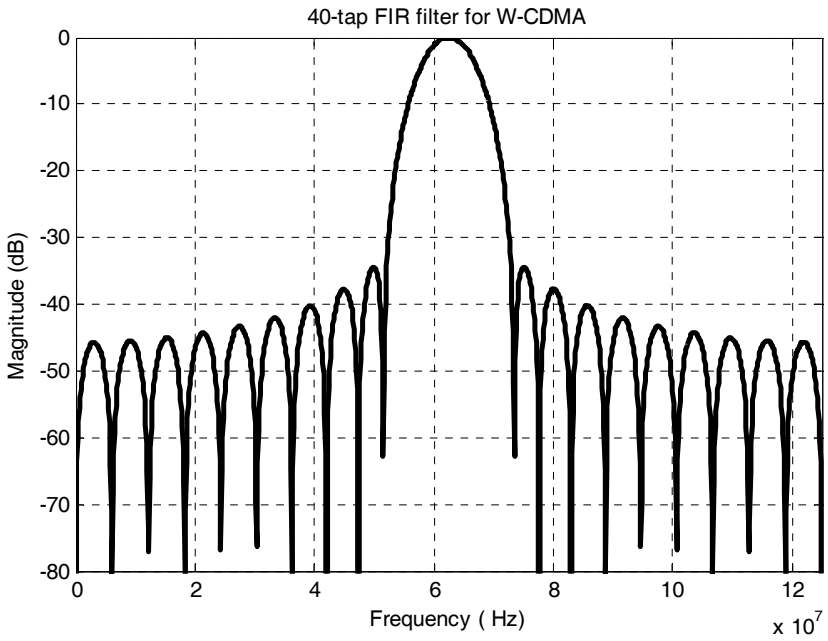


Figure 3.9: 40-tap band-pass FIR magnitude response for W-CDMA

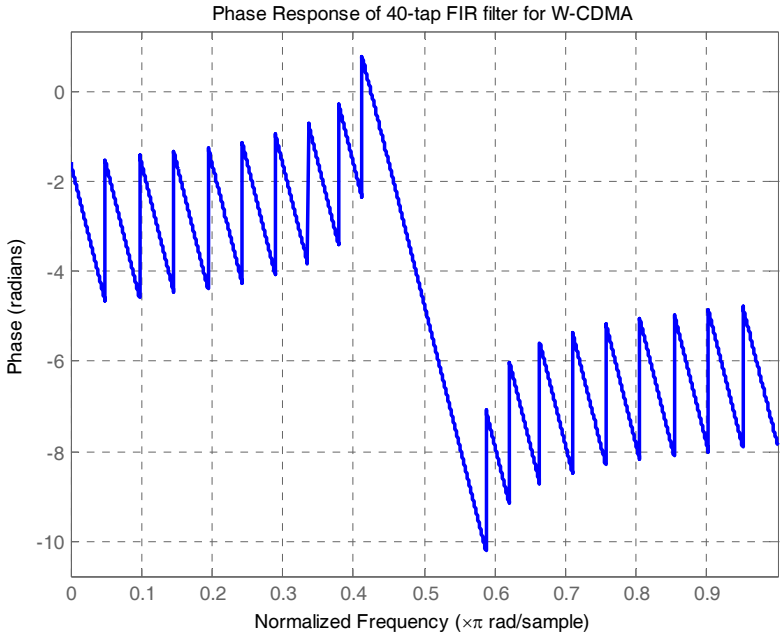


Figure 3.10: 40-tap band-pass FIR phase response for W-CDMA

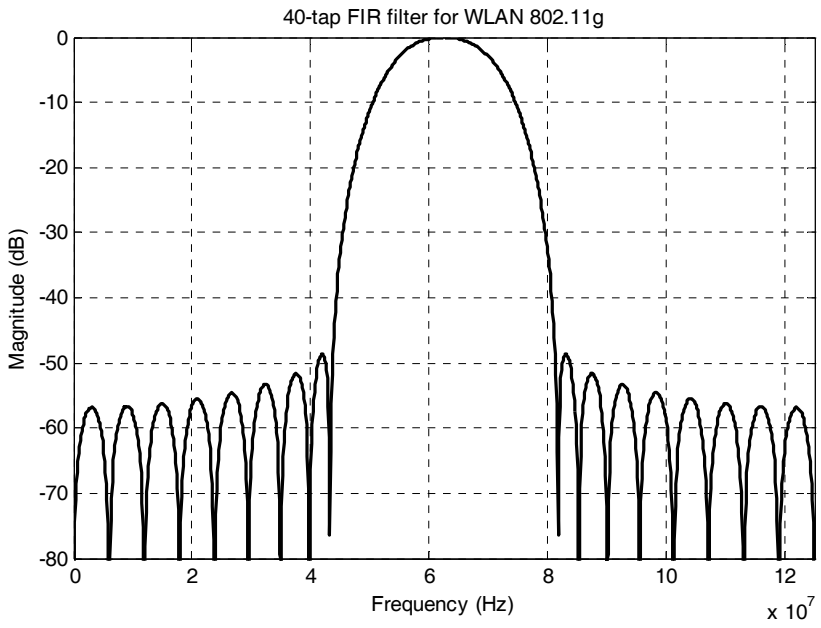


Figure 3.11: 40-tap FIR filter magnitude response for 2.4GHz WLAN band

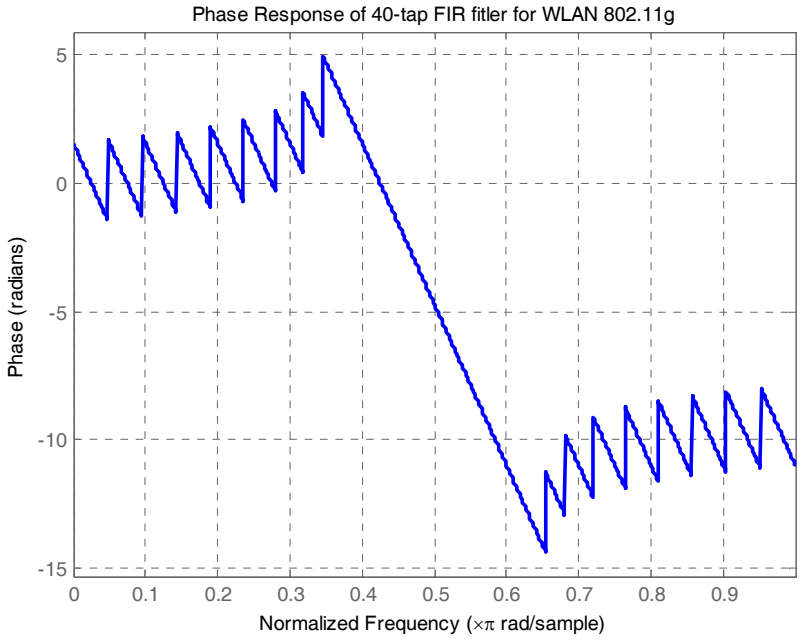


Figure 3.12: 40-tap FIR filter phase response for 2.4GHz WLAN band

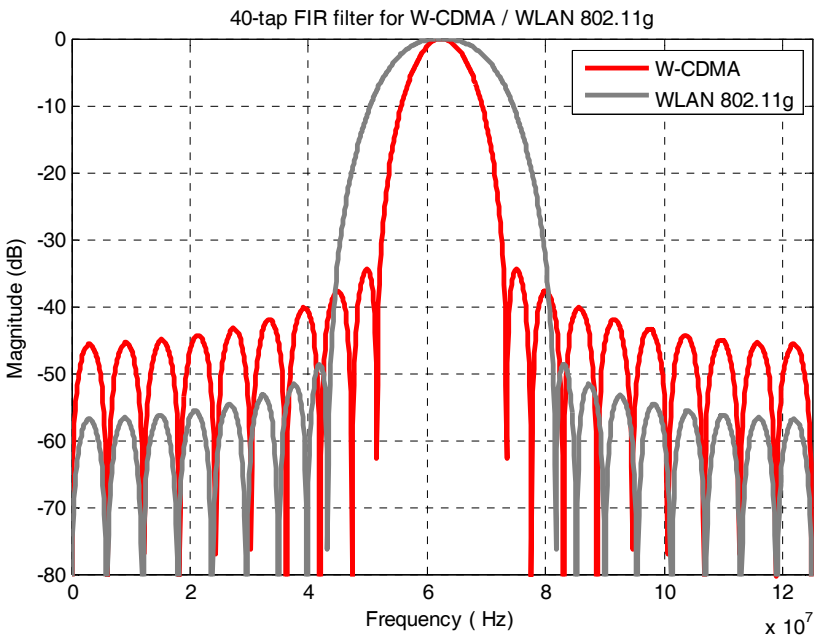


Figure 3.13: 40-tap FIR filter magnitude responses for both W-CDMA and WLAN 802.11g bands

3.4 Summary

In the chapter the linearity requirements of each individual blocks including RFDAC and RFVGA have been derived based on the system link budget analysis and will be used as the guideline for the circuit implementations. From the linearity analysis in order to meet target ACPR of -38dBc at the first channel offset, OIP3 of RFV GA needs to be at least +14.3dBm at the maximum gain of 10 and the minimum unit current source resistance has to be greater than 600kΩ. A 1.5-bit 4^{th}-order band-pass sigma-delta modulator has given based on the trade-off in terms of in-band SNR, out-of-band quantization noise level and the reconstruction filter order. The FIR reconstruction filter has been designed to

meet W-CDMA transmitter emission requirements. Also the programmability of the FIR filter has been demonstrated using 2.4 GHz WLAN 802.11g band as an example.

CHAPTER 4

DESIGN AND IMPLEMENTATION OF IF TO RF DAC

The proposed digital IF to RFDAC transmitter has been integrated in a four-metal 0.18μm CMOS technology. The chip includes major circuits of digital IF to RF converter with embedded band-pass reconstruction FIR filter, RF VGA, clock buffers and frequency dividers. In this chapter, the design and implementation of the FIR reconstruction filter and RFDAC core are presented. The critical design specifications are given based on the W-CMDA transmitter system analysis in chapter 3. Since the RF VGA is a standalone block, the design of RF VGA will be demonstrated in the chapter 5 separately.

4.1 Top-level implementation of IF to RF upconversion

Fig.4.1 shows the top level schematic of digital IF to RF converter with embedded BP FIR filter. It includes a current-steering DAC, 1.5-bit digital IF switching cells, FIR filter and Gilbert-cell up-converter. Since 40-tap BP FIR filter is adopted for this design, there are 20 delay cells each of which realizes inverse of two unit delays based on $-z^{-2}$ in the digital domain, hence 20 IF switching cells each of which is driven by the delayed 3-level digital noise-shaped IF signal. The 20 non-zero FIR coefficients a_1 to a_{20} are embedded in the current sources of the IF switching stages. The output currents from all IF switching stages are summed and sent to the LO quad and then up-converted to the desired frequency of 2GHz. By absorbing FIR coefficients into the current sources of IF switching stages, the RFDAC, up-conversion mixer and BP FIR filter are merged

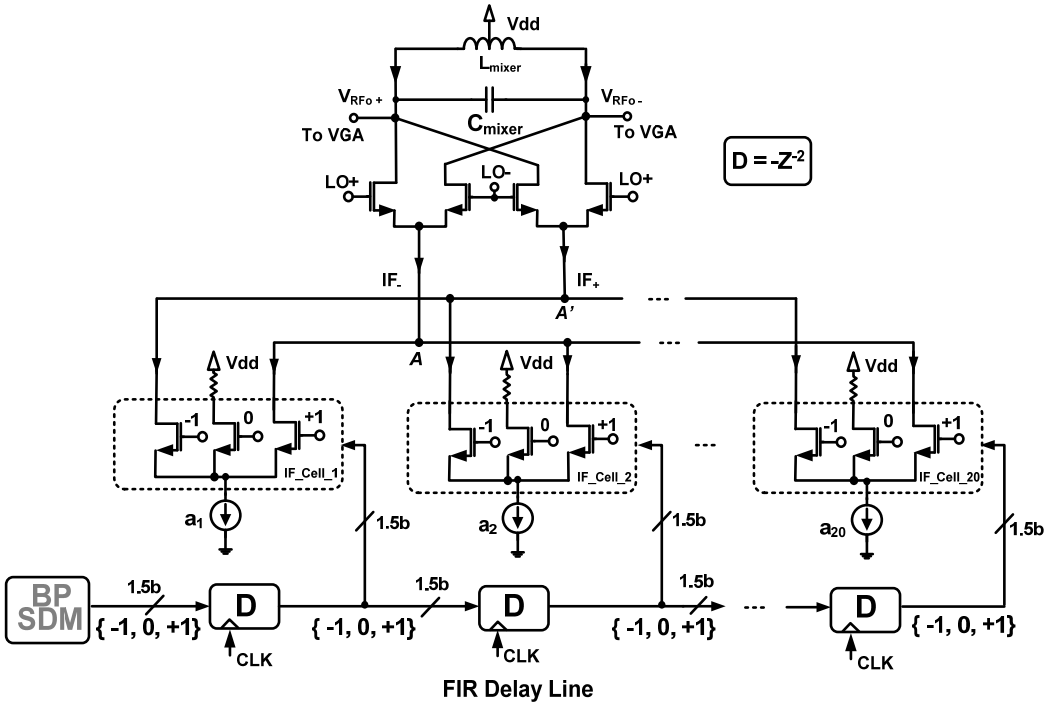


Figure 4.1: Top-level schematic of digital IF to RF converter with BP reconstruction filter

into a compact block.

The three-level IF signaling is achieved in the DAC path by adding a current dump path to the two-level DAC. Therefore there is a positive path corresponding to +1, a negative path corresponding to -1, and a dump path related to 0. As shown in Fig. 4.1for each current source there is an IF switch cell which consists of three NMOS devices to implement the 3-level DAC signaling. Each tap from 1 to 20 has a different DC current weighted by the FIR filter coefficients, therefore the DC current in the conducting device of the IF switches will be different for each tap. For the circuit level implementation of the FIR filter coefficients, DC current sources are used. The DC current sources are implemented using NMOS transistors, and sizes of the transistors are scaled by

the filter coefficients. The length of the current source devices is chosen such that they can achieve the desired output impedance. The output impedances of the current sources should be greater than the value derived in Chapter 3. The widths of NMOS devices consist of multiples of a unit device size for good matching between current sources and the multiples are actually the scaled filter coefficients. The device sizes are symmetrical around the center to maximize phase linearity, so there are only 10 different filter coefficients. The gate voltage of the NMOS devices is biased through a constant-gm current bias circuit. The design and implementation trade-offs of each individual sub-blocks including FIR reconstruction filter, 3-level DAC input signal generation, IF switch cell and RF mixer will be covered from section 4.2 to 4.5.

4.2 Design of FIR reconstruction filter

There are two sets of current source arrays as shown in Figure 4.2. Depending on the standard of operation (W-CDMA or WLAN) one set is turned ON or the other. The selection circuit connects or disconnects the gate of the NMOS current sources to a bias voltage or to ground.

The FIR filter coefficients are implemented by the DC current sources as shown in Figure 4.2, which applies for both sets of current sources. The widths W1 to W10 are different for two modes. The NMOS transistors with Length=0.72um (3 times the minimum length of the process) are used in order to get high output resistance current sources which directly affects the linearity. The widths of NMOS devices consist of multiples of a unit device size for good

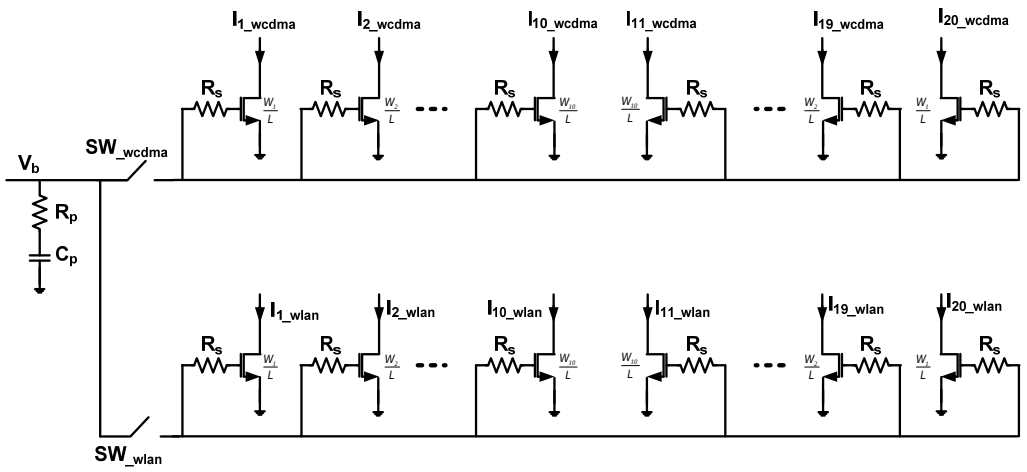


Figure 4.2 The DC current sources forming the FIR filter response (W-CDMA or WLAN)

matching between current sources and the multiples are actually the filter coefficients. The device sizes are symmetrical around the center (W1=W20, I1=I20). The gate voltage of the NMOS devices is biased through a constant-gm current bias circuit “Vb” as shown in Figure 4.2. The bias voltage is grounded by Cp which is about 4pF to filter noise that is coupled to the bias circuitry. In order to avoid oscillation which may occur in bond-wire inductors of the DC ground and the Cp and also the parasitic capacitors, a damping resistor Rp=10 Ω is added in series to the CP and a high resistor Rs=3.6KΩ is added in series to the gate bias.

4.3 A 1.5-bit IF DAC input signal generation

The DAC operates as 1.5-bit DAC (3-level DAC). There are two inputs to the DAC, M and N as shown in Fig.4.3. A three level quantizer is used in noise

shaping and two inputs are taken from the ∑Δ modulator, M and N as shown in Figure 4.3. The addition of the third level is achieved quite simply by adding a dump path to the existing two-level DAC and some simple digital decoding. The DC currents of each unit current source of the current steering DAC have three paths, positive, negative and a dump path. Since the FIR filter is a bandpass filter with factor 2 of interpolation, there is going to be Z^{-1} and $-Z^{-2}$ blocks, where Z^{-1} is implemented by a pseudo-NMOS DFF and the $-Z^{-2}$ by two DFFs following by an inverting block. 3-level DAC logic is defined in Table 4.1.

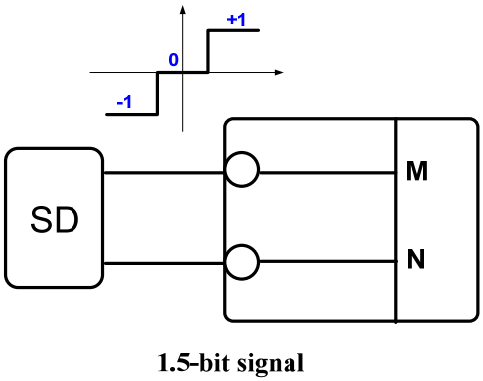


Figure 4.3: 1.5-bit DAC signal generation

Table 4.1: The logic used for DAC

X	Y	Transmitted number
1	0	+1
0	1	-1
0	0	0
1	1	NA (not transmitted)

4.4 IF switching cell

As mentioned before, for each FIR current source there is an IF switch cell which consists of three NMOS devices out of which only one is ON (in saturation) and the other two are off at each time. The DC current of each tap from 1 to 20 are different and modulated by the FIR filter coefficients, therefore the DC current in the conducting device of the IF switches will be different for each tap. In order to maintain the same current density in the IF switches of all taps, the switches are scaled with currents or FIR coefficients. The unit size is designed to optimize for best operation point, allowing highest swing and high gm, and the multiples are used to scale the sizes according to the coefficients.

However there are two possibilities for current value in each tap, corresponding to the two standards. Since the IF switches are shared between WCDMA and WLAN modes, the average of the size needed in each mode is used to minimize the change in current density in the saturated NMOS's. Figure 4.4

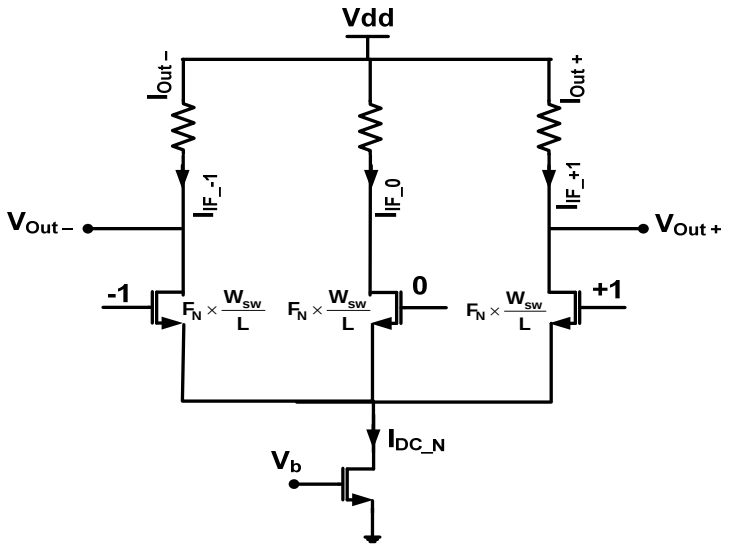


Figure 4.4: The IF switch cell for N_{th} tap

shows the N_{th} tap consisting of positive (+1), negative (-1) and dump current path (0) with device sizes scaled by F_N for the N_{th} tap as explained above.

4.5 Gilbert-cell Mixer

The up-conversion mixer is realized using a double-balanced fully differential Gilbert-cell mixer that offers low LO leakage to the output as shown in Fig. 4.5. In order to have an option for the WLAN band operation, a tunable LC load is designed with variable C_{mixer} and the fixed L_{mixer}.

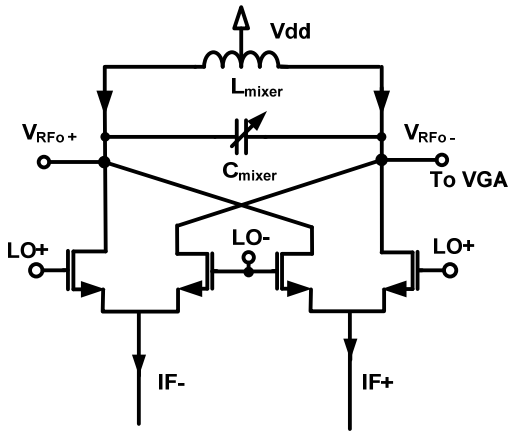


Figure 4.5: The Gilbert-cell based RF up-conversion mixer

4.6 Frequency Divider and Clock Buffer

As explained in [1], in order to push the digital images out of the receiver bands, the LO frequency is chosen to be around 2GHz and the sampling frequency f_s is no less than but close to 250MHz. The on-chip clock of 250MHz is generated by the LO frequency divided down by 8. The frequency divider is shown in Fig. 4.6. It consists of three ÷2 stages and refreshing buffers. The output of the last divider is re-clocked by the input signal at 2GHz. The last DFF is

placed next to the input LO to minimize the on-chip layout length and the delay as shown in the dashed line in Fig. 4.6. The clock buffer is designed to drive a large number of the digital gates. In order to achieve equal length for all the digital paths, the clock buffer layout is in a tree form.

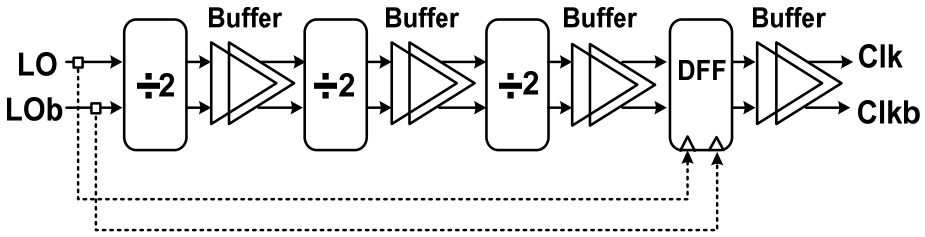


Fig. 4.6: Frequency divider with division ratio of 8

4.7 Summary

The IF to RF DAC presented in this chapter consists of a current-steering 3-level DAC, 1.5-bit digital IF switching cells, FIR filter and Gilbert-cell up-converter. Different form the traditional way of implementation of DAC following RF mixer and then RF band-pass filtering, it merges the DAC, mixer and the reconstruction filter into a single block to reduce circuit complexity and power consumption. The DAC design is based on the linearity requirement derived from Chapter 3. The design details of each individual sub-blocks including the 40-tap FIR filter, 3-level DAC input signal generation, 1.5-bit IF switching cells, RF mixer as well as the clock divider and buffer are demonstrated with the main focus on the design trade-offs. Also the design of IF to RF DAC provides an option for WLAN 802.11g application with different sets of WLAN FIR coefficients and tunable RF mixer load to potentially maximize the circuit

reuse.

The designed IF to RF upconverter with embedded FIR reconstruction filter is implemented using 0.18μm IBM7RF CMOS technology. It consumes approximately 67mA current from 1.8V DC supply and occupies about 0.61μm^2 dies area.

CHAPTER 5

DESIGN OF RF VARIABLE GAIN AMPLIFIER

According to W-CDMA standard, the base station should receive equal power from each other. Therefore, the transmitters need to be regulated based on the different locations and distances from the base station. The minimum 74dB dynamic range is demanded in the W-CDMA mobile transmitter standard [5]. The power control could be done entirely at the RF power amplifier (PA) stage, but it requires super linear and high power PA which makes not only the design of the RF PA extremely challenging but also less benefits on the power consumption and linearity (W-CDMA transmitter employs linear modulation scheme [32]). Instead, by distributing the 74dB power variation to the several blocks before the PA could actually relax the design requirements on the PA and result in a power-efficient transmitter. Therefore RF variable gain amplifier (VGA) becomes an essential block for W-CDMA transmitter to achieve the demanding power-variation task. In this work the required transmitter power control range can be achieved in two separate stages with 50dB from RF VGA and the rest from the sigma-delta IF stage. The design specifications for the RF VGA are listed in Table 5.1. Note that the 2.4GHz WLAN 802.11g band is also included in RF VGA design specifications. Since the WLAN 802.11g transmitter band is not far from W-CDMA transmit band and it requires less power variation compared to that of the W-CDMA, by adding some tunable circuits, one RF VGA can easily support two standards which could potentially be useful for multi-band multi-mode software defined transmitters.

Table 5.1: RF VGA design specifications

Parameters	Specifications
Operation frequency bands	1920 – 1980MHz (W-CDMA) 2400 – 2483.5MHz (WLAN 802.11g)*
Maximum output power	0dBm (with 5dB back-off)
Power range	-50dBm to 0dBm
Power step	10 dB
Dynamic range	50dB from -40dB to 10dB
Power step tolerance	+/- 2dB
Temperature variation	+/- 2dB
Output impedance	100 ohm matching to 50 ohm load using off-chip 2:1 balun.

(* WLAN is optional.)

Recently many VGA designs have been reported [24]-[28]. The VGAs in [24]-[27] are realized using bipolar transistors (BJT) while the VGA in [28] is implemented in the CMOS technology. Except for the VGA in [4], which utilizes the so-called current-bleeding method, the implementations of the linear gain range are achieved unanimously by using variable g_m topology. By changing the bias current I_b of the input transistor or transistor pair, the transconductances g_m of these transistors are changed accordingly. Because the gain of the VGA is proportional to g_m, the gain variation is obtained by modulating the devices transconductances. In this approach, the key for a wide linear-in-dB gain range is to keep the BJTs operating in the active region and the CMOS transistors in the

subthreshold region. Indeed, when the transistors work in those regions, the bias current $I_{b,}$ can be generated by a variable voltage V_{ctrl} and follows an exponential relationship:

$$I_b \propto exp(V_{ctrl}) \tag{5.1}$$

Note that g_m of the transistor is proportional to the bias current I_b. Therefore, g_m is proportional to $exp(V_{ctrl})$ and the gain is linear with V_{ctrl} in the log scale. The advantages of this topology are the low supply voltage and the low power consumption. However, for high-speed applications, such as RF VGA at GHz range and beyond, the CMOS implementation does not perform well because of the poor f_t (MOSFET transition frequency) of subthreshold MOS transistor. Therefore the CMOS variable g_m topology is only limited to the intermediate frequency (IF) applications.

In order to meet specifications listed in Table 5.1 while keeping the design compact, a new CMOS RF VGA topology needs to be developed to support the specifications. In this work a single-stage discrete-power-step VGA for two frequency bands is proposed. The design strategy is shown in Fig. 5.1.

As the RF VGA is a part of a digital transmitter, the gain-control signals are preferred to be done in digital domain to take advantage of digital signal processing in the baseband. In order to utilize one VGA for two frequency bands rather than two standalone variable gain amplifiers, switches are introduced in the input and output tunable LC networks to adaptively select the impedance values to match desired center frequencies, which is a similar scenarios used in [29]. To achieve a wide dynamic range, the VGA needs to adaptively attenuate large input

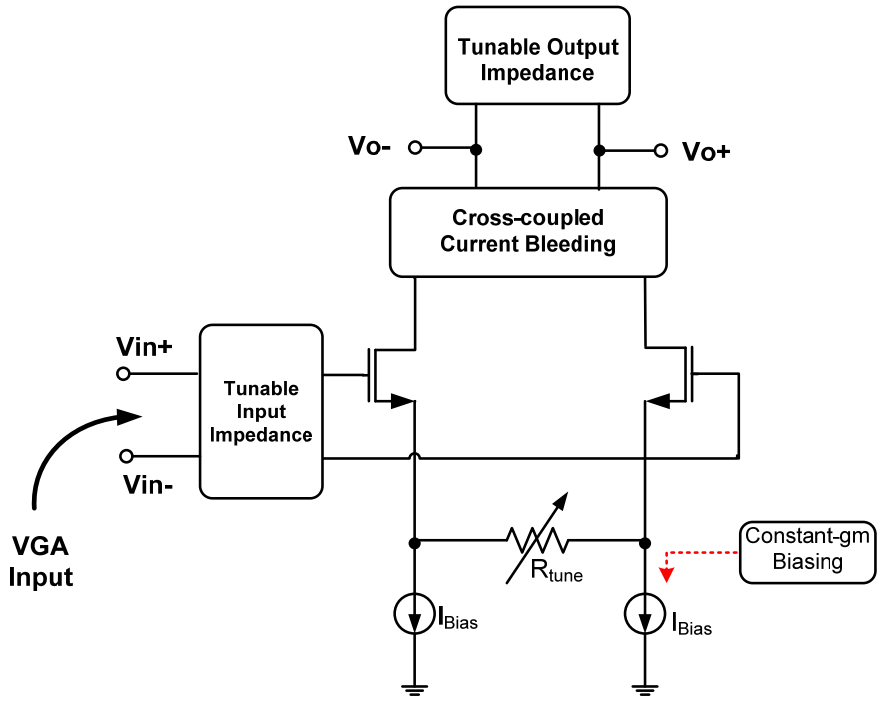


Figure 5.1: VGA design strategy

signal coming from the RF DAC/Mixer. This can be done by using resistor degeneration combined with current bleeding technique. Resistor degeneration is a common approach in VGA design to boost linearity. It can be realized by using MOS transistor, where the resistor value is controlled by the input signal at the gate [25] [30]. However, the control signal is analog. In this work a switchable poly resistor bank R_{tune} is adopted to replace the linear MOS resistors. In this way, the resistor value is controlled by the digital signals applied to the switches. The current bleeding technology is another attractive way to linearly attenuate the input signal. It has been reported in [22][24][28]. However, the control signals in [22][24][28] are still in the analog domain. In order to realize gain control signals all digital, switches are again introduced to selectively turn on and off transistor

pairs to control the amplitude of the output signal. Ideally the resistor degeneration approach should provide a large gain variation, however, in real circuitry implantation, it can only achieve limited attenuation due to the parasitics from the drain of the current source I_{Bias} and the switches used in the R_{tune}. By combining the switchable current bleeding and the resistor degeneration together, the desired attenuation can be achieved while the gain control signals are performed completely in the digital domain. As mentioned in Table 5.1, the VGA should not be sensitive to temperature variation, and constant-gm biasing [12] is famous for its robustness in temperature and simple to implement, therefore it has been used to bias the current source I_{Bias} in Fig. 5.1.

In summary, the design strategies of the proposed RF VGA can be highlighted as follows:

1) The operation frequency of W-CDMA band or WLAN band is determined by the input and output tunable impedances.

2) 50dB dynamic range is achieved by using the resistor degeneration method combined with the current-bleeding scheme. The gain step is controlled by the digital inputs.

3) A minimum gain variation over a large temperature range is guaranteed by a constant-gm biasing topology.

5.1 RF VGA frequency band selection

A tunable LC tank which performs 1st.-odrder band-pass filtering is used to select the desired center frequency. Higher-order filter could provide better

band selection, however for the CMOS technology used for this project it might not provide good performance due to the loss in the CMOS inductors and MOS switches in series with the capacitors. Moreover, higher-order filters result in bulky devices that either collect or inject disturbances from and through the substrate. Also, it consumes more die area. Therefore, a 1st-order LC band-pass filter is the optimal solution to perform the band selection task in monolithic applications for the current process. Theoretically, by either changing inductor and/or capacitor values, the resonant frequency will be changed accordingly. However, the design of variable capacitors is easier to implement compared to the design of variable inductors, either by using varactor (one MOS transistor) or switchable capacitors (capacitor bank). Therefore in this work variable capacitor method is adopted and the frequency band selection is realized by adjusting capacitor values while keeping the inductance at a fixed number as shown in Fig. 5.2(a). The frequency response of the tunable LC tank is illustrated in Fig. 5.2(b). From Fig.5.2, the smaller capacitance is, the higher resonant frequency will result. Note that the inductor value is not chosen arbitrarily. Indeed, monolithic inductors with different values and geometries have different quality factors (Q–factor). It is well-known that Q-factor of the LC tank at the resonant frequency defines the 3-dB signal bandwidth (BW) [31]. In order to have enough BW, Q-factor is chosen to be close to 10. In the real circuitry, there are other devices around the LC tank. Unfortunately, these devices contribute parasitics as well. At the resonant frequency, the capacitor in the LC tank should absorb all the parasitic capacitances both at the input and output, in other words, at the resonant

frequency the input and output impedances only see their real parts.

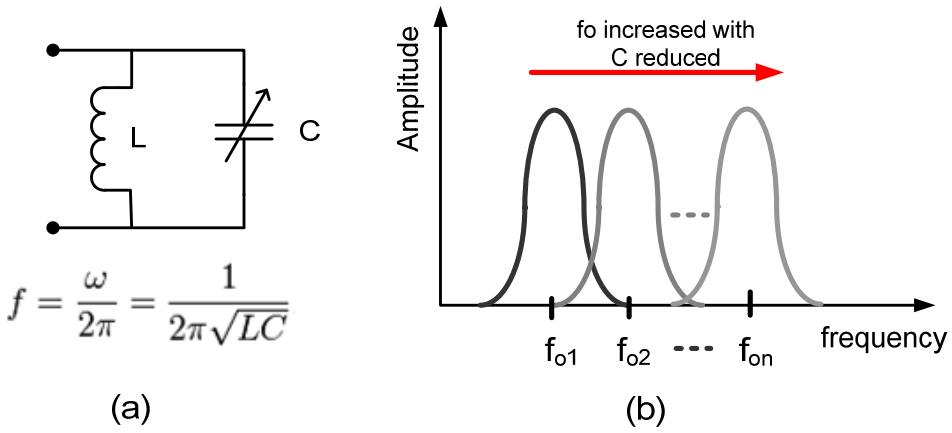


Figure 5.2: (a) Tunable LC tank (b) Frequency response of tunable LC tank

5.2 Wide linear dynamic range

In order to amplify the signal with little or no distortion, the VGA needs to be a linear amplifier. For an ideal linear system, the input and output signals have the following relationship

$$y(t) = k * x(t) \tag{5.2}$$

where *x(t)* and *y(t)* are the input and output signals respectively, and *k* is a constant. It means that the input and output signals keep the same shape. When plotted in time-domain, it should demonstrate a straight line with a certain slope as shown in Fig. 5.3. However, the amplifier can be modeled as a linear block only under the condition of the small-signal input. When the input signal gets larger, the small-signal assumption might not be true any longer and the gain of the amplifier starts to drop. This effect can be described as "1-dB compression point" [12] as shown in Fig. 5.4. When plotted the output and input signals on a

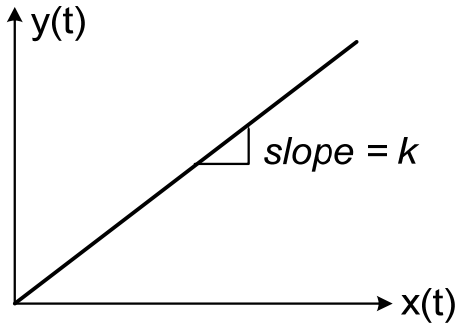


Figure 5.3: Graphic interpretation of a linear system

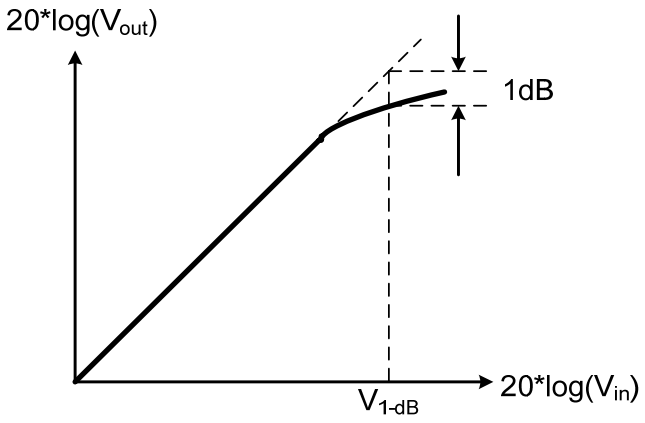


Figure 5.4: 1-dB compression point

log-log scale, at the 1-dB compression point, the output signal level drops 1dB from its linear value.

By using a variable resistor degeneration together with a cross-coupled current bleeding as shown in Fig. 5.5, the VGA not only shows good linearity but also achieve very wide dynamic range, which will be analyzed in detail in the following.

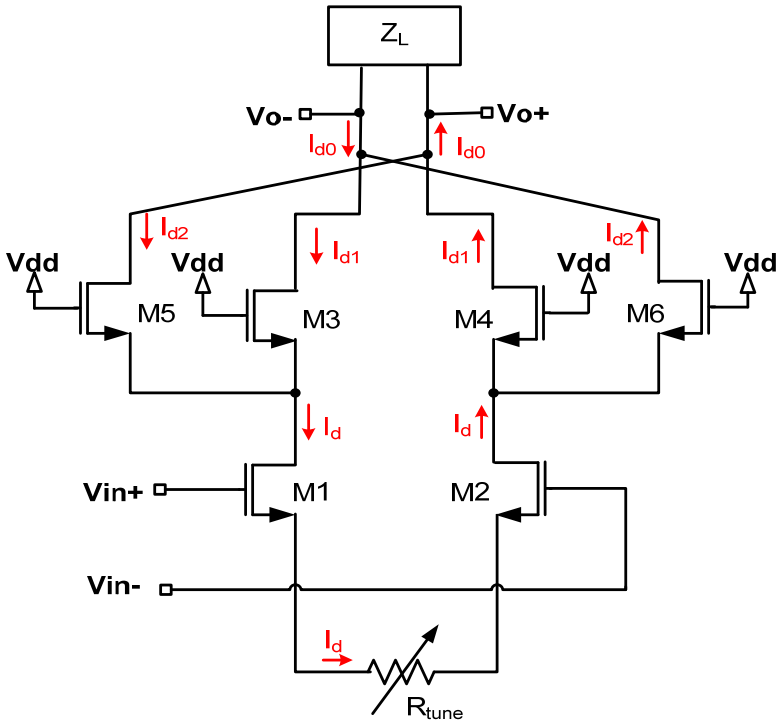


Figure 5.5: Resistor degeneration with the cross-coupled current bleeding

When only applying the resistor degeneration while deactivating current bleeding paths as shown in Fig. 5.6, the input voltage is converted to the ac current I_d by the transistors M_1 and M_2 following the equation

$$V_{in+} - V_{in-} = V_{gs1} + R_{tune} * I_d - V_{gs2} \tag{5.3}$$

Since

$$V_{gs1} = -V_{gs2} = \frac{I_d}{g_{m1}} = \frac{I_d}{g_{m2}} \tag{5.4}$$

where g_{m1} and g_{m2} are the transconductances of M_1 and M_2 respectively, and g_{m1}= g_{m2}. When substituting equation (5.4) into (5.3),

$$V_{in+} - V_{in-} = \left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}} + R_{tune}\right) * I_d \tag{5.5}$$

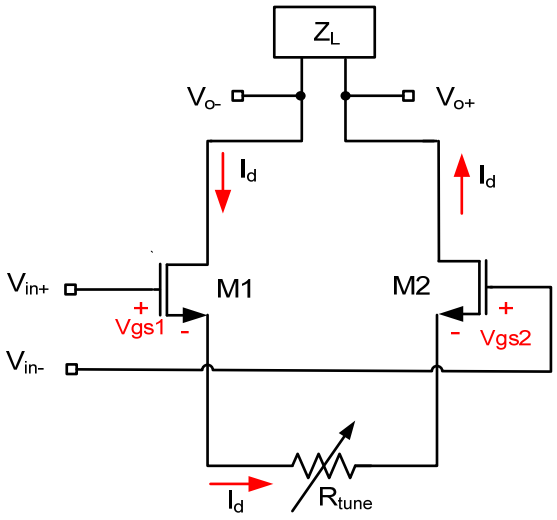


Figure 5.6: Resistor degeneration

and

$$V_{o+} - V_{o-} = Z_L * I_d \tag{5.6}$$

therefore,

$$Gain\_v = \frac{V_{o+} - V_{o-}}{V_{in+} - V_{in-}} = \frac{Z_L}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}} + R_{tune}} \tag{5.7}$$

From equation (5.7), the voltage gain *Gain_v* of the VGA is just an impedance ratio. Under the small-signal input condition, g_{m1} and g_{m2} are constant, and the output impedance Z_L and the degeneration resistor R_{tune} are also signal independent, so *Gain_v* is not dependent on the input signal, which means that the VGA is linear.

For a fixed input voltage, since the transconductances of M_1 / M_2 and Z_L are constant, the drain current I_d decreases with the increase of R_{tune}. As a result, the output voltage decreases accordingly due to less current flowing into the output load. Ideally, the resistor degeneration should provide very large gain

variation if the current source I_{Bias} shown in Fig. 5.1 and switches used in the R_{tune} were ideal. However, in reality the finite output impedance and parasitic capacitance of the current source limit the achievable gain variation range. Also the parasitics from the switches used for R_{tune} selection further shrink the gain range. In order to expand the gain variation transistors M_5 and M_6 are introduced to the cascoded differential pair and connected in a cross-coupled way as shown in Fig. 5.5. The advantage of using these two transistors is to provide additional signal cancellation paths to further reduce the ac current flowing into the output load, which could result in a huge attenuation. As illustrated in Fig. 5.5, when M_5 and M_6 are activated, the drain current of M_1 and M_2 is still I_d, which is equal to the sum of the drain current I_{d1} of M_3/M_4 and the drain current I_{d2} of M_5/M_6,

$$I_d = I_{d1} + I_{d2} \tag{5.8}$$

Due to the cross-coupled structure, the total output current I_{do} is

$$I_{do} = I_{d1} - I_{d2} \tag{5.9}$$

which can approach zero when I_{d1} is equal to I_{d2}, in other words, the infinite attenuation could be achieved as long as the drain currents I_{d1} and I_{d2} are the same. The current bleeding method is inherently linear as the final output current I_{do} is just a scaled version of I_d. The general gain equation for the RF VGA can be described as follows:

$$G_{VGA\_v} = N * \frac{Z_L}{\frac{2}{g_m} + R_{tune}} \tag{5.10}$$

where N is the attenuation factor from the current-bleeding scheme. By applying both the resistor degeneration and the cross-coupled current bleeding, the required

attenuation can be achieved without linearity degradation.

5.3 gm insensitive to temperature variation (constant gm biasing)

The constant-gm biasing circuit with the VGA current source and the input transistor is illustrated in Fig. 5.7. To simply the analysis, a single-ended version of VGA is presented. In this circuit, the transistors M_1 to M_4 and the resistor R_{ext}

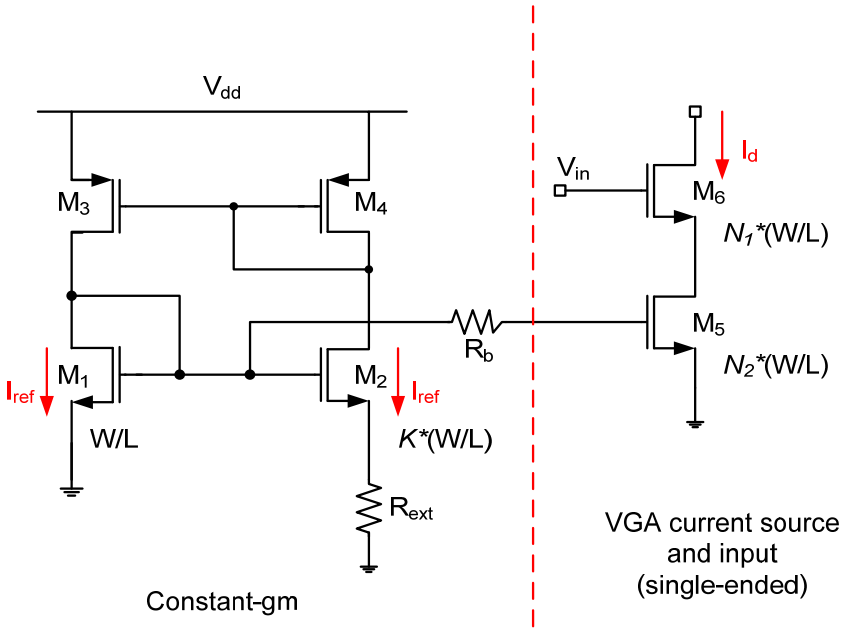


Figure 5.7: Constant-gm biasing circuit for RF VGA

make a constant-gm biasing circuitry. The transistor M_5 is used as a current source of the VGA, and the M_6 is the VGA input transistor. As shown in the Fig. 5.7, the transistors M_2, M_5 and M_6 are K, N_1 and N_2 times larger than the transistor M_1 respectively. The current I_{ref} is given by

$$I_{ref} = \frac{2}{\mu_n C_{ox}(W/L)} \frac{1}{R_{ext}{}^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2 \tag{5.11}$$

Since

$$I_d = N_1 * I_{ref} \tag{5.12}$$

and the transconductance of M_6 is

$$g_{m6} = \sqrt{2\mu_n C_{ox} N_2 * (W/L) I_d} \tag{5.13}$$

When substituting equations (5.11) and (5.12) into (5.13),

$$g_{m6} = \sqrt{2\mu_n C_{ox} N_1 * N_2 * (W/L) I_{ref}}$$

$$= \left(\frac{2N_1 * N_2}{R_{ext}}\right)\left(1 - \frac{1}{\sqrt{K}}\right) \tag{5.14}$$

From equation (5.14), the transconductance of the input transistor g_{m6} is determined by the transistor size ratios and R_{ext} rather than the transistor parameters and the supply voltage. If R_{ext} is temperature independent, then g_{m6} is robust to temperature variation. Since on-chip resistors are more sensitive to temperature and process variations than the off-chip ones, an off-chip resistor is used to implement R_{ext} in the design.

5.4 RF VGA circuit implementation

In the previous sections, RF VGA band selection, linear gain dynamic range and the temperature behavior have been analyzed. Fig. 5.8 shows the schematic diagram for the circuit implementation of the proposed VGA (constant-g_m biasing is not shown). Note that NMOS switches are used in the degeneration resistor bank while PMOS switch is used to control the current-bleeding path. For

the W-CDMA band, C_{VGA} is set about 1.13pF and is reduced down to 0.85pF at the WLAN band.

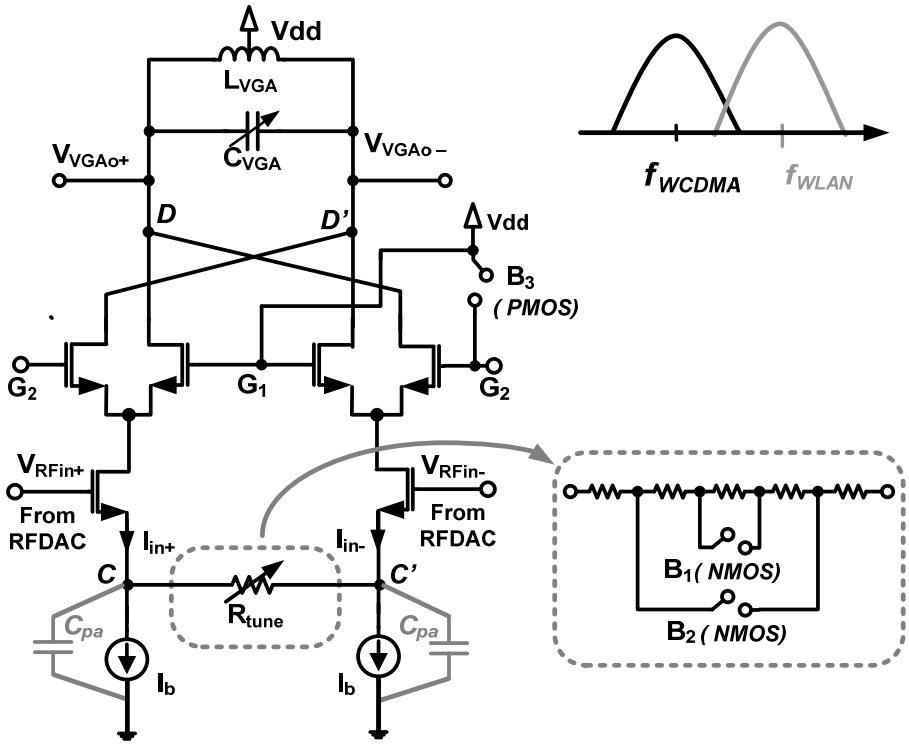


Figure 5.8: Schematic diagram of the proposed VGA

5.5 RF VGA simulation results and layout

5.5.1 Input and output LC tank frequency response

Figs 5.9 and 5.10 show the frequency response of the tunable LC tanks at the RF VGA input and output respectively. As mentioned before, at the resonate frequency the tank impedances only see their real parts where the imaginary parts are completely cancelled out. In Fig. 5.9, the imaginary of the input impedance approaches to zero at the designed frequencies of 1.95GHz for W-CDMA band and 2.42 GHz for WLAN band. Fig.5.10 shows that the VGA output return losses

are more than 12dB for both frequency bands, which guarantees a fair reasonable output matching to 50ohm load.

5.5.2 Linearity (OP1dB plot)

The OP1dB of RF VGA in the W-CDMA mode is illustrated in Fig. 5.11. From the plot, the OP1dB of 6.5dBm can be achieved, which means the designed VGA is linear at the targeted maximum 0dBm output power, and leaves enough at least 6dB margin for power back-off as well. RF VGA for WLAN mode is ignored here because as long as the RF VGA satisfies the linearity requirement for WCDMA, it will guarantee the linearity requirement for 2.4 GHz WLAN with no effort.

5.5.3 Power steps for different input bit settings at 27°C

The power steps vs. different bit inputs are shown in Fig. 5.12. In the plot, B1 to B3 are the digital control signals applied to the switches used in the resistor bank and the cross-coupled current bleeding part as shown in Fig. 5.8. From the plot, 50dB linear gain range is clearly demonstrated. Also the simulated power steps just slightly deviate from their ideal values, but still within the range of +/- 1dB. The power steps at 2.42 GHz are almost 2dB higher than those at 1.95 GHz, which means that less input power is required to achieve 0dBm for the WLAN band

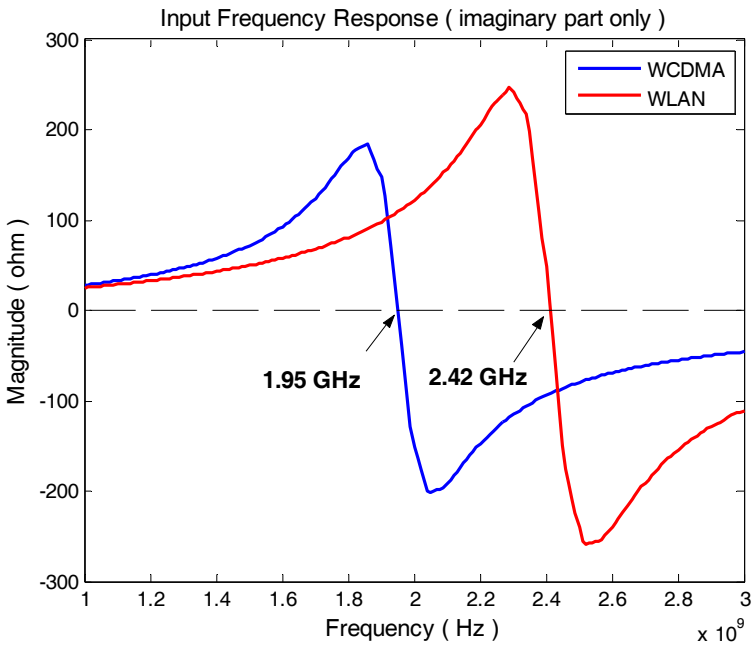


Figure 5.9: RF VGA Input frequency response (imaginary part only)

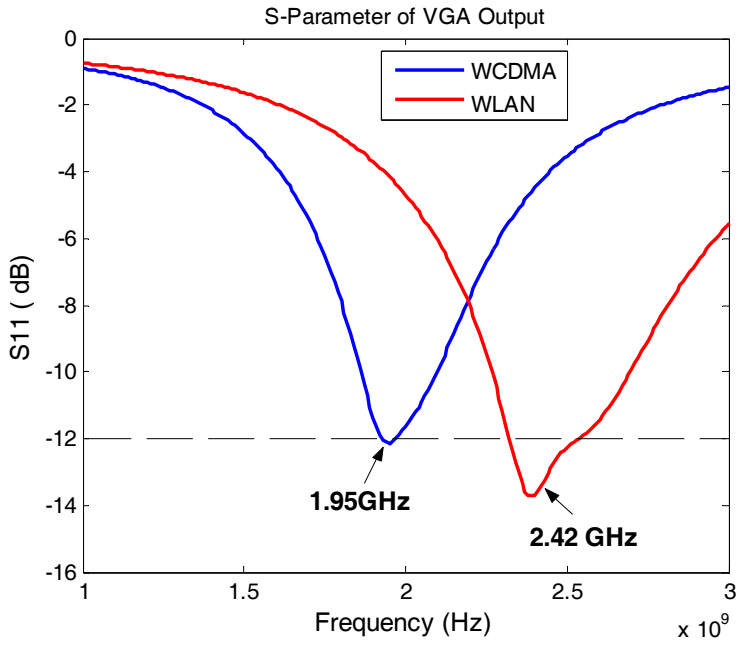


Figure 5.10: RF VGA Output return loss based on 50 ohm load matching

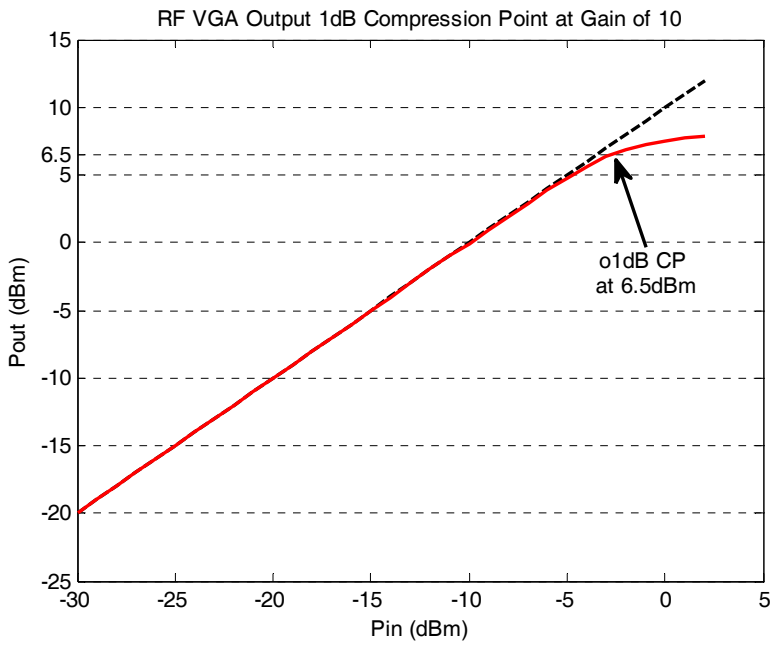


Figure 5.11: OP1dB of RFVGA for W-CDMA

5.5.4 RF VGA output power variation over temperature

The temperature simulation results are plotted in Figs. 5.13. Since only W-CDMA requires stringent power steps, the power steps over temperature simulation is recorded only for the W-CDMA. Thanks to the constant-g_m biasing topology, the power-step deviations are kept within +/-1 dB at 1.95 GHz over the temperature range from -31°C to 85°C compared to those at 27°C.

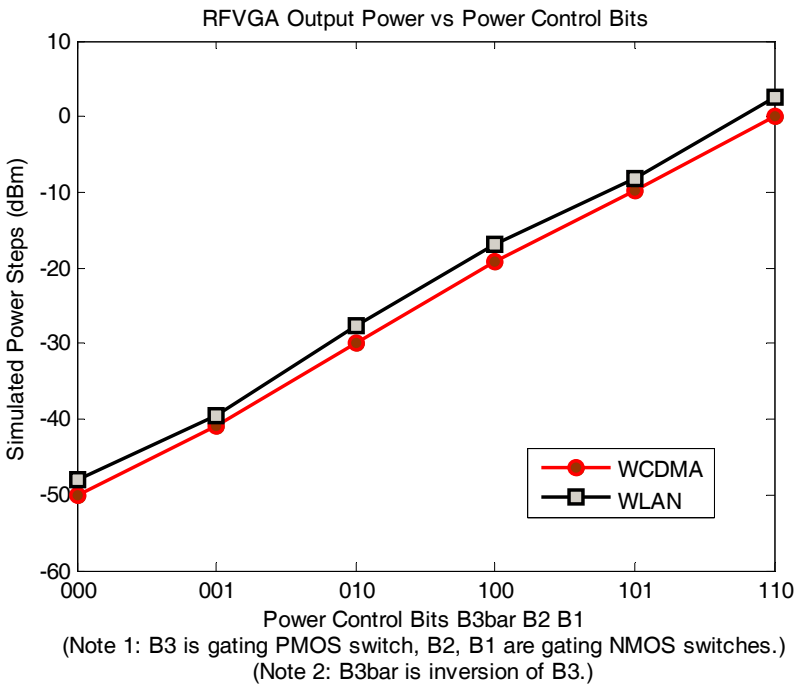


Figure 5.12: Power steps vs. different bits

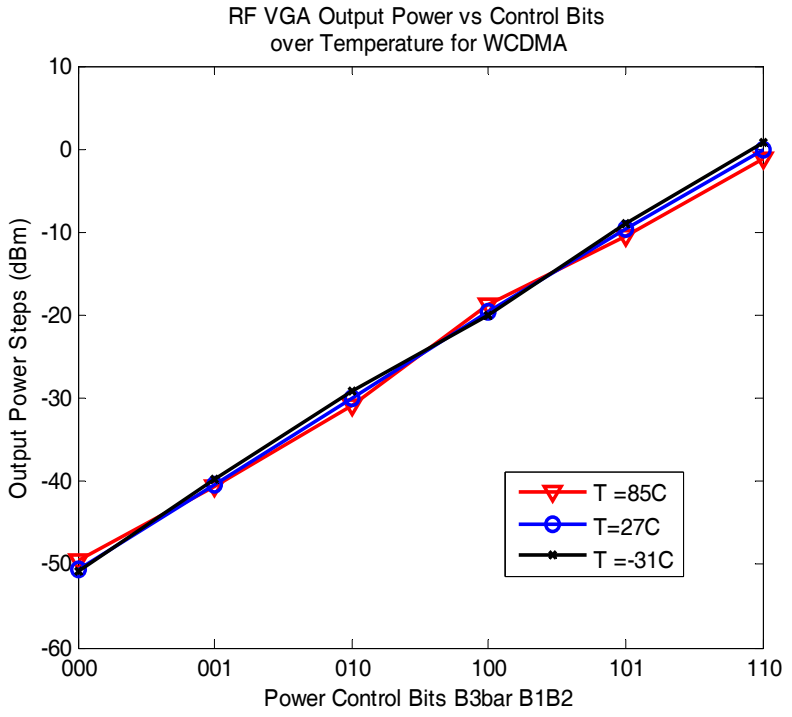


Figure 5.13: Power step vs. control bits at -31°C, 27°C, 85°C (W-CDMA)

5.5.5 RF VGA chip layout

The chip is fabricated using 0.18µm IBM7RF CMOS technology. Fig. 5.14 shows the layout of the designed RF VGA. The VGA itself consumes about 0.83µm^2 die area.

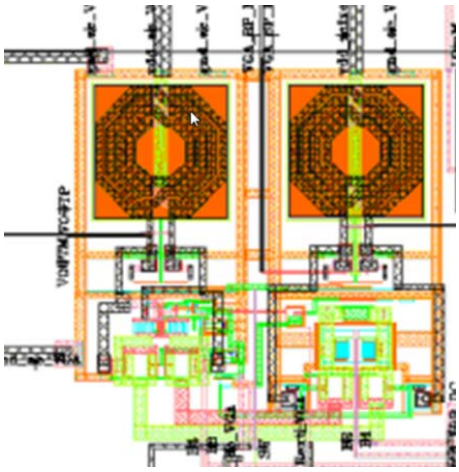


Figure 5.14: Layout of designed RF VGA

From Fig. 5.14, the input and output inductors located on the top occupy a big chunk of the VGA area. This is due to the 0.18µm CMOS technology used for this work. If 0.13µm CMOS technology or more advanced technologies were used, the inductor layout area would be much smaller.

5.6 Summary

The simulated performances of the proposed RF VGA are summarized in Table 5.2. The RF VGA is an essential block for wireless transmitters utilizing linear modulation scheme, such as WCDMA and WLAN transmitters. In this chapter a new compact CMOS RF VGA for W-CDMA with an option for WLAN

Table 5.2: RF VGA performance summaries

Parameters	Simulation Results
Operation frequency	1.95 GHz for W-CDMA 2.42 GHz for WLAN
Power supply voltage	1.8 V
Current consumption	< 36 mA at max. output power
Maximum output power	6.5 dBm
Output power range	-50 to 0dBm
Power step	10dB
Dynamic range	50dB from -40dB to 10dB
power step deviation	Max. +/- 1dB
Temperature variation	Max. +/- 1dB
Output impedance	50 ohm
Current consumption	53mA @ 0dBm

802.11g is proposed based on the comparison of the VGAs in recent papers. The VGA utilizes the resistor degeneration and the cross-coupled current bleeding to achieve a wide linear dynamic range to satisfy the demanding linearity requirement mainly from the 2GHz W-CDMA transmitter. Tunable input and output impedances are adopted to selectively cover W-CDMA or WLAN transmit frequency bands. Constant-g_m biasing is used to minimize gain variation over a large temperature range of -31°C to 85°C. By using MOS switches in the degeneration resistor bank and the current bleeding paths, the gain control signals

are performed completely in the digital domain. Simulation results shows that the proposed VGA can provide 50dB dynamic range with 10dB step with the maximum step deviation of +/- 1dB. Fine gain control of 1-dB step is obtained in the ΣΔ digital IF generator to minimize phase and gain discontinuity in the modulated signal. Also the design is robust to temperature variation. The VGA achieves an output 1dB compression point as high as +6.5dBm and OIP3 of 16dBm at the maximum gain of 10. With the rest of dynamic range from the digital IF stage, a total of 74dB dynamic range demanded by 2GHz W-CDMA can be achieved. The designed RF VGA utilizes 0.18μm IBM7RF CMOS technology and it consumes approximately 53mA at the maximum gain of 10 and utilizes $0.83\mu m^2$ die area.

CHAPTER 6

EXPERIMENTAL RESULTS

The proposed transmitter design is fabricated on a 0.18μm CMOS process. The chip measurement setup with die photo is shown in Figure 6.1. The design occupies a 1.28-mm^2 die area. In order to minimize the coupling between the digital and analog signals, the digital inputs are located at the opposite end of the IC with respect to the RF output and LO inputs are orthogonal to the RF VGA output as shown in Figure 6.1. Moreover, multiple ground bonding wires are used to reduce parasitic inductance impact on circuit stability and performance. As shown in Figure 6.1, the digital IF bits are externally supplied and re-timed with an internal clock, which is derived from the LO frequency. The input LO signal is a single-tone at 2.027GHz and applied to the chip through an off-chip impedance matching network. The differential RF output is transformed to the single-ended signal through an on-board 2:1 balun, and then applied to the 50Ω instrumentation inputs through the 50Ω microstrip transmission line.

Figure 6.2 shows the ideal FIR frequency response along with filtered BP sigma-delta spectrum and compared to the measured carrier at 2.06GHz. A minimum 40dB out-of-band quantization noise suppression can be achieved after FIR filtering. Figure 6.3 shows the two-tone test performance. A two-tone digital IF signal is applied with 1MHz offset. The measured IMD3 is -52dBc, which meets the specifications according to the calculation and simulations in the transmitter link budget analysis in Section 2. Figure 6.4 shows the image rejection of -33dBc can be achieved.

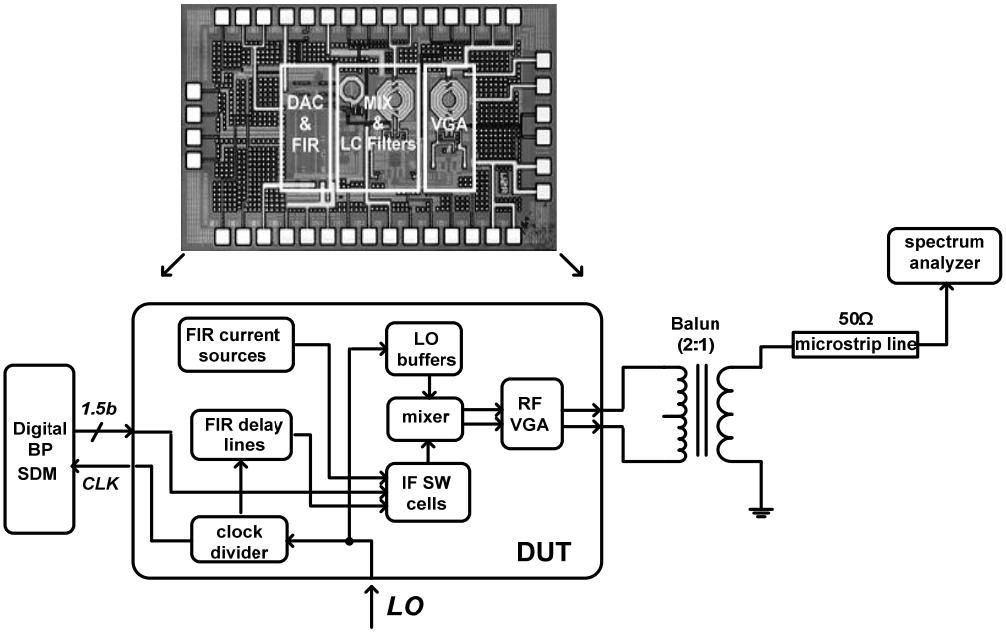


Figure 6.1: Measurement setup for the proposed design

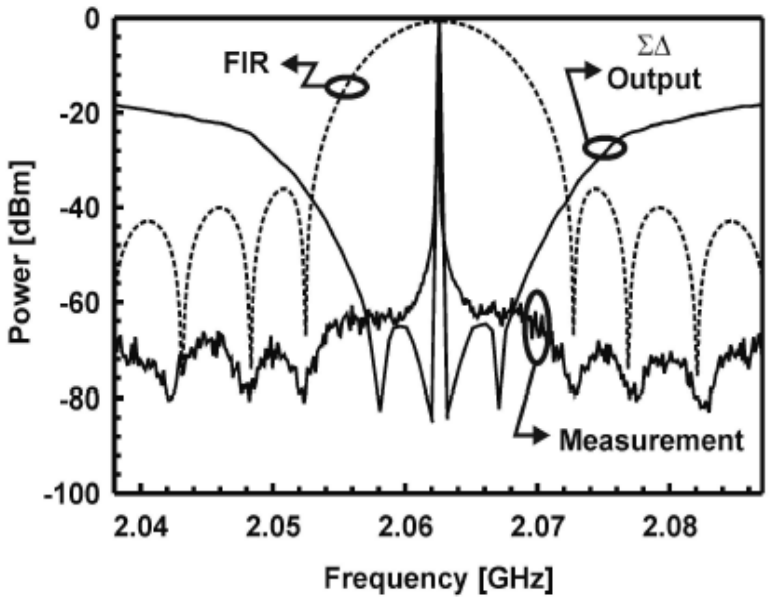


Figure 6.2: Ideal BP FIR response, BP ΣΔ modulated signal and measured single-tone spectrum

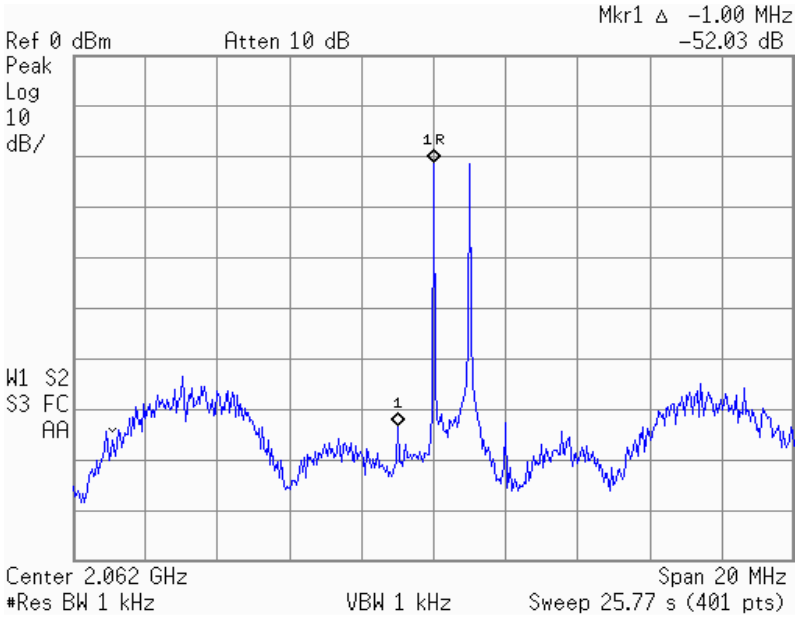


Figure 6.3: Measured IMD3 performance based on the two-tone test

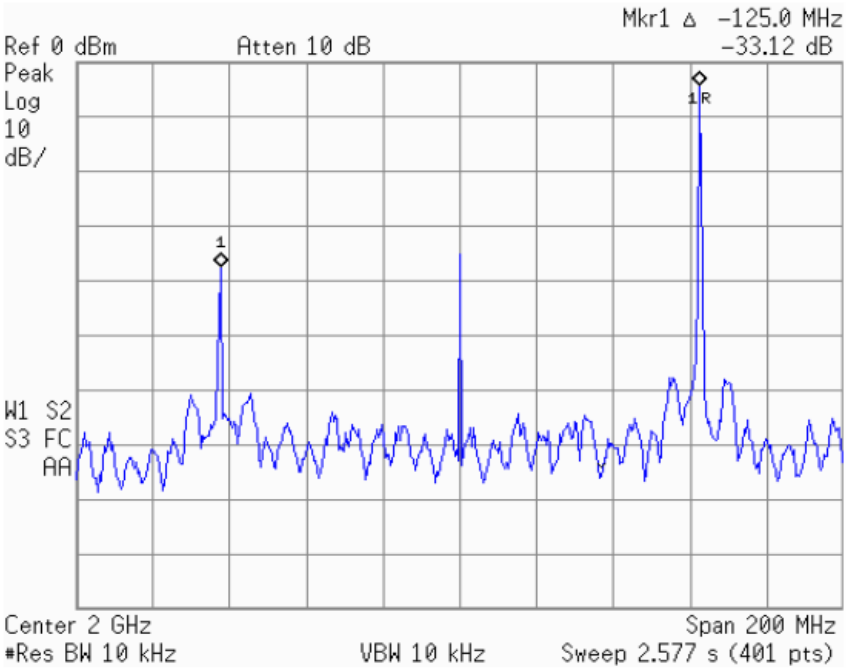


Figure 6.4: Measured image rejection result

The total power control provided by this work is about 74 dB which 50-dB gain control is from RF VGA and the rest is provided by the digital IF stage. The RF VGA controls the output power with 10-dB step with the accuracy of ±1 dB. The fine power control is implemented by scaling the digital IF at the RF DAC input to minimize the parasitic effect on the phase. A 10-dB maximum power control range is achieved without degradation on the linearity. The power control characteristic of the RFDAC transmitter is shown in Figure 6.5.

Figure 6.6 shows the measured W-CDMA output spectrum centered at 2.0626 GHz. The chip achieves -35dBc ACPR at 5MHz offset and -50dBc at 10MHz offset, which meets the W-CDMA ACPR requirements. The measured rms EVM result is less than 4.8% as shown in Figure 6.7. The measured ACPR performance at the first channel offset is close to -33dBc specification, this is partially due to the non-linearity of the bench board. If the bench board is probably characterized, a 2 to 3dB improvement at 5MHz offset can be achieved. The further noise reduction at first channel offset can be improved by optimizing FIR filter coefficients and/or using longer FIR filter to provide sharper roll-off at the first and second side lobes to leave more safety margin for the RF PA stage.

Table 6.1 summarizes the performances of the proposed digital IF to RFDAC transmitter for 2GHz W-CDMA band. Table 6.2 lists the major specifications and performances of the RFDAC architectures reported to date.

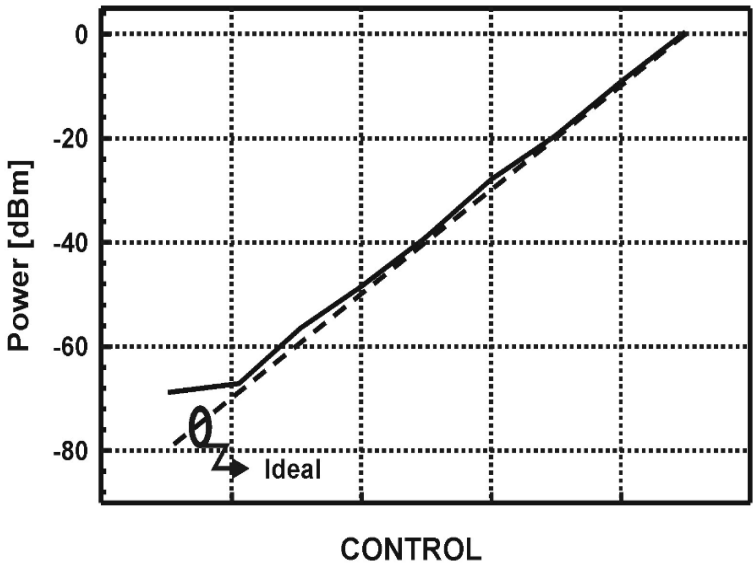


Figure 6.5: Measured power variation of the proposed transmitter (CONTROL is from the DSP in the transmitter)

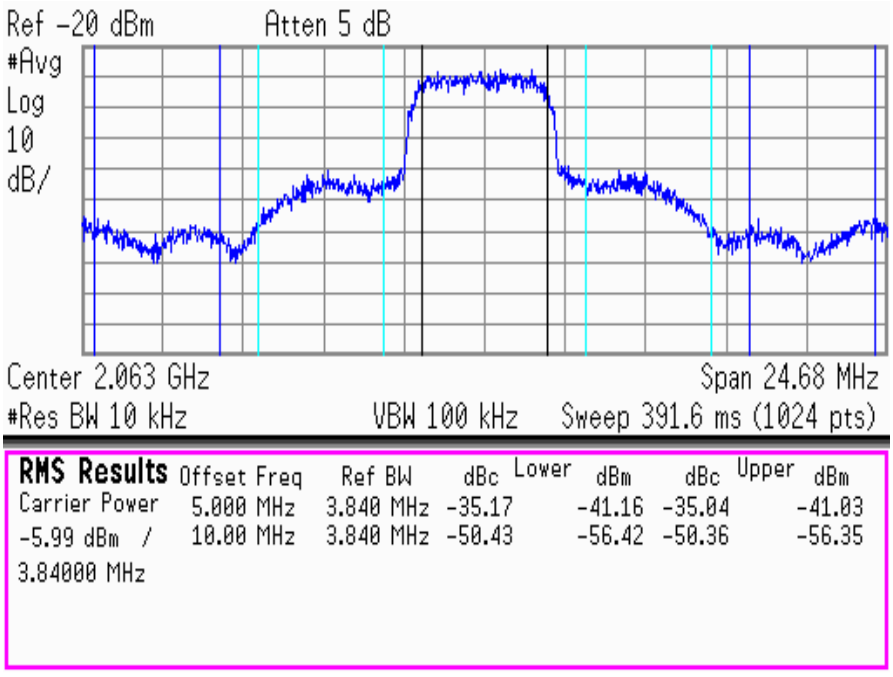


Figure 6.6: Measured W-CDMA ACPR performances

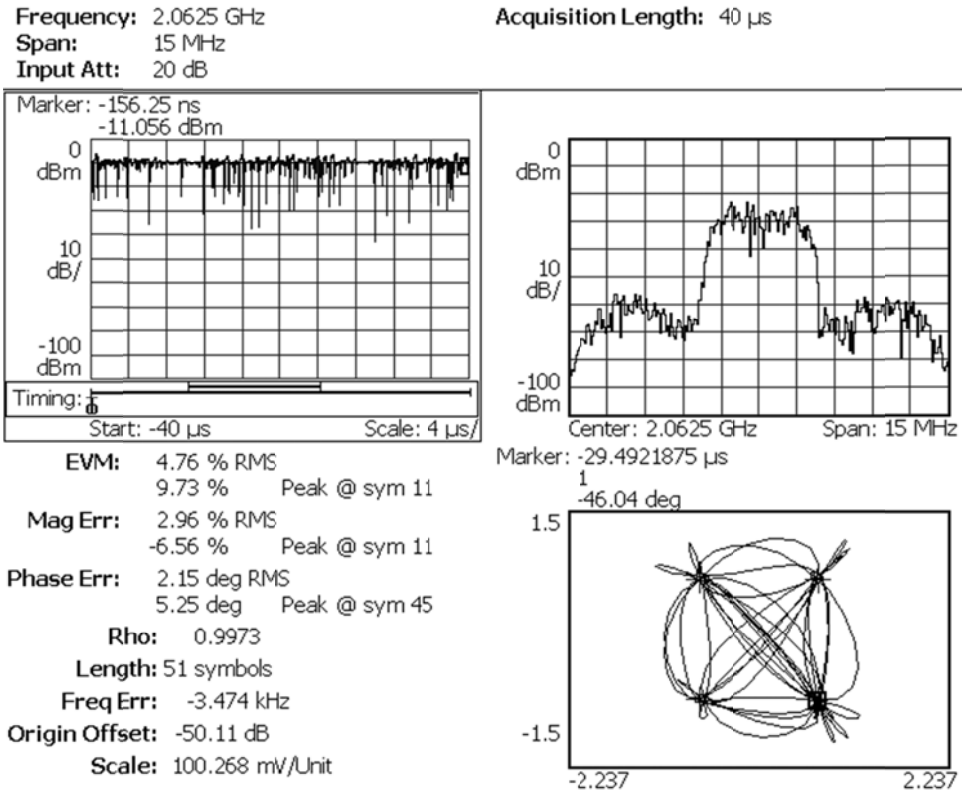


Figure 6.7: Measured rms EVM performance

Table 6.1: Summary of the measured performances

Technology	IBM 0.18µm CMOS, 4M, 1.8V
Center frequency	2 GHz
IMD3	-52dBc
Image rejection	-33 dB
ACPR	-35dBc @ 5MHz offset -50dBc @ 10MHz offset
EVM	< 4.8 %
Power variation	74 dB

Table 6.2: Summaries of the specifications and performances of the RFDAC architectures

Publication	Ref. [4]	Ref. [2]	Ref. [3]	This work
Process	CMOS 0.13μm	CMOS 0.18μm	CMOS 0.25μm	CMOS 0.18μm
Supply voltage (V)	1.2	1.8	2.5	1.8
Center Freq (GHz)	1.9 (WCDMA) 2.4 (WLAN)	0.9	1	2 (WCDMA)
Mode	Dual	Single	Single	Single
Main Blocks	Digital RF Modulator	Digital RF Modulator	Digital RF Modulator + FIR Filter	Digital RF Modulator + FIR Filter + RF VGA
DAC Bits	8	8	1	1.5
Sampling Freq (MHz)	--	514	125	250
SNR (dB)	60 (WCDMA) 44 (WLAN)	53	67	50
Bandwidth (MHz)	60 (WCDMA) 100 (WLAN)	17.5	10	50
Pout (dBm)	-10 (WCDMA) -23.6 (WLAN)	--	--	0
Power consumption (mW)	65	18	125	223
Die area (mm2)	0.7	--	0.23	1.28

CHAPTER 7

EXTENDED APPLICATIONS

A highly digital-intensive sigma-delta modulated IF to RF DAC transmitter has been presented in the previous chapters. The presented architecture not only shows good linearity and low power consumption but also features architectural flexibility which could potentially be reconfigured for other wide-band wireless mobile standards, such as 2.4GHz WLAN 802.11g, with maximum circuit reuse.

The circuit reconfigurability has already been demonstrated in chapter 3, chapter 4 and chapter 5 in terms of FIR filter, RF upconverter and RF VGA. Moreover, the SDM-based digital transmitter can be potentially extended from the Cartesian to polar coordinates to make on-chip CMOS high-power amplification for wide-band wireless mobile standards possible which is the main focus of this chapter.

7.1 Introduction

With the increasing demand for high data-rate transmission in recent mobile communications, the base band modulations have evolved from constant modulation schemes (such as GMSK used in the GSM standard) to the non-constant envelop modulation schemes (such as $\pi/4$-QPSK used in W-CDMA and 64-QAM used in WLAN). Non-constant modulation schemes increases the spectral efficiency with enhanced data rate but traditionally they require linear

amplifiers such class A, class B or class AB amplifiers to boost the transmitted signal power with minimum distortion, which results in a low efficient device and a lot of power is wasted in the power amplification stage. Envelope elimination and restoration (EER) technique provides a way to use high efficient non-linear amplifier such as switch-mode class E, class F amplifiers, while maintain qualified spectrum at the radio frequency. Basically EER is a technique belongs to the polar transmitter category. Recently many works published based on the polar transmitter architecture, such as supply modulator and digital polar transmitter [33][34][37]. Supply modulator has the advantage of improved linearity with large power back-off, but the drawback of this architecture is the limited signal bandwidth (around 1MHz) due to the analog low-pass filter in the envelope path. Moreover, there is a low-frequency inductor which is still realized off-chip due to the technology limitation. Digital polar transmitter reported in [34] provides a solution for wide-band signal amplification but it complicated the design of power amplifier stage, especially in order to reduce digital images, linear interpolation is adopted which results in a large number of power amplifiers. Furthermore, the architecture still utilizes an off-chip balun which increases power consumption, cost and area. In order to overcome the drawbacks in [34][37], a highly integrated, high efficiency, low-voltage wide-band transmitter solution for wireless communication using CMOS technology is proposed. This is achieved through digital polar modulator and parallel amplification technique to reduce circuit complexities with added power efficiency. The proposed architecture can take full advantage of CMOS scaling and low cost digital CMOS process.

7.2 Proposed digital polar transmitter

Figure 7.1 shows the proposed digital polar transmitter architecture. The baseband I /Q signals are first decomposed into baseband amplitude and phase information through rectangular to polar transformation. Then, the baseband amplitude signal sends to the 1-bit oversampled sigma-delta analog to digital converter (ADC) to generate single-bit envelope bit streams. The out-of-band quantization noise due to the sigma-delta noise-shaping is suppressed by the embedded semi-digital FIR filter which is composed of a delay line, gain (FIR coefficients) and summing stages. The delay line is located in the envelop path, and the order of the FIR filter determines the number of the power amplifiers being used. The FIR coefficients and the summing stage are embedded in the PA stages as well as their matching networks. The 1-bit SDM bit streams feed to the FIR delay line to form a FIR-delayed single-bit envelop bits. The baseband phase information is up-converted to RF and then passes through a limiter to generate constant-envelope phase-modulated RF signal to drive a parallel power amplifiers which are modulated by the FIR-delayed envelope bit streams. The envelope and phase are restored at the PA stage. The output of the individual PA is summed to drive 50 ohm load directly. Since the envelop information is located in the low frequency range, a low-pass sigma-delta ADC is utilized in the envelope path. Single bit is adopted to take full advantage of its inherent linearity. The order of the ADC and the oversampling ratio (OSR) are determined based on the in-band SNR requirement. Since the ADC is only one bit, the OSR will be increased to meet the same SNR requirement compared to the multi-bit case if the same order

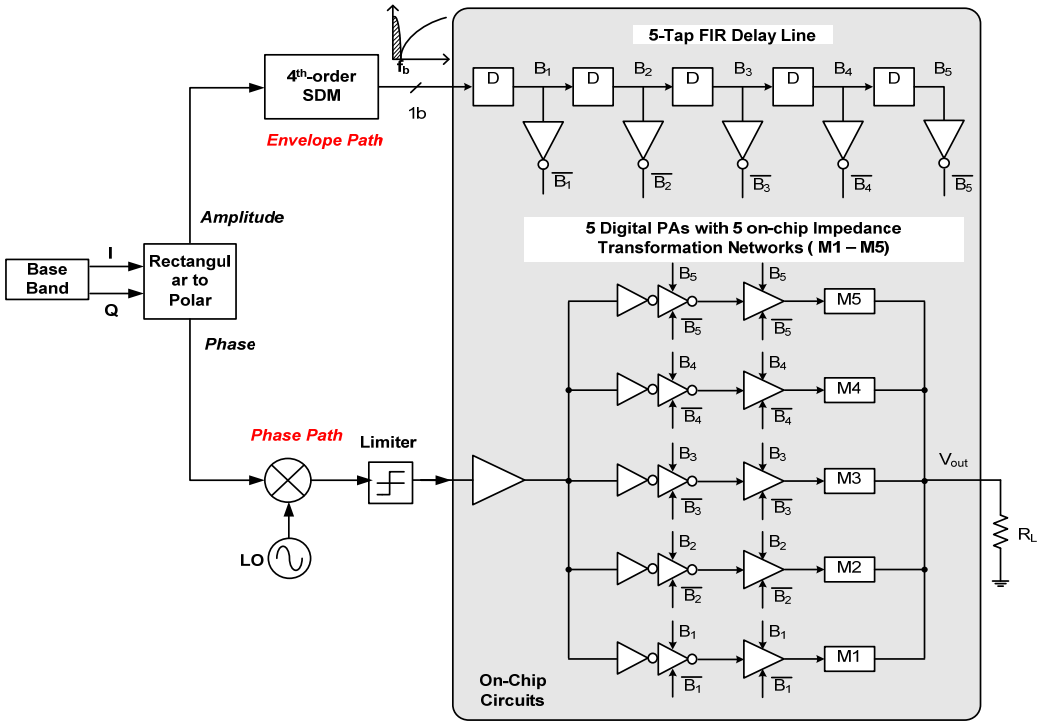


Figure 7.1: Proposed digital polar transmitter architecture

is used. But if a multi-bit ADC is used, the OSR can be reduced with the same loop filter order, but the linearity in the envelop path will be degraded and the number of the power amplifiers will be increased by the factor of 2^N, where N is the quantizer bit number [34]. With the CMOS technology further scaling down, we believe single-bit SDM with relatively high OSR is an attractive approach.

The proposed architecture offers four advantages as follows: first of all, it can use the parallel amplification technique to boost output power with reduced drain voltage of individual amplifier, thus allowing to use low-cost low-voltage CMOS transistor in the final stage of high power amplification (for example, transmitted power of +26dBm). Second, in this architecture, the number of power

amplifier is equivalent to the filter order, therefore, the number of PA can be extremely reduced if we can keep the filter order low without sacrificing the performance, which makes the individual power matching at the output of each PA possible, hence improved power efficiency due to low power enhancement ratio in each matching circuit [36]. Third, as individual impedance transformation is allowed at the output of each of the power amplifier, a LC-balun can be used on-chip to eliminate a standalone off-chip one, which improve the integration level [35]. Fourth, as high oversampling frequency is adopted in the envelope path, the digital images are pushed far away from the transmission band. Moreover, with embedded FIR filtering, the digital images which could be located in the receiver bands are null out due to FIR filter frequency response.

7.3 System design of the proposed digital polar transmitter

In this section, the system design of the proposed digital polar transmitter is presented in terms of wide-band single-bit sigma-delta modulator, 5-tap FIR filter and on-chip high efficient power combining.

7.3.1 Wideband single-bit sigma-delta modulator

Linearity in the digital envelope path is crucial for the overall linearity of the transmitter. From the system level simulation, in-band signal-to-noise ratio (SNR) in the envelope path needs to be at least 36 dB if a 5MHz-channel bandwidth W-CDMA signal is adopted, which is equivalent to at least 6-bit resolution. Single-bit oversampling sigma-delta modulator (OS SDM) has the advantage of inherent linearity while the SNR is determined by the order and the

oversampling ratio of the SDM. Another advantage of single-bit OS SDM is that it provides a way to reduce the complexity in the digital power amplifier implementation and allow efficient on-chip power combining. However, for 1-bit OS SDM, in order to achieve min. 36 dB SNR, one can either use large SDM order with low oversampling ratio (OSR) or vise verse. Since stability is always an issue for higher order OS SDM, one needs to keep SDM order low as low as possible. In the propose architecture, a 1-bit 4^{th}-order SDM is preferred which will be explained next.

In order to take the advantage of high-efficient on-chip individual power matching at each power amplifier output and to save die area, one needs to keep the number of power amplifiers low, hence low FIR filter order. If the signal bandwidth of SDM is set close to channel bandwidth, higher order FIR filter is inevitable to reduce the out-of-band quantization noise otherwise ACPR performance will be degraded. There is always a trade-off between FIR filter order and ACPR and spurious emission performance. In order to keep low FIR filter order while maintain ACRP and spurious emission within standard margin, the signal bandwidth of the SDM needs to be extended. For example, for UMTS W-CDMA transmitted signal with channel bandwidth of 5MHz, the SDM signal bandwidth is expanded close to 30MHz which is half of W-CDMA band. As long as high SNR is maintained during the 30MHz span, the FIR filter design is just to take care of out-of-band quantization noise and spurs, thus reduced order is achieved. In order to achieve high signal bandwidth, a 4^{th}-order 1-bit SDM is adopted to expand the signal by adding zeros in the signal transfer function. Fig.

7.2 shows the potential single-bit 4th.-order low-pass sigma-delta modulator using resonator feedback topology. In Fig. 2, g1 and g2 are in the feedback path to generate optimized zeros in the noise transfer function (NTF) and expand in-band signal bandwidth. The NTF of Fig. 2 can be expressed as follows:

$$NTZ(z) = \frac{1}{1 - L_1(z)} \tag{7.1}$$

$$L_1(z) = \frac{[a_1c_1c_2z + a_2c_2(z-1)] * c_3c_4z + [z^2 - (2 + g_1c_1)z + 1)] * [a_3c_3c_4z + a_4c_4(z-1)]}{[z^2 - (2 + g_1c_1)z + 1)] * [z^2 - (2 + g_2c_3)z + 1)]} \tag{7.2}$$

Fig. 7.3 illustrates the NTF frequency response of the sigma-delta modulator shown in Fig. 2 and expanded signal bandwidth is clear shown. Fig. 7.4 illustrates the simulated result of 1-bit wide-band SDM shown in Fig. 2. It can achieve the signal bandwidth of 33 MHz and SNR of 46.7 dB which is capable for W-CDMA digital polar transmitter application.

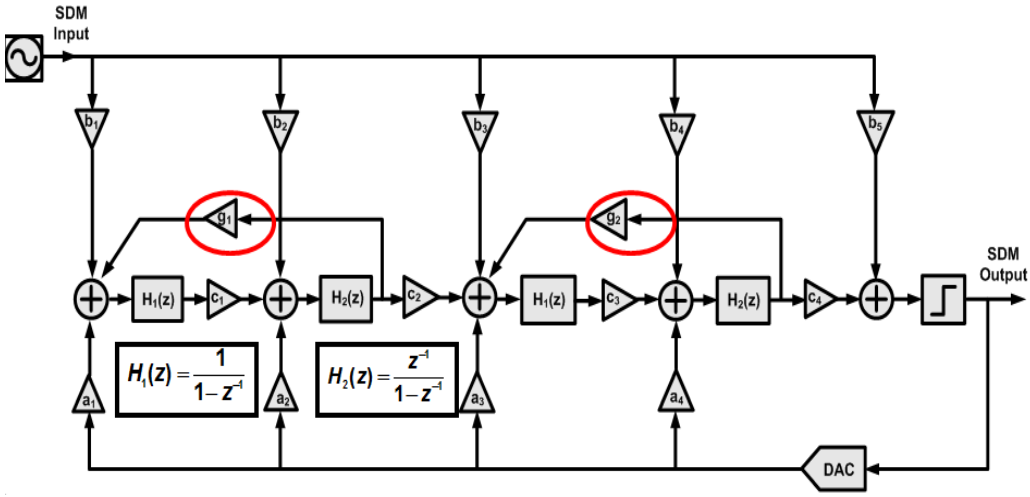


Figure 7.2: 1-bit 4th-order low-pass sigma-delta modulator with OSR = 5

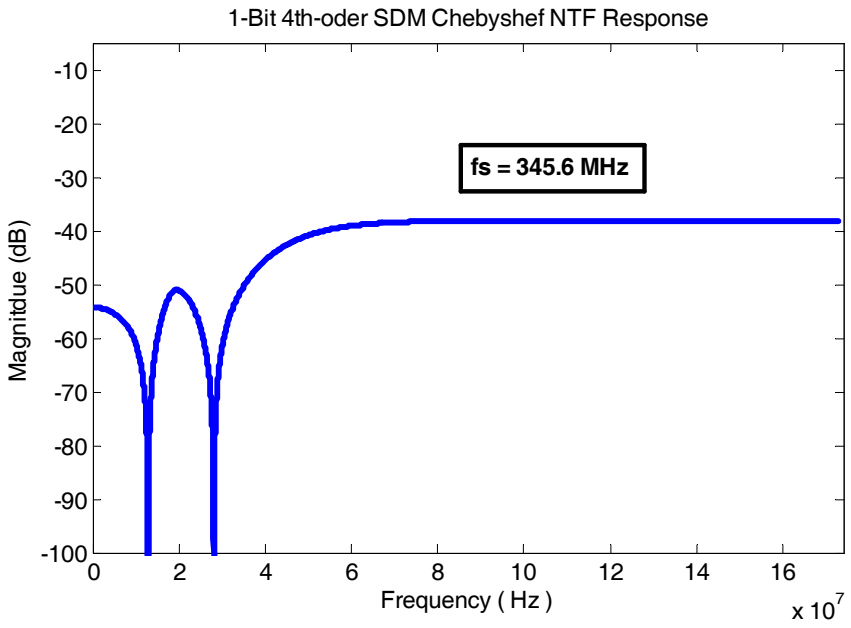


Figure 7.3: 1-bit 4th-order SDM Chebyshef NTF response

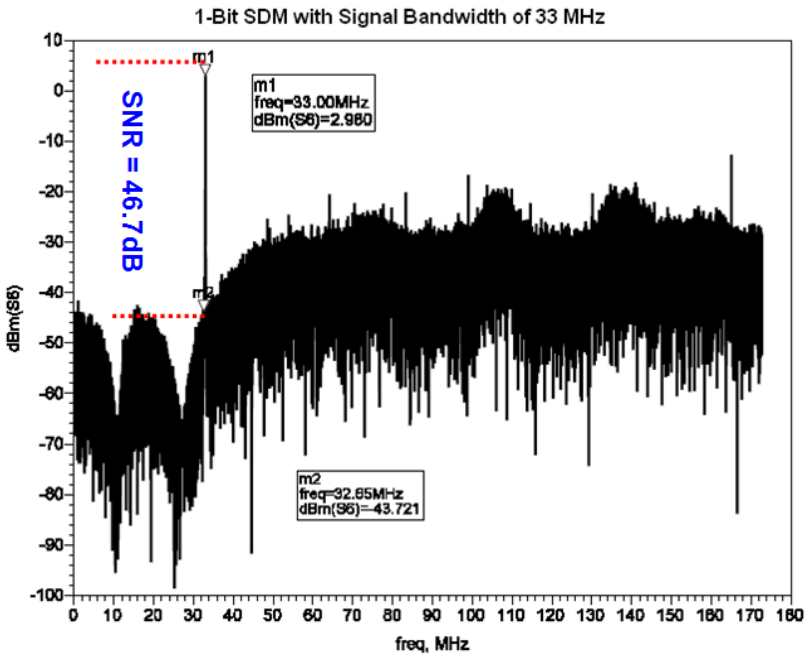


Figure 7.4: 1-bit wide-band sigma-delta modulator frequency response (signal bandwidth = 33 MHz, SNR = 46.7 dB)

7.3.2 5-tap FIR reconstruction filter

Single-bit SDM provides the advantages of inherent linearity and required in-band SNR, but it also brings high level out-of-band quantization noise due to noise shaping. This high level could violate spurious emission mask demanded by the standards even after band selection saw filter and duplex filter between the PA and the antenna. In order to relax analog filtering and meet spurious emission mask, an embedded FIR filter is adopted in the proposed architecture to suppress the noise level first. As analyzed before, in order to reduce the number of power amplifiers, keeping low FIR filter order is a must. FIR filter order can be derived based on spurious emission requirement of specific standard. For example, for W-CDMA signal, 5^{th}-order FIR filter is enough to reduce the out-of-band quantization noise, and spurious emission mask can be met together with band selection SAW filter and duplex filter.

Figure 7.5 illustrated a 5-tap FIR frequency response and the filtered W-CDMA spectrum using the 1-bit oversampled SDM is illustrated in Figure 7.4.

From Figure 7.6, W-CDMA ACPR requirements are met with some safety margin. Since the FIR filter order is only five in this example, the total power amplifier number becomes five also which extremely ease the design of PA stage, and on-chip individual matching is feasible due to the low number of PA with relatively increased die area.

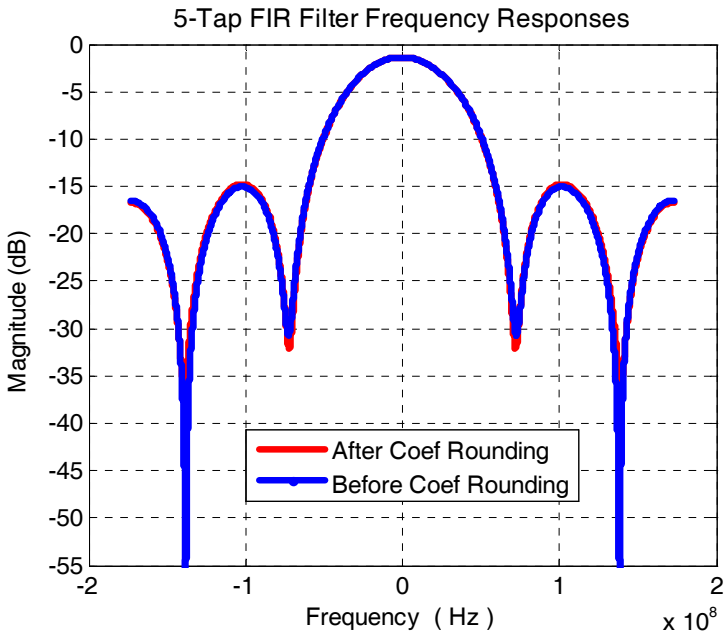


Figure 7.5: 5-tap FIR filter frequency response

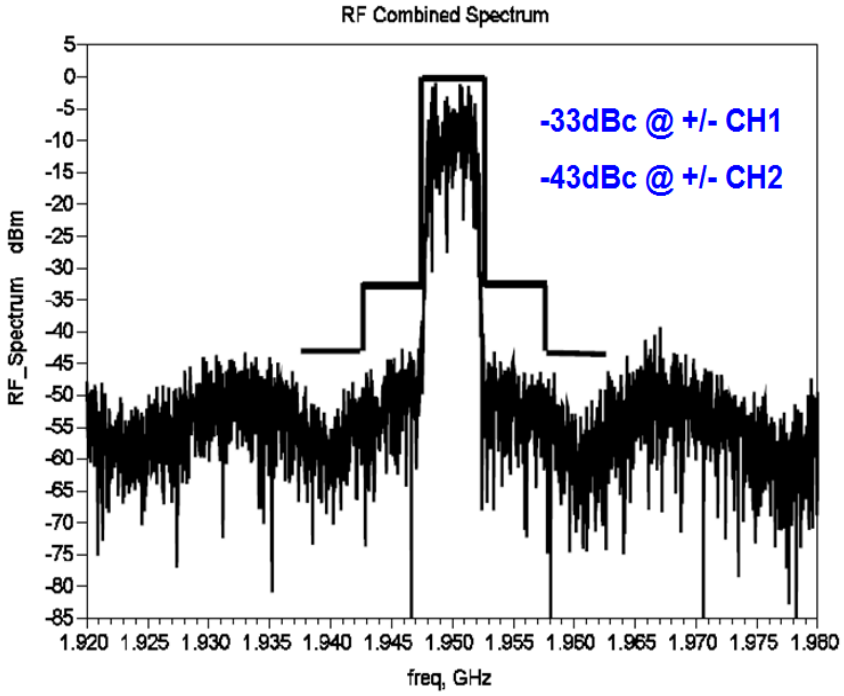


Figure 7.6: 5-tap FIR filtered WCDMA RF spectrum

7.3.3 Concept of high-efficient on-chip power combining

For the high power amplifier design, the loss in the on-chip passive impedance transformation and power combining network places an important role in the total power efficiency, therefore, they deserve special attention. In order to overcome the low breakdown voltage of the silicon transistors, these passive networks are inevitable for the high power amplification. If only a single on-chip impedance transformation circuit is used, then high loss in this circuit will result. The loss in the single impedance transformation circuit can be reduced by using the multi-section parallel impedance transformation networks. For example, as shown in Figure 7.7, the current I is flowing through a lossy impedance transformation network where the loss is represented by R_{loss}. The power at the load end and the power lost in the impedance transformation network can be represented by equations (7.3) and (7.4) respectively,

$$P_{out} = \frac{V_{load}^{\ 2}}{R_{load}} = I^2 * R_{load} \tag{7.3}$$

$$P_{loss,1} = I^2 * R_{loss} \tag{7.4}$$

If the output current I is split into I_1 and I_2 and each of the split currents is flowing into the same individual impedance network as shown in Figure 7.8.

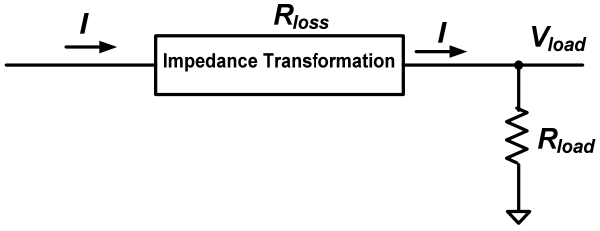


Figure 7.7: One-section lossy impedance transformation network

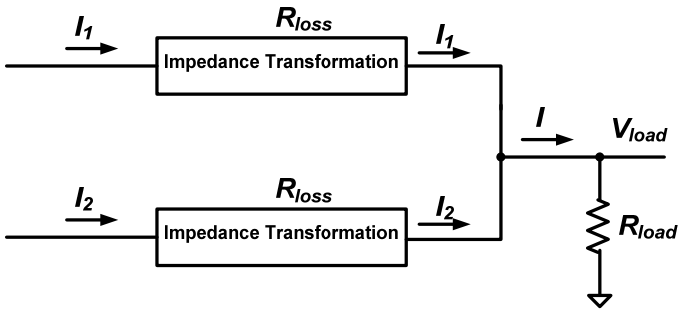


Figure 7.8: Two-section lossy impedance transformation network

Since $I = I_1 + I_2$, the same power is delivered to the output for the same load, but the loss will be different as expressed in equation (7.5)

$$P_{loss,2} = I_1^{\,2} * R_{loss} + I_2^{\,2} * R_{loss} = (I_1^{\,2} + I_2^{\,2}) * R_{loss} \tag{7.5}$$

When rewriting equation (7.4), we get

$$P_{loss,1} = I^2 * R_{loss} = (I_1 + I_2)^2 * R_{loss}$$

$$= (I_1^{\,2} + I_2^{\,2} + 2 * I_1 * I_2) * R_{loss} \tag{7.6}$$

Comparing the equations (7.5) and (7.5), it is obvious that the loss is reduced by the amount of two times $I_1 * I_2 * R_{loss}$ when delivering same power with the same load resistance if the PA output current I split into two currents I_1 and I_2. The loss in the transformation network could be reduced as high as 50% if the current is equally split. It can be concluded that by splitting the PA output current down to several small currents, the reduced loss in the impedance transformation networks can be achieved, thus the enhanced power efficiency can be achieved. The only drawback is the increased die area required.

In the proposed architecture as shown in Fig.7.9, parallel amplification is

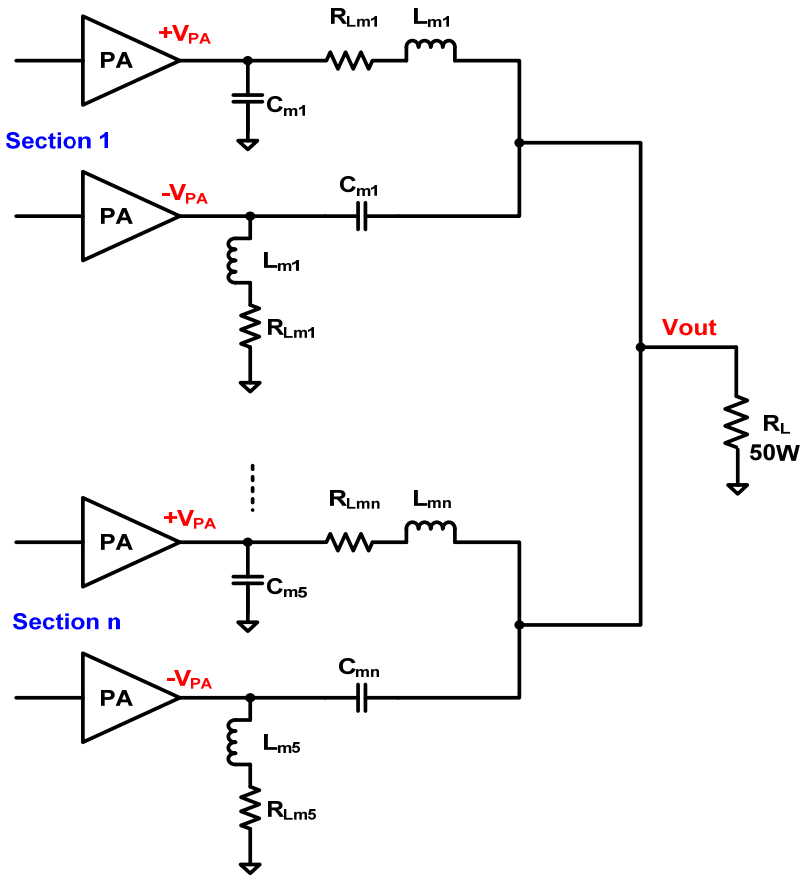


Figure 7.9: Lossy on-chip multi-section FIR power combining

utilized to overcome the low transistor breakdown voltage due to CMOS technology and low loss can be achieved using on-chip multi-section impedance transformation and power combining network. The total 5-tap FIR modulated output power with lossless power combining network can be expressed as

$$P_{out} = 4*[(V_{PA})^2 / R_L]*(\sum_{k=1}^{n} \frac{R_L}{B_k})^2 = 4*[(V_{PA})^2 / R_L]*(\sum_{k=1}^{n} a_k)^2 * \beta^2 \qquad (7.7)$$

where $R_L/B_1 = a_1\beta$, … , $R_L/B_n = a_n\beta$, n is the FIR filter order or the number of power amplifiers, and a_1 to a_n are the FIR coefficients. Total efficiency for the

lossy n-tap FIR (unit FIR coefficient) multi-section LC balun power combining network can be demonstrated in equation (7.8)

$$\eta_{ma} = \frac{1}{1 + n * \frac{R_L}{R_{Lm}} * \frac{1}{\left(1 + Q_L^{\,2}\right)} * \left(\frac{1}{E} + \left| 1 - \frac{V_{PA}}{V_{out}} \right|^2 \right)} \tag{7.8}$$

where η_{ma} is the power efficiency of the matching network itself, R_{Lm} is the loss due to finite inductor quality factor Q_L of 10, E is the total power enhancement ratio of the whole impedance transformation network, and n is the FIR filter order or the number of power amplifiers. Figure 7.10 shows the power efficiency of 1-tap to 5-tap FIR power combining network with unit FIR coefficient as the function of the power enhancement ratio (E). The power enhancement ratio is defined by [36], [38]. It takes the loss of the impedance transformation network into account, and is defined as the ratio of the RF power delivered to the load with the lossy transformation network in place, P_{out}, to the power delivered to the load if this load is directly connected to the power amplifier, $P_{out,0}$,

$$E = \frac{P_{out}}{P_{out,0}} \tag{7.9}$$

From the Figure 7.10, the 5-tap FIR power combining network provides highest power efficiency. Also from the plot, one can conclude that the 4-tap or 5-tap FIR power combining networks could provide the optimal power efficiency. 4-tap FIR implementation could save on-chip area compared to the 5-tap case, however, 5-tap FIR offers better out-of-band quantization noise suppression due to single-bit SDM noise-shaping. Therefore, 5-tap FIR power combining

surpasses 4-tap one in terms of satisfying the W-CDMA spectrum emission requirement while maintaining highest efficiency (with slightly increase on the die size).

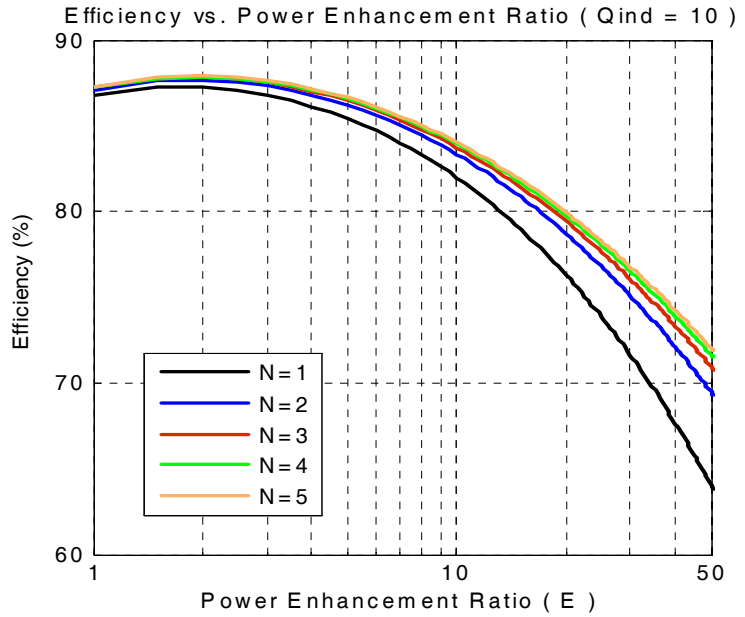


Figure 7.10: Power efficiency of the impedance transformation network function power enhancement ratio with different sections

The overall power efficiency is determined by the power efficiency in the power amplification stage and the power combing stage. With the extremely high efficiency offered by the non-linear class E PA and the boosted efficiency due to the parallel power combining, the overall high power efficiency can be achieved without the need of the off-chip balun.

7.4 Summary of proposed digital polar transmitter

A highly integrated high efficient wide-band digital polar transmitter

architecture targeted for W-CDMA transmitter application is proposed as an extension of the digital SDM-based transmitter architecture. Based on the digital polar modulator design and the parallel amplification technique, the proposed transmitter features the advantages of circuit simplicity, enhanced power efficiency, and a high level of integration.

In this chapter, a 1-bit wide-band sigma delta modulator (SDM) is utilized in the envelope path to generate digital envelope without linearity degradation. The quantization noise due to 1-bit SDM is suppressed by the embedded finite impulse response (FIR) filter. The FIR-delayed envelop bit streams control a number of power amplifiers to restore the spectrum at the radio frequency (RF) and suppress the quantization noise simultaneously when RF powers are combined. The power amplifiers (PAs) are driven by the phase modulated RF signal and the number of PAs is equal to the order of the FIR filter. The PA outputs are combined using on-chip inductor and capacitor (LC) baluns and eliminate the need of an off-chip impedance transformation, a power combining network as well as a standalone balun. The conventional issue of digital image is inherently solved by the null locations set by the embedded FIR filter response. System-level simulation demonstrates that the proposed architecture can efficiently transmit high power using the low-voltage CMOS technology with 5MHz or higher signal bandwidth without spectrum quality degradation. The proposed system takes full advantage of CMOS technology scaling, digital signal processing and parallel amplification to ease the circuit complexity and enhance the power efficiency for wide-band non-constant modulated signals.

CHAPTER 8

CONCLUSIONS

This thesis presents a highly integrated digital IF to RF transmitter (DRFTx) which combines a 1.5-bit current steering DAC, a semi-digital FIR filter and a RF mixer along with a RF VGA implemented in 0.18μm CMOS technology for W-CDMA mobile application. The proposed IC is designed based on the transmitter linearity analysis. The embedded reconstruction filter attenuates the out-of-band quantization noise due to ∑Δ modulator noise-shaping below the spectral emission mask level and ACPR demanded by the 2GHz W-CDMA transmitter. The design of FIR filter results from the linearity derivation and the tradeoff on the filter length and power consumption. 74dB dynamic range is achieved by scaling the power of both sigma-delta digital IF stage and RF VGA stage. The proposed DRFTx achieves good linearity utilizing 1.5-bit DAC. The measured results show that a digital-intensive digital IF to RF upconverter architecture can be successfully employed for W-CDMA transmitter application. The system level simulation shows that the proposed DRFTx has the potential to be extended to other wide-band transmitter application, such as 2.4 GHz WLAN 802.11g transmitter with maximum circuit reuse, and the concept of digital sigma-delta modulator based architecture can be extended from Cartesian to polar coordinates to make CMOS implementation of high efficient power amplification possible for wide-band wireless mobile transmit devices without the need of off-chip balun.

The concept presented in the thesis could be successfully applicable for the next generation wide-band digital-dominant, low cost and low power

consumption devices with decent performances.

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