Digitally Controlled DC-DC Buck Converters with Lossless Current Sensing

by

Tao Liu

A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved October 2011 by the
Graduate Supervisory Committee:

Bertan Bakkaloglu, Chair
Sule Ozev
Bert Vermeire
Yu Cao

ARIZONA STATE UNIVERSITY

December 2011

ABSTRACT

Current sensing ability is one of the most desirable features of contemporary current or voltage mode controlled DC-DC converters. Current sensing can be used for over load protection, multi-stage converter load balancing, current-mode control, multi-phase converter current-sharing, load independent control, power efficiency improvement etc. There are handful existing approaches for current sensing such as external resistor sensing, triode mode current mirroring, observer sensing, Hall-Effect sensors, transformers, DC Resistance (DCR) sensing, Gm-C filter sensing etc. However, each method has one or more issues that prevent them from being successfully applied in DC-DC converter, e.g. low accuracy, discontinuous sensing nature, high sensitivity to switching noise, high cost, requirement of known external power filter components, bulky size, etc.

In this dissertation, an offset-independent inductor Built-In Self Test (BIST) architecture is proposed which is able to measure the inductor inductance and DCR. The measured DCR enables the proposed continuous, lossless, average current sensing scheme.

A digital Voltage Mode Control (VMC) DC-DC buck converter with the inductor BIST and current sensing architecture is designed, fabricated, and experimentally tested. The average measurement errors for inductance, DCR and current sensing are 2.1%, 3.6%, and 1.5% respectively. For the 3.5mm by 3.5mm die area, inductor BIST and current sensing circuits including related pins only consume 5.2% of the die area. BIST mode draws 40mA current for a maximum time period of 200us upon start-up and the continuous current sensing consumes

about 400uA quiescent current. This buck converter utilizes an adaptive compensator. It could update compensator internally so that the overall system has a proper loop response for large range inductance and load current.

Next, a digital Average Current Mode Control (ACMC) DC-DC buck converter with the proposed average current sensing circuits is designed and tested. To reduce chip area and power consumption, a 9 bits hybrid Digital Pulse Width Modulator (DPWM) which uses a Mixed-mode DLL (MDLL) is also proposed. The DC-DC converter has a maximum of 12V input, 1-11 V output range, and a maximum of 3W output power. The maximum error of one least significant bit (LSB) delay of the proposed DPWM is less than 1%.

To My Parents Jiliang Liu and Luying Wu

ACKNOWLEDGMENTS

I would like to express my heartfelt gratitude to my advisor and committee chair, Professor Bertan Bakkaloglu, without whom my research and this dissertation would not have been possible. I am very grateful for his advising, encouragement, inspiration, and enduring patience. Dr. Bakkaloglu has watched every step that I have walked in the past several years. His help has become my life-long heritage.

I would also like to give special appreciation to Dr. Yu (Kevin) Cao, Dr. Sule Ozev, and Dr. Bert Vermeire for serving as my committee members. I benefit a lot from the insightful discussion with Dr. Vermeire on chip ESD design. Dr. Ozev has also given me very valuable suggestions on inductor tests.

I want to thank all the members in analog & RF integrated circuit design lab who helped me throughout my stressful PhD period: Dr. Hyunsoo Yeom, Dr. Hang Song, Dr. Hani Ahmad, Dr. Junghan Lee, Dr. Hyuntae Kim, Dr. Seungkee Min, Mr. Ahmad Dashtestani, Mr. Sridhar Shashidharan, Mr. Chao Fu and. Ms. Jing Bai. I owe special thanks to Dr. Hyunsoo Yeom for his patience and great help on the layout design of my every chip tape-out. I also want to express special thanks to Chao Fu for his critical support on average current mode controller design.

Last but not least, I would like to show my great appreciation to Space Micro, Inc. and NASA Jet Propulsion Laboratory for funding this project. Thank Dr. Philippe Adell from NASA and Dr. Bert Vermeire from Space Micro for their inspiration, comments, and recommendations during design reviews.

TABLE OF CONTENTS

Page

CHAPTER Page

CHAPTER Page

CHAPTER Page

LIST OF TABLES

LIST OF FIGURES

Figure Page

Figure Page

Figure Page

Figure Page

CHAPTER 1

INTRODUCTION

1.1 Research Background

1.1.1 DC-DC Application

Power supply and Power Management Integrated Circuits (PMICs) have been widely used in Computer, Communication and Consumer (3C) electronics. In recent several years, the market of portable devices such as smartphones and tablets has been increasing rapidly. The annual unit growth rate for portable devices is estimated at more than 12%, from about 2 billion in 2008 to over 3.4 billion devices in 2013 [3]. 3C electronics especially portable devices require a large number of PMICs. This is because each subsystem often requires a specific power supply voltage level, while only one voltage level is available at the battery output. A portable device generally needs 7 to 20 PMICs as shown in Table 1.1. In last several years, the market of PMIC has undergone a strong growth. The market for power supply and power management ICs was US $2.8 billion back in 1998 and jumped to over $5.1 billion by the end of 2000 with a compound annual growth rate of 35% [1]. The revenue of PMICs in portable devices alone accounted for more than US $14 billion in revenues and more than 26 billion units in 2008. This represents nearly 40% of total analog IC revenues and 1/3 of total

analog IC units [3]. By 2013, the revenue of PMICs in portable devices alone is estimated to further increase to nearly 1/2 of total analog IC revenues and units (about US$21 billion and 47 billion units, respectively) [3]. From 2010 to 2015, sales of PMICs will grow at a forecast average rate of 8 percent annually [2][4], reaching $30.6 billion in total revenue by 2015 [4].

Table 1.1. Typical Number of PMICs in Portable Devices [3]

Portable Device Type	**Typical Number of PMICs**
Notebook	20
High multimedia / Smartphone	18
MID (Mobile Internet Device)	18
Digital still camera	18
Global Positioning System (GPS) / Portable Navigation Device (PND)	16
Digital picture frame	15
Portable ultrasound	15
Entry / regular phone	13
Netbook	13
Portable medical device (Meters)	11
Digital media player	7
Bluetooth headset	7

Among various PMICs, voltage regulator is one major product type. There are two major categories of voltage regulators: switching mode DC-DC regulator

and Low Dropout Voltage (LDO) regulator. LDO can provide a relatively low-noise output voltage, and is very suitable for powering noise-sensitive analog and radio frequency circuits such as low-jitter Phase Locked Loops (PLL), Delay Locked Loops (DLL) etc. But LDO can only provide lower voltage output from the input and has relatively low efficiency. The efficiency of LDO is approximately the ratio of the LDO output voltage V_{OUT} and the input voltage V_{IN}, V_{OUT}/V_{IN}. LDO is therefore very inefficient when the dropout voltage (V_{IN}-V_{OUT}) is big. DC-DC regulator, on the other hand, can convert input voltage to either higher or lower voltage, and has better efficiency. The typical efficiency of modern DC-DC is larger than 80% and can be up to 98%. Although DC-DC has higher complexity, and generally higher cost, large ripple than LDO due to the switching nature, it still gains the popularity in battery based portable devices. The scope of this dissertation is only limited to switching mode DC-DC regulators.

1.1.2 Digital Control of DC-DC Converter

DC-DC converter usually requires a loop compensator (also called controller) due to the insufficient DC gain and phase margin of the uncompensated DC-DC system. There are two types of DC-DC control methods: analog control and digital control. In recent years, digital control method in DC-DC converters has

been studied by many researchers [5]-[12]. Compared to the traditional analog implementation, digital control method provides several advantages:

1. Less susceptibility to PVT, component variations and ambient noise. Analog controller consists of poles and zeros set by resistors and capacitors. It suffers from Process, Voltage and Temperature (PVT) variations as well as component tolerance variation and drift due to ambient noise. A digital controller is able to precisely position poles and zeros and requires fewer components. Thus, the digital control system is more robust and has high tolerance on all kinds of variations.
2. Possibility of implementing advanced control schemes. It is much easier to implement advanced control techniques into digital control system. Some of these advanced control scheme, such as high order compensator, are considered impractical or too challenging for analog realization. Moreover, digital control enables programmable compensator. Advanced control schemes and programmability can be used to improve system performances such as dynamic performance, efficiency, stability, etc. Some examples of these advanced control schemes are accomplished in prior work [7]-[10].
3. Easiness of integrating with other digital systems. This is particularly attractive for applications where load is in digital implementation as well. In

these scenarios, both PMIC and other functionality chipset can be integrated on the same die or SOC platform. Therefore, it is able to provide a compact and low cost overall solution.

Table 1.2. Comparison Between Digital and Analog Control in DC-DC.

Characteristics	**Analog Control**	**Digital Control**
PVT Variation Tolerance	No	Yes
Component Variation Tolerance	No	Yes
Programmability	No	Yes
Advanced Control Algorithms	No	Yes
Telemetry	No	Yes
Technology Exploitation	No	Yes
System Integration	No	Yes
Accuracy	High	Lower
Speed	Fast	Slower
Complexity	Low	Higher

A comparison of analog and digital control methods is provided by Table 1.2. Analog control method generally has the advantage of high accuracy, fast speed and lower complexity. The accuracy of digital controlled DC-DC depends on the

resolution of the Digital Pulse Width Modulator (DPWM). High resolution DPWM module is required to generate high accuracy DC-DC output voltage. This increases the DC-DC hardware complexity. Also A/D converters are extra demands in digital control method. Thus the hardware cost for digital control is normally higher than that of analog method. In spite of these drawbacks, digital control method is still appealing due to its advantages in robustness, programmability, and easiness of integration.

1.1.3 Research Motivation

Regardless of the success in commercial applications and intensive research work in academy, switching mode DC-DC still has some issues that are not well addressed. One of the biggest issues is the dynamic performance and stability degradation due to the incognizance of off-chip components and load condition. For a generic DC-DC converter system, such as the digital voltage mode controlled DC-DC buck converter shown in Fig. 1.1, the inductor inductance L, DC Resistance (DCR) and load current I_{LOAD} are in the close loop of DC-DC and their values affect the loop response and stability. However, the inductor is usually off-chip due to the large size (normally μH range) and the load current is application dependent. As the exact information of inductor and load current is not known as a prior knowledge. DC-DC is generally designed around a desired

nominal inductor value and specific load current. Unfortunately, inductor usually has large variation which can hurt the system's stability and transient response. In recent years, there is also an increasing interest of using single inductor to drive multiple outputs [13]-[17]. In these Single Inductor Multiple Outputs (SIMO) systems, the impact of inductor variation and potential damage is even more critical. Meanwhile, since the regulator is designed for a specific load current, it's difficult to compensate for a wide load range. Therefore, by monitoring the inductor and load current, we can improve the loop response and enable load independent control [18].

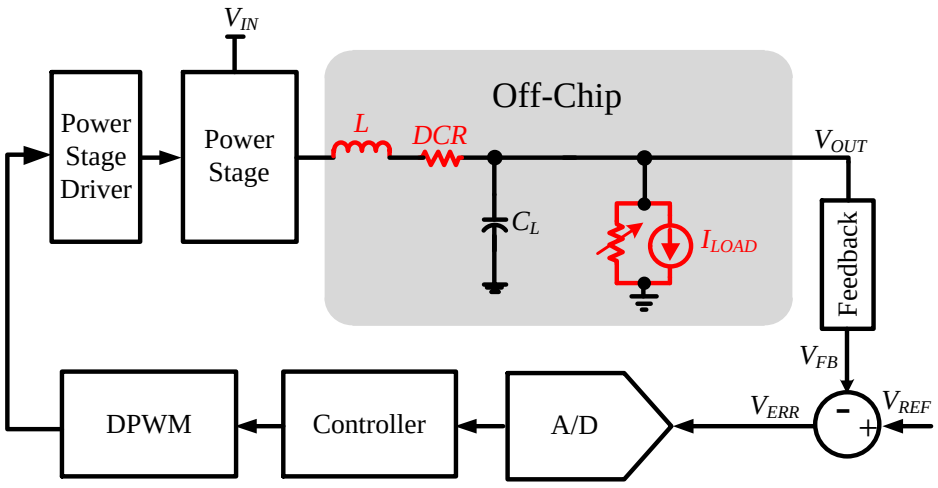


Fig. 1.1. Generic Digitally Controlled Voltage Mode DC-DC Buck Converter.

Load current sensing ability is also one of the most desirable features of contemporary current or voltage mode controlled DC-DC converters. Current sensing can be used for short circuit detection, over current protection, multi-stage

converter load balancing, multi-phase converter current sharing, power efficiency improvement, current-mode control etc.

The motivation of this dissertation is to design DC-DC converters with two major features: 1) load inductor inductance and DCR Built-In Self-Test (BIST) functionality using the existing system resource; 2) lossless, continuous and integrated load current sensing ability. Since efficiency is a key requirement in power management systems, all these features are expected to be implemented with low power consumption and small hardware overhead.

1.2 Dissertation Outline

The organization of this dissertation is as follows:

Chapter 1 provides a brief introduction of DC-DC converters, explains the existing issues of contemporary DC-DC design methodology. Chapter 2 reviews prior current sensing approaches in DC-DC converters. The essentials of the most commonly used current sensing methods together with their advantages and shortages are discussed. Chapter 3 presents a digital Voltage Mode Controlled (VMC) buck converter core. The overall architecture and details of individual modules are described. In Chapter 4, the proposed inductor BIST and lossless current sensing architecture is presented. The VMC buck converter core together with the BIST and current sensing architectures are designed, fabricated and

experimentally tested. Chapter 5 demonstrates the measurement results of the VMC buck converter. As Average Current Mode Control (ACMC) has gained attention due to its advantages over voltage mode control, a digital ACMC buck converter is proposed in Chapter 6. A hybrid DPWM based on a mixed-mode DLL (MDLL) is proposed. Chapter 7 gives the experimental test results of the digital ACMC buck converter. The last Chapter, Chapter 8, offers a brief summary and a discussion of possible future work.

CHAPTER 2

STATE-OF-THE-ART CURRENT SENSING TECHNIQUES

In DC-DC converters, current sensing has various applications such as over load protection, multi-stage converter load balancing, current-mode control, multi-phase converter current-sharing, mode hop etc. Depending on the application, the current to be measured could be the inductor current (I_L), load current (I_{LOAD}), occasionally even the output capacitor current (I_C, equals to inductor ripple current). There are handful existing approaches in the field of current sensing. According to the current to be sensed, we can divide these methods into two major categories: instantaneous inductor current sensing and average inductor current sensing (I_{LOAD} in buck converter). This chapter first reviews state-of-the-art instantaneous inductor current sensing schemes then discusses the existing average inductor current sensing techniques. A summary of these techniques is provided at the end of this chapter. Although there are many existing current sensing schemes, an integratable, continuous, lossless, hardware and power efficient current sensing is still unavailable. The review in this chapter establishes the demand for our current sensing technique which has all the aforementioned features. This technique will be introduced in later chapters.

2.1 Instantaneous Inductor Current Sensing

2.1.1 External R_{SENSE}

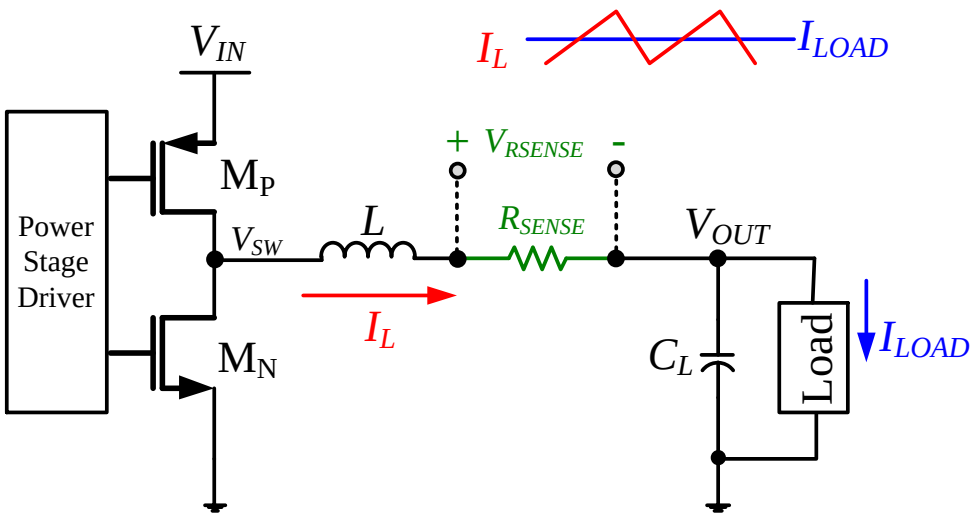


Fig. 2.1. External R_{SENSE} Current Sensing.

The widely used conventional current sensing method is adding a known sensing resistor R_{SENSE} in the current path. One can monitor the current by measuring the voltage cross the R_{SENSE} as shown in Fig. 2.1. Depending on the place to insert R_{SENSE}, current to be sensed can be the power switch current, the inductor current or the load current. As the R_{SENSE} value must be precise to obtain accurate current sensing, external sensing resistor is usually used. The accuracy of this method relies on the type of resistor utilized. In the most common implementation, a discrete metallic resistor with zero temperature coefficient is

used, either manganin or constantan. The accuracy is just determined by the initial tolerance of the part.

This approach generally has high accuracy but is not lossless. The power loss on R_{SENSE} results the power efficiency degradation of the DC-DC converter. The situation becomes worse especially in high load current application. A trade off must be done between the power loss and the sensing accuracy. The power loss can be reduced by using smaller R_{SENSE}. However, when R_{SENSE} is too small, the voltage across R_{SENSE} would be in the order of noise level or the sense amplifier offset thereby reducing the sensing accuracy. Meanwhile, an expensive high performance instrument amplifier may be required, which increases overall system cost.

2.1.2 Power FET R_{DS} Sensing

Power MOSFET turned on resistor R_{DS} can be used as a sensing resistor as shown in Fig. 2.2. When a MOSFET is in triode mode, the R_{DS} can be approximately expressed as:

$$R_{DS} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \tag{2-1}$$

Here μ is the mobility, C_{OX} is the unit area oxide capacitance, L and W are the MOSFET length and width, and V_{TH} is the transistor threshold voltage. Thus, the

current goes through one power MOSFET can be sensed by monitoring the voltage drop on the power FET.

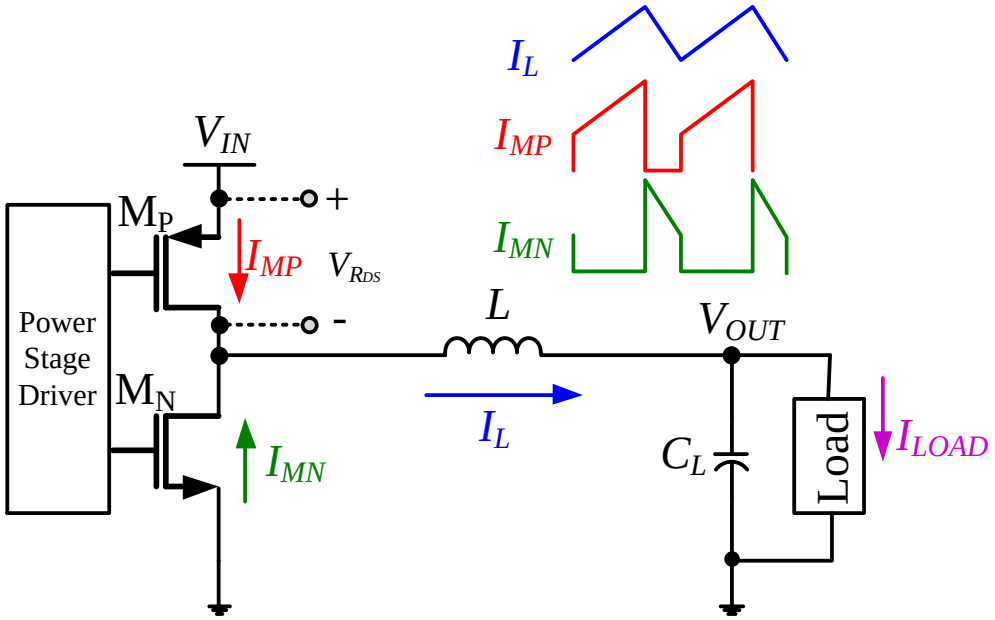


Fig. 2.2. Power MOSFET R_{DS} Current Sensing.

This approach is lossless and does not require external components. However, since the R_{DS} is inherently nonlinear and has significant variations over process, voltage and temperature, it inevitably has low accuracy. Another issue of this approach is that, since only one side MOSFET current is observed, i.e. I_{MP} or I_{MN} as shown in Fig. 2.2, it is not able to sense the inductor current through the entire switching period continuously.

2.1.3 Triode Mode Current Mirroring

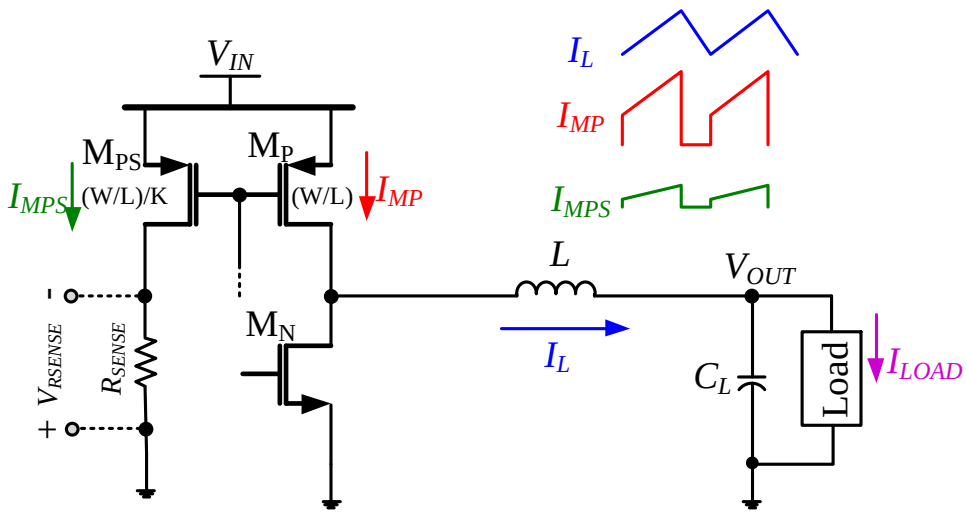


Fig. 2.3. Triode Mode Current Mirroring Current Sensing.

The idea of triode mode current mirroring is adding a sense MOSFET in parallel with the power MOSFET through layout matching [19]-[24]. Fig. 2.3 illustrates the triode mode current mirroring current sensing method. By sensing the current goes through the parallel MOSFET, the power MOSFET current can be predicated.

To assure that the current goes to the parallel sensing MOSFET is very small thus the power consumed for current sensing is ignorable, a large 1:K current mirror ratio is normally utilized. The accuracy of the current-sensing circuit decreases since the matching accuracy between the main MOSFET and the sense-FET degrades. The accuracy of the sense-FET technique is about ±20% in practice. Moreover, the sense-FET technique is sensitive to switching noise during

power FETS switching. In addition, for converters with high load currents where the switches are off-chip, the implementation of the technique may not be feasible because of unavailability of discrete sense-FET switches.

2.1.4 Hall-effect Sensor

Hall-effect current sensor is one of the most popular magnetic field sensors. This sensor is based on the Hall-effect, which was discovered by Edwin Hall in 1879. There are some CMOS Hall-effect sensors reported in [27]-[31]. The most serious limitation of Hall-effect sensor is the degaussing cycle required after an over current incident [41]. Hall-effect sensor provides a current sensing with low loss and good accuracy, but in general at a very high price.

2.1.5 Transformer

Transformer can be used to sense the current by using the mutual inductor properties [32]. The idea of transformer current sensing is shown in Fig. 2.4. Transformer is typically bulky and not able to be integrated. Also, transformers are normally expensive. Besides, since DC current is not able to transferred, this approach cannot be used for over current protection.

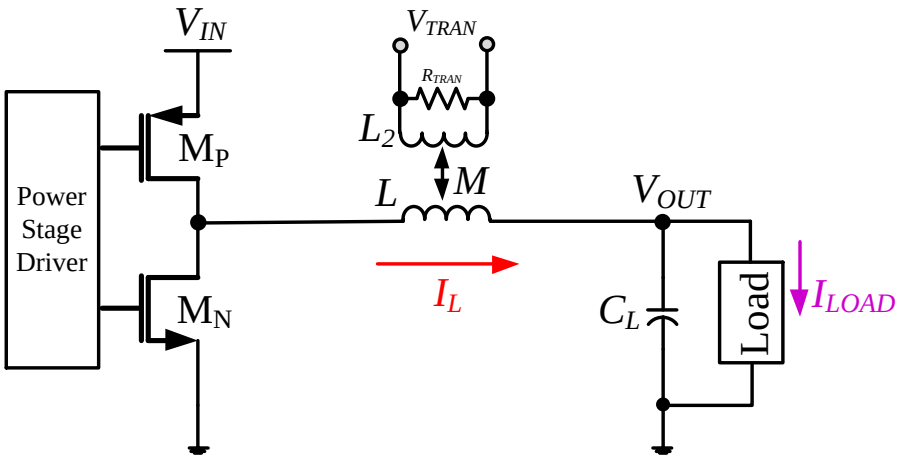


Fig. 2.4. Transformer Current Sensing.

2.1.6 Observer

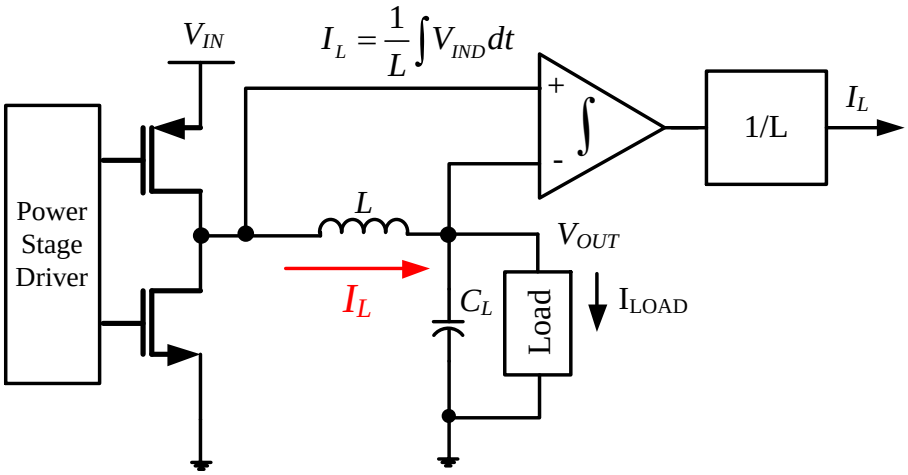


Fig. 2.5. Observer Current Sensing.

Observer current sensing approach was proposed in [33], the voltage over the power filter inductor is integrated over time to obtain the inductor current as shown in Fig. 2.5. Since the voltage over the inductor $V_{IND}=L\times di/dt$, the inductor

current can be obtained by measuring the integrator output. To obtain inductor current, *L* should be known as a prior knowledge. However, to avoid saturation in the integrator because of the voltage over inductor DCR, the integrator is reset periodically [33], and therefore only AC ripple current is estimated.

2.1.7 Inductor DCR Sensing

Inductor DCR current sensing was proposed in [34], an upgraded DCR current sensing approached was also given to deal with the voltage regulators with coupled inductors [35]. The extensive analysis of DCR current sensing can be found in [36][37].

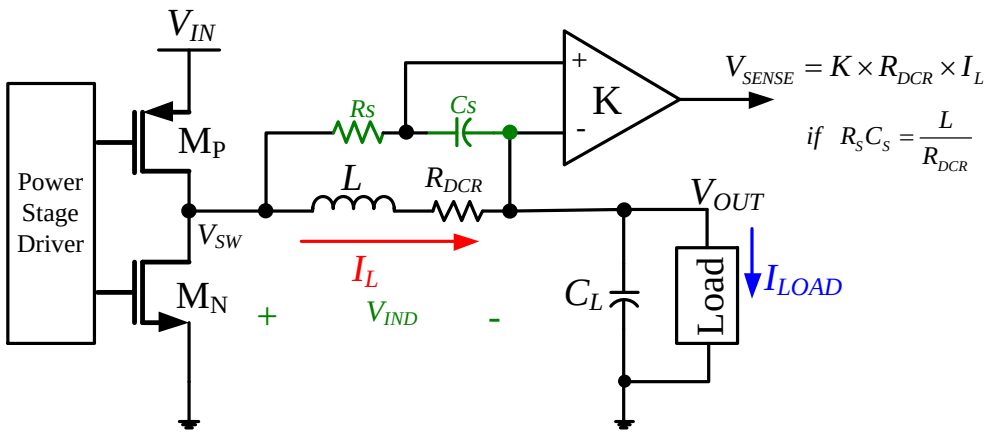


Fig. 2.6. DCR Current Sensing.

The idea of inductor DCR current sensing is illustrated in Fig. 2.6. An RC filter consisting of *Rs* and *Cs* is added between the power stage switching node

V_{SW} and the DC-DC output node V_{OUT}. The voltage across the inductor (also is the voltage over the two terminals of RC filter) is:

$$V_{IND} = (sL + R_{DCR})I_L \tag{2-2}$$

We can obtain the voltage over the capacitor *Cs* by

$$\begin{aligned} V_{Cs} &= V_{IND} \times \frac{\frac{1}{sC_S}}{R_S + \frac{1}{sC_S}} \\ &= (sL + R_{DCR}) \times \frac{1}{1 + sR_S C_S} \times I_L \\ &= \left(\frac{1 + s\frac{L}{R_{DCR}}}{1 + sR_S C_S} \right) \times R_{DCR} \times I_L \end{aligned} \tag{2-3}$$

From equation (2-3) we can notice that, if *Rs* and *Cs* are selected such that the pole formed *Rs* and *Cs* cancels the zero formed by *L* and R_{DCR}, i.e.

$$R_S C_S = \frac{L}{R_{DCR}} \tag{2-4}$$

then we have:

$$V_{Cs} = R_{DCR} \times I_L \tag{2-5}$$

Thus we can sense the inductor current from the voltage over capacitor C_s. Apparently *L* and R_{DCR} need to be known first, and *Rs* and *Cs* are then chosen accordingly. In industry practice, a thermistor is often used in this current sensing method to compensate for the temperature drift of the inductor DCR.

2.1.8 Gm-C Filter

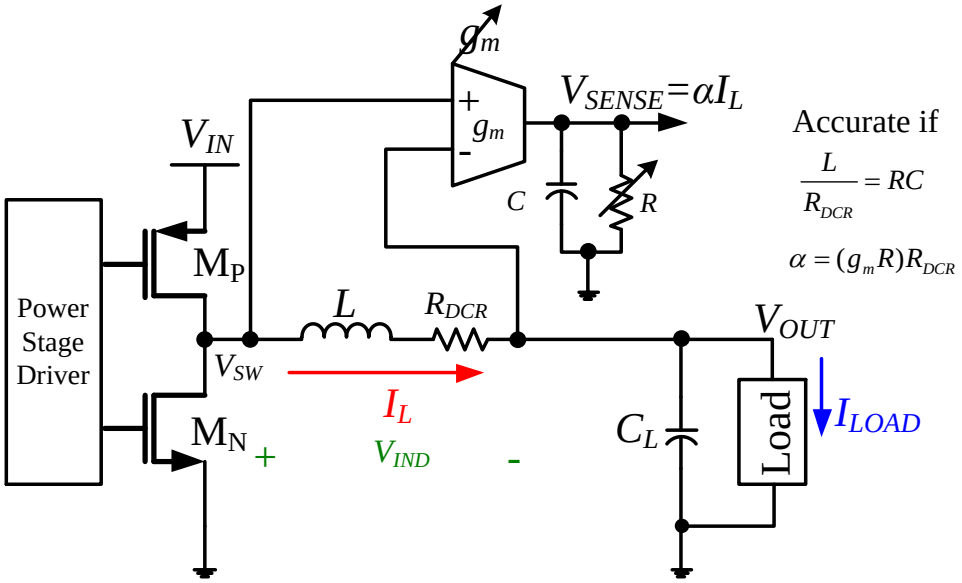


Fig. 2.7. Gm-C Filter Based Current Sensing.

One of the latest and representative current sensing approaches is the Gm-C filter based technique proposed in [40]. The idea of this technique is illustrated in Fig. 2.7. A transconductor Gm block is added to convert the voltage over the inductor into current, which goes through a shunt RC network. As the voltage over the inductor is:

$$V_{IND}=(sL+R_{DCR})I_L \tag{2-6}$$

We could therefore acquire the sensed voltage at the output of Gm block by

$$
\begin{aligned}
V_{SENSE} &= g_m \times V_{IND} \times \left(R \| \frac{1}{sC} \right) \\
&= g_m \times (sL + R_{DCR}) \times I_L \times \left(\frac{R}{1+sRC} \right) \\
&= g_m \times R \times \left(\frac{1+s\frac{L}{R_{DCR}}}{1+sRC} \right) \times R_{DCR} \times I_L
\end{aligned}
\tag{2-7}
$$

If we could tune R so that

$$
RC = \frac{L}{R_{DCR}} \tag{2-8}
$$

then sensing voltage V_{SENSE} becomes

$$
V_{SENSE} = g_m \times R \times R_{DCR} \times I_L \tag{2-9}
$$

Especially, if g_m can be tuned such that

$$
g_m \times R \times R_{DCR} = \alpha \tag{2-10}
$$

where α is a known constant, then V_{SENSE} becomes

$$
V_{SENSE} = \alpha \times I_L \tag{2-11}
$$

Gm-C filter approach requires both inductance L and DCR information, such that the resistor R can be tuned. In [40], an inductor measurement circuit performs the test of L and DCR upon start-up.

Gm-C filter current sensing is an accurate analog technique, but the transconductor and RC filter R require tuning and calibration. Also, the Gm block's offset is cancelled in analog domain, it demands two identical units. The

offset is cancelled by configuring the two units in ping-pong style. The analog calibration and offset cancellation make Gm-C filter current sensing very complex and hardware costly.

2.2 Average Inductor Current Sensing

Average inductor current needs to be sensed in some applications. To obtain the average inductor current, one can use a designated sensing technique to sense the average current directly, or sense the instantaneous inductor current first and then do averaging or prediction based on the instantaneous inductor current. All these methods are reviewed in this section.

2.2.1 Average Current Sensing

Average current sensing was proposed in [55]. This method is similar to the inductor DCR sensing technique introduced in section 2.1.7. In inductor DCR sensing technique, the RC filter consisting of *Rs* and *Cs* is added between the two nodes of inductor. Here in average current sensing technique, the RC low pass filter is added to the DC-DC switching node V_{SW} and ground. The architecture of the average current sensing method is shown in Fig. 2.8.

When applying an ideal LC filter to the switching node V_{SW}, the DC signal of the output of the filter (here is the output voltage V_{OUT}) is the average of V_{SW}. Similarly, when applying an RC filter, the DC signal of the output of the filter

(here is the capacitor voltage V_C) is the average of V_{SW} as well. The difference of the V_{OUT} and V_C is due to the existence of inductor DCR. Thus we have:

$$\bar{V}_C - \bar{V}_{OUT} = R_{DCR} \times I_{LOAD} \tag{2-12}$$

Hence, we could sense the average inductor current by monitoring the voltage different of V_{OUT} and V_C.

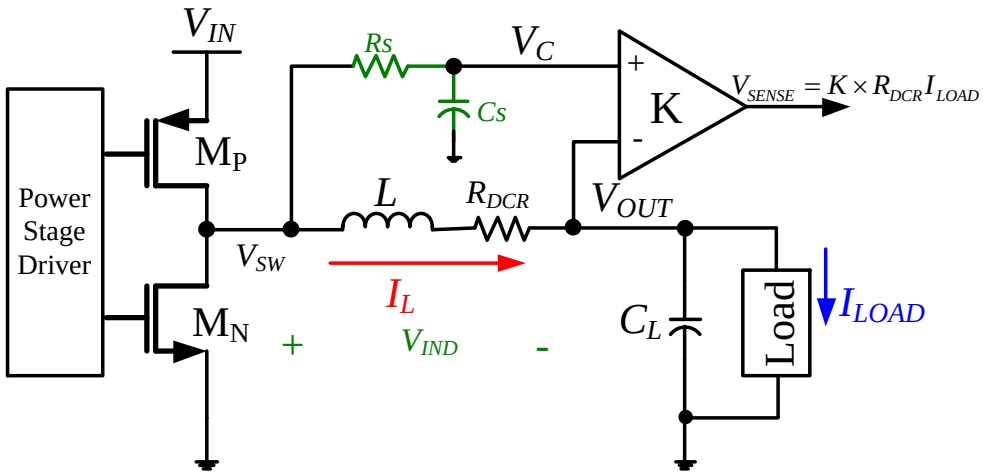


Fig. 2.8. Average Current Sensing.

Since V_{SW} is being switched between V_{IN} and ground at the switching frequency, (V_C-V_{OUT}) has a large AC signal component riding on top of the desired $R_{DCR} \times I_{LOAD}$ information. This AC signal must be filtered out to obtain the current signal. There is going to be a tradeoff between accuracy and RC filter bandwidth. If the bandwidth is too low, the signal will not be useful either for loop control or for current limiting.

2.2.2 Averaging Filter

An intuitive method to obtain average current is to capture multiple instantaneous current samples within one period and then take the average operation. As this method needs to store the sampled current value at multiple time instances, it is more suitable for digital implementation. The average operation realization is adding an averaging filter:

$$F_{AVG}(\mathrm{z}) = \frac{1}{N}\sum_{i=0}^{i=N-1} z^{-i} \qquad (2\text{-}13)$$

Averaging filter provides very high attenuation for the first several harmonics of the switching frequency and significantly removes the effects of the switching noise from the computed average value. For better DSP implementation, an approximation of this averaging filter by using Bessel filter is proposed in [11] where this filter approximates the averaging filter response very well up to one-half of the switching frequency.

2.2.3 Geometric Relation Based Predication

Geometric relation based predication method is another method to obtain the average inductor current. It was first proposed in [12]. Compared to the averaging filter method, this approach just needs to sample once at the peak or valley inductor current instance. The idea of this approach is shown in Fig. 2.9.

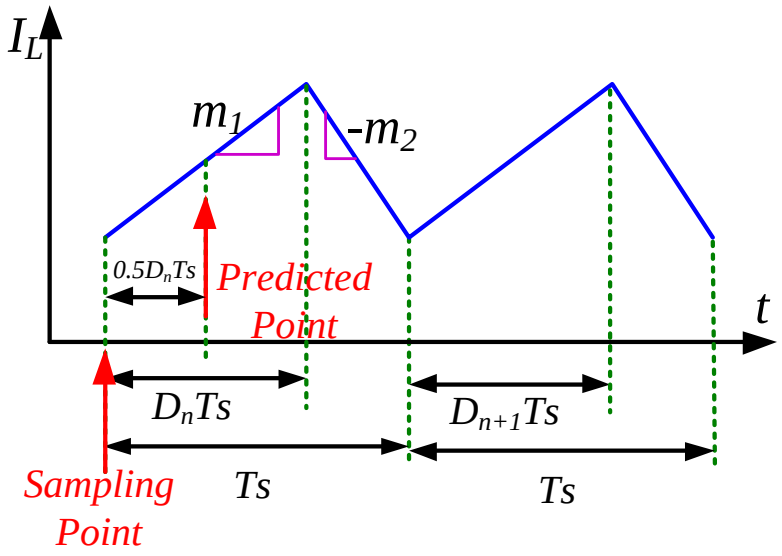


Fig. 2.9. Geometric Relation Based Predication.

The inductor current is DC-DC has a triangular waveform shape. The slopes of the rising and falling parts are determined by the DC-DC input voltage V_{IN}, output voltage V_{OUT}, and the inductor L. The slopes of the inductor current waveforms for basic converters are provided in Table 2.1.

Table 2.1. Slopes of the Inductor Current Waveform.

Buck Converter	$m_1 = \frac{V_{IN} - V_{OUT}}{L}$	$-m_2 = -\frac{V_{OUT}}{L}$
Boost converter	$m_1 = \frac{V_{IN}}{L}$	$-m_2 = -\frac{V_{IN} - V_{OUT}}{L}$
Buck-boost Converter	$m_1 = \frac{V_{IN}}{L}$	$-m_2 = \frac{V_{OUT}}{L}$

If we could detect V_{IN}, V_{OUT}, and L, we would be able to obtain the inductor current waveform slopes. As the duty cycle D is normally known by the DC-DC, the average inductor can be predicated based on the current slope and the valley or peak inductor current as shown in Fig. 2.9. This predication method needs to monitor both input voltage and output voltage, the inductor must be known as a prior knowledge too.

2.3 Summary of Current Sensing Techniques

Table 2.2 summaries all the aforementioned current sensing techniques. For more information of current sensing, one could refer to comprehensive current sensing technique reviews given by [36][38][39][41]. As modern high performance DC-DC converter may exploit the current information for all kinds of applications, an integrated, lossless, accurate, hardware and power efficient current-sensing technique is required for state-of-the-art switching regulators. Although we have many available current sensing techniques as shown in Table 2.2, each one has one or more issues that prevent them from being successfully applied in DC-DC converter, e.g. low accuracy, discontinuous sensing nature, high sensitivity to switching noise, high cost, requirement of known external power filter components, bulky size, etc. The current sensing solution proposed in

this dissertation has all required features for high performance DC-DC regulators. The detailed implementation is discussed in the following chapters.

Table 2.2. Summary of Conventional Current Sensing Techniques

	Techniques	**Pros**	**Cons**
Instantaneous Inductor Current Sensing	External R_{SENSE}	Accurate	Low Efficiency
	Power FET R_{DS}	Lossless	Low Accuracy Discontinuous Noisy
	Triode Mode Current Mirroring	Lossless	Matching Issue Only for On-Chip Switches Discontinuous Noisy
	Hall-effect Sensor	Lossless	High Cost
	Transformer	Lossless	High Cost Bulky, not Integratable No DC Current Information
	Observer	Lossless	Known *L* Need Discrete Components
	Inductor DCR Sensing	Lossless	Known *L* and *DCR*
	Gm-C Filter	Lossless	Known *L* and *DCR* Hardware Costly
Average Inductor Current Sensing	Average Current Sensing	Lossless	Known *DCR*
	Averaging Filter	Low complexity	Needs Multiple Current Samples
	Geometric Relation Based Predication	Needs only one sample	Known V_{IN}, V_{OUT}, *L*

CHAPTER 3

DIGITAL VMC BUCK CONVERTER CORE

The goal of this dissertation is to design DC-DC converters with inductor BIST and load current sensing abilities. Before implementing these two major features, a DC-DC converter needs to be designed at first to work as a platform. In this chapter, a digital Voltage Mode Controlled (VMC) DC-DC buck converter core is proposed with the detailed module implementation elaborated.

3.1 Digital VMC Buck Converter Core Architecture Overview

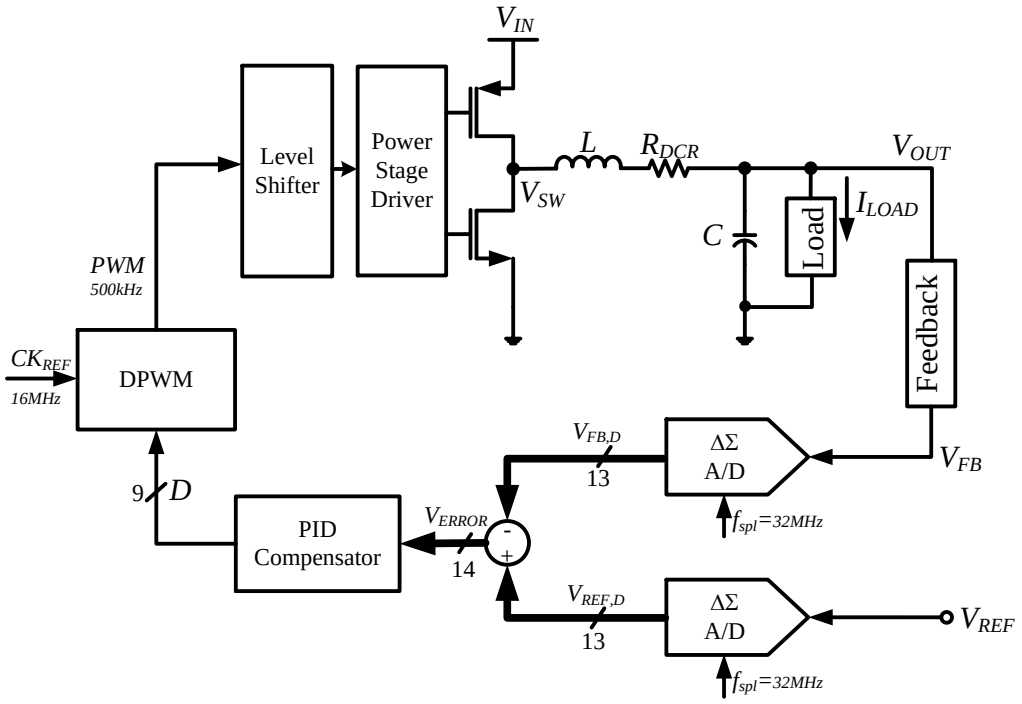


Fig. 3.1. Digitally Controlled Buck Converter Architecture.

The proposed overall digital VMC buck converter core architecture is shown in Fig. 3.1. The operation of this buck converter regulation is as follows: two ΔΣ

A/D converters are used to digitize the DC-DC feedback voltage V_{FB} and the reference voltage V_{REF}. The error signal of the digitized feedback voltage $V_{FB,D}$ and the digitized reference voltage $V_{REF,D}$ is applied to the Proportional Integral Derivative (PID) compensator. The PID compensator calculates the required duty cycle *D*. The Digital Pulse Width Modulator (DPWM) converts this duty cycle requirement into a Pulse Width Modulation (PWM) signal and sends it to the level shifter. The level shifter's output then drives the power MOSFTES via a built in dead-time controlled gate driver. When feedback voltage and reference voltage are equal, error V_{ERROR} will be equal to zero. This DC-DC is designed with a close loop system crossover frequency 50kHz while PWM switching frequency is 500kHz.

3.2 Digital VMC Buck Converter Core Implementation

The digital DC-DC buck converter core architecture contains several critical blocks such as A/D converter, DPWM, power stage driver, PID compensator. This section explains all the major blocks used in the proposed digital VMC buck converter core architecture in details.

3.2.1 DPWM

A 9bits hybrid DPWM is utilized to generate the pulse signal, where a 5bits digital counter controls the 5bits Most Significant Bits (MSBs) coarse part, and a

Type-I 4bits Delay Lock Loop (DLL) controls the Least Significant Bits (LSBs) fine delay part. The overall architecture of DPWM and its corresponding operation waveform is shown in Fig. 3.2. The detailed operation of the DPWM is as follows:

A $1/2^{\#MSB}$ (#MSB is the number of MSBs bits) ratio frequency divider takes the reference clock 16MHz CK_{REF} and generates switching clock signal CK_{SW}. CK_{SW} runs at DC-DC switching frequency 500kHz. The rising edge of CK_{SW} works as the rising edge of the PWM signal.

Meanwhile, a 5bits counter running at CK_{REF} followed by a 5bit comparator generates the coarse part ready signal *CR*. After releasing from the reset, counter starts to count the number of CK_{REF} cycles. Once it reaches the PID MSBs code, the comparator set the *CR* to logic high. The delay from the rising edge of CK_{SW} to rising edge of *CR* is the coarse delay part of PWM.

In parallel with frequency divider and digital counter, a locked DLL generates 16-tap delay outputs of CK_{REF}. A multiplexer selects one of the DLL output CK_{MUX} based on the 4b LSBs of PID Code. The delay between CK_{MUX} and CK_{REF} is the fine delay part. CK_{MUX} is used to sample the coarse part ready signal *CR*, once *CR*=1, the delay between CK_{MUX} and *CR* is the fine delay part as well. The

PWM high width is then determined by combining the coarse part and fine part, i.e. from rising edge of CK_{SW} to the rising edge of CK_{MUX} right after CR=1.

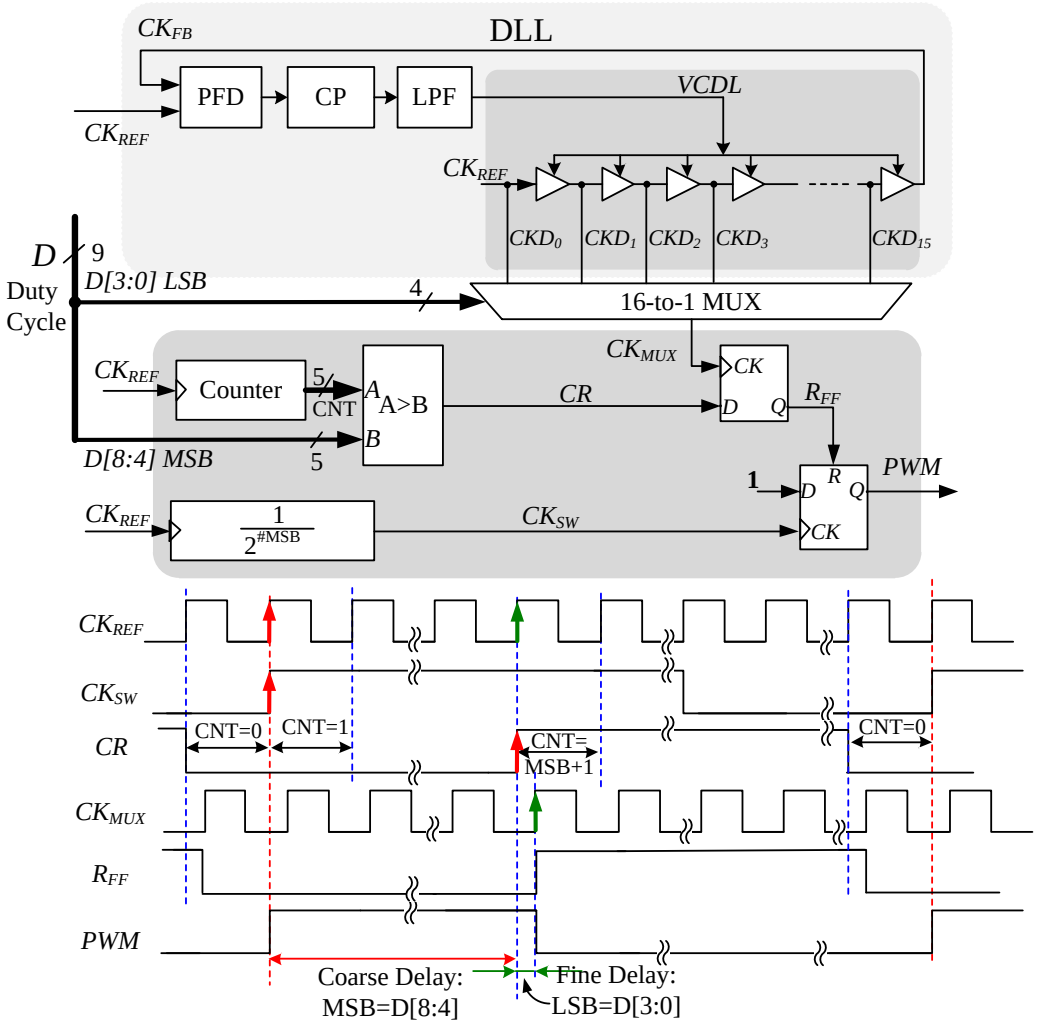


Fig. 3.2. DPWM Architecture and Operation Waveform.

There are two types of conventional DPWM implementation methods: digital counter based DPWM or analog circuits (such as DLL) based DPWM. Digital counter based DPWM needs to run at $f_{clk}=2^n \times f_s$. Here n is DPWM resolution and f_s is the switching frequency. f_s needs to be balanced between the

requirement of smaller off-chip inductor (the bigger f_s the better) and the requirement of lower switching power loss (the smaller f_s the better). Typical f_s is from ~100kHz order to ~10MHz order. DPWM resolution n is determined by the DC-DC output voltage control resolution, e.g. to achieve 0.1% DC voltage error, a 10bits DPWM is needed such that $1/2^{10}$ <0.1%. According to these conditions, the DPWM clock f_{clk} can be up to ~GHz or higher frequency which incurs significant digital circuits switching power loss.

All analog implementation solution such as DLL based DPWM requires 2^n DLL delay stages, which is both power and hardware costly.

In this work, by using hybrid structure, i.e., digital counter for the coarse delay part and DLL for the fine delay part, we could reduce digital clock frequency from $f_{clk}=2^n \times f_s$ to $f_{clk}=2^{MSBs} \times f_s$ and decrease the DLL delay stages from 2^n to $2^{\#LSB}$. Therefore, both digital circuits and DLL can have low power consumption and small chip area.

3.2.1.1 DLL Overall Architecture

The core circuit of DPWM is the DLL shown in Fig. 3.3. It consists of a Phase Frequency Detector (PFD), a Charge-Pump (CP), a Low Pass Filter (LPF) and a Voltage Controlled Delay Line (VCDL). The PFD compares the feedback clock signal CK_{FB} and the reference clock CK_{REF}, then generates up and down

signals. Up and down signals are used to control the LPF capacitor charge and discharge time. VCDL generates 16-tap delay output. The delay of each tap is controlled by the voltage over the capacitor (*Vctrl)*. When the CK_{FB} and CK_{REF} are aligned, PFD produces identical up and down signal, thereby the capacitor voltage *Vctrl* maintains the same and DLL is locked.

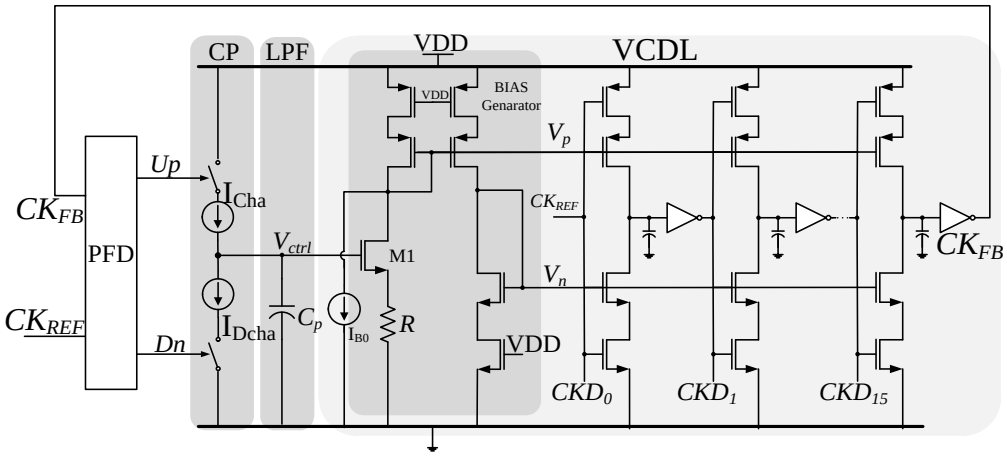


Fig. 3.3. DLL Architecture.

3.2.1.2 Charge Pump

A low jitter DLL is a critical requirement for a high precision DPWM. The jitter of DLL is caused by many reasons such as power supply and ground noise, mismatch in charge pump etc. Low jitter DLL therefore demands a charge pump with high supply and ground immunity and high precision matching between the charge and discharge current biases.

The charge pump of DLL in this work is shown in Fig. 3.4. It was originally proposed in [42]. To obtain better matching of the charge current I_{Cha} and the

discharge current I_{Dcha}, wide-swing current mirrors are adopted in both PMOS and NMOS sides. The charge and discharge control switch M1 and M6 are placed to the source side of the current mirror transistors. Thus the switching noise of M1 and M6 can be isolated by two cascaded bias transistors (M2, M3 or M4, M5 in Fig. 3.4). Moreover, four bypass capacitors C1, C2, C3 and C4 are also connected to bias voltage nodes to stabilize the current biases and absorb switching noise.

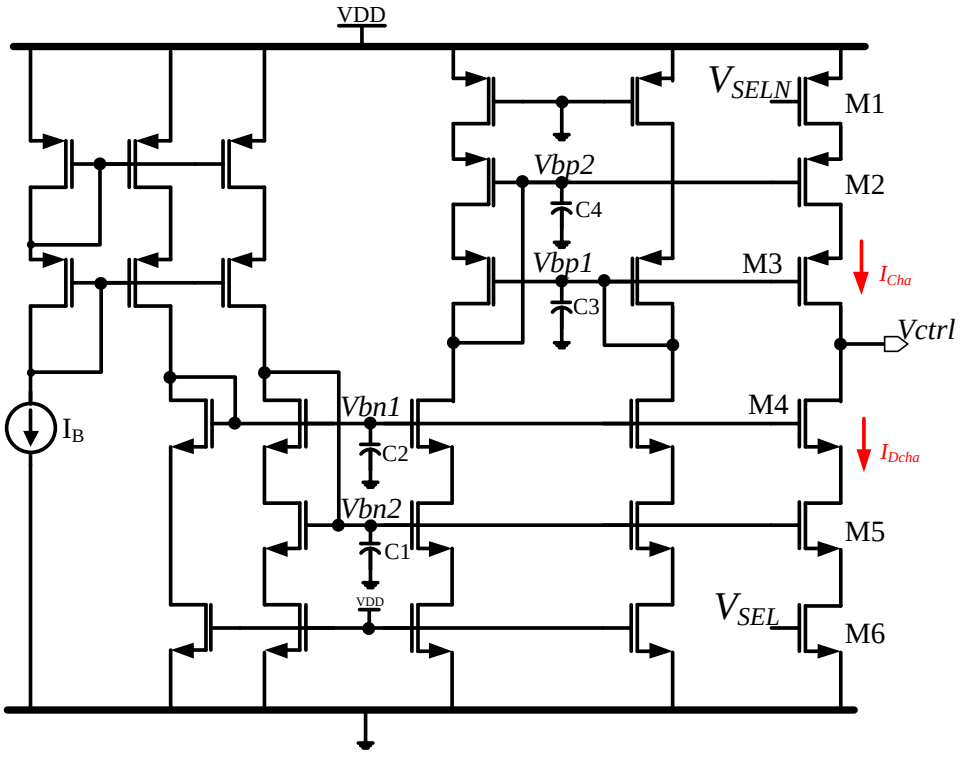


Fig. 3.4. Charge Pump in DLL.

The power supply and ground noise are isolated by cascaded transistors M1 to M6, and further suppressed by the bypass capacitors as well. By using all these techniques, this charge pump is not susceptible to switching and power supply

noise, and has highly matched charge and discharged current biases, eventually makes low jitter DLL practical.

3.2.1.3 Delay Stage

DLL has a well-known issue of being locked at multiple reference clock periods, which comes with its nature. DLL is designed to be locked when the delay from the reference clock CK_{REF} to the feedback clock CK_{FB} is just one period of CK_{REF}. However, DLL can also be locked when the delay from CK_{REF} to CK_{FB} is multiple periods of CK_{REF}.

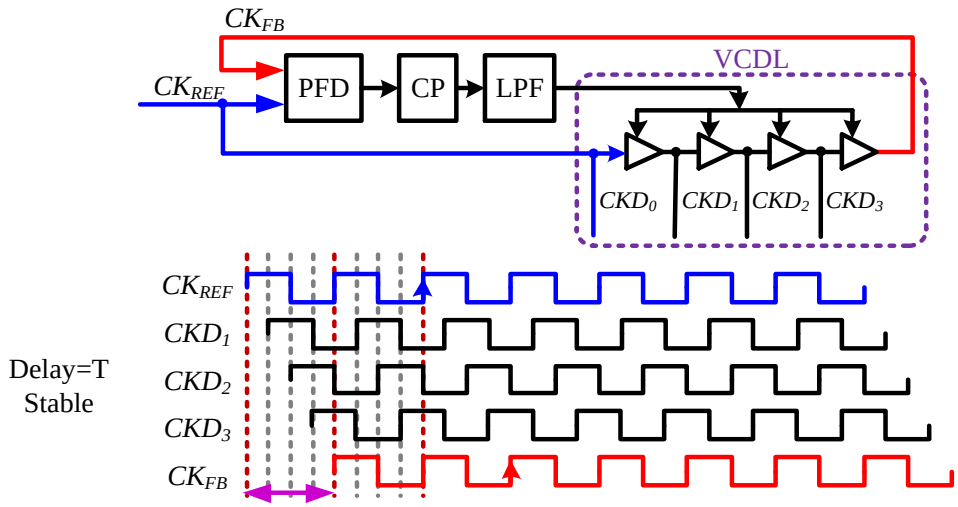


Fig. 3.5. Waveforms of DLL at Normal Lock Status (Delay=T).

Fig. 3.5 shows the waveforms of a 4-tap DLL when it is locked at the desired delay, i.e. delay=T (T is the period of CK_{REF}). In this scenario, each delay stage has a delay of T/4. The rising edges of CK_{REF} and CK_{FB} are aligned. DLL is locked as desired. However, when the delay=nT (n>1 is an integer), DLL is

locked as well. Shown in Fig. 3.6 is a case of delay=2T. Each delay stage has a delay of T/2 rather than the desired T/4. The rising edges of CK_{REF} and CK_{FB} are still aligned. PFD produces identical up and down signal, the cap voltage *Vctrl* maintains the same and DLL is locked falsely.

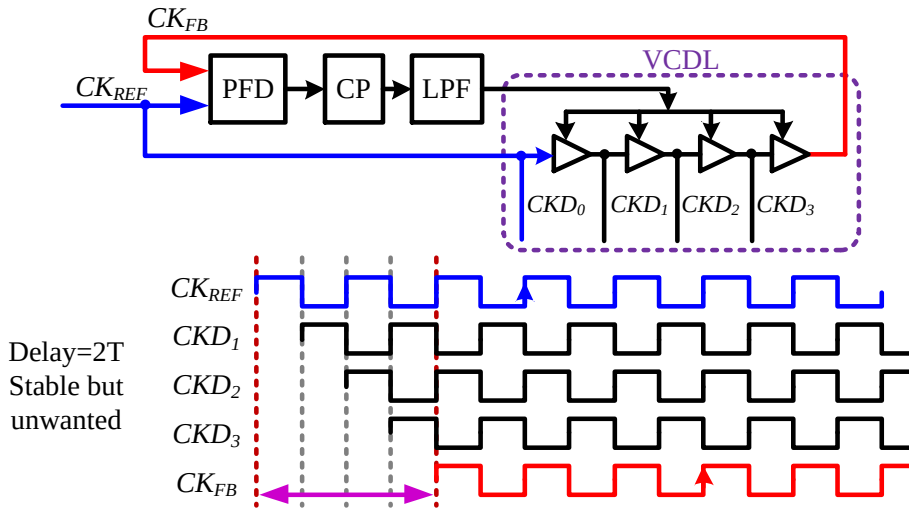


Fig. 3.6. Waveforms of DLL at Multiple-Period-Lock Status (Delay=2T).

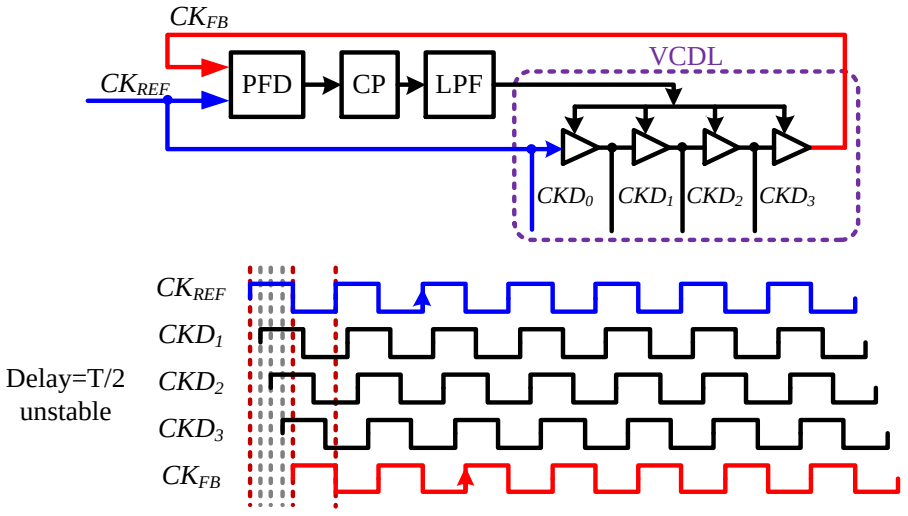


Fig. 3.7. Waveforms of DLL at Half Period Delay Status (Delay=T/2).

DLL does not have issue when delay=T/n. A delay=T/2 example is shown in Fig. 3.7. As CK_{REF} and CK_{FB} do not arrive at the same time, PFD detects the difference and adjusts the LPF cap through CP, DLL is not locked in this case.

To avoid multiple-period-lock status, the tuning rage of the delay cell must be properly designed. As long as the delay of VCDL does not reach 2T or higher value for all VCDL control voltage *Vctrl* range, the multiple period lock issue will not exist. In our design, DLL has 4bits resolution, i.e. 16 stages VCDL. The reference clock CK_{REF} is 16MHz. When DLL is locked, the delay of each stage is:

$$Delay_{1stage} = \frac{1}{f_{CK_{REF}}} \times \frac{1}{2^{\#LSB}} = \frac{1}{16M} \times \frac{1}{16} \approx 3.91n \qquad (3\text{-}1)$$

As shown in Fig. 3.3, when the VCDL input voltage *Vctrl* rises from 0 to M1 threshold voltage V_{TH}, M1 is not turned on. Bias generator is only proved by bias I_{B0}. After V_{TH}, as *Vctrl* rises, the current goes to M1 increases, the delay of VCDL stages increase accordingly. When *Vctrl* reaches the power supply V_{DD}, the current replicas have the largest current and DLL has the minimum delay. The typical DLL delay line delay versus *Vctrl* curve is something like Fig. 3.8.

To avoid multiple-period-lock issue, the maximum delay of each stage for the entire *Vctrl* range is set to be 7.2ns at typical process and room temperature, which is less than 2 times of 3.91ns. 7.2ns is selected in a way that the maximum

delay of the VCDL is less than 2 times of 3.91ns for all other process and temperature corners as well.

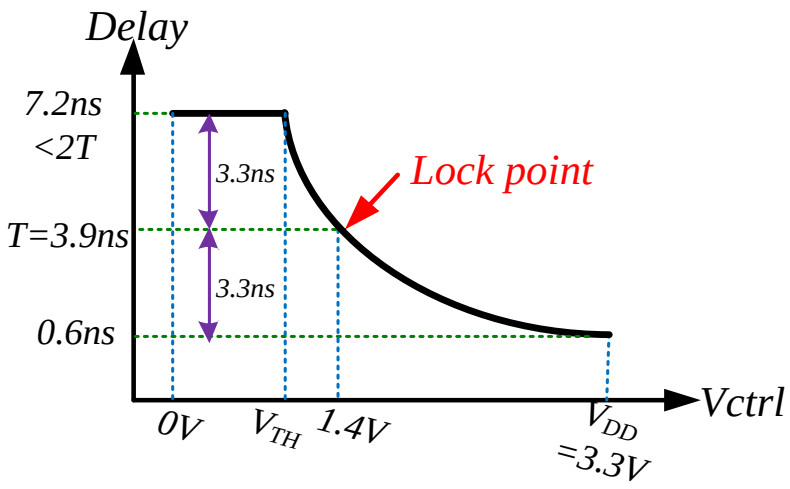


Fig. 3.8. DLL VCDL Delay vs *Vctrl*.

The *Vctrl* voltage at DLL lock status (typical 1.4V) is picked in a way that delay line has the same tuning range around the lock point, e.g, 3.3ns above or below the desired 3.91ns in this work as shown in Fig. 3.8.

3.2.2 ΔΣ ADC

A/D Converters (ADCs) are required in digitally controlled DC-DC converters to digitize the DC-DC feedback voltage, reference voltages etc. Frequency domain ΔΣADCs are utilized in our DC-DC converter feedback path.

The ADC is composed of a non-feedback ΔΣ modulator and a Cascaded Integrator-Comb (CIC) decimator as shown in Fig. 3.9.

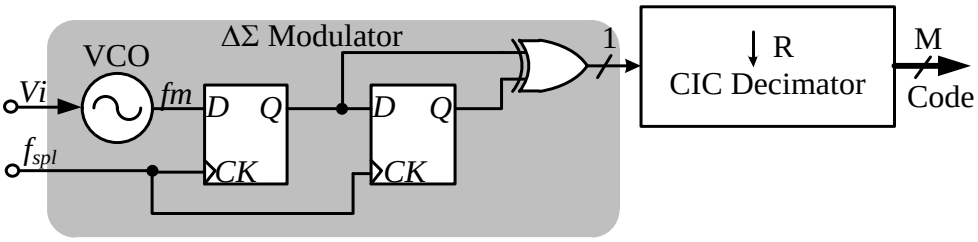


Fig. 3.9. ΔΣ ADC Architecture.

3.2.2.1 ΔΣ Modulator

The first-order ΔΣ modulator is a Voltage Controlled Oscillator (VCO) followed by a ΔΣ frequency discriminator (ΔΣFD). ΔΣFD consists of two D flip-flops and an XOR gate. The frequency domain ΔΣ modulator was proposed in [43][44][45] and firstly used in DC-DC buck converter in [5].

The input of the ΔΣ modulator is the voltage signal V_i. V_i is converted to a Frequency Modulation (FM) modulated signal $f_m(t)$ after voltage-to-frequency conversion by VCO. An FM modulated signal can be described as:

$$fm(t) = \sin\left[\theta(t)\right] \tag{3-2}$$

where the total angle is given by

$$\theta(t) = 2\pi\int_{-\infty}^{t}\left[f_c + k\cdot x(\tau)\right]d\tau \tag{3-3}$$

Here f_c is the FM carrier frequency, k is the frequency sensitivity of the modulator and $x(\tau)$ is the modulating signal. The instantaneous frequency is equal to the derivative of the phase and is defined as:

$$f_{ins}(t) = \frac{1}{2\pi}\frac{d\theta(t)}{dt} = f_c + k \cdot x(\tau) \qquad (3\text{-}4)$$

ΔΣFD digitizes the deviation of $f_{ins}(t)$ from its carrier frequency f_c with high pass quantization noise shaping similar to the traditional ΔΣ modulator. The output of this ΔΣ modulator is a stream of ones and zeros.

This non-feedback ΔΣ modulator is equivalent to the traditional ΔΣ modulator because it performs the same three main functions on a signal similar to the traditional modulator: integration, quantization and differentiation. The integration is achieved by the VCO, i.e. FM modulator; the quantization is accomplished via the detection of the FM phase zero-crossings position utilizing D flip flops, and the differentiation is done by the digital differentiator gate (XOR).

In terms of pattern noise, the first-order frequency ΔΣ modulator is equivalent to a traditional ΔΣ modulator as well. Simulation in [45] has found exact match between the pattern noise model introduced by Candy and Benjamin [46] and the pattern noise behavior of the frequency ΔΣ modulator for constant inputs signals. In [45][47], it is pointed out that the first-order frequency ΔΣ modulator shows

20dB/decade noise shaping ability as that of the conventional first-order ΔΣ modulator.

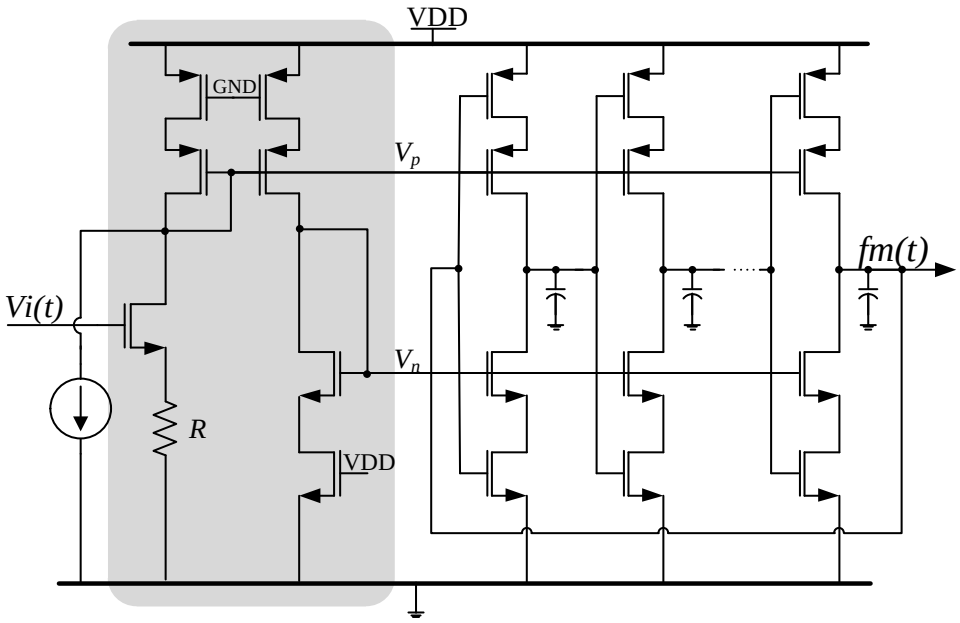


Fig. 3.10. VCO in ΔΣ Modulator.

The most challenging module in frequency ΔΣ Modulator is the FM modulator, i.e. the VCO. The VCO in ΔΣ modulator in this work uses a similar structure as that in DLL for easiness of implementation. The architecture of VCO is shown in Fig. 3.10. One big difference is that: each delay stage in DLL produces the delay of the input clock while each ring oscillator stage in VCO produces the inverted phase of the input clock.

3.2.2.2 CIC Decimator

The noise shaped ΔΣ modulator output signal is decimated by using CIC filter. Decimation is an important component of ΔΣADC. It transforms the

digitally modulated signal from short words occurring at high sampling rate to longer words at a rate close to Nyquist rate. This reduction in the bit rate makes the data more suitable for processing.

An efficient way of performing decimation and interpolation was introduced in [48]. It is a flexible, multiplier-free filter which is suitable for hardware implementation. It also can handle arbitrary and large rate changes. This filter is known as Cascaded Integrator Comb (CIC) filter. An overview of CIC filter can also be found in [49] and an extension of CIC filters is available in [50].

An N-stage CIC decimator has N cascaded integrator stages clocked at sampling frequency f_{spl}, followed by a rate change of factor R, and then followed by N cascaded comb stages running at f_{spl}/R. A two-stage CIC decimator example is provided in Fig. 3.11.

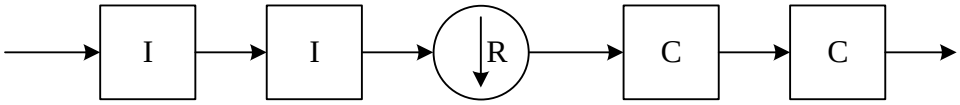


Fig. 3.11. Two-Stage CIC Decimator.

In CIC decimator, an integrator stage is simply a single-pole IIR filter with a unit feedback coefficient: $y[n]=y[n-1]+x[n]$. The corresponding transfer function of this integrator (accumulator) can be described as

$$H_I(z) = \frac{1}{1-z^{-1}} \tag{3-5}$$

A comb filter is an odd-symmetric FIR filter described by: *y[n]=x[n]+x[n-RM]*. *M* is the *differential delay* and can be any integer but usually limited to1 or 2. *R* is the rate reduction factor. The corresponding transfer unction of a comb filter stage can be described as

$$H_C(z) = 1 - z^{-RM} \tag{3-6}$$

Thus, the system function for the CIC filter referenced to the high sampling rate f_{spl} is:

$$H(z) = H_I^N(z) H_C^N(z) = \frac{\left(1 - z^{-RM}\right)^N}{\left(1 - z^{-1}\right)^N} = \left(\sum_{k=0}^{RM-1} z^{-k} \right)^N \tag{3-7}$$

CIC filters have a low-pass frequency characteristic. The frequency response is given by (3-7) evaluated at

$$z = e^{j(2\pi \hat{f} / R)} \tag{3-8}$$

where $\hat{f}$ is the frequency relative to the low sampling rate f_{spl}/R. By using mathematical approximations, we could obtain the magnitude response at the output of the CIC decimator:

$$\left|H(\hat{f})\right| \approx \left| RM \frac{\sin(\pi M \hat{f})}{\pi M \hat{f}} \right|^N \quad \text{for } 0 \le \hat{f} \le \frac{1}{M} \tag{3-9}$$

From (3-9), we notice that CIC filter has transmission zeros at $\hat{f} / M$. Thus, the differential delay *M* can be used as a design parameter to control the placement of

nulls. The DC gain of the CIC filter is $(RM)^N$. The bigger the decimator is, the larger the number of CIC filter stages, the bigger CIC filter DC gain is.

In our design, a two-stage CIC filter is used as a decimator. The differential delay M is picked as 1. The sampling frequency of CIC filter f_{spl} is 32MHz. CIC decimator output, PID compensator and DPWM share the same date rate, i.e. DC-DC switching frequency. This can be expressed as:

$$f_s = \frac{f_{spl}}{R} \tag{3-10}$$

Since the DC-DC switching frequency f_s is 500kHz, the decimation ratio R is therefore selected to be 32MHz/500kHz=64.

As the CIC filter's gain is $(RM)^N$, we can then calculate the number of bits required for the last comb stage due to bit growth. If B_{in} is the number of input bits, then the number of output bits, B_{out}, is

$$B_{out} = \left[N \log_2 (RM) + B_{in} \right] \tag{3-11}$$

Here operation [ ] denotes taking the upper rounded integer value of the argument. (3-11) is a guide to implement CIC decimator. A practical implementation normally uses B_{out} bits for each integrator and comb stage. The input is often sign extended to B_{out} bits and LSBs are either be truncated or rounded at later stages.

3.2.2.3 ADC Resolution

To satisfy specifications for the output voltage regulation, resolution of the ADC converter has to enable error that is lower than the allowed variation of the output voltage (ΔV_{OUT}) [52]. The required resolution is described as:

$$n_{ADC} = \text{int}\left[\log_2\left(\frac{V_{\max,ADC}}{V_{REF}} \cdot \frac{V_{OUT}}{\Delta V_{OUT}}\right)\right] \qquad (3\text{-}12)$$

where n_{ADC} represents the ADC resolution, i.e. the number of output bits of the ADC converter, V_{REF} is the reference voltage and $V_{max,ADC}$ is the full range voltage of the ADC assuming unipolar conversion in the range from 0 to $V_{max,AD}$. Operation int[ ] denotes taking the upper rounded integer value of the argument. Equation (3-12) gives the minimum number of bits for the A/D converter to meet the design specifications in terms of the output voltage regulation. In our design, 8-bit ADC is used in design to enable less than 0.5% output voltage variation control.

The theoretical resolution of the single D flip-flop ΔΣ Modulator is:

$$SQNR = 20\log_{10}\left(\frac{3}{2\pi}\right) + 20\log_{10}\left(\frac{\Delta f}{f_{bw}^{1.5}}\right) + 10\log_{10}\left(f_{spl}\right) \qquad (3\text{-}13)$$

where Δf is the maximum deviation of the FM-signal, f_{bw} is the bandwidth of the modulating signal while f_{spl} is the sampling clock frequency. In our system, f_{bw} is equal to the loop bandwidth which is limited to crossover frequency of 50kHz.

Equation (3-13) makes it easy to adjust the SQNR by simply changing the sampling clock frequency and the sensitivity of the FM modulator taking into account the effect of Δf on the linearity of the FM modulator.

In digitally controlled PWM converters, there is a potential issue called limit cycling. When limit cycling happens, the DC-DC output shows steady state oscillations. To avoid limit cycling, several conditions must be met as analyzed in [45]. One of them is that the DPWM must have higher resolutions than ADC. In our design, since the ADC has 8 bits resolution, we use a 9bits DPWM as discussed in section 3.2.1 to avoid limit cycling.

3.2.3 PID Compensator

The PID compensator is used to compensate the loop such that the system is stable with sufficient phase margin under the specified range of input voltage and load condition. At the system level, there are two main approaches in designing the digital control loop: digital redesign and direct digital design. In the digital redesign approach, the designer uses the well-understood method of feedback analysis and well-established results in analog domain and then uses a standard method of translation between analog and digital domains (such as bilinear transformation). In the direct digital design, the system is converted to a sampled discrete system because of the switching action. Every block is treated as a digital

block including the power stage. This method may generate more accurate results than the digital redesign but it is more complex due to lack of resemblance to analog design techniques. In this work, the digital redesign approach is used.

A well-established analog PID compensator design method is provided in [56]. Our design procedure is based on this method. The PID compensator is observed to be a product of Proportional Derivative (PD) and Proportional Integral (PI) compensators. That is, the PID compensator is a PD compensator in series with a PI compensator. So, the approach to the design of the PID compensator in this work is to design the PD and PI parts sequentially.

3.2.3.1 Uncompensated Loop

The open-loop control-to-output transfer function for DC-DC buck converter is given by

$$G_{vd}(s) = \frac{V_{OUT}}{D} \frac{1}{1 + s\frac{L}{R_L} + s^2 LC} \tag{3-14}$$

where R_L is the equivalent load resistance, L and C are power LC filter inductor and capacitor. Here the DCR of inductor and Equivalent Series Resistance (ESR) of capacitor are not considered. The open loop transfer function has two poles and therefore can also be expressed as

$$G_{vd}(s) = G_{d0} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{3-15}$$

where

$$\begin{aligned} G_{d0} &= \frac{V_{OUT}}{D} \\ \omega_0 &= \frac{1}{\sqrt{LC}} \\ Q_0 &= R_L \sqrt{\frac{C}{L}} \end{aligned} \tag{3-16}$$

The feedback scalar, which is usually a resistor voltage divider, can be modeled as

$$H = \frac{V_{REF}}{V_{OUT}} \tag{3-17}$$

The quiescent duty cycle is given by the steady state solution of the converter:

$$D = \frac{V_{OUT}}{V_{IN}} \tag{3-18}$$

The open-loop line-to-output transfer function is

$$\begin{aligned} G_{vg}(s) &= D \frac{1}{1 + s\frac{L}{R_L} + s^2 LC} \\ &= G_{g0} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0}\right)^2} \end{aligned} \tag{3-19}$$

with Gg0=D. The uncompensated complete system transfer function is

$$T_u(s) = G_{ADC} \frac{V_{OUT}}{D} G_{vd}(s) H \tag{3-20}$$

Here G_{ADC} is the ADC gain. Substitution of equations (3-15) into (3-20) leads to

$$\begin{aligned} T_u(s) &= G_{ADC} H \frac{V_{OUT}}{D} \frac{1}{1+\frac{s}{Q_0\omega_0}+\left(\frac{s}{\omega_0}\right)^2} \\ &= T_{u0} \frac{1}{1+\frac{s}{Q_0\omega_0}+\left(\frac{s}{\omega_0}\right)^2} \end{aligned} \tag{3-21}$$

where T_{u0} is the DC gain of the complete system transfer function. (3-21) is the uncompensated complete system transfer function.

3.2.3.2 PD Compensator

The PD compensator (also called lead compensator) is used to improve the phase margin. PD compensator acts like a high pass filter. The transfer function of PD compensator is

$$G_{C\_PD}(s) = G_{C\_PD0} \frac{\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_p}\right)} \tag{3-22}$$

Here, a zero is added to the loop gain at a frequency ω_z far below the overall system crossover frequency ω_c such that the phase margin is increased by the desired amount. $\omega_c=2\pi f_c$ and f_c is the crossover frequency in terms of Hz and is selected to be 50kHz in our design. A high frequency ω_p is also added to attenuate high-frequency noise. The fundamental goal of DC-DC is to regulate DC output.

If the compensator gain at the switching frequency is too big, then the switching harmonics are amplified by the compensator, eventually disrupting the operation of DPWM. By considering these constrains, ω_p is selected to be less than the switching frequency ω_s (ω_s =2π f_s). Particularly, to optimally obtain a compensator phase lead of θ at crossover frequency f_c, the pole and zero frequencies (ω_z and ω_p) are chosen as follows:

$$\omega_z = \omega_c \sqrt{\frac{1-\sin(\theta)}{1+\sin(\theta)}}$$
$$\omega_p = \omega_c \sqrt{\frac{1+\sin(\theta)}{1-\sin(\theta)}} \qquad (3\text{-}23)$$

To avoid changing the crossover frequency, the magnitude of the compensator gain is chosen to be unity at crossover frequency f_c. Thus G_{C_PD0} in equation (3-22) is chosen as

$$G_{C\_PD0} = \sqrt{\frac{\omega_z}{\omega_p}} \qquad (3\text{-}24)$$

3.2.3.3 PI Compensator

The PI compensator (also called lag compensator) is used to improve the DC and low-frequency loop gain. PI compensator acts as a low pass filter. The transfer function of PI compensator is

$$G_{C\_PI}(s) = G_{C\_PI\infty}\left(1+\frac{\omega_L}{s}\right) \qquad (3\text{-}25)$$

Here, a zero is added to the loop gain at a frequency ω_L. If ω_L is sufficiently lower than the crossover frequency ω_c, the phase margin is unchanged. The pole at the origin 1/s is added to make the DC loop gain arbitrarily large. Therefore the DC component of the error signal between V_{FB} and V_{REF} is almost zero. The steady state output voltage is perfectly regulated accordingly.

To obtain a desired crossover frequency ω_c, the PI compensator gain at very high frequency needs to be chosen as

$$G_{C\_PI\infty} = \frac{\omega_c}{T_{u0}\omega_0} \tag{3-26}$$

where ω_0 is defined in(3-16) and T_{u0} is from (3-21).

3.2.3.4 Combined PID Compensator

The product of the PD and PI compensator discussed can be expressed as

$$G_{c\_PID}(s) = G_{cm}\frac{\left(1+\frac{\omega_L}{s}\right)\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_p}\right)} \tag{3-27}$$

This is a 2-pole 2-zero system. In practice, an extra pole is added at high frequency to increase the gain margin. It helps to prevent the switching ripple from disrupting the DC-DC regulation. A typical combined PID compensator is therefore a 3-pole 2-zero system. This type of compensator is also called Type-III compensator. The corresponding transfer function of this compensator is

$$G_c(s) = G_{cm} \frac{\left(1+\frac{\omega_L}{s}\right)\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \tag{3-28}$$

The bode plot of the PID compensator in (3-28) is shown in Fig. 3.12.

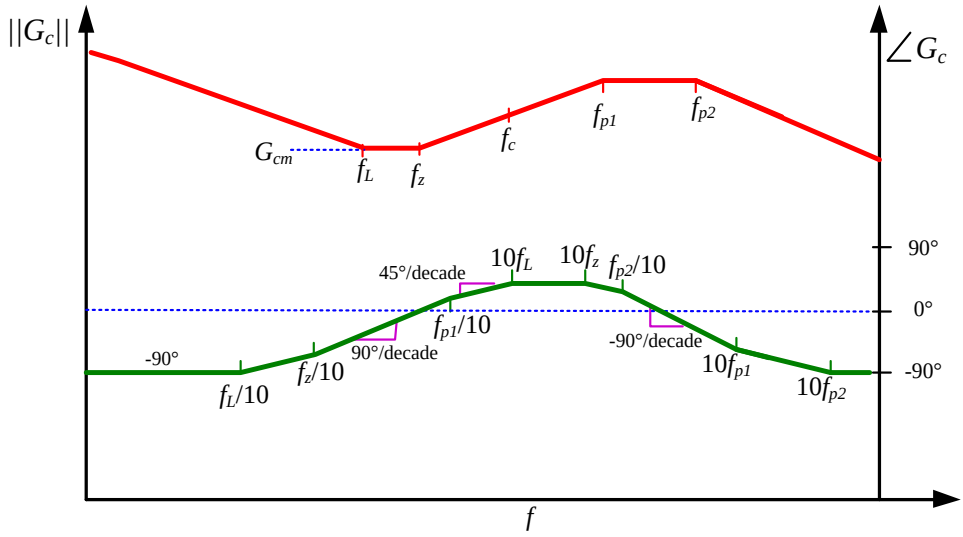


Fig. 3.12. Bode Plot of the Combined PID Compensator.

Equation (3-28) and Fig. 3.12 illustrate the poles and zeros in PID compensators. The inverted zero at ω_z is added to extend the bandwidth of the feedback loop while maintaining an acceptable phase margin. The zero at ω_L is used to increase the phase margin. The pole at the origin is inserted to boost the feedback loop DC gain to infinite large, thereby forcing the regulation error to be near zero. Two poles ω_{p1} and ω_{p2} are placed at high frequency to increase gain margin and to suppress the switching noise.

Once the PID compensator is designed in s-domain, we could convert the continuous-time s-domain transfer function to the corresponding discrete-time z-domain transfer function via bilinear (Tustin) approximation method. For a Type-III PID compensator, the converted z-domain transfer function generally has the form of

$$H(z)=\frac{a_0z^3+a_1z^2+a_2z+a_3}{z^3+b_1z^2+b_2z+b_3} \tag{3-29}$$

The system in (3-29) can be implemented by using the architecture illustrated in Fig. 3.13.

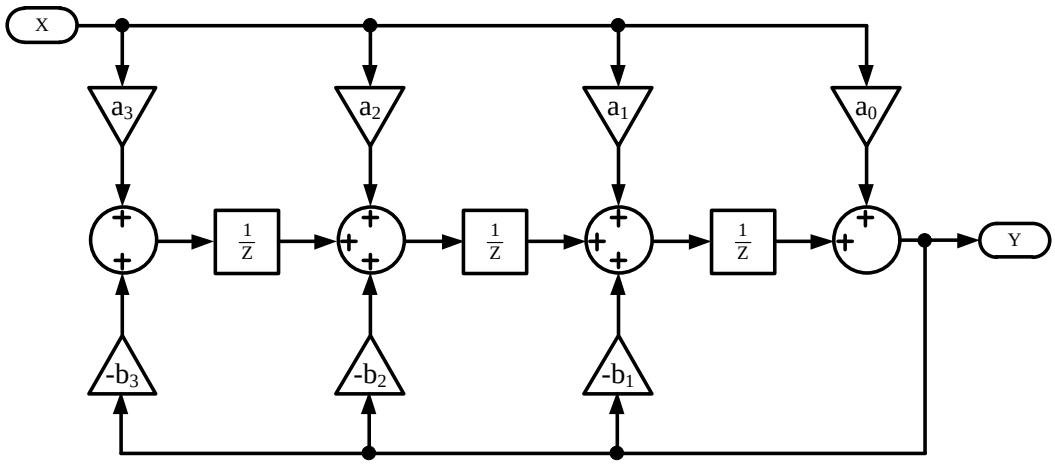


Fig. 3.13. Digital Implementation of PID Compensator.

Please notice that the power inductor DCR R_{DCR}, power capacitor ESR R_{ESR}, and the turn-on resistance R_{DS} of the power switches were not considered in previous discussion. The small signal model of the buck converter taking these components into account is shown in Fig. 3.14.

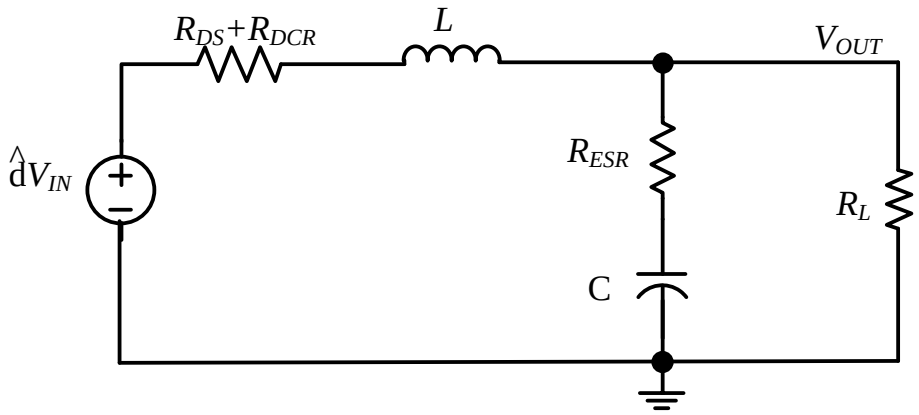


Fig. 3.14. Small Signal Model of Buck Converter.

After considering R_{DCR}, R_{ESR} and R_{DS}, the control-to-output transfer function from (3-14) becomes

$$G_{vd}(s)=\frac{V_{IN}}{R_L+R_D}\frac{1+sR_{ESR}C}{1+s\left(R_{ESR}C+\frac{R_LR_D}{R_L+R_D}C+\frac{L}{R_L+R_D}\right)+s^2LC\frac{R_L+R_{ESR}}{R_L+R_D}} \quad (3\text{-}30)$$

where R_D is the sum of power inductor DCR R_{DCR} and the power switch turn-on resistance R_{DS}:

$$R_D=R_{DS}+R_{DCR} \quad (3\text{-}31)$$

The required duty cycle from (3-18) becomes

$$D=\frac{V_{OUT}+\left(R_{DCR}+R_{DS\_N}\right)I_{LOAD}}{V_{IN}-\left(R_{DS\_P}-R_{DS\_N}\right)I_{LOAD}} \quad (3\text{-}32)$$

Here R_{DS_N} and R_{DS_P} are the R_{DS} of NMOS and PMOS power switches respectively. I_{LOAD} is the load current:

$$I_{LOAD}=\frac{V_{OUT}}{R_L} \quad (3\text{-}33)$$

The PID compensator designed in this work is demonstrated in the following figures. Fig. 3.15 shows the uncompensated complete system $T_u(S)$. It apparently shows very limited DC gain (less than 20dB) and insufficient phase margin (25˚).

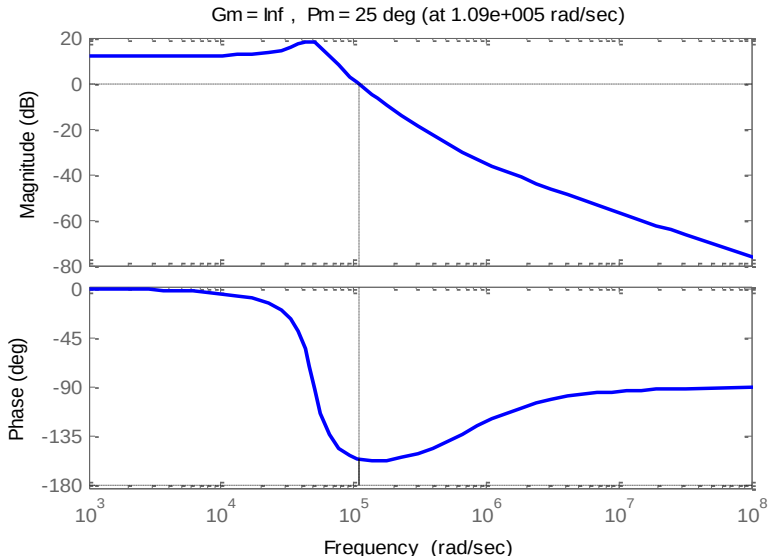


Fig. 3.15. Bode Plot of the Uncompensated Loop.

The constructed Type-III PID compensator is shown in Fig. 3.16. Fig. 3.17 is the compensated overall system. The crossover frequency f_c is selected to be 50kHz, i.e. 1/10 of the DC-DC switching frequency 500kHz. The phase margin is designed around 70 degree. This is to ensure the system's stability over certain range of input voltage, load current etc.

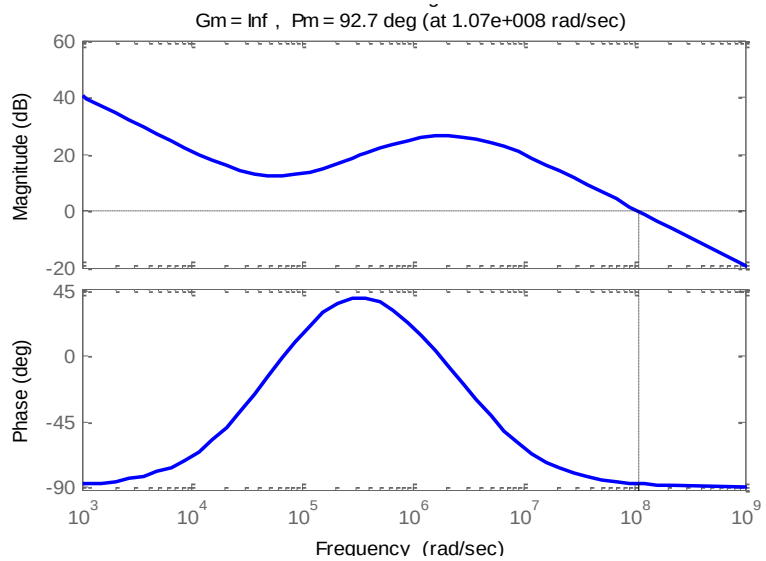


Fig. 3.16. Bode Plot of the PID Compensator.

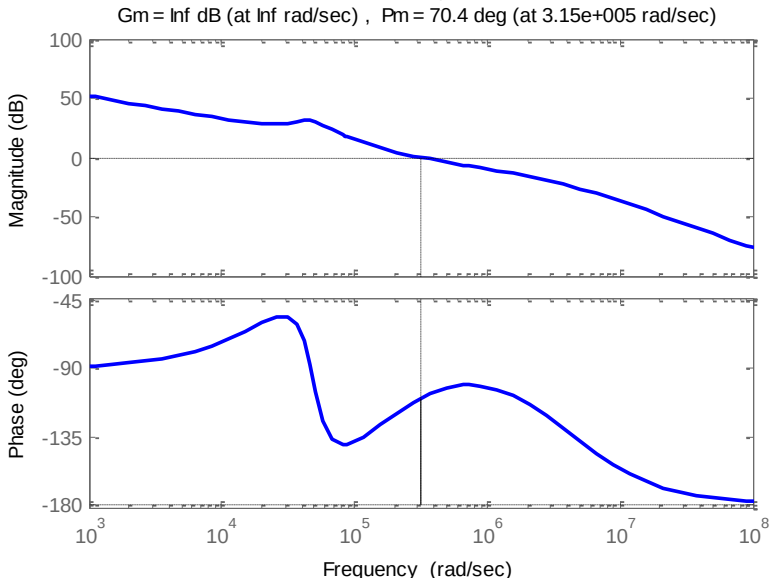


Fig. 3.17. Bode Plot of the Compensated Complete System.

The values of all components and other parameters used in the PID design are summarized in Table 3.1.

Table 3.1. Summary of Parameters Used in PID Compensator Design.

Inductor	L = 18μH	R_{DCR} = 60mΩ
Capacitor	C = 22μF	R_{ESR} = 70mΩ
I/O Voltage	V_{IN} = 5V	V_{OUT} = 3.3V
Feedback	H = 0.6	V_{REF} = 1.98V
Other	R_{DS_P}= R_{DS_N} =150mΩ	I_{LOAD} = 0.3A

3.2.4 Level Shifter

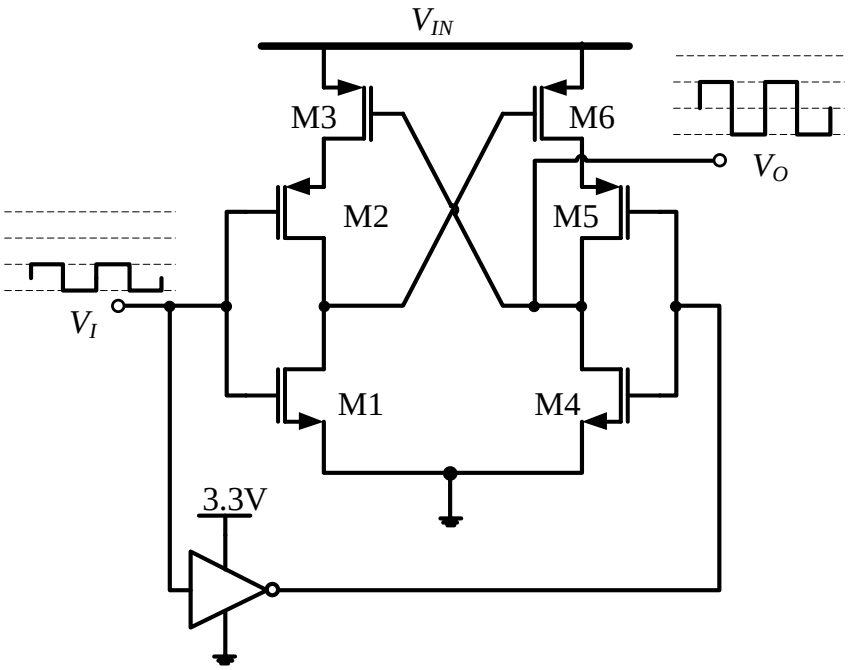


Fig. 3.18. Level Shifter.

The targeted maximum input voltage of our DC-DC is 5.5V. To achieve high efficiency DC-DC, we minimized DC-DC power consumption by using 3.3V supply for all the analog and digital blocks except the power stage which runs at

V_{IN} supply. A level shifter is therefore required to boost the voltage swing range [0V, 3.3V] to the desired [0V, V_{IN}] level to drive the power MOSFETS. The architecture of the level shifter is shown in Fig. 3.18. Two more PMOS transistors (M2 and M5) were added to the conventional level shifter to speed up the transitions of the level-shifter output signal.

3.2.5 Power Stage Driver

Power switches are crucial in switching mode DC-DC converters. Power switches can be one of PMOS-NMOS, NMOS-NMOS or PMOS-Diode combinations. In PMOS-Diode combination, the rectifying diode incurs large power loss. The power dissipated is simply the forward voltage drop multiplied by the current going through it. The reverse recovery for silicon diodes can also create loss. To minimize this loss, the rectifier can use Schotty diode which has a lower forward voltage drop and good reverse recovery. In PMOS-NMOS, NMOS-NMOS combinations, a MOSFET instead of a diode is used as the rectifier. MOSFET rectifier is also called synchronous rectifier since the current is always conducting between the main switch and NMOS rectifier in every switching cycle. In this work PMOS-NMOS combination is used in the switch stage. PMOS-NMOS combination has higher efficiency advantage over the PMOS-Diode topology but comes with a little more complicated gate drive.

A power stage driver with built-in dead time proposed in [53] is used in this DC-DC core. The main idea of this power stage driver is to turn off one power FET before turning on the other power FET. This is important to avoid shoot through current which, in addition to causing unnecessary power consumption, it may cause damage to the whole system. The circuitry of the built-in dead time driver is shown in Fig. 3.19.

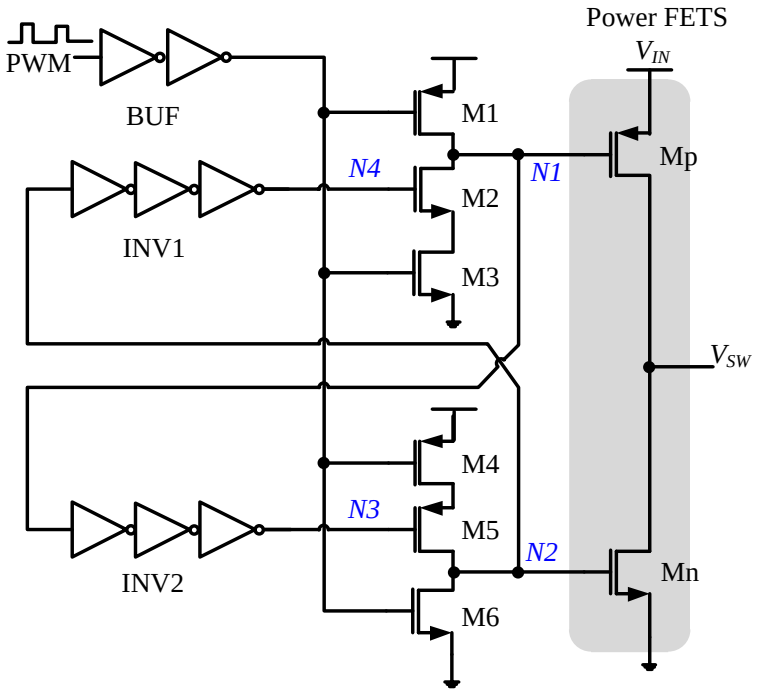


Fig. 3.19. Power Stage Driver with Built-In Dead Time.

As shown in Fig. 3.19, if the input PWM signal is logic high, M1 and M4 are turned off, M3 and M6 are turned on, node *N2* is pulled down to ground, thus the power switch Mn is turned off right away. After the inverter chain INV1, node

N4 is pulled up to logic high after a certain amount delay. When *N4* eventually reaches logic high, M2 is turned on and node *N1* is pulled down. Power switch Mp is on. So when PMW signal is logic high, power switch Mn is turned off first before power switch Mp is turned on. Similarly, when PWM signal is logic low, power switch Mp is turned off before Mn is turned on. The time period when both Mp and Mn are turned off is called dead time. The shoot through current is avoided by adding this built-in dead time.

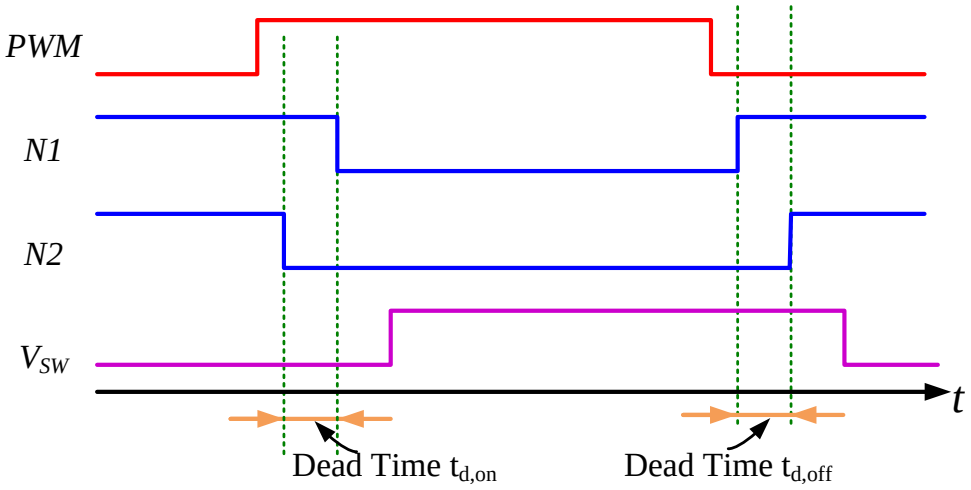


Fig. 3.20. Illustration of the Dead Time in Power Stage Driver.

The waveforms of the nodes in the power stage driver are shown in Fig. 3.20. In more advanced power stage driver, the dead time can be controlled to achieve optimal DC-DC efficiency [54].

CHAPTER 4

INDUCTOR BIST AND CURRENT SENSING ARCHITECTURE

As discussed in Chapter 2, although there are many existing current sensing techniques, we are still lacking an integrated, lossless, accurate, hardware and power efficient current-sensing technique which is required by state-of-the-art switching regulators. In this chapter, an offset-independent inductor BIST architecture is proposed to measure the inductor inductance and DCR. The measured DCR enables the proposed continuous, lossless, average current sensing scheme which will be discussed in detailed in this chapter.

4.1 Inductor BIST Architecture

One of the key contributions in our DC-DC converter system is the offset independent inductor BIST as shown in Fig. 4.1. During BIST mode, the power train is put into high impedance mode by cutting off the power stage PMOS and NMOS. Meanwhile, the inductor is isolated by shorting the load capacitor to ground. Due to a differential measurement, the R_{DS} of the FET shorting the filter capacitor does not need to be low. Following these steps, a symmetric triangular current I_{TRI} is applied to the inductor. The voltage across the inductor V_{IND} is amplified by a non-inverting, resistor-feedback differential sense amplifier (SA). The gain of SA is set by resistor ratio R_F/R_G. The output of this sense amplifier

V_{DIFF} is digitized by a ΔΣ ADC described in section 3.2.2. The digital code is then sent to a post-processing block. L and R_{DCR} are calculated here. The measured L can be used to update PID compensator to minimize the impact of inductor variation and R_{DCR} is used in load current I_{LOAD} computation.

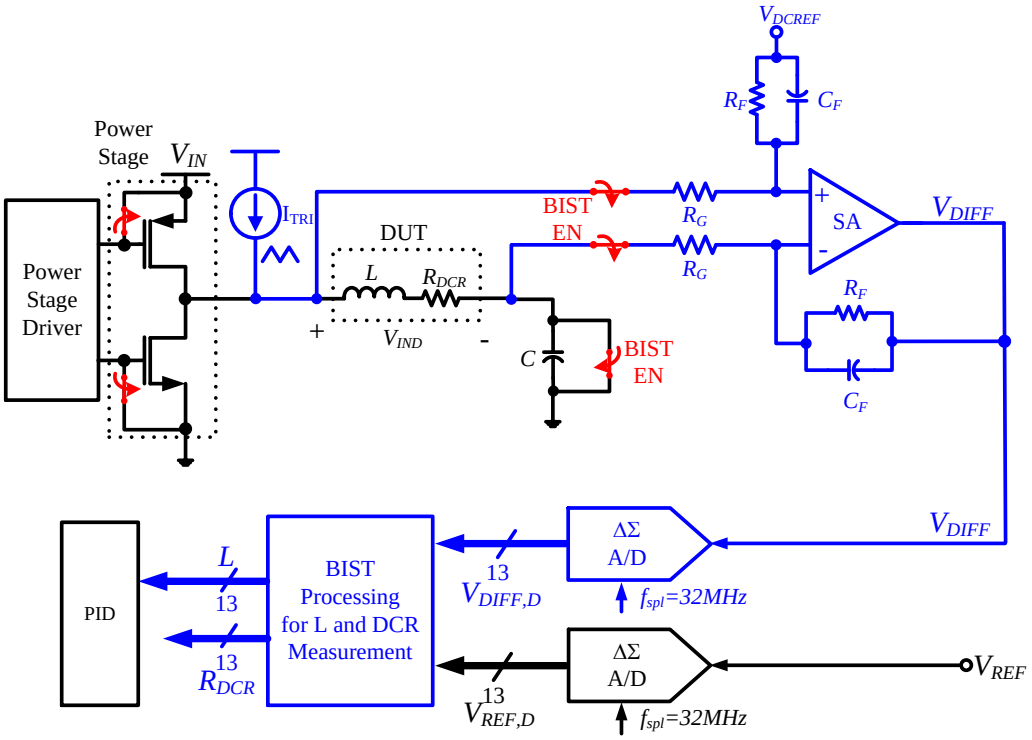


Fig. 4.1. Overall Inductor BIST Architecture.

The extra hardware modules required for inductor BIST feature are a symmetrical triangular current source, a sense amplifier, an extra ΔΣ ADC and a digital processing block for the inductance and DCR computation.

4.1.1 Inductance and DCR measurement

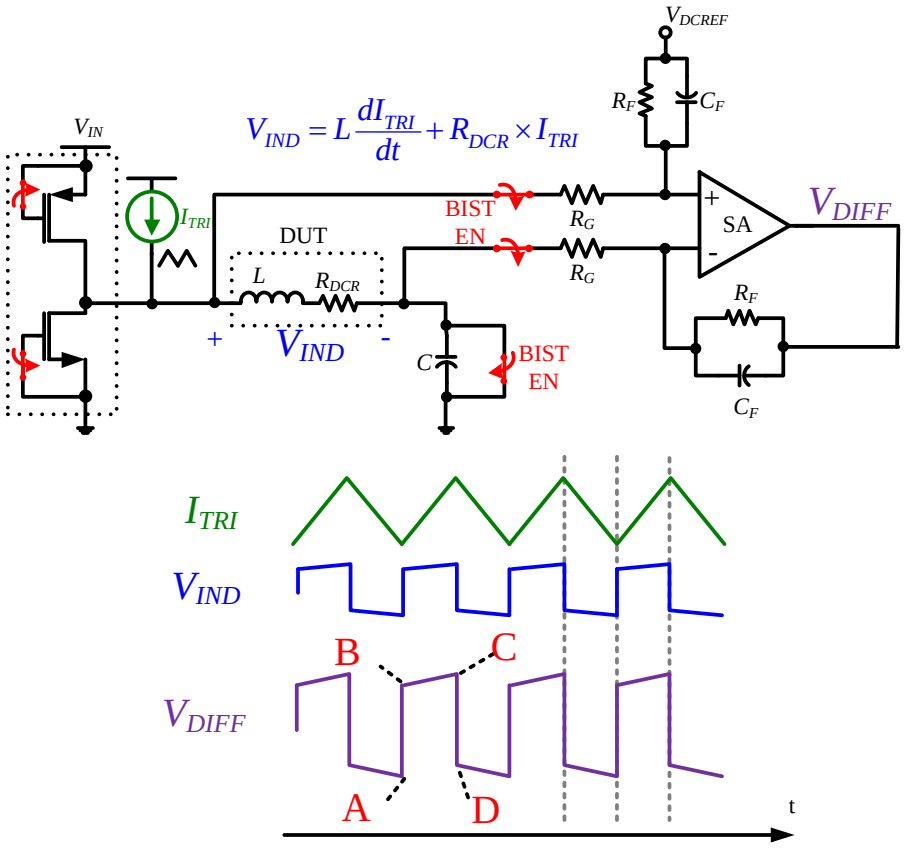


Fig. 4.2. Illustration of Inductance and DCR measurement.

The proposed BIST architecture obtains the inductance and DCR by detecting differential sense amplifier output. Let *Slope* be the triangular current source I_{TRI} slope, the voltage across the inductor under BIST mode V_{IND} is defined as $V_{IND} = L \times Slope + I_{TRI} \times R_{DCR}$ .When applying a triangular current over the inductor, V_{IND} is a trapezoidal waveform as shown Fig. 4.2. After the differential amplifier, the waveform has a similar shape and larger amplitude. There are several critical

time instances that we use to calculate L and DCR. They are marked by A, B, C and D in Fig. 4.2.

Consider the rising part of I_{TRI} from the minimum triangular current $I_{TRI,min}$ to the maximum triangular current $I_{TRI,max}$, i.e. from time point B to time point C, as *slope* maintains the same, the change of V_{IND} is only contributed by R_{DCR}, i.e.$(I_{ITR,max}$-$I_{TRI,min})\times R_{DCR}$. Similarly, at the peak I_{TRI} instance, i.e. time point A and B, I_{TRI} maintains $I_{TRI,max}$ but slope changes from rising part *slope* to falling part -*slope*, and V_{IND} has a change of $2\times Slope\times L$ correspondingly. When we look at SA's output V_{DIFF}, since it's the exact same sense amplifier, the SA input-referred offset V_{offset} and common mode level V_{DC} at time instance A, B and C should be the same. V_{DIFF} change from A to B only results from I_{TRI} slope change. V_{DIFF} change from point B to C only results from I_{TRI} value change. The values of the SA's output V_{DIFF} at different time instances are given by

$$\begin{aligned} V_{DIFF,A} &= (-L\times Slope + R_{DCR}\times I_{TRI,\min} + V_{offset}\times\frac{R_F+R_G}{R_F})\times\frac{R_F}{R_G}+V_{DC} \\ V_{DIFF,B} &= (+L\times Slope + R_{DCR}\times I_{TRI,\min} + V_{offset}\times\frac{R_F+R_G}{R_F})\times\frac{R_F}{R_G}+V_{DC} \\ V_{DIFF,C} &= (+L\times Slope + R_{DCR}\times I_{TRI,\max} + V_{offset}\times\frac{R_F+R_G}{R_F})\times\frac{R_F}{R_G}+V_{DC} \end{aligned} \quad (4\text{-}1)$$

where R_{DCR} is the DCR of the power inductor. From (4-1), L can be obtained by measuring the V_{DIFF} change ($V_{DIFF,B}$-$V_{DIFF,A}$) and DCR by measuring V_{DIFF} change ($V_{DIFF,C}$-$V_{DIFF,B}$).

$$L = \frac{V_{DIFF,B} - V_{DIFF,A}}{2 \times Slope} \times \frac{R_G}{R_F}, \quad R_{DCR} = \frac{V_{DIFF,C} - V_{DIFF,B}}{I_{TRI,\max} - I_{TRI,\min}} \times \frac{R_G}{R_F} \qquad (4\text{-}2)$$

From above equation, we can notice that the measured L and DCR do not dependent on the common mode level or input referred offset of the SA. This is one advantage of this inductor BIST architecture. The traditionally analog offset cancellation requires two identical sensing units [40]. In this work, due to the digital offset cancellation, only one sensing unit is needed.

4.1.2 Triangular Current Generator

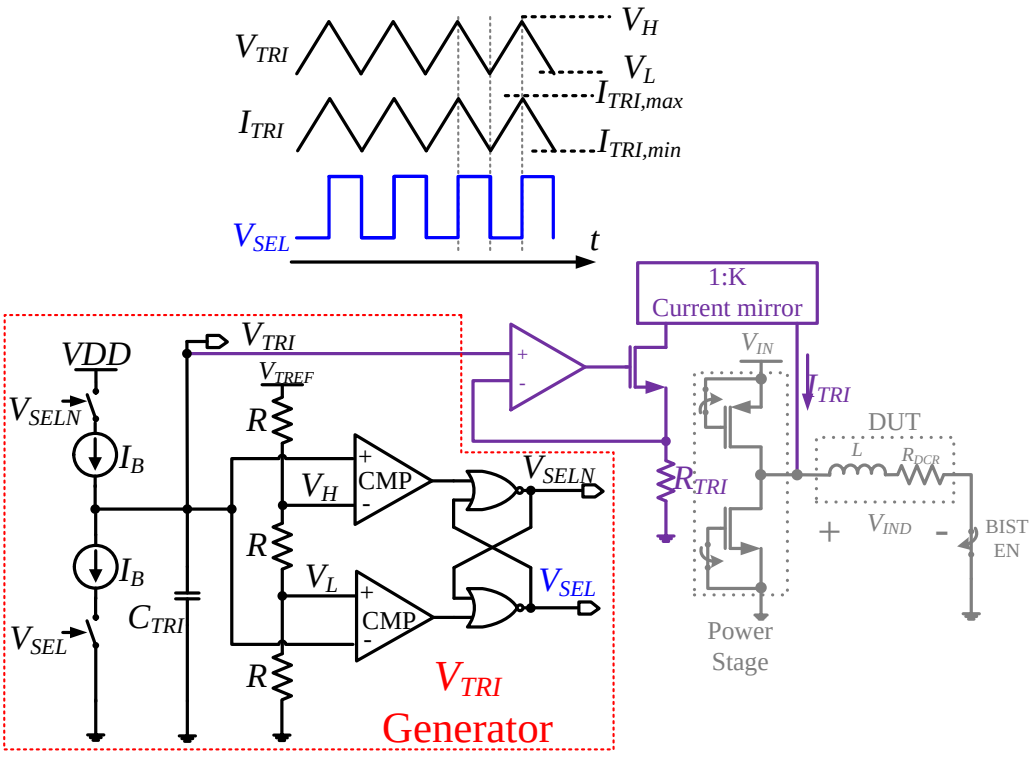


Fig. 4.3. Triangular Current Generator.

The inductor BIST approach requires a triangular current source I_{TRI} whose parameters, for example, the *Slope*, $I_{TRI,min}$ and $I_{TRI,max}$, are controllable. Also, we

need circuits to detect those time instants that amplifier's output should be sampled. All these functions are achieved by our triangular current generator shown in Fig. 4.3.

Triangular current I_{TRI} generator consists of a triangular voltage V_{TRI} generator followed by a linear V-I converter. V_{TRI} is generated by applying a matched charge and discharge bias current pair I_B to a known capacitor C_{TRI}. The charge and discharge times are controlled by two comparators followed by an R-S flip-flop. V_{TRI} maximum voltage V_H and minimum voltage V_L are precisely set by matched series resistors. I_{TRI} slope is controlled by bias I_B and V-I converter current mirror ratio. The maximum and minimum triangular current values are controlled by the series resistor ratio and current mirror ratio. The comparator output V_{SEL} and its one clock delayed signal $V_{SEL,Delay}$ are used as clock signals to detect and differentiate the output V_{DIFF} maximum and minimum values at peak triangular current instance.

There is a constraint of the triangular current generator that needs to be considered. As the power FETs are generally in huge size, the parasitic capacitances such as Cgd can be as much as ~100pF. Meantime, the power inductor is very large (normally ~10μH). The Self-Resonance Frequency (SRF) of

switching node due to the parasitic capacitance *Cp* and power inductor *L* can be very low. The SRF of LC circuits is defined as

$$SRF = \frac{1}{2\pi\sqrt{LC_P}} \tag{4-3}$$

SRF could be as low as ~1MHz range. To avoid the potential resonance resulting from large inductance and parasitic capacitance of power FETs, I_{TRI} frequency is limited to 10kHz. This is 2 orders away from the SRF. Thus, we can obtain steep edges of V_{DIFF} which are required by *L* and DCR measurement.

4.1.2.1 Charge Pump

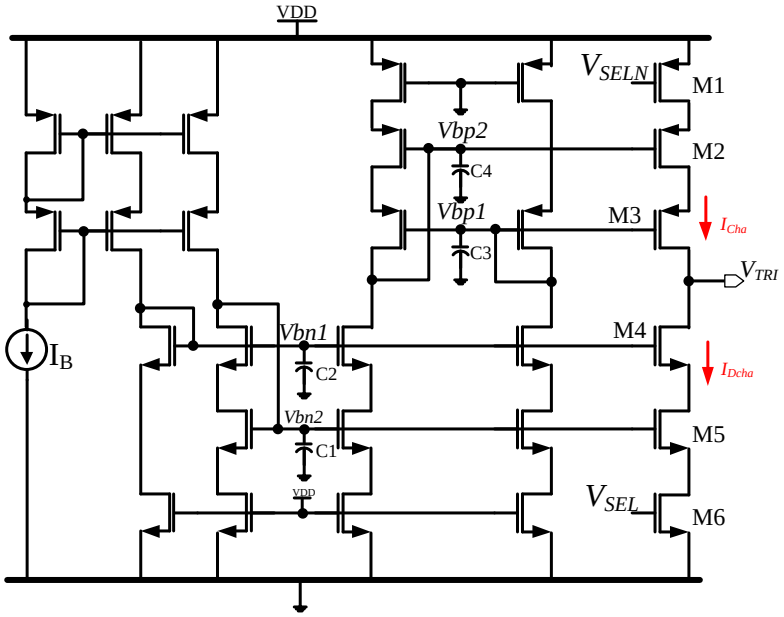


Fig. 4.4. Charge Pump in Triangular Current Generator.

Charge pump in the triangular current generator is very crucial for inductor BIST. First of all, a good symmetry of the triangular current source is required for

the inductance measurement. A good matching between the charge and discharge current biases in the charge pump is therefore indispensable. Secondly, as the switching node is highly sensitive to as low as ~1MHz range signals, the transitions of triangular current, e.g. from rising part to the fall part, need to be performed smoothly without bringing switching noise component. Thus the charge pump needs to be designed to suppress switching noise as much as possible.

The charge pump in this triangular current generator is shown in Fig. 4.4. To obtain good matching of the charge current I_{Cha} and the discharge current I_{Dcha}, wide-swing current mirrors are utilized in both PMOS and NMOS sides. The switching transistors are placed to the source side of the current mirror transistors. Thus the switching noise can be isolated by cascaded bias transistors. Moreover, four bypass capacitors are also connected to bias voltage nodes to stabilize the current biases and absorb switching noise.

4.1.2.2 Hysteric Comparator

Two comparators are needed in the triangular current generator to control the maximum and minimum triangular voltage levels. Shown in Fig. 4.5 is the hysteric comparator used.

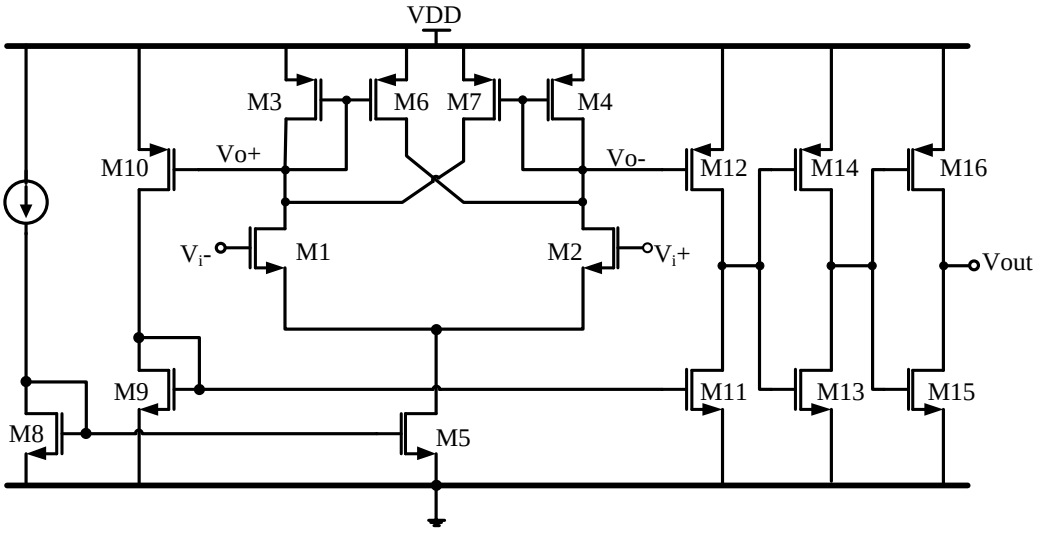


Fig. 4.5. Hysteric Comparator in Triangular Current Generator.

The comparator is implemented by a differential pair with positive feedback to provide a high gain [59][60]. The gain of the positive feedback gain stage is

$$A_V = \sqrt{\frac{\mu_n \left(\frac{W}{L}\right)_1}{\mu_p \left(\frac{W}{L}\right)_3}} \frac{1}{1-\alpha} \tag{4-4}$$

Here $\alpha=(W/L)_6/(W/L)_3$ is the positive feedback factor. The inverter chain formed by M11-M16 is added to the gain stage to improve the transient performance of the comparator output signal.

4.1.3 ADC Gain Calibration

From previous sections, we discussed how to obtain *L* and DCR based on the differential amplifier's output V_{DIFF} and the computation is summarized in (4-2). In this work, A ΔΣ ADC is used to digitize the V_{DIFF}. After the digitization, all

arithmetic computation in (4-2) such as subtraction, multiplications are completed in digital domain.

When using frequency domain ΔΣ ADC for digitization, the digitized code is proportional to VCO output frequency f_{VCO} and VCO gain. VCO gain drift will result in digitized code drift. To achieve a stable ΔΣ ADC, matched VCOs are used in V_{REF} and V_{DIEF} digitization ΔΣ ADCs. Since the DC-DC regulator reference voltage V_{REF} is normally a known value, by comparing the digitized code $V_{REF,D}$ and V_{REF}, we can monitor the ΔΣ ADC gain. The monitored ADC gain is used to normalize the digitized code of SA output, i.e. $V_{DIFF,D}$ so the code does not drift across temperature and process variations.

4.1.4 Power Stage Driver Modification

Under inductor BIST mode, the built-in dead time power stage driver in DC-DC VMC buck converter core does not function properly. It contains short paths from power supply to ground. A modified power state driver is therefore introduced in this section to provide the required features for both DC-DC normal regulation and inductor BIST.

4.1.4.1 Short Path Issue

The short path issue is illustrated in Fig. 4.6. During inductor BIST mode, the power FETs Mp and Mn are switched off to isolate the inductor. Thus node *N1* is

logic ‘1’ and node *N2* is logic ‘0’. Node *N3* and *N4* are ‘0’ and ‘1’ respectively as they are inverted and delayed signals of *N1* and *N2*. M2 and M5 are therefore turned on. This traditional driver has direct short path between power supply and ground and results in logic error. As shown in Fig. 4.6, if the input PWM signal ‘X’ is in ‘0’, M4 is turned on and there is a short path from V_{IN} to ground at the power NMOS side. If the input PWM signal ‘X’ is in logic ‘1’, M3 is turned on, there is a short path from V_{IN} to ground at the power PMOS side. To avoid the short pass issue, a modification of the power stage driver must be made.

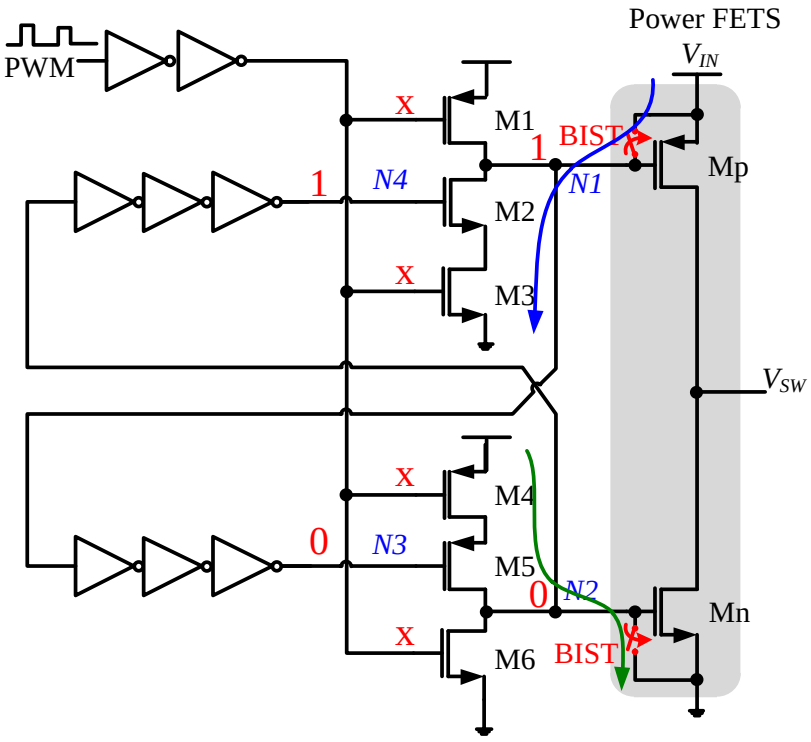


Fig. 4.6. Illustration of Short Paths in Conventional Power Stage Driver.

4.1.4.2 Modified Power Stage Driver

The modified power stage driver is shown in Fig. 4.7. Three 2-to-1 MUXs are added in front of node *N3*, *N4* and after PWM input signal respectively.

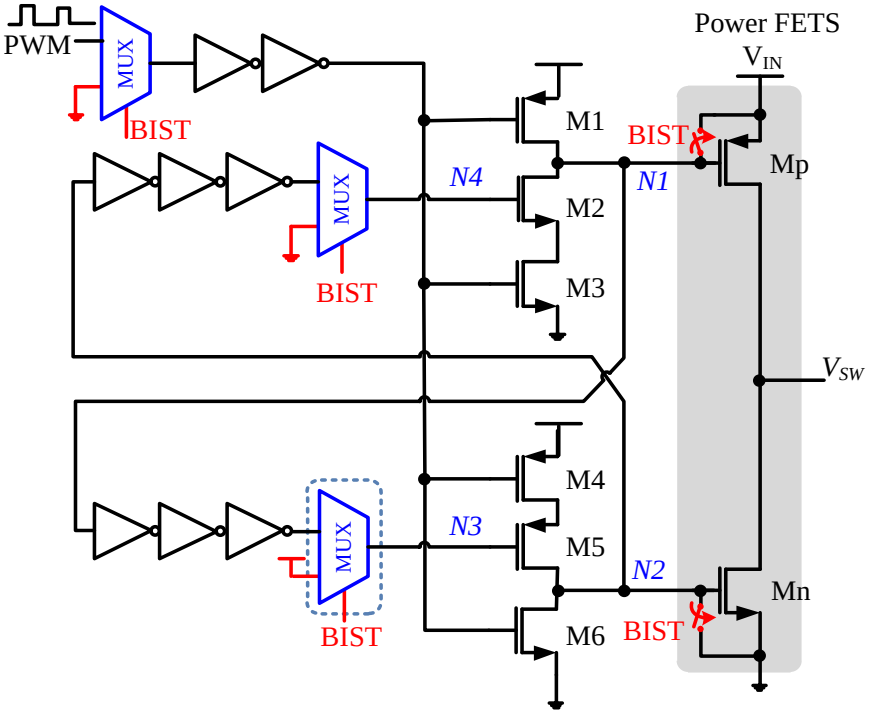


Fig. 4.7. Modified Power Stage Driver with Built-In Dead Time.

In normal DC-DC regulation mode, the enable signal BIST is '0'. As shown in Fig. 4.7, the modified driver works as same as the traditional power stage driver in Fig. 4.6. Under BIST mode, node *N1* is pulled up to switch Mp off, node *N2* is pulled down to turn Mn off. The enable signal BIST is logic '1', MUX put node *N4* to '0' and *N3* to '1' such that M2 and M5 are always switched off. As a

result, both short paths shown in Fig. 4.6 are prevented. Also the PWM signal is blocked outside of the driver so it does not bring any noise injection.

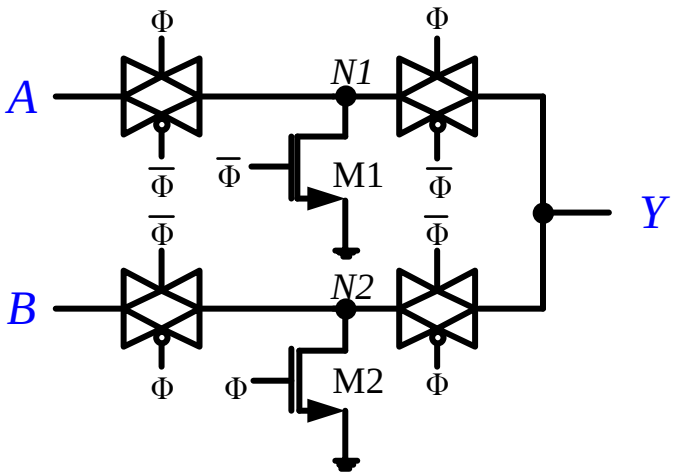


Fig. 4.8. MUX in Modified Power Stage Driver.

The MUX in the modified driver uses T-shape transmission gate based configuration as shown in Fig. 4.8. Due to the usage of transmission gates rather than the standard digital logic gates, the drive abilities of inverter chains in the driver can be preserved. At the same time, T-shape transmission gate is able to isolate the noise injection of one way when the other way is selected. In Fig. 4.8 for example, when select signal Φ is '1', path A is selected. The MUX output *Y* equals to the input *A*. At the same time, M2 is also turned on to short the node *N2* to ground. Thus the switching on MUX input *B* has no impact on MUX output *Y*. This is especially attractive during normal DC-DC regulation.

4.2 Current Sensing Architecture

The measured inductor DCR by inductor BIST circuit is used for our current sensing technique shown in Fig. 4.9.

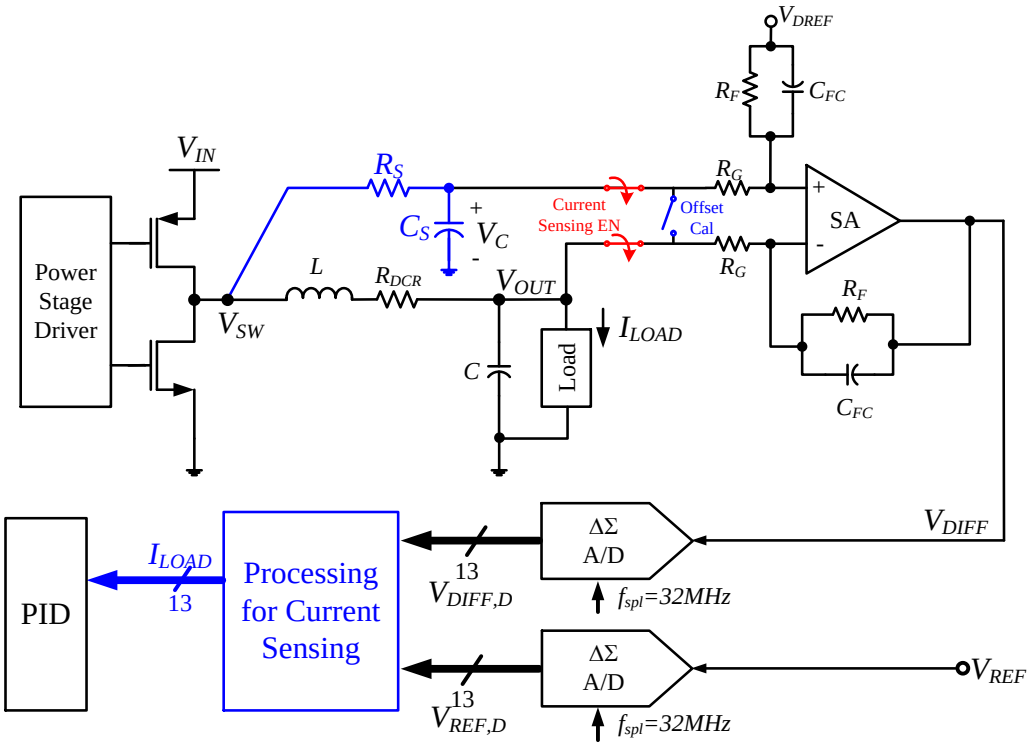


Fig. 4.9. Proposed Current Sensing Architecture.

The current sensing is based on the average current sensing technique proposed in [55]. To sense the load current, an RC network set by R_S and C_S is added in parallel to the power MOSFETS switching node V_{SW}. The difference of the regulator steady state output V_{OUT} and the RC filter output V_C is amplified by a resistor feedback non-inverting differential sense amplifier. The amplifier's output V_{DIFF} is digitized by the frequency ΔΣADC. The digitized V_{DIFF} is then sent to a

post-processing block which calculates the load current I_{LOAD} based on the digitized amplifier's output. This current sensing architecture shares the same SA and the digitization ΔΣADC with inductor BIST architecture. The only extra hardware cost for current sensing comes from the RC filter and digital post-processing block.

A table look-up approach based compensator is used in the digital voltage mode controlled DC-DC buck converter control loop. The sensed load current is utilized to select suitable prestored PID coefficient set, thereby achieves quasi load independent control. The details of this programmable compensator are discussed in later chapters.

4.2.1.1 Current Sensing Theory

When applying an ideal LC filter or an RC filter to the switching node V_{SW}, the DC component of the filter output should be the same, i.e., the average of V_{SW}. Here in the buck converter, V_{OUT} is the LC filter output and V_C is RC filter output. The difference of the V_{OUT} and V_C is due to the existence of inductor DCR. From the average current sensing theory [55], we have:

$$\bar{V}_C - \bar{V}_{OUT} = I_{LOAD} R_{DCR} \tag{4-5}$$

In our current sensing architecture, the difference of the V_{OUT} and V_C is amplified by the differential amplifier. The output of the SA is then

$$\bar{V}_{DIFF} = I_{LOAD} \times R_{DCR} \times \frac{R_F}{R_G} \tag{4-6}$$

Here R_F/R_G is the SA's gain which can be preciously controlled by layout matching. By considering the sense amplifier's offset and output DC level $V_{DIFF,offset,DC}$, the SA's output is given by

$$\bar{V}_{DIFF} = I_{LOAD} \times R_{DCR} \times \frac{R_F}{R_G} + V_{DIFF,offset,DC} \tag{4-7}$$

We then could obtain the load current

$$I_{LOAD} = \frac{\bar{V}_{DIFF} - V_{DIFF,offset,DC}}{R_{DCR}} \times \frac{R_G}{R_F} \tag{4-8}$$

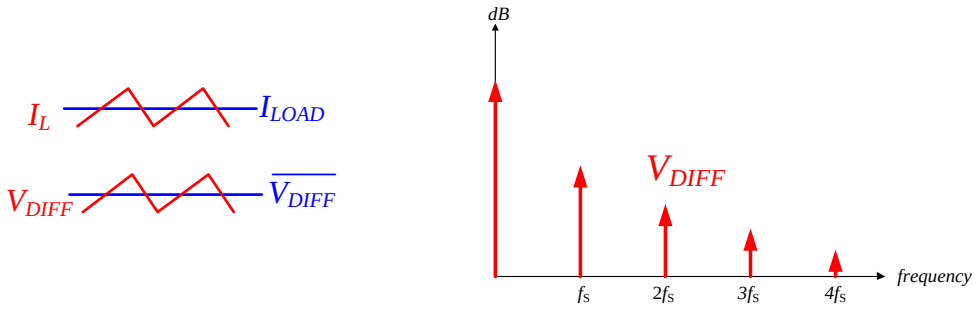
As we can see form (4-8), the load current does not depend on absolute values of *Rs* and *Cs*, so they can be integrated on-chip. The power FETs resistance R_{DS} does not affect the current sensing accuracy either. Once the SA output V_{DIFF} is digitized, all these arithmetic operations in (4-8) such as subtraction, multiplication etc are completed in digital domain.

To eliminate the effects of SA offset and DC level, the SA's input is shorted by turning on switch *Offset_Cal* in Fig. 4.9 before load current measurement. The readout chain offset is digitally restored. In current sensing mode, it is subtracted in digital domain.

4.2.1.2 SA Output Averaging

Equation (4-8) indicates that an averaging operation of V_{DIFF} is required to obtain the load current. An intuitive method is to take multiple instantaneous samples within one period and then take the arithmetic average value of them. A similar approach with a digital implementation optimization based on this idea is already discussed in section 2.2.2. In this work, a different and more efficient method is used.

In DC-DC buck converters, the inductor current I_L, the steady state output V_{OUT} and the RC filter output V_C in current sensing scheme all are triangular waveforms. Thus, the SA's input signal, i.e. the difference of V_{OUT} and V_C, is a triangular waveform as well. The frequency for these triangular waveforms is the DC-DC switching frequency f_s. The spectrum for this type of triangular waveform is a DC component plus harmonics at multiples of f_s.



(a) (b)

Fig. 4.10. SA Output V_{DIFF} (a) Time-Domain (b) Spectrum.

The SA output V_{DIFF} has similar spectrum as shown in Fig. 4.10. V_{DIFF} does not have an ideal triangular waveform spectrum as V_{DIFF} has attenuated high frequency harmonics due to the low pass filter formed by *Rs* and *Cs*. Also the limited bandwidth of the SA itself will shape the high frequency components.

The digitization of V_{DIFF} is performed by our frequency ΔΣ ADC which is illustrated in Fig. 4.11.

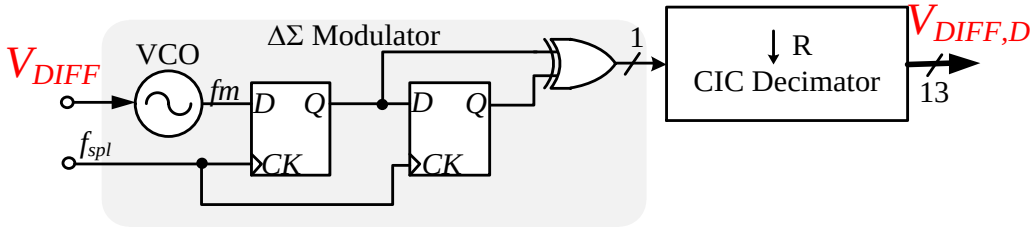


Fig. 4.11. V_{DIFF} Digitization.

Recall the magnitude response of the CIC decimator:

$$\left|H(\hat{f})\right| \approx \left|RM\frac{\sin(\pi M\hat{f})}{\pi M\hat{f}}\right|^{N} \quad \text{for } 0 \le \hat{f} \le \frac{1}{M} \tag{3-9}$$

We notice that CIC filter has transmission zeros at multiples of $\hat{f}/M$. Here $\hat{f}$ is the frequency relative to the low sampling rate f_{spl}/R, which is f_s in this scenario. The differential delay *M* is selected to be 1 in this work. Therefore, the CIC filter has nulls at multiples of f_s. The spectrum of the CIC decimator is depicted in Fig. 4.12.

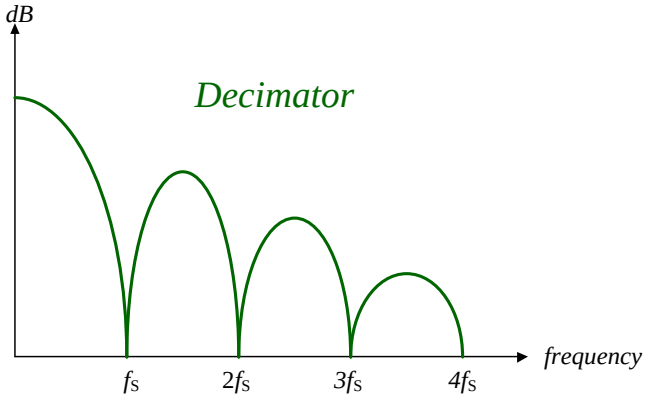
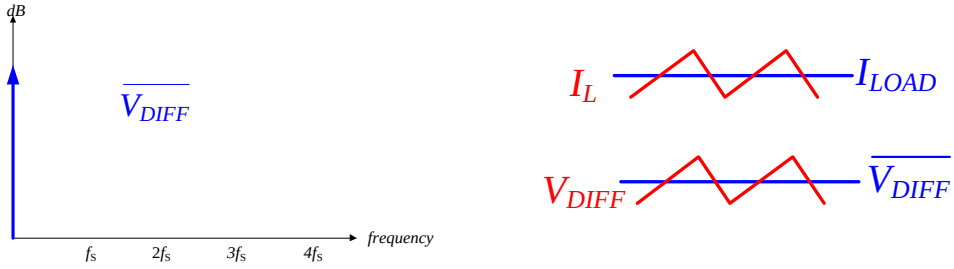


Fig. 4.12. Spectrum of CIC Decimator.

By using this ΔΣ ADC to digitize V_{DIFF}, the DC component which contains the information of load current is amplified by decimator gain. For a 2-stage CIC filter, the gain is R^2. The V_{DIFF} ripple which results from the inductor ripple is significantly suppressed. Since the harmonics at multiples of f_s are eliminated, the remaining signal at the ΔΣ ADC output is the DC component of V_{DIFF}, which is the average V_{DIFF} we wanted. The spectrum and time domain signals of ΔΣ ADC output are demonstrated in Fig. 4.13



(a) (b)

Fig. 4.13. Digitized V_{DIFF} (a) Spectrum (b) Equivalent Time Domain Signal

The analysis of SA output averaging by CIC filter itself is only for steady state. During the load transition, the spectrum for the inductor current and SA

output average V_{DIFF} are more complicated, but this averaging method is overall very attractive due to its simplicity and effectiveness.

CHAPTER 5

DIGITAL VMC BUCK CONVERTER MEASUREMENT

The proposed inductor BIST and current sensing architectures together with the DC-DC VMC buck converter core are implemented in high voltage AMI i2t100 0.7µm power CMOS process. The die micrograph is shown in Fig. 5.1. The chip size is 3.5mm by 3.5mm. The extra hardware cost for BIST and current sensing including related pads is 5.2% of the total chip area.

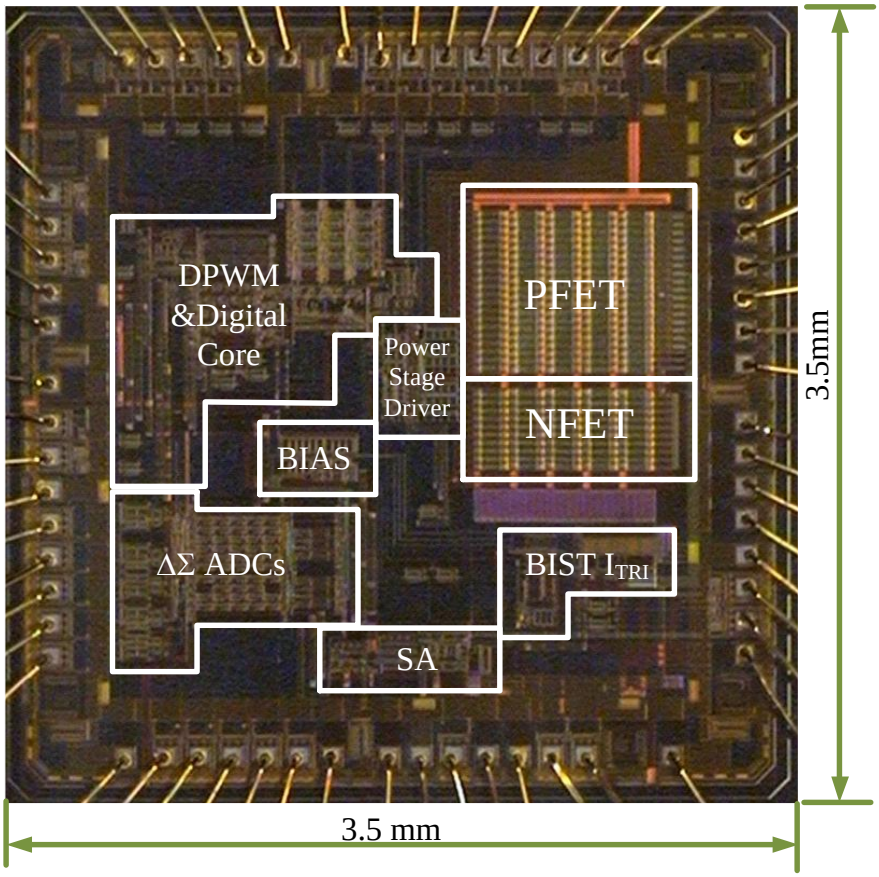


Fig. 5.1. Digital VMC Buck Converter Die Micrograph.

5.1 PCB Design and Test Setup

A test Print Circuit Board (PCB) is designed for the digital VMC buck converter verification and test. The PCB has two metal layers and uses the standard FR4 board material. The size of the PCB is 6.63 inch by 5.86 inch. The photo of the PCB with all the components soldered is shown in Fig. 5.2.

The test board can perform comprehensive tests and measurement including inductor BIST function test, DC-DC normal load regulation test, DC-DC efficiency test and key individual modules test including DLL, DPWM etc.

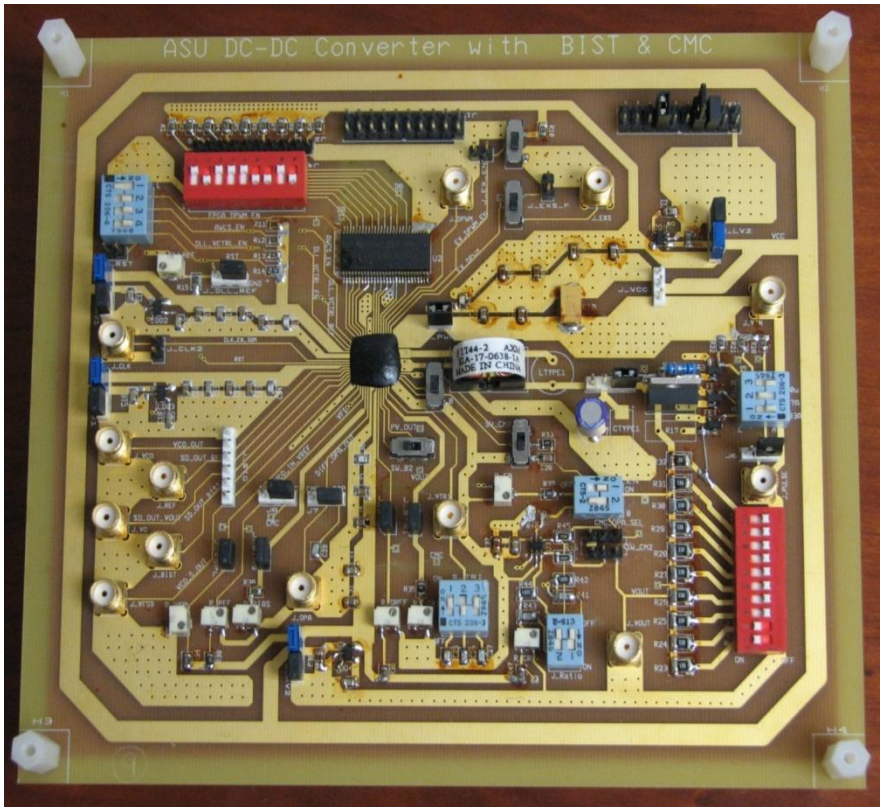


Fig. 5.2. Digital VMC Buck Converter Test Board.

The lab setup is demonstrated in Fig. 5.6. One arbitrary function generator is used to provide the clock signal of the chip. Another arbitrary function generator provides the load regulation switching control signal. The oscilloscope monitors the signals to be observed. When testing BIST and current sensing accuracy, a logic analyzer is utilized to track the output digital codes of ΔΣ ADCs. A spectrum analyzer is used to measure the DC-DC key output signals spectrum. Current meters and voltage meters are used to measure the DC-DC efficiency.

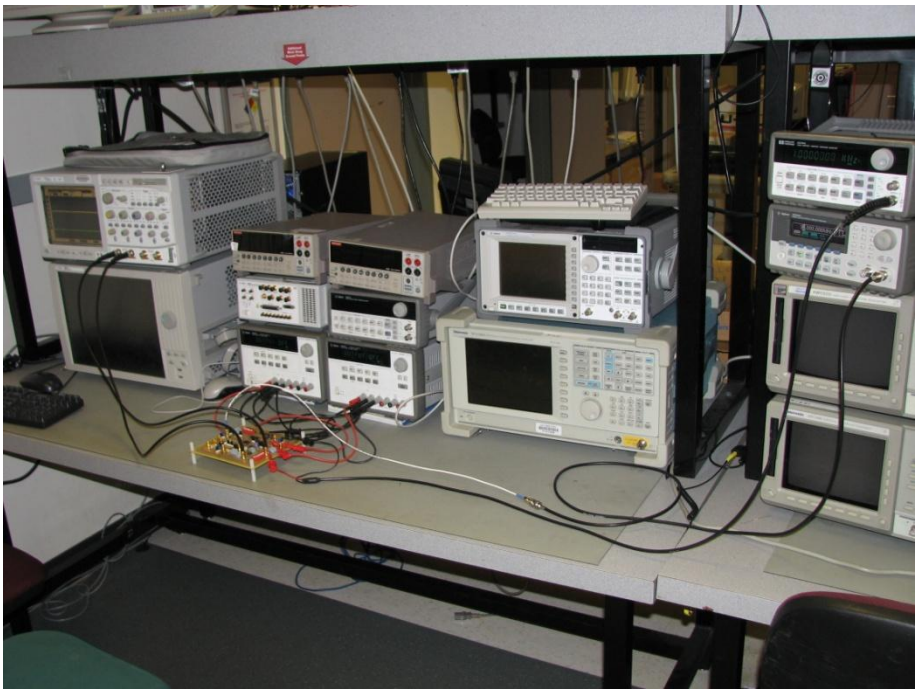


Fig. 5.3. Digital VMC Buck Converter Test Lab Setup.

5.2 Measurement Results

Ten PCBs are manufactured, assembled and tested. The measurement results shown in this section are the typical data we collected.

5.2.1 DPWM Linearity

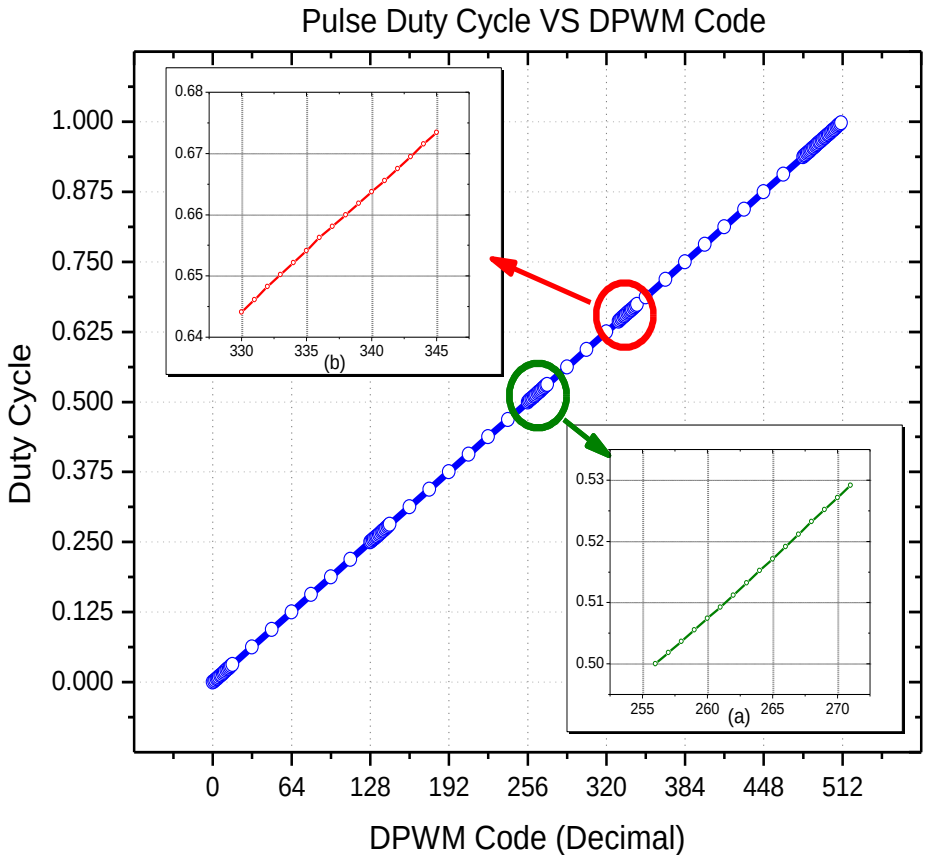


Fig. 5.4. Measured Digital VMC Buck Converter DPWM Linearity.

To measure the linearity of DPWM, we used several group measurement setups. First of all, we set LSBs to constants and change MSBs from zeros to full ones. This is to test the DPWM coarse part operation. Then we set MSBs to constants and change LSBs from zeros to full ones to test the DLL operation. Finally, we set DPWM code from {MSB 0000} to {MSB+1 1111} to test the DPWM linearity when both MSB and LSB change.

Shown in Fig. 5.4 is the measured PWM duty cycle for all DPWM input codes. The inset (a) shows duty cycle for code range of [10000*0000*, 10000*1111*]. It purely demonstrates the linearity of the DLL since only LSBs are changed here. The inset (b) shows duty cycle for code range of [10100*1010*, 10101*1001*]. As both MSBs and LSBs are varying, it tests the linearity of DPWM when its digital counter and DLL work jointly. Fig. 5.4 indicates that DPWM has good linearity and monotonicity over the entire input code range.

5.2.2 ΔΣADC

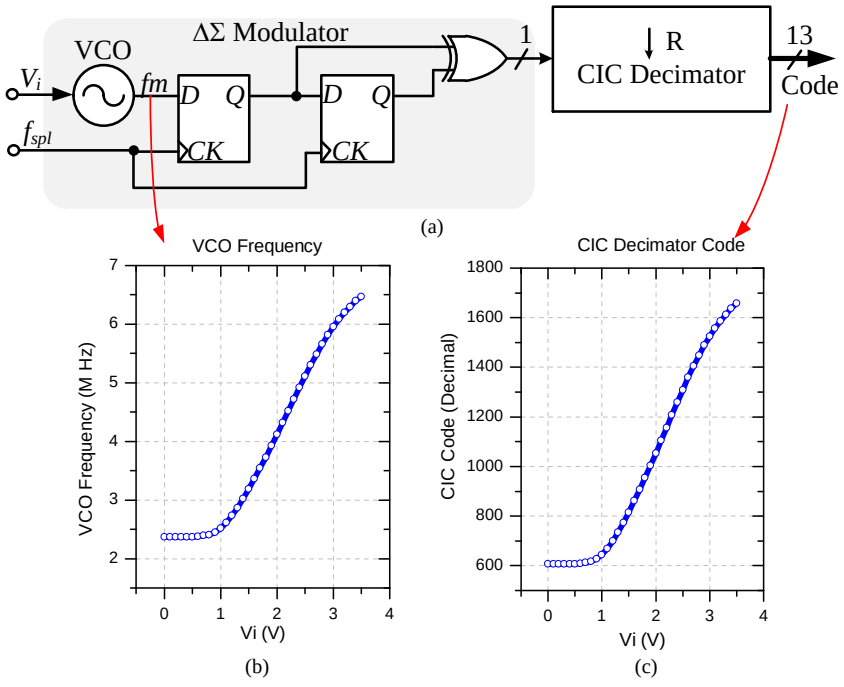


Fig. 5.5. Measured Frequency ΔΣ ADC Performance.

The measured ΔΣ ADC performance is illustrated in Fig. 5.5. Fig. 5.5 (a) shows the ΔΣADC architecture and the internal signals to be measured. Fig. 5.5 (b)

demonstrates the measured VCO frequency (FM modulated signal) for different ΔΣADC input voltages. Fig. 5.5 (c) shows the ΔΣADC output code for different input voltages. As shown in Fig. 5.5, the frequency ΔΣADC's linearity is primarily determined by the linearity of VCO. The decimation ratio *R* for this measurement is 64, CIC sampling frequency f_{spl} is 32MHz, CIC decimator output code rate is 500kHz. In our DC-DC, the ΔΣADC is only used in range 1.5V-2.5V for reference, feedback voltage and sense amplifier output digitization. The ΔΣADC has very high linearity in range 1.5V-2.5V as illustrated in Fig. 5.5.

5.2.3 Load Regulation Measurement

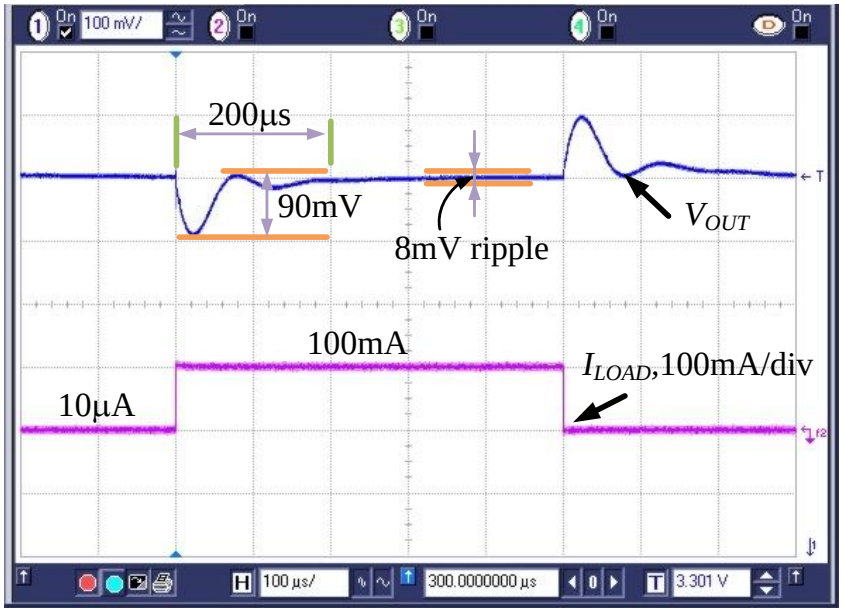


Fig. 5.6. Typical Digital VMC Buck Converter Transient Response.

A typical DC-DC regulator transient response is given in Fig. 5.6. The DC-DC input is 5V and output is 3.3V. For a load current step from 10µA to

100mA, the regulator achieves 200μs settling time and 90mV overshot voltage. The regulator output steady state ripple is about 8mV. The parameters of the power LC filter for this measurement are: C=22μF, ESR=70mΩ, L=18μH, DCR=63mΩ.

5.2.4 Efficiency Measurement

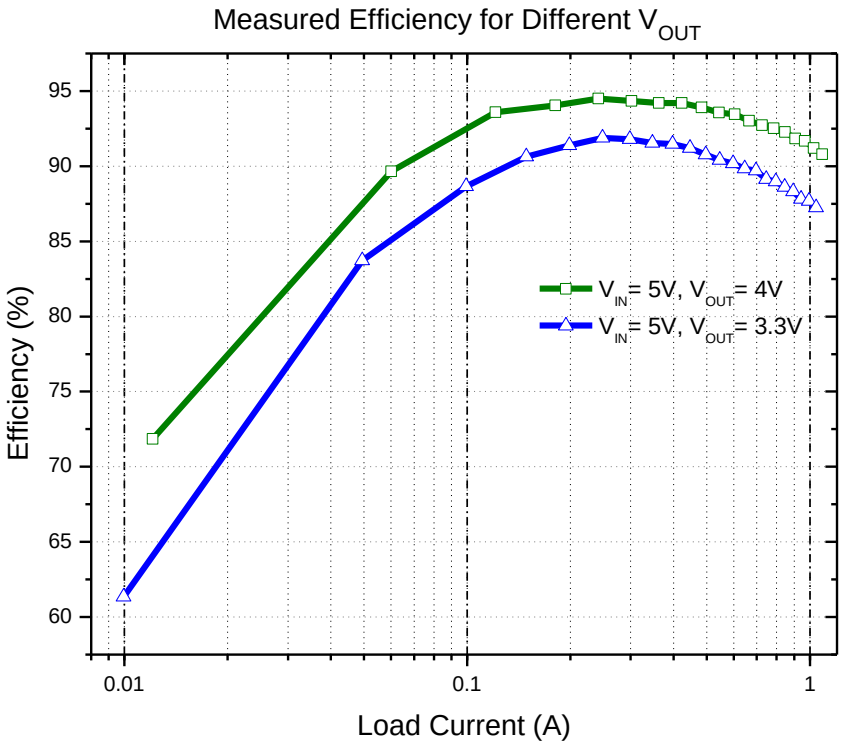


Fig. 5.7. Measured Digital VMC Buck Converter Efficiency.

The measured DC-DC efficiency is shown Fig. 5.7. For our targeted 0.1A up to 1A load current range, the efficiency is above 88% for 5V input, 4V or 3.3V output conditions. The peak efficiency is larger than 94%. One thing to mention is that since the converter is working in PWM and not in Pulse-Frequency

Modulation (PFM) mode, the efficiency on very small load current side is expected to be lower.

5.2.5 BIST Mode Measurement

5.2.5.1 BIST Mode Analog Signal

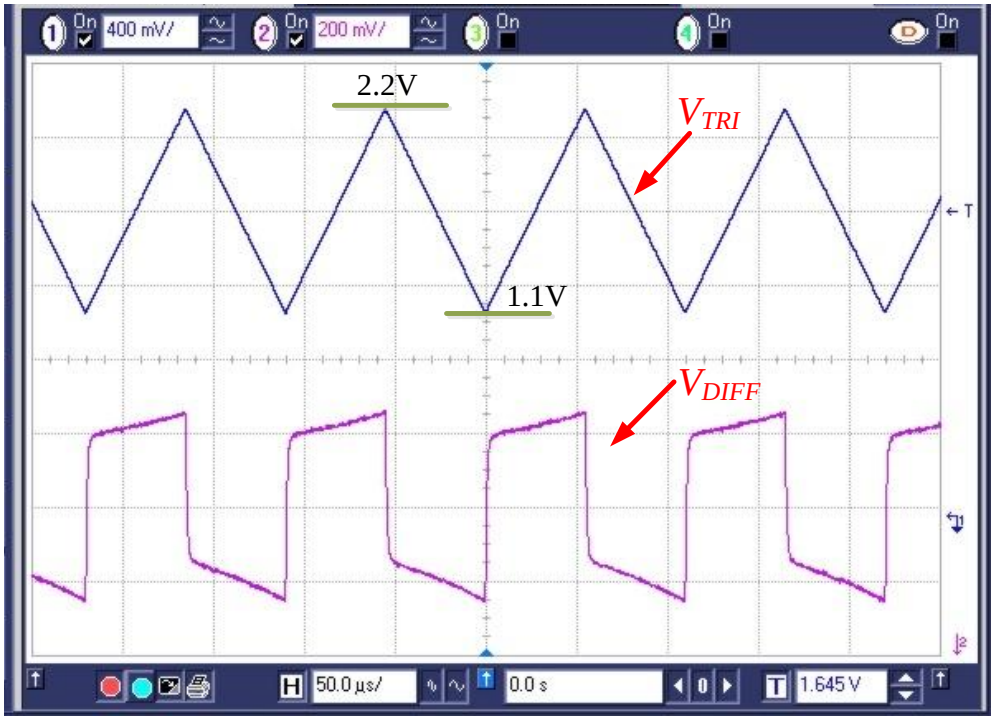


Fig. 5.8. Typical BIST Mode Waveforms.

Fig. 5.8 shows typical analog domain major nodes waveforms under inductor BIST mode. On the top is the triangular voltage generated by BIST circuits. It shows high symmetry. The maximum and minimum triangular voltages are 2.2V and 1.1V, which are expected levels set by our I_{ITR} genitor serials resistors in Fig. 4.3. On the lower side of Fig. 5.8 is the analog sense amplifier output. We could

observe steep edges which are desired to do inductor inductance and DCR measurement. Here the Device Under Test (DUT) is a 10.90μH inductor.

5.2.5.2 Inductance Measurement

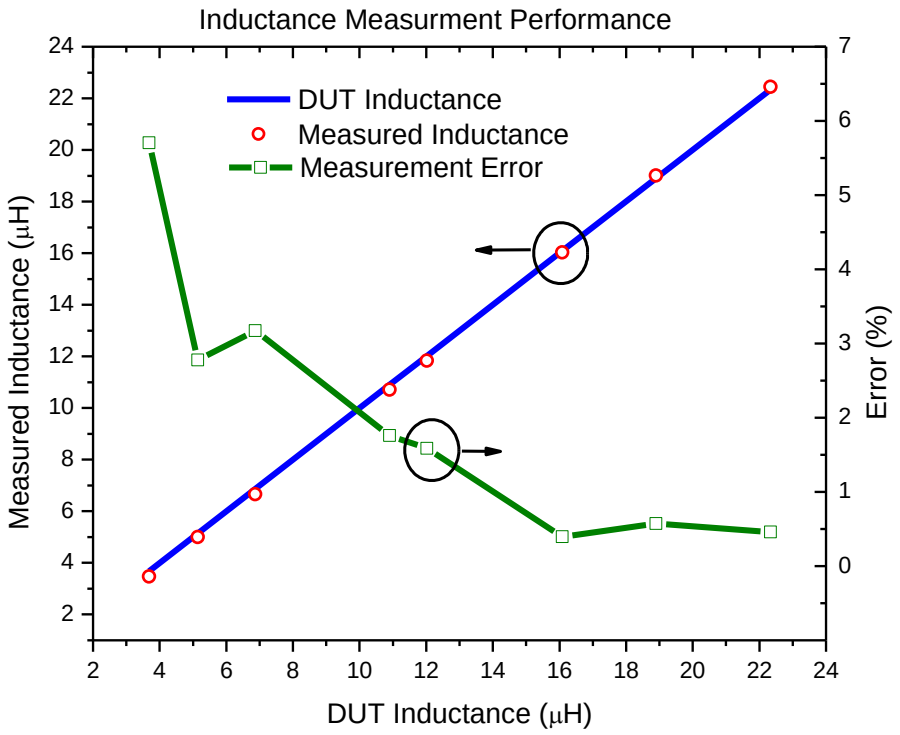


Fig. 5.9. Inductor Inductance Measurement Performance.

Fig. 5.9 shows the inductor inductance measurement result. The line without marker represents the inductance values measured by our lab LCR meter. We used these values as our benchmark references. And circle is the measured inductance by our chip. The line with square mark is the measurement error. We tested inductors with inductance values from 3.7μH to 22.3μH. The average error was about 2%.

5.2.5.3 DCR Measurement

Fig. 5.10 shows the inductor DCR measurement results. We tested inductors with DCR range of 15mΩ to 80mΩ, the average measurement error was 3.6%.

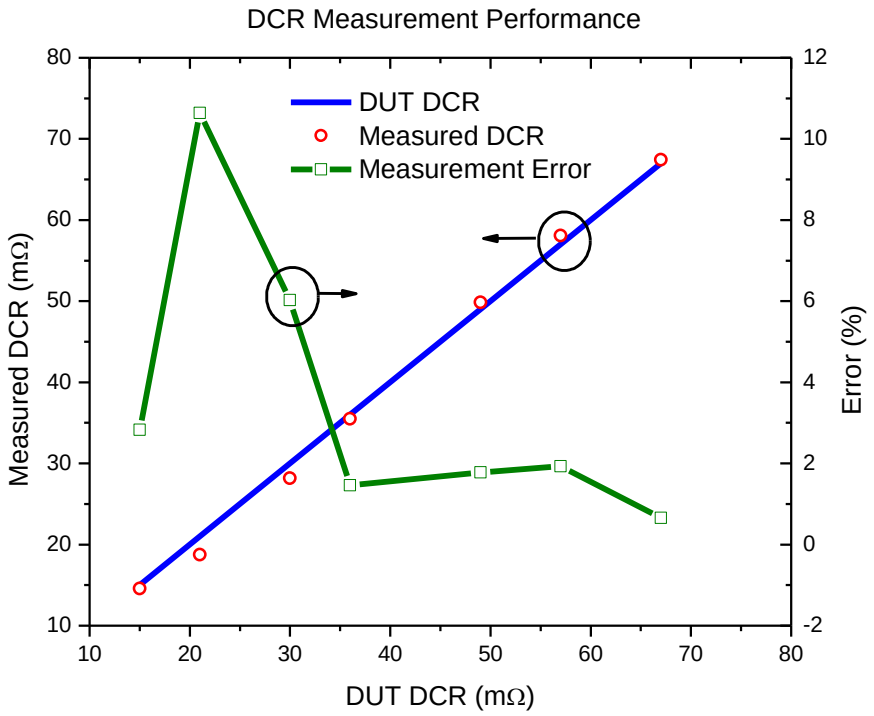


Fig. 5.10. Inductor DCR Measurement Performance.

5.2.6 Current Sensing Performance

The load current sensing performance is depicted in Fig. 5.11. We tested the current sensing ability with a DCR=63mΩ inductor, V_{IN}=5V V_{OUT}=3.3V case, for I_{LOAD} range of [100mA – 750mA], the average error was about 1.5%.

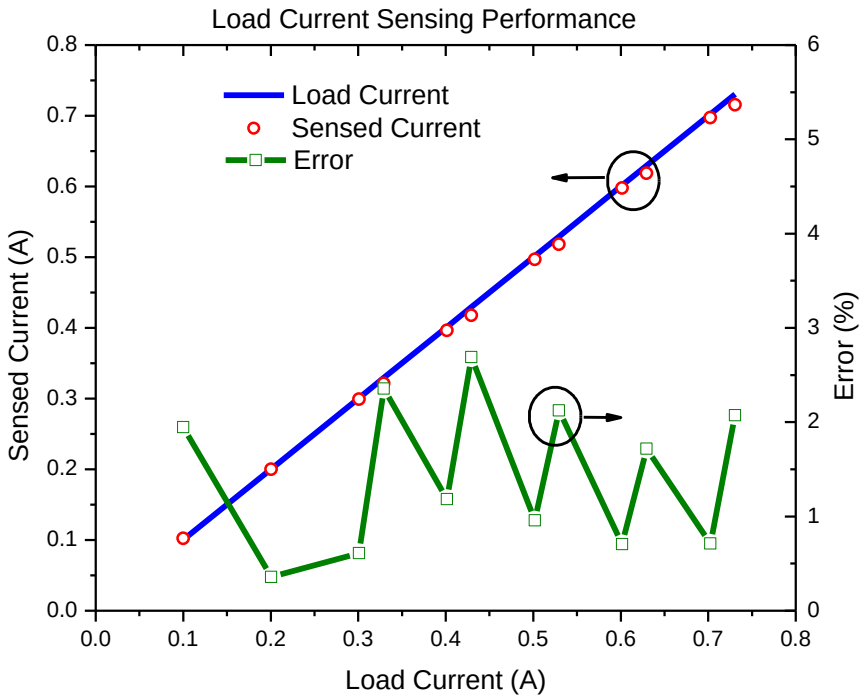


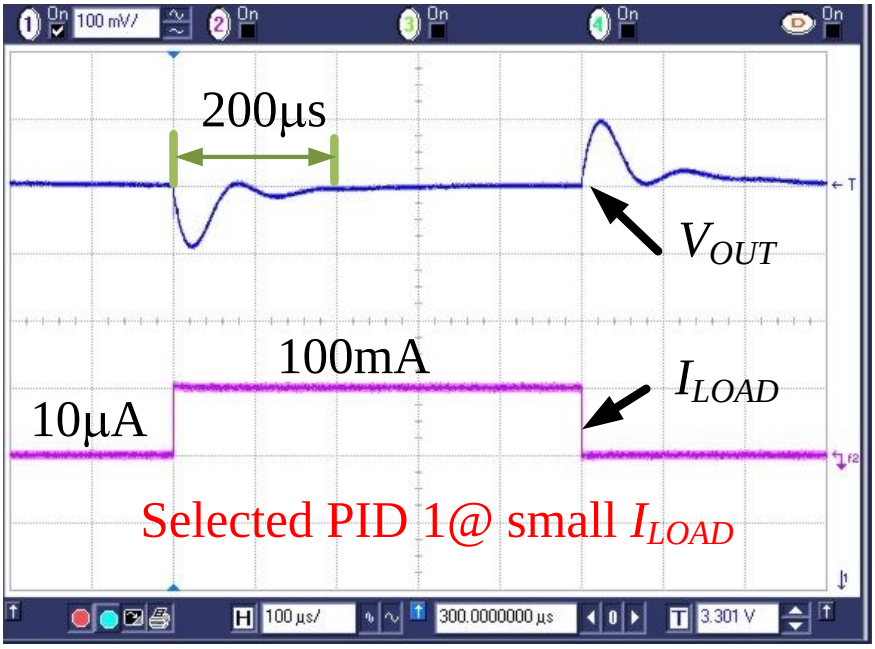
Fig. 5.11. Load Current Sensing Performance.

5.2.7 Load current based PID Adaptation

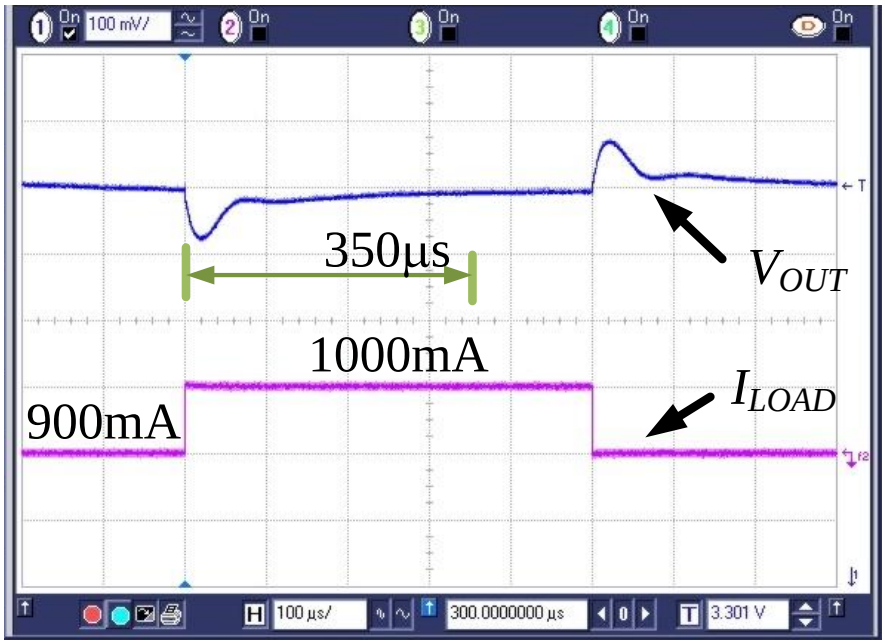
Programmable compensator is a big advantage of digital controlled converter compared to the traditional analog control implementation. Some programmable compensator methods are already proposed and used in prior work [8]-[9]. Especially, table look-up approaches are implemented in [8][10]. The table look-up approach is adopted in this digital voltage mode controlled buck converter as well. The sensed load current information is utilized to optimize the overall system's close loop response, achieving quasi load independent control.

We designed several PID compensators and prestored the PID coefficients on the chip. Shown in Fig. 5.12 is the transient response of DC-DC converter with PID 1, which is designed for small load current. And Fig. 5.13 shows the transient response of PID 2, which is designed for large load current. We can see from Fig. 5.12, as PID1 is designed for small load current, it shows clear overdamped transient response when load current is large. The settling time is increased from 200μs to 350μs. Similarly, as PID2 is designed for large load current, it shows underdamped transient response when load is small. The settling time is increased from 150μs to 250μs as shown in Fig. 5.13.

In our design, when the global PID update enable signal is turned to logic high, the table loop-up approach is used to select the proper PID coefficients. Here for example, based on the sensed load current, the 1st PID coefficients set is selected if I_{LOAD} is low and the 2nd PID coefficients set is selected if I_{LOAD} is high. Thus, we could maintain a suitable transient response for large load current range achieving quasi load independent control.

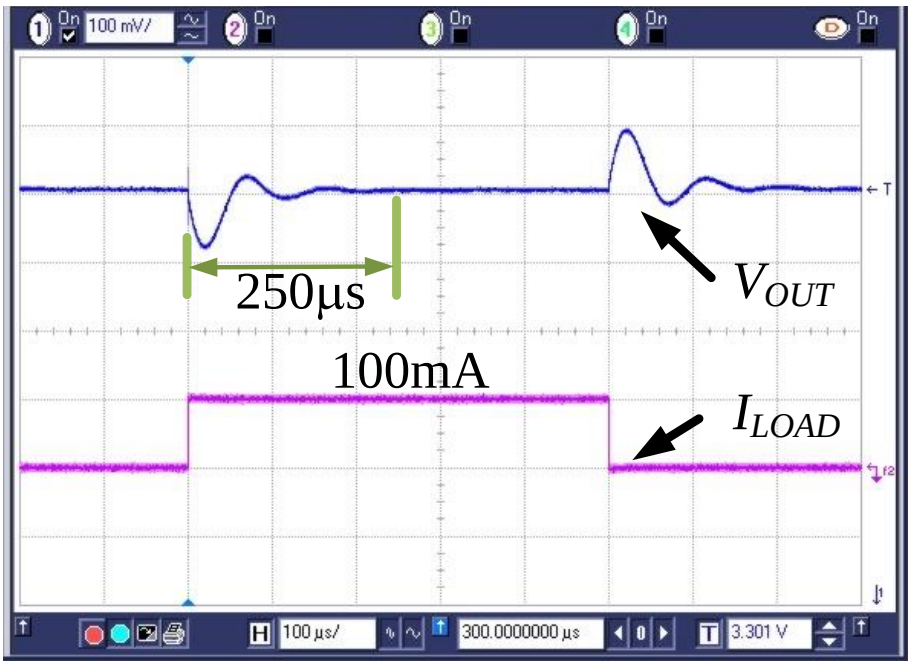


(a) PID1 for small I_{LOAD}.

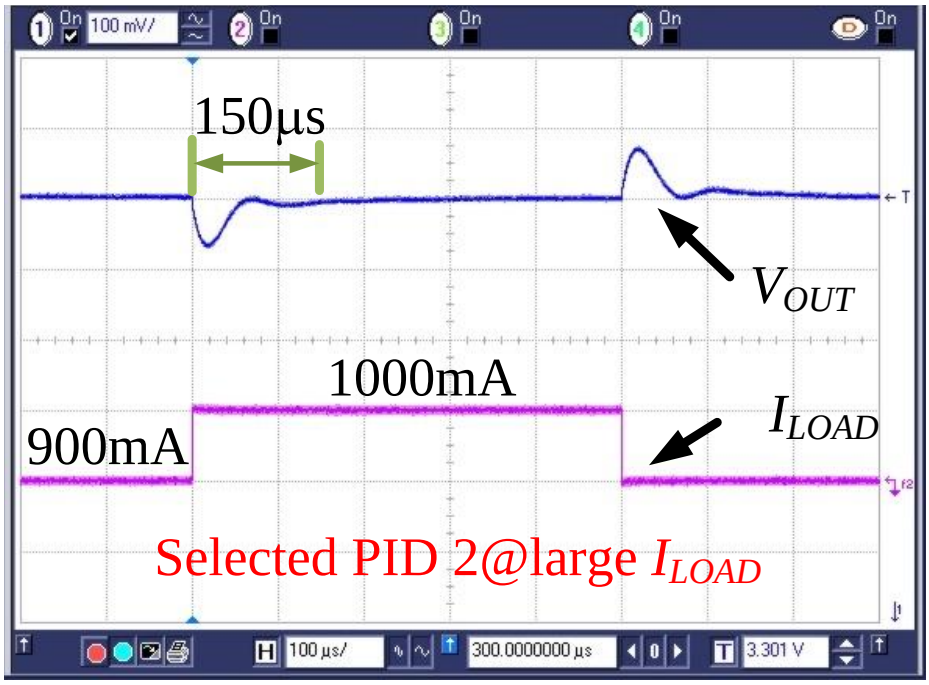


(b) PID1 for large I_{LOAD}.

Fig. 5.12. Transient Response for PID 1.



(a) PID2 for small I_{LOAD}.



(b) PID2 for large I_{LOAD}.

Fig. 5.13. Transient Response for PID 2.

5.3 Chip Performance Summary

The digital voltage mode controlled DC-DC buck converter with inductor BIST and continuous, lossless, and accurate load current sensing architecture is designed, fabricated, and experimentally tested. The overall chip performance is summarized in Table 5.1.

Table 5.1. Summary of Digital VMC DC-DC Performance

DC-DC Converter Parameters	
Technology	AMI i2t100 0.7μm CMOS
V_{IN}	1V-5.5V (5V typical)
V_{OUT}	1V-5.5V
Max load current	1A
Output voltage ripple	≤10mV
Switching frequency	500kHz
Crossover frequency	50kHz
Off-chip Capacitor	22μF
ESR of Capacitor	70mΩ
Efficiency	
I_{LOAD} [0.1A – 1A] @V_{IN}=5V, V_{OUT}=4V	89.7% ≤ η ≤ 94.5%
I_{LOAD} [0.1A – 1A] @V_{IN}=5V, V_{OUT}=3.3V	88.6% ≤ η ≤ 91.8%
BIST Performance	
Inductance [3.7μH – 22.3μH]	Average Error 2.1%
DCR [15mΩ – 80mΩ]	Average Error 3.6%
Load Current Sensing Performance	
I_{LOAD} [100mA – 750mA] (@DCR=63mΩ, V_{IN}=5V V_{OUT}=3.3V)	Average Error 1.5%
Chip Area	
Die	3.5mm×3.5mm
Inductor BIST & Current Sensing	5.2% of Die Area
Quiescent Current Consumption	
BIST mode	40.85mA for max 200μs
Current sensing	390μA
Normal regulation	610μA

The chip is a 0.7μm process, typical 5V input, maximum 1A load current, 8mV steady state ripper DC-DC converter with a 22μF cap. The typical efficiency for load range of 0.1A to 1A is above 88% with peak efficiency of 94.5%. The average measurement errors for inductance, DCR and current sensing are 2.1%, 3.6%, and 1.5% respectively. For the 3.5mm by 3.5mm die area, inductor BIST and current sensing circuits including related pins only consume 5.2% of the die area. BIST mode draws 40mA current for a maximum time period of 200μs upon start-up and the continuous current sensing consumes about 400μA quiescent current.

CHAPTER 6

DIGITAL ACMC BUCK CONVERTER

In previous chapters, we have discussed the proposed inductor BIST and average current sensing architectures. A digital voltage mode controlled DC-DC buck converter is designed, fabricated and experimentally tested to verify the performance of inductor BIST and current sensing approach. In this voltage mode controlled buck converter, the sensed load current is utilized to update the look-up table based programmable PID compensator to achieve quasi load independent control.

Similarly to the digital VMC buck converter, most prior digitally controlled single chip regulators use voltage control mode approaches [5][6]. Average current mode control (ACMC) in contrast has advantages in current-sharing, multi-stage converter load balancing and built-in overload protection. To enable ACMC, prior digital converters use either pricy Hall-effect current sensor [11] or lossy sensing resistor method to detect the inductor current. The average inductor current is obtained by adding extra averaging filter [11] or by prediction based on geometric relation of inductor current and the duty ratio [12]. In this chapter, an integrated digital ACMC buck converter with lossless average current sensing

method is proposed. A hybrid DPWM with a Mixed-Mode DLL (MDLL) is also proposed to reduce chip area and power consumption.

6.1 Digital ACMC Buck Converter Overall Architecture

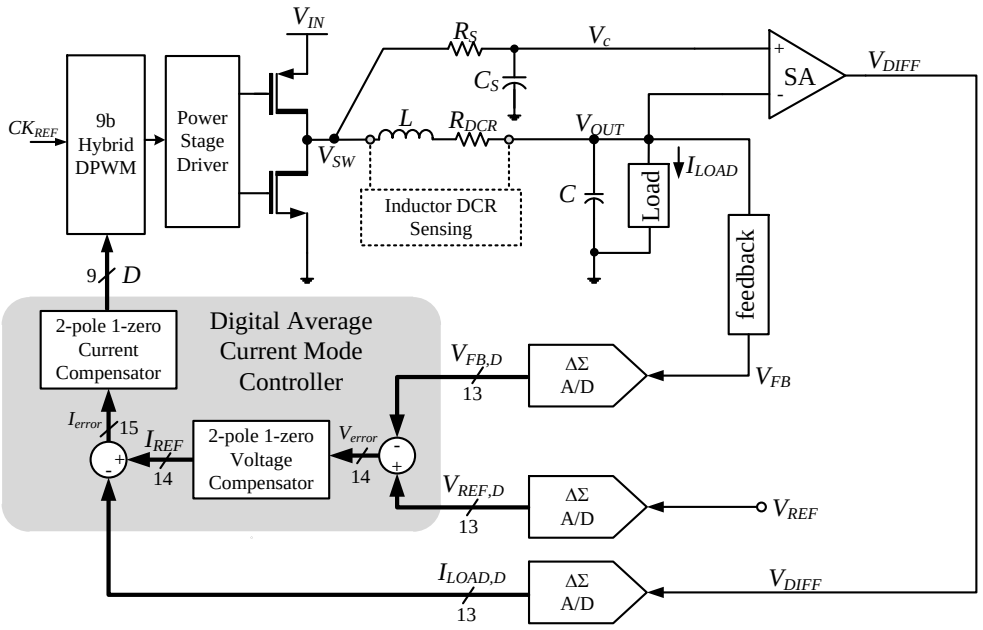


Fig. 6.1. Digital ACMC DC-DC Buck Converter Architecture.

Fig. 6.1 shows the proposed digital ACMC DC-DC buck converter architecture with the digital average current sensing circuitry and hybrid DPWM. An average current mode controller calculates the required pulse duty cycle D based on the digitized DC-DC feedback voltage V_{FB}, reference voltage V_{REF} and sensed average inductor current, i.e. the load current I_{LOAD}. A 9b MDLL based hybrid DPWM module generates the desired pulse signal. The PWM signal is sent to a level shifter followed by a power stage driver and then drives the power FETs.

The average inductor current is sensed by the lossless digital average current sensing technique discussed in Chapter 4. As shown in Fig. 6.1, an RC network set by R_S and C_S is added in parallel to the switching node V_{SW}. A differential sense amplifier (SA) whose gain is set by feedback resistor ratio amplifies the difference between RC filter output V_C and DC-DC output voltage V_{OUT}. The difference of V_C and V_{OUT} represents the DC voltage across the inductor. Thus the average inductor current (here in buck converter is also the load current) can be obtained by $I_L(AVE)=[V_C-V_{OUT}]/R_{DCR}$. Here R_{DCR} is the inductor DC resistance. In this sensing approach, high accuracy DCR measurement is essential. Upon start-up, DCR measurement is performed by the inductor BIST circuit proposed in Chapter 4, which is able to sense DCR with <2% error for >40mΩ range of DCR values within 200μs.

The digitization of SA output $V_{DIFF,}$ V_{FB} and V_{REF} is carried out by low cost digitally intensive frequency domain ΔΣ ADCs proposed in Chapter 3. ΔΣADC runs at oversampling frequency $f_{spl}=R\cdot f_s$. R=64 is the decimation ratio, f_s is the digital ACMC buck converter switching frequency, typically 375kHz. After decimation, ADC generates 8b resolution code updated at f_s. The CIC filter has transmission zeros at multiples of f_s suppressing noise-folding at multiples of sampling frequency. By using this ΔΣ ADC to digitize V_{DIFF}, DC inductor current

is amplified by decimator gain R^2 and current ripple is suppressed. This approach can achieve less than 3% current measurement error without the need for extra digital averaging filtering.

6.2 Digital ACMC Buck Converter Implementation

6.2.1 DPWM

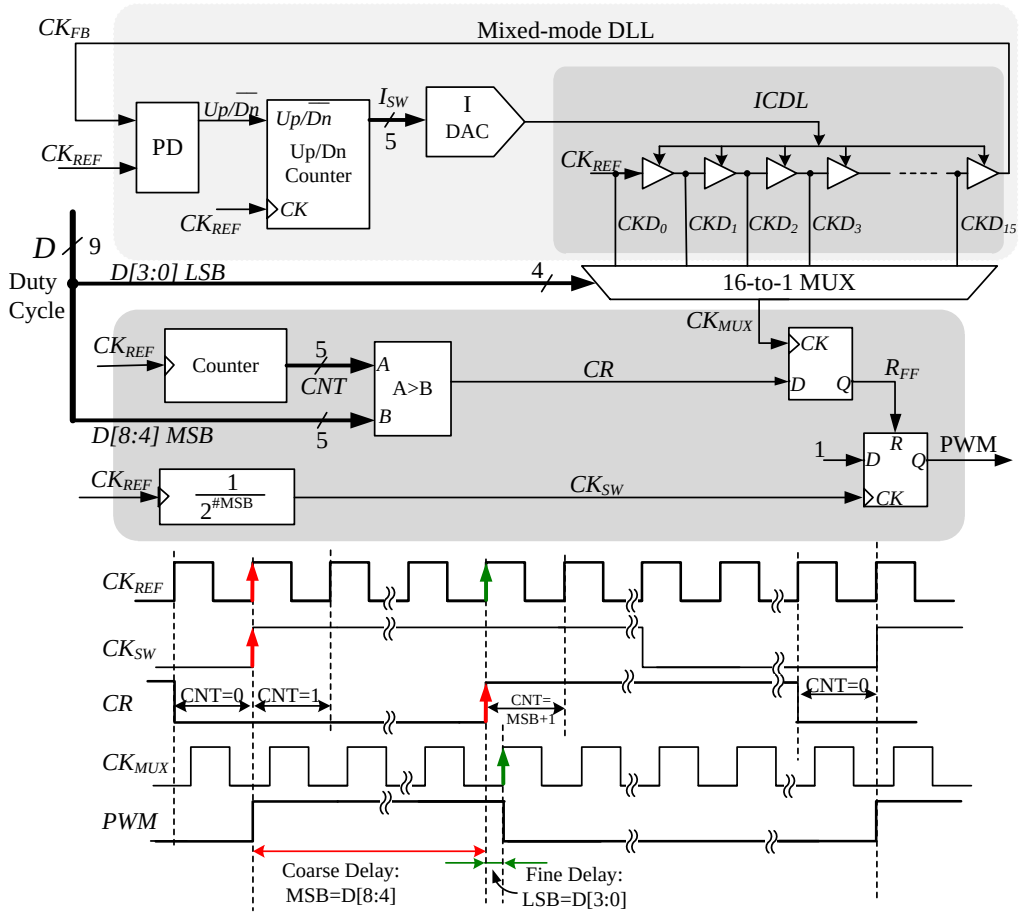


Fig. 6.2. Hybrid DPWM Architecture Using Mixed-Mode DLL.

The proposed 9b DPWM shown in Fig. 6.2 uses a hybrid architecture to achieve high resolution with low power and hardware cost. Here 5b MSBs of duty

cycle *D* are controlled by a counter and a comparator. The 4b LSBs of *D* are controlled by the proposed MDLL.

The upper part of the architecture in Fig. 6.2 is the MDLL comprising a phase detector (PD), an Up/Dn counter, a current-steering DAC (I-DAC) and a current controlled delay line (ICDL). The control word I_{SW} at the up/down counter output determines the delay time of ICDL. MDLL generates 16-tap delayed signal *CKD* of MDLL reference clock CK_{REF}. A 16-to-1 MUX selects desired tap based on 4b LSBs of *D*. The delay from CK_{REF} to MUX output is the fine delay.

The lower part of the architecture in Fig. 6.2 is the 5b counter comparator path generating the coarse delay. After releasing from the reset, it starts to count the cycles of CK_{REF}. Once the MSBs of *D* match counter output *CNT*, a coarse delay ready signal *CR* is sent out to add up the fine delay and set the PWM width.

6.2.1.1 Up/Dn Counter

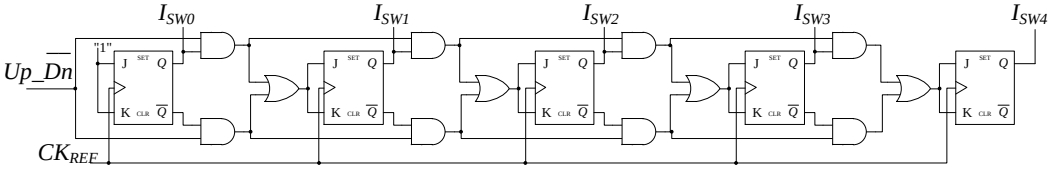


Fig. 6.3. Up/Dn Counter in MDLL.

The Up/Dn counter used in MDLL is shown in Fig. 6.3. The Up/Dn counter runs at CK_{REF}, typically 12MHz. The counter accumulation direction is controlled by $Up\overline{Dn}$. If the selector $Up\overline{Dn}$ is '1', the counter increases its value. When the

selector $Up\overline{Dn}$ is ‘0’, the counter decreases the count. The selector of the Up/Dn counter is from the MDLL PD. As PD compares the MDLL feedback clock signal CK_{FB} and the reference clock CK_{REF}, the PD output, i.e. $Up\overline{Dn}$, tells whether CK_{FB} arrives earlier or later than CK_{REF}. It then sends requirement to ICDL for less or more delay. The MDLL in this design is a bang-bang DLL. When MDLL is locked, PD generates up and down selector signals one after one repeatedly. The edge of the DLL feedback clock CK_{FB} starts to move back and forth around the edge of the reference clock CK_{REF} to keep the MDLL in the lock condition. The jitter due to the CK_{FB} move is designed to be small enough that it can be ignored compared to the 1LSB DPWM delay.

6.2.1.2 I-DAC and ICDL

In conventional DLLs, digital delay lines are often used to achieve fast lock-in while analog control circuits are usually used to achieve small jitter. Since the DLL in DPWM only operates at fixed reference clock, fast lock-in is not a critical requirement. Thus an I-DAC controlled current-starved delay line ICDL is used in this MDLL as shown in Fig. 6.4. Analog delay line significantly reduces chip area since it only requires one multi-bit current tuning DAC rather than tuning delay cells individually in traditional digital delay line implementations [57][58]. Also, all digital control circuits instead of the traditional charge pump

and LPF approach [5] are used to increase the system noise immunity and overall robustness.

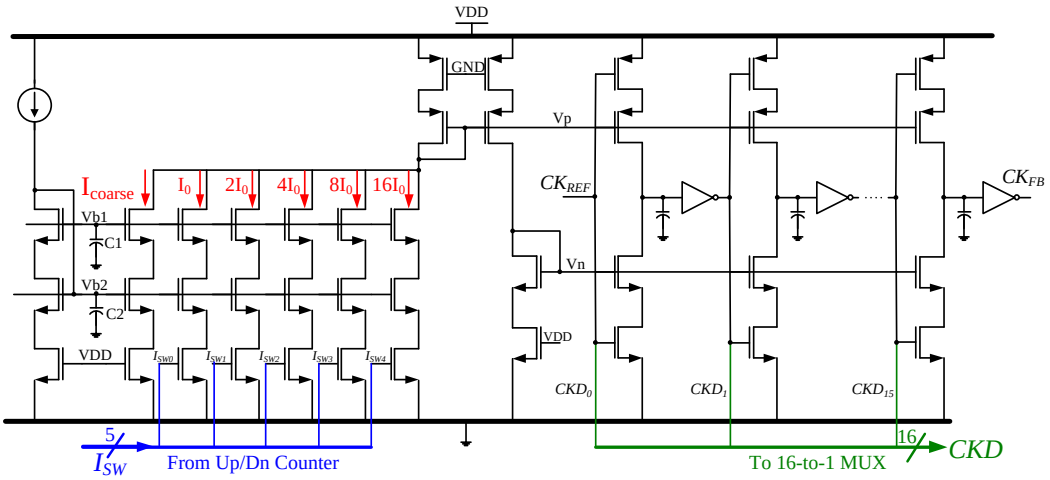


Fig. 6.4. Current-Steering DAC Followed by ICDL in MDLL.

The control word I_{SW} from up/dn counter controls binary weighed current bias array. To achieve low jitter with low hardware cost, a segmented approach is used in the I-DAC as shown in Fig. 6.4. A coarse bias I_{coarse} is pre-selected to be close to the amount of current needed for ICDL locked at CK_{REF}. The control word I_{SW} only controls the fine current part. Thus, only 5bits I_{SW} is needed to achieve 40ps delay control resolution. This is 1% error for the 9b DPWM, whose typical 1 LSB delay is around 4ns depending on f_s. To reduce the switching noise during MDLL locking and avoid differential output dump path, a single-ended DAC with source side switching scheme is adopted. The switching noise can be isolated by two

cascaded bias transistors. Two bypass capacitors C1 and C2 are also connected to bias voltages to stabilize the current biases and absorb switching noise.

6.2.2 Level Shifter

The targeted maximum input voltage of this buck converter is 12V. To be able to operate under 12V input voltage, the power MOSFETs use 42nm thick oxide DMOS transistors that can operate at a maximum V_{DS} of 30V and a maximum V_{GS} of 12V.

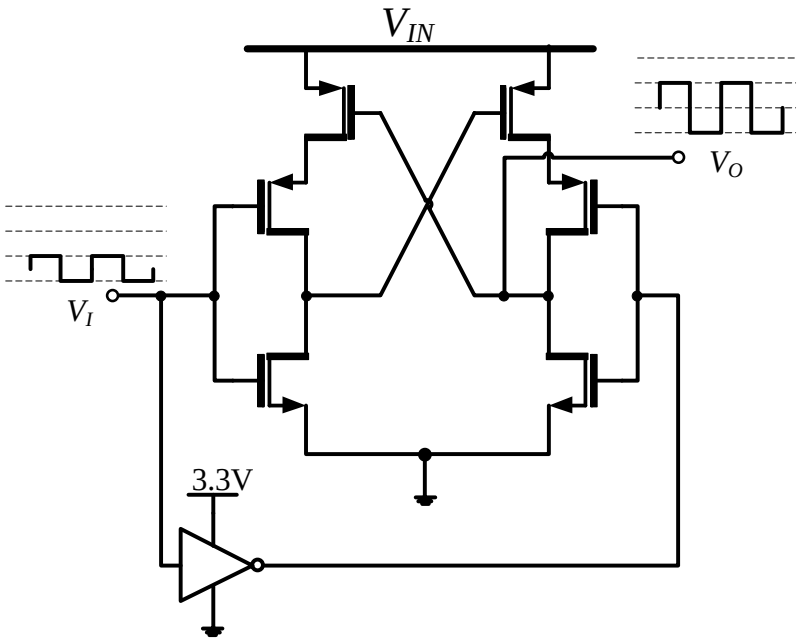


Fig. 6.5. Level Shifter.

To obtain high efficiency of this converter, we minimized DC-DC power consumption by using 3.3V supply for all the analog and digital blocks. Only power stage and power stage drive operate under V_{IN} supply. So a level shifter is required to boost the voltage swing range [0V, 3.3V] to the desired [0V, V_{IN}] level

to drive the power MOSFETs. The architecture of the level shifter is shown in Fig. 6.5. It's similar to the level shifter used in digital VMC buck converter. However, the transistors here are DMOS which can operate under voltage up to 12V V_{GS}.

6.2.3 Average Current Mode Controller

Modeling of average current model control has been widely studied in the last two decades [63]-[70]. Procedures to design the current mode controller are given in [63][66][69][70]. The average current mode controller is typically a 2-loop compensator. An outer voltage loop compensator takes the difference of V_{FB} and V_{REF} and generates the desired reference current I_{REF}. An inner current loop compensator compares I_{LOAD} to I_{REF} and calculates the duty cycle D.

6.2.3.1 Current Loop Compensator Design

For the current loop compensator, a 2-pole 1-zero compensator is generally used in prior work [63][66][69][70]. The general compensator design guidelines can be summarized as: a pole is placed at origin to boost the compensator DC and low frequency gain. Another high frequency pole is placed close to DC-DC switching frequency f_s to attenuate switching noise. The zero is below the power LC filter resonant frequency $1/\sqrt{(L\times C)}$ to boost phase margin and maximize current compensator crossover frequency. The bandwidth of the compensated current loop is typically designed to be around 1/10 to 1/5 of the DC-DC

converter switching frequency. In this work, three types of current loop compensators are introduced. A detailed *K-factor* approach based design procedure is elaborated.

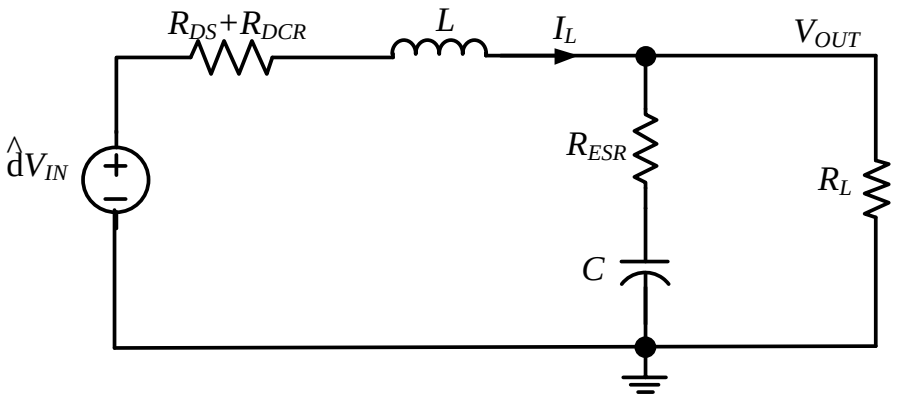


Fig. 6.6. Small Signal Model of Buck Converter.

The inner current loop compensator design starts with the analysis of the uncompensated current loop. Shown in Fig. 6.6 is the small signal model of the DC-DC buck converter with the consideration of the inductor DCR R_{DCR}, capacitor ESR R_{ESR}, and the turn-on resistance R_{DS} of the power FETs. The control to inductor current transfer function $G_{id}(s)$ is:

$$G_{id}(s)=V_{IN}\frac{1}{sL+R_D+\dfrac{R_L(1+sR_{ESR}C)}{1+sC(R_L+R_{ESR})}}$$
$$=\frac{V_{IN}}{R_L}\frac{1+sC(R_L+R_{ESR})}{s^2LC\left(1+\dfrac{R_{ESR}}{R_L}\right)+s\left[\dfrac{L}{R_L}+\left(R_D+R_{ESR}+\dfrac{R_DR_{ESR}}{R_L}\right)C\right]+\left(1+\dfrac{R_D}{R_L}\right)} \quad (6\text{-}1)$$

Here R_D is the sum of power inductor DCR R_{DCR} and the power switch turn-on resistance R_{DS}:

$$R_D = R_{DS} + R_{DCR} \tag{6-2}$$

The next step is to obtain the phase of the system $G_{id}(s)$, Φ_{Gid}, at the desired current loop cross over frequency ω_{c_c}. According to the phase that needs to boost by the rest of zeroes and poles of the controller, a suitable compensator from three types of compensators needs to be selected. Type-I compensator is a single pole integrator.

$$G_{c\_c}(s) = \frac{K_C}{s} \tag{6-3}$$

And Type-II compensator is a typical 2-pole 1-zero PI compensator.

$$G_{c\_c}(s) = \frac{K_C\left(1+\frac{s}{\omega_z}\right)}{s\left(1+\frac{s}{\omega_p}\right)} \tag{6-4}$$

Type-III compensator is a 3-pole 2-zero compensator.

$$G_{c\_c}(s) = \frac{K_C\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{s\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \tag{6-5}$$

In ACMC, a simplified Type-III compensator is normally used.

$$G_{c\_c}(s) = \frac{K_C\left(1+\frac{s}{\omega_z}\right)^2}{s\left(1+\frac{s}{\omega_p}\right)^2} \tag{6-6}$$

All the three controllers have a pole at the origin which introduces a 90˚ phase lag. Let PM_C be the phase margin expected for the compensated current loop at ω_{c_c}, the phase needs to boost is:

$$\Phi_{boost\_c} = PM_C - \Phi_{Gid} - 90^{\circ} \tag{6-7}$$

If Φ_{boost_c}=0, the pole at the origin is sufficient to obtain the required phase margin, a Type-I integrator should be used. If Φ_{boost_c} <90˚, one extra zero should be added to improve the phase margin, therefore a Type-II is a suitable solution. If Φ_{boost_c} >90˚, a single extra zero is not enough to boost the required phase, a Type-III compensator becomes an appropriate option. The choice of compensator type is summarized in Table 6.1.

Table 6.1. Choice of Compensator Type.

Required Φ_{boost_c}	Compensator Type
0˚	Type-I
<90˚	Type-II
>90˚	Type-III

Once the compensator type is chosen, we then design the parameters of each compensator such as positions of poles, zeros, gain etc.

For Type-I compensator, as the compensated system $G_c(s) \times G_{id}(s)$ should have a unity gain at the crossover frequency ω_{c_c}, we could pick Kc of (6-3) in the manner of

$$K_C = \frac{\omega_{c\_c}}{K_{Gid}\,|_{\omega_{c\_c}}} \tag{6-8}$$

Here $K_{Gid}|_{\omega c\_c}$ is the magnitude of $G_{id}(s)$ at ω_{c_c}.

In Type-II compensator, other than the pole at the origin, one extra zero ω_z and one extra pole ω_p are used to increase system phase. For maximum phase boost at the crossover frequency ω_{c_c}, ω_z and ω_p are normally selected in a way that ω_{c_c} is the geometric mean of ω_z and ω_p, i.e.

$$\frac{\omega_{c\_c}}{\omega_z} = \frac{\omega_p}{\omega_{c\_c}} = k_2 \tag{6-9}$$

We can derive k_2 from (6-4) and (6-7) :

$$k_2 = \tan\left[\frac{\Phi_{boost\_c}}{2} + 45°\right] \tag{6-10}$$

ω_z and ω_p are then obtained by

$$\omega_z = \frac{\omega_{c\_c}}{k_2},\ \omega_p = k_2\omega_{c\_c} \tag{6-11}$$

Once the poles and zeros are designed, we can obtain the compensated system with compensator parameter K_C=1.

$$T_{c2}(s)|_{K_c=1}=\frac{\left(1+\frac{s}{\omega_z}\right)}{s\left(1+\frac{s}{\omega_p}\right)}G_{id}(s) \tag{6-12}$$

Let $K_{Tc2}|\omega_{c\_c}$ be the magnitude of the system in (6-12) at crossover frequency ω_{c_c}, K_c in (6-4) can be simply determined by

$$K_C=\frac{1}{K_{T_{C2}}|_{\omega_{c\_c}}} \tag{6-13}$$

As a result, the compensated system

$$T_{c2}(s)=\frac{K_C\left(1+\frac{s}{\omega_z}\right)}{s\left(1+\frac{s}{\omega_p}\right)}G_{id}(s) \tag{6-14}$$

will have a unity gain at the desired current loop crossover frequency ω_{c_c}.

In Type-III compensator, other than the pole at the origin, one extra second-order zero ω_z and one extra second-order pole ω_p are used to increase system phase. For maximum phase boost at the crossover frequency ω_{c_c}, ω_z and ω_p are also generally selected in a way that ω_{c_c} is the geometric mean of ω_z and ω_p:

$$\frac{\omega_{c\_c}}{\omega_z}=\frac{\omega_p}{\omega_{c\_c}}=k_3 \tag{6-15}$$

We can derive k_3 from (6-6) and (6-7) :

$$k_3 = \tan\left[\frac{\Phi_{boost\_c}}{4} + 45°\right] \tag{6-16}$$

ω_z and ω_p are then can be obtained by

$$\omega_z = \frac{\omega_{c\_c}}{k_3},\ \omega_p = k_3\omega_{c\_c} \tag{6-17}$$

Similar to that of Type-II compensator design, once the pole and the zero are designed, we then obtain the compensated system with compensator K_C=1.

$$T_{c3}(s)|_{K_c=1} = \frac{\left(1+\frac{s}{\omega_z}\right)^2}{s\left(1+\frac{s}{\omega_p}\right)^2} G_{id}(s) \tag{6-18}$$

Let $K_{Tc3}|\omega_{c\_c}$ be the magnitude of the system in (6-18) at crossover frequency ω_{c_c}, K_c in (6-6) can be chose by

$$K_C = \frac{1}{K_{T_{C3}}|_{\omega_{c\_c}}} \tag{6-19}$$

so that the compensated system $G_{c\_c}(S)G_{id}(S)$ will have a unity gain at the desired current loop crossover frequency ω_{c_c}.

The current loop compensator designed in this work is demonstrated in the following figures. Fig. 6.7 shows the uncompensated current loop. To compensate this loop, a Type-II compensator is designed whose bode plot is shown in Fig. 6.8.

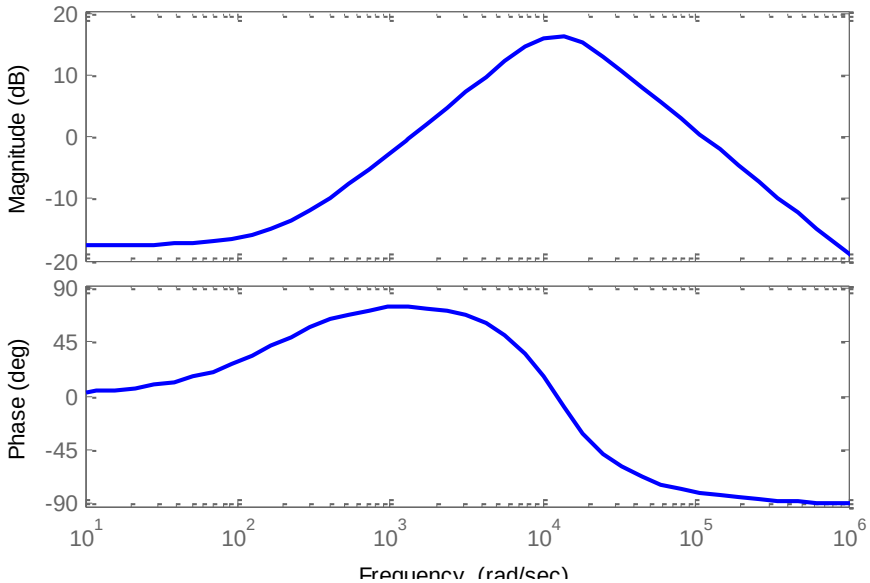


Fig. 6.7. Bode Plot of the Uncompensated Current Loop.

Fig. 6.9 is the compensated current loop. The crossover frequency is selected to be around 1/10 of the DC-DC switching frequency typically 375kHz ($2.36x10^6$rad/s). The phase margin is designed around 70 degree.

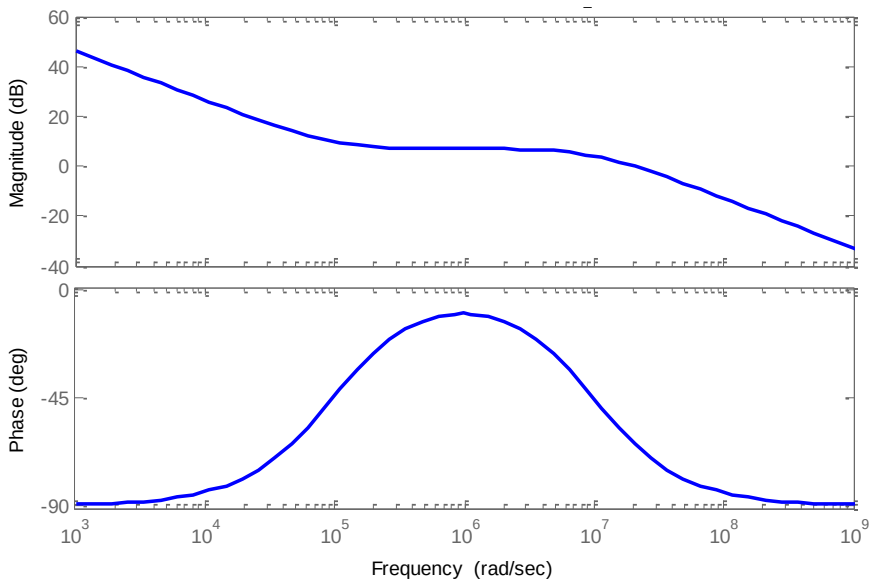


Fig. 6.8. Bode Plot of the Current Loop Compensator.

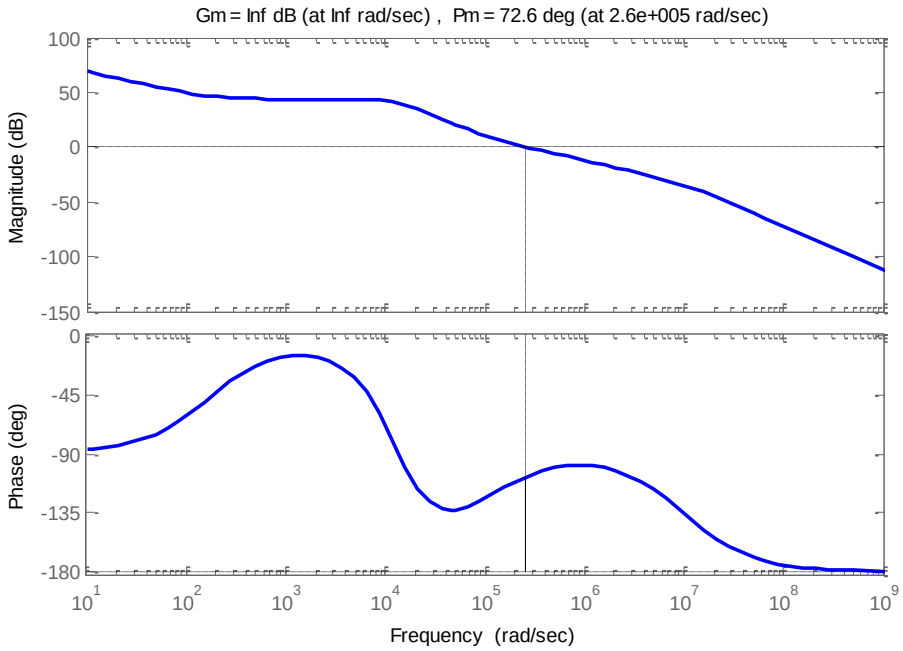


Fig. 6.9. Bode Plot of the Compensated Current Loop.

6.2.3.2 Voltage Loop Compensator Design

The outer voltage loop compensator design starts with the analysis of the uncompensated voltage loop. Showing in Fig. 6.10 is the signal flow of average current mode controlled buck converter. This is a simplified model because other modules such as DPWM are not depicted, but it still captures the essential of the buck converter without sacrificing accuracy since K_{DPWM}=1 here. In Fig. 6.10, G_{c_c} is the inner current loop compensator designed in previous section. G_{c_v} is the outer voltage loop compensator. As current loop operates at a much faster speed than that of voltage loop, when the voltage changes in the outer loop, the current

transfer function can be considered as 1. That is, an ideal current loop (gain=1) is assumed during the design of voltage compensator.

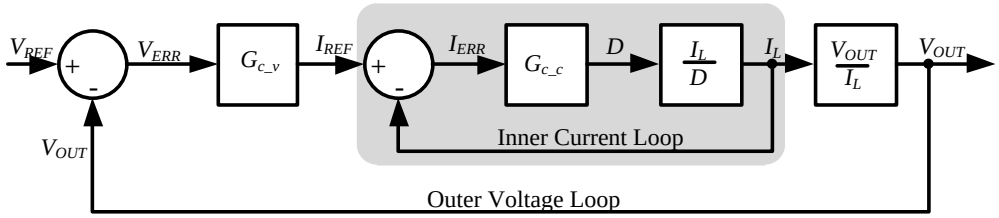


Fig. 6.10. Simplified Signal Flow of ACMC Buck Converter.

From the small signal model of the DC-DC buck converter shown in Fig. 6.6, we can obtain the inductor current-to-output transfer function $G_{vi}(s)$:

$$G_{vi}(s) = \frac{R_L(1+sR_{ESR}C)}{1+sC(R_L+R_{ESR})} \tag{6-20}$$

$G_{vi}(s)$ in (6-20) is 1-pole 1-zero system, to compensate it with desired phase margin PM_v, a Type-II compensator is normally sufficient:

$$G_{c\_v}(s) = \frac{K_C\left(1+\frac{s}{\omega_z}\right)}{s\left(1+\frac{s}{\omega_p}\right)} \tag{6-21}$$

The phase to be boosted is:

$$\Phi_{boost\_v} = PM_V - \Phi_{Gvi} - 90^\circ \tag{6-22}$$

where Φ_{Gvi} is the phase of $G_{vi}(s)$ at the desired voltage loop crossover frequency ω_{c_v}. ω_{c_v} is about 1/10 of the current loop crossover frequency ω_{c_c}. The compensator zero and pole ω_z and ω_p are obtained by

$$\omega_z = \frac{\omega_{c\_v}}{k},\ \omega_p = k\omega_{c\_v} \tag{6-23}$$

where

$$k = \tan\left[\frac{\Phi_{boost\_v}}{2} + 45°\right] \tag{6-24}$$

Once the poles and zeros are designed, we then obtain the compensated system with compensator (6-21) K_C =1.

$$T_v(s)|_{K_c=1} = \frac{\left(1+\frac{s}{\omega_z}\right)}{s\left(1+\frac{s}{\omega_p}\right)} G_{vi}(s) \tag{6-25}$$

Let $K_{Tv}|\omega_{c\_v}$ be the magnitude of the system in (6-25) at crossover frequency ω_{c_v}, K_c in (6-21) can be determined by

$$K_C = \frac{1}{K_{Tv}|_{\omega_{c\_v}}} \tag{6-26}$$

Thus the compensated system

$$T_v(s) = \frac{K_C\left(1+\frac{s}{\omega_z}\right)}{s\left(1+\frac{s}{\omega_p}\right)} G_{vi}(s) \tag{6-27}$$

will have a unity gain at the desired voltage loop crossover frequency ω_{c_v}.

The following figures demonstrate the voltage loop compensation designed in this work. Fig. 6.11 is the bode plot of the uncompensated voltage loop.

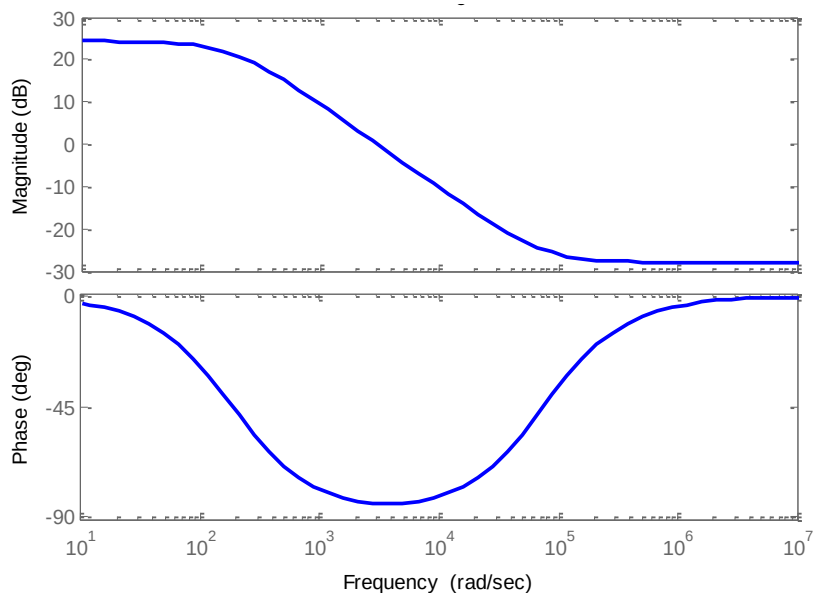


Fig. 6.11. Bode Plot of the Uncompensated Voltage Loop.

Fig. 6.12 shows the Type-II voltage loop compensator constructed. It's a standard 2-pole 1-zero system.

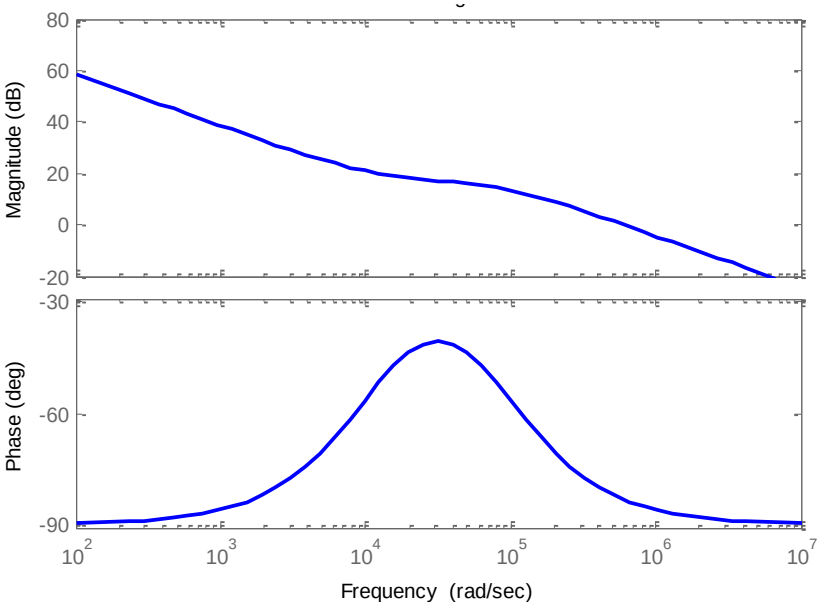


Fig. 6.12. Bode Plot of the Voltage Loop Compensator.

The compensated voltage loop is shown in Fig. 6.13. The phase margin is designed around 65˚ and the crossover frequency is around 1/10 of the current loop crossover frequency.

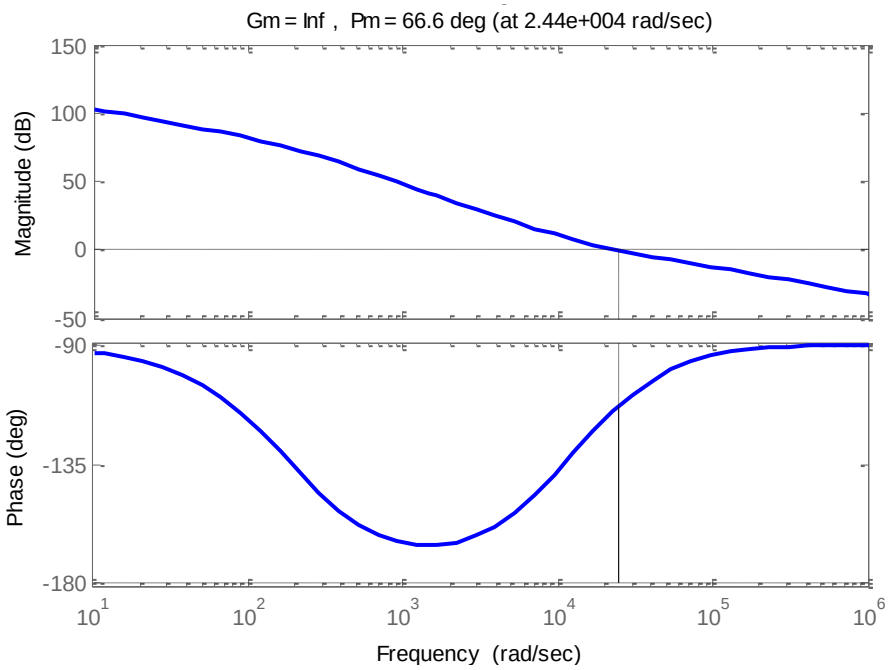


Fig. 6.13. Bode Plot of the Compensated Voltage Loop.

6.2.3.3 Compensator Implementation

Once the current loop compensator G_{c_c} and the voltage loop compensator G_{c_v} are designed in s-domain, we could convert the continuous-time s-domain transfer functions to the corresponding discrete-time z-domain transfer functions via bilinear (Tustin) approximation method. In this section, the digital implementations of all three types of compensators are discussed.

For Type-I compensator, recall the transfer function of the compensator:

$$G_{c\_c}(s) = \frac{K_C}{s} \tag{6-3}$$

After applying the Tustin approximation

$$s = 2 \times f_s \times \frac{z-1}{z+1} \tag{6-28}$$

the Type-I compensator in (6-3) can be converted to

$$H(z) = \frac{K_C}{2f_s}\frac{(z+1)}{(z-1)} = \frac{a(z+1)}{(z-1)} \tag{6-29}$$

Here $a=K_C/2f_s$.The system in (6-29) can be implemented by using the architecture shown in Fig. 6.14.

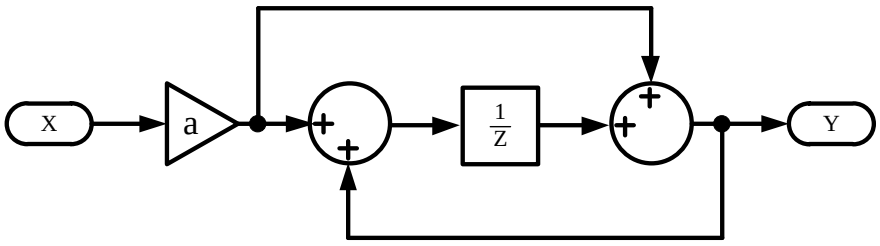


Fig. 6.14. Digital Implementation of Type-I Compensator.

The converted z-domain transfer function for a Type-II compensator generally has the form of

$$H(z) = \frac{a_0 z^2 + a_1 z^1 + a_2}{z^2 + b_1 z + b_2} \tag{6-30}$$

The system in (6-30) can be implemented by using the architecture illustrated in Fig. 6.15.

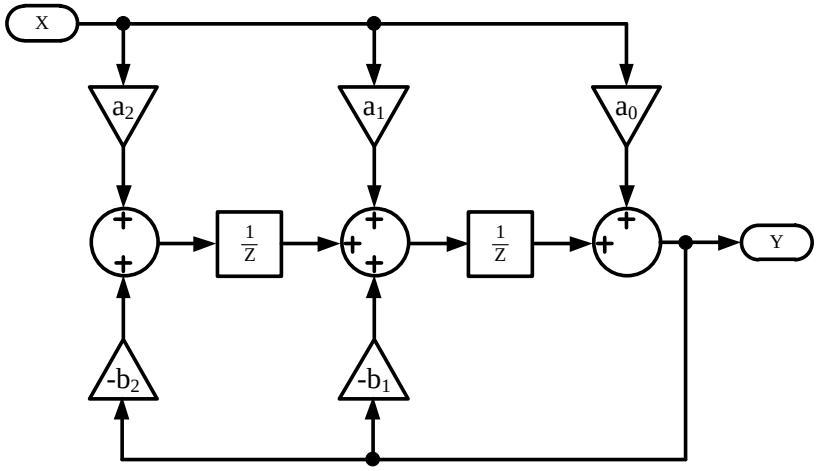


Fig. 6.15. Digital Implementation of Type-II Compensator.

For Type-III PID compensator, the converted z-domain transfer function generally has the form of

$$H(z) = \frac{a_0 z^3 + a_1 z^2 + a_2 z + a_3}{z^3 + b_1 z^2 + b_2 z + b_3} \qquad (6\text{-}31)$$

It can be implemented by using the architecture given in Fig. 6.16.

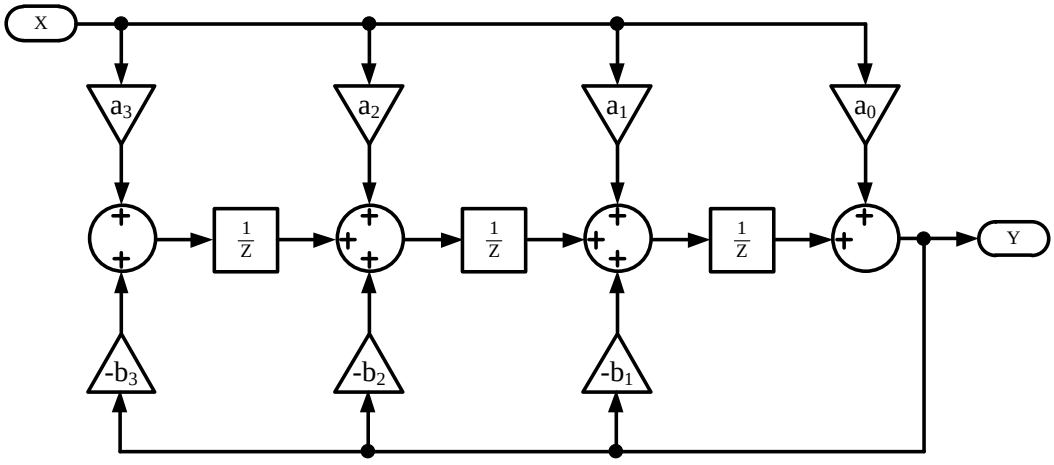


Fig. 6.16. Digital Implementation of Type-III Compensator.

CHAPTER 7

DIGITAL ACMC BUCK CONVERTER MEASUREMENT

The digital ACMC buck converter together with the average current sensing architecture is implemented in high voltage ON i2t100 0.7µm power CMOS process. The die micrograph is shown in Fig. 7.1. The chip size is 3.5mm by 3.5mm.

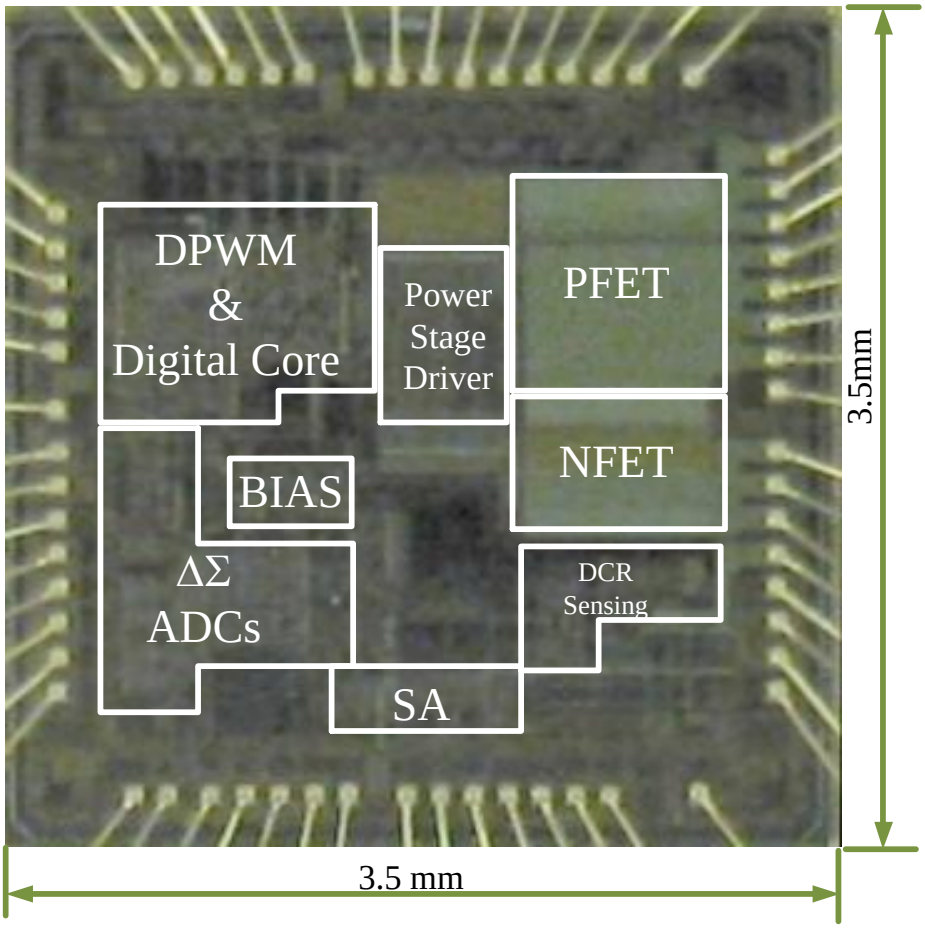


Fig. 7.1. Digital ACMC Buck Converter Die Micrograph.

7.1 PCB Design and Test Setup

A test PCB is designed for the digital ACMC buck converter verification and test. The PCB has two soft bondable gold metal layers. The die of the digital ACMC buck converter is wire-bonded to the PCB directly. PCB uses the standard 62 mil thickness FR4 board material. The size of the PCB is 6.9 inch by 5.5 inch. The photo of PCB with all the components soldered is shown in Fig. 7.2.

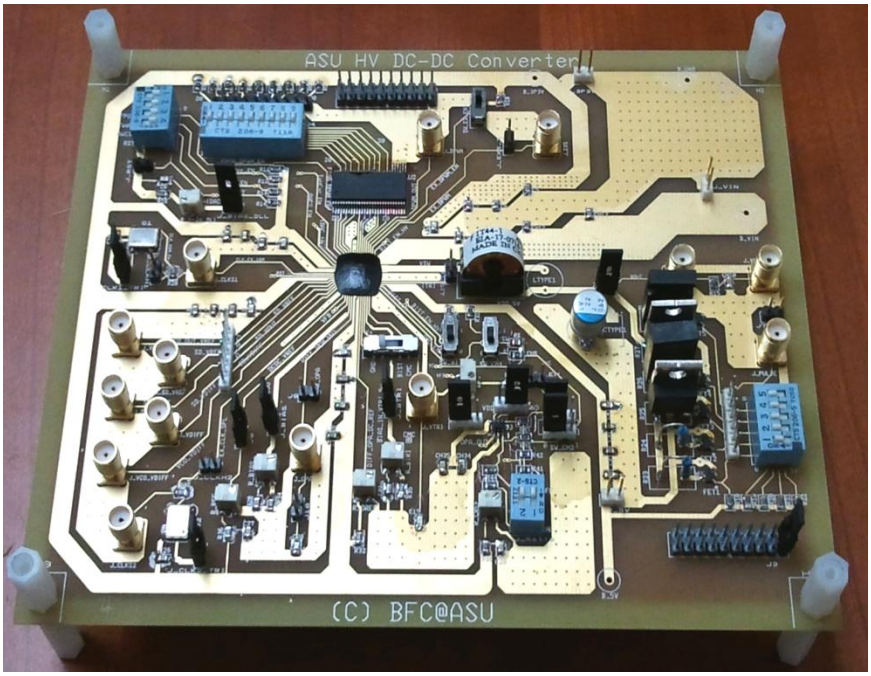


Fig. 7.2. Digital ACMC Buck Converter Test Board.

The test board can perform comprehensive tests and measurement including DC-DC normal load regulation test, DC-DC efficiency test and key individual modules test including DLL, DPWM etc.

The lab setup is similar to that of digital VMC DC-DC buck converter measurement. One arbitrary function generator is used to provide the load regulation switching control signal. The oscilloscope monitors the signals to be observed. When testing current sensing accuracy, a logic analyzer is utilized to track the ΔΣ ADC digitized current. A spectrum analyzer is used to measure the DC-DC key output signals spectrum.

7.2 Measurement Results

A batch of 7 PCBs are manufactured, assembled and tested. Unless specially clarified, the measurement results shown in this section are the typical data.

7.2.1 DPWM Linearity Measurement

The digital ACMC buck converter's DPWM linearity measurement result is given in Fig. 7.3. To measure the linearity of DPWM, we used similar measurement setup as that of digital VMC buck converter DPWM linearity measurement in Chapter 5. As the DPWM 5b MSBs are merely controlled by counter and comparator path, we first set LSBs to constants and change MSBs from zeros to full ones. This can test the DPWM coarse part operation. Next we set MSBs to constants and change LSBs from zeros to full ones to test the DLL operation. Finally, we set DPWM code from {MSB 0000} to {MSB+1 1111} to test the DPWM linearity when both MSB and LSB change.

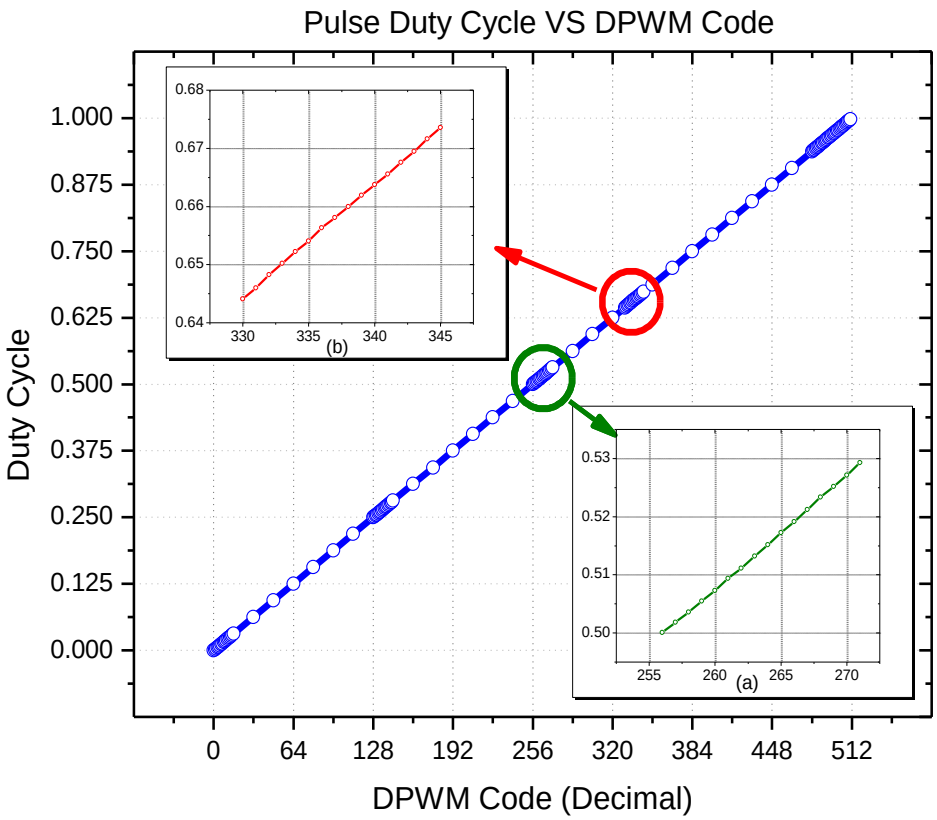


Fig. 7.3. Measured Linearity of MDLL Based DPWM.

The DPWM input duty cycle code we tested covered all the corners and full range. Inset (a) shows the duty cycles for code range [1000*0000*, 1000*1111*]. It purely demonstrates the linearity of the MDLL since only LSBs are changed here. As MDLL is bang-bang DLL, the linearity shown is the worst case scenario. Inset (b) shows the duty cycle for code range of [10100*1010*, 10101*1001*]. As both MSBs are LSBs are varying, it tests the linearity of DPWM when its digital counter and DLL work together. As shown in Fig. 7.3, DPWM shows good linearity and monotonicity. The maximum error of one least significant bit (LSB) delay of the proposed DPWM is less than 1%.

7.2.2 Average Current Sensing Performance

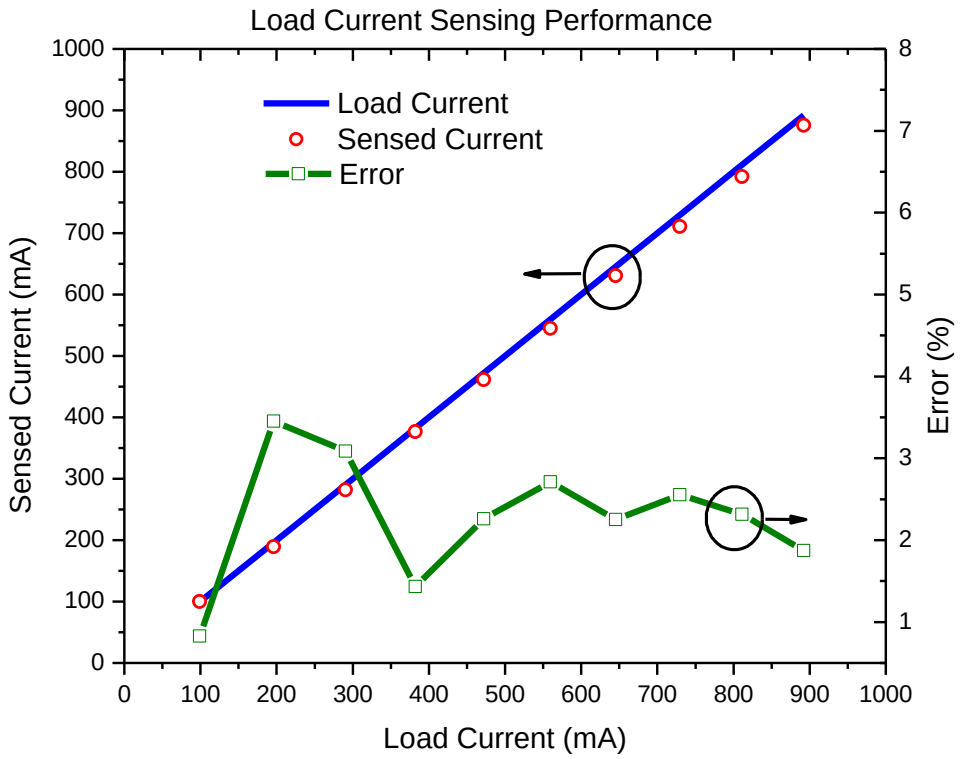


Fig. 7.4. Average Inductor Current Sensing Performance.

An accurate average inductor current sensing ability is a requirement for average current mode control. The performance of the proposed average inductor current (i.e. the load current) sensing performance is depicted in Fig. 7.4. It achieves 2.3% average error for 0.1-0.9A range load current. Here current sensing is based on an L=18μH, R_{DCR}=62mΩ inductor. And the buck converter output voltage V_{OUT} is 3.3V under all current sensing benchmark.

7.2.3 Load Regulation Measurement

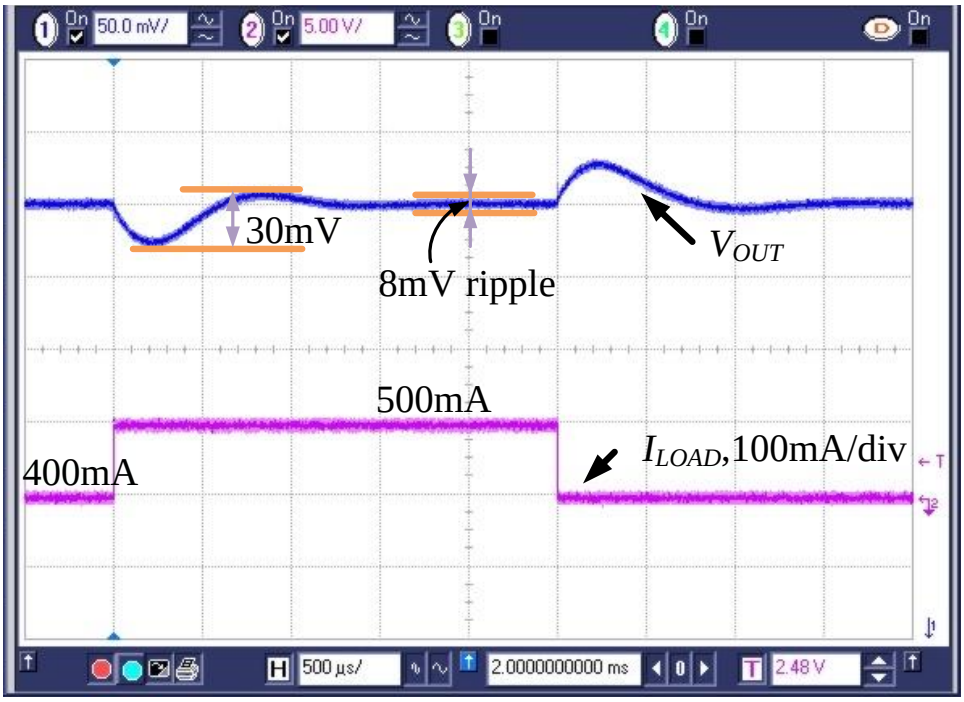


Fig. 7.5. Typical Digital ACMC Buck Converter Transient Response.

A typical load regulation transient response of the proposed digital ACMC buck converter is given by Fig. 7.5. Here, the DC-DC output voltage V_{OUT} is 3.3V. For a load current change of 100mA switching at 200kHz, the regulator shows an overshoot voltage of about 30mV and settling time of around 1.25ms. The parameters of power LC filter are: filter capacitance C=330µF, capacitor ESR=25mΩ, filter inductor inductance L =18µH, and inductor R_{DCR}=62mΩ.

7.2.4 Efficiency Measurement

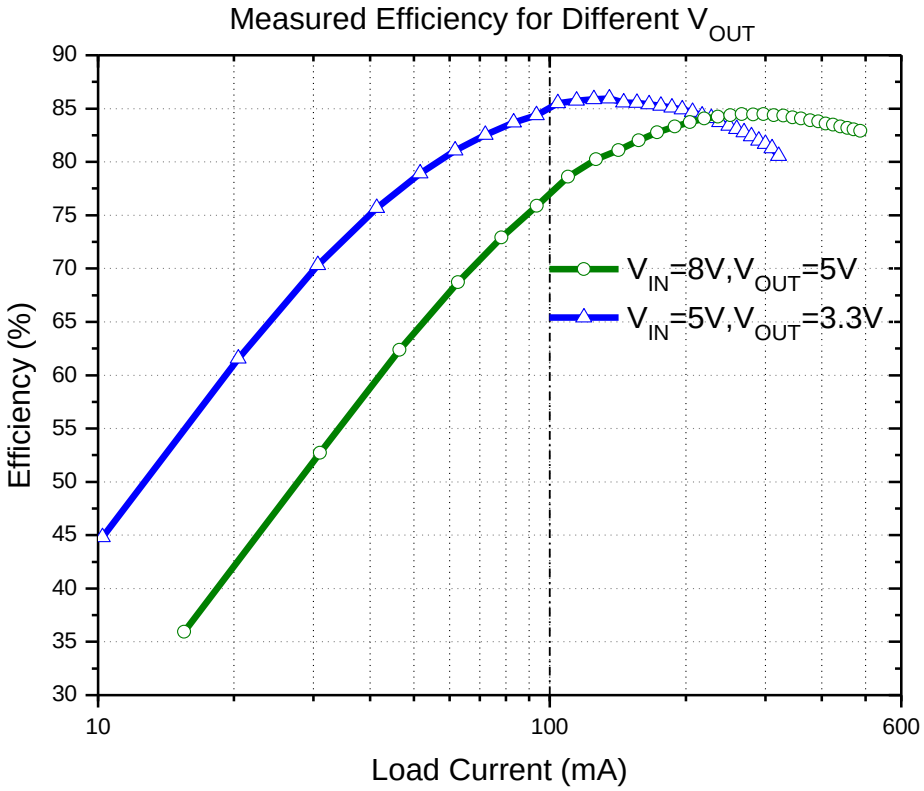


Fig. 7.6. Measured Digital ACMC Buck Converter Efficiency.

The measured digital ACMC buck converter efficiency curve is depicted in Fig. 7.6. When converter V_{IN}=8V, V_{OUT}=5V, converter achieves >78.6% efficiency for load range [0.1A, 0.5A] with a peak efficiency of 84.5%. When converter V_{IN}=5V, V_{OUT}=3.3V, converter achieves >78.9% efficiency for load range [0.05A, 0.35A] with a peak efficiency of 85.9%. The measured efficiency of this digital ACMC buck converter is worse than the digital VMC buck converter. This results from the high voltage transistor used in this ACMC buck converter. The 30V DMOS consumes larger chip area than the standard 5V MOSFET used in the

VMC buck converter. Due to the limitation of the same chip area, the R_{DS} of this converter power switch increases nearly five times. Power switches R_{DS} power loss becomes a major reason of efficiency degradation.

7.3 Chip Performance Summary

A summary of the digital ACMC DC-DC converter performance is provided in Table 7.1.

Table 7.1. Summary of Digital ACMC DC-DC Performance

DC-DC Converter Parameters	
Technology	ON i2t100 0.7μm CMOS
V_{IN}	3V-12V
V_{OUT}	1V-11.5V
Max Output Power	3W
Output Voltage Ripple	≤15mV
Switching Frequency	375kHz-500kHz (Typical 375kHz)
Off-chip Capacitor	330μF
ESR of Capacitor	25mΩ
Off-chip Inductor	18μH
DCR of Inductor	62mΩ
Efficiency	
I_{LOAD} [100mA – 500mA] @V_{IN}=8V, V_{OUT}=5V	78.6% ≤η≤ 84.5%
I_{LOAD} [50mA – 350mA] @V_{IN}=5V, V_{OUT}=3.3V	78.9% ≤η≤ 85.9%
Load Current Sensing Performance	
I_{LOAD} [100mA – 900mA] (@DCR=72mΩ, V_{OUT}=3.3V)	Average Error 2.3%
Chip Area	
Die	3.5mm × 3.5mm
Quiescent Current Consumption	
Current sensing	390μA
Normal regulation	980μA

The chip is a 0.7μm process, maximum 12V input, 1-11.5V output range, maximum 3W output power digital average current mode controlled DC-DC buck converter. The steady state ripper of DC-DC is less than 10mV with a 330μF, 25mΩ ESR capacitor and an 18μH, 62mΩ DCR inductor. The typical efficiency is above 78% with peak efficiency of around 85%. The average current sensing error is 2.3%. For the 3.5mm by 3.5mm die area, current sensing circuits including related pins only consume 5.2% of the die area.

CHAPTER 8

CONCLUSION

8.1 Summary

Current sensing ability of DC-DC converters has drawn wide attention due to its popular applications in current mode control, over current protection, current sharing, load balancing, mode hop, load current based compensation etc. After analyzing the issues of state-of-the-art current sensing approaches, an inductor BIST architecture is proposed to measure the inductor inductance and DCR. BIST functionality enables the proposed continuous, lossless, and accurate average current sensing scheme.

To verify the inductor BIST and current sensing method, a digital voltage mode controlled DC-DC buck converter with the inductor BIST and current sensing architectures is designed, fabricated, and experimentally tested. The chip is a 0.7μm process DC-DC converter with typical 5V input, maximum 1A load current, 8mV steady state ripper and a 22μF cap. The typical efficiency for load range of 0.1A to 1A is above 88% with a peak efficiency of 94.5%. The average measurement errors for inductance, DCR and current sensing are 2.1%, 3.6%, and 1.5% respectively. Among the 3.5mm by 3.5mm die area, inductor BIST and current sensing circuits including related pins only consume 5.2% of the die area.

BIST mode draws 40mA current for a maximum time period of 200μs upon start-up and the continuous current sensing consumes about 400μA quiescent current. This VMC buck converter embeds a look-up table based programmable loop controller. It is able to adjust the compensator based on the sensed inductor inductance and load inductor, hence achieving proper loop response for a wide range of inductor and load conditions.

Another digital average current mode controlled DC-DC buck converter is designed based on the inductor BIST and average current sensing architecture as well. It's fabricated by using ON i2t100 0.7μm 3-layer metal process. This ACMC buck converter has a maximum of 12V input, 1-11.5V output range, and a maximum of 3W output power. The steady state ripper of DC-DC is less than 10mV with a 330μF, 25mΩ ESR capacitor and an 18μH, 62mΩ DCR inductor. The typical efficiency is above 78% with a peak efficiency of around 85%. A 9 bits hybrid DPWM which uses a MDLL is also proposed. The maximum error of one LSB delay of the proposed DPWM is less than 1%.

The proposed inductor BIST and continuous lossless current sensing architecture have the following features:

1. High accuracy measurement of power inductor inductance, DCR and load current.

2. Low complexity. The effectiveness comes from mainly two aspects:

    2.1. SA offset independence. The measurement accuracy does not depend on sense amplifier's offset and DC level. Thus high performance instrument amplifier is not necessary.

    2.2. Intensive digital domain processing nature. Due to the digital processing approach, low power consumption, low hardware overhead PMIC with advanced PID control method becomes feasible.

3. High reliability. Since the monitored inductor information and load current are used to update the system controller, the system has very high robustness against temperature, process variation, and external components aging effect. This makes it suitable for harsh environment and high reliability applications.

4. Wide application possibilities. The inductor BIST and current sensing architecture demonstrated in this dissertation is based on DC-DC buck converters, but it can be applied to other converter configurations as well, such as boost, buck-boost, SIMO sytem etc.

8.2 Future Work

In the current sensing architecture, the current sense amplifier uses a resistor feedback configuration. Compared to the conventional switching capacitor method, it significantly reduces the switching noise at the DC-DC output node.

The drawback is that it’s not suitable for ultra light load application where the current that goes through the sense amplifier feedback resistors is no longer ignorable. A different architecture needs to be used to handle the light load condition.

The proposed accurate current sensing scheme makes advanced control methods feasible. They can be applied to both digital VMC and ACMC buck converters. For example, PFM mode can be utilized when the sensed load current is low, thus the overall efficiency can be improved. Also, the switching frequency can be adjusted for different load conditions to achieve optimal efficiency.

In addition to the inductor BIST, a capacitor BIST architecture can be developed as well so that the DC-DC can perform self-tuning based on sensed power capacitor and inductor, eventually achieving off-chip components independent control.

REFERENCES

[1] N. Andrews, "The Global Market for Power Supply and Power Management Integrated Circuits," *IEEE Applied Power Electronics Conference and Exposition*, pp.126-131, Mar. 2002.

[2] "Thirty Billion Power Conversion ICs Enable Power Management Applications, Says Petrov Group," [online Document], Petrov Group, compiled by Digitimes, August 2010, Available HTTP: http://www.petrovgroup.com/pdfs/Aug%2024-10%20article%20-%2030B%20power%20conversion%20ICs.pdf

[3] "Power Management ICs in Portable Devices Represent nearly 40% of Total Analog IC Revenues, Says Petrov Group," [online Document], Petrov Group, compiled by Digitimes, August 2010, Available HTTP: http://www.petrovgroup.com/pdfs/Aug%2010-10%20-%20Power%20management%20ICs%20in%20portable%20dev..pdf

[4] Power Management Market Report, [online Document], Electronics.ca Publications, 2010. Available HTTP: http://www.electronics.ca/publications/products/Power-Management-Market-Report.html

[5] H. Ahmad, B. Bakkaloglu, "A 300mA 14mV-Ripple Digitally Controlled Buck Converter Using Frequency Domain ΔΣ ADC and Hybrid PWM Generator," *ISSCC Dig. Tech. Papers*, pp. 202-203, Feb. 2010.

[6] E. Soenen, A. Roth, J. Shi, et al., "A Robust Digital DC-DC Converter with Rail-to-Rail Output Range in 40nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 198-199, Feb. 2010.

[7] T. Liu, H. Yeom, B. Vermeire, et al., "A Digitally Controlled DC-DC Buck Converter with Lossless Load current Sensing and BIST Functionality," *ISSCC Dig. Tech. Papers* pp. 388-390, Feb. 2011.

[8] D. Prodic, D. Maksimovic and W. Erickson, "Design of a Digital PID Regulator Based on Look-Up Tables for Control of High-Frequency DC-DC Converters ," *IEEE COMPEL*, pp. 18-22, Jun. 2002.

[9] M. Chui, W. Ki, and C. Tsui, “A Programmable Integrated Digital Controller for Switching Converters with Dual-Band Switching and Complex Pole-Zero Compensation,” *IEEE* J. *Solid State Circuits*, vol. 40, Mar. 2005.

[10] D. Maksimovic, R. Zane, R. Erickson, “Impact of Digital Control in Power Electronics,” *IEEE ISPSD*, pp.13-22, Sep. 2004.

[11] M. Ilic, D. Maksimovic, “Digital Average Current-Mode Controller for DC–DC Converters in Physical Vapor Deposition Applications,” *IEEE Tran. Power Electronics*, vol. 23, pp. 1428 - 1436, May. 2008.

[12] J. Chen, A. Prodic, R. W. Erickson, et al., “Predictive Digital Current Programmed Control,” *IEEE Trans. Power Electron.*, vol. 18, pp. 411–419, Jan. 2003.

[13] M. Belloni, E. Bonizzoni, E. Kiseliovas, et al., “A 4-Output Single-Inductor DCDC Buck Converter with Self-Boosted Switch Drivers and 1.2A Total Output Current,” *ISSCC Dig. Tech. Papers*, pp. 444-445, Feb., 2008.

[14] K-C. Lee, C-S. Chae, G-H. Cho, et al., “A PLL-Based High-Stability Single-Inductor 6-Channel Output DC-DC Buck Converter,” *ISSCC Dig. Tech. Papers*, pp.200-201, Feb., 2010.

[15] K-S. Seol, Y-J. Woo, G-H. Cho, et al., “Multiple-Output Step-Up/Down Switching DC-DC Converter with Vestigial Current Control,” *ISSCC Dig. Tech. Papers*, pp. 442-443, Feb., 2009.

[16] M-H. Huang and K-H. Chen, “Single-Inductor Dual Buck-Boost Output (SIDBBO) Converter with Adaptive Current Control Mode (ACCM) and Adaptive Body Switch (ABS) for Compact Size and Long Battery Life in Portable Devices,” *Dig. Symp. VLSI Circuits*, pp. 164-165, Jun., 2009.

[17] W. Xu, Y. Li, X. Gong, et al., “A Dual-Mode Single-Inductor Dual-Output Switching Converter with Small Ripple,” *IEEE Tran. Power Electronics*, vol. 25, no. 3, pp. 614-623, Mar., 2010.

[18] Y. Woo, H. Le, G. Cho, et al., "Load-Independent Control of Switching DC-DC Converters with Freewheeling Current Feedback," *ISSCC Dig. Tech. Papers*, pp. 446 - 447, Feb. 2008.

[19] W. Schults, "Lossless Current Sensing with SENSEFET Enhance the Motor Drive," Motorola Technical Report, 1988.

[20] S. Yuvarajan, "Performance Analysis and Signal Processing in a Current Sensing Current MOSFET (SENSEFET)," in *Proc. Industry Applications Society Annual Meeting*, pp. 1445–1450, 1990.

[21] P. Givelin, M. Bafleur, "On-Chip Over-Current and Open-Load Detection for a Power MOS High-Side Switch: a CMOS Current-Source Approach," in *Proc. European Conference on Power Electronics and Applications*, pp. 197–200, 1993.

[22] S. Yuvarajan and L. Wang, "Power Conversion and Control Using a Current-Sensing MOSFET," *in Proc. Midwest Symposium on Circuits and Systems (MWSCAS)*, pp.166 –169, 1992.

[23] J. Chen, J. Su, H. Lin, et al., "Integrated Current Sensing Circuits Suitable for Step-Down DC-DC Converters," *Electronics Letters*, vol. 40, pp. 200-201, Feb. 2004.

[24] C. Lee and P. Mok, "A Monolithic Current-mode CMOS DC-DC Converter with On-Chip Current-Sensing Technique," *IEEE Journal of Solid States Circuits*, vol. 39, pp. 3-14, Jan. 2004.

[25] D. Grant and R. Pearce, "Dynamic Performance of Current-Sensing Power MOSFETs," *Electronic Letters*, pp. 1129-1131, Sep. 1988.

[26] D. Grant and R. Williams, "Current Sensing MOSFETs for Protection and Control," *IEE Colloquium on Measurement Techniques for Power Electronics*, pp. 8/1-8/5, 1992.

[27] C. Xiao, L. Zhao, T. Asda, W. Odendaal, and J. van Wyk, “An overview of Integratable Current Sensor Technologies,” in *Proc. Industry Applications Conference*, pp. 1251-1258, 2003.

[28] Z. Randjelovic, M. Kayal, R. Popovic, and H. Blanchard, “Highly Sensitive Hall Magnetic Sensor Microsystem in CMOS Technology,” *IEEE Journal of Solid States*, pp. 151-159, Feb. 2002.

[29] A. Bilotii, G. Monreal, and R. Vig, “Monolithic magnetic Hall sensor using dynamic quadrature offset cancellation,” *IEEE Journal of Solid States*, vol. 32, pp. 829-836, Jun.1997.

[30] K. Nose and T. Sakurai, “Integrated Current Sensing Device for Micro IDDQ Test,” in *Proc. test symposium*, pp. 323-326, 1998.

[31] Datasheet, “Current Sensor: ACS750xCA-050,” Allegro Microsystems Inc., 2001.

[32] N. McNeill, N.K. Gupta, W.G. Armstrong, “Active Current Transformer Circuits for Low Distortion Sensing in Switched Mode Power Converters,” *IEEE Tran. Power Electronics*, pp.908 - 917 , vol.19, July 2004.

[33] P. Midya, M Greuel and P. Krein, “Sensorless Current Mode Control - An Observer Technique for DC-DC Converters,” *IEEE Tran. Power Electronics*, vo. 16, pp. 522-526, July 2001.

[34] X. Zhou, X. Peng and F. Lee “A High Power Density, High Efficiency and Fast Transient Voltage Regulator Module with A Novel Current Sensing And Current Sharing Technique,” *Applied Power Electronics Conference and Exposition*, vol. 1, pp 289-294, 1999.

[35] Y. Dong, M. Xu, and. Lee, “DCR Current Sensing Method for Achieving Adaptive Voltage Positioning(AVP) in Voltage Regulators with Coupled Inductors,” *IEEE Power Electronics Specialists Conference*, pp. 1-7, 2006.

[36] R. Lenk, “Application Bulletin AB-20: Optimum Current-Sensing Techniques in CPU Converters,” *Fairchild Semiconductor Application Notes*, 1999.

[37] E. Dallago, M. Passoni, and G. Sassone, “Lossless Current-Sensing in Low-Voltage High-Current DC-DC Modular Supplies,” *IEEE Tran. Industrial Electronics*, pp. 1249-1252, Dec. 2000.

[38] H. Forghani-zadeh and G.A. Rincón-Mora, “Current-sensing techniques for DCDC converters,” in *Proc Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 577-580, 2002.

[39] H. Forghani-zadeh, “An Integrated, Lossless, and Accurate Current-Sensing Technique for High-Performance Switching Regulators,” Ph.D. Dissertation, Georgia Institute of Technology, Aug. 2006.

[40] H. Forghani-zadeh, G. Rincón-Mora, “An Accurate, Continuous, and Lossless Self-Learning CMOS Current-Sensing Scheme for Inductor-Based DC-DC Converters,” *IEEE Journal of Solid States Circuits*, pp. 665-679, vol.42, Mar. 2007.

[41] S. Ziegler et al., “Current Sensing Techniques: A Review,” *IEEE Sensors Journal*, vol. 9, no. 4, Apr. 2009.

[42] W. Rhee, “Design of High-Performance CMOS Charge Pumps in Phase-Locked Loops,” *IEEE International Symposium on Circuits and Systems*, pp. 545-548 vol.2, 1999.

[43] D. Wisland, M. Høvin, T. Lande, “A Novel Multi–bit Parallel ΔΣ FM–to–digital Converter with 24–bit resolution”, *Proc. 28th European Solid-State Circuits Conference*, pp. 687-690, 2002.

[44] M. Hovin, A. Olsen, T. Lande, et al., “Delta-Sigma Modulators using Frequency-Modulated Intermediate Values” *IEEE Journal of Solid-Sate Circuits*, vol. 32, no. 1, pp. 13-22, Jan 1997.

[45] M. Hovin, D. Wisland, J. Marienborg, et al., "Pattern Noise in the Frequency ΔΣ Modulator." *Analog Integrated Circuits and Signal Processing*, pp. 75-82, 2000.

[46] J. C. Candy and O. J. Benjamin, "The Structure of Quantization noise from Sigma-Delta Modulation," *IEEE Tran. Communication*, pp. 1316-1323, 1981.

[47] H. Ahmad, "Digitally Controlled DC-DC Buck Converter Utilizing ΔΣ Frequency Discriminators," Ph.D. Dissertation, Arizona State University, Dec. 2009.

[48] E. Hogenauer, "An Economical Class of Digital Filters for Decimation and Interpolation," *IEEE Tran. Acoustics, Speech, and Signal Processing*, vol. ASSP-29, no. 2, pp.155-162, Apr. 1981.

[49] M. Frerking. *Digital Signal Processing in Communication Systems*. Kluwer Academic Publishers, Boston, 1994.

[50] A. Kwentus, Z. Jiang, and A. Wilson, Jr. "Application of Filter Sharpening to Cascaded Integrator-Comb Decimation Filters," *IEEE Tran. Signal Processing*, vol. 45, pp. 457-467, 1997.

[51] A. Peterchev, S. Sanders, "Quantization Resolution and Limit Cycling in Digitally Controlled PWM Converters," *IEEE Tran. Power Electronics*, vol.18, pp.301-308, 2003.

[52] D. Prodic, D. Maksimovic and W. Erickson, "Design and Implementation of a Digital PWM Controller for a High-Frequency Switching DC-DC Power Converter", *IECON*, vol. 2, pp. 893-898, Nov 2001.

[53] C. Yoo, "A CMOS Buffer Without Short-Circuit", *IEEE Tran. Circuits and Systems II*, vol. 47, no. 9, pp: 935-937, Sept, 2000.

[54] S. Lee, S. Jung, J. Huh, et al., "Robust and Efficient Synchronous Buck Converter with Near-Optimal Dead-Time Control," *ISSCC Dig. Tech. Papers*, pp. 392-393, Feb. 2011.

[55] X. Zhou, P. Xu, F. Lee, "A Novel Current-Sharing Control Technique for Low-Voltage High-Current Voltage Regulator Module Applications," *IEEE Tran. Power Electronics*, pp.1153-1162, vol. 15, Nov. 2000.

[56] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Norwell, MA: Kluwer, 2001.

[57] P. Li, L. Xue, D. Bhatia, et al., "Digitally Assisted Discontinuous Conduction Mode 5V 100MHz and 10V 45MHz DC-DC Boost Converters with Integrated Schottky Diodes in Standard 0.13μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 206-207, Feb. 2010.

[58] B. Mesgarzadeh, and A. Alvandpourand, "A Low-Power Digital DLL-Based Clock Generator in Open-Loop Mode," *IEEE Journal of Solid States Circuits*, vol. 44, pp. 1907-1913, Jul. 2009.

[59] R. Gregorian, *Introduction to CMOS Op-Amps and Comparators*. New York: Wiley, 1999.

[60] P. Allen, D. Holberg, *CMOS Analog Circuit Design*, New York, Offord University Press, 2002.

[61] W. Ki, "Signal Flow Graph in Loop Gain Analysis of DC–DC PWM CCM switching converters," *IEEE Tran. Circuits Syst. I*, vol. 45, pp. 644-655, Jul. 1998.

[62] V. Vorperian, "Simplified Analysis of PWM Converters Using Model of PWM switch-Part I: Continuous Conduction Mode," *IEEE Tran. Aerospace Electron. Syst*., vol. 26, pp. 490-496, May. 1990.

[63] L. Dixon, "Average Current-Mode Control of Switching Power Suppliers," *Unitrode Power Supply Design Seminar Manual*, SEM-700, 1990

[64] R. Ridley, "A New Small Signal Model for Current Mode Control," Ph.D. Dissertation, Virginia Polytechnic lnstitute and State University, November 1990.

[65] R. Ridley, “A New, Continuous-Time Model for Current-Mode Control,” *IEEE Tran. Power Electronics*, vol. 6, no. 2, pp. 271-280, 1991.

[66] W. Tang, F. Lee, and R. Ridley, “Small Signal Modeling of Average Current Mode Control,” *IEEE Tran. on Power Electronics*, vol. 8, pp.112-119, April 1993.

[67] W. Tang, “Average Current-Mode Control and Charge Control for PWM Converters,” PhD Dissertation, Virginia Polytechnic Institute and State University, Oct. 1994.

[68] Y. Jung, J. Lee, and M. Youn, “A New Small-Signal Modeling of Average Current Mode Control,” *IEEE Power Electronics Specialists Conference*, pp. 1118-1124, 1998.

[69] J. Sun and R. Bass, “Modeling and Practical Design Issues for Average Current Control,” *IEEE Applied Power Electronics Conference*, pp. 980-986, Mar. 1999.

[70] P. Cooke, “Modeling Average Current Mode Control,” *IEEE Applied Power Electronics Conference and Exposition*, vol.1, pp.: 256-262, 2000.