A 5 GHz Ring-Oscillator PLL with Active Delay-Discriminator Phase Noise Cancellation Loop

by

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ABSTRACT

Voltage Control Oscillator (VCO) is one of the most critical blocks in Phase Lock Loops (PLLs). LC-tank VCOs have a superior phase noise performance, however they require bulky passive resonators and often calibration architectures to overcome their limited tuning range. Ring oscillator (RO) based VCOs are attractive for digital technology applications owing to their ease of integration, small die area and scalability in deep submicron processes. However, due to their supply sensitivity and poor phase noise performance, they have limited use in applications demanding low phase noise floor, such as wireless or optical transceivers. Particularly, out-of-band phase noise of RO-based PLLs is dominated by RO performance, which cannot be suppressed by the loop gain, impairing RF receiver's sensitivity or BER of optical clock-data recovery circuits. Wide loop bandwidth PLLs can overcome RO noise penalty, however, they suffer from increased in-band noise due to reference clock, phase-detector and charge-pump. The RO phase noise is determined by the noise coming from active devices, supply, ground and substrate.

The authors adopt an auxiliary circuit with inverse delay sensitivity to supply noise, which compensates for the delay variation of inverter cells. Feed-forward noise-cancelling architecture that improves phase noise characteristic of RO based PLLs is presented. The proposed circuit dynamically attenuates RO phase noise contribution outside the PLL bandwidth, or in a preferred band. The implemented noise-cancelling loop potentially enables application of RO based

PLL for demanding frequency synthesizers applications, such as optical links or high-speed serial I/Os.

The PLL is fabricated in a 90 nm CMOS technology. The core of the IC occupies 0.38mm × 0.32mm silicon area. The current consumption of the PLL is 24.7 mA when the cancellation technique enabled. PLL output spectra at 5.1 GHz when the PLL divider is modulated with a 10 MHz clock signal. Phase noise reduces in the cancellation bandwidth up to 20 MHz with a 200 kHz PLL loop bandwidth. The proposed cancellation loop suppresses the phase noise at 1 MHz offset by 12.5 dB and reference spur by 13dB, with a quiescent power consumption of 3.7 mA.

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CHAPTER 1

INTRODUCTION

Phase noise is important consideration in many wireless communication applications. Phase noise in a system can degrade the bit error rate of a communications link. In many wireless applications, a phase locked-loop circuit for providing low noise clock signals is required.

The role of oscillator in transceiver systems is frequency translation. Local oscillator uses to up-convert or down-convert the signals for transmitting and receiving between wireless applications. Phase noise and spurious tones of oscillator determines the limitation of selectivity of a system while strong adjacent interferers are considered.

In many digital and analog communications systems, when the signals are received and transmitted in channels, the data is modulated using not only the amplitude of the signal, but also the phase of the signal. PLL in the transceiver modulates and demodulate the desired information. Therefore, phase noise in PLL causes to degrade selectivity and sensitivity in translating the information to different frequency bands.

A local crystal oscillator uses to generate reference frequency. However, in many communication systems, PLL easily generates clock or oscillator signals compared to the crystal oscillators. The sensitivity is the smallest detecting RF power at the input and recovering a digital signal at given signal to noise ratio. The noise produced by the passive and active components in the system can limit the sensitivity. The noise figure, which is the ratio of the signal to noise ratio at

the input to that at the output, determines the performance of the sensitivity. The other factor of performance in the transceiver is selectivity. The selectivity makes receiving signals from strong signal in adjacent channel or other channel bands. If the system products the distortion and the inter-modulated signal generates, this signal can swamp out the desired signal and we called blocker requirements in wireless system.

In frequency domain, the close-in phase noise of the VCO is filtered by the PLL loop filter, however, the far-out noise of the VCO cannot be shaped and filtered by the PLL and which will impact the overall system performance. For example, for data converters, the far-out noise, impacts the SNR. For high-speed optical communication, the jitter requirement is less than few ps and it can impact the SNR and the BER of the transceiver. For RF transmitter, the far-out noise impacts the out-of-band transmit noise and the PSD of the transmitted signal. For RF receivers, the out-of band noise impacts the adjacent channel noise and will alias in receive band.

1.1 PHASE NOISE SPECIFICATIOIN

For the receiver, the purpose of the specifications is to ensure that the receiver is able to receive the wanted signal correctly in an environment where other users of the frequency spectrum are causing interference. The specifications typically include the minimum power of the wanted signal that the receiver should still be able to receive correctly. In addition, the interfering signals are specified

that the receiver is required to tolerate while still correctly receiving the wanted signal. The interferers can be much higher in power than the wanted signal.

For the transmitter, the purpose of the specifications is to restrict the amount of interference cause by the transmitter to other users of the frequency spectrum, and to ensure that the quality of the transmitted signal is good enough to be received correctly with a receiver fulfilling the specifications of the same system. Typically, the specifications include a spectral mask, which means the maximum power level of the components of the transmitted spectrum at different offset frequencies. In phase modulated signals, this is typically the maximum phase error of the actual transmitted signal with respect to the ideal one. In more complex modulation types, the typical measure of modulation quality is error vector magnitude (EVM), which takes into account both the phase error and the amplitude error of the actual transmitted signal with respect to the ideal one.

Phase noise determines the overall performance of the wireless system. Phase noise and spurious tones in the local oscillator translate the signal in the desired channel into the adjacent channel. The blocking specifications in the receiver also determine the acceptable phase noise and spurious levels in the sidebands of the local oscillator spectrum. In order to meet receiver blocking requirements, phase noise and spurious tone levels need to be smaller than any interfering signal compared to the desired. For a spurious tone, the amplitude of the tone needs to be below that of the carrier by an amount equal to the worst case difference in signal power levels plus the minimum signal-to-interferer ration required at the end of the receive chain. The requirements for phase noise are

similar to those for spurious tones. The power spectral density of the oscillator is integrated over that channel's bandwidth to find the total power in a given channel band. This power level must be below the receiver's signal-to-interferer noise requirements.

The phase noise specification at large offset frequency can be calculated from adjacent channel interference requirements [2].

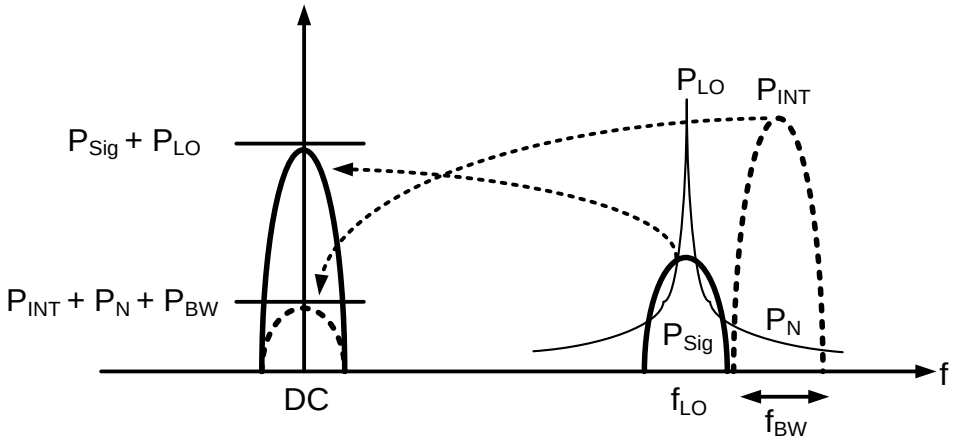


Figure 1.1 The effect of phase noise and interference.

Figure 1.1 shows the effect of phase noise and adjacent channel interference. While the signal (P_{Sig}) is downconverted to DC by the LO signal (P_{LO}), the interference (P_{Int}) is also downconverted to DC by the phase noise (P_N) and is added to the desired signal. The signal to noise ratio (SNR) of the baseband signal is the difference of the power of the two, and it must be larger than the minimum SNR required to meet the receiver bit error rate (BER) requirement

$$SNR = (P_{Sig} + P_{LO}) - (P_{INT} + P_N + P_{BW}) > SNR_{\min} \tag{1.1}$$

$$P_N - P_{LO} < P_{Sig} - P_{INT} - P_{BW} - SNR_{\min} \tag{1.2}$$

where P_N - P_{LO} denotes the phase noise requirement in dBc. For example, IEEE 802.11a standard uses 64-QAM with OFDM in a 20 MHz channel bandwidth for highest data rate of 54 Mb/s. The standard specifies an adjacent interferer +32 dB stronger than the desired channel at 40 MHz away. The minimum SNR requirement for BER of 10^{-6} in 64-QAM system is 19 dB.

$$\begin{aligned} P_N - P_{LO} &= P_{Sig} - P_{INT} - P_{BW} - SNR_{\min} \\ &= -32 - 73 - 19 = -124 dBc/Hz \quad at\ 40\ MHz \end{aligned} \tag{1.3}$$

The phase noise requirement at 1 MHz is lower than -108dBc/Hz according to $1/f^2$ phase noise spectrum.

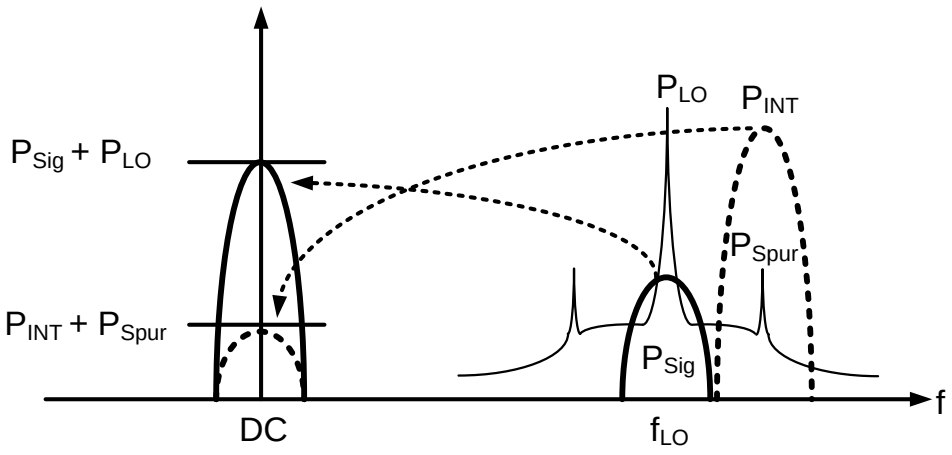


Figure 1.2 The effect of phase noise and interference.

In narrow band systems, the reference spur coincides with the adjacent channels as shown in Fig. 1.2. It causes more serious problem. The spur requirements in frequency synthesizer can be determined by donwconverting the interference by the spurious tone.

$$SNR = (P_{Sig} + P_{LO}) - (P_{INT} + P_{Spur}) > SNR_{\min} \quad (1.4)$$

$$P_{spur} - P_{LO} < P_{Sig} - P_{INT} - SNR_{\min} \quad (1.5)$$

Where P_{Spur} - P_{LO} denotes the power of spurious signal in dBc. The SNR of the received signal is degraded by a pair of downconverted signals of itself due to spurs. For example, the standard specifies an interferer of +32 dB ($P_{Sig} - P_{INT}$) at 40 MHz away from the desired signal. The minimum SNR requirement is 19 dB. From equation (1.5), the spurious signal requirement is -51 dBc at 40 MHz.

1.2 IMPACT OF PHASE NOISE IN WIRELESS COMMUNICATIONS

In this section the impact of phase noise on BER performance of a digital communications system will be examined.

1.2.1 Close-in Phase Noise

Phase noise of the PLL changes the phase of the modulated signal and cause phase error. The effect of close-in phase noise shows the modulated signal in the constellation diagram. Fig. 1.3 shows the constellation diagram of a QPSK system in the presence of the closed-in phase noise. The deviation between the ideal vector and the real one in the constellation diagram can be modeled as a random signal with Gaussian distribution. The standard deviation of this random signal is equal to the RMS phase error of the PLL. If the RMS value of the phase error is large, it degrades the detectable signal and increase the BER in communication system.

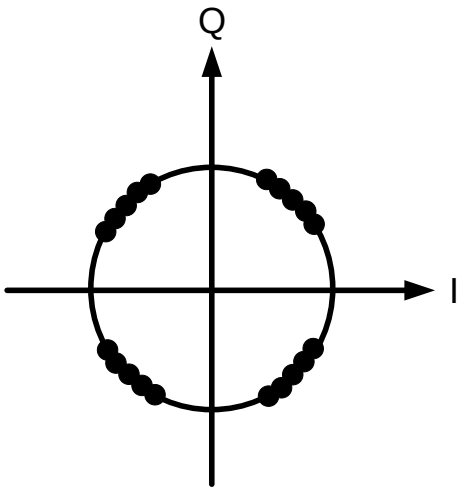


Figure 1.3 Phase noise in constellation diagram.

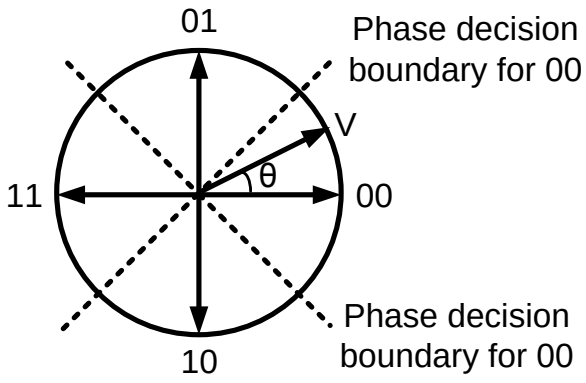


Figure 1.4 Error diagram for QPSK system.

Fig. 1.4 shows vector state diagram for QPSK system. This diagram shows phase decision boundaries that determine the state of the received vector. The enclosed radial distance between boundaries is equal to $2\pi/M$, where M=4 for

this system. When the angle θ of received vector, V placed between - $\pi/4$ and $\pi/4$ interprets this as the binary state 00. Variation in vector angle θ due to local oscillator phase noise are caused by the same random sources. The mean value of vector angle is zero and then the standard deviation is equal to RMS phase error Φ_{rms} [3]. If the AM noise is small relative to the phase noise, the mean square deviation in vector angle can be assumed to the integrated spectral density of phase fluctuations such as:

$$\theta_{rms}^2 = \phi_{rms}^2 \tag{1.6}$$

The probability of error P(e) for an M state PSK system may be approximated as [4]:

$$P(e) = K \cdot \exp\left[-\frac{C}{N} \sin^2\left(\frac{\pi}{M} \right) \right] \tag{1.7}$$

Where C/N is the mean-carrier power to mean-noise power ration specified in the double sided Nyquist bandwidth which equals the symbol rate bandwidth. The ration C/N may be equated directly with the total integrated mean-phase noise power to mean carrier power:

$$\left(\frac{C}{N} \right)^{-1} = \theta_{rms}^2 = \phi_{rms}^2 = 2\int L(f_m) df_m \tag{1.8}$$

It shows that BER can be estimated directly from the phase noise power spectrum. An example of BER versus C/N is shown in Fig. 1.5 for the QPSK system. QPSK modulation degrades the performance when rms phase error increases.

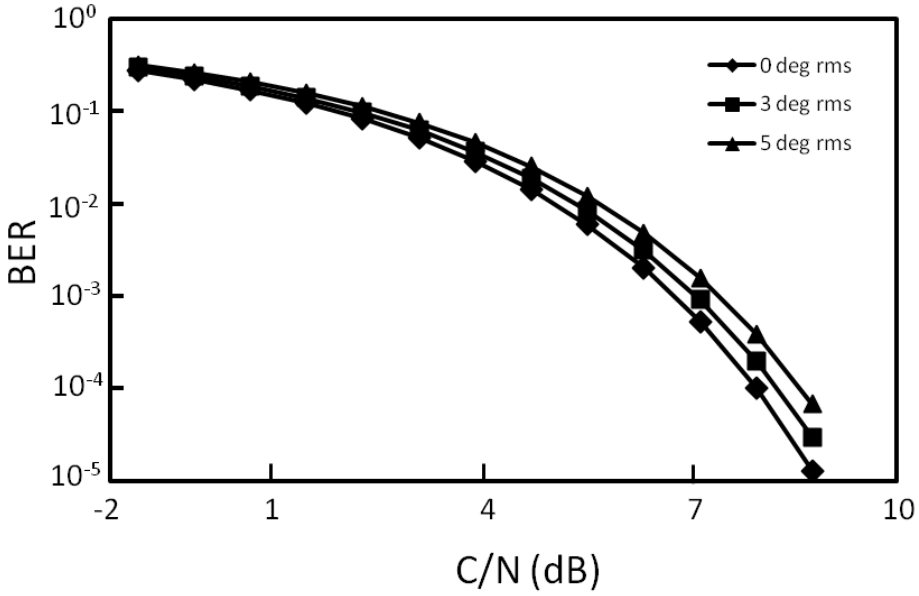


Figure 1.5 C/N versus BER for different rms phase error.

1.2.2 Far-out Phase Noise

The phase noise of the frequency synthesizer at large offset frequencies is specified. The reason for this is a phenomenon commonly referred to as reciprocal mixing. The phase noise tail of the local oscillator signal mixes with undesired interfering signals, and the mixing result ends up at the same intermediate frequency as the wanted signal, thus impairing the signal-to-noise ratio (SNR).

Since the interfering component can be much stronger that the wanted signal, the phase noise power of the local oscillator at the same offset frequency must correspondingly be much lower to maintain a useful SNR of the downconverted signal. The specification for the local oscillator power at a given offset frequency can be derived from the power levels of the wanted signal and

the interfering signal, and the SNR required to guarantee signal reception at the desired bit error rate:

$$L(\Delta f) < P_{desired} - SNR - P_{unwanted} - 10\log(BW) \tag{1.4}$$

where BW is channel bandwidth.

For far-out frequencies, the phase noise properties of a PLL based frequency synthesizer are normally dominated by the voltage-controlled oscillator, since the noise from the rest of the loop components is low-pass filtered.

In the transmitter, modulated signal transmits without undesired spectral emissions. However, this is rarely the case and thus limits must be set for the levels of unwanted spectral emissions. The spectral mask requirements affect both in-band and out-band emissions. Unwanted emissions are caused by phase noise from frequency synthesizers. Phase noise changes the modulated spectrum and cause spectral mask violations. Although phase noise decrease as the frequency of interest moves away from the LO frequency, phase noise is still a major concern at large offset frequencies because the spectral mask often decreases faster than the phase noise as shown in Fig. 1.6. As a result phase noise at large offset frequencies is often problematic in transmitter design.

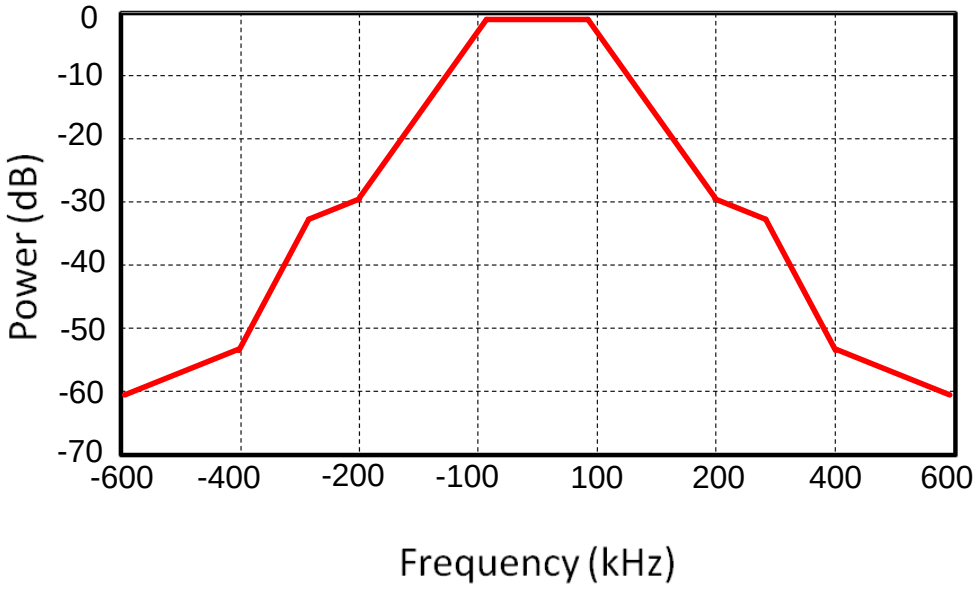


Figure 1.6 GSM spectral mask.

1.3 WIRELESS COMMUNICATION STANDARD

The IEEE 802.11a wireless local area network (WLAN) employs Orthogonal Frequency Division Multiplexing (OFDM) and is allocated at 5GHz with the signal bandwidth of 300MHz. This band can reach high data transmission of 54 Mb/s or higher. As shown in Fig. 1.1, WLAN consists of three sub-bands, which are low band operating from 5.15 to 5.25GHz, middle band operating from 5.25 to 5.35GHz, and high band from 5.725 to 5.825GHz.

IEEE 802.11a scheme defines four 20 MHz wide channels in each 100 MHz of two lower bands. Each of these channels is subdivided into 52 subcarriers and each subcarrier has 312.5 kHz bandwidth. The data in each channel are modulated with binary/quadrature phase shift keying (BPSK/QPSK), 16 or 64

quadrature amplitude modulation (QAM) and mapped into 52 subcarriers of an OFDM signal.

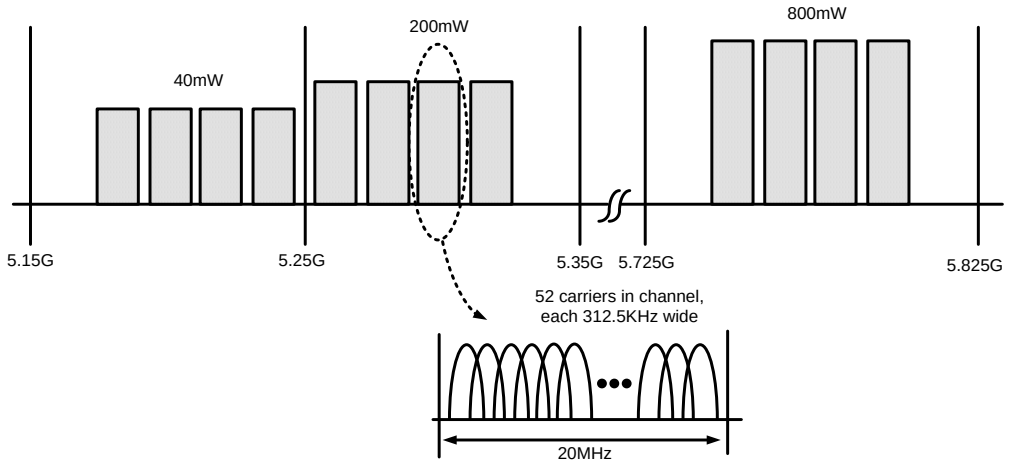


Figure 1.7 Channel allocation of the IEEE 802.11a standard.

The IEEE 802.11a standard and key parameters for the RF circuit designer are summarized in Table 1.1 [1].

Table 1.1 IEEE 802.11a Standard

Attribute	IEEE 802.11a
Frequency Band	5.150-5.350 GHz 5.725-5.825 GHz
Maximum Data Rate	54 Mb/s
Channel Spacing	20 MHz
Interference	+32 dB at 40 MHz
Modulation	OFDM (BFSK, QPSK, 16-QAM, 64-QAM)

20MHz wide channel spacing relaxes the loop bandwidth limitation of frequency synthesizer. In an integer-N synthesizer, output frequencies can synthesize only integer times of f_{REF}. Because of the relaxation of bandwidth limitation, the integer-N architecture will be adopted instead of fractional-N architecture.

1.4 Thesis Organizations

The rest of chapters are described as follow. Chapter 2 provides background material including phase noise in oscillators, methods of measuring phase noise, and explanation of phase-locked loop (PLL). In chapter 3, proposed adaptive phase noise cancellation PLL is described. Analysis of noise in cancellation loop and noise transfer function is explained detail. Chapter 4 introduces transistor level implementation of proposed PLL system. Chapter 5

presents the measurement results and comparison of performances. Finally, the conclusions are drawn in chapter 6.

CHAPTER 2

BACKGROUND

In designing integrated wireless transceiver, the frequency synthesizer is a major design challenge. It has to satisfy stringent and conflicting requirements, which have enough rejection from the unwanted signals. One of the main drawbacks of integer-N architecture is the spurious tones caused by the reference frequency through the phase frequency detector (PFD) and charge pump (CP). Specially, in narrow band communication systems, the spurious tones occur at other channel bands and may downconvert the adjacent channels into the desired channel. If the reference frequency is smaller than the channel bandwidth, the spurious tone of the reference frequency downconverts within the desired signal. The spurious tones degrade the bit error rate (BER) in the receiver chain. In designing the frequency synthesizer, narrow loop bandwidth can improve the reference spur rejection. However, narrow loop bandwidth causes slow settling time.

2.1 PHASE NOISE

The most critical specification for any oscillator is its spectral purity. The output spectrum of an ideal oscillator is an impulse at ω_0, as shown in Fig. 2.1.

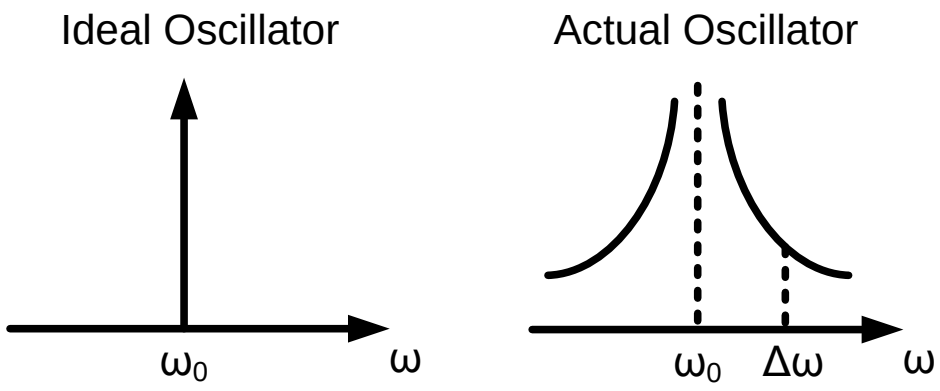


Figure 2.1 The output spectrum of an ideal oscillator and actual oscillator.

An ideal oscillator can be described as a pure sine wave in time domain,

$$V(t) = V_0 \sin(\omega_0 t) \tag{2.1}$$

where, V_0 and ω_0 are nominal amplitude and nominal frequency and $\Delta\omega$ is offset frequency from ω_0.

However, in any practical oscillator, the spectrum has power distributed around the center frequency (ω_0) as shown in Fig. 2.1. This leads to the noise sidebands on either side of ω_0. The instantaneous output of a practical oscillator be represented by

$$V(t) = V_0[1 + A(t)]\sin(\omega_0 t + \phi(t)) \tag{2.2}$$

where $A(t)$ and $\Phi(t)$ represent amplitude modulation (AM) noise and phase amplitude (PM) noise. Since oscillators typically run with fully saturated mode resulting in extreme compression of the AM noise, AM noise is negligible relative to PM noise. Therefore, the phase noise dominates the noise power spectrum of an oscillator.

By taking the Fourier transform of *V(t)*, we represent the power spectrum of *V(t)* in the frequency domain. The power spectrum is measured by the power dissipated in a specified load resistor as a function of frequency. When the noise is ignored, normalized carrier power is described by

$$P_C(f) = \frac{V_C^2}{2} \quad (watts) \tag{2.3}$$

When the power spectrum is normalized to unity the power spectral density, this is express as:

$$\int_{-\infty}^{\infty} P_n(f)df = 1 \quad (watt) \tag{2.4}$$

The power spectrum from a spectrum analyzer is able to determine what portion of the noise power at the offset frequencies is a result of phase noise or amplitude noise. This method is, we called, direct spectrum measurement in the frequency domain. This method involves measuring the PSD of the single where phase noise is represented in the sideband power on either side of the carrier. The offset frequency, Δf, is the frequency difference between a specified spectral component and the fundamental carrier frequency f_0. Phase noise is extracted by measuring the sideband spectral density, $S_v(f_0 \pm \Delta f)$ at a given frequency offset. $S_v(f_0 \pm \Delta f)$ is defined the PSD of the voltage fluctuations and measured in Watts/Hz and includes both amplitude and phase noise. If AM noise is negligible related to PM noise, $S_v(f_0 \pm \Delta f)$ can measure the phase fluctuations of a signal.

As mentioned before, the power spectrum has two independent components. One is the spectral density of phase fluctuations $S_\Phi(\Delta f)$ and the other

is the power spectral density of amplitude fluctuations $S_v(\Delta f)$. These two quantities are clarified in [5].

$$S_{\phi}(\Delta f) = \frac{\phi_{rms}^2(\Delta f)}{BW} \quad (rad^2/Hz) \tag{2.5}$$

$$S_{v}(\Delta f) = \frac{\varepsilon_{rms}^2(\Delta f)}{V^2 \cdot BW} \quad (Hz^{-1}) \tag{2.6}$$

where $\Phi_{rms}(\Delta f)$ is the rms phase deviation and the $\varepsilon_{rms}(\Delta f)$ rms voltage amplitude deviation measured at an offset frequency Δf from the carrier frequency f_0 in a bandwidth BW. The RMS phase and amplitude error can be extracted by taking the inverse relations of equation (2.5) and (2.6).

$$\phi_{rms}^2(\Delta f) = \int_{\Delta f - BW/2}^{\Delta f + BW/2} S_{\phi}(f)df \tag{2.7}$$

$$\varepsilon_{rms}^2(\Delta f) = \int_{\Delta f - BW/2}^{\Delta f + BW/2} S_{v}(f)df \tag{2.8}$$

2.2 PHASE NOISE IN OSCILLATOR

Phase noise and jitter in the RO can arise from many sources, including supply noise, and coupling from other circuits and via the power supply. Moreover, each RO stage's phase error impacts also the switching time of the next stage, thus accumulating phase noise.

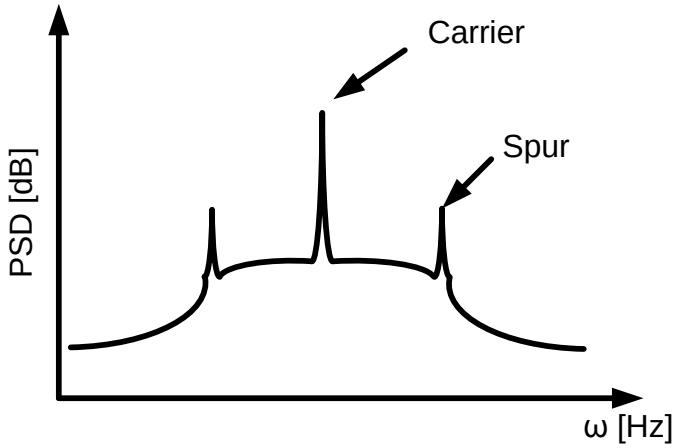


Figure 2.2 Power spectral density of oscillator output signal.

There are mainly two types of phase terms appearing at the output spectrum of oscillator. The first type appears as a distinct component in the spectrum, and it is referred to as a spurious tone or signal. The second type appears as random phase fluctuations, and it is referred to as phase noise as shown in Fig. 2.2. The phase noise in an oscillator is mainly due to internal noise sources such as thermal noise and active device noise source (flicker noise or 1/*f*, shot noise) [7]. They are random in nature. The internal noise sources set a fundamental limit for a minimum obtainable phase noise in oscillator design.

The spurious tones are due to external noise sources such as noise on control voltage, power supply, and bias current coupled clock signals. They are deterministic in nature. The spurious tones are not directly related to the oscillator but are important in the frequency synthesizer output and the PLL design specifications.

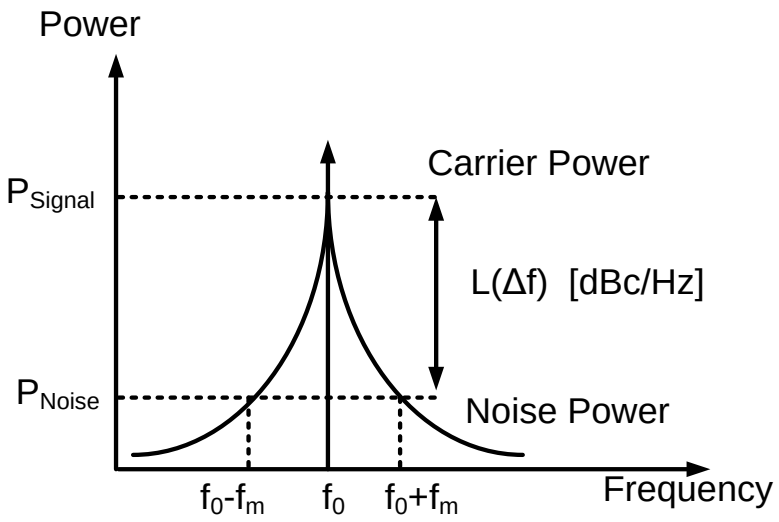


Figure 2.3 The power spectrum of an oscillator with phase noise.

As shown Fig. 2.3, the phase noise of an oscillator is typically quantified by the single-side band (SSB) phase noise, which is defined as the ratio of noise power in a 1 Hz bandwidth at an offset, Δf, to the signal power. Single-sideband (SSB) phase noise is specified in dBC/Hz at a given frequency offset, Δf, from the signal frequency f_0.

$$L(\Delta f) = 10\log\left(\frac{P_{Noise}(f_0 + \Delta f)}{P_{Signal}(f_0)}\right) \quad (dBc/Hz) \tag{2.9}$$

The equation (2.9) is also can be written as:

$$L(\Delta f) = 10\log\left(\frac{v^2_{n.rms}(f_0 + \Delta f)}{v^2_{c,rms}(f_0)}\right) \quad (dBc/Hz) \tag{2.10}$$

where $V_{n,rms}$ is the rms value of the sinusoid representing the phase noise sideband at the offset frequency Δf and $V_{c,rms}$ is rms value of the carrier signal.

Single sideband phase noise can be measured by phase modulation techniques [6].

A sinusoidal signal source *V(t)* with phase modulation can be expressed as:

$$V(t) = V_0 \cos(2\pi f_0 t + \phi(t)) \tag{2.11}$$

where V_0 is the peak voltage amplitude and $\Phi(t)$ is the phase modulation.

Equation (2.11) is expressed as:

$$V(t) = V_0 \cos(2\pi f_0 t + \frac{\Delta f}{f_m} \cos 2\pi f_m t) \tag{2.12}$$

where f_m is the modulation frequency and Δf is the peak frequency deviation.

In phase noise calculation, the noise power in the sidebands assumes very small relative to the carrier power. This assumption means that small phase deviation, $\Delta f/f_m << 1$, allows following approximations.

$$\cos(\frac{\Delta f}{f_m} \cos 2\pi f_m t) \approx 1 \tag{2.13}$$

$$\sin(\frac{\Delta f}{f_m} \cos 2\pi f_m t) \approx \frac{\Delta f}{f_m} \cos 2\pi f_m t \tag{2.14}$$

Therefore, equation (2.12) is extended as:

$$V(t) = V_0 \left[\cos(2\pi f_0 t) \cdot \cos(\frac{\Delta f}{f_m} \cos 2\pi f_m t) - \sin(2\pi f_0 t) \cdot \sin(\frac{\Delta f}{f_m} \cos 2\pi f_m t) \right]$$

$$\approx V_0 \left[\cos(2\pi f_0 t) - \sin(2\pi f_0 t) \cdot \frac{\Delta f}{f_m} \cos(2\pi f_m t) \right]$$

$$\approx V_0 \left\{ \cos(2\pi f_0 t) - \frac{\Delta f}{2 f_m} \left[\sin(2\pi (f_0 + f_m) t) - \sin(2\pi (f_0 - f_m) t) \right] \right\} \tag{2.15}$$

The above equation shows upper and lower sidebands of the carrier signal at amplitude of $\Delta f/2f_m$. Using equation (2.9), the phase noise, *L(f)*, is expressed as the power in a sideband of 1 Hz bandwidth relative to the carrier power:

$$
\begin{aligned}
L(f) &= 10\log\left(\frac{P_{Noise}}{P_{Signal}}\right) \\
&= 10\log\left(\frac{V_{Noise}}{V_{Signal}}\right)^2 \\
&= 10\log\left(\frac{\Delta f}{2 f_m}\right)^2 \\
&= 10\log\frac{1}{4}\left(\frac{\Delta f}{f_m}\right)^2
\end{aligned}
\tag{2.16}
$$

rms phase deviation, Δf_{rms}, is used from peak phase deviation $\Delta f_{rms} = \frac{\Delta f}{\sqrt{2}}$.

The equation (2.16) can be rewritten:

$$
L(f) = 10\log\frac{1}{2}\left(\frac{\Delta f_{rms}}{f_m}\right)^2 \tag{2.17}
$$

Since the sidebands are correlated the single sided spectral density of phase fluctuations is the sum of both sidebands. Therefore, the power spectral density of the phase fluctuations can be expressed as:

$$
\begin{aligned}
S_\phi(f) &= 10\log\frac{1}{2}\left(\frac{\Delta f}{f_m}\right)^2 \\
&= 10\log\left(\frac{\Delta f_{rms}}{f_m}\right)^2
\end{aligned}
\tag{2.18}
$$

Substituting (2.18) into (2.17) yields the relation between *L(f)* and $S_\Phi(f)$ as:

$$
L(f) = 10\log\left(\frac{S_\phi(f)}{2}\right) \tag{2.19}
$$

Above the approximations, *L(f)* could be expressed in rad^2/Hz and also be properly expressed in dBc/H when the assumption holds for $\Delta f/f_m << 1$. If phase

error is large enough, the spectral density of phase fluctuations is not a power spectral density.

2.3 METHOD OF MEASURING PHASE NOISE

All measurements of phase noise could be made at the carrier frequency of the source. Different techniques for measuring phase noise have been developed [9], [10]. We can categorize them into three major methods. There are direct measurement, phase detector measurement and delay line discriminator measurement.

2.3.1 Direct Measurement

If a synthesized signal source is multiplied by a high frequency reference signal, the phase noise sidebands are multiplied by the same factor as the frequency. In this case, direct RF spectrum measurements at the multiplied frequency are a good approximation of the phase noise sidebands. When corrected and normalized to the carrier power, the sidebands represent the phase noise of the signal, *L(f)*, described below equation:

$$L(f) = 10\log(\frac{S_v(f_0 + \Delta f)}{P_{Signal}})\ (dBc/Hz) \tag{2.20}$$

where P_{signal} represents the DUT signal power.

This straightforward method of phase noise measurement is typically used in spectrum analyzers. However, this method has limitations of equipments'

dynamic range, resolution, and LO phases noise. Moreover, the noise power of a DUT cannot distinguish a different from measuring amplitude noise and phase noise in direct measurement.

2.3.2 Phase Detector Measurement

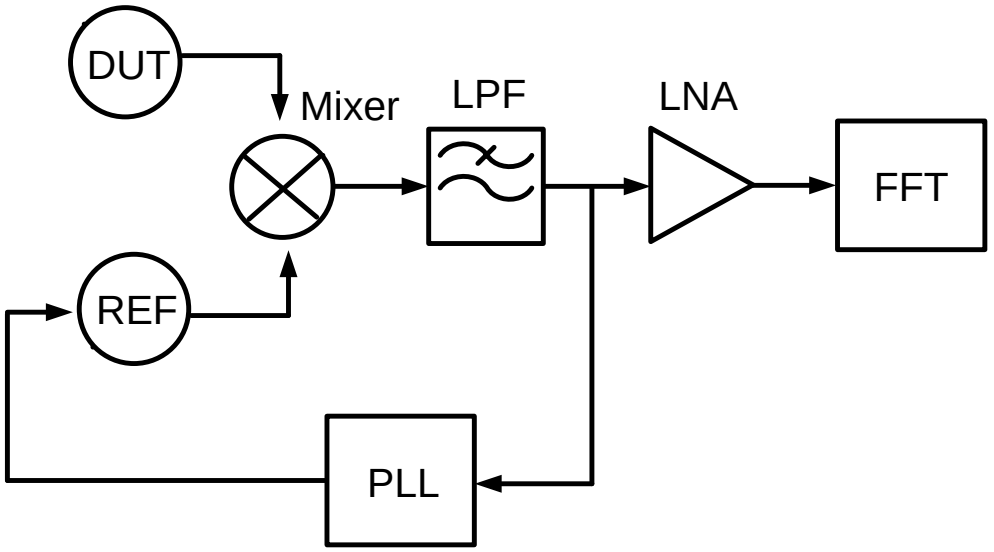


Figure 2.4 Basic diagram of phase detector method.

As shown in Fig. 2.4, one way to achieve better resolution is to convert the test signal down in frequency to the range of an analyzer with the desired IF bandwidth [11]. Double balanced mixer and a low pass filter is used in this method. A Fast Fourier Transform (FFT) analyzer or a spectrum analyzer measures the output of signal. The DUT source and the reference are used at identical frequencies. This method has disadvantage. Phase noise sidebands from

the reference frequency are down-converted by mixer. Therefore, the reference frequency has better phase noise performance than the DUT phase noise.

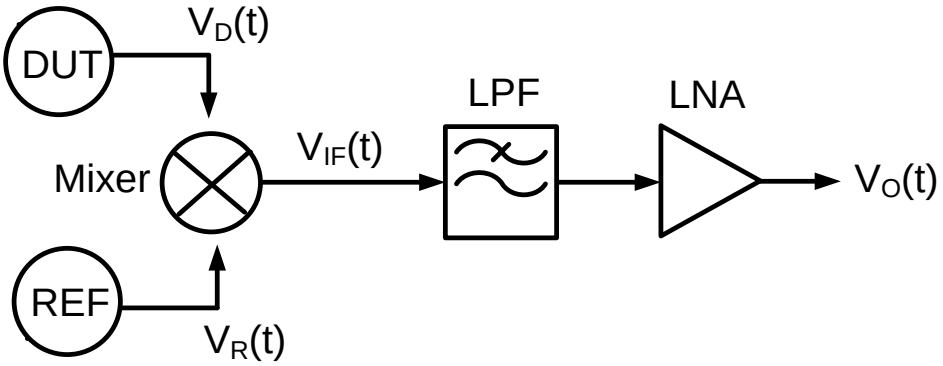


Figure 2.5 Operation of mixer as phase detector.

When two input signals defines the same frequency and have AM and PM noise, the $V_D(t)$ and $V_R(t)$ are expressed as:

$$V_D(t) = V_D[1 + A_D(t)]\sin(\omega_0 t + \phi_D(t)) \tag{2.20}$$

$$V_R(t) = V_R[1 + A_R(t)]\sin(\omega_0 t + \phi_R(t)) \tag{2.21}$$

where V_D and V_R are the AM noise free amplitude of signals and $A_D(t)$ and $A_R(t)$ are the AM noise components and $\Phi_D(t)$ and $\Phi_R(t)$ are the PM noise components.

The output of the mixer $V_{IF}(t)$ is the product of the two signals.

$$V_{IF}(t) = V_D V_R[1 + A_D(t)][1 + A_R(t)] \cdot \left[\cos(2\omega_0 t + \phi_D(t) + \phi_R(t)) + \cos(\phi_D(t) - \phi_R(t))\right] \tag{2.22}$$

The low pass filter will remove high frequency term at $2\omega_0 t$ and the output signal $V_O(t)$ is expressed as:

$$V_O(t) = V_D V_R [1 + A_D(t)][1 + A_R(t)] \cos(\phi_D(t) - \phi_R(t)) \tag{2.23}$$

Below equations, the output signal $V_O(t)$ can detect AM or PM noise depending on the phase difference of two signals.

$$V_O(t) = V_D V_R [1 + A_D(t)] \qquad when\ \phi_D(t) - \phi_R(t) = k\pi \tag{2.43}$$

$$\begin{aligned} V_O(t) &= V_D V_R \sin(\Delta\phi(t)) \approx V_D V_R \Delta\phi(t) \\ when\ \phi_D(t) - \phi_R(t) &= \Delta\phi(t) + \pi \cdot \frac{2k+1}{2} \end{aligned} \tag{2.44}$$

where k is an integer and assumes $\Delta\Phi(t) << 1$ and $\Delta\Phi(t)$ is instantaneous phase fluctuations. When the two input signals are in-phase, the output can detect AM noise. When the two signals are 90 degrees out of phase, the output can detect PM noise. To measure the phase noise, the phase difference of two input signal maintains 90 degrees out of phase.

Consider K_m that mixer conversion gain in volts/rad and two input signal of mixer are locked at quadrature. The mixer conversion gain is the slope of the mixer sine wave output at the zero crossings. The output of the mixer is expressed by:

$$\begin{aligned} V_O(t) &= V \cdot K_m \sin(\Delta\phi(t)) \\ &\approx V \cdot K_m \Delta\phi(t) \end{aligned} \tag{2.45}$$

This yields a direct linear relationship between the voltage fluctuations at the mixer output and the phase fluctuations of the input signals. The voltage output of the mixer as a function of frequency will be directly proportional to the input phase deviations. Taking the frequency transform to both sides of the above

equation, the power spectral density of the output signal is proportional to the *rms* sum of the phase noise contribution of the DUT and reference sources:

$$V_O(f) = V \cdot K_m \Delta\phi(f) = \sqrt{2} V_{rms} \Delta\phi(f) \tag{2.46}$$

$\Delta\Phi_{rms}(f)$ measured on the spectrum analyzer can be expressed as:

$$S_{\Delta\phi}(f) = \frac{\Delta\phi_{rms}^2}{Bandwidth} \quad (rad^2 / Hz) \tag{2.47}$$

$$S_{\Delta\phi}(f) = \Delta\phi_{rms}^2(f) = \frac{V_{O,rms}^2}{2V_{rms}^2} \tag{2.48}$$

Therefore, the phase noise of DUT signal can be expressed as:

$$L(f) = \frac{1}{2} S_{\Delta\phi}(f) = \frac{V_{O,rms}^2}{4V_{rms}^2} \tag{2.49}$$

The phase noise of the DUT can be calculated by measuring the power spectral density of the output voltage signal and then adjusting for the gain factor and error due to the phase noise of the reference signal. Using phase detector method, the phase quadrature is the point of maximum phase sensitivity and the region of the most linear operation. However, any small deviation from quadrature results in a measurement error.

2.3.3 Delay-line Frequency Discriminator Measurement

A noise source can distinguish amplitude noise and phase noise. Phase noise is defined as the noise generated from random fluctuations in the phase of a frequency source. Amplitude is defined as the noise generated from random fluctuations in the amplitude of a frequency source.

Advantage of a frequency discriminator is insensitive to amplitude noise when measuring phase noise. In addition, compared to phase detector method, the frequency discriminator method does not require a second reference signal phased locked to a DUT. These advantages provide to be able to measure high-level, low-rate phase noise or high close-in spurious sidebands, which can impose serious problems for phase detector method [12].

In order to understand the function of the delay line as a discriminator, Fig. 2.6 shows the process of differentiation implemented by a time-delay line.

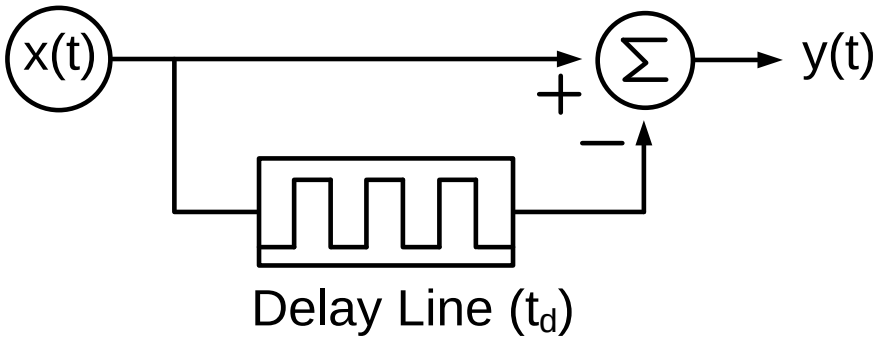


Figure 2.6 Discriminator implementation using time delay.

$$y(t) = x(t) - x(t - t_d) \tag{2.50}$$

Which can be written

$$\frac{y(t)}{t_d} = \frac{x(t) - x(t - t_d)}{t_d} \tag{2.51}$$

Since, by definition:

$$\lim_{t_d \to 0} \frac{y(t)}{t_d} = \lim_{t_d \to 0} \frac{x(t) - x(t - t_d)}{t_d} = \frac{dx(t)}{dt} \tag{2.52}$$

It follows that for small t_d

$$y(t) \approx t_d \frac{dx(t)}{dt} \tag{2.53}$$

Through the delay-line discriminator, the voltage fluctuations can be measured by the spectrum analyzer and converted phase noise units.

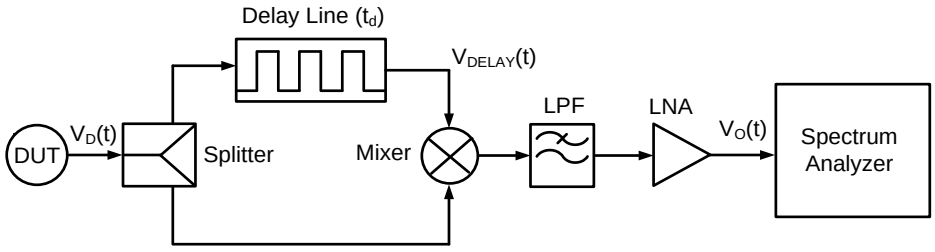


Figure 2.7 Block diagram of delay-line frequency discriminator system

As shown Fig. 2.7, the delay line and mixer implementation of a frequency discriminator converts frequency fluctuations into voltage fluctuations that can be measured by a baseband spectrum analyzer. The conversion is a two part process, first converting the frequency fluctuations into phase fluctuations, and then converting the phase fluctuations to voltage fluctuations. a delay line and mixer (i.e., delay-line discriminator) are used to convert instantaneous phase deviations of an oscillator to voltage deviations, enabling an on-chip phase noise measurement system with -124 dBc/Hz sensitivity. This technique does not

require a spectrally clean reference clock and can extract phase noise for a wide range of frequency offsets from carrier by using selective filters.

The frequency fluctuation to phase fluctuation transformation ($\Delta f \rightarrow \Delta \Phi$) takes place in the delay line. When the small frequency changes, the phase shift passed through the fixed delay (t_d) proportionally changes. The delay line converts the frequency change at the line input to a phase change at the line output when mixing with the un-delayed signal arriving at the mixer in the second path. The mixer transforms the phase fluctuations into voltage fluctuations ($\Delta \Phi \rightarrow \Delta V$). The voltage output is proportional to the input phase fluctuations.

The output of DUT is described by:

$$V_D(t) = V_D \cos(2\pi f_0 t + \frac{\Delta f}{f_m} \cos 2\pi f_m t) \qquad (2.54)$$

Where Δf is frequency fluctuation and f_m is frequency offset from the carrier.

The frequency fluctuation to phase fluctuation transformation takes place in the delay line. The output signal of the delay line is shown in equation 2.54.

$$V_{DELAY}(t) = V_D \cos(2\pi f_0 (t - t_d) + \frac{\Delta f}{f_m} \cos 2\pi f_m (t - t_d)) \quad \text{where } t_d \text{ is delay} \quad (2.55)$$

The frequency arrives at the mixer at a particular phase. As the frequency changes slightly, the phase shift incurred in the fixed delay time will change proportionally. The delay line converts the frequency changes at the line input to a phase change at the line output when compared to the un-delayed signal arriving at the mixer.

After mixing the two signals, the output is the multiplied form of the two signals. Passing through a low pass filter, the high frequency term is removed and the output is expressed as:

$$V_O(t) = V_D^2 K_{mix} G \cos(2\pi f_0 (t - t_d) + \frac{\Delta f}{f_m} \cos 2\pi f_m (t - t_d)) \cos(2\pi f_0 t + \frac{\Delta f}{f_m} \cos 2\pi f_m t) \tag{2.56}$$

where K_{mix} is the mixer gain and G is the LNA gain.

When the two signals adjust the quadrature and small phase deviation assumes $\Delta f/f_m << 1$, equation 2.56 can be derived as:

$$\begin{aligned}
V_O(t) &= V_D^2 K_{mix} G \cos(2\pi f_0 (t - t_d) + \frac{\Delta f}{f_m} \cos 2\pi f_m (t - t_d)) \cos(2\pi f_0 t + \frac{\Delta f}{f_m} \cos 2\pi f_m t) \\
&\approx V_D^2 K_{mix} G \cos(2\pi f_0 t_d - \frac{\Delta f}{f_m} \cos 2\pi f_m (t - t_d) + \frac{\Delta f}{f_m} \cos 2\pi f_m t) \\
&= V_D^2 K_{mix} G \begin{bmatrix} \cos 2\pi f_0 t_d \cos(-\frac{\Delta f}{f_m} \cos 2\pi f_m (t - t_d) + \frac{\Delta f}{f_m} \cos 2\pi f_m t)) \\ -\sin 2\pi f_0 t_d \sin(-\frac{\Delta f}{f_m} \cos 2\pi f_m (t - t_d) + \frac{\Delta f}{f_m} \cos 2\pi f_m t)) \end{bmatrix} \\
&\approx V_D^2 K_{mix} G \sin(\frac{\Delta f}{f_m} \cos 2\pi f_m t - \frac{\Delta f}{f_m} \cos 2\pi f_m (t - t_d)) \\
&= V_D^2 K_{mix} G \sin\left(t_d \frac{\frac{\Delta f}{f_m} \cos 2\pi f_m t}{dt} \right) \\
&= K_\phi \Delta f \sin(2\pi f_m t) \qquad \text{where } K_\phi = V_D^2 K_{mix} G 2\pi t_d
\end{aligned} \tag{2.57}$$

The voltage fluctuations can be measured by a baseband spectrum analyzer and converted to phase noise units. The output signal power can be expressed in mean square value of $V_o(t)$ as follows:

$$V_{o,rms}^2(t) = K_\phi^2 \Delta f_{rms}^2(t) \tag{2.58}$$

After transforming the frequency domain, the power spectral density of the frequency noise is below:

$$\begin{aligned} V_{o,rms}^2(f) &= K_\phi^2 \Delta f_{rms}^2(f) \\ &= K_\phi^2 2f^2 \frac{\Delta f_{rms}^2(f)}{2f^2} \\ &= K_\phi^2 2f^2 L(f) \end{aligned} \tag{2.59}$$

The power spectral density of the phase noise is described as:

$$L(f) = \frac{V_{o,rms}^2(f)}{2f^2 K_\phi^2} \tag{2.60}$$

The phase noise of DUT can be measured at a given offset frequency (*f*). The sensitivity of frequency discriminator is related with discriminator constant K_Φ. To get high sensitivity, the delay line should be longer and keep quadrature signals to make high mixer constant (K_{mix}).

2.4 PHASE LOCKED LOOP (PLL)

The basic block diagram of a PLL is shown in Fig. 2.8

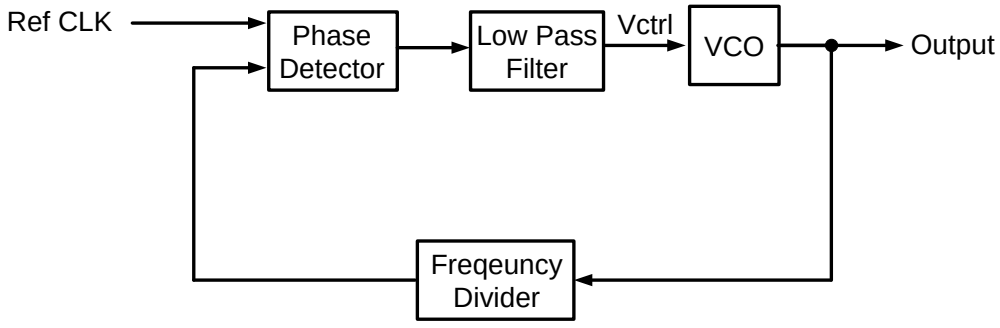


Figure 2.8 Basic block diagram of a PLL.

PLL is a feedback system that maintains a defined phase relationship between its input and output. In general, a PLL consists of a phase detector, a low pass filter, and oscillator, and a frequency divider. The phase detector compares the input phase with the divider output phase and produces the phase error in Fig. 2.8, which is an error signal that is proportional to the phase difference between the output of reference clock and divider. The phase error is then filtered by the low-pass filter to eliminate its high-frequency components and produce the Vctrl. The output frequency of the VCO is proportional to the VCO is proportional to the Vctrl. Therefore, the VCO frequency is updated as the phase error signal changes in the loop. The frequency divider divides the PLL output frequency to a lower frequency in the range of the input clock. The divider is needed in systems where the output clock frequency is much higher than the input clock frequency, for example, in clock generation and frequency-synthesis applications. The system tries to align the inputs to the phase detector and to produce an output clock synchronized to the input reference clock. The output frequency in a PLL with a divider is equal to the input frequency multiplied by the division ratio.

2.4.1 Charge Pump PLL

PLL with charge pump phase comparators are widely used in wireless applications. Charge pump PLL has advantage of no false locking problems, and the input and output are exactly in phase when the PLL is in lock. In addition, the static phase error is zero if mismatches and offsets of charge pump are negligible.

The charge-pump PLL is analyzed in many published papers [13], [14]. The schematic block diagram of a PLL is shown in Fig 2.9.

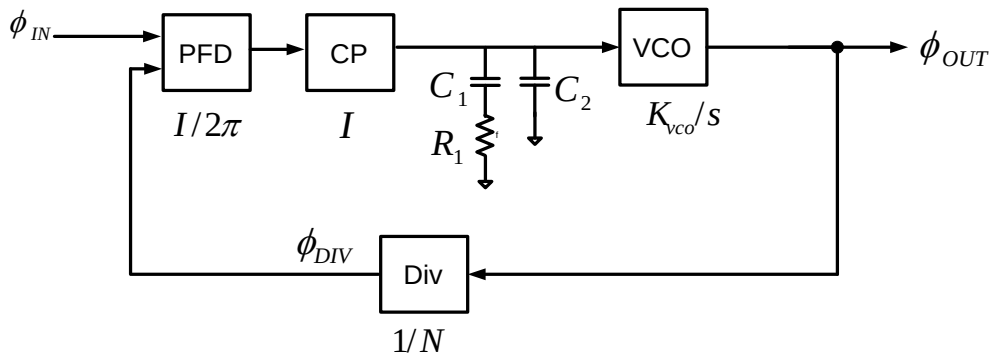


Figure 2.9 Basic block diagram of charge pump PLL.

It consists of four basic functional blocks. First, the voltage-controlled oscillator (VCO) runs at its natural frequency assuming the control voltage is arbitrary at the beginning. The PFD compares the phase difference between the reference signal Φ_{IN} and the VCO output divided by the frequency divider, Φ_{DIV}. The output of the PFD is a series of pulses whose duty cycle is proportional to the phase difference Φ_{IN} - Φ_{DIV}. The CP converts the voltage pulses into current pulses with pre-determined amplitude I. The loop converts the current pulses into a low-pass filtered voltage signal that controls the frequency of the VCO. If the feedback is negative, the error between Φ_{IN} and Φ_{DIV} gradually become smaller and smaller until $\Phi_{IN} = \Phi_{DIV}$. In this state the loop is referred to be locked. Once the loop is locked, the frequency of the VCO output is equal to the frequency of the reference multiplied by the feedback factor N.

The process of locking is not instantaneous because the loop has a limited bandwidth. The transfer function of the loop has to be studied to estimate the behavior of the loop during its transient operation. Since the operation of the PFD and CP is performed in the discrete-time domain, the complete transfer function becomes complicated due to the z-transform representation. A more intuitive equation can be obtained by assuming the phase error is small. With this assumption, the PFD and CP are modeled as simple gain blocks, $1/2\pi$ and I respectively, as shown in Fig. 2.9. During the initial transient, PLL goes into non-linear operating region as the VCO tries to find the correct frequency. As soon as the loop is in the locked condition, the small-signal linearized model can be used. The charge pump output is filtered by the low-pass filter and generates a control voltage for the VCO. The filter output varies the output frequency of the VCO. Because phase is the integral of frequency, the S-domain transfer function for VCO is K_{VCO}/s. the divider in feedback path divides the VCO output frequency by N and has a transfer function of $1/N$.

The linear approximation gives two critical equations useful for the initial design of a PLL. The first equation is an open-loop transfer function which is Φ_{OUT}/Φ_{IN} assuming the loop is opened between the frequency divider and the PFD.

$$H_{open}(s) = \frac{\Phi_{OUT}}{\Phi_{IN}} = \frac{K_D K_{vco}(1+s/\omega_z)}{(1+s/\omega_p)s^2} \tag{2.61}$$

where KD=I/(2πC$_1$N), ω_z=1/(R$_1$C$_1$) and ω_p=1/(R$_1$C$_2$). The open-loop transfer function is important because its phase margin indicates how stable the system will be after the loop is closed. Note that there are two poles at the origin and a stabilizing zero is required to compensate for them.

The second equation is a closed-loop transfer function Φ_{OUT}/Φ_{IN}. It can be also calculated from $H_{open}(s)/(1+H_{open}(s))$.

$$H_{close}(s)=\frac{\Phi_{OUT}}{\Phi_{IN}} =\frac{1+s/\omega_z}{1+s/\omega_z+s^2/(K_D K_{vco})+s^3/(\omega_p K_D K_{vco})} \tag{2.63}$$

For simplicity, it is assumed that ω_p is placed at very high frequency with respect to the natural frequency, $\omega_n=\sqrt{K_D K_{vco}}$,then the transfer function becomes second order.

$$H_{close}(s)\approx\frac{1+s/\omega_z}{1+s/\omega_z+s^2/(K_D K_{vco})} \tag{2.64}$$

The step response of the closed-loop transfer function shows the locking transient, and settling time performance can be determined from the transient waveform.

2.4.2 Phase Noise in PLL

The phase errors in electronic system fall into two categories of random variations and systematic variations. Thermal noise and 1/f noise in the active and passive devices in a circuit are the main sources of random variations. The phase error due to the supply and substrate noise in the circuit components is the main

source of systematic variations. Power supply or substrate results from the switching operations of clock generating system. In addition, the reference clock in a PLL contributes the systematic variations. In the frequency domain, these interfering signals represent spurious tones in the oscillator spectrum.

In frequency synthesizer, phase noise and spurious tones has negative effect on the signal purity. Phase noise associates with physical devices in PFD, loop-filter, VCO and frequency divider and degrades the synthesized signal from pure sine wave. Spurious tones are relatively high-energy. It appears at multiples of the comparison frequency. Usually, spurs are caused by either a leakage or a charge pump mismatch. Depending on their cause, reference spurs have differently when the offset frequency or the loop filter is changed.

The VCO noise is the contributor of the synthesizer out-of-band noise. All other noise sources such as PFD, CP, divider, and loop filter are the contributor of the in-band noise. The in-band noise transfer function has a lowpass characteristic. At high offset frequencies, this noise is suppressed by the lowpass filter. As a result, the noise coming from the PFD, CP, divider, and loop filter contributes to the in-band noise at the output of the PLL. On the other hand, the VCO noise transfer function is different and has a high pass characteristic. At low offset inside the loop bandwidth, the VCO noise is suppressed by highpass filter. As a result, the VCO noise contributes to the out-band noise at the output of the PLL.

2.4.3 PLL Phase Noise Analysis

Phase noise of a VCO placed inside a PLL is shaped by PLL noise transfer functions. A free running VCO phase noise is will be called as simply VCO phase noise, and phase noise of a VCO locked inside PLL lock will called PLL output phase noise.

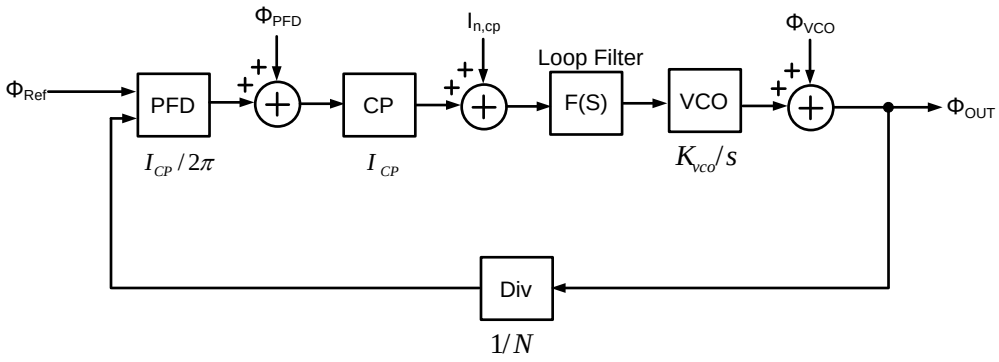


Figure 2.10 Phase noise model

A linear phase-domain model of a PLL with additive noise sources is shown in Fig 2.10. Φ_{Ref} represents the noise appearing on the reference input of PFD. It includes the crystal oscillator and crystal buffer noises. Φ_{PFD} is the phase of PFD. $I_{n,cp}$ is the noise of the CP current. Φ_{VCO} is the phase noise of the VCO. The transfer functions from these noise sources to the output can be written as:

$$\frac{\Phi_{OUT}}{\Phi_{Ref}} = \frac{G(S)}{1+G(S)H(S)} \tag{2.65}$$

$$\frac{\Phi_{OUT}}{\Phi_{PFD}} = \frac{G(S)}{1+G(S)H(S)} \tag{2.66}$$

$$\frac{\Phi_{OUT}}{I_{n,cp}} = \frac{2\pi}{I_{CP}} \frac{G(S)}{1+G(S)H(S)} \tag{2.67}$$

$$\frac{\Phi_{OUT}}{\Phi_{VCO}} = \frac{1}{1+G(S)H(S)} \tag{2.68}$$

The transfer functions, G(s) and H(s), are defined as:

$$G(S) = \frac{I_{CP}}{2\pi} \cdot F(S) \cdot \frac{2\pi K_{VCO}}{S} \tag{2.69}$$

$$H(S) = \frac{1}{N} \tag{2.70}$$

where I_{CP} is the CP current. K_{VCO} is the VCO gain. F(S) is the loop filter transfer function.

Analysis of the noise transfer function reveals more information about PLL noise shaping effect. The common factor for reference, divider, PFD and CP noise is

$$\frac{G(S)}{1+G(S)H(S)} \tag{2.71}$$

Noise sources experience different transfer functions to the output. For the noise present at the phase detector input, the transfer function is a low-pass filter. The noise is enhanced by the divider ratio in the pass-band and falls off beyond the PLL loop bandwidth. For the noise at the charge pump output, it is subject to a band-pass response where the pass-band of the band-pass transfer function depends on the pole/zero location of the loop filter.

The amplitude response of this common factor is shown in Fig 2.11. It exhibits low pass characteristics, and at low frequencies, the noise of the PLL is dominantly contributed by the reference, divider, PFD and CP noises. Also the noise contributions from references, divider, PFD and CP are increased by the feedback divider ratio N inside the loop bandwidth. The amplitude response of common factor, 1/[1+G(S)H(S)], for VCO is shown in Fig 2.11. It exhibits high pass filter behavior.

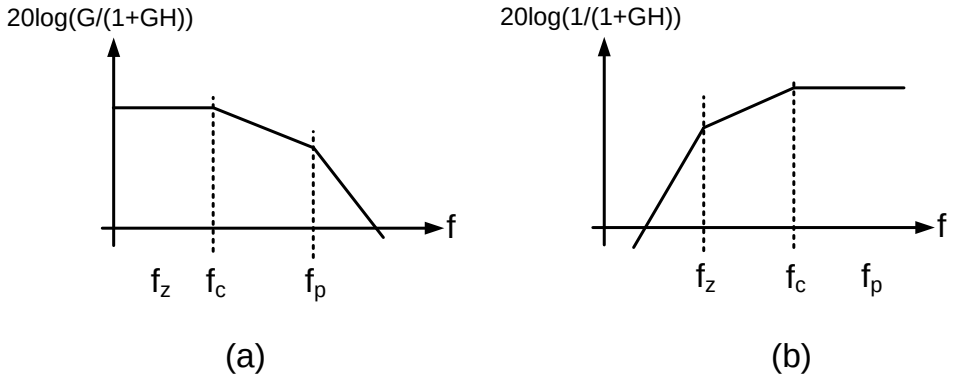


Figure 2.11 (a)Transfer function of reference, PFD, and CP noise (b) Transfer function of the VCO.

The PLL bandwidth determines the total PLL noise shape. For minimization residual phase error at the PLL output, the PLL bandwidth is chosen at the intersection of close-in noise and VCO noise as shown in Fig. 2.12 (a). Performance loss occurs if a non-optimum bandwidth is used as shown in Fig. 2.12 (b) and (c). Wide bandwidth loop filter has less attenuation for the noise

from the reference oscillator and suppresses more noise of the VCO, but the noise from the reference input and the other components (PFD, CP, and divider) are less suppressed. On the other hands, decreasing the loop bandwidth suppresses more noise from the reference clock, PFD, CP and divider, but the VCO noise is less suppressed. Therefore, there is a trade-off between the close-in phase noise and the loop bandwidth.

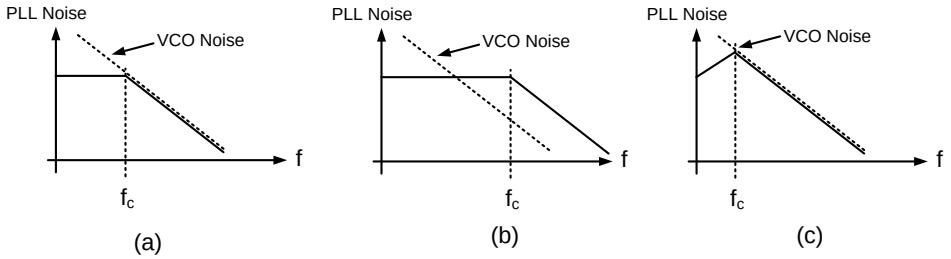


Figure 2.12 (a) Optimum PLL bandwidth (b) PLL bandwidth is too large (c) PLL bandwidth is too narrow.

A typical phase noise of a PLL is shown in figure 2.13. The phase noise behavior exhibits three different regions. The first phase noise region is the reference oscillator noise. The second region is called close-in noise, which is dominantly contributed by PFD, CP and divider noise. The third region beyond the loop bandwidth is practically the VCO noise. The first and third regions are primarily determined by the crystal and VCO. Usually the close-in phase noise has less impact than the VCO phase noise on the overall receiver performance. The PLL loop filter suppresses the close-in noise, but the far-out noise of the RO

VCO will not be filtered. The overall RO The phase error accumulation in the ring oscillators can be modeled as a phase error integrator with the power spectrual density of the phase integration represented as $1/f^2$.

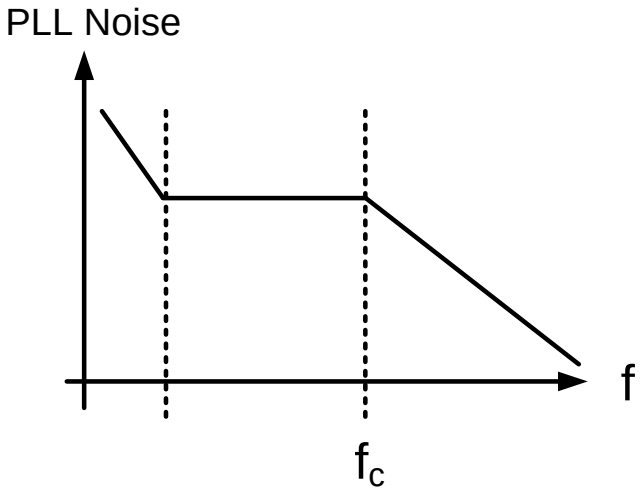


Figure 2.13 Typical PLL output phase noise.

CHAPTER 3

PROPOSE ADAPTIVE PHASE NOISE CANCELLATION PLL

The design of low phase noise frequency synthesizer requests in high-performance wireless communication system. The phase noise is determined by the noise coming from active devices, supply, ground and substrate. Due to ring oscillator (RO) supply sensitivity and poor phase noise performance, they have limited use in applications demanding low phase noise, such as wireless or optical transceivers. Recently, different approaches have been proposed to minimize RO PLL phase noise through cancellation techniques [15-18]. A current-steering DAC in parallel to the charge-pump is employed in [16] to cancel the ΣΔ modulator quantization noise in a fractional-*N* PLL. In [17], a dedicated supply regulator is used to attenuate RO supply noise at the cost of reduced voltage headroom and power efficiency. Open loop noise cancellation technique with negative supply compensation is explored in [18]. This chapter introduces the proposed adaptive phase noise cancellation PLL. A feed-forward, delay-discriminator based noise-cancelling architecture that improves phase noise characteristic of ring-oscillator based PLLs in an arbitrary bandwidth is presented. The proposed topology enables application of RO based PLL for highly sensitive frequency synthesizers that can be used for RF Transceivers, Optical communication, and data converters.

3.1 PROPOSE PLL ARCHITECTURE

The system level block diagram of the proposed PLL architecture is shown in Fig. 3.1.

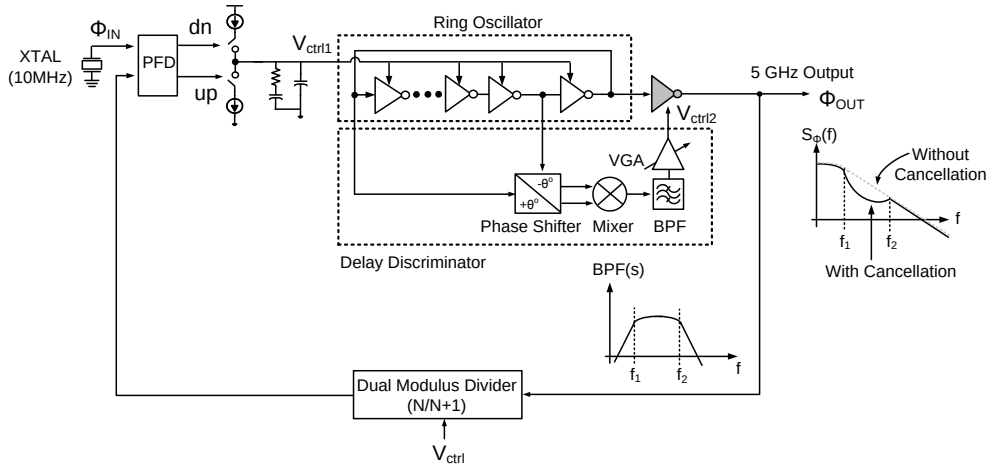


Figure 3.1 Block diagram of the delay-discriminator based feed-forward phase noise cancellation PLL.

Fig. 3.1 shows the block diagram of the proposed PLL with RO and adaptive feed-forward phase noise-cancelling architecture, which employs a delay-line discriminator for phase noise extraction. In [19], a delay line and mixer (i.e., delay-line discriminator) were used to convert instantaneous phase deviations of an oscillator to voltage deviations, enabling an on-chip phase noise measurement system with -124 dBc/Hz sensitivity. This technique does not require a spectrally clean reference clock and can extract phase noise for a wide range of frequency offsets from carrier by using selective filters. The proposed PLL utilizes a similar delay-line discriminator to extract RO's instantaneous

phase noise in a given bandwidth, and cancel it with a matched delay element. As shown in Fig. 3.1, the noise-cancelling loop consists of a polyphase filter, mixer, band-pass filter (BPF) and a variable gain amplifier (VGA). The proposed approach exploits the ring-oscillator architecture as a delay-line discriminator together with the mixer, converting phase fluctuations to a voltage signal.

A charge-pump phase comparator is followed by a loop filter, which produces the VCO control voltage. The PLL utilizes a *N*-stage ring oscillator and an analog phase detector (mixer) is used to extract the phase difference between (*N-1*) stages of the ring. The phase shifter maintains two signals within quadrature to get maximum mixer conversion gain. This signal is then high-passed to remove the static phase offset and feedback to the control the VCO control voltage of ring's *N-th* stage. In this way any jitter due to the *N-1* stages is corrected modulating the delay of the *N-th* stage. The output of the VCO is fed back to the input of PFD through a frequency divider. In proposed PLL architecture, the reference frequency is 10MHz and the output center frequency of the PLL is 5 GHz, resulting in the divider ration of 512.

3.2 PHASE NOISE IN VCO

When an oscillator is free running without noise, the output of the oscillator runs at its center frequency and zero-crossings would be uniformly spaced in time and phase also increases uniformly as shown in Fig 3.2.

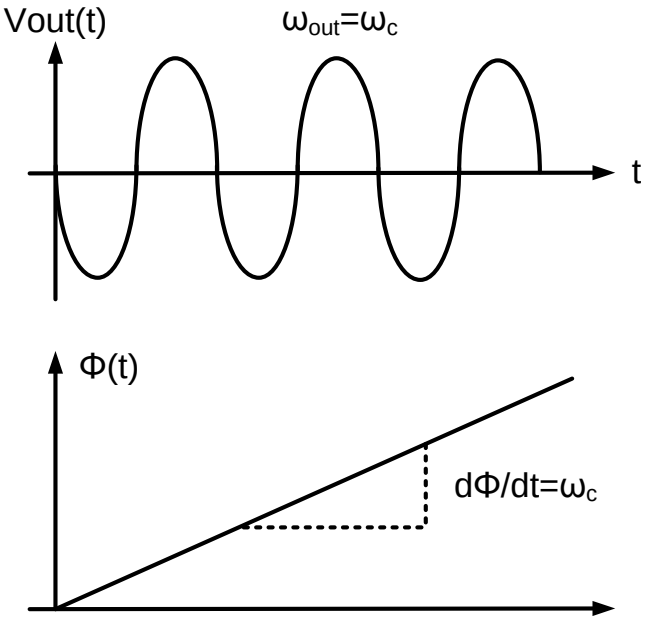


Figure 3.2 Ideal free running oscillator.

However, the oscillator with noise causes phase fluctuations which results non-uniformly spaced in time in the zero-crossing times as shown in Fig 3.3.

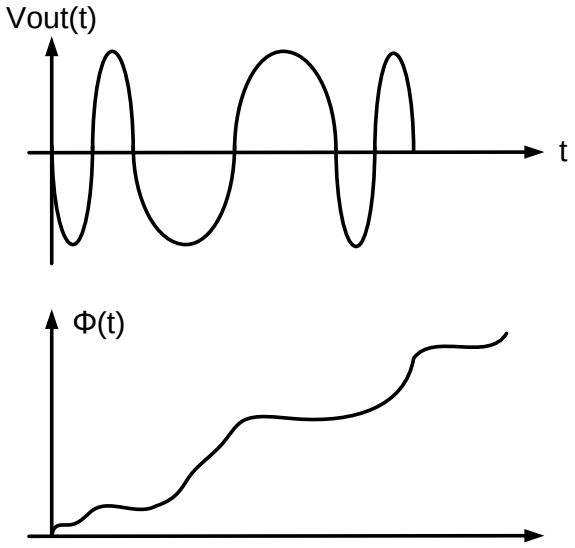


Figure 3.3 Free running oscillator with noise.

In a free-running RO, each variable delay cell exhibits random phase error due to active device noise and supply noise sources. The source of phase noise in each inverter device is from thermal and/or shot noise, and device non-linearity. The RO phase error consists of the phase noise for each inverter stage and the previous stage noise, which accumulates and impacting the overall VCO phase as shown in Fig. 3.4.

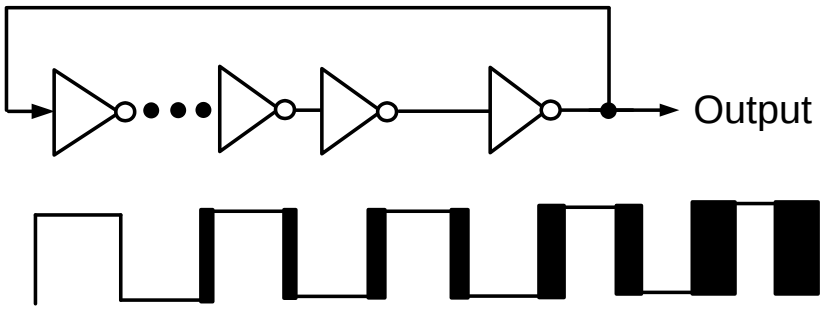


Figure 3.4 Free running oscillator.

Accumulating phase error in ring oscillator can model as a phase error integrator [20]. In frequency domain, the phase error accumulation is represented by the $1/f^2$ region of phase noise power spectral density as shown in Fig. 3.5.

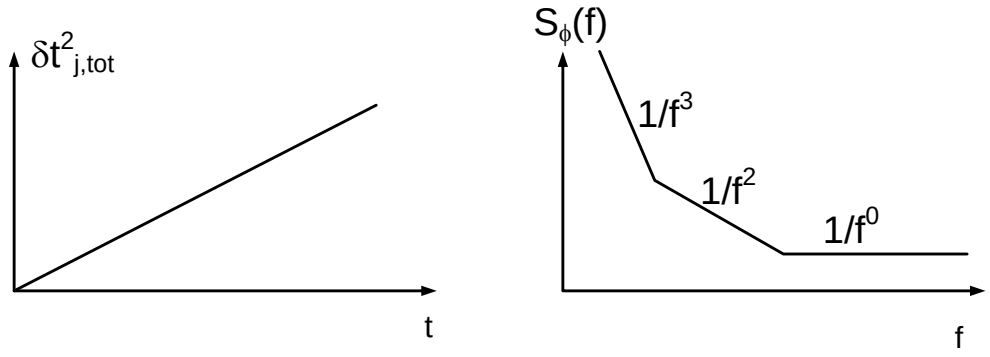


Figure 3.5 Jitter accumulation and phase noise in free-running RO.

In a phase-locked RO, the phase error accumulation is bounded by the PLL dynamics, and steady-state phase error is determined by the noise

characteristics of the reference frequency and phase/frequency detector, as shown in Fig. 3.6.

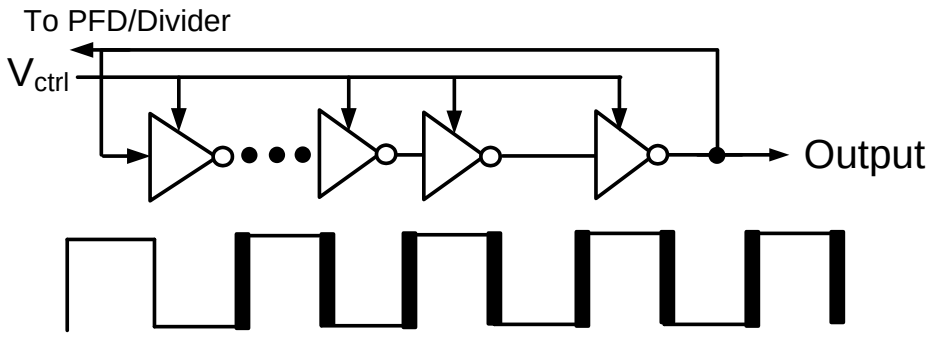


Figure 3.6 Ring oscillator in a PLL.

In frequency domain, the PLL phase noise is dominated by the RO's $1/f^2$ characteristic only at frequency offsets higher than PLL bandwidth as shown in Fig. 3.7.

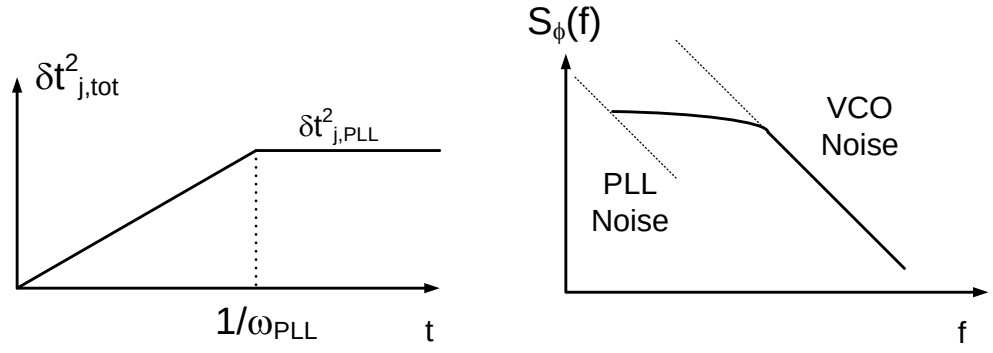


Figure 3.7 Jitter accumulation and phase noise in phase-locked RO.

For an *N*-stage RO, the mixing product of the output phase and output of the $(N\text{-}1)^{th}$ delay stage can be represented as

$$v_{mix}(t) = \sin(\omega t) \cdot \sin\left(\omega t + 2\pi \frac{N-1}{N} + \phi_n(t) \right) \approx \alpha \phi_n(t) \qquad (3.1)$$

Where $\phi_n(t)$ is the instantaneous phase deviation from its carrier and α is the mixer gain. The high frequency terms represent high order harmonics and far-out phase noise. In a closed loop PLL, the DC component of the tuning voltage and close-in phase noise are determined by the loop filter, and the loop gain suppresses low frequency deviations within the PLL bandwidth. Assuming the DC terms and higher harmonic component are filtered from the mixer output, the bandpass filtered output of the cancellation loop contains the phase noise information of the oscillator inside a desired bandwidth. In the proposed approach the extracted phase noise at the bandpass filter output is inverted and applied to the tuning port of an auxiliary delay stage to cancel instantaneous phase error outside the PLL loop bandwidth, as shown in Fig. 3.8.

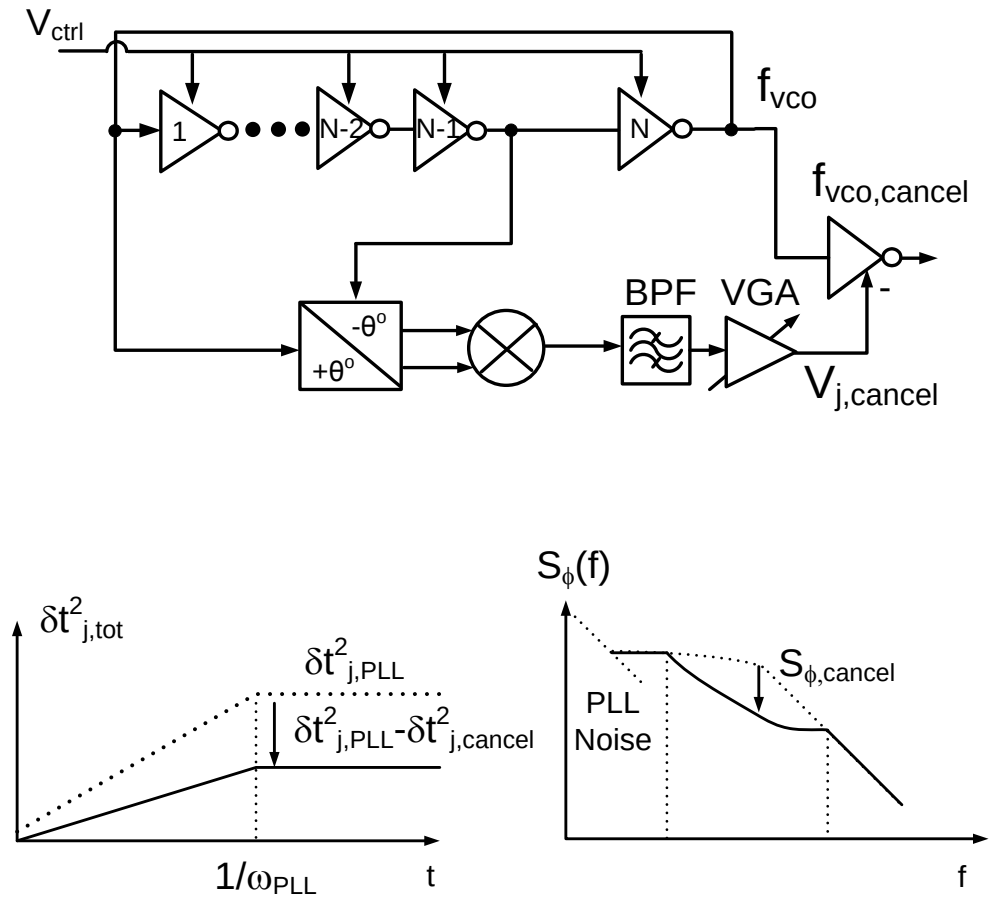


Figure 3.8 Jitter accumulation and phase noise in the proposed delay-discriminator based noise-cancellation architecture.

3.3 CANCELLATION LOOP NOISE ANALYSIS

The cancellation loop implements phase shifter, mixer, band pass filter and VGA. Voltage noise of cancellation loop contributes phase noise of ring oscillator by voltage gain constant (K_v). Therefore, cancellation loop noise floor is lower than phase noise of ring oscillator itself. This chapter will discuss the noise contribution of cancellation loop.

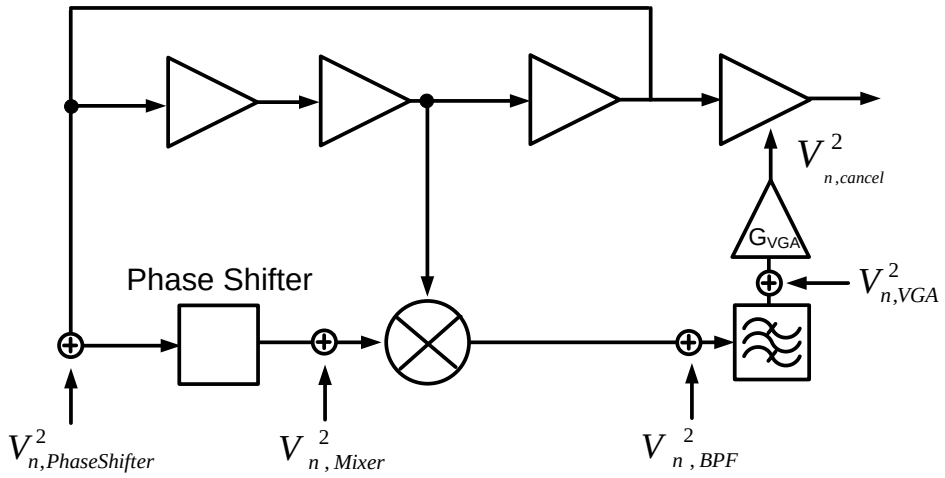


Figure 3.9 Noise model of cancellation loop.

The noise of cancellation loop is contributed by thermal noise and 1/f noise of phase shifter, mixer, BPF, and VGA as shown in Fig 3.9. The output referred noise power of cancellation loop, $V^2_{n,cancel}$,can be extracted by summing each noise source multiplied by each gain.

$$V^2_{n,cancel}(f) = G^2_{PS}G^2_{Mixer}G^2_{BPF}G^2_{VGA}v^2_{n,PS}(f) + G^2_{Mixer}G^2_{BPF}G^2_{VGA}v^2_{n,Mixer}(f) + G^2_{BPF}G^2_{VGA}v^2_{n,BPF}(f) + G^2_{VGA}v^2_{n,VGA}(f) \quad (3.2)$$

The phase noise in oscillator can increase due to noise of V_{cancel} node. The relationship phase noise and control voltage nose is described by

$$S_{OSC}(f) = (\frac{K_v}{3})^2 S_{cancel}(f) \quad \text{where } K_v \text{ is voltage gain constant} \quad (3.3)$$

The resulting cancellation loop noise $L_{OSC}(f)$ can be calculated as

$$L_{OSC}(f) = 10\log\left(\frac{\frac{K_v^2}{9}V_{n,cancel}^2(f)}{2(K_\phi f)^2}\right)$$
$$= 10\log\frac{K_v^2}{18K_\phi^2 f^2}\begin{pmatrix} G_{PS}^2 G_{Mixer}^2 G_{BPF}^2 G_{VGA}^2 v_{n,PS}^2(f) \\ + G_{Mixer}^2 G_{BPFr}^2 G_{VGA}^2 v_{n,Mixer}^2(f) \\ + G_{BPFr}^2 G_{VGA}^2 v_{n,BPF}^2(f) + G_{VGA}^2 v_{n,VGA}^2(f) \end{pmatrix} \quad (3.4)$$

where $K_\Phi = G_{PS}\, G_{Mixer}\, G_{BPF}\, G_{VGA}$ is overall system gain.

The higher gain reduces noise contribution of the cancellation loop as shown in equation 3.4. On the other hand, higher voltage gain introduces higher noise contribution of the cancellation loop.

To check the output referred noise of cancellation loop, the test set up performs as shown in Fig. 3.10.

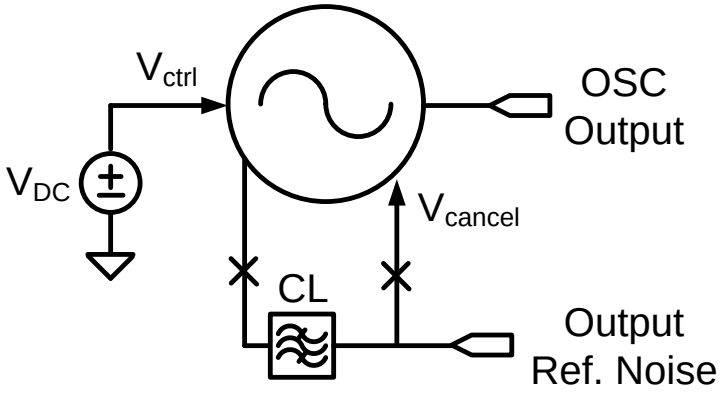


Figure 3.10 Test setup for the output referred noise of cancellation loop

The output referred noise of cancellation loop is about 140nV/sqrt(Hz) at 100 kHz as shown in Fig. 3.11

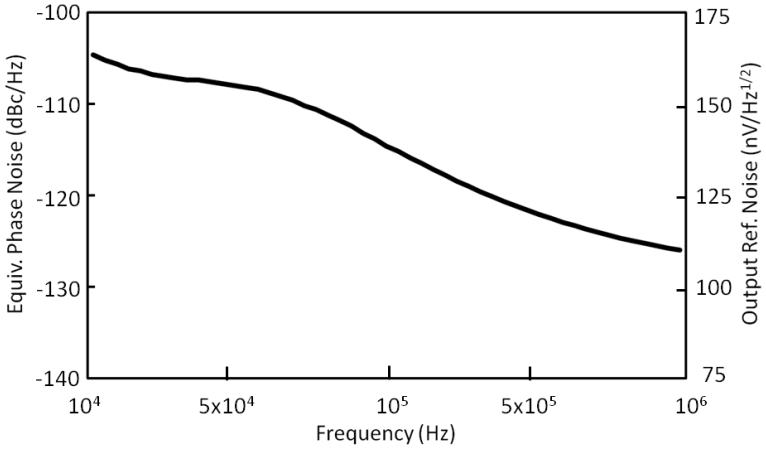


Figure 3.11 Output referred noise of the cancellation loop and equivalent phase noise contribution.

Next, the phase noise contribution from cancellation loop is verified by injecting the white noise to V_{cancel} node in oscillator as shown in Fig 3.12

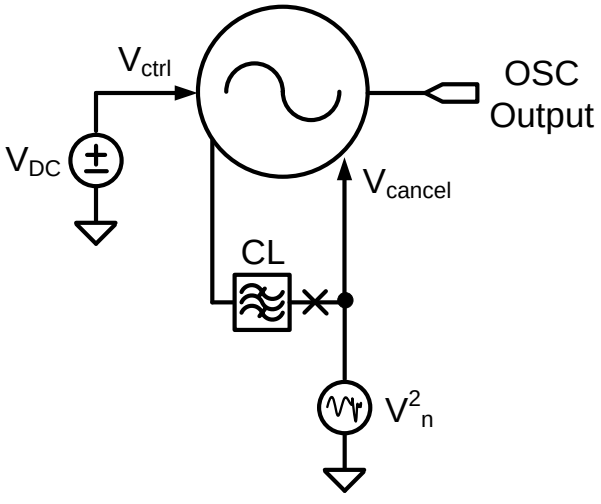


Figure 3.12 Test set up for cancellation loop noise to phase noise in oscillator.

In PSS noise simulation results, phase noise increases every 3dB by increasing 2uV/sqrt(Hz) injection white noise as shown in Fig 3.13.

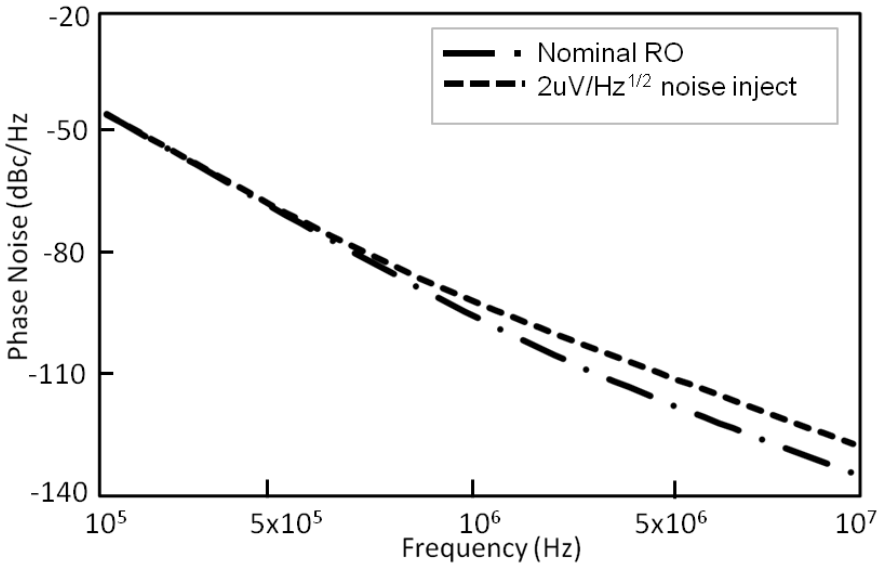


Figure 3.13 Phase noise of RO with free running and noise inject

The plot shows less than 2uV/sqrt(Hz) noise from cancellation loop is required to minimized on oscillator phase noise. In addition, the noise contribution from cancellation loop has minor impact on oscillator phase noise.

3.4 SMALL SIGNAL MODEL ANALYSIS

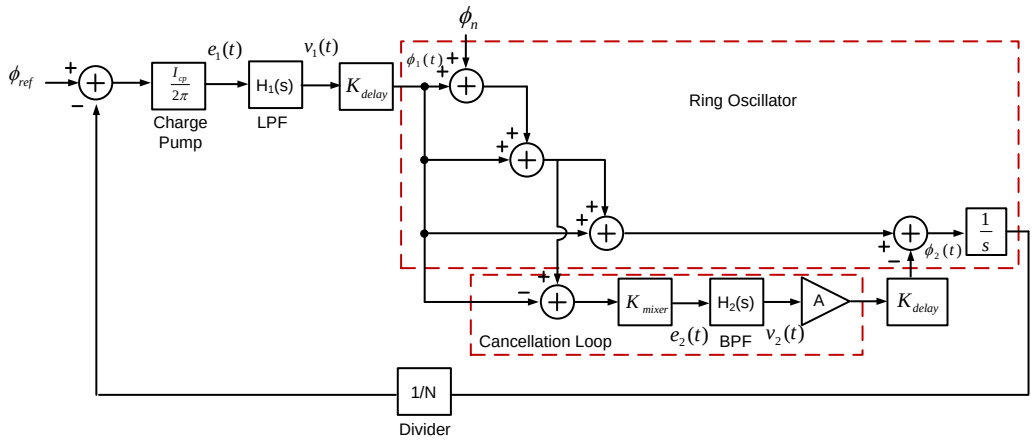


Figure 3.14 Adaptive noise cancellation PLL small signal model.

When the loop is in the locked condition, the small signal model can be used. Fig. 3.14 is a small signal AC model of each building block in adaptive noise cancellation PLL. The phase detector compares the phase difference between two inputs, and the charge pump converts the phase difference into a voltage signal. The charge pump output is filtered by the low pass filter and generates a control voltage for the VCO. The transfer function for the loop filter is $H_1(s)$, and the filter output varies the output frequency of the VCO. Because phase is the integral of frequency, the s domain transfer function for VCO is K_{delay}/S. the divider in the feedback path divides the VCO output frequency by N and has a transfer function of *1/N*. In cancellation loop, the mixer has phase detector constant K_{mixer}. Two signals from different stages in ring oscillator go through the mixer and detect the phase error. The transfer function for the BPF is $H_2(s)$, and it filters out the high frequency and DC term. So phase error information remains

after BPF. Voltage noise after BPF calibrates gain matching from VGA gain of A. After calibrating, the voltage noise injects to last stage of delay cell and transforms voltage to phase by K_{delay}.

Fig. 3.15shows the transfer function of output phase noise to VCO phase noise and represents as:

$$\frac{\Phi_{OUT}}{\Phi_{VCO}}(s) = \frac{(1 - K_D H_{BPF}(s)) \cdot s}{s + K_{PD} K_{VCO} H_{LPF}(s) \cdot \frac{1}{N}} \tag{3.5}$$

where K_D is discriminator gain and K_{VCO} is VCO gain.

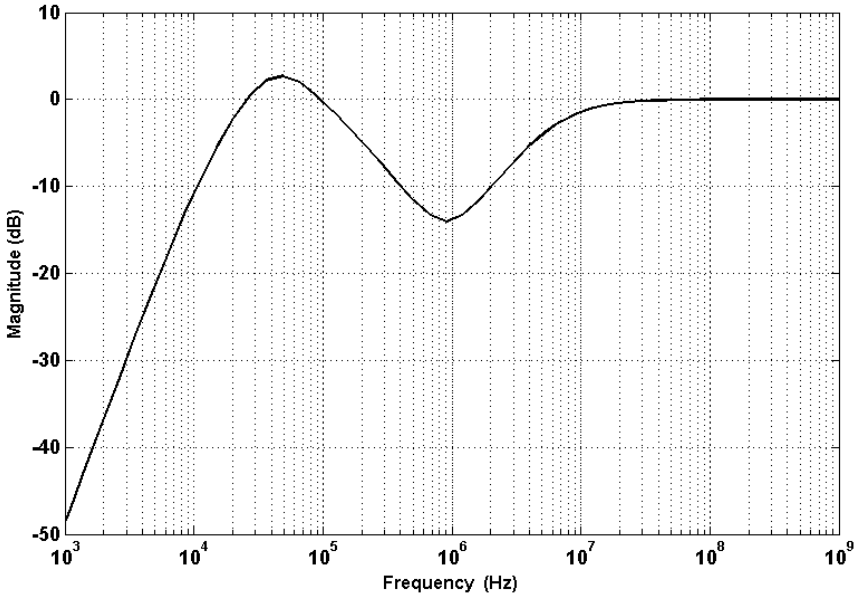


Figure 3.15 Transfer function of output phase noise to VCO phase noise.

Fig. 3.16 shows phase noise characteristic of with and without active noise cancellation loop in PLL. PLL has high pass filter characteristic for VCO phase

noise. Phase noise attenuates -20 dB/c per decade below PLL bandwidth. In addition, phase noise reduces by cancellation enabled in far-out PLL bandwidth.

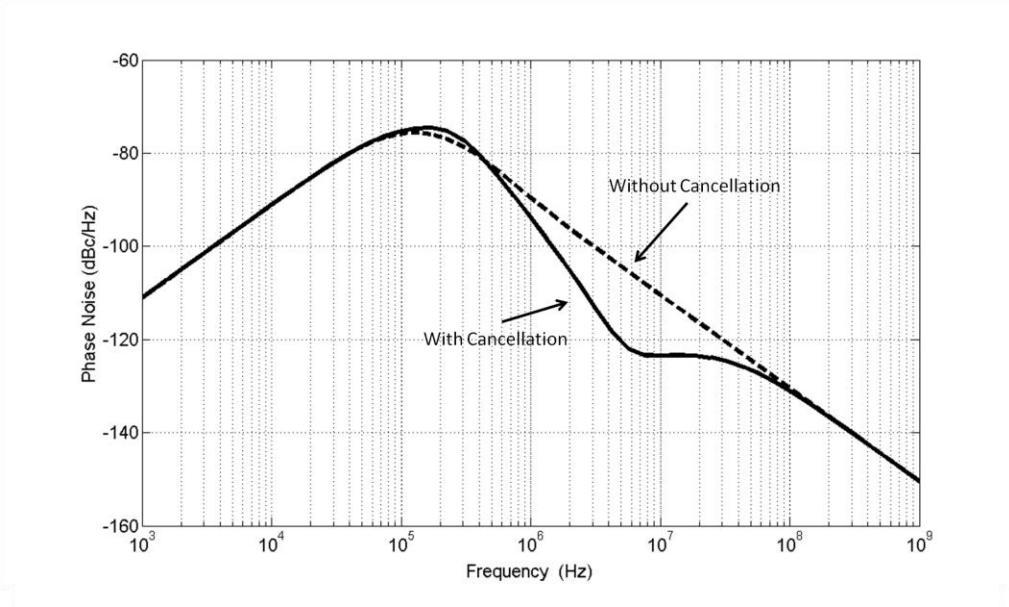


Figure 3.16 RO contribution to PLL phase noise *with and without* active noise cancellation enabled.

CHAPTER 4

CIRCUIT IMPLEMENTATIONS

The schematic of the proposed RO and delay-discriminator based noise-cancelling loop is shown in Fig. 4.1. Ring oscillator is implemented with 5 pseudo-differential variable delay inverter cells. The delay cells topology uses active inductors to compensate for parasitic capacitors' speed limitation. Although active inductors avoid the drawbacks of passive spiral inductors such as large die area and substrate noise coupling, they suffer from broadband noise generated due to active devices.

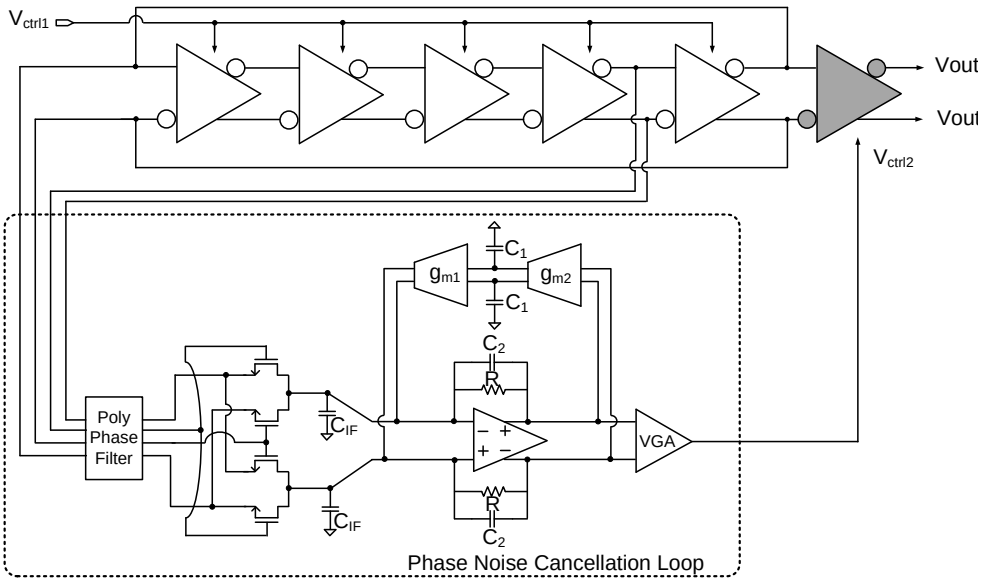


Figure 4.1 Schematics of ring oscillator delay cells with active inductors and feed-forward noise-cancelling loop.

A polyphase filter is used in the discriminator to maintain the phase difference of mixer input signals in quadrature. The quadrature configuration achieves maximum phase discriminator sensitivity and linearity. Fully differential double-balanced passive mixer with transimpedance amplifier (TIA) provides a first order low-pass filtering. Passive mixer operating in triode mode is selected guarantees high linearity and low flicker noise compared to active mixers. A two-stage TIA structure minimizes the input referred noise of the measurement chain. TIA with single RC pole determines the phase noise measurement bandwidth of LPF and rejects higher mixer harmonics.

The DC component of the discriminator output determines the steady-state frequency of the RO and should be filtered before being applied to the cancellation delay element. As shown in Fig. 4.1, a DC feedback path through gm1 and gm2 removes DC offset at the mixer output providing a high pass pole. The high-pass cut-off frequency of the BPF is controlled by changing transconductance g_{m1} and g_{m2}. The high-pass pole can be placed outside the PLL bandwidth to benefit from noise cancellation effect. An active-RC integrator is used to implement a high linearity low-pass filter. Finally, a current-steering fully differential VGA provides high linearity and wide gain tuning range to compensate for variations in the variable-delay cell tuning characteristics.

4.1 VOLTAGE CONTROL OSICLLATOR (VCO)

A voltage control oscillator is an oscillator whose frequency is controlled by a voltage or current. In general, LC and ring oscillators are widely used in

recent applications. The tuning range of LC oscillators is usually small, and process and temperature variations affect the output frequency to a great extent. LC oscillators also occupy a large area, which is needed for inductor. Therefore, the fabrication cost is high in comparison with ring oscillators. Ring oscillators are popular due to their low cost and wide tuning range. These oscillators are used in integrated circuit applications where their phase noise is small enough for the specific application.

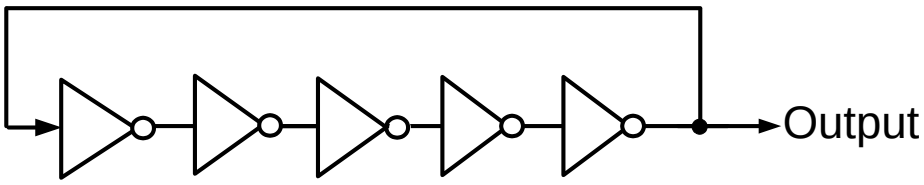


Figure 4.2 Ring oscillator with 5 stage delay cell.

Ring oscillators are realized by placing an odd number of inverters in a feedback loop, as shown in Fig. 4.2. The loop gain should be greater than unity when the phase shift around the loop is 180 degrees. This condition guarantees that the loop is unstable and oscillation occurs. Each half period, the signal is inverted by propagating around the loop once. The oscillation frequency is $f_{OSC} = \frac{1}{T_{OSC}} = \frac{1}{2N \cdot T_{delay}}$ where N is the number of inverters, and T_{delay} is delay of one inverter.

Controlled oscillators are realized by making the delay of the inverter programmable. This delay can be programmed by changing the inverter's current

or its supply voltage. A popular method for programming the VCO frequency in PLLs is converting the VCO control voltage to the current that changes the delay of the inverters.

For differential ring oscillator, the total power dissipation is given by:

$$P = NI_{dd}V_{dd} \tag{4.1}$$

Where N is the number of stages, I_{dd} is the total current of the differential pair, and V_{dd} is the supply voltage. The frequency of oscillation can be derived by:

$$f_{osc} = \frac{I_{dd}}{2NC_{tot}V_{swing}} \tag{4.2}$$

where C_{tot} is the total capacitance of load and V_{swing} is the maximum single-ended voltage swing at the output of each stage.

For differential ring oscillator using short-channel devices, one may derive the following lower bound on the signal-sideband phase noise in the $1/f^2$ region [21].

$$S_{\Phi}(f_m) = \left(\frac{f_0}{f_m}\right)^2 \cdot \left(\frac{F \cdot kT}{I_{dd}(V_{GS} - V_T)}\right) \tag{4.3}$$

where the offset frequency is denoted by f_m, the distance of the offset frequency from carrier. This equation shows that phase noise is related to the ration of the center frequency to the offset frequency squared, times a factor related to delay cell device design. *kT* in the numerator is the thermal noise factor, and is multiplied by the term *F*. This term is a simplified constant equal to the interstage gain times the noise contribution factor in silicon.

Phase noise is a strong function of power consumption in observation of the equation. Increasing the current consumption reduces the phase noise. For ring oscillator design, since the device sizes are scaled with the current, this implies an increase in area as well.

4.1.1 Ring Oscillator with Active Inductor Load

The design of the ring oscillator for 5GHz applications is especially challenging. The proposed noise-cancelling architecture can benefit speed-up from active inductors, without the noise penalty due to active cancellation. Inverter's topology uses active inductors to minimize parasitic capacitors' speed limitation in this project. The simplified schematic of the proposed inverter in shown in Fig 4.3.

Active inductors are realized by MOS active loads formed by Mn_1-Mn_2 and MOS variable resistors Mg_1-Mg_2. The impedance seen at Mn_1-Mn_2 sources shows an inductive behavior with inductance value determined by the equivalent resistance at Mn_1-Mn_2 gates. By adjusting Mg_1-Mg_2 variable resistors, the equivalent impedance at the inverter load is changed thus varying the stage delay and, ultimately, the RO's oscillation frequency. The implemented ring oscillator operates from 3.5GHz up to 7.1GHz.

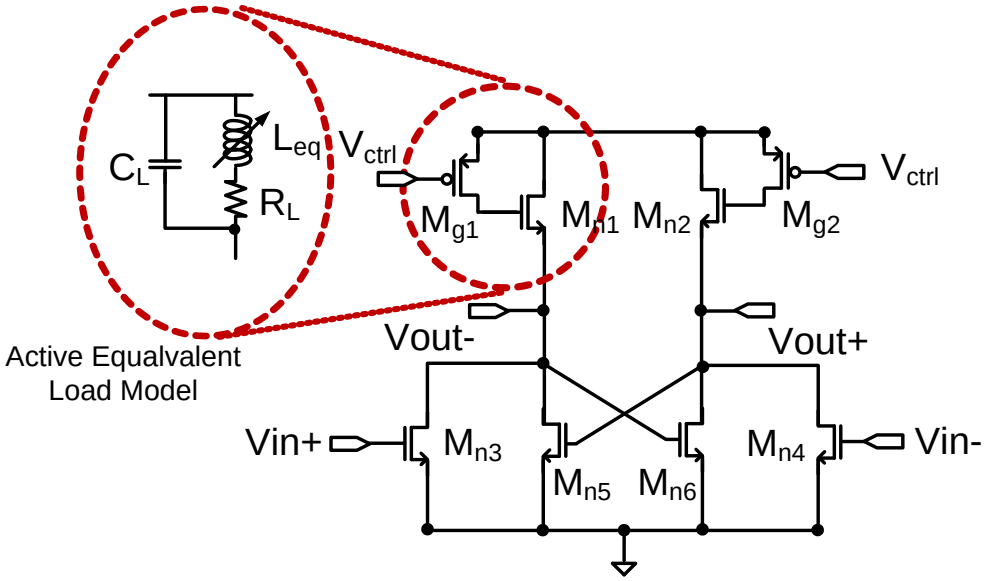


Figure 4.3 Ring oscillator delay cell with active inductors.

To avoid the drawbacks of passive spiral inductors including extremely area consuming, small inductance, and strong interaction with the substrate, active inductors can be used. The self-bias active inductor is applied in [22]. Using the first order analysis and neglecting Cgd, we obtain the impedance looking into the active inductor

$$Z(s) = \frac{1}{g_{m,Mn1\&2}} \frac{sR_{on,Mg1\&2}C_{gs,Mn1\&2} + 1}{s\dfrac{C_{gs,Mn1\&2}}{g_{m,Mn1\&2}} + 1} \tag{4.4}$$

The active inductor has a zero at $\omega_z = \dfrac{1}{R_{on}C_{gs}}$ and a pole at $\omega_p = \dfrac{g_m}{R_{on}C_{gs}}$. Also $\dfrac{\omega_p}{\omega_z} = R_{on}g_m$. The active inductor is resistive when $0 < \omega < \omega_z$, inductive when ω_z

$< \omega < \omega_p$ and resistive when $\omega > \omega_p$. The condition that the active inductor exhibits an inductive characteristic is $\omega_z < \omega_p$.

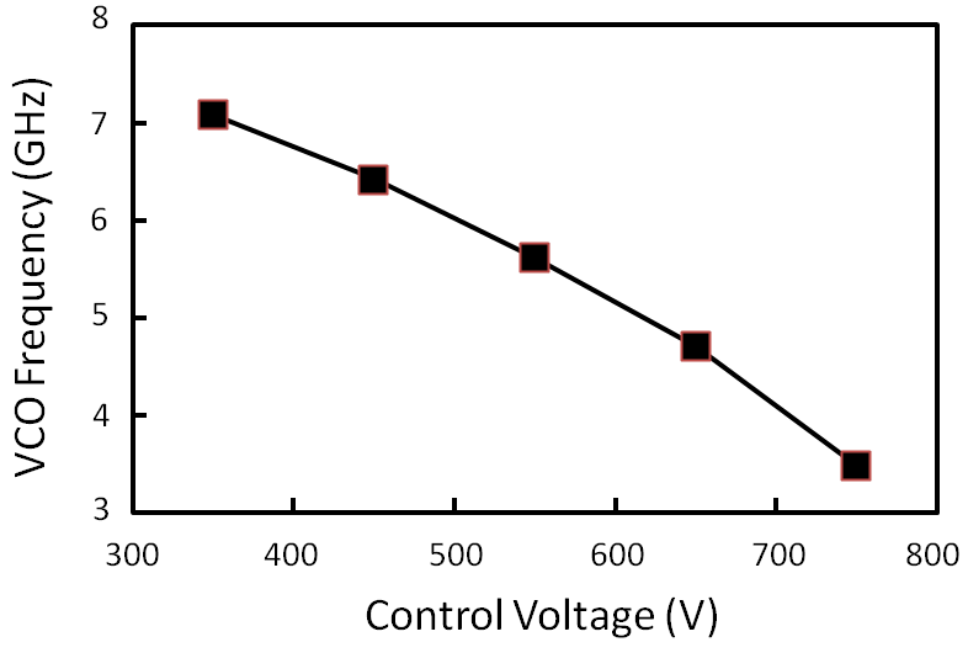


Figure 4.4. Frequency range respect to control voltage.

Fig. 4.4 represents the measurement result of ring oscillator with active inductor load. The frequency of oscillator operates up to 7.1GHz respect to control voltage from 350mV to 750mV. Oscillator voltage gain (K_v) is about 900MHz/V.

4.2 STATIC DC PHASE OFFSET CANCELER

There are several DC offset cancellation schemes established in recent papers [23-25]. In paper [23], the shunt capacitor is applied negative feedbakc to flow the mixer load. Utilizing baseband processor senses the DC offset and

controls the current to cancel the DC offset digitally [24]. Both DC offset cancellation schemes are not applied to passive mixer.

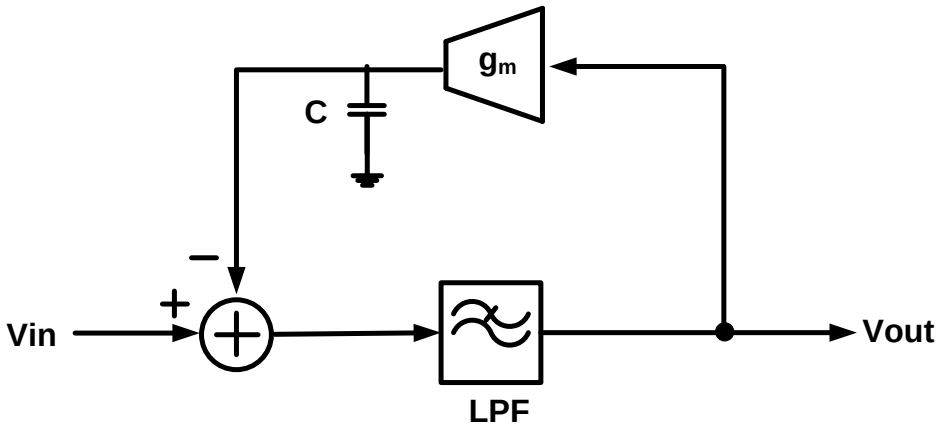


Figure 4.5 Static DC offset canceller.

To cancel the static DC phase offset, we have to cut out some portion of the spectrum around DC using high pass filtering. We adopt a DC feedback loop shown in Fig. 4.5 as a static DC offset canceller. A DC feedback loop creates a high pass pole at a frequency close to DC to remove a static DC offset. We could use an AC coupling capacitor or a high pass filter instead of a DC feedback loop to create a high pass pole. Also, we can easily control the high pass cutoff frequency with smaller capacitance values.

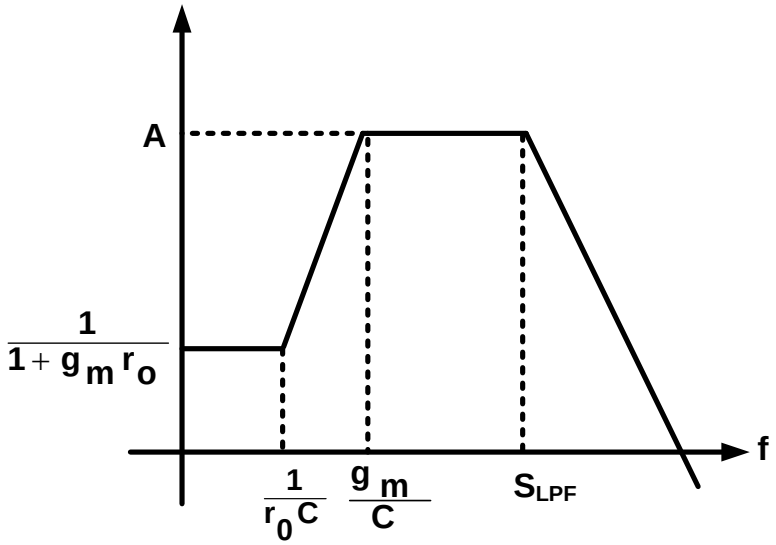


Figure 4.6 Frequency response of the static DC offset canceller.

The transfer function of the static DC offset canceller shown in Fig. 4.6 can be found as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1+s(r_oC)}{(1+g_m r_o)+s(r_oC+\frac{1}{S_{LPF}})+s^2(\frac{r_oC}{S_{LPF}})} \tag{4.5}$$

Where r_o is the output resistance of the transconductance (g_m) cell and S_{LPF} is the low pass pole created by the low pass filter (LPF). Assuming $\frac{1}{r_oC} << S_{LPF}$, the transfer function can be approximated near DC as:

$$\frac{V_{out}(s)}{V_{in}(s)} \approx \frac{1}{1+g_m r_o}\frac{1+s(r_oC)}{1+s(\frac{r_oC}{1+g_m r_o})} \tag{4.6}$$

which clearly shows that the DC feedback loop functions as a high pass filter. Fig. 4.6 shows the frequency responses for the static DC offset canceller. By fixing the value of g_m and r_o and changing the value of C, we can easily change the high pass cutoff frequency of the static DC offset canceller.

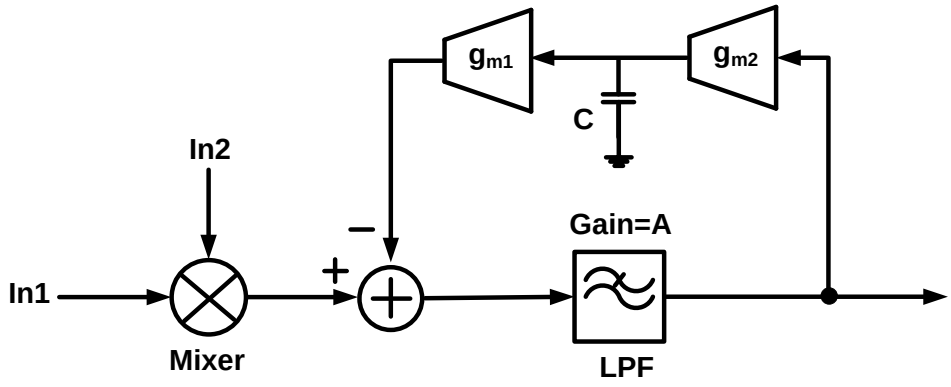


Figure 4.7 Detailed block diagram of static DC offset canceller.

Fig. 4.7 is the detailed block diagram of the static DC offset canceller implemented in this project. Often, the output of the mixer is current mode, so the transconductance cell is g_m included in the feedback path is also to convert the g_m C integrator output into the current so that the feedback current is subtracted from the input current.

DC feedback path through gm1 and gm2 removes DC offset at the mixer output providing a high pass pole. The high-pass cut-off frequency of the BPF is controlled by changing transconductance g_{m1} and g_{m2}. The high-pass pole is placed outside the PLL bandwidth to avoid any impact to the synthesizer's dynamic response. An active-RC integrator is used to implement a high linearity low-pass filter.

The output of the mixer contains DC term representing the LO frequency and close-in phase noise and high frequency terms representing higher harmonics and far out phase noise. In a closed loop PLL, the DC term and low-frequency phase noise is controlled by the loop filter and the loop gain suppresses low frequency deviations within the closed-loop bandwidth. When the DC terms and second harmonic component is filtered out, the band-pass filter output contains the phase noise of the oscillator for a desired bandwidth. In the proposed approach the extracted phase noise at the band-pass filter output is inverted and used as a tuning port of the auxiliary delay stage to cancel instantaneous phase error outside the PLL loop bandwidth.

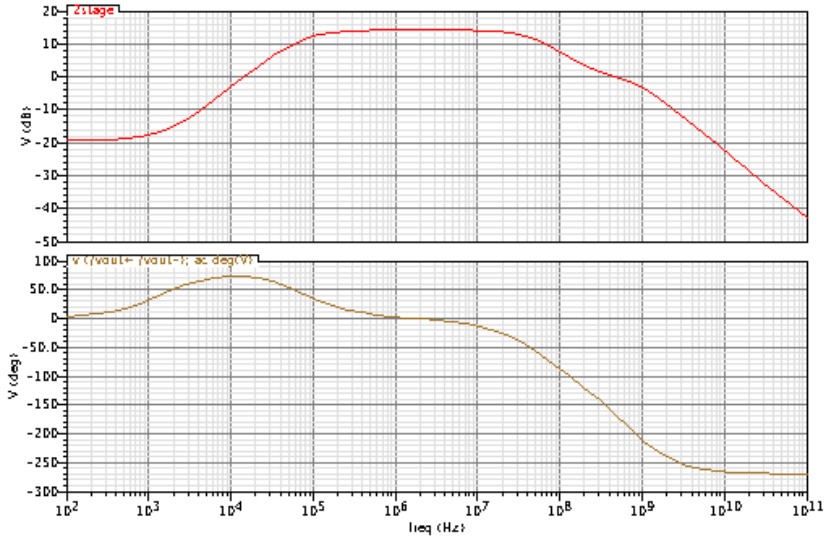


Figure 4.8 Simulation frequency response of static DC offset canceller.

The frequency response is illustrated in Fig. 4.8. The cut-off frequency of low pass filter was set to 20 MHz, and the location of the high pass pole was

made at 100 kHz. By varying the value of capacitance, we can change the high pass cut-off frequency.

Tradition active mixers can provide higher signal gain than passive mixers. However, they suffer from the noise generated by the transconductor and the switching transistors [26].

Although passive mixers have less gain and even introduce loss, they are more linear than active mixers. The other advantage of using a passive mixer is that is does not consume any DC power [27].

The main task in designing a passive mixer is to determine the sizes of the four transistors, since the noise figure, linearity, and conversion gain all depend on the widths of these transistors. As the widths of the transistors increase, linearity improves due to the decrease of the series resistances of the transistors. However, the conversion gain decreases as the series resistances decrease. As a result, the design of the widths of the transistors is a trade-off between noise, linearity and conversion gain. Fig. 4.9 shows schematic of the passive mixer used in cancellation loop.

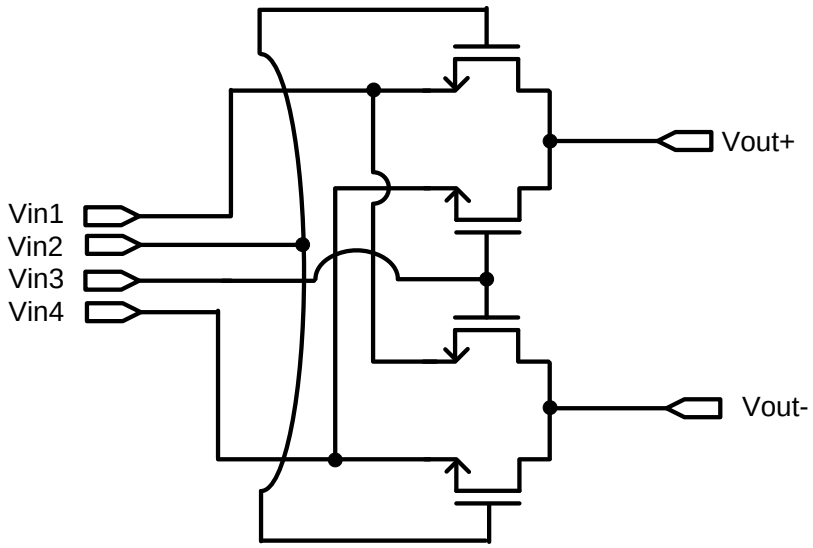


Figure 4.9 Passive mixer circuit schematic.

The passive mixer architecture is current input and current output. Transimpedance amplifier (TIA) provides the low impedance not at the mixer output [28]. Fig. 4.10 shows the schematic of TIA. TIA is composed of a two stage op amp with a 200 MHz unity gain bandwidth. RC feedback in low-pass filter is applied around the op amp to produce a 20 MHz pole frequency.

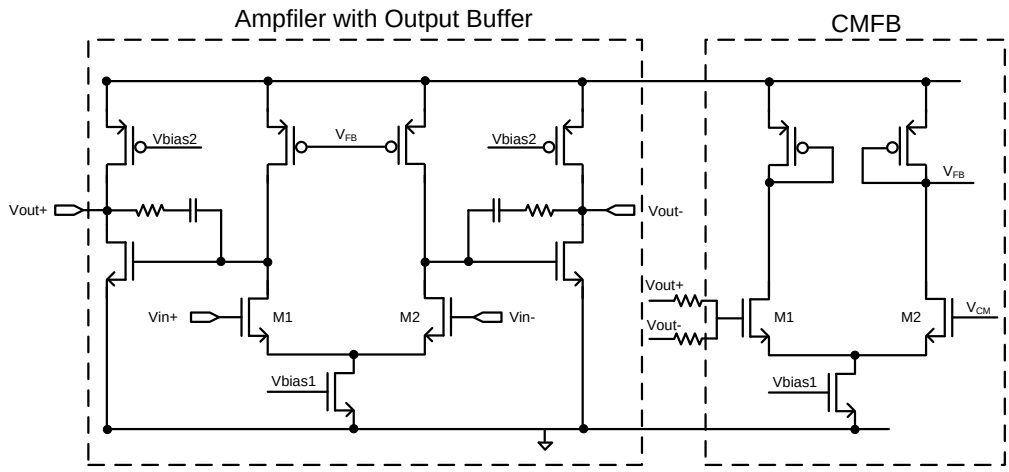


Figure 4.10 Schematic of TIA stage.

4.3 VARIABLE GAIN AMPLIFIER (VGA)

A current-steering fully differential VGA provides high linearity and wide gain tuning range to compensate for variations in the variable-delay cell tuning characteristic.

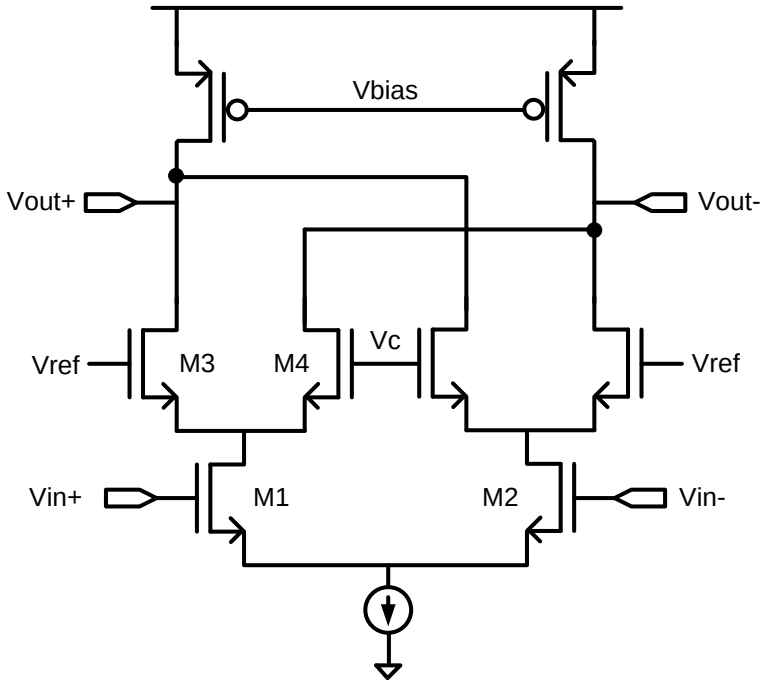
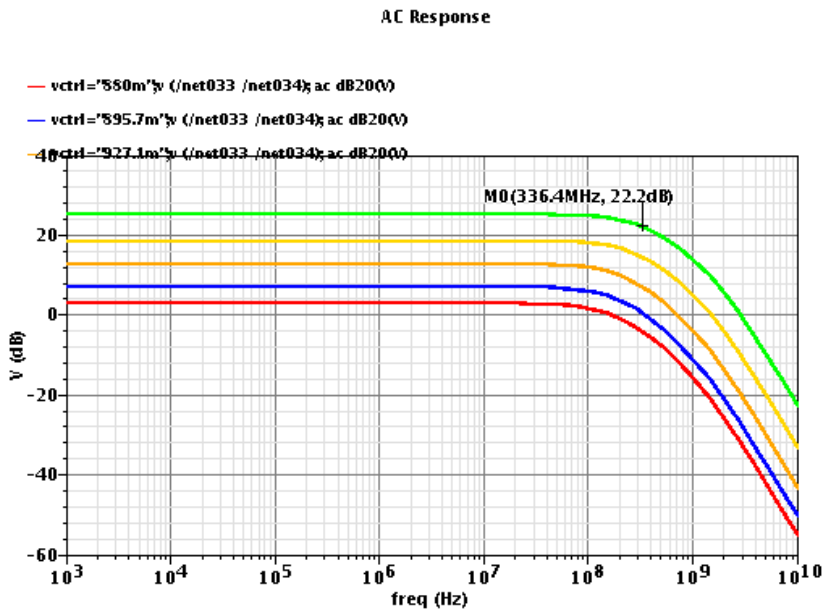


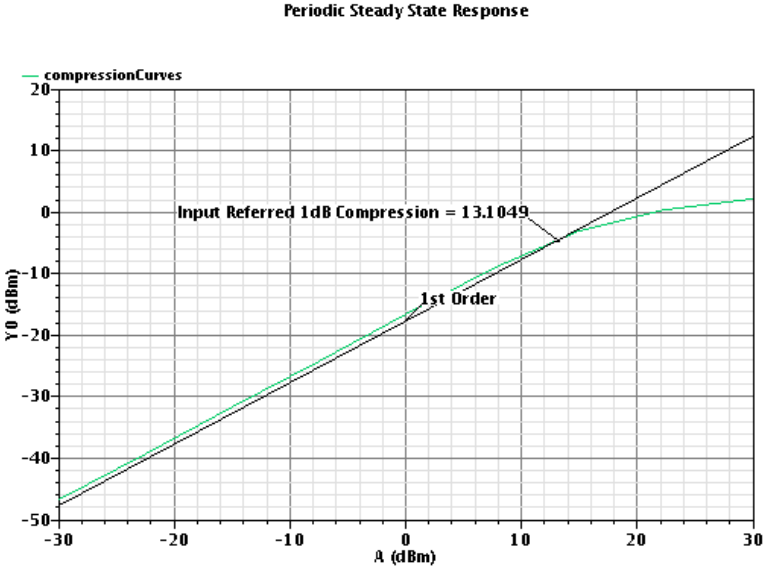
Figure 4.11 VGA circuit schematic.

Fig. 4.9 shows a core of VGA. Vin+ and Vin- are the differential input signal and Vr and Vc are the control voltage from reference bias circuit [29]. A current steering circuit is adopted for high linearity consideration and gain of this circuit is given by:

$$Av = 2\frac{g_{m3}}{g_{m3} + g_{m4}} g_{m1,2} R_{out} \tag{4.7}$$



(a) AC simulation result of VGA



(b)Simulation result of P1dB compression point

Figure 4.12 Simulation results of VGA

-3 dB frequency of VGA has 300 MHz when gain is 25 dB. The gain has a function of external control voltage (Vc) with a range of 22 dB. 1dB compression point is at least 13 dBm. Simulation results of AC response and 1dB compression point shows in Fig 4.10.

4.4 POLYPHASE FILTER

The mixer acts as an ideal phase detector by forcing the input signals to be in quadrature. Considering the mixer in a standalone operation, any deviation error from quadrature results in an output amplitude error, which is very small when the deviation around quadrature is small. For example, a 1 degree offset from quadrature results in an amplitude error of -0.001 dB. In the delay-line discriminator is much worse than the standalone mixer case. The deviation from a quadrature condition is amplified by the delay, which results in significantly larger dc offset and amplitude detection errors. Polyphase filter maintains the output of the ring oscillator in quadrature to reduce the dc offset errors.

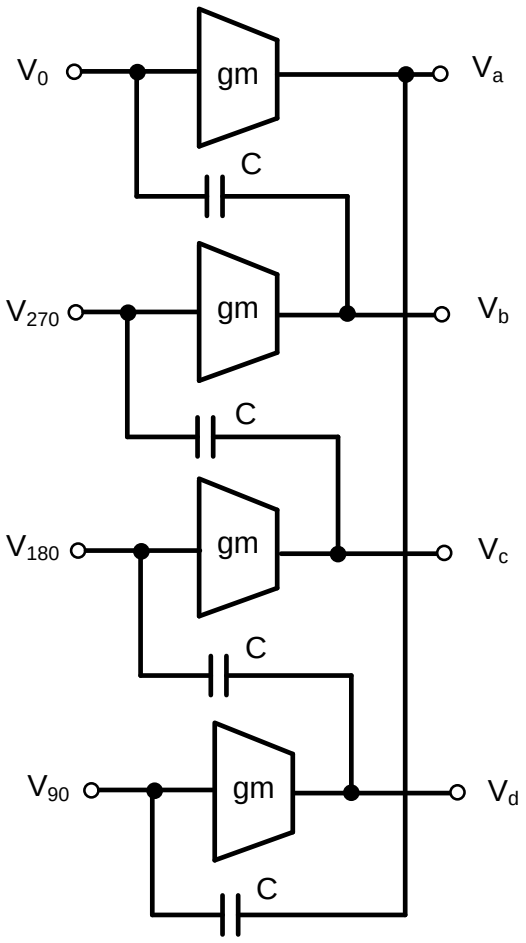


Figure 4.13 The active polyphase filter.

The passive polyphase filter is lossy and needs additional buffers among the stages to compensate the loss. Furthermore, the variation of resistances and capacitances should be kept within a desired small range. When it comes to on-chip implementations, passive elements such as varactors, capacitors and inductors are very limited. On the other hands, active polyphase filters have the general advantages of low power dissipation, small chip area and high signal gain.

In active polyphase filter, the resistors are replaced by transconductances as shown in Fig. 4.12. This topology of active polyphase filter has benefit of high input impedance and relaxes the loading of the preceding stage. The effective g_m can be implemented with CMOS inverters. Active polyphase filter avoids the degradation of gain among stages [30]. In addition, sufficient gain and isolation can be achieved without additional buffers compared to passive polyphase filter.

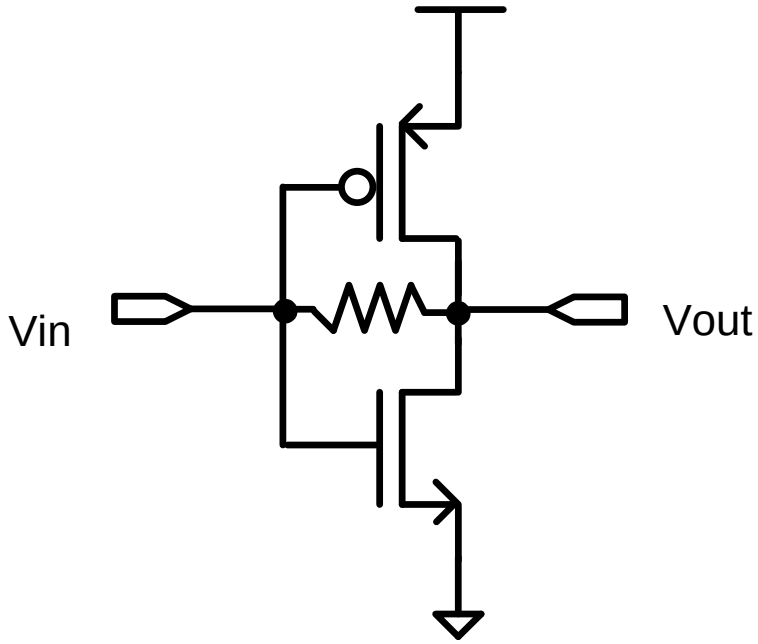


Figure 4.14 CMOS inverter with internal resistor feedback.

4.5 PHASE FREQUENCY DETECTOR

Fig. 4.13 shows the block level schematic of PFD. all the blocks use standard CMOS logic circuits [31]. The delayed reset signal path made by two inverters resolves deadzone issue.

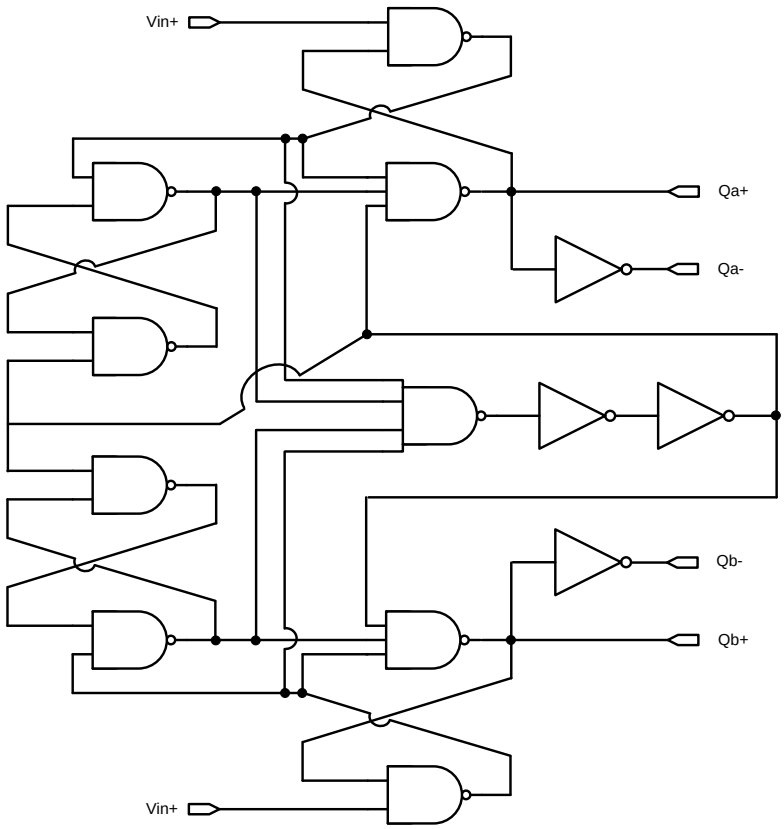


Figure 4.15 PFD schematic.

CHAPTER 5

EXPERIMENT RESULTS

The PLL was fabricated in a 90nm CMOS technology. The chip was mounted on a standard FR4 PC board. The current consumption of the PLL is 24.7mA when the cancellation technique enabled. Die photo is shown in Fig. 5.1. The core of the IC occupies 0.38mm × 0.32mm silicon area.

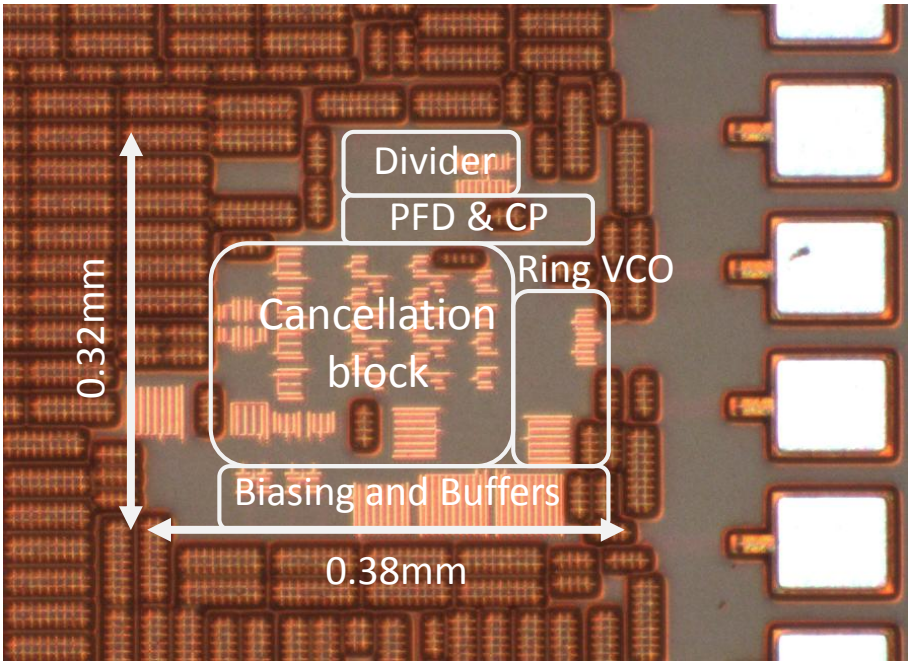


Figure 5.1 Micrograph of the IC

Fig. 5.2 shows the test setup for measuring PLL performances. Agilent E4443A spectrum analyzer is used to measure the spectrum and the phase noise of the output. The frequency synthesizer was tested with a reference frequency of 10 MHz. Signal generator provides the control signal of the divider and external modulated noise signal to use the calibration of cancelation the loop gain.

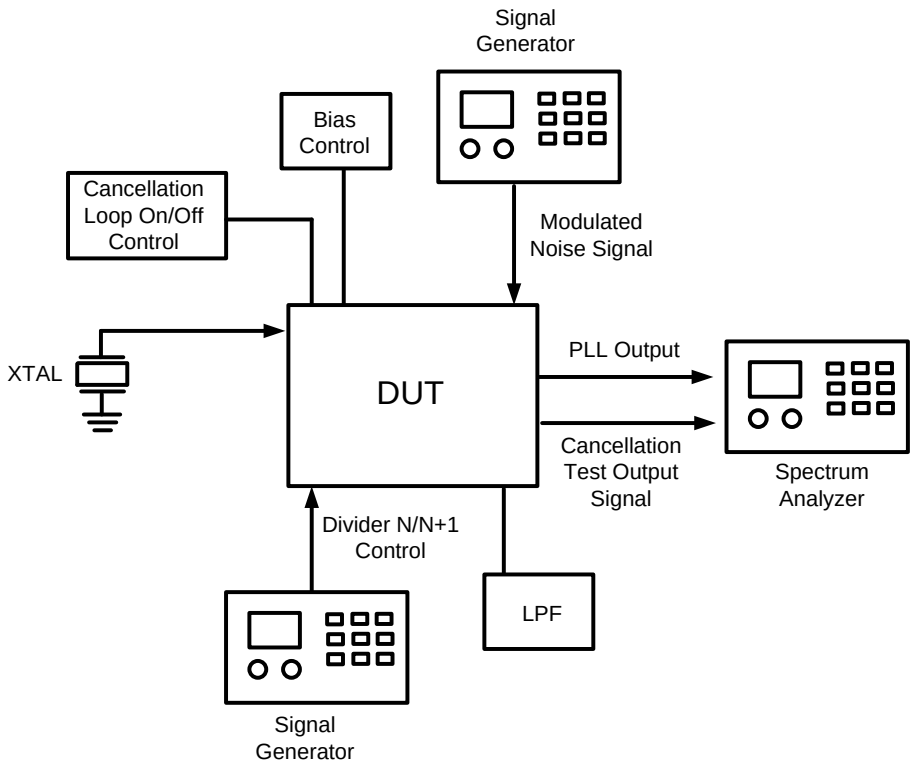


Figure 5.2 Test setup.

Fig. 5. 4 shows the single tone (ST) sensitivity of delay-line discriminator in the cancellation loop. The equivalent phase noise sensitivity is calculated from the ST results by averaging the three consecutive ST results.

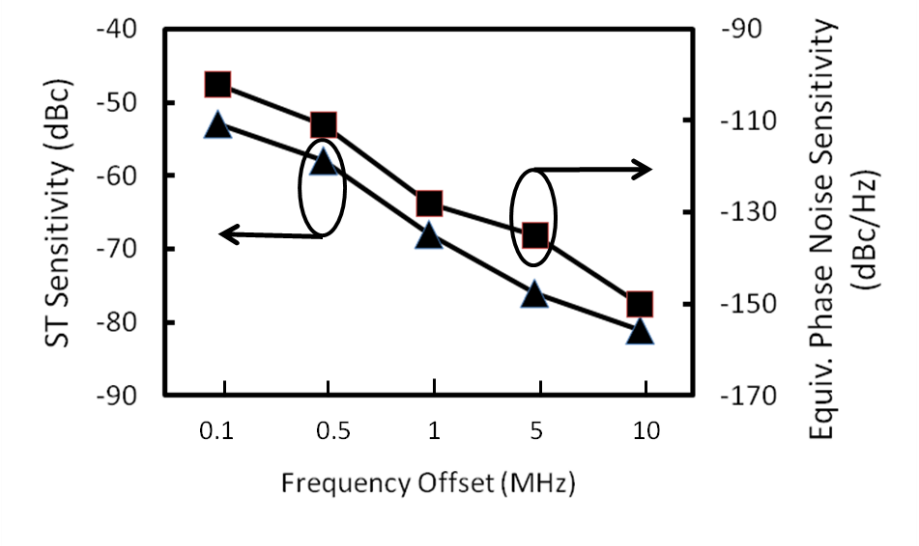


Figure 5.3 Single tone (ST) sensitivity (left), and equivalent phase noise sensitivity (right) of the proposed feed-forward delay discriminator noise cancellation path as a function of offset frequency from carrier.

Fig. 5.1 shows the phase noise measurements before and after enabling cancellation loop. Phase noise reduces in the cancellation bandwidth up to 20 MHz with a 200 kHz PLL loop bandwidth. The cancellation loop attenuates the phase noise at 1 MHz offset by 12.5 dB. The measured phase noise at 1 MHz offset is -105 dBc/Hz.

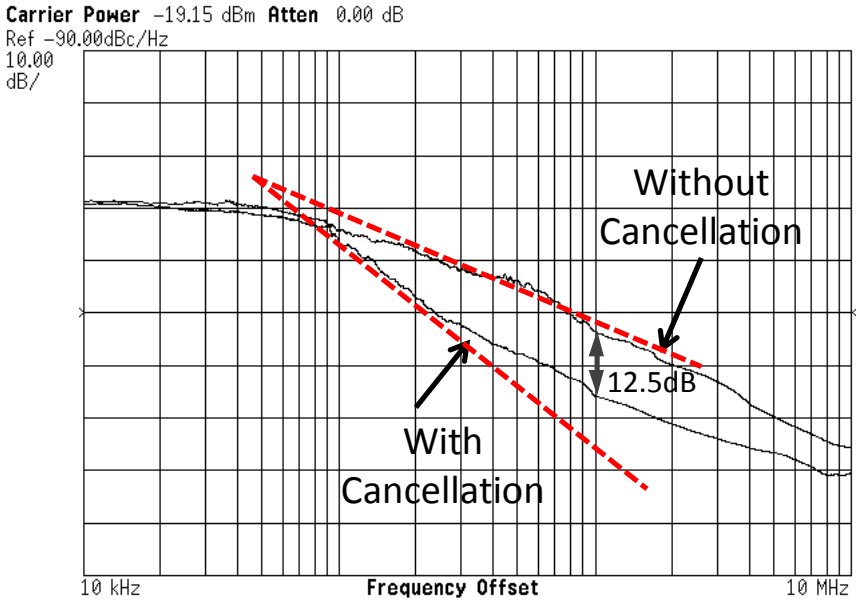
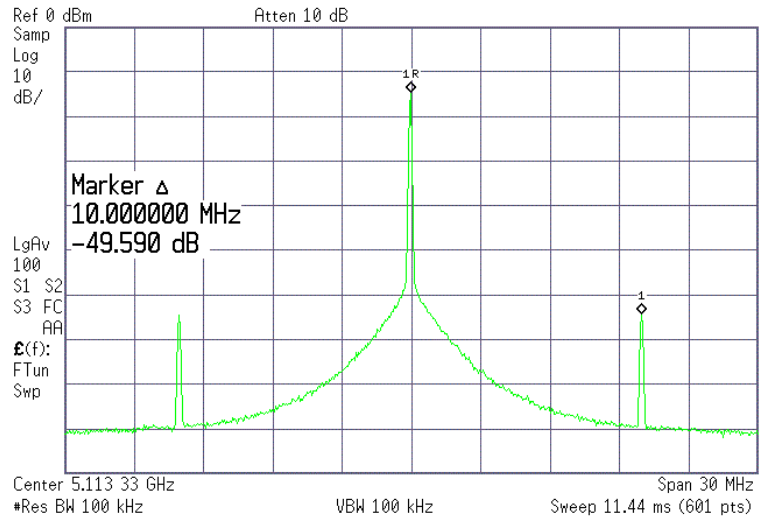
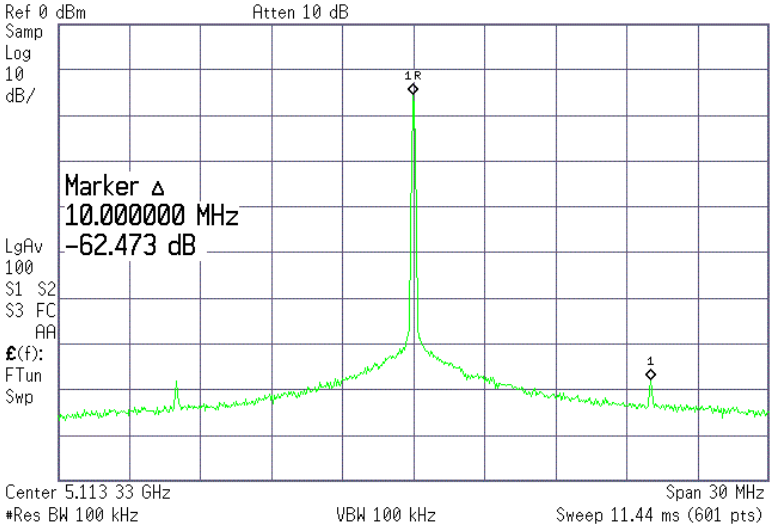


Figure 5.4 Measured PLL output phase noise with and without phase noise cancellation.

Fig. 5.2 shows PLL output spectra at 5.1GHz when the PLL divider is modulated with a 10 MHz clock signal. The cancellation loop reduces the 10 MHz spurious tone level by 13 dB. This result shows that the proposed architecture can also be used to mitigate out of band quantization noise of ΣΔ fractional-*N* frequency synthesizers.



(a) Noise-cancelling loop OFF



(b) Noise-cancelling loop ON

Figure 5.5 PLL output PSD with 10MHz digital divider modulation showing 13dB spur reduction (a) PSD without noise-cancelling loop. (b) PSD with loop enabled.

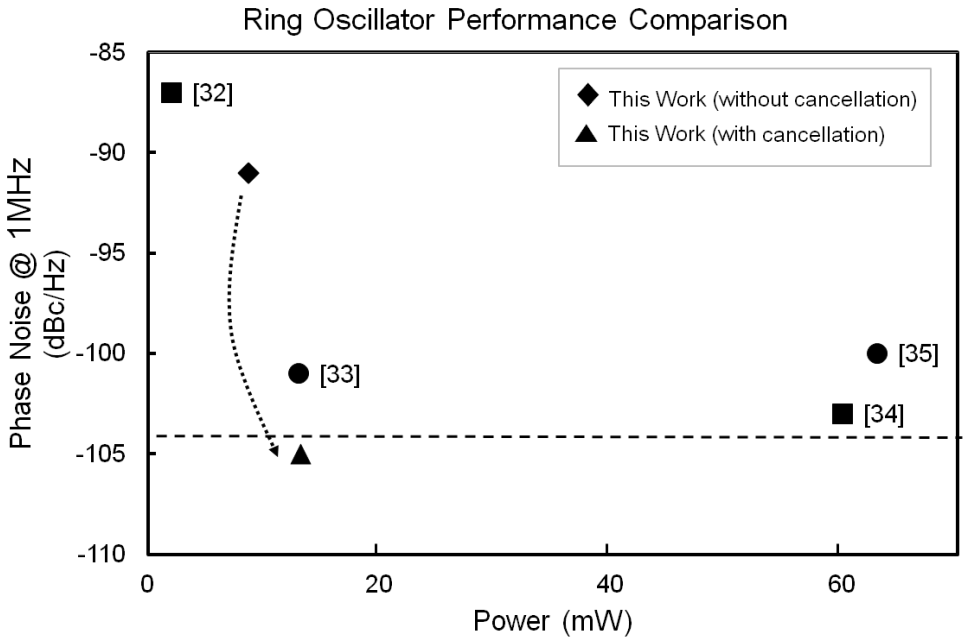


Figure 5. 6 Performance comparison of state-of-the-art ring oscillators with respect to the proposed approach, *with and without* active noise cancellation.

Ring oscillator has strong trade-off between phase noise and power consumption in the equation 4.3. Fig. 5.2 shows a comparison to previous work reported on ring oscillators. The performance of the implemented PLL is summarized in the table of Table. 5.1.

Table 5.1 PLL performance summary.

Main Parameters	
Technology	90nm CMOS
Supply Voltage	1.2V
Operating Frequency	5GHz
Tuning Range	3.5GHz – 7.1GHz
Reference Frequency	10MHz
Loop Bandwidth	200kHz
Phase Noise @1MHz (5GHz)	-105dBc/Hz
Reference Spur	-64.8dBc
Phase Noise Cancellation Bandwidth	100kHz – 20MHz
Phase Noise Cancellation @1MHz	12.5dB
Current Consumption (@5GHz)	
VCO	7.3mA
Cancellation Loop	3.7mA
Charge-pump, PFD, Divider and Bias Circuitry	13.7mA
Total	24.7mA
Core Die Area	
0.38mm×0.32mm	

CHAPTER 6

CONCLUSIONS

Voltage Control Oscillator (VCO) is one of the key components in Phase Lock Loops. LC tank based VCOs have a superior phase noise performance, and narrower loop bandwidth which makes it suitable for RF and high-speed optical communication, however, its performance is limited by the large area of the resonator circuit, it has higher power consumption, and has limited tuning range. Ring Oscillators (RO) are widely used in PLL and has a wider loop bandwidth and is suitable for circuits with more relaxed phase noise requirement such as clock generation and clock synchronization in microprocessors, and data recovery. The (RO) PLL is preferred due to its reduced size, lower power consumption, scalability, and ease of implementation in the digital process. However, the RO VCO has higher jitter and phase noise due to active device noise, thermal noise, supply, ground noise, and substrate noise coupling which limits is application for RF transceiver, data converters, serial I/O bus, and high-speed optical communications. Although LC tank VCO generally has better phase noise performance, there is a strong motivation to develop RO with comparable phase noise. Particularly, out-of-band phase noise of RO-based PLLs is dominated by RO performance, which cannot be suppressed by the loop gain, impairing RF receiver's sensitivity or BER of optical clock-data recovery circuits. The implemented noise-cancelling loop potentially enables application of RO based PLL for demanding frequency synthesizers applications, such as optical links or high-speed serial I/Os. The objective of the adaptive feed-forward noise

cancelation is on-chip far-out phase noise measurement and cancelation to achieve low phase noise performance. The proposed PLL utilizes a similar delay-line discriminator to extract RO's instantaneous phase noise in a given bandwidth, and cancel it with a matched delay element. This thesis presents design, integration, and measurement of an adaptive noise canceling RO based PLL fabricated in 90nm IBM process.

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