A 280 mW, 0.07 % THD+N Class-D Audio Amplifier

Using a Frequency-Domain Quantizer

by

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ABSTRACT

Pulse Density Modulation- (PDM-) based class-D amplifiers can reduce non-linearity and tonal content due to carrier signal in Pulse Width Modulation - (PWM-) based amplifiers. However, their low-voltage analog implementations also require a linear- loop filter and a quantizer. A PDM-based class-D audio amplifier using a frequency-domain quantization is presented in this paper. The digital-intensive frequency domain approach achieves high linearity under low-supply regimes. An analog comparator and a single-bit quantizer are replaced with a Current-Controlled Oscillator- (ICO-) based frequency discriminator. By using the ICO as a phase integrator, a third-order noise shaping is achieved using only two analog integrators. A single-loop, single-bit class-D audio amplifier is presented with an H-bridge switching power stage, which is designed and fabricated on a 0.18 um CMOS process, with 6 layers of metal achieving a total harmonic distortion plus noise (THD+N) of 0.065% and a peak power efficiency of 80% while driving a 4-ohms loudspeaker load. The amplifier can deliver the output power of 280 mW.

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1 INTRODUCTION

1.1 Overview of Class-D Audio Amplifier

High power efficiency and reduced thermal losses associated with class-D amplifiers offer many benefits in low-cost and low-power audio products, including extended battery life, reduced heat dissipation, and external component count. The power stages of class-D amplifiers most commonly use Pulse Width Modulation (PWM) control techniques, which offer simplicity and the lowest possible switching frequency, thus minimizing switching losses in the output stage [1].

Typical class-D amplifiers mainly consist of three stages, as shown in Figure 1-1: the pulse width modulation stage, the power amplification stage, and the output filter stage. In the pulse width modulation stage, audio input signal is compared with a carrier waveform, like sawtooth or triangular, in a comparator. As a result, audio input signal is converted into higher frequency switching pulses, with widths proportional to the input amplitude. The gate driver controls the switching transistors by using these pulses.

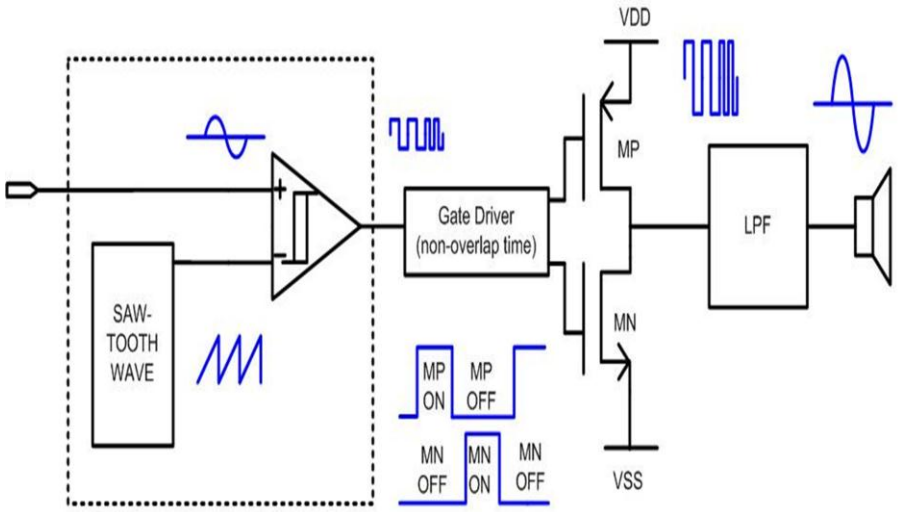

Figure 1-1: Typical class-D amplifier.

The power amplification stage of Class-D amplifiers operates like switches. Switching transistors are either fully turned on or fully turned off. When the transistor is off, the current through it is zero. When it is on, the voltage across it is small—ideally, zero. In each case, the power dissipation is very low. Therefore, Class-D amplifiers can achieve a higher efficiency compared to other types of amplifiers such as Class-A or Class-AB. Class-D amplifiers require less power from the power supply and can reduce the size of heat sinks for the amplifier. An amplified square wave signal from the switching transistors is demodulated by a low-pass filter that removes the high frequency elements. Therefore, an equivalent amplified analog signal is regenerated after passing through the low pass filter.

The reproduced output voltage in the output filter stage can be mathematically derived by using the equation of the inductor voltage and current. The filtered output voltage and current can be considered constant during a switching period because the carrier switching frequency is much greater than the maximum input audio frequency [2].

The instantaneous inductor current is

$$I_L(t) = \frac{1}{L}\int V_L(t)\,dt \tag{1.1}$$

where $V_L(t)$ is the instantaneous voltage across the inductor. The inductor current at t_0 should be equal to the inductor current at t_2, as shown in Figure 1-2, because the average inductor current is assumed constant during one switching period. Hence, equation (1.2) can be obtained.

$$\frac{1}{L}\int_{t_0}^{t_2} V_L(t)dt = I_L(t_2) - I_L(t_1) = 0 \tag{1.2}$$

The absolute values of the areas, A_{ON} and A_{OFF}, should be equal to each other to satisfy equation (1.2). In other words,

$$A_{ON} = |A_{OFF}| \tag{1.3}$$

$$A_{ON} = (V_{DD} - V_O) \times t_{ON} \tag{1.4}$$

$$A_{OFF} = V_O \times t_{OFF} \tag{1.5}$$

Substituting equation (1.4) and (1.5) into equation (1.3) will give

$$(V_{DD} - V_O) \times t_{ON} = V_O \times t_{OFF} \tag{1.6}$$

From equation (1.6),

$$V_O = V_{DD} \times \frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{DD} \times D \tag{1.7}$$

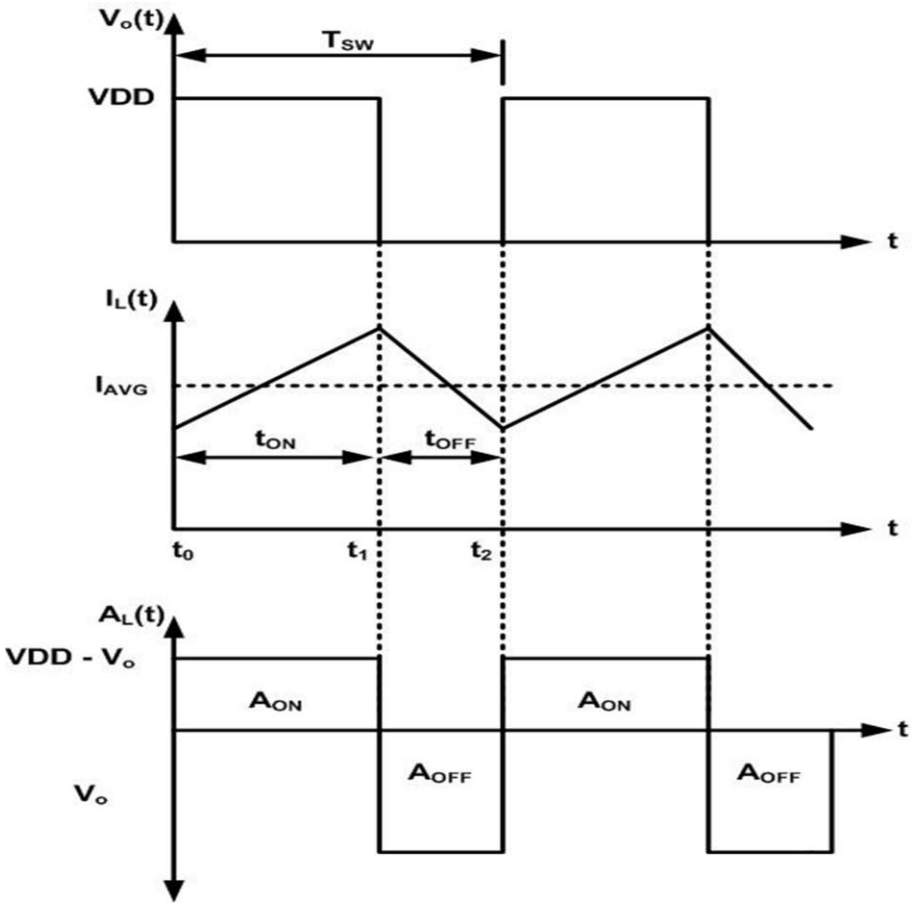

Figure 1-2: Inductor current and voltage waveforms.

where D is the duty ratio of the output switching waveform.

1.2 Total Harmonic Distortion and Noise in Closed-Loop Architecture

Many class-D amplifiers with PWM based control have adopted both open-loop and closed-loop architectures. The open-loop architecture directly feeds a signal into the PWM generator, and may enable easier digital-input implementation. However, open-loop architectures as shown in Figure 1.1 suffer from nonlinearities and noise due to dead time, amplitude-dependent output impedance modulation, linearity of the carrier waveform, and limited Power-Supply Rejection Ratio (PSRR) [3],[4].

Closed-loop PWM-based class-D amplifiers, due to their negative feedback operations, can address many of the problems associated with open-loop, class-D amplifiers. Figure1-3 shows a typical closed-loop class-D amplifier, and Figure 1-4 shows the linear model of its amplifier, where the gain of the PWM and output stage is assumed to be constant [5]. In Figure 1-4, the system transfer function (V_{out} / V_{in}) and noise transfer function (V_{out} / V_N) are represented as

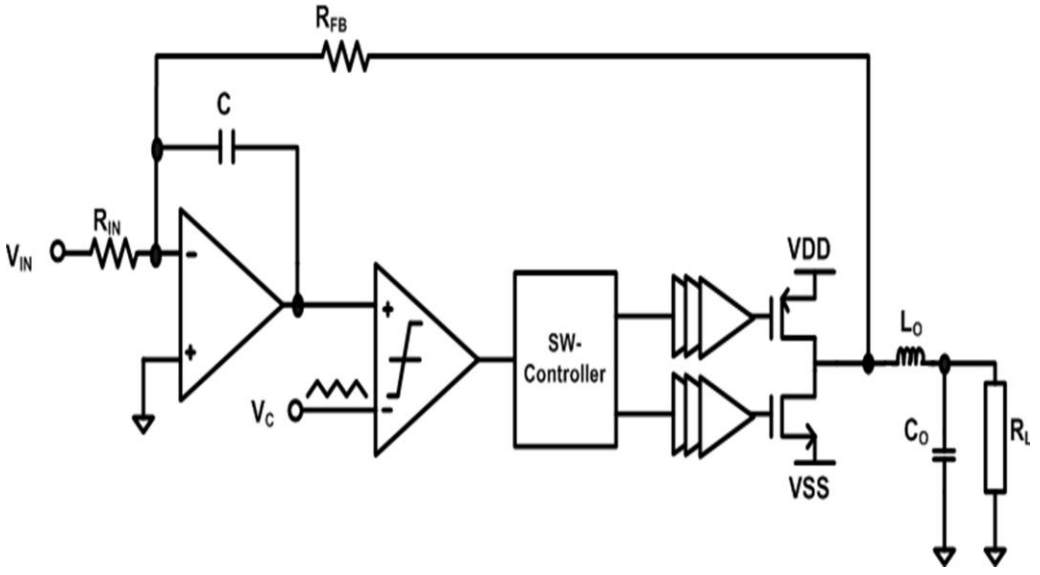

Figure 1-3: A closed-loop class-D amplifier.

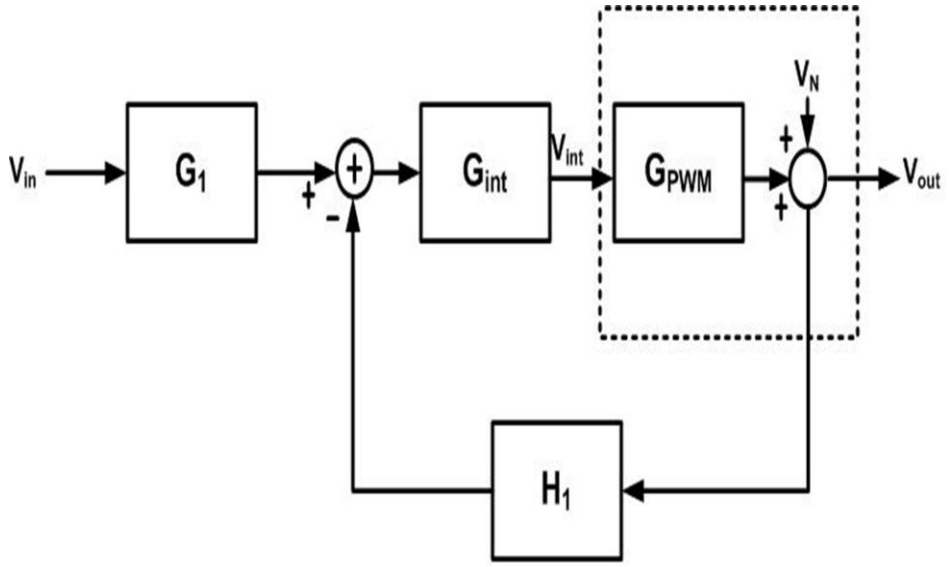

Figure 1-4: A linear model of a closed-loop class-D amplifier.

$$\left.\frac{V_{out}}{V_{in}}\right|_{V_N=0} = \frac{G_1 G_{\text{int}} G_{PWM}}{1+G_{\text{int}} G_{PWM} H_1} \approx -\frac{R_{FB}}{R_{IN}} \tag{1.8}$$

$$\left.\frac{V_{out}}{V_N}\right|_{V_{in}=0} = \frac{1/2}{1+G_{\text{int}} G_{PWM} H_1} \tag{1.9}$$

$$G_1 = R_{FB}/(R_{IN}+R_{FB}) \tag{1.10}$$

$$H_1 = R_{IN}/(R_{IN}+R_{FB}) \tag{1.11}$$

$$G_{\text{int}} = \frac{A}{1+sCR_{IN}(1+A)} \tag{1.12}$$

where A is a DC open-loop gain of the amplifier, and V_N is the non-linearities due to harmonic distortion and power supply noise. From equation (1.9), V_N can be reduced by optimizing the gain of the PWM stage, G_{PWM}, the feedback factor, H_1, and the gain of the integrator, G_{int} in the closed-loop architecture [5]. The gain of the PWM stage, G_{PWM}, is obtained by calculating the ratio of the power supply voltage over the amplitude of the

carrier signal. The linearity of the carrier waveform is one of important practical parameters in PWM-based class-D amplifiers that directly affect the performance of THD. In [6], the effect of the carrier non-linearity related to THD is mathematically analyzed.

The feedback schemes of PWM-based closed-loop amplifiers still present the problem of undesirable amounts of distortion and Electro-Magnetic Interference (EMI), which is harmonically related to the PWM carrier [4]. The EMI in a PWM-based amplifier is produced by the concentrated spectral energy in its switching frequency and harmonics.

1.3 Output Stage of Class-D Amplifier

The output architectures for class-D amplifiers can be categorized into two architectures; half-bridge and full-bridge topologies. There are advantages and disadvantages to each. A half-bridge architecture uses two transistors, while a full-bridge architecture uses four transistors as shown in Figures 1.5 and 1.6. Therefore, a half-bridge architecture is simpler and thus results in fewer components and less conduction and switching losses than that of a full-bridge architecture. On the other hand, a full-bridge architecture, which is often referred to as a bridge-tied load (BTL) or as H-bridge, even-

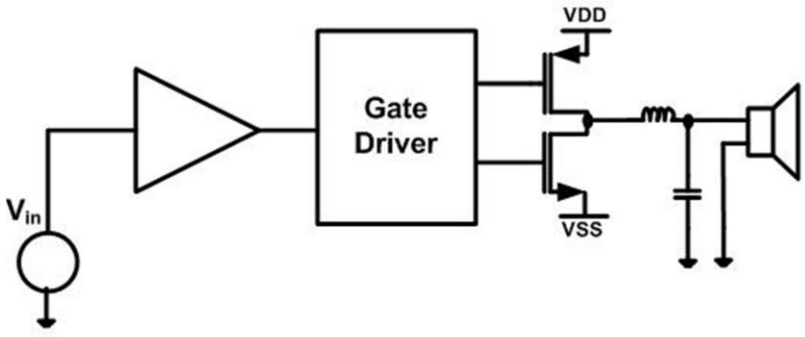

Figure 1-5: Half-bridge configuration.

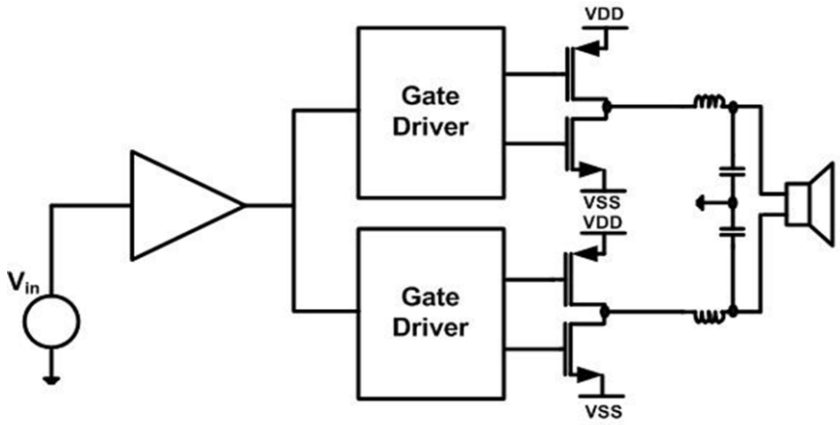

Figure 1-6: Full-bridge configuration.

order harmonic distortion can be eliminated because a full-bridge architecture has the differential output structure and generates a differential PWM signal across the load. A three-level PWM operation scheme can be also implemented for filterless applications in a full-bridge topology. Another advantage of a full-bridge is that it can achieve twice the output signal swing and thus deliver up to four times the power to the load than a half-bridge topology operating from the same supply voltage.

The power efficiency of the ideal class-D amplifier is 100%. In practice, however, there is a limit to how much power efficiency can be achieved due to power losses in the output stage. The power efficiency of the output stage can be expressed as

$$\eta = \frac{P_{Load}}{P_{Load} + P_{Loss}} \times 100\,[\%] \tag{1.13}$$

The main power dissipations in the output stage are conduction losses, switching losses, and capacitive losses. Conduction losses are due to the on-resistance of the switches. Switching losses are a result of the short-circuit path from the supply to ground when two switching transistors are simultaneously ″on″ during the transitions of input

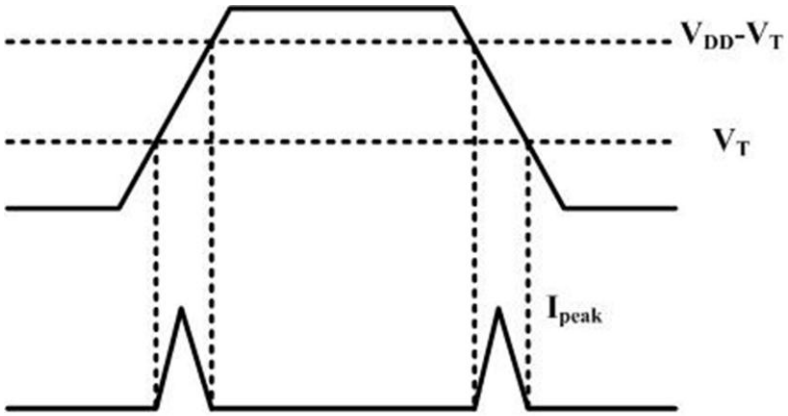

Figure 1-7: Voltage across and current through the transistor during the transitions of input signal.

signal as shown in Figure 1-7. Capacitive losses are a result of charging and discharging parasitic load capacitances. The total power loss can be represented as

$$P_{Losses} = P_{cond} + P_{sw} + P_{cap} \tag{1.14}$$

$$P_{cond} = I^2 R_{on} \tag{1.15}$$

$$P_{sw} = \left(\frac{t_r + t_f}{2} \right) \cdot V_{DD} \cdot I_{peak} \cdot f_{PWM} \tag{1.16}$$

$$P_{cap} = C_{in} \cdot V_C^2 \cdot f_{PWM} + C_{out} \cdot V_{dd}^2 \cdot f_{PWM} \tag{1.17}$$

where I is equal to the output current, R_{on} is the on-resistance of the switching transistors, f_{PWM} is the switching frequency, V_c is the voltage to which parasitic capacitances are charged, and C_{in} and C_{out} represent the total parasitic capacitances.

1.4 Voltage Domain Vs. Frequency Domain Signal Processing

In typical low-power analog loop filter implementations, although the power supply voltage decreases, threshold voltages and saturation voltage (V_{DSAT}) required by the transistor operation are not scaled down linearly. This causes the dynamic range of

the analog signals to decrease and the nonlinearity generally increases because the transistor is working close to V_{DSAT}. Hence, low supply voltage operation results in lower signal swing, which makes analog circuit design a lot more difficult in voltage domain signal processing. However, as shown recently in several data converter applications [7],[8],[9], frequency domain signal processing maps the low-supply regime challenges to time domain, which resembles digital processing in its dynamic range requirements.

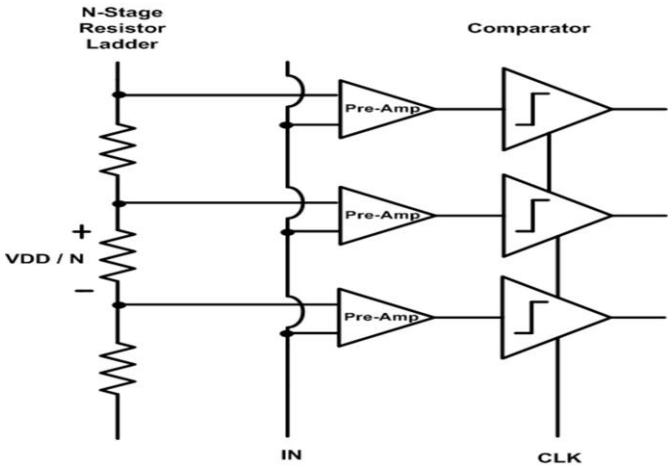

Figure 1-8: Voltage-domain comparator-based quantizer.

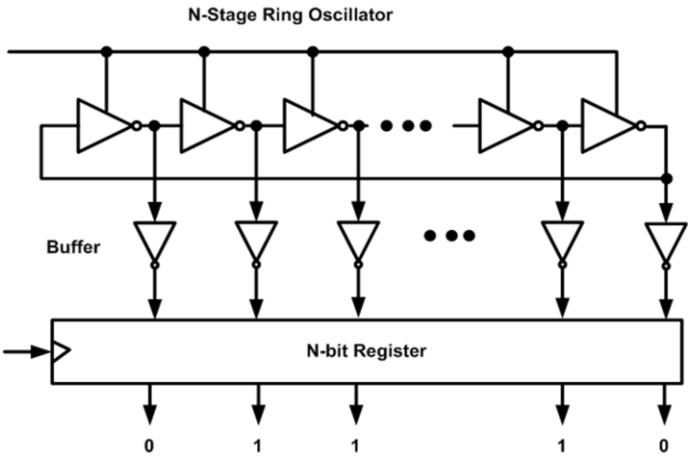

Figure 1-9: Frequency-domain quantizer.

The voltage-domain comparator-based quantizer and the frequency-domain quantizer are shown in Figure1-8 and 1-9, respectively. If we compare a traditional voltage-domain comparator-based quantizer with the oscillator-based frequency quantizer to achieve multiple quantization levels, the reference voltage is divided by the number of bits in the comparator-based quantizer. Therefore, step size is reduced by increasing the number of bits in the voltage-domain signal processing. It can also generate metastability in low-voltage design. Therefore, low offset pre-amplifier is required before comparator to avoid this problem. Low offset pre-amplifier often consumes a relatively large area and a large amount of power in order to achieve low offset voltages and high speed operation [8].

Kickback noise is also a problem in latched comparators because the instantaneous currents are coupled with inputs of comparator through parasitic gate-source and gate-drain capacitance of transistors as shown in Figure. 1-10. The instantaneous large currents are created by the large voltage variation in regeneration nodes when the latch part of comparator regenerates the difference signals. This also causes harmonic distortion in class-D applications.

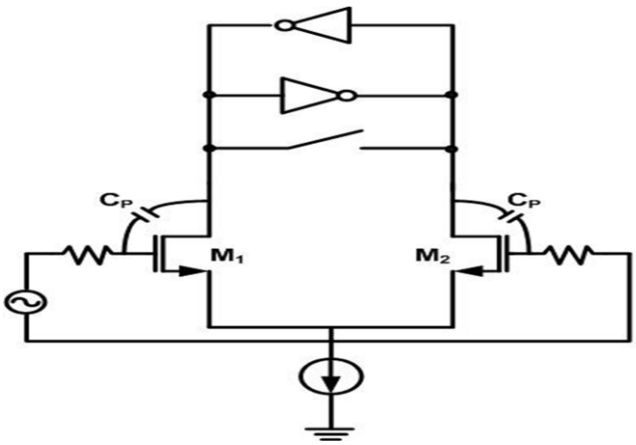

Figure 1-10: Example of parasitic capacitances of the latched comparator.

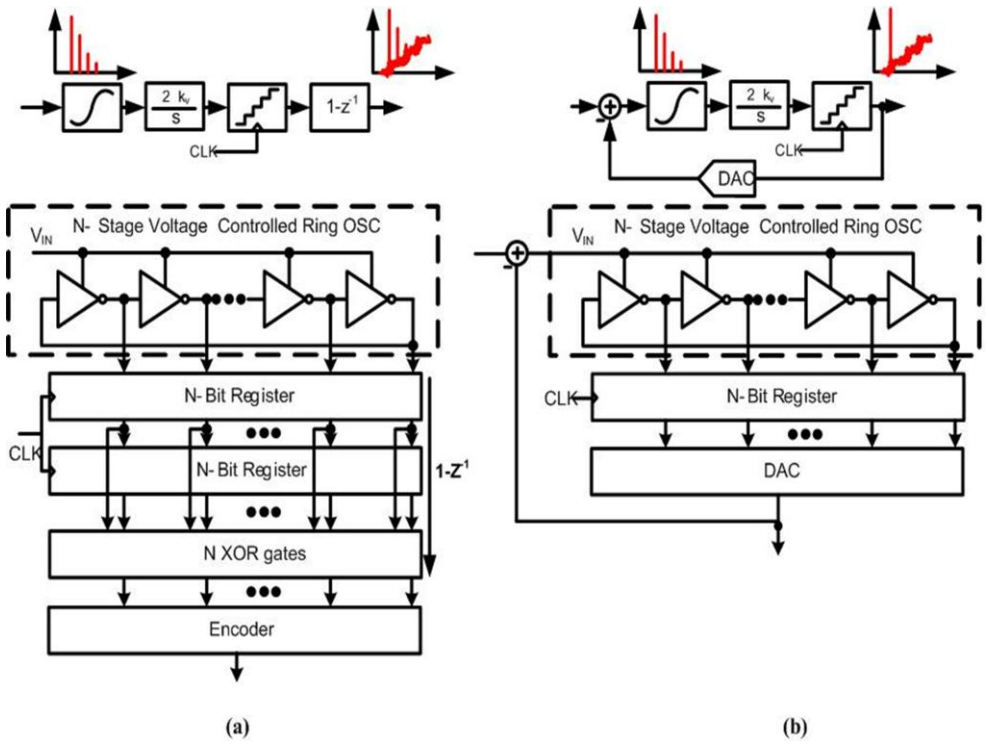

Figure 1-11: Examples of the frequency-domain ADCs with (a) the open-loop and (b) the closed-loop architecture.

However, in frequency-domain quanitzer, voltage-controlled oscillator (VCO) generates the frequency, which is proportional to the average analog input signal. Frequency-domain quantizer doesn't require the power consuming pre-amplifier and it is also a highly digital implementation.

Therefore, frequency-domain signal processing offers a better resolution than that of voltage-domain methods in low-voltage designs. Table 1-1 shows a summary comparing the voltage domain and frequency domain quantizer. Figure1-11 shows examples of ADCs using the frequency-domain. In Figure 1-11a, registers and XOR gates perform the first-order difference of sampled/quantized VCO phases and thereby convert the VCO phase signal to a corresponding VCO frequency signal [10]. Therefore, frequency is the output variable of the quantizer and the mismatch in delay across the

stages of VCO is effectively first-order noise shaped. However, the nonlinearity of the VCO′s voltage-to-frequency conversion gain (K_{vco}) severely limits the resolution of this open-loop architecture. In Figure 1-11b, the VCO phase is sampled and quantized by registers and the output of DAC is feedback. Therefore, linearity is improved but the closed-loop architecture lost the first order shaping of VCO′s delay mismatch [7].

Table 1-1

The Comparison of the Voltage Domain and the Frequency Domain Quantizer

Voltage Domain Quantizer	Frequency Domain Quantizer
Vref / N	Variable delay of VCO stages
- Metastability - Requiring low offset pre-amplifier - Kickback of comparator - Increased area / power consumption	- Highly digital implementation - Compact & high speed operation without requiring high-power consumption

1.5 Motivation and Goals of Thesis

The range of audio input frequencies is from about 20 Hz to 20 kHz. Therefore, audio amplifiers in this range should have good frequency response. The objective of audio amplifiers is to regenerate amplified audio input signals faithfully, efficiently, and with low distortion. Therefore, audio amplifier designs mainly require a low THD+N operation, high power efficiency, high power-supply rejection ratio, feedback of the

output signal to reduce or eliminate distortion and noise from the output power stage and low EMI.

Low-supply voltage operation makes analog circuit design more difficult in voltage-domain signal processing. An effective way to overcome the difficulty of low-voltage design is to process the signal in the frequency domain. Circuits operated in the frequency domain are basically digital. Therefore, frequency-domain signal processing offers advantages such as less consuming power and smaller chip size.

The aim of this research is to define a new class-D audio amplifier architecture and develop design techniques to satisfy the above requirements in low power supply. A PDM-based class-D audio amplifier using frequency-domain quantizer is proposed to satisfy these requirements. The fully differential topology is used to increase the noise-dependent dynamic range, which is also an important issue in low-voltage design.

1.6 State of Arts

There are a variety of topologies to achieve the required performances in class-D audio amplifiers. Alternative approaches are using a mixed voltage/current feedback to reduce distortion [11] and using a linear amplifier and a switching amplifier in a master-slave configuration [12]. The mixed voltage/current feedback configuration is shown in Figure1-12. The LC output filter is placed outside the feedback loop in the typical voltage-mode class-D amplifier because of the significant phase shift of the filter. Because of this, the feedback configuration of the typical voltage-mode class-D amplifier cannot reduce the distortion from the low-pass LC output filter due to the behavior of the inductor′s magnetic core (hysteresis and saturation). However, in mixed voltage/current feedback configuration, the filter is placed in feedback path and this configuration can reduce filter non-linearities by one order of magnitude. The disadvantage of this

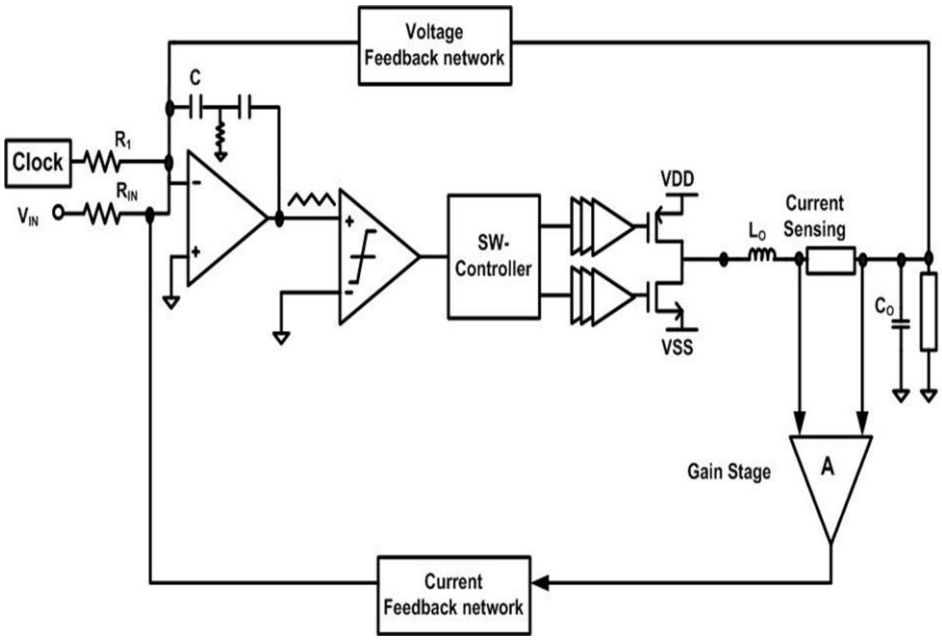

Figure 1-12: Mixed current/voltage feedback configuration.

configuration is that ensuring stability in various load and signal swing conditions is a critical requirement.

Figure 1.13 shows the linear-switch mode combination amplifier. In linear-switch mode combination amplifiers, the linear amplifier cancels the ripple associated with the switching amplifier. This topology is an intermediate solution between pure linear and pure class-D power amplifiers. Most of the output current is delivered by switched-mode amplifier and the linear amplifier only supplies the current to compensate for the ripple due to switching operation. In this configuration, the linear amplifier should have a high gain and a wide bandwidth with low output impedance in order to achieve a high noise rejection. And the current-sensing block should have high accuracy with much faster response than the switching frequency.

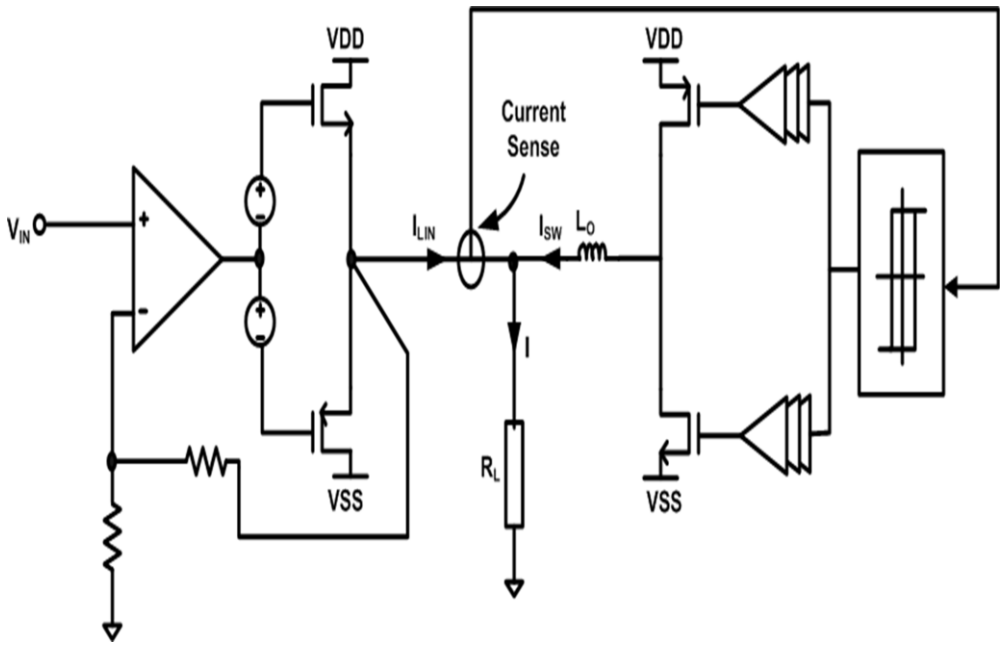

Figure 1-13: The linear-switch mode combination amplifier.

Recently, Pulse Density Modulated (PDM) class-D amplifiers based on analog ΣΔ modulators with high-pass noise-shaping characteristics have been introduced as an alternative scheme for controlling the switching power stage [13]-[16]. PDM based class-D amplifiers, as shown in Figure 1.14, can eliminate harmonic distortion caused by the nonlinearity of the carrier and have the characteristic of shaped quantization noise, achieving a lower total harmonic distortion (THD) performance. PDM modulation also minimizes EMI because it spreads out the spectral energy of the output signal over a wide range of frequencies [13], [17]. A PDM-based class-D amplifier is closely related to this thesis.

1.7 Thesis Organization

The outline of the dissertation is as follows. Chapter 2 introduces the concept of

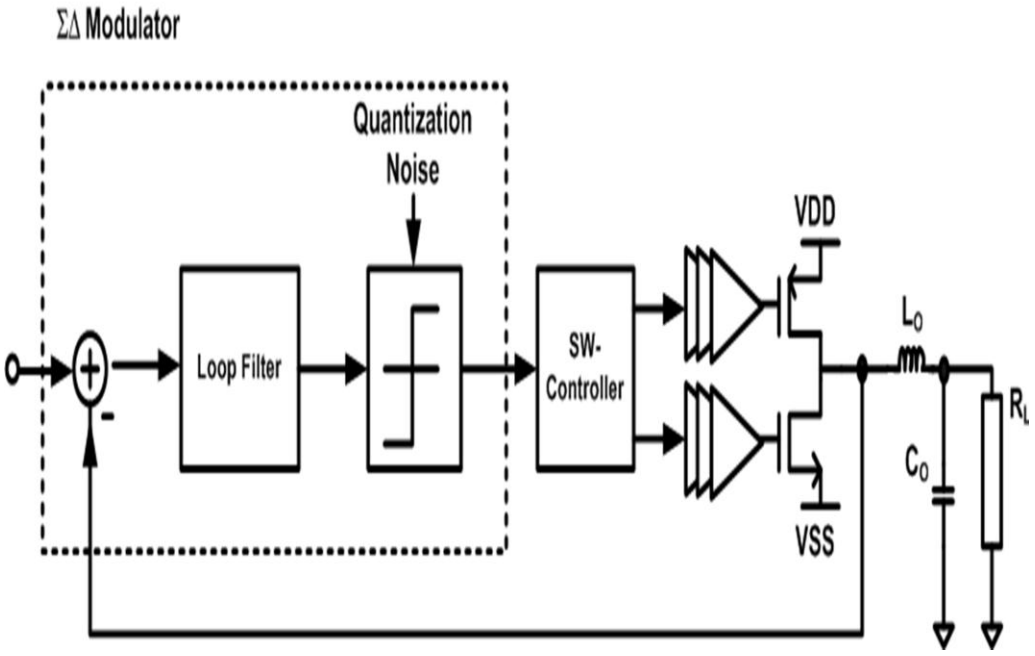

Figure 1-14: PDM based class-D amplifier.

modulation scheme and typical ΣΔ modulators. In chapter 3, system level implementation of the proposed class-D amplifier is provided. Chapter 4 describes circuit level implementation. Characterization results are presented in Chapter 5, and conclusions are provided in chapter 6.

2 MODULATION SCHEMES AND OVERVIEW OF ΣΔ MODULATORS

2.1 Pulse Width Modulation (PWM)

PWM compares the input signal to a triangular or saw -tooth waveform that runs at a fixed carrier frequency. It generates a stream of pulses at the carrier frequency, and the duty cycle of the PWM pulse is proportional to the amplitude of the input signal. Therefore, PWM has two important advantages. The first advantage is that it encodes a signal into a few discrete levels, with the information represented in pulse duty ratios. The second advantage is the ability to recover the signal from its discrete-level form with a passive filter [18]. Two main forms of PWM are the natural pulse width modulation (NPWM) and the uniform pulse width modulation (UPWM) as shown in Figure 2-1. NPWM is basically an analogue process. Thus, it implies a natural selection of the sampling points. UPWM defines the pulse widths from regular samples of the signal, and it is suitable for a digital system [19]. Figure 2-2 shows the spectrum of PWM when the

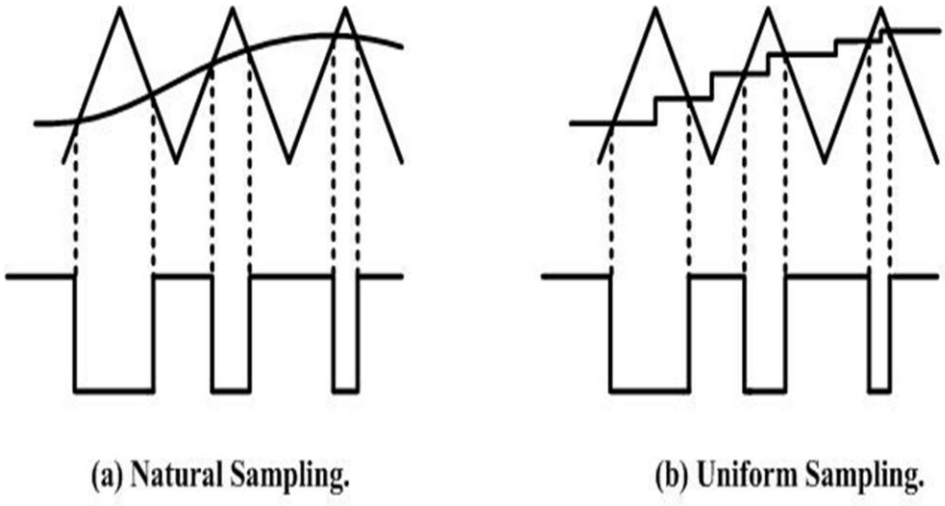

Figure 2-1: Natural sampling and uniform sampling.

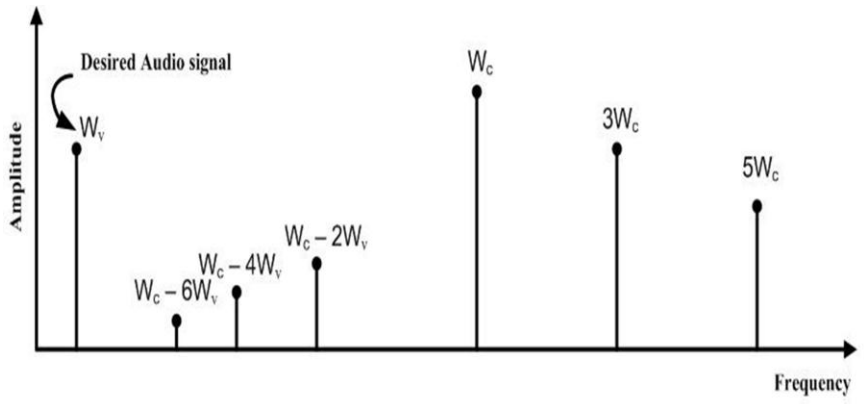

Figure 2-2: Spectrum of PWM.

frequency of the input signal is ω_V and the carrier frequency is ω_C. Fourier series expressions are given by equation (2.1) for NPWM and equation (2.2) for UPWM, where *M* is a modulation depth, *m* is a carrier harmonic number, *H* is pulse height, *n* is a signal harmonic number, and J_n is a Bessel function of the first kind with integer order *n*. The Fourier series of a typical PWM signal consists of four components; the first component is the DC component and the second is the modulating signal. The third is the carrier and its associated harmonics. The last is the intermodulation products between the fundamental and harmonic components of the modulating signal and the carrier.

$$f_N(t) = \frac{HM\cos(n\omega_v t)}{2} + \sum_{m=l}^{\infty}\sum_{n=-\infty}^{\infty}\frac{2HJ_n(M\pi m/2)}{\pi m}\sin\left((m+n)\frac{\pi}{2}\right)\cos(n\omega_v t + n\omega_c t) \quad (2.1)$$

$$f_U(t) = \sum_{n=l}^{\infty} 2HJ_n\left(\frac{Mn\omega_v}{2\omega_c}\right)\sin\left(n\frac{\pi}{2}\right)\cos\left(n\omega_v t - \frac{n\pi\omega_v}{2\omega_c}\right) + \sum_{m=l}^{\infty}\sum_{n=-\infty}^{\infty}\frac{2HJ_n\left(M\pi/2\left(m+\frac{n\omega_v}{\omega_c}\right)\right)}{\pi\left(m+\frac{n\omega_v}{\omega_c}\right)}\sin\left((m+n)\frac{\pi}{2}\right)\cos\left(n\omega_v t + m\omega_c t - \frac{n\pi\omega_v}{\omega_c}\right) \quad (2.2)$$

In the ideal PWM-based class-D amplifier, the first term (DC component) is eliminated by a bridge-tied-load differential drive configuration. The third term and the

last term are effectively removed by the low pass filter. As a result, the second term (the modulation signal) is just used in class-D amplifier, and THD of PWM generated from the carrier is ideally zero. The spectral characteristics of the output signal depend on the type of carrier used for PWM generation.

However, it is very difficult to obtain the ideal triangular carrier without nonlinearity in low-voltage PWMs. The nonlinearity of the carrier introduces the harmonic distortion in the PWM-based class-D amplifier.

2.2 Pulse Density Modulation (PDM)

PDM is generally accomplished with a sigma-delta (ΣΔ) modulator. Although a fast switching rate restricts the frequency range of the sigma delta modulator for class-D audio amplifiers, this modulation technique can avoid the nonlinear problem caused by

Table 2-1

Comparison of PWM and PDM

	PWM	PDM
Pros	- Low implementation complexity - Low switching frequency - High power efficiency	- High pass noise shaping characteristic - EMI advantage
Cons	- EMI issue (the concentrated spectral energy in the switching frequency and its harmonics) - Nonlinearity caused by the carrier frequency	- High switching frequency (trade-off high THD performance with the power efficiency) - Design complexity - Stability issue

the carrier and achieve a high THD performance. Also, PDM modulation minimizes EMI because it spreads out the spectral energy of the output signal over a wide range of frequencies [20]. Table 2-1 shows a comparison of PWM and PDM.

2.3 Overview of ΣΔ Modulators

2.3.1 Over-Sampled Noise-Shaping

ΣΔ modulators have the characteristic of over-sampling input signal and shaping of the quantization noise that is realized using a closed-loop feedback around a quantizer. Therefore, signal-to-noise ratio (SNR) can be improved compared to unshaped converters employing oversampling [21]. The input signal feeds to the quantizer through integrators, and the quantized output signal feeds back to obtain the error signal that is the difference between the input and the feedback signal. The error signal accumulates in integrator and finally corrects itself because the feedback architecture forces the average value of the quantized signal to track the average input signal. The basic structure and linear model of

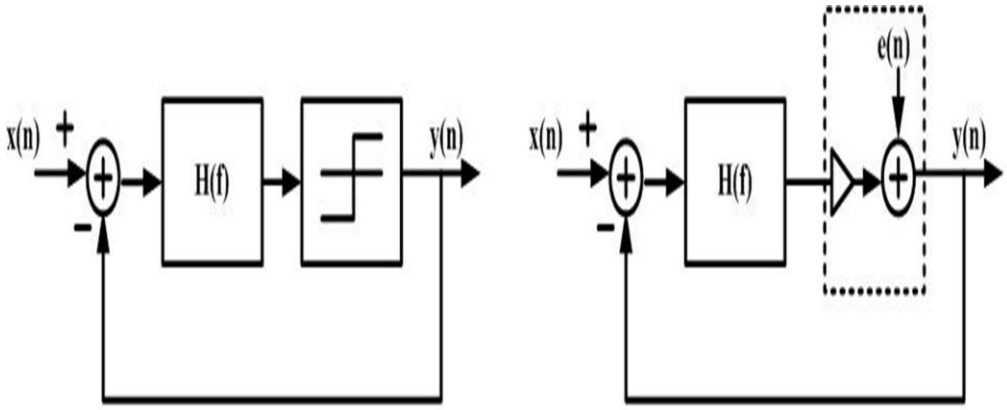

Figure 2-3: Basic structure and linear model of ΣΔ modulator.

ΣΔ modulator are shown in Figure 2.3. It consists of a loop-filter *H(f)* and a 2-bit quantizer. In a linear model of a quantizer, the output waveform is generated by multiplying the input signal with the quantization gain *k* and adding the quantization error *e(n)*. The quantization error can be approximately a random number and represented by a white noise source. It uniformly distributes between -Δ/2 and Δ/2 and is independent of the input signal. Δ is the step size of the output waveform. Figure 2-4 shows the probability density function of the quantization error. The total quantization noise power, which is independent of the sampling frequency f_s, can be calculated as

$$\begin{aligned} e_q^2 &= \int_{-\infty}^{\infty} e^2 \, pdf_e \\ &= \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 de \\ &= \frac{\Delta^2}{12} \end{aligned} \tag{2.3}$$

The output in Figure 2.3 can be represented as

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{2.4}$$

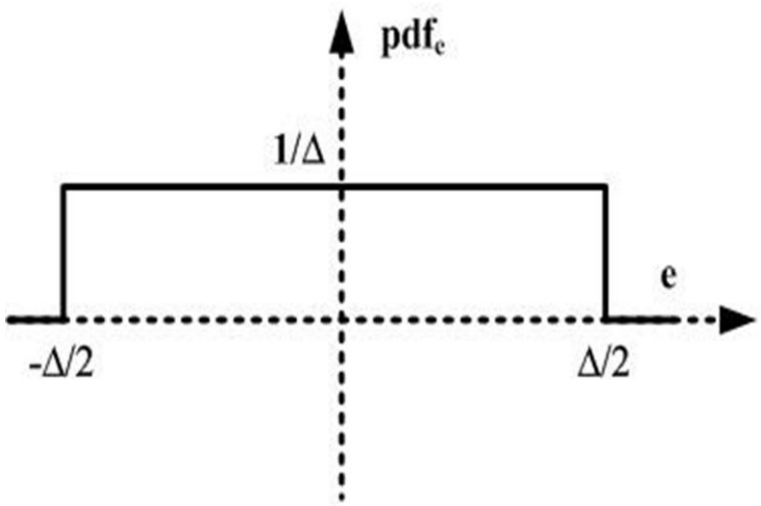

Figure 2-4: Probability density function (pdf) of the quantization error.

where *X(z)* and *E(z)* are the Z-domain representation of the input signal and quantization error. The signal and noise transfer functions can be respectively calculated as

$$STF(z) = \frac{H(z)k_q}{1+H(z)k_q} \tag{2.5}$$

$$NTF(z) = \frac{1}{1+H(z)k_q} \tag{2.6}$$

where k_q is a quantizer gain.

If the loop filter transfer function *H(z)* is designed to have a large gain within the desired signal band and a small gain outside the band to suppress the noise, the signal and noise transfer functions can be calculated as

$$STF(z) = 1 \tag{2.7}$$

$$NTF(z) = \frac{1}{H(z)k_q} << 1 \tag{2.8}$$

Therefore, the signal can be passed directly to the ΣΔ modulator, and the noise is greatly reduced inside the signal band. If the loop filter *H(z)* is designed by an integrator in a first-order low-pass ΣΔ modulator, its transfer function is represented as

$$H(z) = \frac{z^{-1}}{1-z^{-1}} \tag{2.9}$$

The signal and noise transfer function can be calculated as

$$STF(z) = z^{-1} \tag{2.10}$$

$$NTF(z) = 1-z^{-1} \tag{2.11}$$

The input signal is passed to ΣΔ modulator with a delay of one clock cycle, and the quantization noise is passed through a first-order high-pass filter [21]. Therefore, the

quantization noise is shaped. The peak SNR of the first-order ΣΔ modulator can be represented as

$$SNR = 6.02B - 3.41 + 30\log(OSR) \tag{2.12}$$

where B is the number of bits, and OSR is the oversampling ratio (OSR). The peak SNR of an oversampled modulator results in a 0.5-bit increase when OSR is doubling. However, from equation (2.12), a 1.5-bit increase (or 9-dB increase) in SNR can be obtained when OSR is doubling.

2.3.2 Performance Increase in ΣΔ Modulators

High-order noise shaping characteristics can be achieved by high-order loop filter, *H(z)*. The transfer function of N^{th}-order modulator is represented as

$$Y(z) = z^{-N}X(z) + \left(1 - z^{-1}\right)^{N} E(z) \tag{2.13}$$

$$NTF(z) = \left(1 - z^{-1}\right)^{N} \tag{2.14}$$

NTF plots of the higher order are shown in Figure 2.5, where *z* is equal to $e^{(j2\pi f/fs)}$ and N = 1, 2, and 3. The increase of the order of the modulator reduces the in-band noise through higher-order filtering and significantly improves the dynamic range (DR). However, the high-frequency gain of the higher-order NTF increases rapidly as shown in Figure 2.5. The higher gain of the NTF amplifies the high-frequency quantization noise and the amplified high-frequency quantization noise overloads the quantizer input. It results in instability. Therefore, to ensure the stability, it requires the reduction of the loop-gain or the maximum input signal level. If poles are introduced into pure N^{th}-order differentiators, *NTF(z)*, by using Butterworth high-pass response, it can maximally flatten the high-frequency region of *NTF(z)* and improve the stability due to the reduction in the high-frequency gain of NTF. Equation (2.15) shows the modified NTF by adding *D(z)*.

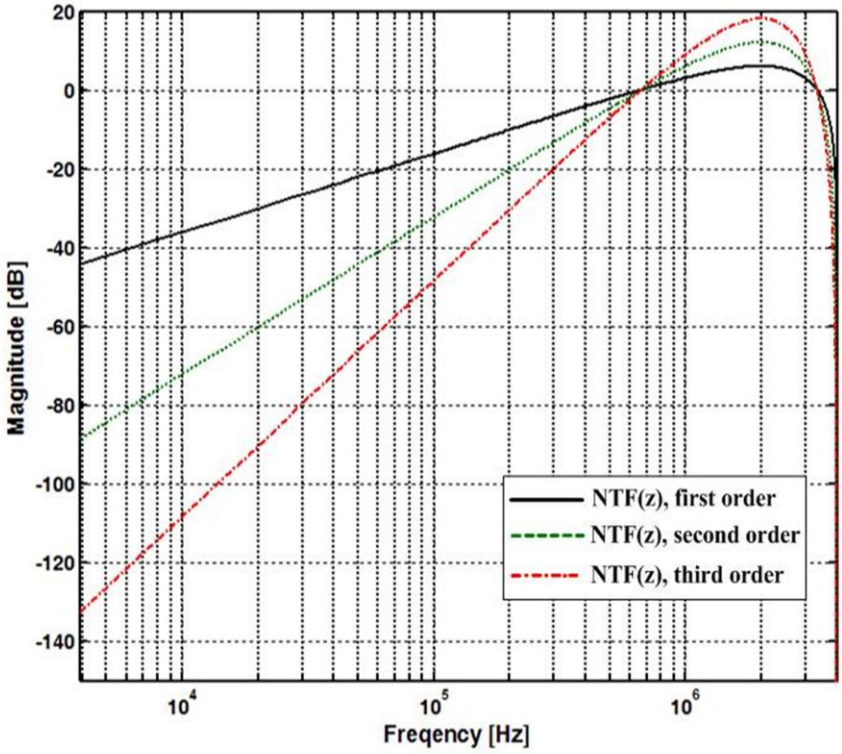

Figure 2-5: NTF (z) of N^{th}-order ΣΔ modulator.

$$NTF(z) = \frac{(1-z^{-1})^n}{D(z)} \tag{2.15}$$

The comparison between the pure 5th-order NTF and Butterworth NTF is shown in Figure 2-6. The 30-dB high frequency gain of the pure 5th-order NTF is reduced by the 3-dB gain in the Butterworth NTF in Figure 2-6. Another advantage of the Butterworth high-pass filter is that the poles are low Q instead of high-Q poles (poles very closed to the unit circle). Hence, it tends to be less susceptible to oscillations caused by input signal that are at the same frequency as the poles [22].

Increasing the OSR reduces the in-band noise power by 9 dB per octave as aforementioned. However, if the signal bandwidth of the input signal is a constant, the sampling frequency must be increased for higher OSR. It requires faster circuits and an

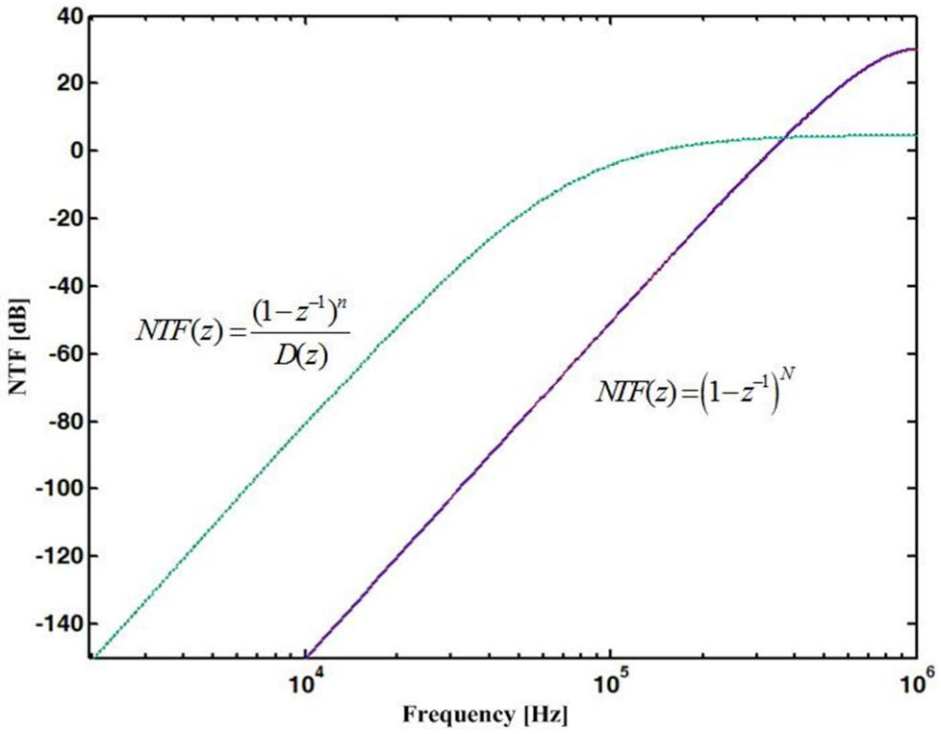

Figure 2-6: NTFs of a 5th-order pure differentiator and Butterworth high-pass filter.

increasing power consumption. Therefore, the increase of the OSR has the limitation and is usually kept as low as possible.

A multibit quantization can improve the performance of ΣΔ modulators because the quantization error is reduced due to the decrease of the step size of the quantizer. A multibit quantization tends to assist the stability of higher order modulators. Its gain can be approximately represented as unity, and it reduces the requirement of loop gain scaling. However, the linearity of the feedback DAC can restrict the performance of modulators because its error directly feeds into the input of the modulator. For a one-bit quantizer, there is no problem regarding the linearity of a feedback DAC, since a two-level DAC is intrinsically linear [23].

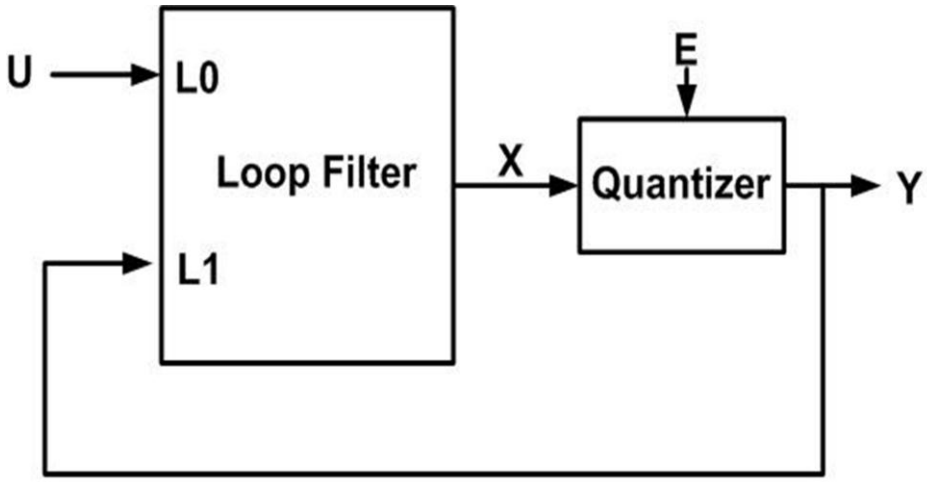

Figure 2-7: General single-loop ΣΔ Architecture.

2.3.3 Single-Loop, Single-Bit, Higher Order ΣΔ Modulators

Single-loop architectures are introduced to review the fundamentals of ΣΔ loop filter design in this section. All ΣΔ feedback topologies consist of the STF and the NTF [22]. In general, single-loop ΣΔ architectures can be also described as shown in Figure 2-7. The loop filter $L_0(z)$ and $L_1(z)$ can be represented as functions of the loop parameters from the implemented architecture. Single-loop, single-bit ΣΔ modulators are widely used due to their simplicity and insensitivity with regard to circuit imperfections [24]. Three single-loop architectures are commonly exploited to implement the single-loop structure. The first single-loop structure is the chain of integrators with distributed feedback. The second is the chain of integrators with weighted feedforward summation. The last is the distributed feedback structure with local resonator feedback loops [22]. The chain of integrators with distributed feedback is shown Figure 2-8. The output $Y(z)$ is fed back to each of the integrators through each gain stage a_1-a_4. Its loop filters are represented as

$$L_0(z) = \frac{b_1}{(z-1)^4} \tag{2.16}$$

$$-L_1(z) = \frac{a_1}{(z-1)^4} + \frac{a_2}{(z-1)^3} + \frac{a_3}{(z-1)^2} + \frac{a_4}{(z-1)} \tag{2.17}$$

Therefore, NTF can be given by

$$NTF(z) = \frac{(z-1)^4}{(z-1)^4 + a_4(z-1)^3 + a_3(z-1)^2 + a_2(z-1) + a_1} \tag{2.18}$$

All zeros of NTF are at z =1. In other words, the zeros are all at DC in the frequency-domain. The main advantage of this architecture is that it can achieve nearly flat passband response by using the Butterworth filter as in the above-mentioned equation 2.15. The main disadvantage of this architecture is that the integrator outputs contain a significant amount of the input amplitude as well as the filtered quantization noise. It requires the large swing capabilities of integrators or a scaling down of coefficients.

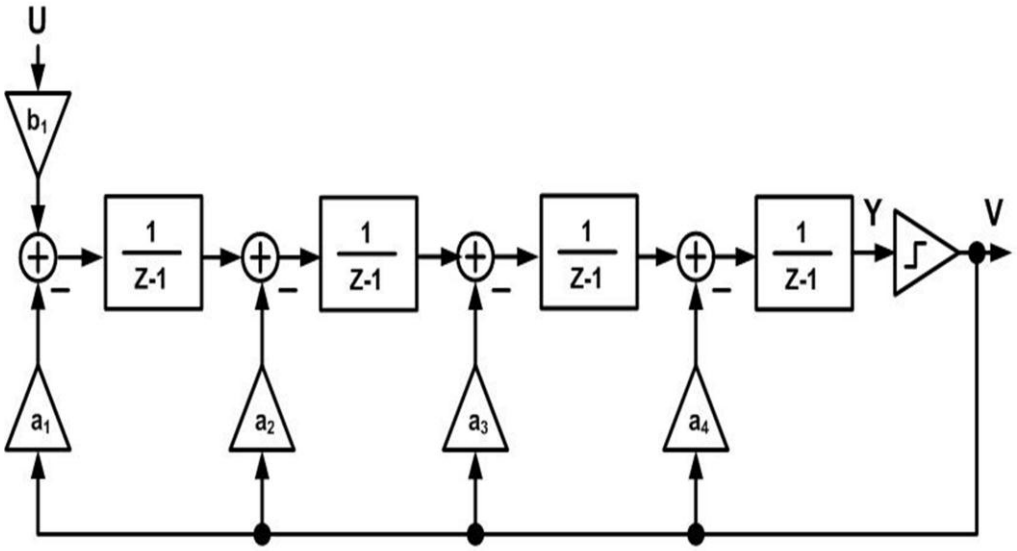

Figure 2-8: Chain of integrators with distributed feedback.

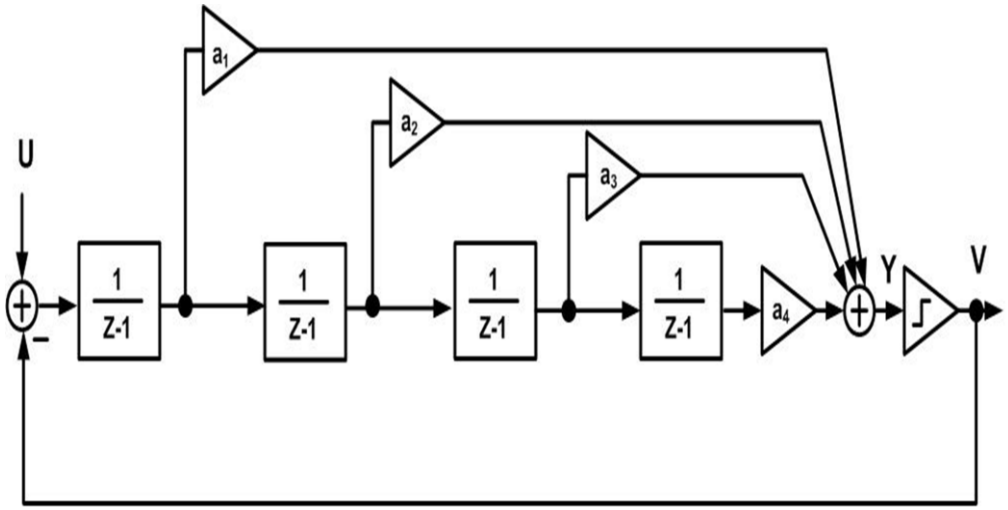

Figure 2-9: Chain of integrators with weighted feedforward summation.

Hence, the chip size and power consumption can be increased. The circuit noise contribution can be also increased because small-scaling coefficients are designed by a small-sampling capacitor in discrete-time (DT) SC integrators or large resistance in continuous-time (CT) integrators. The other disadvantage of this architecture is that the STF is dependent on the NTF. If the NTF is optimized, the STF is fixed because the loop filter for the signal and noise are identical.

The chain of integrators with weighted feedforward summation is shown in Figure 2-9. The loop filters of this architecture are represented as

$$L_0(z) = -L_1(z) = \frac{a_1}{(z-1)} + \frac{a_2}{(z-1)^2} + \frac{a_3}{(z-1)^3} + \frac{a_4}{(z-1)^4} \qquad (2.19)$$

This architecture also shows that the STF is fixed if the loop filter is determined for optimum noise shaping. The main advantage of this architecture is that the outputs of integrators do not contain the significant amount of input signal and only operates on the quantization noise.

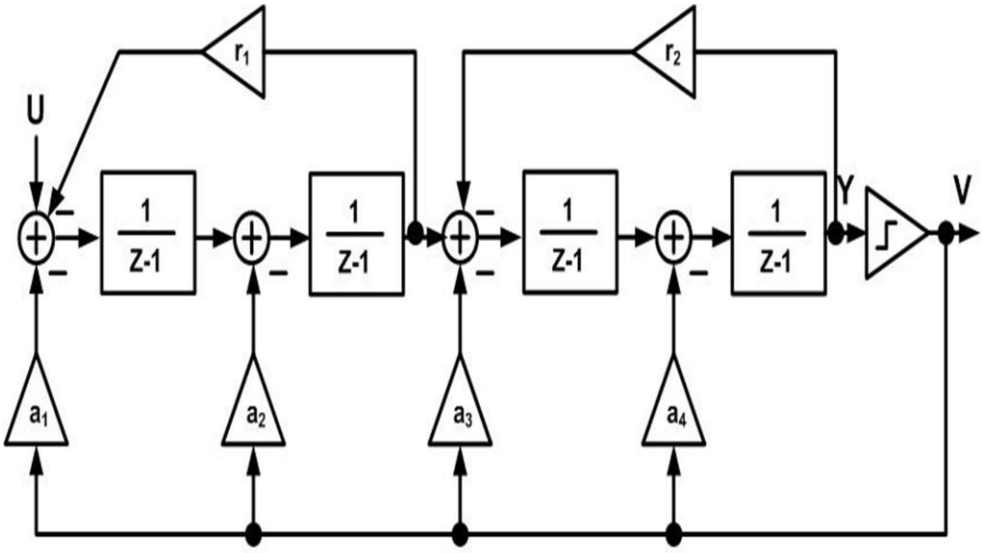

Figure 2-10: Chain of integrators with distributed feedback and local resonator feedbacks.

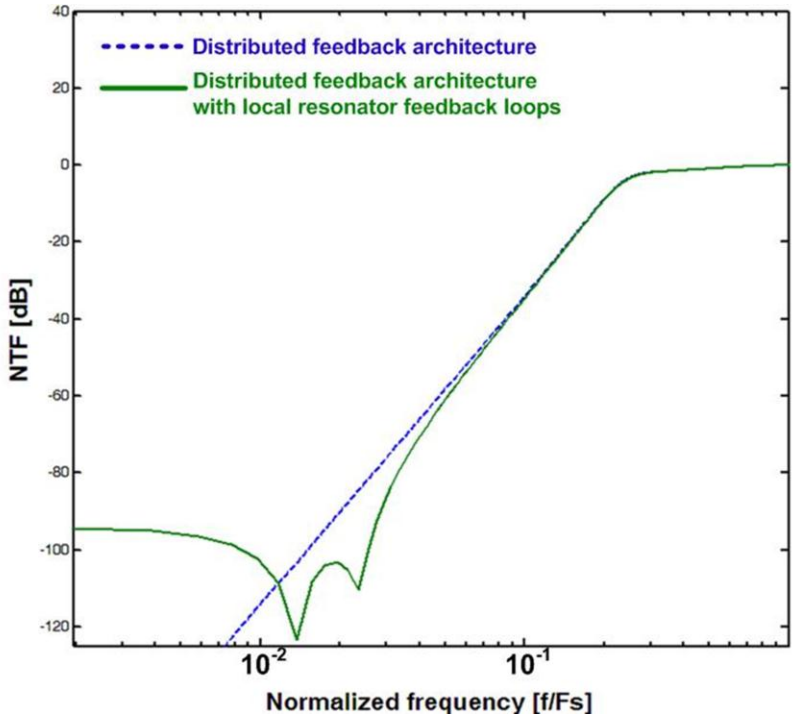

Figure 2-11: The NTFs of distributed feedback architecture without / with local resonator feedback loops.

Therefore, it does not require the small scaling of coefficients and the large output swing

of integrators. The disadvantage of this architecture is that the STF contains peaking at high frequencies. Input signals at these frequencies can make modulators with this architecture overload. Thus, an additional pre-filter would be required in the input of the modulator to prevent input signals at these frequencies [22].

The distributed feedback architecture with local resonator feedback loops is shown in Figure 2-10. Additional local resonators in the distributed feedback or feedforward summation architectures can spread the NTF zeros over the signal bandwidth from DC due to generating pairs of complex zeros. This method can suppress the in-band quantization noise more as shown in Figure 2-11.

2.3.4 Stability of ΣΔ Modulators

The main drawback of higher-order ΣΔ modulators is instability for higher input

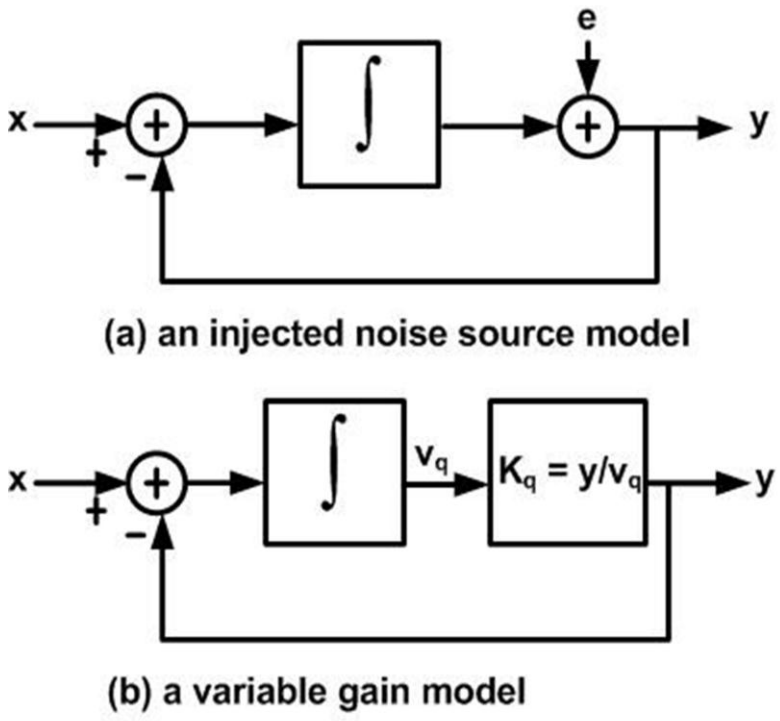

Figure 2-12: Quantizer models.

signal amplitude if all zeros of their NTF (z) are at 1. If the modulator is instable, the amplitude of the internal signal of integrators is rapidly increased, and this results in oscillations at low frequency. Therefore, the loop gain is generally reduced by filter-scaling to increase the stability. The stability of ΣΔ modulators can be analyzed by using the variable quantizer gain model instead of the injected noise source model as shown in Figure 2.12. Using the injected noise source model, the noise shaping characteristic which is the benefit of ΣΔ modulators can be obtained from the transfer function between the noise input and output. However, this model does not give any information related to the stability of the modulator [25]. The variable quantizer gain model is that the quantizer gain k_q is variable and dependent on the input signal of the quantizer as given by equation (2.20).

$$k_q = \frac{y}{v_q} \tag{2.20}$$

where y is the output signal and v_q is the input to the quantizer. A modulator's transfer function with the variable quantizer gain model can be obtained and root locus techniques can be exploited to analyze the modulator stability. The use of the variable quantizer gain model generates a root locus where roots move along the locus as the quantizer gain changes. If roots are driven outside the unit circle, the modulator is unstable or has limit cycles. Figure 2-13 shows the root locus plot of a third-order modulator with distributed feedback. When a quantizer gain is less than k_{crit} = 0.54, the modulator is unstable because the input signal levels of quantizer are large, k_q falls, and poles move outside the unit circle.

The above root locus method is a linear approach to analyzing the nonlinear system. Therefore, the stability analysis of ΣΔ modulators should be confirmed by behavioral simulations as well as the variable quanitzer gain model [23].

2.3.4 DT Vs. CT ΣΔ Modulators

Most of the ΣΔ modulators have been designed in DT circuits, like using the switched capacitor (SC) technique during the last decades. DT ΣΔ modulators employing the SC technique can be designed with a high degree of linearity and can be easily simulated and implemented. However, its maximum clock rate is limited by the OTA bandwidth and slew rate [26]. The advantage of CT ΣΔ modulators is that sampling operation is inside the ΣΔ loop, unlike DT ΣΔ modulators, where a sample-and-hold (S/H) circuit is at the input of modulators, as shown in Figure 2.14. As a result, all non-

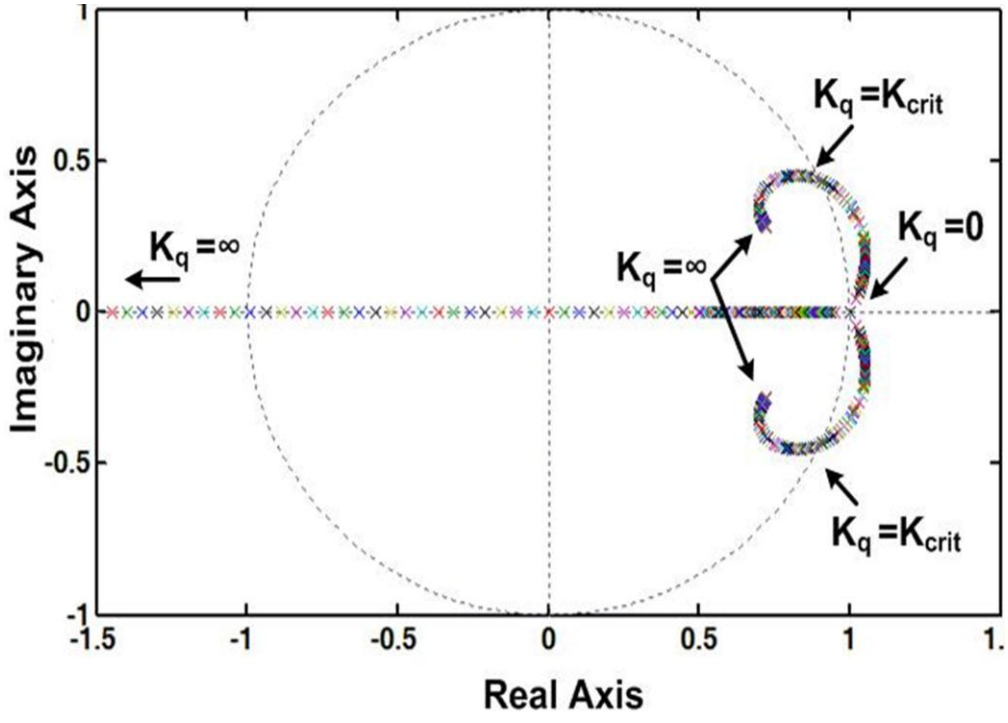

Figure 2-13: Root locus of a third-order modulator with distributed feedback.

idealities of the sampling process can be noise-shaped in CT ΣΔ modulators, while the error from a S/H circuit adds to the input signal in the DT ΣΔ modulators [26]. CT ΣΔ modulators also have an implicit antialiasing filtering due to the shift of the sampling operation. Hence, CT ΣΔ modulators can relax the required performance of a front-end AAF or eliminate the necessity of a front-end AAF [23]. The comparison between DT and CT ΣΔ modulators is shown in Table 2-2.

Table 2-2

Comparison of DT and CT ΣΔ Modulator

	DT	CT
Pros	- Low sensitivity to clock jitter - Low sensitivity to DAC waveform - Highly linear SC integrator - Capacitive loads only - Compatible with VLSI CMOS processes - Accurate pole-zero locations that are set by capacitor ratios - Easily simulated	- Implicit anti-aliasing filter - Relaxed op amp speed requirements - High-speed operation - Less glitch sensitive - Easy to breadboard - Less digital switching noise - SNR is not limited by cap size
Cons	- Large capacitors required for high SNR (kT/C noise) - Large spike currents and glitches drawn by capacitors - Sampling operation at the outside of the ΣΔ loop	- RC time variation - Needs large capacitors, linear high-value resistors, low-noise op amps - Sensitivity to clock jitter, noise, and switching characteristics of 1-bit feedback waveform - Loop filter does not scale with sampling frequency

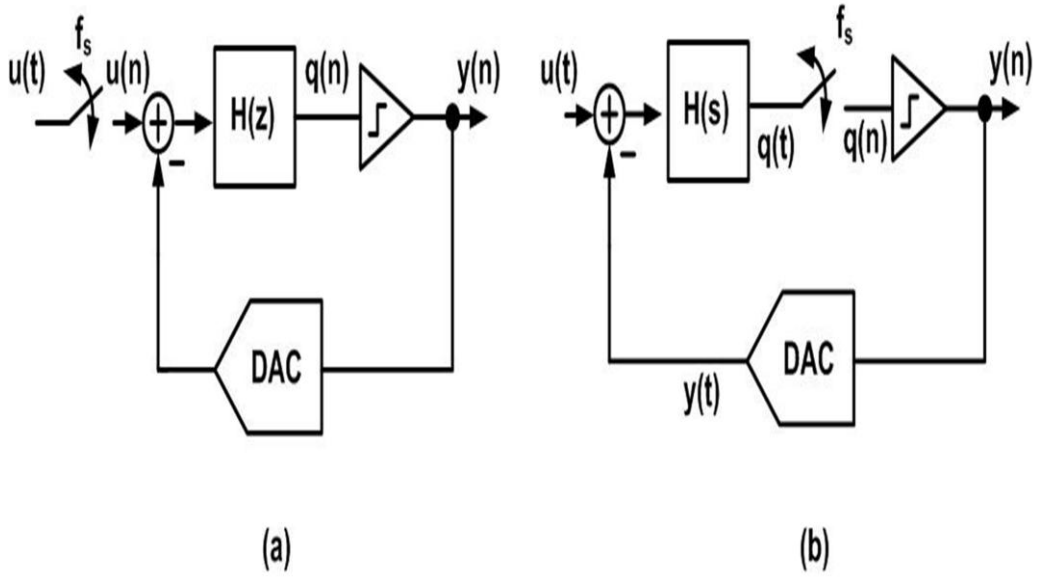

Figure 2-14: Block diagram of (a) DT and (b) CT modulators.

2.3.5 DT-to-CT Conversion

A number of software tools and architectures are developed and presented in the design of DT ΣΔ modulators. If the procedure of the design of the CT ΣΔ modulators begins in the DT-domain, the required overall design time can be reduced. DT integrators can be converted into CT integrators if the DT-to-CT conversion is used to transfer the coefficients from DT modulators to CT modulators. The most common methods of DT-to-CT conversion are the impulse-invariant transformation and the modified Z-transform. The overall loop transfer function of the CT modulator can be considered as the DT transfer function because the internal quantizer of the CT modulator is clocked and performs the sampling operation inside loop. Thus, the equivalent z-domain transfer function *H(z)* of the loop transfer function from the output of the quantizer to its input can be defined as Figure 2-15 at the sampling instants [28].

Its relationship can be represented as

$$Z^{-1}\{H(z)\} = \mathcal{L}^{-1}\{R_{DAC}(s)H(s)\}\Big|_{t=nT_s} \tag{2.21}$$

In the time domain,

$$h(n) = \left[r_{DAC}(t) * h(t)\right]\Big|_{t=nT_s} = \int_{-\infty}^{+\infty} r_{DAC}(\tau)h(t-\tau)d\tau\Big|_{t=nTs} \tag{2.22}$$

where $r_{DAC}(t)$ is the impulse response of the specific DAC such as return to-zero (RZ), non-return to-zero (NRZ), and half-delay return to-zero (HZ) DAC as shown in Figure 2.16. This DT-to-CT transformation is called the impulse-invariant transformation. The specific rectangular DAC pulse with magnitude 1 can be defined as

$$r_{DAC}(t) = \begin{cases} 1, & \alpha \le t \le \beta, 0 \le \alpha < \beta \le 1 \\ 0, & otherwise. \end{cases} \tag{2.23}$$

Its Laplace transform of (2.23) is

$$R_{DAC}(s) = \frac{e^{-\alpha s} - e^{-\beta s}}{s} \tag{2.24}$$

If R_{DAC} (s) is NRZ DAC, $(\alpha,\beta) = (0, 1)$ in (2.23).

For second-order modulator ($N = 2$) with NRZ feedback DAC pulse, substituting

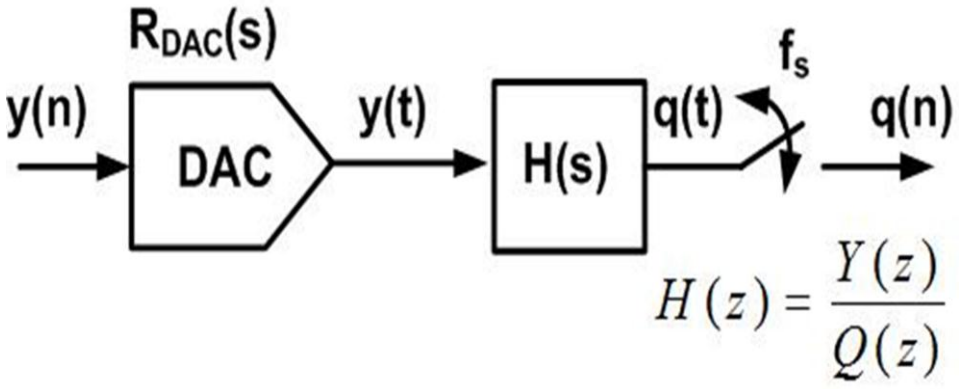

Figure 2-15: CT ΣΔ open loop block diagram.

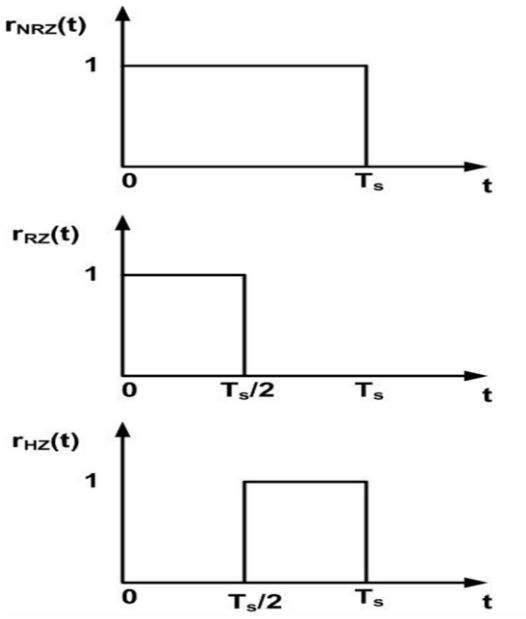

Figure 2-16: NRZ, RZ, and HZ DAC feedback impulse response.

(2.14) in (2.6) results in the DT loop filter transformation as shown in equation (2.25)

$$\begin{aligned} H(z) &= \frac{2z-1}{(z-1)^2} \\ &= \frac{2}{z-1} + \frac{1}{(z-1)^2} \end{aligned} \tag{2.25}$$

Applying the first row of Table 2-3 to the first term of (2.25) and the second row to the second term with $(\alpha,\beta) = (0, 1)$ results in the equivalent s-domain transfer function *H(s)*:

$$H(s) = \frac{2}{sT_S} + \frac{1-0.5sT_S}{(sT_S)^2} \quad \rightarrow \quad H(s) = \frac{1+1.5sT_S}{(sT_S)^2} \tag{2.26}$$

Another DT-to-CT transformation is the modified *Z*-transformation [28], [30]. In this method, the discrete system behavior is not considered in a sampling instant but at all instants of time. Thus, the modified Z-transformation is useful in determining the equivalent CT loop filter with arbitrary feedback DAC waveforms [31]. It can be expressed as

$$H(z) = \sum_i Z_{mi} \left\{ H(s) R_{DAC}(s) \right\} \tag{2.27}$$

The equivalent s-domain transfer function *H(s)* can be determined in the same way as shown during the impulse-invariant transform by using equation (2.27).

The direct design method of a CT loop filter from the desired noise-transfer function is explained in the following statement. If the quantizer gain, *k*, is assumed to unity for the simplicity, the *NTF(s)* from the noise source to the modulator output is given as

$$NTF(s) = \frac{A(s)}{B(s)} = \frac{1}{1 + H(s)} \tag{2.28}$$

where *H(s)* is the CT loop filter. From (2.28), *H(s)* is derived as

$$H(s) = \frac{B(s) - A(s)}{A(s)} \tag{2.29}$$

Next, the loop filter can be easily designed by using the MATLAB Signal Processing Toolbox command:

[B, A] = butter (N, Wn, ′high′, ′s′)

where *N* is the filter order, *Wn* is the stopband edge frequency, and ′high′ and ′s′ design a CT high-pass filter. It is important to consider a trade-off between the ΣΔ modulator noise attenuation and stable amplitude range in the feedback filter design because increasing of the high frequency gain of NTF causes the maximal stable amplitude to reduce [32].

Table 2-3

s-domain Equivalences for *z*-domain Loop Filter Poles [23], [29]

z-domain	*s*-domain equivalents with T_s
$\frac{1}{(z-1)}$	$\frac{\omega_0}{s}$, $\omega_0 = \frac{1}{T_s(\beta-\alpha)}$
$\frac{1}{(z-1)^2}$	$\frac{\omega_1 s+\omega_0}{s^2}$, $\omega_0 = \frac{1}{T_s^2(\beta-\alpha)}$, $\omega_1 = \frac{0.5(\alpha+\beta-2)}{T_s(\beta-\alpha)}$
$\frac{1}{(z-1)^3}$	$\frac{\omega_2 s^2+\omega_1 s+\omega_0}{s^3}$, $\omega_0 = \frac{1}{T_s^3(\beta-\alpha)}$, $\omega_1 = \frac{0.5(\alpha+\beta-3)}{T_s^2(\beta-\alpha)}$ $\omega_2 = \frac{1}{12}\frac{[\beta(\beta-9)+\alpha(\alpha-9)+4\alpha\beta+12]}{T_s(\beta-\alpha)}$
$\frac{1}{(z-1)^4}$	$\frac{\omega_3 s^3+\omega_2 s^2+\omega_1 s+\omega_0}{s^4}$, $\omega_0 = \frac{1}{T_s^4(\beta-\alpha)}$, $\omega_1 = \frac{0.5(\alpha+\beta-4)}{T_s^3(\beta-\alpha)}$ $\omega_2 = \frac{1}{12}\frac{[(\beta-\alpha)^2+2\beta\alpha-12(\beta-\alpha)+22]}{T_s^2(\beta-\alpha)}$, $\omega_3 = \frac{1}{12}\frac{[\beta^2(\alpha-2)+\alpha^2(\beta-2)-8\alpha\beta+11(\beta+\alpha)-12]}{T_s(\beta-\alpha)}$

2.3.6 Nonidealities in CT ΣΔ Modulators

In practice, there are certain nonidealities that decline the performance of ΣΔ modulators. These include a finite op amp gain, a finite gain-bandwidth product (GBW), slew rate, non-linearity amplifier gain, circuit noise, time-constant error of integrator, and integrator nonlinearity, etc [23] [29].

Finite op amp gain

Figure 2-17 shows a typical schematic of an active RC-integrator. The dc gain of an integrator is ideally infinite. Thus, the integrator transfer function is given as

$$TF_{ideal} = \frac{\frac{1}{RC}}{s\left(1+\frac{1}{A(s)}\right)+\frac{1}{A(s)RC}} \approx \frac{1}{sRC} \tag{2.30}$$

However, the op amp gain is limited by circuit constraint. The transfer function of the integrator with the finite dc gain, A_{dc}, and for a frequency-independent is given as

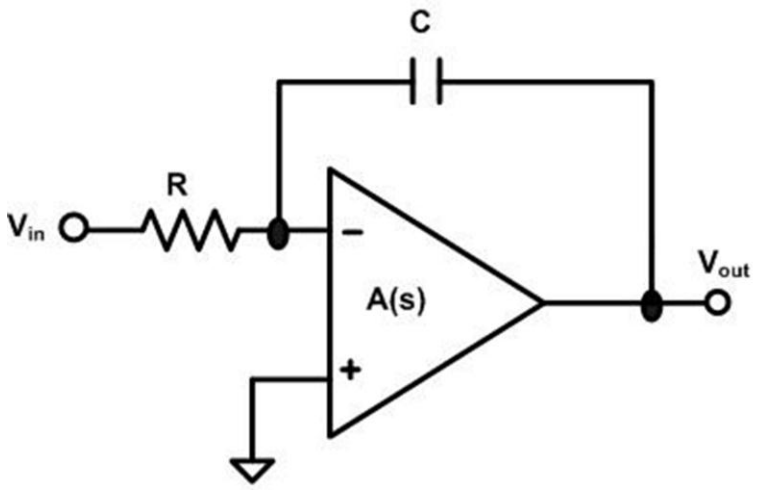

Figure 2-17: Active RC integrator with single pole amplifier.

$$TF = \frac{\frac{1}{RC}}{s\left(1+\frac{1}{A_{dc}}\right)+\frac{1}{A_{dc}RC}} \approx \frac{\frac{1}{RC}}{s+\frac{1}{A_{dc}RC}} \tag{2.31}$$

The poles of the loop filter are the zeros of the NTF. Thus, all zeros of NTF are pushed away from dc. It causes to reduce the amount of attenuation of the quantization noise in the baseband and it is known as leaky integration. If the integrators have $A_{dc} \approx OSR$, the SNR will be about 1dB worse than if the integrators had infinite dc gain [33] [34].

Finite gain bandwidth product

A GBW of the op amps introduces non-dominant poles into the integrator transfer function. The finite GBW in CT ΣΔ modulators causes integrator gain errors. The unit-gain bandwidth of the op amps should be at least an order of magnitude higher than the sampling rate [23]. The GBW in cascaded DT implementations is required to a factor of at least five or ten times the sampling frequency due to their increased sensitivity to nonidealities [35]. However, the GBW in CT ΣΔ modulators can be decided lower than the sampling frequency [36].

Finite slew rate

ΣΔ modulators are also affected by finite slew rate (SR) of the op amps. The finite SR causes distortion as well as an increase of the noise floor [37]. In DT implementations, signal transitions are very fast SC-pulse. Thus, the finite SR can induce incomplete setting and yield a gain error. In CT modulators, the specifications of the SR can be relaxed because the various signals are changing much more slowly depending on the feedback waveform [23] [38].

Non-linearity of amplifier gain

If the gain of op amps depends on its input signal, harmonic distortion is shown in the output spectrum [39]. The dominant source of the distortion is the input pairs of the first op amps because the non-linear behaviors of later-stage are divided by the gains of the previous stages when referred to the input. If the op amp for the first integrator stage has low distortion, the third-harmonic distortion of the ΣΔ modulator is given as

$$HD3 \approx \frac{g_3}{16g^4} \cdot \left(\frac{1}{R_{in}} + \frac{1}{R_{dac}} \right) \cdot \left(\frac{V_{in}}{R_{in}} \right)^2 \tag{2.32}$$

with

$$g = g_1 - \frac{1}{2}\left(\frac{1}{R_{in}} + \frac{1}{R_{dac}} \right) \tag{2.33}$$

where R_{in} is the input resistor, R_{dac} is the feedback DAC resistor, and g_1 and g_3 are the linear and third harmonic transfer coefficients, respectively [40]. However, if the op amp has the large distortion, the expressions for the linear and non-linear transfer coefficients can be shown as

$$g_1 = \frac{I_D}{V_{GT}} = \frac{g_m}{2}, \quad g_3 = \frac{I_D}{8V_{GT}^3} = \frac{g_m^3}{64I_D^2} \tag{2.34}$$

where I_D is the transistor bias current of op amps, V_{GT} is the effective gate-source voltage, and g_m is the transconductance of the input transistors. If equation (2.34) is substituted into equation (2.32), the third-harmonic distortion is modified as

$$HD_3 \approx \frac{V_{in}^2}{64 g_m R_{in}^3 I_D^2} \left(1 + \frac{R_{in}}{R_{dac}} \right) \tag{2.35}$$

Thus, the linearity can be improved if R_{in} is increased up to the allowable thermal noise limit or the input transconductance is increased [40].

Time-constant error (Integrator gain error)

The variation of *RC* time constant in CT ΣΔ modulators can be more than 30% because process variations of the absolute component values are reported by 10-20%. The variation of the *RC* time constant can be modeled by an error Δ_{RC} and the integrator transfer function is defined as

$$TF_{\Delta_{RC}} = \frac{1}{sRC} \approx \frac{f_s}{s\left(1+\Delta_{RC}\right)} \tag{2.36}$$

with

$$\Delta_{RC} \in \pm\sqrt{\left(\Delta_R\right)^2 + \left(\Delta_C\right)^2} \tag{2.37}$$

where f_s is the sampling frequency. Considering this variation, the total in-band quantization noise power (IBN) of the single-loop, M-order modulator is given as

$$IBN(\Delta_{RC}) \approx \frac{\Delta^2}{12k_1^2k_q^2} \frac{\pi^{2M-1}\left(1+\Delta_{RC}\right)^{2M-1}}{\left(2M+1\right)OSR^{2M+1}} \tag{2.38}$$

where Δ is quantizer step size, k_1 is the feedback scaling coefficient of the first integrator, an *OSR* is the oversampling ratio [41]. A time-constant variation of Δ_{RC} = 20% results in a 5-dB increased IBN.

Circuit noise

The most critical error source is located at the input of the modulator because no noise shaping takes place at the input stage [41]. Thus, the overall noise power is governed by the input-referred noise of the first integrator if a ΣΔ modulator is designed that the overall noise power is dominated by circuit noise. The dominant noise sources in the active RC integrator are shown in Figure 2-18. The total input-referred noise is given as

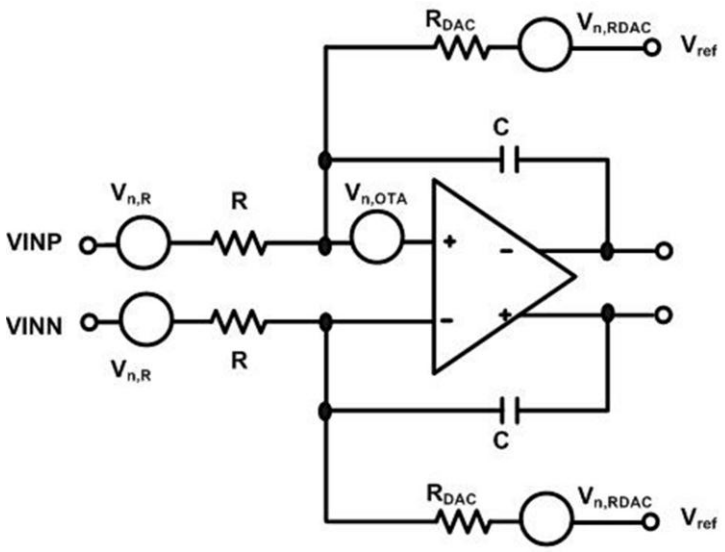

Figure 2-18: Schematic of a fully differential active RC-integrator with noise sources

$$\overline{v}_{n,in}^{2} \approx 2\left(\overline{v}_{n,R}^{2} + \overline{v}_{n,R_{DAC}}^{2}\frac{R^2}{R_{DAC}^2} + \overline{v}_{n,R_z}^{2}\frac{R^2}{Z_F^2}\right) + \overline{i}_{n,OTA}^{2}R^2 + \overline{v}_{n,OTA}^{2}\left(1+\frac{R}{R_{DAC}}+\frac{R}{Z_F}\right)^2 \tag{2.40}$$

where Z_F is the feedback impedance. Each resistance (R and R_{DAC}) generates thermal noise and the amplifier introduces the thermal noise and 1/f noise like equation (2.41) and (2.42).

$$\overline{v}_{n,R}^{2} \approx 4kTR, \quad \overline{v}_{n,R_{DAC}}^{2} \approx 4kTR_{DAC} \tag{2.41}$$

$$\overline{v}_{n,OTA}^{2} = \frac{8}{3}\frac{kTn_{e,th}}{gm_{OTA}} + \frac{k_f n_{e,f}}{C_{ox}^2 WL}\frac{1}{f_f^{a}} \tag{2.42}$$

Where, $n_{e,th}$ and $n_{e,f}$ are the thermal and flicker noise excess factors and k_f and a_f are the flicker noise parameters [23]. Table 2-4 shows the summary of impact of nonidealities of integrator.

Table 2-4

Impact of Nonidealities of Integrator [23]

Block	Nonideality	Impact
Op amp	Finite and nonlinear gain	Increased noise floor, Harmonic distortion
	Finite unity gain bandwidth	Increased noise floor, Stability properties
	Finite slew rate	Quantization noise increase, Harmonic distortion
	Op amp gain nonlinearity	Harmonic distortion
	Thermal and 1/*f* noise	Increased noise floor
V-I Conv. (R)	Nonlinearity	Harmonic distortion
	Thermal noise	Increased noise floor
Integrator Gain	Time constant mismatch	Less aggressive noise shaping or stability issues

3 PROPOSED ARCHITECTURE

3.1 Loop Filter Design

The system level block diagram of the proposed closed-loop class-D amplifier is shown in Figure 3.1. Although class-D amplifiers operating in the open loop mode remove the need for an additional DAC, they typically have inferior PSRR and distortion [42]. Therefore, closed-loop analog input class-D amplifier architecture is adopted to improve distortion and supply rejection performance [4]. The nonlinearity of the ramp generator introduces harmonic distortion in typical PWM-based class-D amplifiers. On the other hand, higher oversampling rate, single bit PDM drivers work on a single-bit

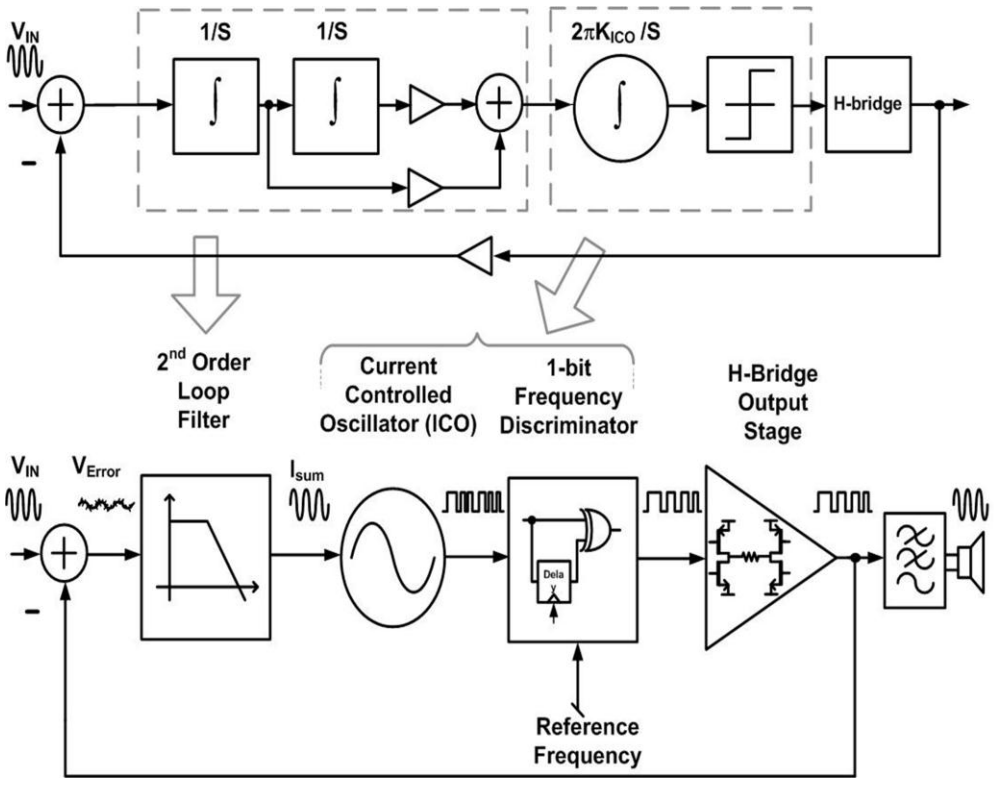

Figure 3-1: System level diagram of the proposed class-D audio amplifier.

comparison (quantization) at the loop filter output. The single-bit quantization achieves a high linearity, and the harmonic distortion caused by the nonlinearity of the carrier can be eliminated. On the other hand, the limiting factor for the proposed architecture is the oversampling rate of the modulator, and the order of loop filter (defined by the number of integrators in the loop). The proposed class-D amplifier consists of a second-order feed-forward type loop filter, an ICO-based voltage-to-phase integrator, and a digital frequency discriminator that can obtain a 3rd order noise shaping. As an output topology, a full-bridge topology is adopted to cancel the even order harmonic distortion components and to drive low impedance speaker loads. The external low pass filter is used to reconstruct the input signal. If the loop filter order is increased in the proposed system, we can obtain better SNR and DR, while keeping the superior distortion characteristics of the approach. The proposed architecture is capable of supporting a higher SNR, as long as the power consumption limits can allow a higher order loop filter. As shown in previous ΣΔ ADC designs, the choice of a frequency domain quantizer in place of voltage domain implementations enables lower power supply operation with higher order noise-shaping benefits [8]. In frequency domain quantizers, ICO generates a frequency that is proportional to the average analog input signal. It does not require the power- consuming pre-amplifier, and it is also highly digital implementation. Therefore, frequency-domain signal processing offers a better resolution than that of voltage-domain methods in low-voltage designs. In another ADC application, phase has been used as the quantizer output variable, which further improves linearity, by utilizing VCO as the loop integrator [9]. In both these approaches, a multi-bit quantizer is used to increase ADC SNR. However, multi-bit quantizers are not suitable for H-bridge driven class-D amplifier applications because only two switches and a single supply rail are preferred in the switching power stage.

3.2 Reduction of Non-linearity of the ICO Gain Transfer Function

The main disadvantage of an ICO-based quantizer is that its linearity is impacted by the ICO gain transfer function with respect to input voltage. The non-linearity of the ICO is specified as the ratio of the maximum frequency error to the ideal frequency of the ICO [7]. In the proposed approach, the ICO is inside the main loop of the proposed class-D amplifier. Therefore its non-linearity is suppressed by the loop-gain of the feedback amplifier. Figure 3-2 shows the overall THD performance at different levels of the ICO non-linearity (K_{ICO}). K_{ICO} is the ICO gain. Figure 3-3 shows the output spectra of the stand-alone ICO-based quantizer, which is in open-loop condition and the proposed ICO-based modulator in the case where the K_{ICO} has 5% non-linearity. The proposed system is in feedback operation with a second-order loop filter. As shown in Figure 3-3, harmonic distortion products are suppressed in the feedback system with the second-order loop filter; and a third-order noise-shaping characteristic is also achieved.

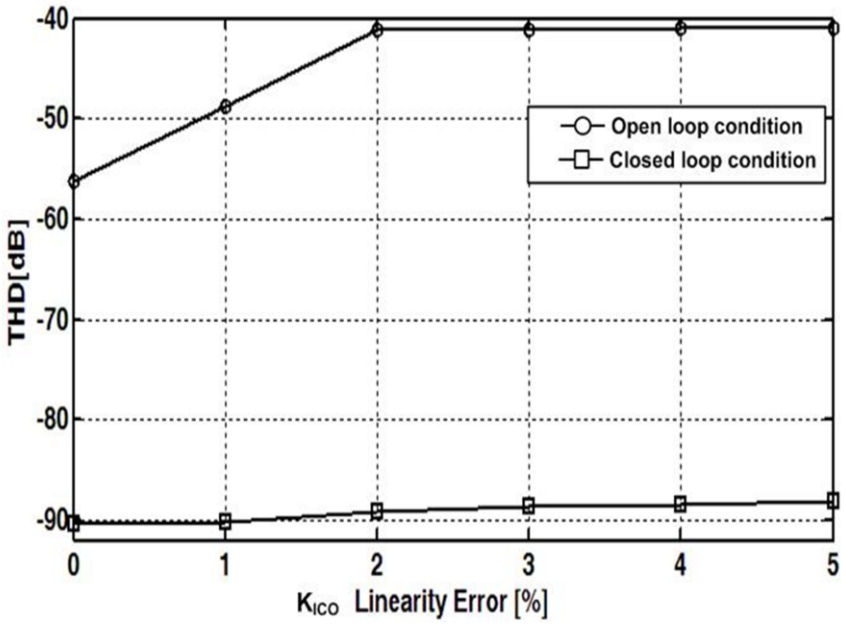

Figure 3-2: Simulated THD results of the class-D amplifier in open and closed loop conditions.

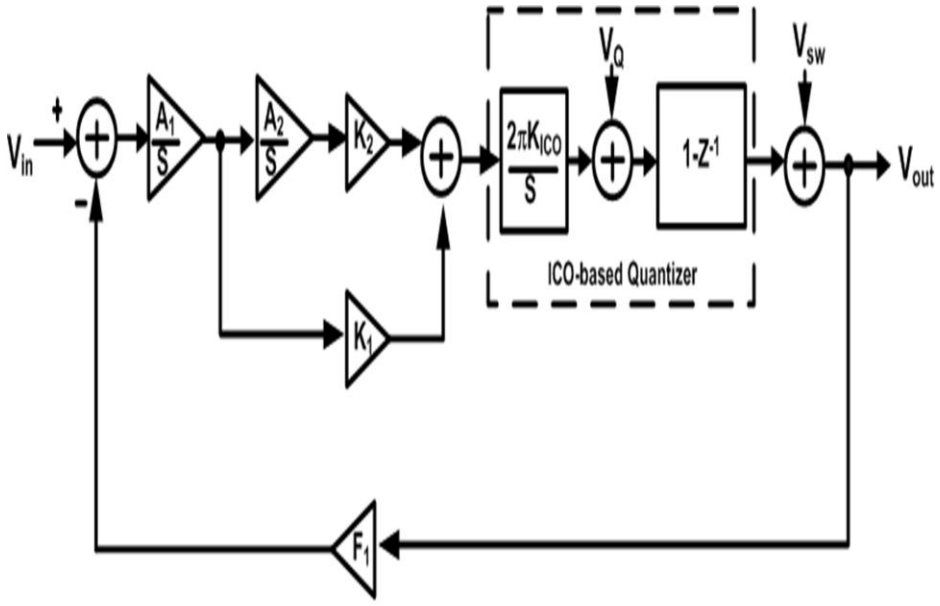

Figure 3-4: Linear model of the proposed class-D amplifier with frequency domain quantizer.

Figure 3-4 depicts the linear model of the modulator in the proposed class-D amplifier. V_Q and V_{SW} represent quantization noise and switching noise of the output power stage, respectively. The transfer function of the loop filter, $LF(s)$ as shown in Figure 3-4 is

$$LF(s) = F_1 \cdot (1 - e^{-sT_s}) \cdot \left[\frac{2\pi K_{ICO} A_1 (K_1 s + K_2 A_2)}{s^3} \right] \tag{3.1}$$

where F_1 is the feedback coefficient, A_1 and A_2 are integrator coefficients, K_1 and K_2 are feed-forward coefficients, and T_s is the sampling period. The Over-Sampling Ratio (OSR), defined by the ratio of the sampling frequency to the Nyquist rate is designed to be 100, which corresponds to a sampling frequency of 4MHz.

After the OSR is selected for best signal-to-noise and distortion ratio (SNDR), the ICO center frequency (F_{center}) and current-to-frequency gain (K_{ICO}) needs to be optimized. The ICO frequency transfer functions according to the variation of K_{ICO} and

F_{center} are shown in Figures 3-5a and 3-6a, respectively. The histogram of the ICO input voltage according to the variation of K_{ICO} and F_{center} are shown in Figures 3-5b and 3-6b, respectively. As shown in the histograms of the ICO input voltage in Figures 3-5b and 3-6b, the variation of K_{ICO} and F_{center} can cause overloading or clipping at the quantizer input.

When the value of K_{ICO} is increased due to increased loop gain as shown in Figure 3-5a, the voltage swing of the ICO input signal is reduced as shown in Figure 3-5b. As an example, when K_{ICO} is 8 kHz/μA in Figure 3-5b, the input signal of ICO is over the limitation of the input signal range. As a result, the power spectrum density of odd harmonic distortion products is increased, as shown in Figure 3-7. However, with an increase in ICO gain, the effect of phase noise in the output frequency of ICO also

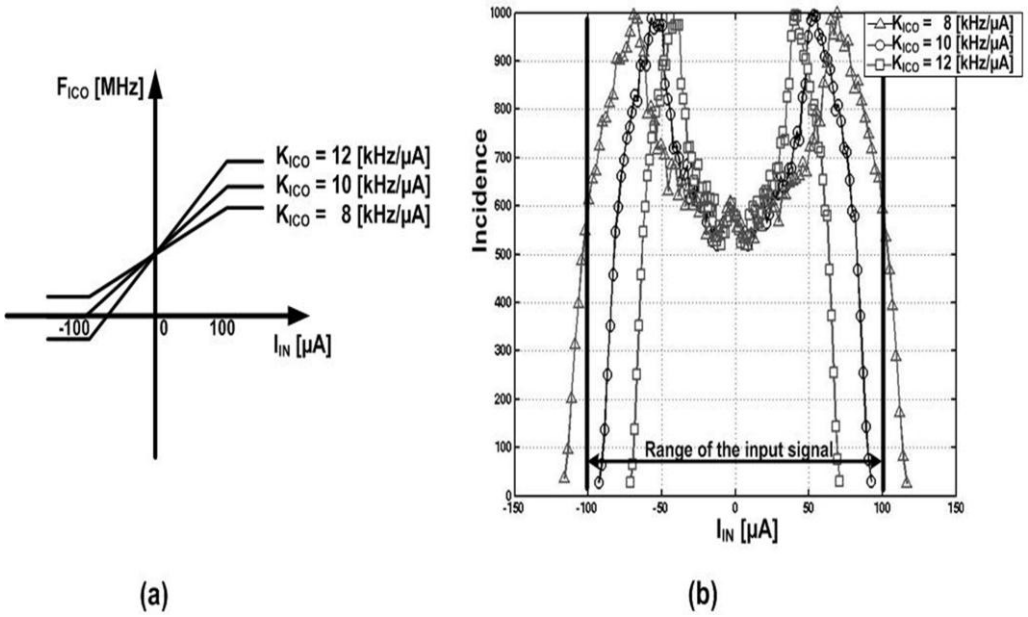

Figure 3-5: (a) ICO frequency transfer function according to the variation of K_{ICO} (b) Histograms of the ICO input signal according to the variation of K_{ICO}.

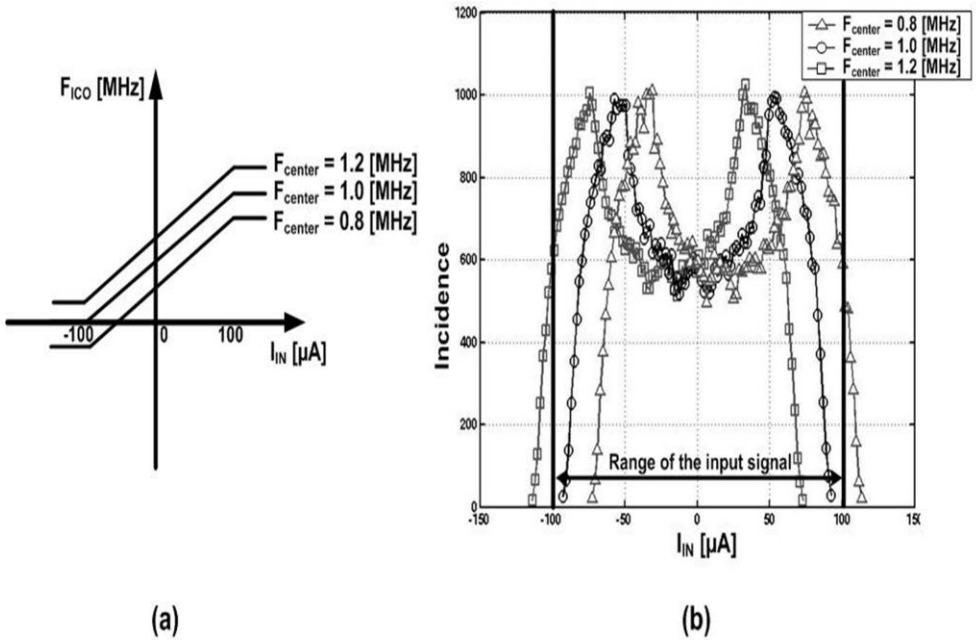

Figure 3-6: (a) ICO frequency transfer function according to the variation of F_{center} of ICO (b) Histograms of the ICO input signal according to the variation of F_{center} of ICO.

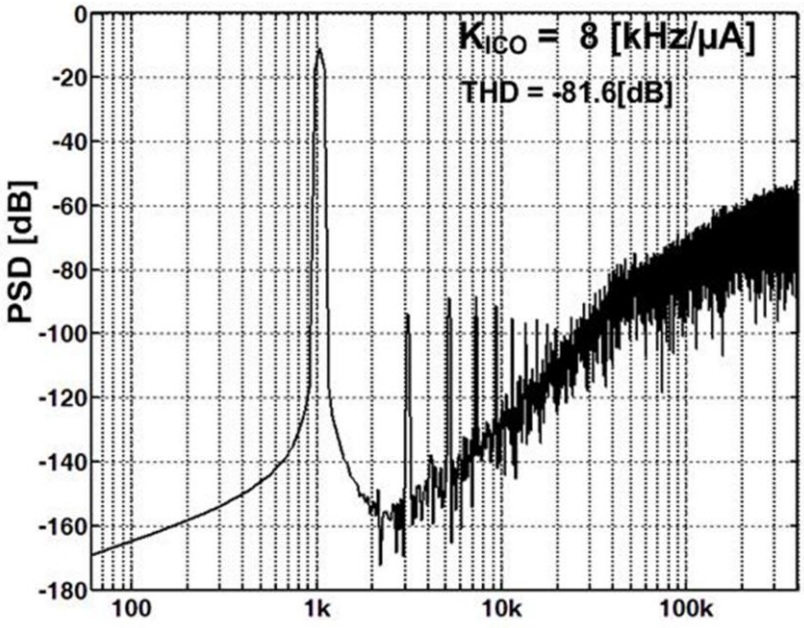

Figure 3-7: Power spectrum with K_{ICO} = 8 kHz/μA.

increases. Thus, K_{ICO} is designed to be 10 kHz/μA in the proposed class-D amplifier as an optimum point between phase noise and comparator input voltage spread, based on transient simulations and ICO input node voltage histograms.

Figure 3-6b shows the ICO input histogram when F_{center} is swept from 0.8 MHz to 1.2 MHz. At 0.8 MHz and 1.2 MHz of the F_{center} the input voltage range of the ICO shifts from the center, and its input voltage goes out of range of the ICO linear transfer function. As a result, even harmonic distortion products, as well as odd harmonic distortion products, are generated, as shown in Figures 3-8 and 3-9. Therefore, F_{center} of the ICO is designed to be 1.0 MHz. Figure 3-10 shows the power spectrum with the optimized K_{ICO} and F_{center} of ICO. K_{ICO} = 10 kHz/μA and F_{center} = 1.0MHz is used in the propose class-D amplifier.

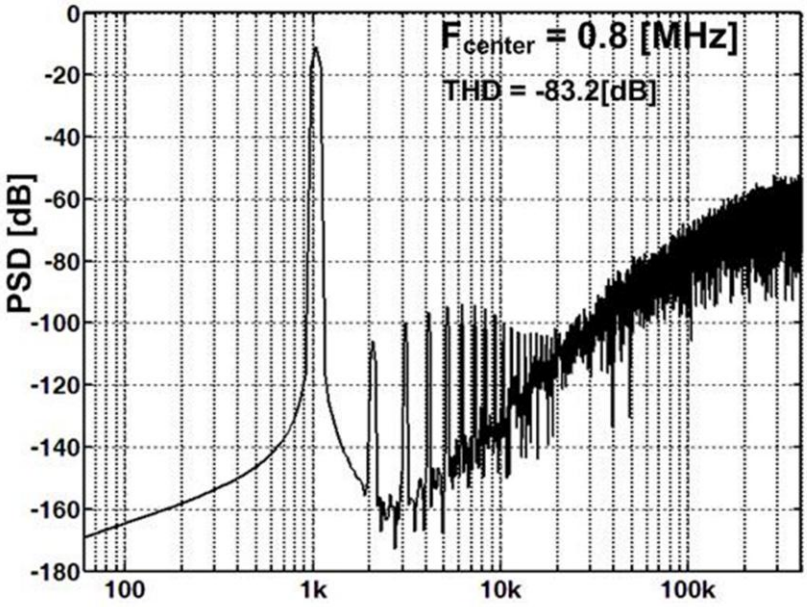

Figure 3-8: Power spectrum with F_{center} = 0.8 MHz.

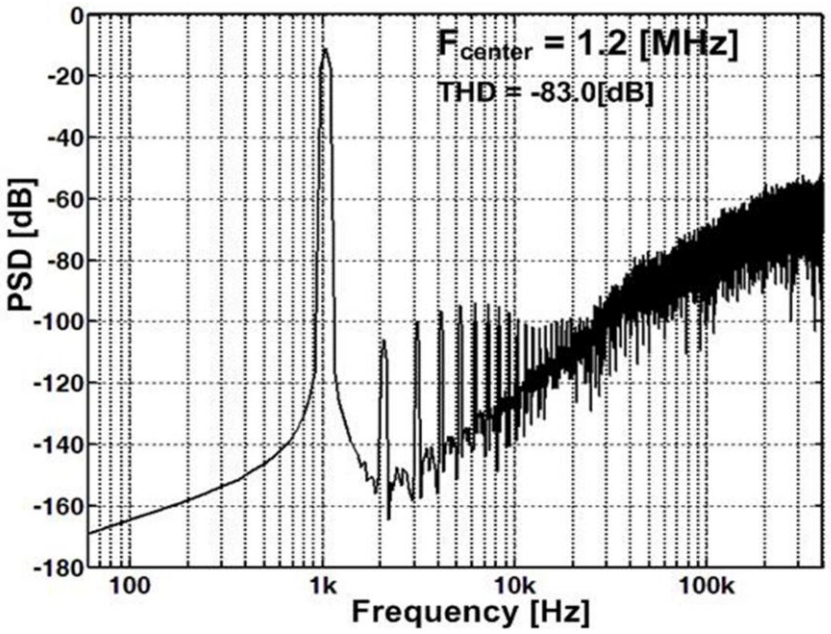

Figure 3-9: Power spectrum with F_{center} = 1.2 MHz.

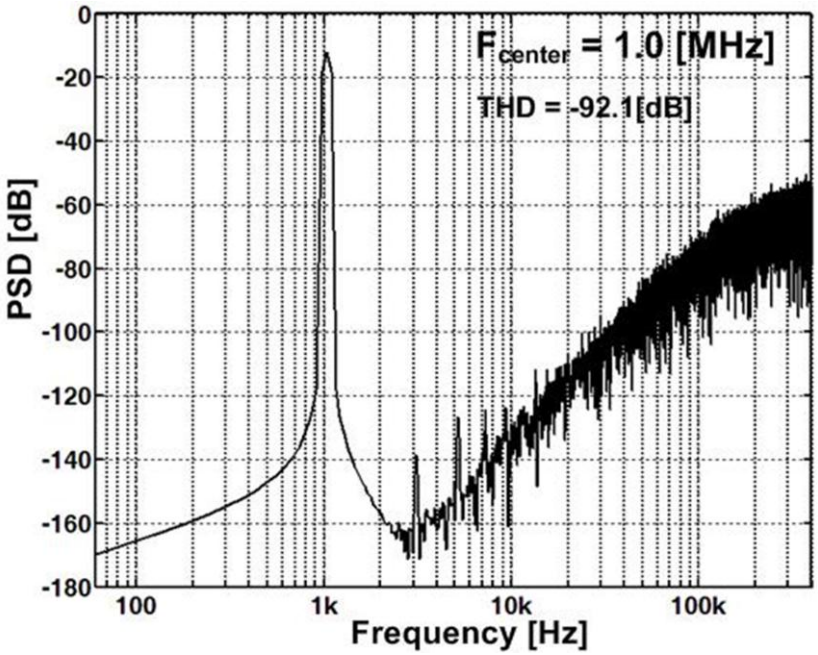

Figure 3-10: Power spectrum with K_{ICO} = 10 kHz/μA and F_{center} = 1.0 MHz.

The *STF(s)* and the *NTF(s)* of the proposed system model can be expressed from equation (3-1) as

$$\begin{aligned} STF(s) &= \frac{V_{out}}{V_{IN}}(s) = \frac{LF(s)}{F_1 \cdot (1 + LF(s))} \\ NTF_Q(s) &= \frac{V_{out}}{V_Q}(s) = \frac{(1 - e^{-sT_S})}{(1 + LF(s))} \\ NTF_{SW}(s) &= \frac{V_{out}}{V_{SW}}(s) = \frac{1}{(1 + LF(s))} \end{aligned} \tag{3-2}$$

As shown in equation (3-2), the *STF*(s) shows a low-pass characteristic; the quantization noise goes through a third-order noise shaping (NTF_Q (s)), and the switching noise associated with the output stage goes through a second-order noise shaping (NTF_{SW} (s)). The frequency response of STF and NTF of quantization and switching noise is reported in Figure 3-11.

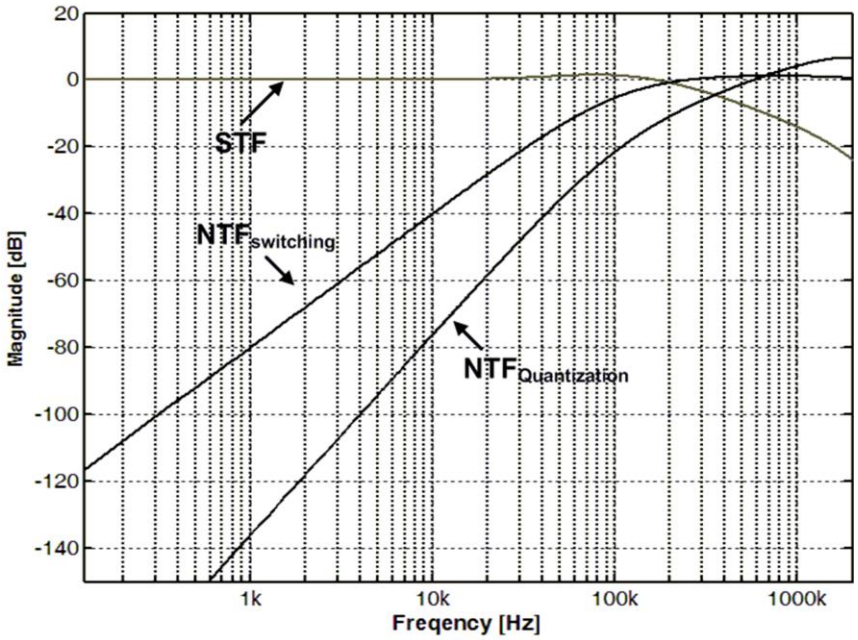

Figure 3-11: STF and NTF responses for quantization and switching noise.

3.3 Stability of Proposed Architecture

A critical requirement of a higher order noise-shaped ADC and class-D amplifier is the stability of their feedback systems. In noise-shaped systems, the system's stability is controlled by the poles of NTF. A variable quantizer gain method is used to analyze system stability [25]. Figure 3-12 shows the root locus of the proposed system for various quantizer gain levels. Another requirement is the robustness of this stability condition under coefficient variations across process, temperature, and voltage. Figure 3-13 shows the pole location for coefficient variations within ±20% of nominal values. The proposed system is stable since the poles of NTF are inside the unit circle across all quantizer gains and coefficients.

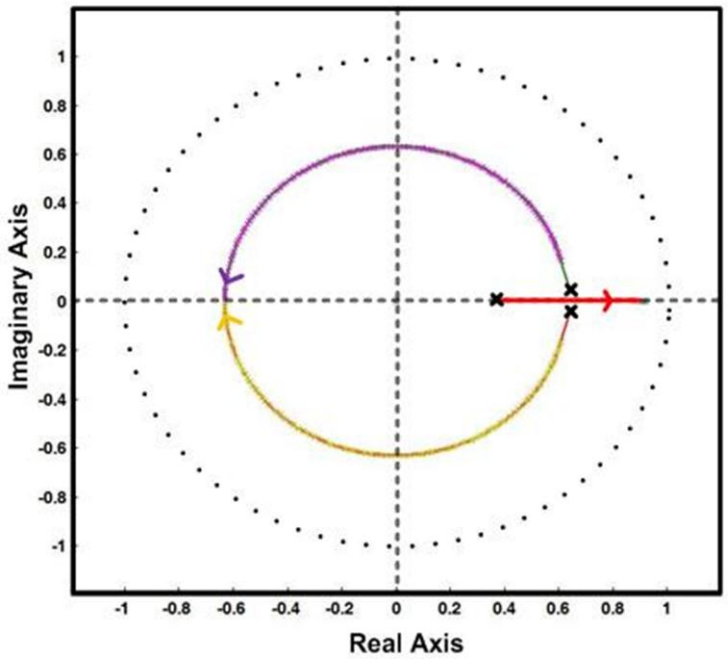

Figure 3-12: Root locus plot of NTF_Q.

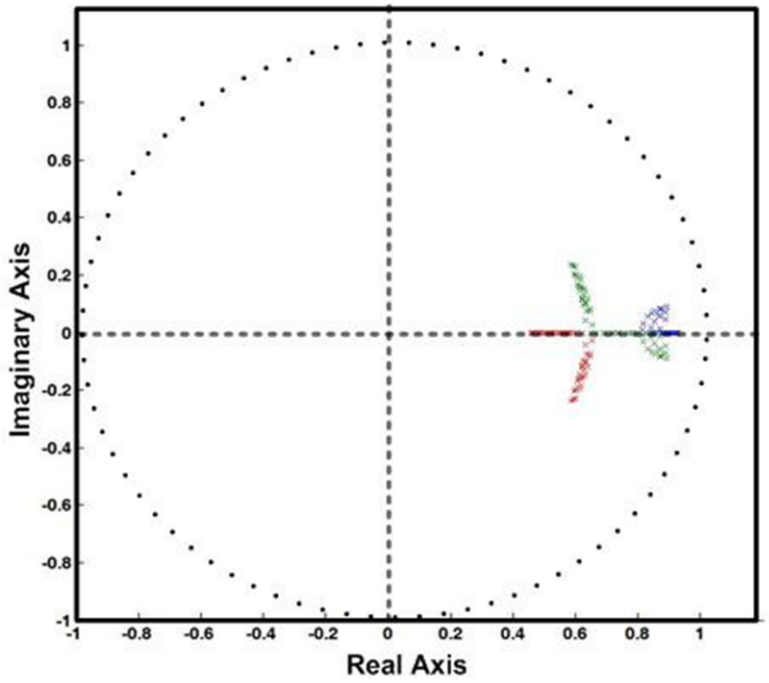

Figure 3-13: Poles locations for process and temperature based coefficient variation.

3.4 PSRR of the Proposed Class–D Amplifier

Power Supply Rejection Ratio (PSRR) is an important parameter of the class-D amplifier, and it is defined by the ratio of the output ripple voltage to the power supply ripple voltage. Any ripple from the power supply input at various frequencies is transferred to the outputs of class-D amplifiers. With high PSRR, the ripple noise can be rejected and does not disturb the audio performance.

By using equation (3.1), the expression of PSRR of the proposed class-D amplifier can be derived as

$$PSRR = 20\log\left(\frac{V_{out}}{V_{ps\ ripple}}(s)\right) = 20\log\left(\frac{1}{1+LF(s)}\right) \tag{3-3}$$

where the $V_{ps\ ripple}$ is the noise components introduced by the ripple noise in the power supply input. As shown in the equation (3-3), the loop gain affects PSRR – the higher the loop gain, the higher the PSRR [43][44].

3.5 Comparison between 1-bit and 1.5-bit digital frequency discriminator

The ICO-based quantizer can be modified for three-level modulation to permit operation without an output LC filter. Figure 3-14 shows 1.5-bit digital frequency discriminator version of the quantizer for three-level modulation as the example. Two D-FFs and a XOR gate are added in parallel with a previous set of D-FFs and a XOR gate. Simulated PSDs for this topology is shown in Figure 3-15. SNRs / SNDRs of the system with a 1-bit frequency to digital convert quantizer (FDC) versus 1.5-bit FDC quantizer are 78.8 [dB] / 78.6 [dB] and 80[dB] / 77.7 [dB], respectively. Although the extra level of quantization enhances the SNR by approximately 1.5dB, it is still not sufficient to get rid of the out of band noise. Also, adding an extra level (zero state) and associated three-level operation breaks the fully differential operation principle and the zero state

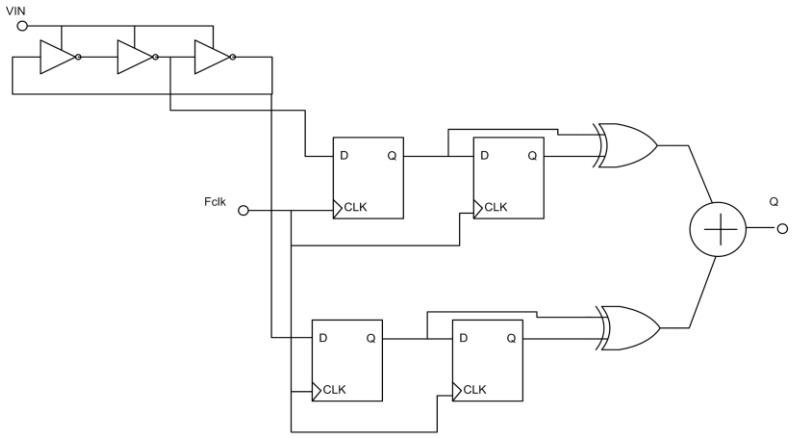

Figure 3-14: 1.5-bit digital frequency discriminator version of the quantizer

contributes to the common mode noise generation. As shown in Figure 3-15, although in-band noise reduces, harmonic distortion increases due to the zero state to +/-1 state transitions and mismatch between the two states. Therefore, a compensation technique should be employed to solve this problem in three-level modulation. In order to minimize the common mode noise and distortion, we chose single-bit quantization.

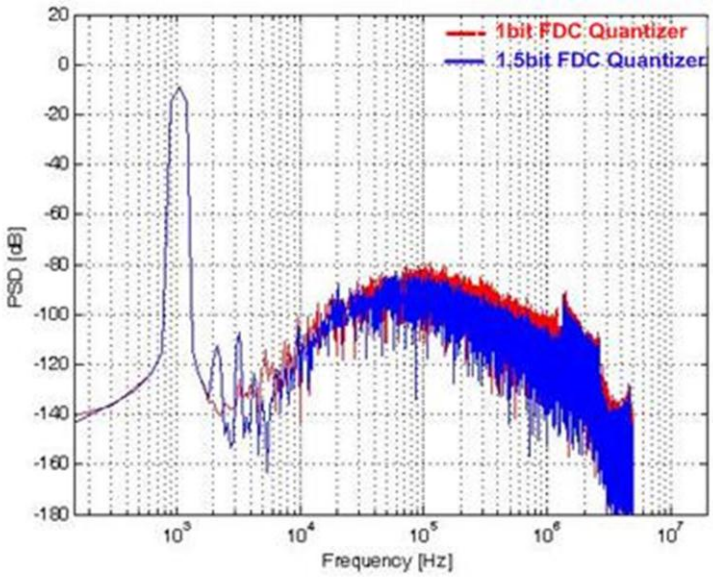

Figure 3-15: PSDs with a 1bit FDC quantizer versus with a 1.5 bits FDC quantizer

4 CIRCUIT IMPLEMENTATION

4.1 Loop Filter

The simplified schematic of the proposed class-D amplifier's implementation is shown in Figure 4-1. The second-order loop filter consists of two analog active-RC integrators. Each integrator has the manually controlled binary-weighted tunable capacitor arrays to compensate the RC time constant variation by +/-20% as shown in Figure 4-2. A Voltage-to-Current (V-I) converter stage is used to drive a ring oscillator-based ICO. The use of a V-I converter stage allows implementation of summing nodes for the feed forward paths, K_1 and K_2, as shown in Figure 3-4, without using additional power hungry op amps. The digital frequency discriminator is based on a logic XOR gate and a digital delay line. Use of an ICO-based quantizer eliminates an analog integrator. An additional benefit to this method is that due to high impedance loads provided by the ICO-based quantizer, an OTA rather than a two-stage op amp can be used for the second

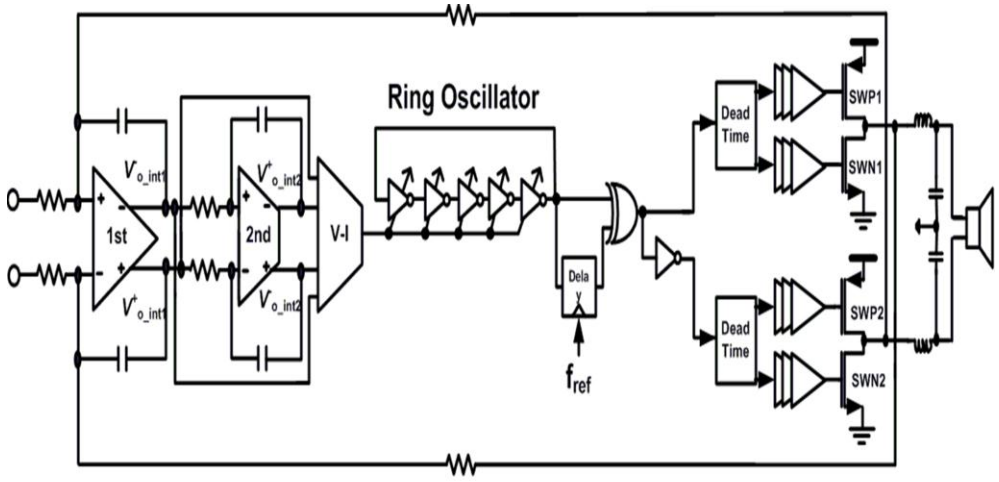

Figure 4-1: Simplified schematic of the proposed class-D amplifier.

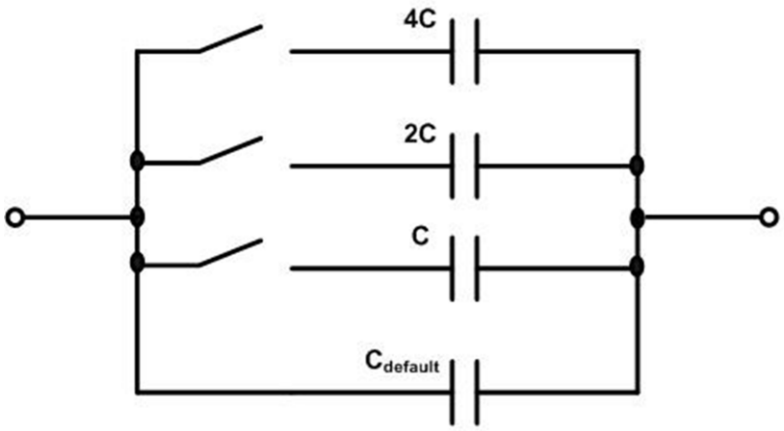

Figure 4-2: Binary weighted tunable capacitor array.

integrator, thus reducing overall power consumption. The topological differences between the conventional three integrators approach with respect to the proposed ICO-based architecture is shown in Figure 4-3. In a typical loop-filter implementation, analog loop filter integrators definitely have both die area and power consumption impact. The power consumption of the proposed architecture is reduced by 30%, and the area is also reduced by 38% in comparison to the conventional architecture, which consists of three integrators, summing op amp, and quantizer.

Output of the frequency discriminator is passed to a switching power stage with a Bridge-Tied-Load (BTL) differential drive configuration [45]. Two dead-time generators are employed to ensure that both nMOS and pMOS output devices are off during transition times, which would affect the amplifier's efficiency and non-linearity [46]. Finally, an on-board discrete low-pass filter is used for signal reconstruction and to knock down high-frequency signal content due to noise shaping.

4.2 First and Second OP AMP Design

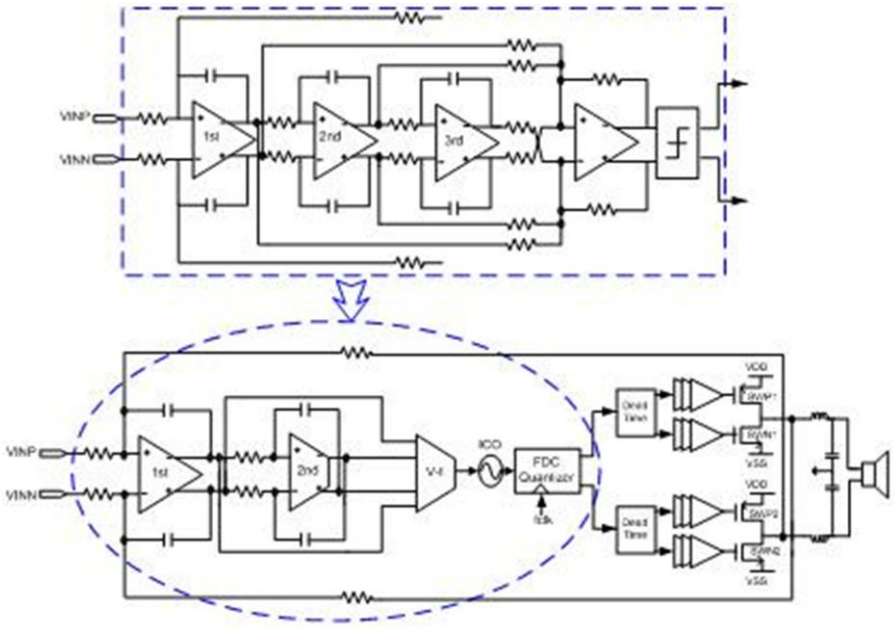

Figure 4-3: The topological differences between the conventional three integrators approach with respect to the proposed ICO-based architecture

The gain and linearity of the first integrator affects the performance of the overall class-D amplifier. Therefore, a high gain two-stage operational amplifier is used for the first active-RC integrator, as shown in Figure 4-4. The noise from the first integrator is the dominant circuit noise source and its equivalent noise source is shown in Figure 4-5. This is expressed as

$$\begin{aligned} V_{n,in}^2 &= 2V_{n,R_1}^2 + 2\left(\frac{R_1^2}{R_2^2}\right)V_{n,R_2}^2 + \left(1+\frac{R_1}{R_2}+2\pi fR_1C\right)^2 V_{n,op}^2 \\ &= 8kTR_1 + \frac{R_1^2}{R_2^2}\left(8kTR_2\right) + \left(1+\frac{R_1}{R_2}+2\pi fR_1C\right)^2 V_{n,op}^2 \end{aligned} \tag{4.1}$$

where *k* is the Boltzmann constant and T is the absolute temperature. The equivalent noise of the first stage for an audio frequency range from 20 Hz to 20 kHz has been designed to be approximately equal to the in-band quantization noise as 58.3μV/$\sqrt{\text{Hz}}$.

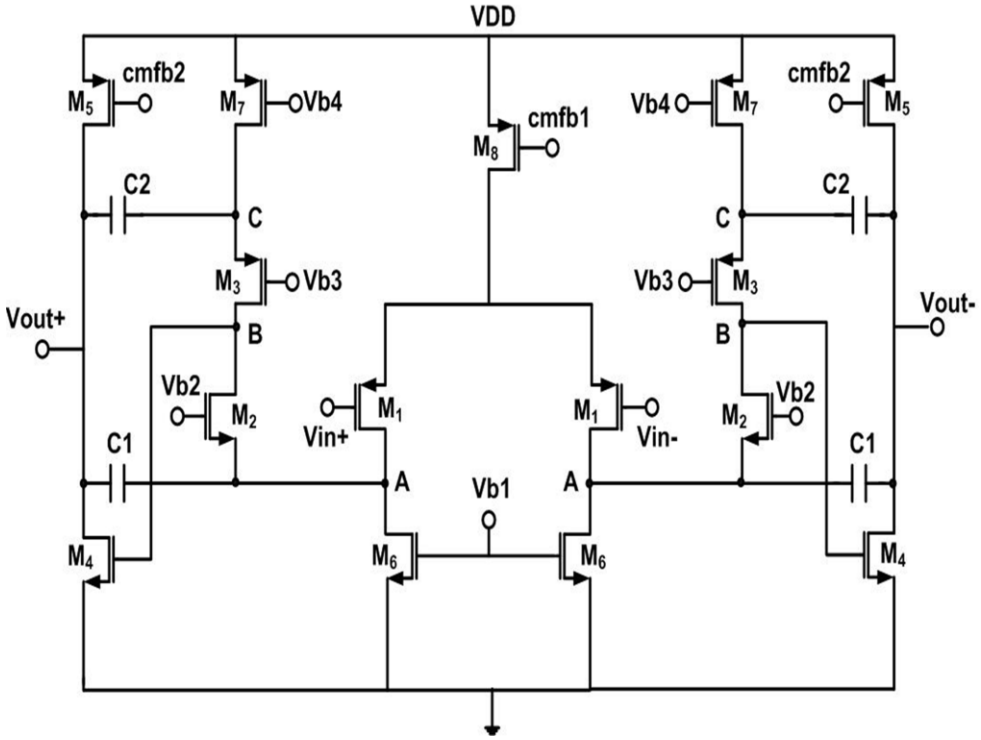

Figure 4-4: First stage integrator op amp with hybrid cascode compensation.

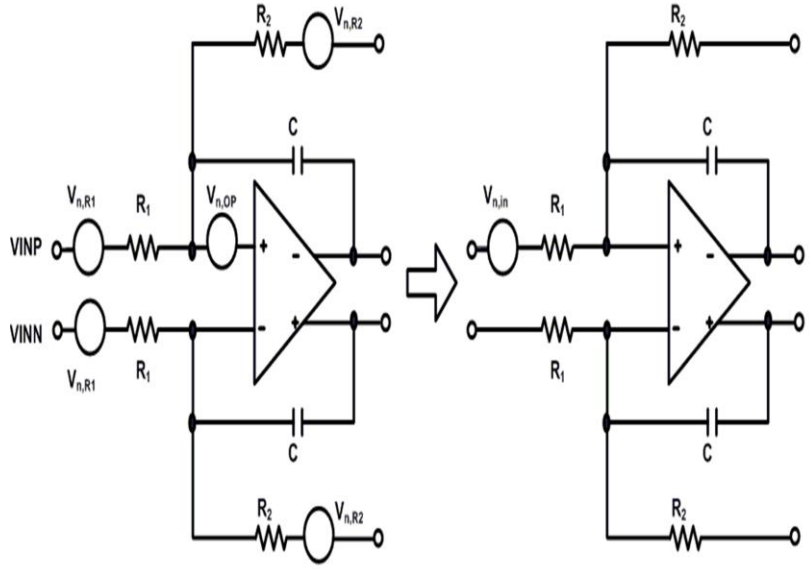

Figure 4-5: The equivalent noise source of the first integration.

The first amplifier consists of a folded cascode stage followed by a common-source amplifier that uses hybrid cascode compensation. The hybrid cascode compensation technique employs two capacitors, *C1* and *C2*, between the output node and the two low-impedance nodes A and B of the first stage. This improves frequency response and settling behavior. Although when compared to the conventional cascode compensation, an extra zero and pole is generated, the first zero is cancelled with the second pole when the op amp is designed, such that $g_{m2} = g_{m3}$ and $C1=C2=0.5C$ [47]. The small signal model of the first amplifier is shown in Figure 4-6. From Figure 4-6, the small signal equations can be defined as

$$g_{m1}v_{in} + \frac{v_a}{R_A} + sC_A v_a + g_{m2}v_a + sC_1(v_a - v_{out}) = 0 \tag{4.2}$$

$$\frac{v_b}{R_B} + sC_B v_b - g_{m2}v_a - g_{m3}v_c = 0 \tag{4.3}$$

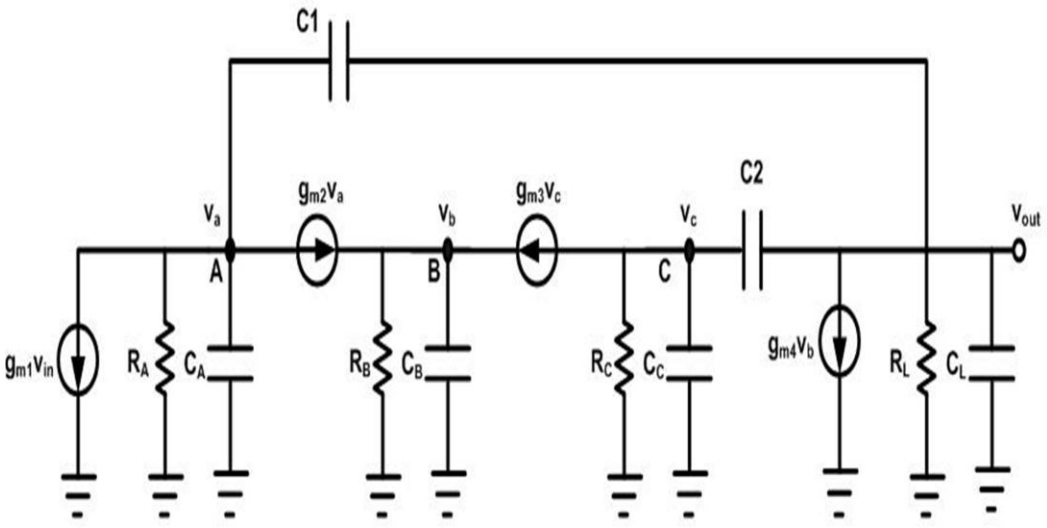

Figure 4-6: Small-signal model of the first op amp.

$$\frac{v_c}{R_C} + sC_C v_c + g_{m3} v_c + sC_2 \left(v_c - v_{out} \right) = 0 \tag{4.4}$$

$$g_{m4} v_b + sC_2 (v_{out} - v_c) + \frac{v_{out}}{R_L} + sC_L v_{out} + sC_1 (v_{out} - v_a) = 0 \tag{4.5}$$

$$R_A = r_{ds1} \parallel r_{ds6} \parallel \frac{g_{m3} r_{ds3} r_{ds7}}{1 + g_{m2} r_{ds2}} \tag{4.6}$$

$$R_B = g_{m2} r_{ds2} \left(r_{ds1} \parallel r_{ds6} \right) \parallel g_{m3} r_{ds3} r_{ds7} \tag{4.7}$$

$$R_C = r_{ds7} \parallel \frac{g_{m2} r_{ds2} \left(r_{ds1} \parallel r_{ds6} \right)}{1 + g_{m3} r_{ds3}} \tag{4.8}$$

$$R_L = r_{ds4} \parallel r_{ds5} \tag{4.9}$$

$$C_A = C_{db1} + C_{gs2} + C_{db6} + C_{sb2} \tag{4.10}$$

$$C_B = C_{db2} + C_{db3} + C_{gs4} + C_{gd2} + C_{gd3} \tag{4.11}$$

$$C_C = C_{gs3} + C_{sb3} + C_{gd7} + C_{db7} \tag{4.12}$$

$$C_L = C_{db4} + C_{db5} + C_{gd4} + C_{gd5} \tag{4.13}$$

where R_A, R_B, R_C, R_L and C_A, C_B, C_C, C_L are total resistances and capacitances seen at node A, B, C, and output, respectively.

After making appropriate simplifications, the small-signal transfer function is obtained as follows;

$$A_v(s) \approx \frac{\left(g_{m1} g_{m3} + \frac{g_{m1}}{R_C} + s g_{m1} \left(C_2 + C_C \right) \right) \left(g_{m2} g_{m4} - \frac{sC_1}{R_B} - s^2 C_1 C_B \right)}{P} \tag{4.14}$$

$$\begin{aligned} P = {} & s^4 (C_B C_L C_1 C_2) + s^3 \left[g_{m2} C_2 (C_1 + C_2) + g_{m3} C_1 C_B (C_2 + C_L) \right] \\ & + s^2 \left[g_{m2} g_{m3} C_B (C_1 + C_2 + C_L) + g_{m4} C_1 C_2 (g_{m2} + g_{m3}) \right] \\ & + s \left[g_{m2} g_{m3} g_{m4} (C_1 + C_2) \right] + \frac{g_{m2} g_{m3}}{R_B R_L} \end{aligned} \tag{4.15}$$

If $C_1=C_2=0.5C$, the poles and zeros of the hybrid cascode compensation are defined as

$$S_{p1} = \frac{-2}{g_{m4} C R_L R_B} \tag{4.16}$$

$$S_{p2} \approx \frac{-4 g_{m2} g_{m3}}{C\left(g_{m2} + g_{m3}\right)} \tag{4.17}$$

$$S_{p3,4} = \frac{-\left(g_{m2} + g_{m3}\right)\left(C + 2C_L\right)}{2C_L C} \pm j\sqrt{\frac{g_{m4}\left(g_{m2} + g_{m3}\right)}{C_B C_L}} \tag{4.18}$$

$$S_{z1} \approx \frac{-2 g_{m3}}{C} \tag{4.19}$$

$$S_{z2,z3} \approx \pm\sqrt{\frac{2 g_{m2} g_{m4}}{C C_B}} \tag{4.20}$$

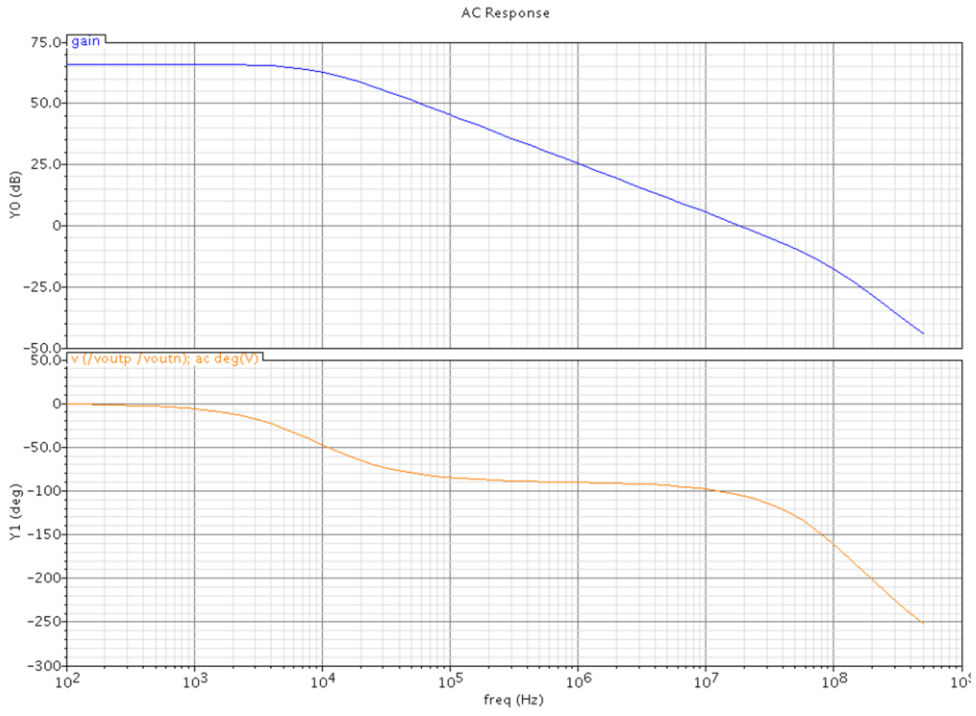

Figure 4-7: Frequency response of the simulated op amp.

The frequency response of the amplifier is shown in Figure 4-7. The first amplifier has 67-dB open-loop DC gain and 20-MHz GBW with 32-pF load capacitance while consuming a 3.45 mA quiescent current.

The second OTA is a conventional folded cascode amplifier. Its schematic is shown in Figure 4-8. It has 63-dB open-loop DC gain and 20-MHz GBW while consuming a 1.34 mA quiescent current.

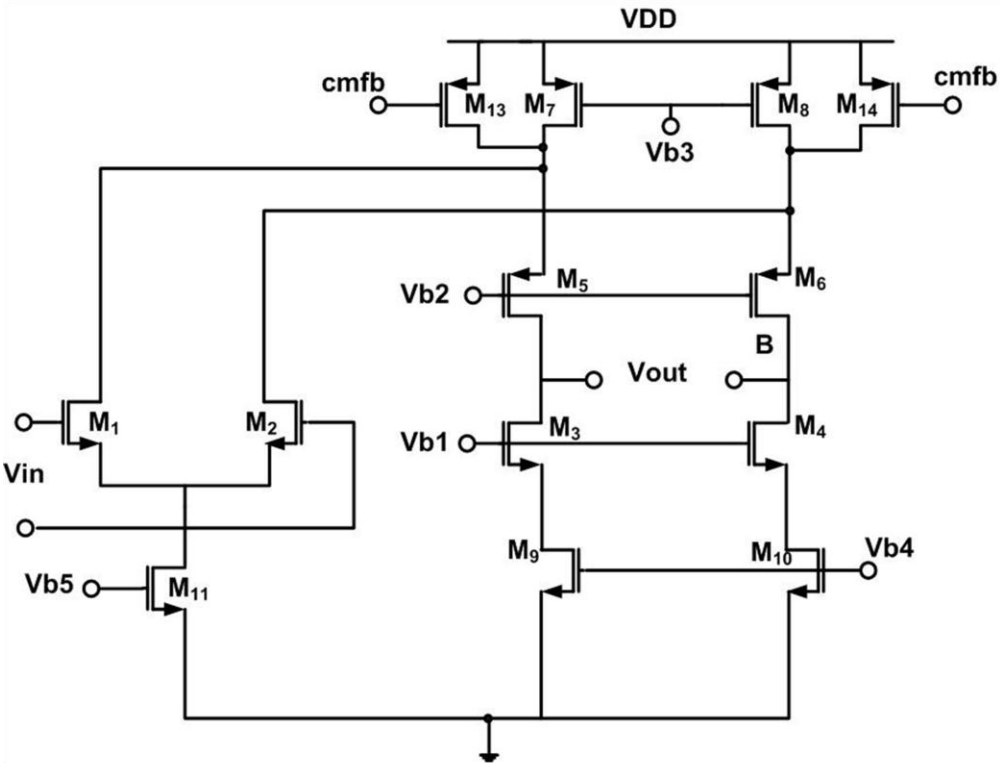

Figure 4-8: The schematic of the second OTA.

4.3 Voltage-To-Current Converter

The two integrator outputs shown in Figure 4-1 are summed by a V-I converter before driving the ICO. The detailed schematics of the V-I converter is shown in Figure 4-9. The current I_1 is proportional to the ratio of the difference between output voltages of the first analog integrator, $V^{+}_{o\_int1}$-$V^{-}_{o\_int1}$ and R_1. The current I_2 is also proportional to the

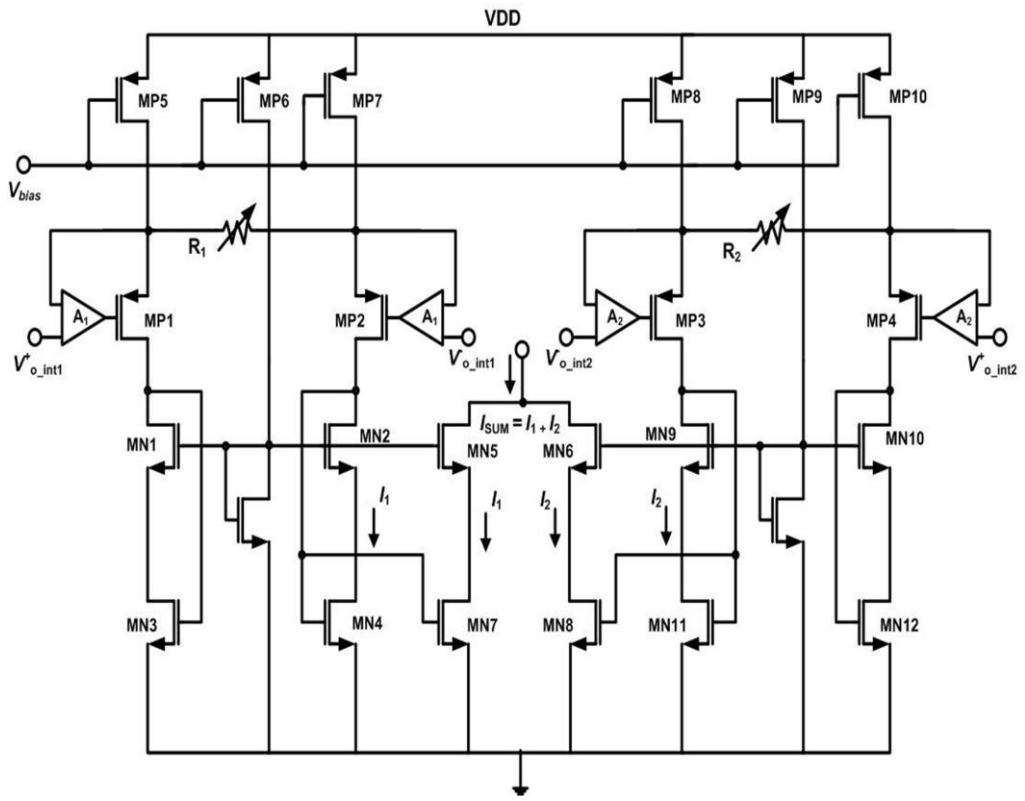

Figure 4-9: Schematic of V-I converter driving the current controlled oscillator.

ratio of the difference between output voltages of the second integrator, $V^+_{o\_int2}$-$V^-_{o\_int2}$ and R_2. Current I_1 and I_2 are then mirrored by transistors MN5-MN8 to generate the summing current I_{sum}. To enhance the linearity of the V-I converter, a gain boosted design is adopted by using auxiliary amplifiers A_1 and A_2. Their schematics are shown in Figure 4-10. The output signal current of the V-I converter drives the ICO for frequency tuning. Eventually, the ICO output frequency, f_{ICO}, is given by the following relationship:

$$f_{ICO} = \left[K_1 \cdot \left(V^+_{\text{o\_int1}} - V^-_{\text{o\_int1}} \right) + K_2 \cdot \left(V^+_{\text{o\_int2}} - V^-_{\text{o\_int2}} \right) \right] \cdot K_{ICO} \qquad (4.21)$$

Finally, the degeneration resistors, R_1 and R_2, set the value of the feed-forward coefficients, K_1 and K_2, in the linear model of Figure 3-4. The degeneration resistors, R_1 and R_2, can be manually controlled to compensate the coefficient variation by +/-20% with

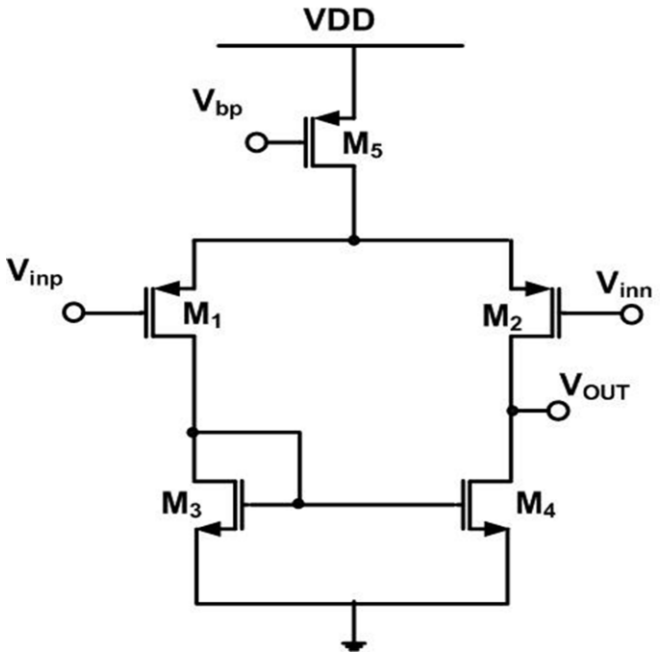

Figure 4-10: Schematics of auxiliary amplifiers A1 and A2.

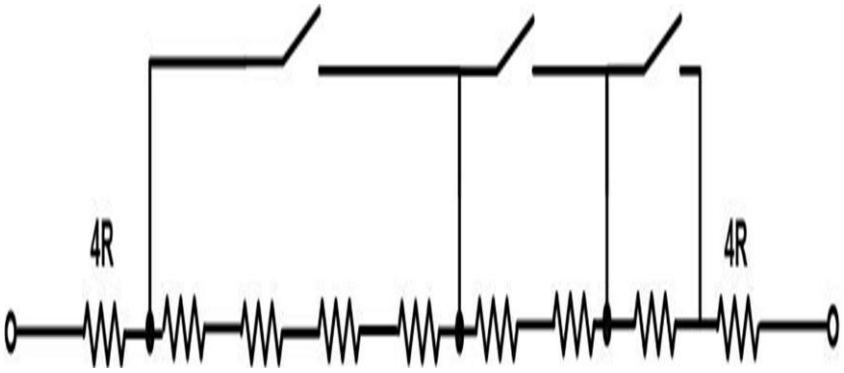

Figure 4-11: Binary weighted tunable resistor array for R_1 and R_2.

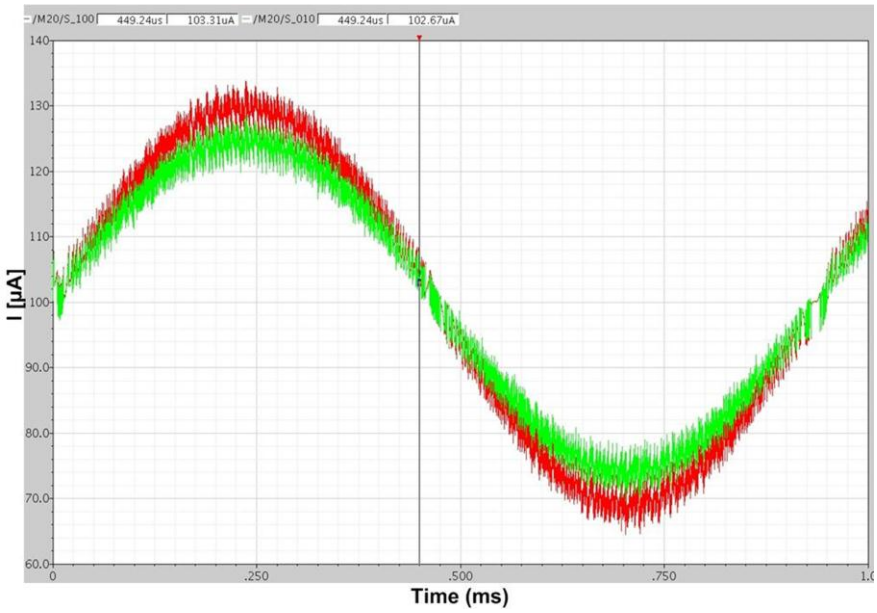

Figure 4-12: The simulated summing current of V-I converter.

the binary-weighted tunable resistor arrays as shown in Figure 4-11. Figure4-12 shows the simulated summing current I_{sum} of V-I converter according to the sinusoid input signal when sw = 010 and sw = 100 to set up the values of R_1 and R_2.

4.4 Current Controlled Oscillator

The ICO converts the analog input current signal into phase domain and generates the output frequency, which is proportional to the average analog input current signal. The schematic of ICO is shown in Figure 4-13. Each delay cell is based on a Maneatis load NMOS transistor consisting of one NMOS in triode region in parallel with a diode-connected NMOS and differential configuration, which offers robust operation against power-supply and substrate noise [48][49][50]. The frequency of the oscillator can be derived as

$$f_{osc} = \frac{1}{N\tau} \tag{4.22}$$

where N is the number of cells and τ is the delay imposed by each cell. The delay of each

cell will be given by

$$V_{osc} = \int \frac{I_{ctrl}}{C_{out}} dt \tag{4.23}$$

$$\tau = \frac{V_{osc} C_{out}}{I_{ctrl}} \tag{4.24}$$

where V_{osc} is the oscillation amplitude, C_{out} is the capacitance seen at each output node, and I_{ctrl} is the control current. Substituting (4.24) into (4.22) will give

$$f_{osc} = \frac{I_{ctrl}}{N V_{osc} C_{out}} \tag{4.25}$$

The oscillator's frequency can be controlled by adjusting control current when C_{out}, N, and V_{osc} are fixed in (4.25). However, the ICO has mismatches of each delay cell causing error in their propagation delay and generating a phase error in practice. Fortunately, the phase error as a result of the mismatch of the ICO delay cells is suppressed by the gain of

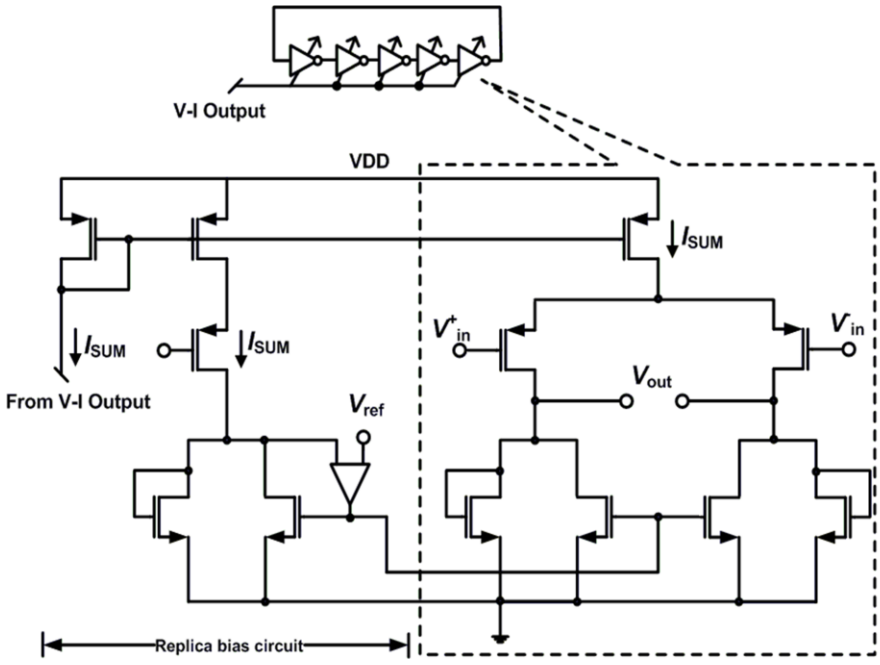

Figure 4-13: Ring oscillator with Maneatis load cell and replica bias circuit.

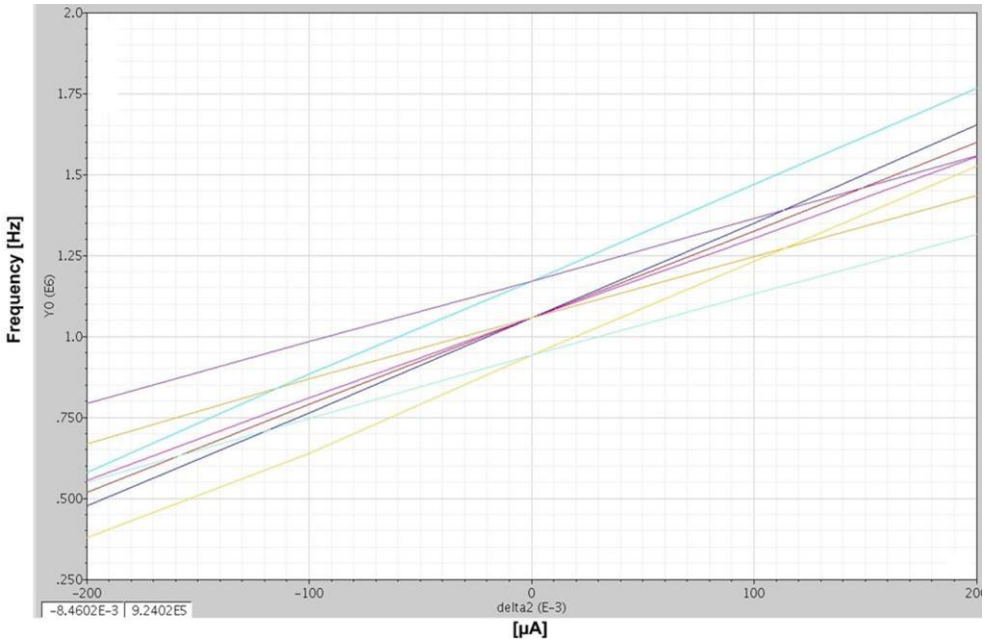

Figure 4-14: Simulated frequency-current characteristics of ICO.

the loop filter [9]. The ring oscillator in the proposed class-D amplifier consists of five delay cells that optimize the linearity of the frequency tuning characteristic. Figure 4-14 shows the simulated frequency-current characteristics according to changing the R_1 and R_2 values of V-I converter. The last stage of the ring oscillator consists of the amplifier with diode-connected loads to amplify the output signal of ICO as shown in Figure 4-15.

4.5 Dead Time Generator

It is important to make sure PMOS and NMOS are never on at the same time in order to prevent a large current between rails caused by the low on resistance of each transistor. This time duration is called a *dead time*. Dead time is a source of distortion and an important design parameter in class-D audio amplifiers. Both PMOS and NMOS in the output stage are turned off during a dead time to prevent the flow of cross-conduction current directly from the supply to the ground, which degrades amplifier efficiency. Therefore, it requires a trade-off between the distortion and the power efficiency. Figure

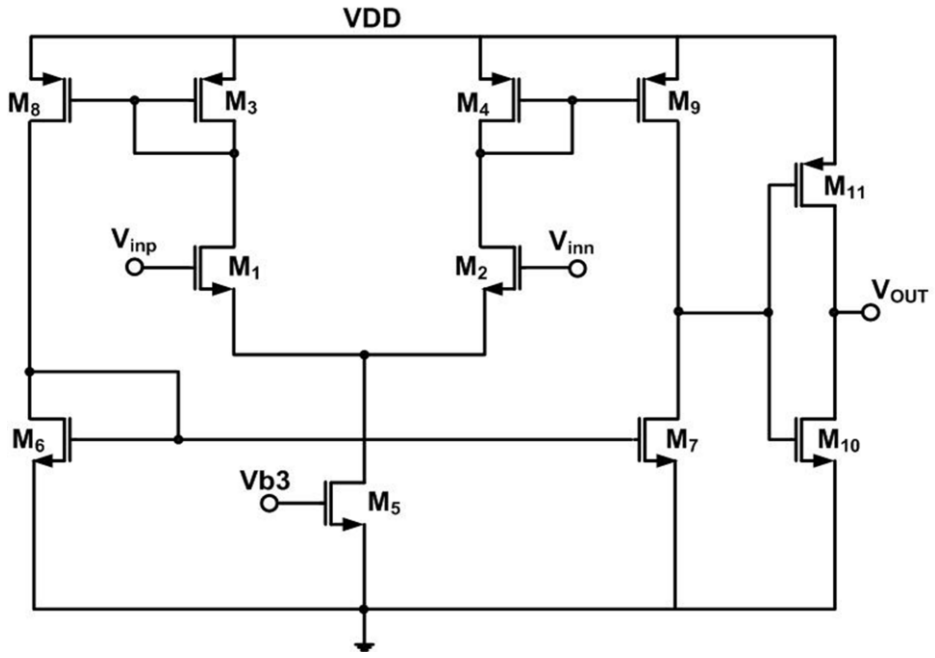

Figure 4-15: The schematic of the amplifier in the last stage of the ring oscillator to amplify the output signal of the ICO.

4-16 shows the dead time generator circuit of the proposed class-D amplifier. The nonoverlapping time of the dead time generator is programmed as 10 nsec by I_{ctrl}.

4.6 Single-Bit Digital Noise Shaped Quantizer (DNSQ)

In the proposed design, the ICO drives a 1-bit digital frequency discriminator, which performs as a DNSQ. The schematic of the DNSQ is shown in Figure 4-17 [51]. Its power spectral density is shown in Figure 4-18. SNDR is about 57 dB when the input frequency is 2.1 kHz and the sampling frequency is 4 MHz.

The encoded phase information $\theta(t)$ at the output of the ICO is given by

$$\theta(t) = 2\pi \int_{-\infty}^{t} \left(f_c + k_{ICO} \cdot x(\tau) \right) d\tau \tag{4.26}$$

where f_c is the carrier frequency and $x(\tau)$ is the input signal of the ICO [51]. Therefore, the ICO performs integration of the input signal through phase modulation as shown in

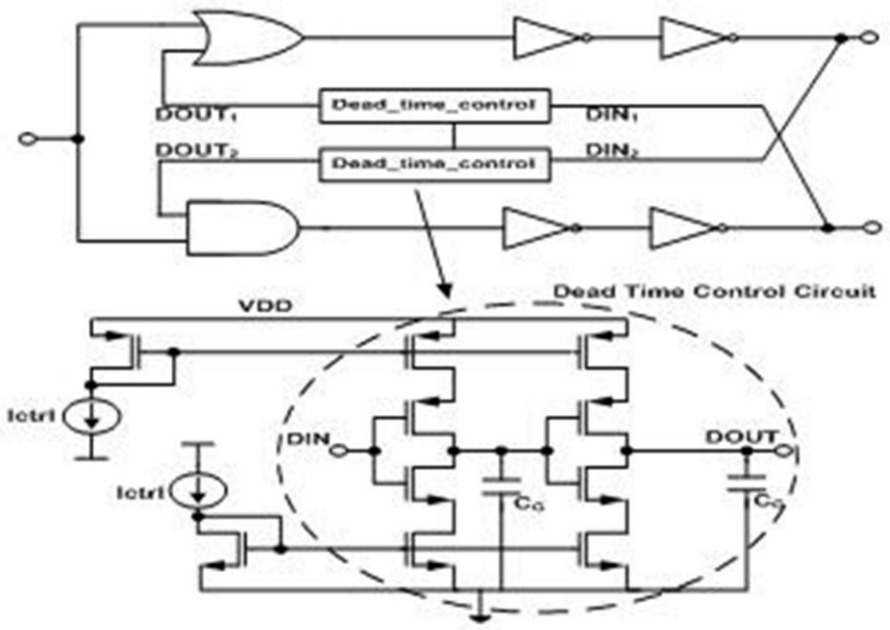

Figure 4-16: Schematic of dead-time generator.

equation (4.26). In the circuit shown in Figure 4-17, a D-flip-flop samples the phase of the modulated signal, while the digital XOR gate compares the previous sample to the current one, thus performing a digital differentiation. The accumulated phase is quantized by detecting the FM signal zero-crossing positions during one sampling period.

The sampling phase through D-flip-flops and the differentiation phase of the XOR gate are combined to achieve a first-order 1-bit modulator block. The output of quantizer is a digital signal containing both the integrated input signal and quantization noise. Both the integrated input signal and its quantization error are subsequently differentiated by a XOR operation. Therefore, the integrated input signal (phase) is converted into a corresponding frequency signal and its quantization noise is differentiated and the quantization noise will be first-order noise-shaped since the quantization error is not integrated. In other words, the useful signal goes through without a change, while the white quantization noise is differentiated and high-pass filtered. As discussed in [8], this extra high-pass noise response adds to the overall noise-shaping

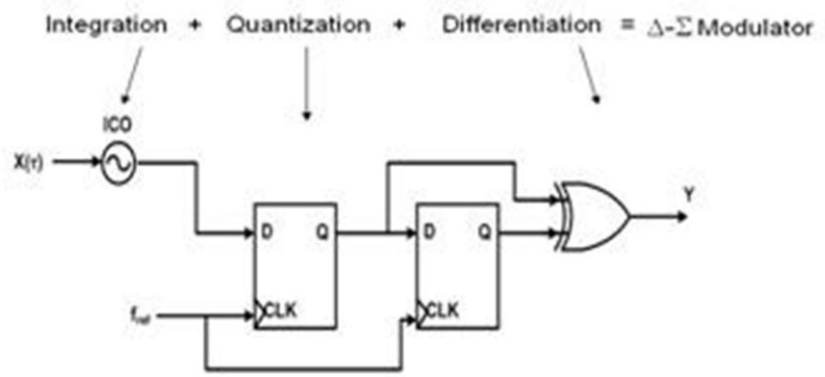

Figure 4-17: A first-order, single-bit, ΣΔ frequency to digital converter quantizer controlling the class-D stage.

characteristics of the analog loop filter, without the need for an additional integrator. From [52], the reference clock phase noise generates a baseband component as well as a sideband frequency error.

The impact of reference clock phase noise can be verified by deriving Spurious-Free Dynamic Range (SFDR) of the output bitstream in the frequency discriminator. The worst case SFDR due to the reference clock phase noise is related to a strong baseband tonal content associated with the reference clock FM jitter and can be represented by

$$SFDR = -20\log(\frac{m_1 f_1 f_{ref}}{m_2 f_2 f_c}) \tag{4.27}$$

where f_{ref} is the reference frequency, f_1 is the modulating frequency, f_2 is FM jitter frequency, m_1 is the modulation index of the input frequency, and m_2 is the FM jitter frequency modulation index.

Assuming a jitter-free sampling clock, the theoretical Signal-to-Quantization Noise Ratio (SQNR) of the D-flip-flop DNSQ is defined as

$$SQNR = 20\log(\frac{3}{2\pi}) + 20\log(\frac{\Delta f}{f_{bw}^{1.5}}) + 10\log(f_{ref}) \tag{4.28}$$

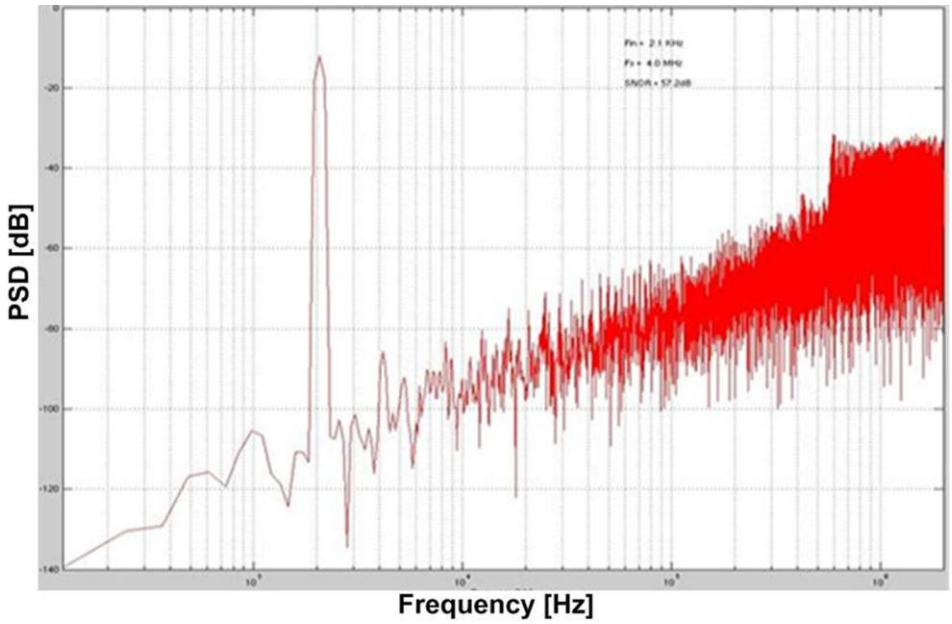

Figure 4-18: Power spectral density of a 1-bit digital frequency discriminator.

where Δf is the maximum frequency deviation from f_c when the maximum input voltage is applied and f_{bw} is the bandwidth of the modulating signal at the ICO input. As shown in equation (4.28), SQNR can be increased by increasing clock frequency and the frequency deviation of the ICO.

4.7 Output Stage and Filter Design

The sizes of output devices in the power stage are large for small on-resistance and they result in large gate capacitance. Therefore, the need for the cascade buffer architecture is required to drive the output power stage. Figure 4-19 shows the cascade buffer architecture which consists of a chain of N inverters. The capacitance and time constant of each stage are

$$\begin{aligned} C_k &= \beta^{k+1} C_i \\ \tau_k &= \beta \tau_i \end{aligned} \tag{4.30}$$

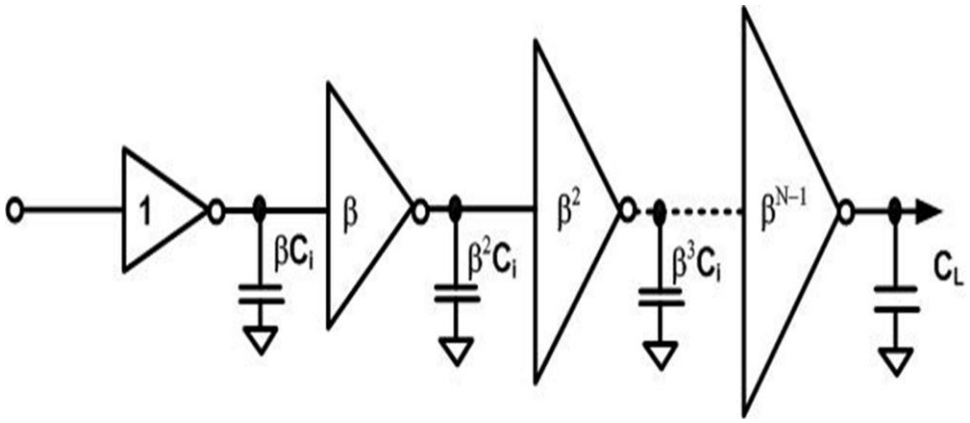

Figure 4-19: Cascade buffer architecture.

where C_i and τ_i are capacitance and time constant of the minimum (unit) size inverter, respectively [53][54]. β is the ratio of *W/L* of stage *(k+1)* to *W/L* of stage *k* :

$$\beta = \frac{\left(W/L\right)_{k+1}}{\left(W/L\right)_k} \tag{4.31}$$

The load capacitance at the output stage (C_L) is

$$C_L = \beta^N C_i \tag{4.32}$$

The overall time constant is given as

$$\tau_o = \tau_i \ln\left(C_L / C_i\right)\frac{\beta}{\ln\left(\beta\right)} \tag{4.33}$$

The output stage of the dead-time generator can drive 0.032pF of the load capacitance. Thus, the input capacitance of the minimum size inverter, C_i, is 0.032pF. C_L

Table 4-1

The parameter of the minimum size inverter

W_p	76 μm
W_n	24 μm
C_i	0.032 pF

is 8pF, which is obtained from SPICE simulation. When β is equal to 4, the optimized stage, *N*, is 4 from equation (4.32). Table 4-1 shows the minimum size inverter.

The external output filter in the class-D amplifier is used to attenuate the high frequency switching component while passing the audio signals. This goal can be achieved by the Butterworth low-pass filter that has the advantage of the very flat pass-band response. Since a differential filter (called a balanced filter) consists of two identical filters in BTL structures, a half-circuit model for the low-pass filter design can be used. The half-circuit model is shown in Figure 4.20.

The transfer function of a second-order Butterworth approximation is

$$H(s) = \frac{1}{s^2 + \sqrt{2}\, s + 1} \tag{4.34}$$

From Figure 4-20, the transfer function is given as

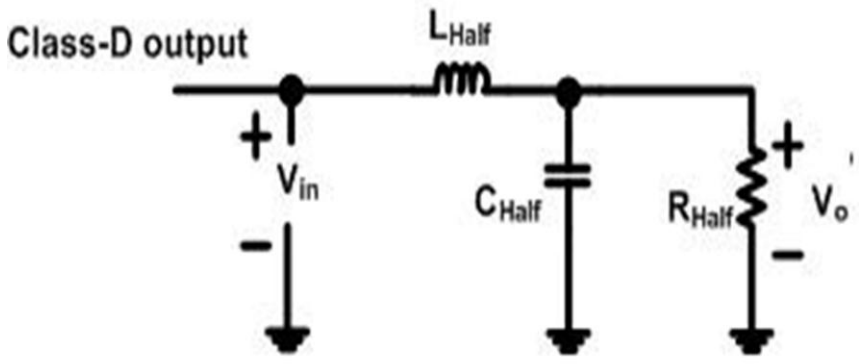

Figure 4-20: Half-circuit model for the low-pass filter.

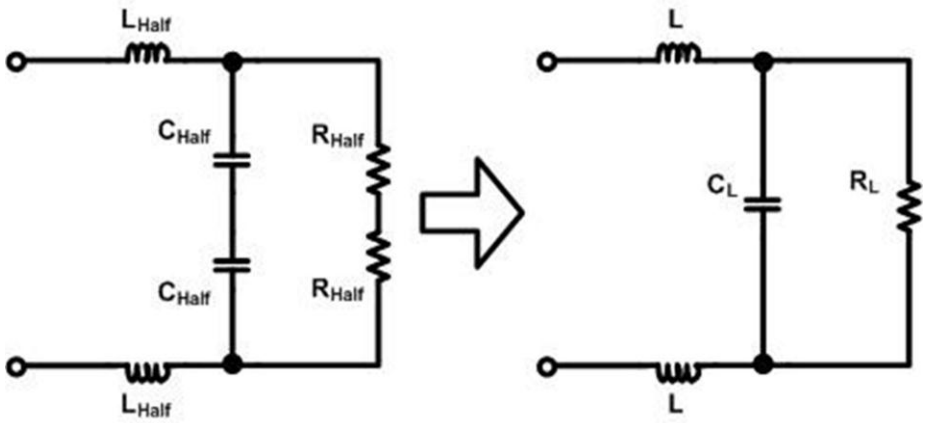

Figure 4-21: The balanced filter with two identical half filters.

`q2w2qq1q

$$H(s)=\frac{V_o(s)}{V_{in}(s)}=\frac{\dfrac{1}{L_{HALF}C_{HALF}}}{s^2+\dfrac{1}{R_{HALF}C_{HALF}}s+\dfrac{1}{L_{HALF}C_{HALF}}} \tag{4.35}$$

From comparing between equations (4.34) and (4.35), the half circuit values for C_{HALF} and L_{HALF} are obtained when ω_0= 1 rad/sec, like in the equations below.

$$\left.\begin{aligned} C_{HALF} &= \frac{1}{\sqrt{2}R_{HALF}} \\ L_{HALF} &= \frac{1}{C_{HALF}} \end{aligned}\right|_{\omega_0=1[rad/\sec]} \tag{4.36}$$

The equation (4.36) needs to be frequency scaled by dividing through by $\omega_0= 2\pi f_C$. The equation (4.37) is finally derived:

$$\begin{aligned} C_{HALF} &= \frac{1}{2\pi f_C\sqrt{2}R_{HALF}} \\ L_{HALF} &= \frac{\sqrt{2}R_{HALF}}{2\pi f_C} \end{aligned} \tag{4.37}$$

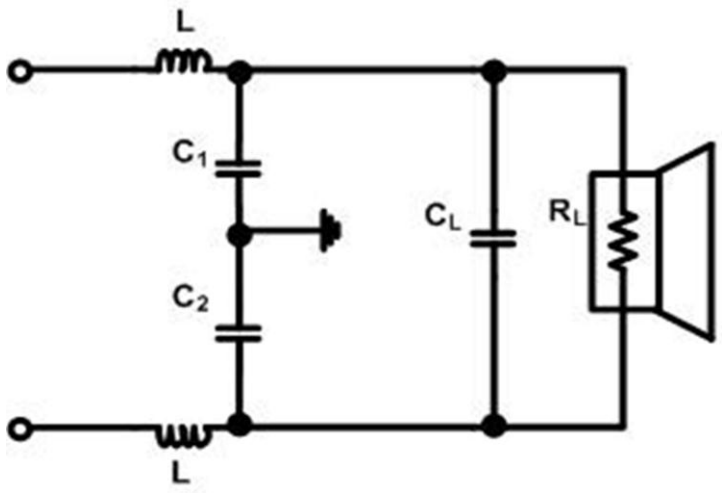

Figure 4-22: The output filter for the proposed class-D amplifier.

where f_C is the cutoff frequency [55]. The balanced filter model is obtained from using two half circuit models as shown in Figure 4.21. Their relation are defined as

$$\begin{aligned} R_L &= 2R_{HALF} \\ C_L &= \frac{C_{HALF}}{2} = \frac{1}{2 \cdot 2\pi f_C \sqrt{2} R_{HALF}} \\ L = L_{HALF} &= \frac{\sqrt{2} R_L}{2 \cdot 2\pi f_C} = \frac{\sqrt{2} R_{HALF}}{2\pi f_C} \end{aligned} \tag{4.38}$$

Since the -3dB cutoff frequency of the balanced filter should be the same as that of the half-circuit model, the -3dB cutoff frequency for the LC filter, based on the balanced filter, is given as

$$f_C = \frac{1}{2\pi\sqrt{L_{HALF} C_{HALF}}} = \frac{1}{2\pi\sqrt{2LC_L}} \tag{4.39}$$

Figure 4- 22 shows the low-pass filter used in the proposed class-D amplifier. C_1 and C_2 provide a high-frequency short to ground as the high frequency bypass capacitors. These capacitors should be approximately $0.2C_L$ [55].

From the equations above, the values of discrete components are obtained: L = 22µH, C_L = 1µF, and C_1= C_2 = 0.22 µF for R_L =4 and f_C = 24 kHz. It is important for the

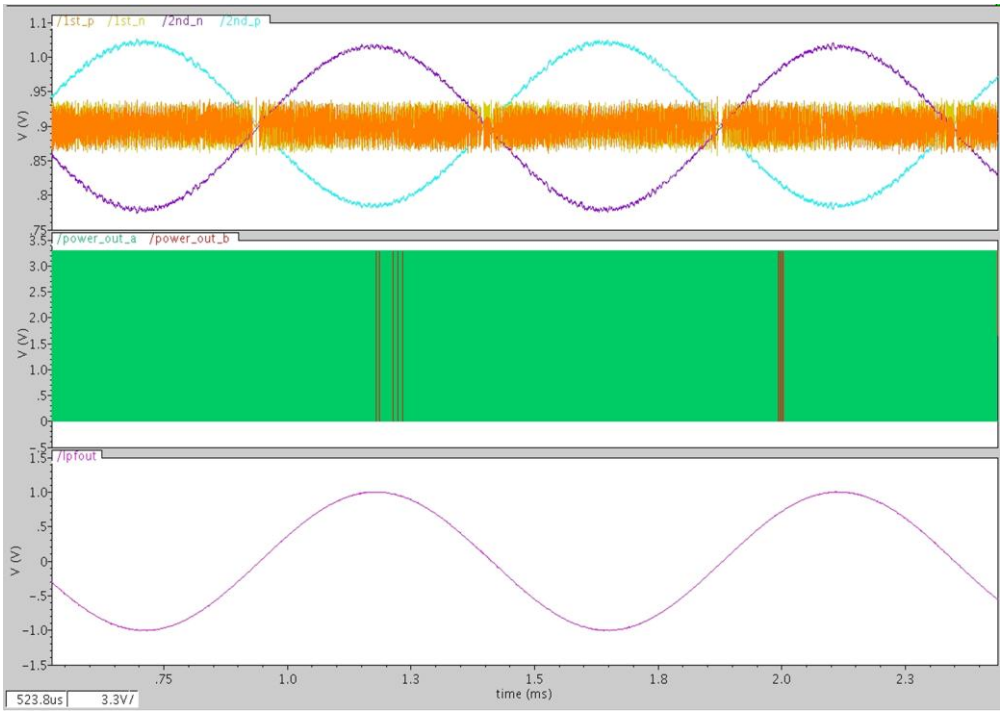

Figure 4-23: The top level transient domain simulation results.

inductor to have a low ESR since it is in series with the speaker load and its DC current rating should be greater than or equal to the maximum current flowed through it.

Figure 4.23 shows the top-level simulation results related to node voltages in the outputs of the first and the second integrators (*1st_p*, *1st_n*, *2nd_p*, and *2nd_n*), the power output stage (*power_out_a* and *power_out_b*), and the final signal (*lpfout*) after passing through the low-pass filter.

4.8 Floor Plan and Layout Consideration

The primary principle of the floor plan is to separate the digital and analog signals as far as possible in order to minimize the effect of the digital switching on the analog circuits. The system performance can be affected by the layout. Thus, some analog layout techniques are employed to minimize degradation of the performance due

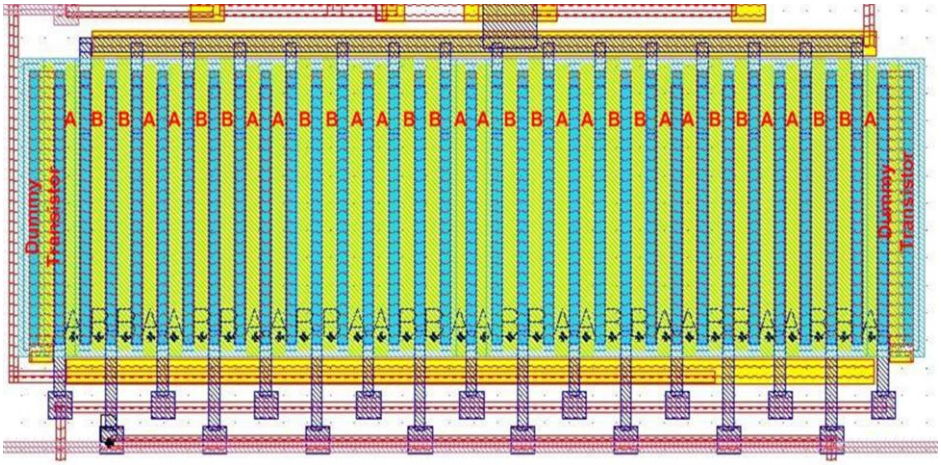

Figure 4-24: Layout of the differential input stage of the OP AMP.

to the layout [56] [57] [58]. The common-centroid layout technique is mainly used and the dummy devices are added at the edges to improve transistor matching. The devices to be matched have the same shape, type, size, and number of contacts, and they consist of multiples of the unit-sized device. In other words, the fully differential circuits are drawn as symmetrically as possible. Figure 4-24 shows the layout of the differential input stage of the OP AMP. Figure 4-25 shows the example of the PMOS arrangement in the H-bridge power stage.

The separated power supplies of analog and digital circuits are used to reduce noise coupling and the orthogonal signal lines are also used to reduce the signal interference between two cross layers.

Figure 4-26 shows the overall layout of the chip that is done on the basis of the guidelines above. The layout size is 1500µm x 1500µm = 2.25 mm^2.

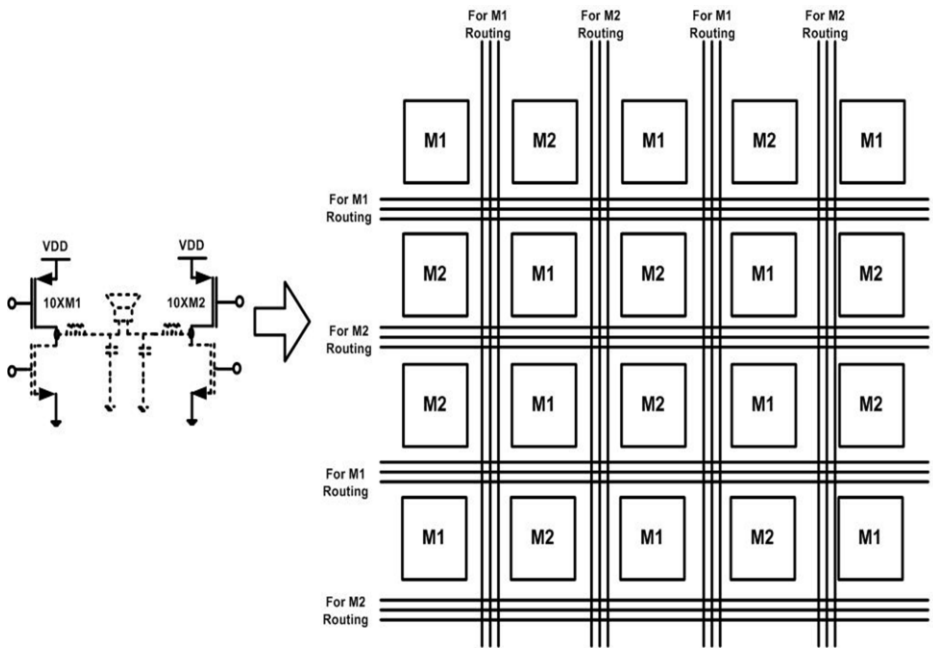

Figure 4-25: The example of the arrangement of the H-bridge power output stage.

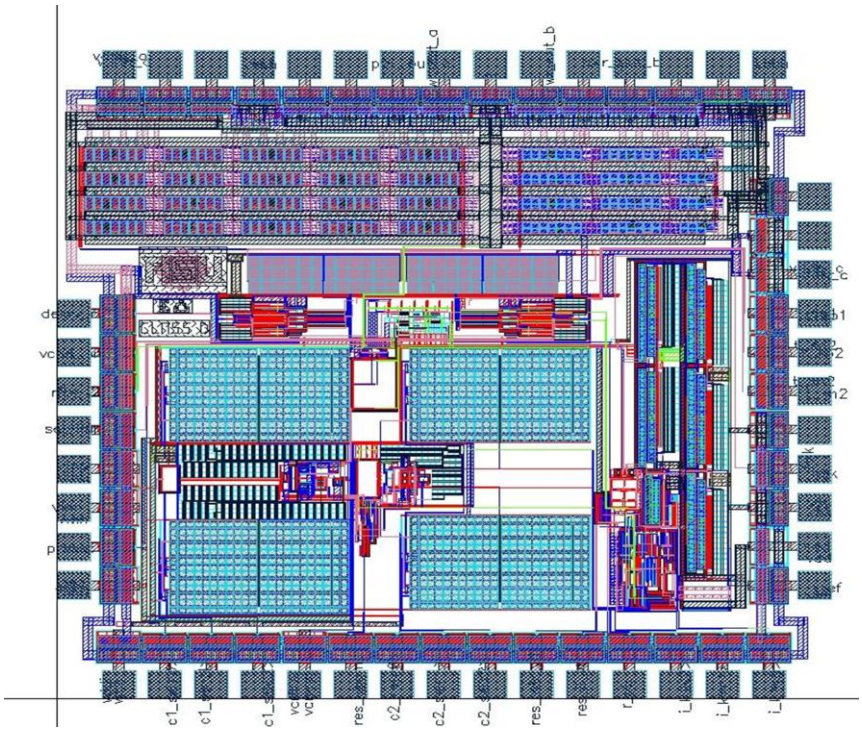

Figure 4-26: The top-level layout of the proposed class-D amplifier.

5 PERFORMANCE OF THE CLASS D AUDIO AMPLIFIER

5.1 Test Setup

Figure 5.1 shows the test setup to characterize the prototype class-D audio amplifier. The input signal is generated by the arbitrary waveform generator (Agilent N8241A AWG). Its output signal is applied to the single-ended to differential amplifier (THS4130). The clock signal is generated by the signal generator (Agilent 33250A). The audio transformer (Hammond 108H) is used to obtain a differential to single-ended output signal in the output of the class-D amplifier. The output of the class-D amplifier is analyzed by using an Agilent 35670A dynamic signal analyzer.

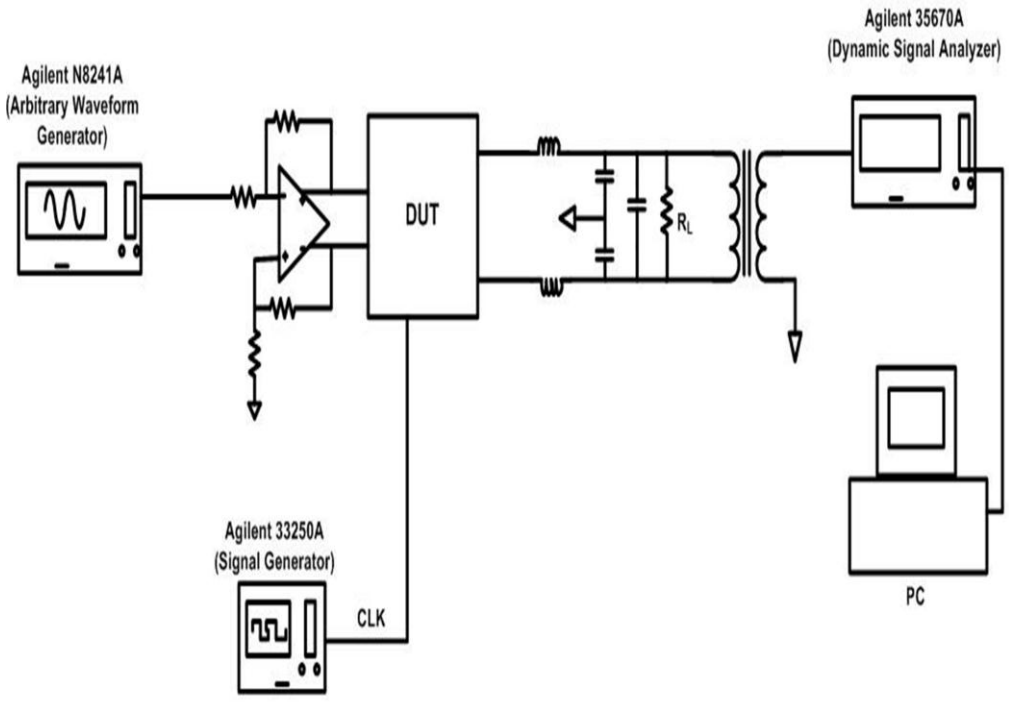

Figure 5-1: Test setup for evaluation of the prototype class-D amplifier.

5.2 Test Results

The proposed class-D amplifier has been implemented in a 0.18 µm digital CMOS process. The IC has been mounted on a FR4 board and a discrete LC output filter is used to remove high-frequency noise components and for signal reconstruction.

Figure 5-2 shows the output power spectrum when a signal with 1-kHz sine wave of 100-mW output power is applied and the output load is 4Ω.

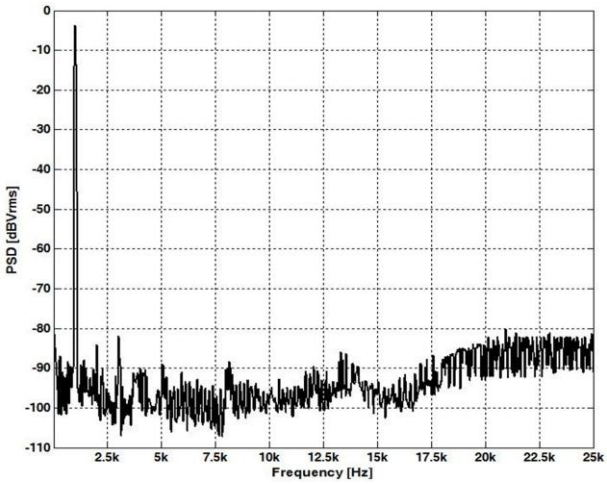

Figure 5-2: Measured power spectrum with a 4Ω load and 100 mW output power.

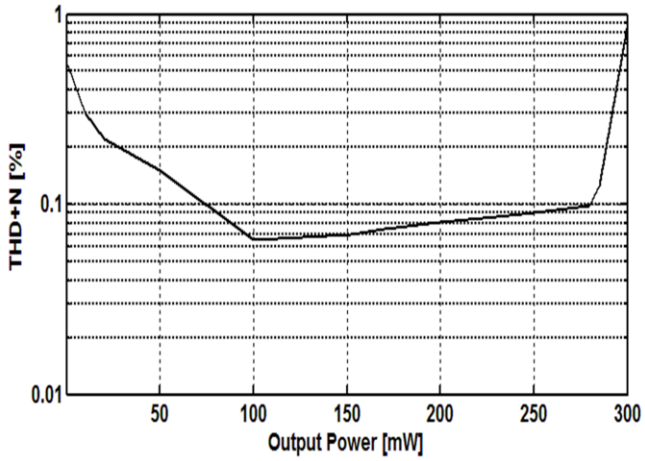

Figure 5-3: Measured THD+N versus Output power.

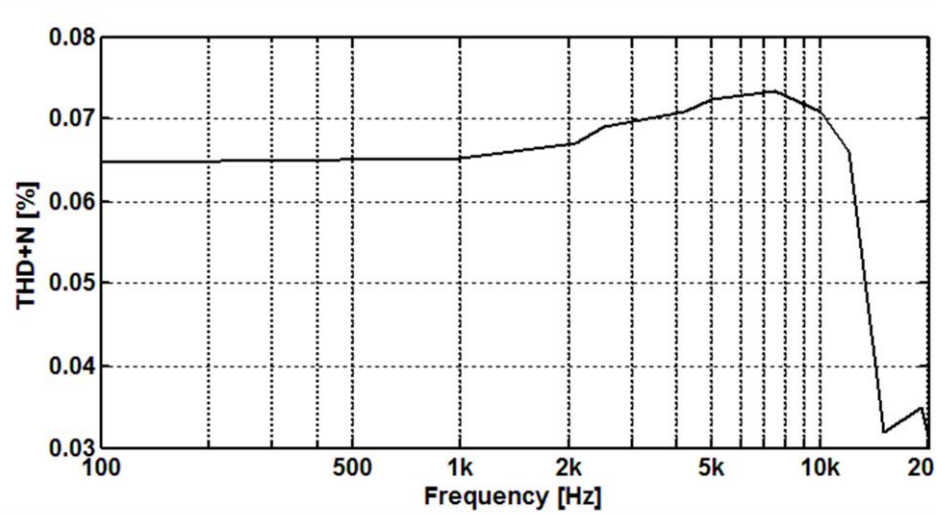

Figure 5-4: Measured THD+N versus frequency.

Figure 5-3 shows THD+N performance against the output power. The lowest THD+N is 0.065 % with a 1-kHz sinusoidal signal. Figure 5-4 shows THD+N according to variation of the input frequency. The improvement of THD+N from around 8 kHz corresponds to the filtering effect of the signal-transfer function on third harmonic distortion. Figure 5-5 shows PSRR versus the ripple frequency when a ripple voltage of

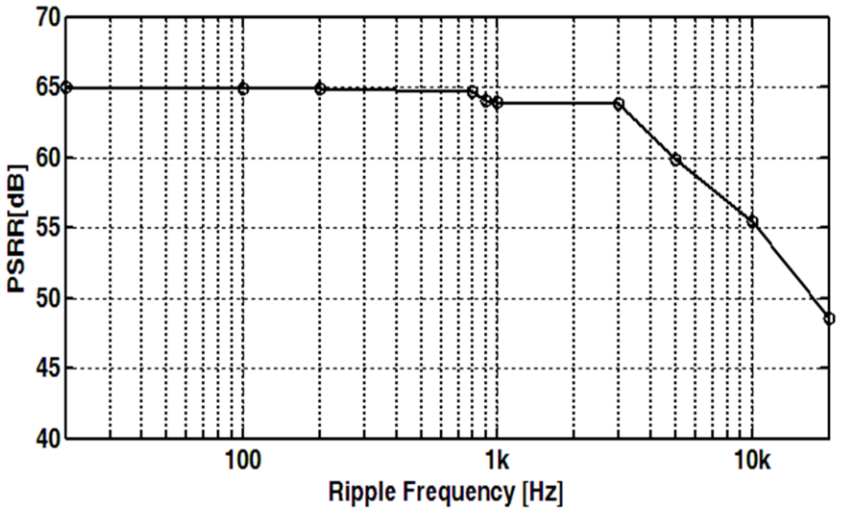

Figure 5-5: PSRR versus the ripple frequency.

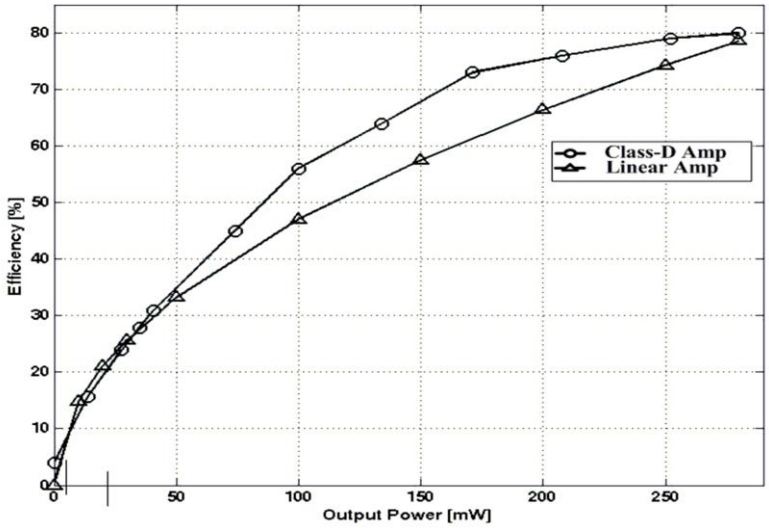

Figure 5-6: The theoretical power efficiencies of the linear amplifier and the measured power efficiency of the propose class-D amplifier with respect to output power.

100 mVpp is added to the power supply and the input is idle. PSRR is approximately 65 dB at 217 Hz.

Figure 5-6 shows power efficiency versus output power. The amplifier achieves 80% peak power efficiency at an output power of 280 mW. The efficiency of the proposed class-D amplifier is better than that of a conventional linear amplifier when the output power is above 40 mW as shown in Figure 5-6. Transient, start-up and clipping characterizations of the proposed class-D amplifier are shown in Figures 5-7 and 5-8, respectively. Both resistive load on the scope and on an actual loudspeaker do not show an audible pop in Figure 5-7. As shown in Figure5-8, output signal recovers gracefully, with no folding or ringing. A comparison between the proposed class-D amplifier and other integrated-audio amplifiers is summarized in Table 5-1. Target application is for portable audio such as 4Ω / 8Ω speaker headphone drivers in handsets. The performance of the proposed system satisfies for this specific application. In [62], the performance is reported to be higher than 0.2% THD+N and 72% efficiency for 280mW, 71dB PSRR at 217Hz. [63] achieves 0.3% THD+N at 200mW, 60dB PSR at 217Hz. The W/L of PMOS

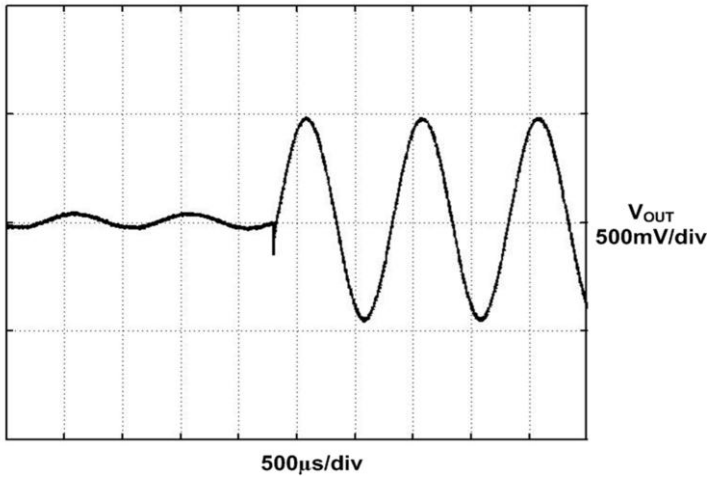

Figure 5-7: Start-up transients for a 1kHz audio input.

and NMOS output devices is 19600/0.34 and 7000/0.34, respectively, giving a total output resistance of 200mΩ. The chip micrograph of the proposed class-D amplifier is shown in Figure 5-9.

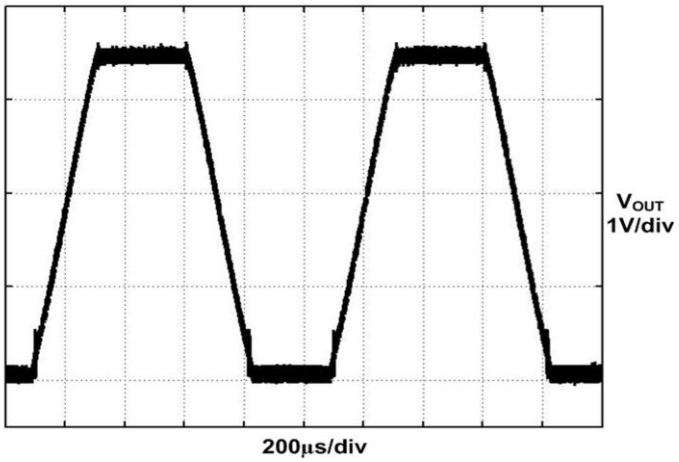

Figure 5-8: Clipping recovery for the proposed class-D amplifier.

Table 5-1

Performance Comparison

Reference	THD +N (%)	Efficiency (%)	PSRR [dB]	Supply (V)	Load (Ω)	Quiescent Power Consumption (mW)	Output power (mW)	Area (mm^2)	Fs (MHz)	Process	Architecture
[14] /2005	0.0015	89[b]	-	5	-	150	-	12.6	5.6	0.35 µm CMOS	7th ΔΣ
[15] /2008	0.02	87	-	3~5.5	4	39	-	6	3.125/ 4	0.35 µm CMOS	5th ΔΣ
[16] /2008	0.022	77	-	3	32	7.7[a]	-	1.6	3.2	0.18 µm CMOS	4th ΔΣ
[59] / 2008	0.10	80	-	3.0~3.6	8	14.85	80	-	3	-	6th ΔΣ
[42] / 2010	0.01	92	80	3.7/5	8	-	-	4	0.35[c]	0.14 µm CMOS	PWM
[60] / 2004	0.05[d]	-	58	1.4 / 5.4	8	-	250	0.77	-	0.09 µm CMOS	PWM
[61] / 2005	0.50	92	85	2.5	8	0.063	450	589.5	>200k Hz	0.5 µm CMOS	RWDM
This Work	0.065	80	65	1.8/3.3	4	14.6 [a]	280	2.25	4	0.18 µm CMOS	2nd ΔΣ w/ Freq. Quantizer

a = Modulator power consumption

b = The ratio of the peak value of the filtered signal to the amplitude of the pulse signal at the output of the power switches

c = PWM carrier frequency

d = THD

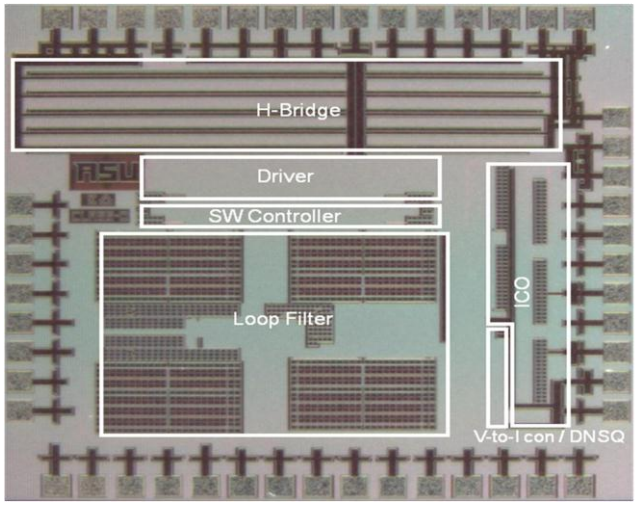

Figure 5-9: Chip micrograph.

6 CONCLUSIONS

The dissertation presents a closed-loop PDM-based class-D audio amplifier with a single-bit, third-order noise-shaped modulator, using a high linearity frequency-domain quantizer.

The nonlinearity of the carrier introduces the harmonic distortion in the PWM-based class-D amplifier. On the other hand, use of higher oversampling-rate, single-bit, PDM drivers only makes a comparison with respect to a fixed digital reference. The single-bit comparison has the characteristic of shaped quantization noise, and the harmonic distortion caused by the nonlinearity of the carrier can be eliminated. PDM modulation minimizes EMI due to the spreading out of the spectral energy of the output signal while the concentrated spectral energy in the switching frequency and its harmonics causes EMI in the PWM-based class-D amplifier.

The modulator of the proposed class-D amplifier is designed in 1.8V. The supply voltage reduction results in lower signal swing and it makes analog circuit design difficult in voltage domain signal processing. However, frequency-domain signal processing offers a better solution than voltage domain signal processing in low voltage design. Thus, the proposed class-D amplifier is based on the frequency-domain signal processing by using an ICO-based frequency discriminator. The proposed approach is a first implementation of the frequency domain quantization in class-D amplifiers.

The proposed class-D audio amplifier is based on a Continuous-Time (CT) modulator. An ICO is operated as a CT integrator and also used as part of a CT loop filter. In the proposed approach an analog comparator and a single-bit quantizer are replaced with an ICO-based frequency discriminator. By using the ICO as a phase integrator, third-order noise shaping is achieved using only two analog integrators. A

digital frequency discriminator is then used to realize a single-bit quantizer instead of an analog comparator. The use of a rail-to-rail oscillator also allows supply voltage reduction, thus enabling highly digital implementations without impacting quantizer accuracy. The proposed class-D amplifier achieves 0.065 % THD+N, 65-dB PSRR at 217 Hz, and 80 % peak power efficiency driving a 4-Ω load.

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APPENDIX A

VERILOG-A CODES

```
************************************************************
SW_Controller_P_type
************************************************************
`include "constants.vams"
`include "disciplines.vams"
// 3 level operation (1.5bit)
module sw_controller_P(qin,clk,swp1,swn1);
input qin, clk;
output swp1, swn1;
voltage qin, clk, swp1, swn1;
parameter real vh = 3.3;
parameter real vl = 0.0;
parameter real Td = 0.0;
parameter real Tt = 10p;
parameter real vth = 1.6;
parameter real vth1 = (vh+vl)/2;
real temp1;
real temp3;
real prep;
real memop;
real memon;

 analog begin
 @(initial_step("static")) begin
  V(swp1) == vh;
```

```
V(swn1) == vl;
memop == vh;   //PMOS - off
memon == vh;   //NMOS - on
end
@(cross(V(clk)-vth, 1)) begin
 if ( V(qin) >=1.5) begin
  temp1 = vl;    // PMOS1- on
  temp3 = vl;    // NMOS1- off
 end
 else if (V(qin) >=0.7) begin
  prep = memop;    // PMOS1- off / on
  if (prep > vth1) begin
   memop = vl;
   memon = vl;
  end
  else begin
   memop = vh;
   memon = vh;
  end

  temp1 = memop;
  temp3 = memon;
 // temp1 = vh;
 // temp3 = vh;
 end
```

```
 else if (V(qin) ==0.0) begin
  temp1 = vh;    // PMOS1- off
  temp3 = vh;    // NMOS1- on
 end
end
V(swp1)<+ transition(temp1, Td, Tt);
V(swn1)<+ transition(temp3, Td, Tt);
end
endmodule

*************************************************************
SW_Controller_N_type
*************************************************************

`include "constants.vams"
`include "disciplines.vams"

module sw_controller_N(qin,clk,swp2,swn2);

input qin, clk;
output swp2, swn2;
voltage qin, clk, swp2, swn2;

parameter real vh = 3.3;
parameter real vl = 0.0;
```

```
parameter real Td = 0.0;
parameter real Tt = 10p;
parameter real vth = 1.6;
parameter real vth1 = (vh+vl)/2;

real temp1;
real temp3;
real prep;
real memop;
real memon;

 analog begin
 @(initial_step("static")) begin
  V(swp2) == vh;
  V(swn2) == vl;
  memop == vh;   //PMOS - off
  memon == vh;   //NMOS - on
  end

 @(cross(V(clk)-vth, 1)) begin

   if ( V(qin) >=1.5) begin
    temp1 = vh;    // PMOS2- off
    temp3 = vh;    // NMOS2- on
   end
```

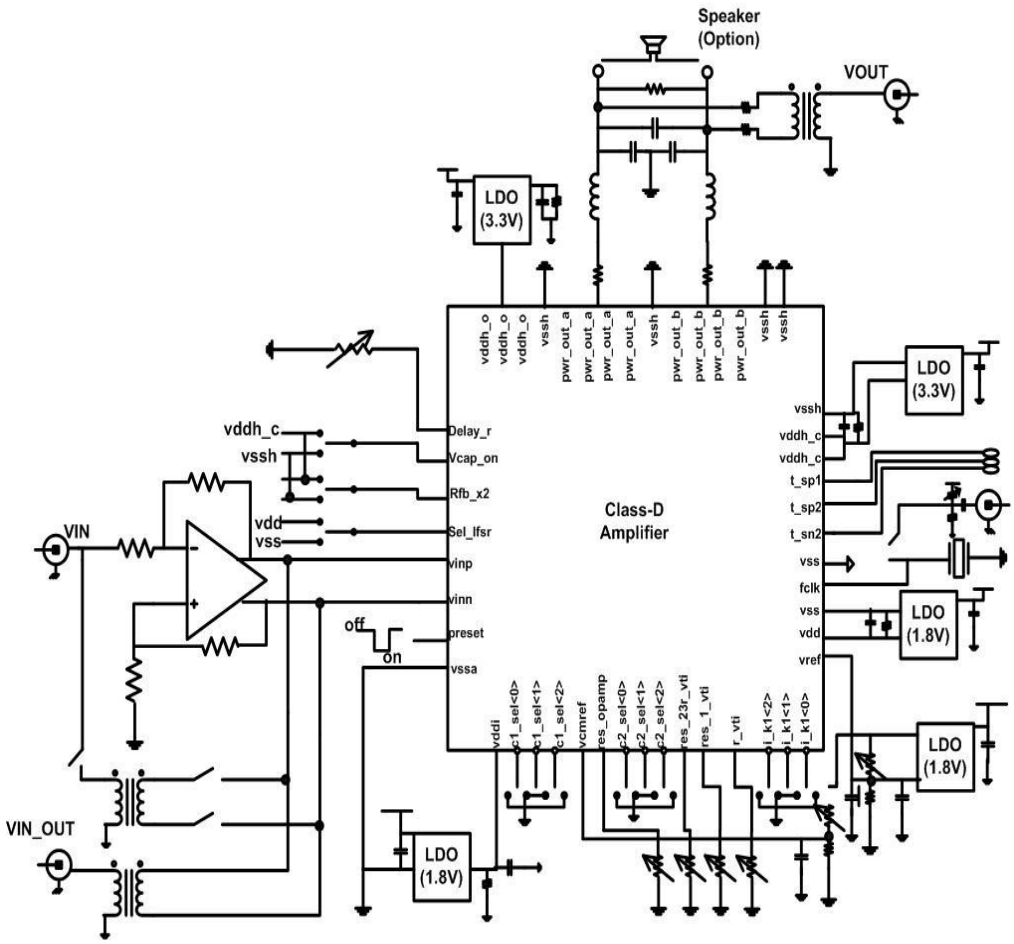
```
 else if (V(qin) >=0.7) begin
  prep = memop;    // PMOS2- off / on
  if (prep > vth1) begin
   memop = vl;
   memon = vl;
  end
  else begin
    memop = vh;
    memon = vh;
  end

  temp1 = memop;
  temp3 = memon;
 end

 else if (V(qin) ==0.0) begin
  temp1 = vl;    // PMOS2- on
  temp3 = vl;    // NMOS2- off
 end
end

V(swp2)<+ transition(temp1, Td, Tt);
V(swn2)<+ transition(temp3, Td, Tt);
end
```

```
endmodule

**************************************************************
                    For inverter in ring oscillator
**************************************************************
`include "constants.vams"
`include "disciplines.vams"

module inv_for_vco_1_8_frunning(in,out,vtune1, vtune2);

output out;
input in,vtune1, vtune2;
voltage in,out,vtune1, vtune2;

parameter real tt=1e-9;
parameter real vh=1.0;
parameter real vl=-1.0;
parameter real in_val=-1.0;
parameter real vth=0.0;
parameter real kv=1000e3;
parameter real finit=1000e3;

parameter real num=3;
real temp;
real td;
```

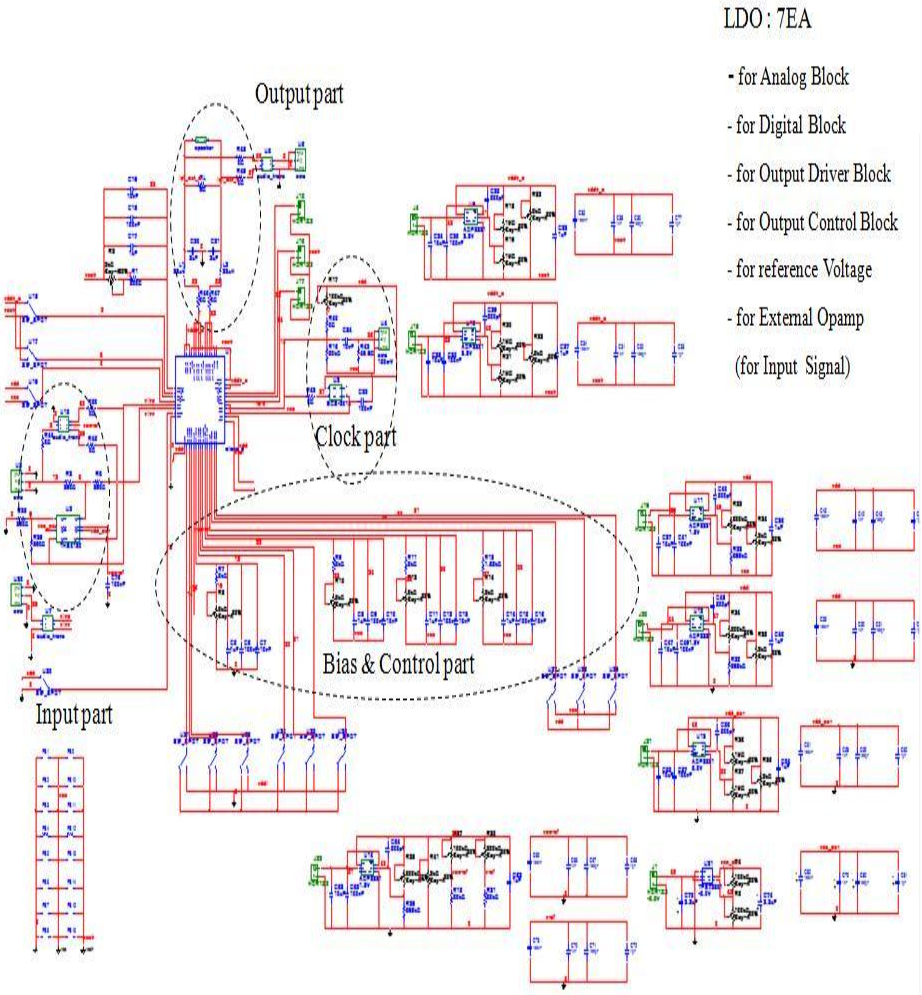
```
analog begin
//@(cross(V(in)-vth,0))
if(V(in)>vth)
   temp=vl;
else
   temp=vh;

@(initial_step) begin
   temp=in_val;
      td = 0;
end
 td = 1/(2*num*(kv*(V(vtune1)-V(vtune2))+finit));
if(td <0)
 td = 0;
else
 td = 1/(2*num*(kv*(V(vtune1)-V(vtune2))+finit));
V(out)<+transition(temp, td,tt);

end
endmodule
```

APPENDIX B

TEST CHIP APPLICATION, BOARD SCHEMATIC, AND PCB LAYOUT


Speaker
(Option)
VOUT
LDO
(3.3V)
vddh_o
vddh_o
vddh_o
vssh
pwr_out_a
pwr_out_a
pwr_out_a
vssh
pwr_out_b
pwr_out_b
pwr_out_b
vssh
vssh
LDO
(3.3V)
vddh_c
vssh
VIN
vdd
vss
Delay_r
Vcap_on
Rfb_x2
Sel_Ifsr
vinp
vinn
preset
vssa
off
on
Class-D
Amplifier
vssh
vddh_c
vddh_c
t_sp1
t_sp2
t_sn2
vss
fclk
vss
vdd
vref
LDO
(1.8V)
vddi
c1_sel<0>
c1_sel<1>
c1_sel<2>
vcmref
res_opamp
c2_sel<0>
c2_sel<1>
c2_sel<2>
res_23r_vti
res_1_vti
r_vti
i_k1<2>
i_k1<1>
i_k1<0>
LDO
(1.8V)
VIN_OUT
LDO
(1.8V)

BOARD SCHEMATIC



PCB LAYOUT