Studies of Epitaxial Silicon Nanowire Growth at Low Temperature

by

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A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved June 2011 by the
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August 2011

ABSTRACT

Silicon nanowires were grown epitaxially on Si (100) and (111) surfaces using the Vapor-Liquid-Solid (VLS) mechanism under both thermal and plasma enhanced growth conditions. Nanowire morphology was investigated as a function of temperature, time, disilane partial pressure and substrate preparation. Silicon nanowires synthesized in low temperature plasma typically curved compared to the linear nanowires grown under simple thermal conditions. The nanowires tended bend more with increasing disilane partial gas pressure up to 25 $x10^{-3}$ mTorr. The nanowire curvature measured geometrically is correlated with the shift of the main silicon peak obtained in Raman spectroscopy. A mechanistic hypothesis was proposed to explain the bending during plasma activated growth. Additional driving forces related to electrostatic and Van der Waals forces were also discussed. Deduced from a systematic variation of a three-step experimental protocol, the mechanism for bending was associated with asymmetric deposition rate along the outer and inner wall of nanowire. The conditions leading to nanowire branching were also examined using a two-step growth process. Branching morphologies were examined as a function of plasma powers between 1.5 W and 3.5 W. Post-annealing thermal and plasma-assisted treatments in hydrogen were compared to understand the influences in the absence of an external silicon source (otherwise supplied by disilane). Longer and thicker nanowires were associated with longer annealing times due to an Ostwald-like ripening effect. The roles of surface diffusion, gas diffusion, etching and deposition rates were examined.

ACKNOWLEDGMENTS

I would like to thank my advisor, William T. Petuskey for taking care of me always, supporting me through difficult times, and most importantly for keeping faith and encouraging me in my research ideas. I truly appreciate his advising throughout my graduate research work, helping me to stay on course. Also, I express my appreciation to Dr. Jeff Drucker and Dr. Andrew Chizmeshya for their advice and attention to my dissertation.

I would also like to thank David Wright for his help in rebuilding my LPCVD chamber, as well as, his advice in maintaining it. I also thank Tim Karcher for his creative solutions of problems related to LPCVD chamber and pumps. I also gratefully acknowledge the Center for Solid State (CSSS) and Center for Solid State Engineering Research (CSSER) for research facility support. I am especially grateful to my working group members -- Feng, Alicia, Nicole, and Reddy.

I would like to thank my family, Timo (Choong-do), Jeong-Gi, Ji-Hae, Ka-Hyun, and my parents for their constant and continuing emotional support at all times during my graduate studies here in the US.

Finally, I thank God for everything, especially for His unswerving provision of guidance and protection and grace.

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Chapter 1

Introduction

1.1 Nanotechnology Background

The field of nanotechnology represents an exciting and rapidly expanding research area that crosses the boundaries between the physical, life and engineering sciences.[1] Much of the excitement in this area has arisen from the recognition that new phenomena and unprecedented integration density are possible with nanometer scale structures. Correspondingly, these ideas have driven scientists to develop methods for making nanostructures. In general, there are two approaches for creating small objects, which can be characterized as top-down and bottom-up (Figure 1.1).[1, 2]

In the top-down approach, small features are patterned onto bulk materials by combining lithography, etching and deposition to form functional devices as shown in Figure1.2 (a). It has been exceedingly successful in many venues with microelectronics being perhaps that the best example today. While developments continue to push the resolution limits, these improvements are associated with a near exponential increase in cost associated with each new level of manufacturing. Economic limitations and other scientific issues have motivated efforts worldwide to search for new strategies to meet the demands for nanoscale structures today and in the future.[3, 4]

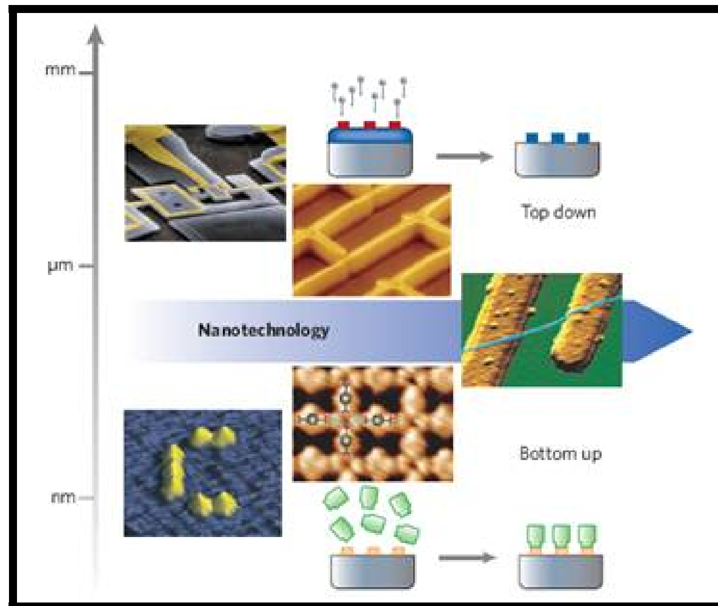


Figure 1.1 General approach of Top-down and Bottom-up in Nanotechnology.[1]

The bottom-up approach (Figure 1.2 (b)), involves assembling functional electronic structures from chemically synthesized, well-defined nanoscale building blocks, much like the way nature uses proteins and other macromolecules to construct complex biological systems. This approach represents a powerful alternative to conventional top-down methods.[1, 5] It has the potential to go far beyond the limits of top-down technology by defining key nanometer scale metrics through synthesis and subsequent assembly that does not involve lithography.

To enable this bottom-up approach, a focus on three key areas is required, which are at the heart of devices and integration (Figure 1.3). First, the bottom-up approach necessitates developing nanoscale building blocks with precisely

controlled and tunable chemical composition, structure, size, and morphology, since these characteristics determine their corresponding physical properties. Second, it is critical to develop and explore the limits of functional devices based on these building blocks. Nanoscale structures may behave in ways similar to current electronic and optoelectronic devices, although it is also expected that new and potentially revolutionary concepts might also emerge due to the increased quantum mechanical nature at smaller and smaller dimensions. Third and central to the bottom-up concept will be the development of architectures that enable high-density integration with predictable function, and the development of hierarchical assembly that organizes building blocks into these architectures.[1]

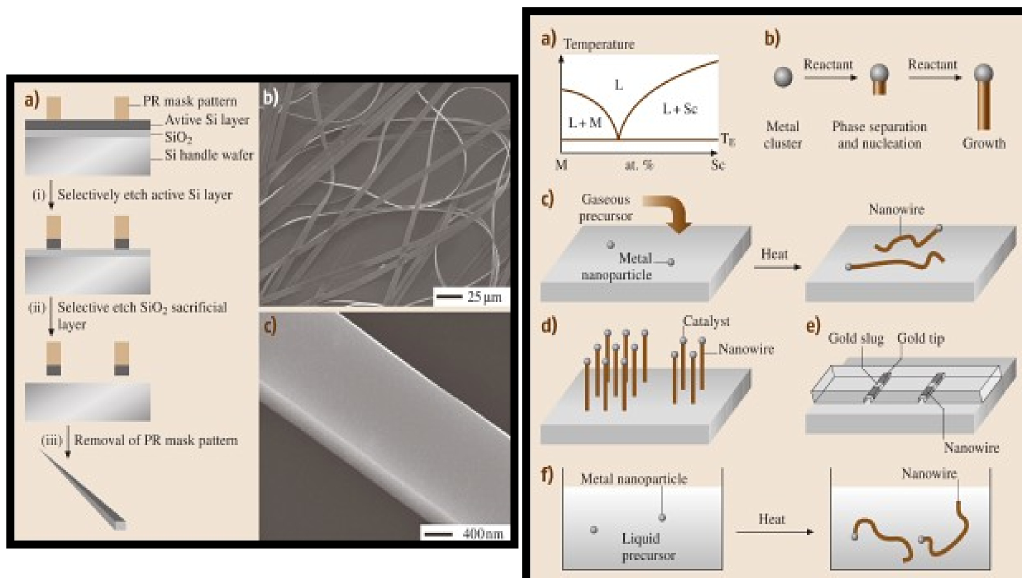


Figure 1.2 **(Left)** Process of Top-down Nanofabrication. (a) rectangular nanowires (or nanoribbons) from high-quality wafers with multiple layers: active semiconductor (Si), sacrificial layer (SiO_2) and handle wafer (Si). (b), (c) SEM images of silicon ribbons with thicknesses of 100 nm and widths of 1 µm

fabricated from commercial SOI wafers through the processes in (a). PR:photoresist **(Right)** Process of bottom-up nano-synthesis of single crystalline nanowires of semiconductors by the use of metal nanoparticle catalysts. (a) Binary metal-semiconductor phase diagram used to select a catalyst for growth of semiconductor nanowires. (b) Schematic illustration of the steps of catalytic growth of semiconductor nanowires. (c) Growth of semiconductor nanowires on substrates, which can withstand high temperatures (higher than the eutectic point of alloy of metal and semiconductor), by feeding the system with gaseous precursors. This synthesis is referred to as the vapor-liquid-solid (VLS) process. (d) Preferential growth of a vertically oriented nanowire array on a single crystal substrate through the VLS process. (e) Growth of horizontal nanowires in template channels through the VLS process. (f) Growth of nanowires in a solvent with high boiling point by delivering liquid precursors to catalyst.[5, 6]

Figure 1.3 Schematic outlining key challenges (open rectangular) and specific research areas (ellipses) required to enable the bottom-up approach to functional nanosystems.[6]

Addressing and overcoming the hurdles in these three major areas of the bottom-up approach could revolutionize a wide range of technologies of today. Moreover, it is very likely that the bottom-up approach will enable entirely new device concepts and functions, thereby creating technologies that have not been imagined. For example, it is possible to seamlessly combine chemically distinct, nanoscale building blocks, which could not otherwise be integrated in a top-bottom approach.

1.2. Nanowire Building Blocks

Individual molecules and quantum dots,[7] which can be classified as zero dimension (0D) structures, are attractive building blocks for bottom-up assembly of nanoscale electronics. These 0D structures have been intensively pursued over the past decade since they represent the smallest building blocks with correspondingly high potential for integration. However, the uses of individual molecules or quantum dots in integrated systems have been limited due to challenges in establishing reliable electrical contact. Thus, it has been difficult to elucidate and understand the intrinsic properties of individual devices, and to develop and demonstrate realistic schemes for scalable interconnection and integration of 0D devices into functional architectures.[4]

1.2.1 Two-dimensional (2D) Superlattice Nanostructures

Superlattices are artificial periodic structures composed of alternating layers (usually of several-to-tens of nanometers in thickness) of different materials grown generally by molecular beam epitaxy (MBE) or molecular organic chemical vapor deposition (MOCVD). The electronic, optoelectronic, and thermal properties of nanostructures can be tuned for specific applications by varying material combinations and layer thicknesses. For instance, Figure 1.3 (a) shows a cross-section transmission electron microscopy image of the Ⅲ-Ⅴ layers.[4, 7]

1.2.2 One-dimensional (1D) Nanotubes and Nanowires

One-dimensional nanostructures have also been the focus of extensive investigations worldwide due to their unique physical properties and potential to revolutionize broad areas of nanotechnology.[7] Firstly, one-dimensional nanostructures represent the smallest structure that can efficiently transport electrical carriers and, thus, are ideally suited for the critical task of directing charges within integrated nanoscale systems. Secondly, 1D nanostructures can serve functions such as for nano-scaled electronics.[5] In this regard, two classes of materials, i.e., carbon nanotubes and semiconductor nanowires (Si or Ge nanowires), have shown particular promise (Figure 1.3 (b)). For example, germanium nanowires have been used to fabricate field effect transistors, diodes, and logic circuits.[4, 7]

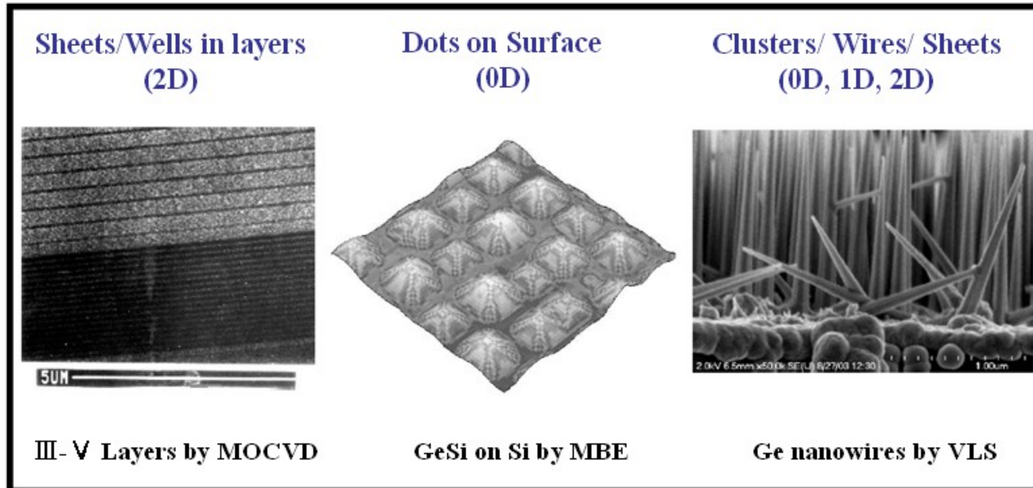


Figure 1.4 Nanowire Building Blocks (a) III-V layers by MOCVD (b) GeSi on Si wafer by MBE (c) Ge nanowires by VLS.[8]

1.2.3 Zero-dimensional (0D) Quantum Dots

A quantum dot is a semiconductor whose excitations are confined in all three spatial dimensions. As a result, they have properties that are between those of bulk semiconductors and those of discrete molecules.[3,4] They can be thought of as tiny boxes with a dimension less than 100 nm space, as is shown in Figure 1.3 (b) of an atomic force microscopy (AFM) image of SiGe nanodots on Si wafer and Figure 1.3 (c) Ge nanoclusters. Quantum dots represent perhaps the ultimate component in miniaturizing electronic circuits. The number of free electrons contained in these boxes can be varied from one to a few hundreds. Transport through a quantum dot with only one electron can be used as a single electron device, such as, a transistor for superior sensitivity.[4, 7]

1.3 Silicon Nanowires

Semiconductor nanowires typically have nanometer diameters (10^{-9} meters) and lengths of up to several micrometers. These 1D components are the fundamental building blocks for nanoscale architectures as already discovered, however, our current understanding of the mechanisms and materials science controlling their fabrication is limited. Recent studies demonstrate that controlling size, morphology, and crystallographic orientation are critical in advancing the science of nanowire growth. Among all potential materials, silicon nanowires have attracted the most attention due to interesting properties that are different than for bulk materials.[3]

Silicon plays an important role in the semiconductor industry and current technologies, making it possible for integration with electronic devices. Silicon nanowires have unique physical and electronic properties along with the potential for device applications including biosensors, chemical sensors, transistors, and light-emitting devices. Silicon nanowires have been synthesized by a variety of methods including laser ablation, thermal evaporation, chemical vapor deposition (CVD), and plasma enhanced CVD. The most widely used method is chemical vapor deposition (CVD) using the vapor-liquid-solid (VLS) growth mechanism.

1.3.1 Vapor-Liquid-Solid (VLS) Growth Mechanism

In the VLS process, liquid gold is commonly employed as a catalyst to enhance nanowire growth and to control the nanowire diameter. The main aspect

of the growth mechanism is the formation of a liquid metal alloy at the nanowire tip. The Au-Si binary phase diagram indicates that liquid alloy droplets will equilibrate with pure silicon at temperatures higher than the eutectic temperature 363 °C and liquid compositions greater than 16.6 % silicon [Figure 1.5].[2, 3]

Silicon atoms from gaseous disilane (Si_2H_6) or silane (SiH_4) precursors react at the liquid surface to leave silicon to diffuse through the bead. When the eutectic alloy becomes saturated, silicon precipitates at the liquid-solid interface producing an equilibrium solid/liquid Si/Au-Si alloy interface. There are two active interfaces during nanowire growth, namely, the liquid/solid interface between the eutectic and the nanowire and the gas/solid interface.

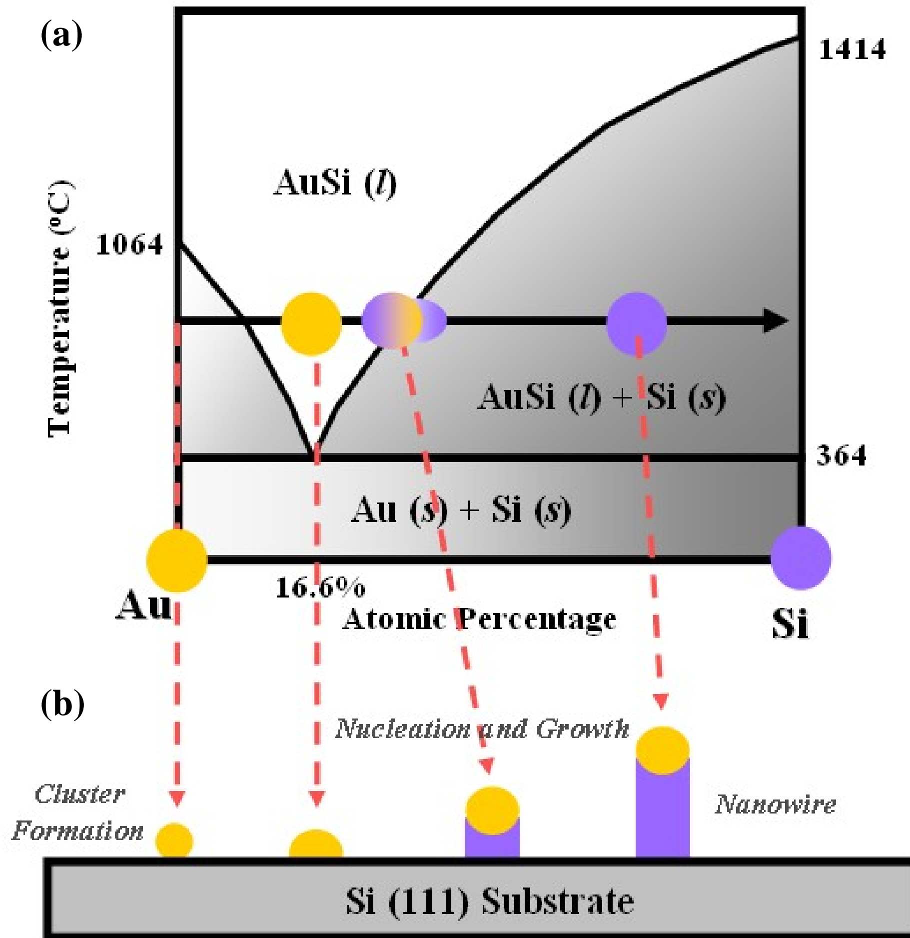


Figure 1.5 Schematic of VLS growth of Si nanowire. (a) Binary phase diagram for Au and Si illustrating the thermodynamics of VLS growth; (b) an AuSi liquid alloy droplet is first formed by absorbing silicon from the vapor phase. Oversaturation of silicon drives the growth of the nanowire at the liquid-solid interface.[3]

Precipitation at the solid-liquid interface results in the axial growth of the nanowire. Silicon is supplied from the gas phase by dissociative adsorption at the gas-liquid interface. Nanowire thickening in the radial direction occurs more slowly, if at all, because gold is rarely present at the nanowire walls to catalyze reaction.

The reaction at either interface can dominate the overall growth process, and depends on the detailed growth conditions such as gas pressure, flow rate, temperature, type of reactant species and gaseous byproducts. For example, in the abovementioned Si nanowire growth process, low temperature growth can reduce the rate of direct thermal dissociation of silane; hence, axial nanowire growth is increasingly favored. Hydrogen has also been found to mitigate radial growth by suppressing either the adsorption of the reactants due to "passive" terminating the Si surface[2, 9] or by hindering the surface dissociation of silane.[9] The use of H_2 as the carrier gas also passivates the nanowire surface in a manner similar to that observed in thin-film growth[4] and coincidentally reduces roughening along the nanowire. Uniform nanowires with negligible diameter variation can thus be achieved through careful control of the growth conditions, including the employment of local heaters to reduce uncontrolled decomposition of silane.[9] On the other hand, tapered nanowires are products from simultaneous growth in both the axial and radial directions. This has been observed in plasma-assisted chemical vapor deposition of silicon nanowires at intermediate temperatures in the vicinity of 500˚C.[10]

Thus, the vapor-liquid-solid mechanism basically consists of three steps: first, the adsorption and cracking of the gaseous silicon precursor to provide atomic silicon for absorption into the droplet; second, the diffusion of the silicon through the droplet; and third, the condensation of silicon onto the silicon wire tip at the liquid-solid interface. Which of these three steps effectively controls the overall growth rate has been the subject of significant discussion and controversy. Generally, it is thought that the diffusion step cannot be rate determining, since liquid diffusion is simply too fast.[10] Concerning the remaining two steps, Bootsma and Gassen[2, 7, 11] favored step one, whereas Givargizov took the opposite opinion where condensation at the liquid silicon interface is rate determining.[2, 11] Regardless as to who is correct, it is clear that under steady state growth conditions the incorporation rate has to equal the condensation rate, which requires some kind of cooperate interaction between both processes. Thus, neither process is thought to be independent nor such discussions are thought to overly simplify the problem. A general description, therefore, has to consider both processes simultaneously in order for a meaningful model to be generated.

1.3.2 Deposition by Epitaxial Growth mechanisms for Si Nanowire

Island growth on a flat silicon wafer surface plays an important part in silicon surface growth and it is also the basis for nanowires growth.[11] For example, in the VLS nanowire growth, metallic nanoparticles, such as gold particles on silicon, behave as catalyst droplets in the presence of a silicon containing gas. They catalyze gas decomposition, leading to the silicon atoms precipitating at the

interface between the gold particle and the semiconductor surface, giving rise to a nanowire growth. While seed particles can be obtained by using Au colloids or dewetting a thin fold film, the growth of Au islands on he Si (111) 7x7 surface offers the unique advantage to control the interface between the Si surface and the Au droplet due to the ultra clean environment.

Typically, epitaxial growth refers to the method of depositing a monocrystalline film on a monocrystalline substrate while maintaining crystallographic alignment. An epitaxial film may be grown from gaseous or liquid precursors. Because the substrate acts as a seed crystal, the deposited film takes on the lattice structure and orientation identical to those of the substrate. If a film is deposited on a substrate of the same composition, the process is called homoepitaxy, otherwise it is called heteroepitaxy.

Based on thermodynamics,[2, 4, 7, 11] the mechanism of epitaxial growth has been separated into three different growth mode categories by Bauer. The description relies on the relative magnitudes of the free energy, E_f, and interface energy, γ. For a clean surface in vacuum, the free energy is given as:

$$E_f = \gamma_i - \gamma_s + \gamma_o \qquad (1.1)$$

Where γ_s is the substrate-vacuum interface energy, γ_i is the overlayer-substrate interface energy and, γ_o is the overlayer-vacuum interface energy. As indicated in Figure 1.6 (a), the three growth modes are:

- Frank-van der Merwe (FM) growth, which correlates with a layer-by-layer growth when $E_f < 0 \rightarrow \gamma_o + \gamma_i < \gamma_s$, as shown in Figure 1.6 (b). Adatoms attach preferentially to surface sites resulting in

atomically smooth, fully formed layers continuously cover the surface. An experimental example of this growth behavior is the deposition of Ag on Pt (111).

- Volmer-Weber (VW) growth, which is observed when $E_f > 0 \rightarrow \gamma_o + \gamma_i > \gamma_s$ [Figure 1.6 (c)]. In this case, adatom-adatom interactions are stronger than those of an adatom with the surface. This leads to the formation of three-dimensional clusters or islands. Growth of these clusters, along with coarsening, will cause rough multi-layer films to grow on the substrate surface. An example is the growth of Pb islands on graphite.
- Stranski-Krastanov (SK) growth, which is an intermediate process characterized by both 1D layer and 3D island growth mechanisms, as illustrated in Figure 1.7 (d). Transition from the layer-by-layer to island-based growth occurs at critical layer thickness where $\gamma_o + \gamma_i > \gamma_s$. Therefore, the SK mode is accompanied by a crystallographic change to the bulk lattice structure of the film at a critical thickness. This induces an abrupt increase in free energy at the interface between the two crystal structures and changes the energy balance in favor of 3D growth. An experimental example for this mode is the growth of Ge on Si (100).

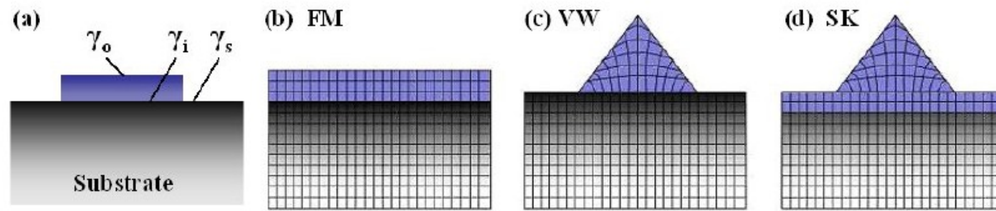


Figure 1.6 Growth modes (a) Surface energy is of three different interfaces (b) Frank-van der Merwe growth (c) Volmer-Weber growth and (d) Stranski-Krastranov growth[4]

1.3.3 Surface Diffusion

The migration of individual atoms across solid surfaces and their aggregation into clustered nuclei are among the most fundamental processes in surface science.[11] A detailed understanding of these basic processes becomes even more important as we attempt to control the growth of semiconductor nanowires, specifically the nanowire diameters, which are governed by the catalyst nanocluster diameter. The fabrication of these nanostructures by the VLS mechanism requires an atomic-level understanding of surface diffusion of the catalytic seed atoms and substrate adatoms across the surface.[2, 7, 11]

Fundamental surface processes such as surface diffusion, adsorption, and desorption define the kinetics for clustering on surfaces, and these three are functions of temperature and deposition rate. Adatoms migrating on an atomically clean sample surface have a characteristic surface diffusion coefficient, which is

determined by temperature and characteristic of the diffusion, activation energy, as described by the equation.[4, 7]

$$D = \frac{v a_0^{\,2}}{4} \exp\left(\frac{-E_d}{k_B T}\right) \qquad (1.2)$$

Here, E_d is the diffusion activation energy and v is the characteristic vibrational energy of the surface atoms. a_o, k_B, and T have their regular meanings, that is, substrate lattice constant, Boltzmann's constant, and substrate temperature, respectively. Effectively the surface diffusion coefficient increases with increasing temperature and decreases when the coordination of the mobile surface adatom increases – for example, when the adatom bonds with other atom(s) on surface steps or within clusters.

The surface diffusion length, $1 \propto \sqrt{Dt}$, where D in our case is the characteristic surface diffusion coefficient of gold adatoms on the silicon substrate, shows that longer diffusion distances occur with longer average diffusion times or with an increase in diffusion coefficient. Consider the case where a monolayer of gold is evaporated onto a substrate at elevated temperature. The diffusion length depends on the time allowed for diffusion, which, in turn, is affected by the deposition of successive layers of material. Thus, the rate of deposition becomes critical. For high deposition rates, the adatoms deposited have less time to diffuse on the surface before encountering other atoms and being locked into position. In addition, there is a high frequency of nucleation events. Hence, the short diffusion length before collisions causes a high density of clusters on the surface (similar effects occur as a result of low deposition temperatures, as this decreases the

diffusion coefficient). Alternatively, at low deposition rates or high substrate temperatures, the Au atoms have more time to diffuse over a larger area, effectively correlating with a lower density of clusters on the surface. [2, 7, 11]

1.3.4 Gibbs-Thomson Effect

In the 1920s, Gibbs theorized a limit to the smallest sized liquid cluster which could nucleate solid particles.[2, 11] This led to what is now known as the Gibbs-Thomson effect, which is a thermodynamic phenomenon that correlates the curvature and surface tension with the chemical potential and vapor pressure of fine particles. It is an especially important topic for surface deposited objects such as clusters, water, and quantum dots. This effect is traditionally illustrated with a liquid cluster of radius r and surface tension γ. Thermodynamic arguments reveal that the cluster's curved surface exerts a pressure of $2\gamma/r$ on atoms inside the cluster. It is worth noting, in fact, that the pressure induced by this surface tension in very small clusters can also have an effect on the position of the phase boundaries of an alloy phase diagram of alloys.[3] A gas which is in equilibrium with the cluster will have a vapor pressure given by[11]

$$P(r) = P_{bulk} \exp\left(\frac{2\gamma v_m}{r k_B T}\right) \qquad (1.3)$$

where P_{Bulk} is the vapor pressure above a flat liquid surface. The cluster's chemical potential is then given by[4, 7, 11]

$$\mu_r = k_B T \ln\left(\frac{P(r)}{P_{bulk}}\right) = \frac{2\gamma v_m}{r}, \qquad (1.4)$$

where v_m is atomic volume. Hence, smaller clusters have greater chemical potentials and higher vapor pressures than larger clusters. This gives rise to ripening or coarsening phenomena in which larger clusters grow at the expense of smaller ones due to the greater thermodynamic stability of atoms in larger clusters.[2, 4, 7, 11]

Upon heating, a deposited cluster will form a liquid on a surface in the shape of a spherical dome with a contact angle θ that depends on the surface tensions of the various interfaces: vapor-liquid (VL), liquid-substrate (LS), and substrate-vapor (SV), as illustrated in Figure 1.7. The contact angle θ is given by Young's equation: $\gamma_{SV} = \gamma_{LS} + \gamma_{LV} \cos \theta$. When $\theta = 0$, the liquid completely wets the surface forming a continuous film, and there are no distinctive droplets. For $0 < \theta < \pi$, the liquid partially wets the surface. The contact angle θ for the cluster can also be a function temperature and composition of the cluster. Such variations in contact angle lead to variations in nanowire growth, as will be described in subsequent sections.[2, 4, 11]

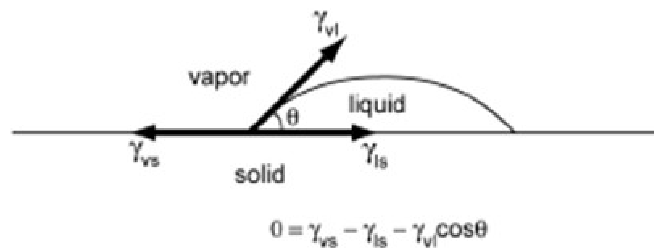


FIGURE 1.7 Schematic of a three-phase equilibrium for wetting of a surface by the liquid seed droplet. γ_{VL} represents the liquid-vapor surface tension and γ_{LS} and γ_{VS} represent the liquid-solid and vapor-solid interfacial energies, respectively.[4, 7]

The application of this theory to nanowire axial growth rate, as originally explained by Givargizov, proposes that nanowires of larger diameter grow faster in length than small wires. The reduction in growth rate for smaller diameter nanowires is the result of the increased free energy of the liquid seeds at very small diameters, which requires a higher partial pressure for supersaturation of the growth species, such as silicon. However, Givargizov's theory dealt with Group IV semiconductor whiskers of diameters of up to three orders of magnitude larger than contemporary nanowires.[4, 7]

Today's experiments with smaller diameters tend to show different behavior, whereby growth rates have been observed to be slower, faster or constant regardless of their diameters. In fact, the growth rate appeared to depend on kinetic parameters, rather than strictly thermodynamic driving forces, such as specific rate limiting steps at the vapor-liquid or liquid-solid interfaces. Beyond this, one major influence of the Gibbs-Thomson effect is that it suppresses the melting point and eutectic temperatures for very fine particles. The thermodynamic equilibrium vapor pressure of small particles as a function of their size, the melting point of nanoparticles decreases with nanocluster radius, and thereby extends the utility of liquid alloy catalysts to lower temperatures.[2, 11]

1.3.5 Ostwald Ripening

The continuous attachment and release of Au atom from clusters at elevated temperatures and the net diffusion of adatoms from smaller Au clusters

across atomically clean surfaces to larger Au droplets follows a process known as Ostwald ripening. It is driven largely by the Gibbs-Thompson effect described above. The process leads to a distinct size-distribution of nanoclusters for given deposition parameters, i.e., substrate temperature, impinging atom flux during deposition, surface cleanliness, etc. Ripening can also occur subsequent to deposition during high temperature annealing. Essentially, Ostwald ripening is the coarsening of the cluster size distribution with the associated increase in mean cluster diameter.[4, 11, 12]

Recently, it has even been shown that for excessively clean surfaces, Au atoms from the liquid beads atop nanowires can diffuse down the nanowire sidewalls during the growth process, migrate across the substrate surface to neighboring larger-diameter nanowires, diffuse up the sidewall of said nanowire, and reabsorb into the larger metal-eutectic seeds atop the larger nanowires. This can effectively eliminate small-diameter nanowire growth due to the loss of catalytic eutectic seed, at the benefit of the larger nanowires. However, it is worth noting that the reported experiments, where this coarsening of the Au seeds during nanowire growth was demonstrated were carried out at extreme growth conditions: high temperatures and extremely low disilane partial pressures, and thus at very slow nanowire growth rates within the highly clean surfaces of an ultra-high vacuum. For our growth temperatures and pressures as well as those typically used by others, this previously observed coarsening during the total nanowire growth time would be negligible. Thus, while Au migration certainly plays a vital role during the deposition and coalescence of seeds prior to nanowire

growth, such migration is not expected to impact the nanowire growth in our investigations, appropriately high growth rates and median temperatures were used in all our studies to ensure this is the case.[12]

1.3.6 Growth and Orientation of Silicon Nanowires

Now the Si crystal structure and the possible growth orientations for a nanowire will be reviewed.[2] Si crystallizes in the face-centered cubic (FCC) diamond lattice structure. A unit cell of Si is actually two interpenetrating FCC lattices. The lattice constant, 'a' for Si is 0.543 nm. Figure 1.8 shows a Si unit cell, the diamond structure and the lattice constant. The notation {hkl} represents the set of all planes that are equivalent to the plane (hkl). Similarly, <hkl> denotes the set of all directions that are equivalent [hkl]. While the angular relations of a set of {hkl} planes or <hkl> directions are different relative to each other, they are energetically the same. The top and bottom plane of the unit cell define the {001} family of planes. The {111} and {110} set of planes run diagonally across the unit cell. The set of {100}, {111}, and {110} represent the primary planes.[2, 13, 14]

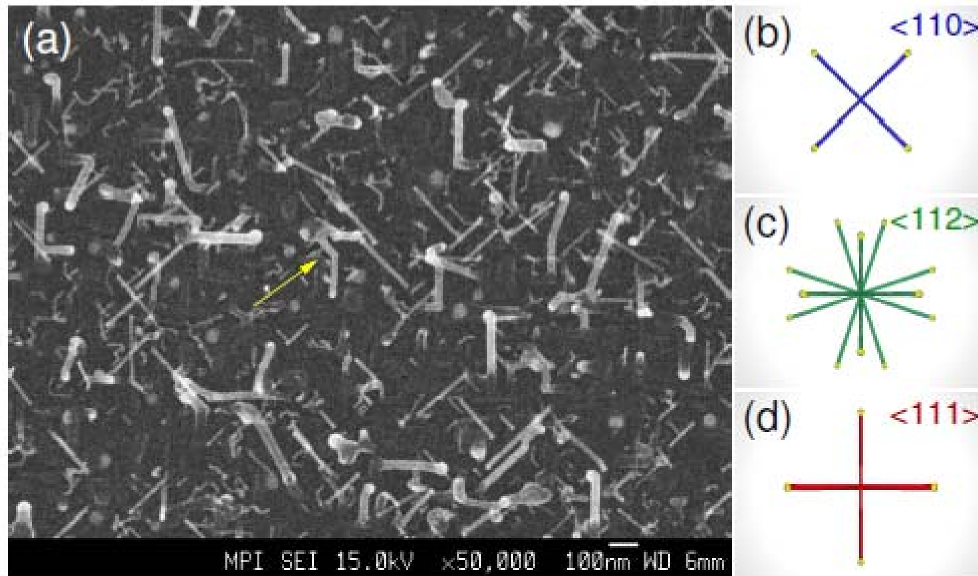


Figure 1.8: (a) Top view scanning electron micrograph of nanowires grown on a silicon (100) substrate. (b) Schematic top view image of <110> oriented nanowires on a (100) substrate of the same azimuthal orientation as in (a). (c) Schematic top view image of <112> oriented nanowires on a (100) substrate of the same azimuthal orientation as in (a). (d) Schematic top view image of <111> oriented nanowires on a (100) substrate of the same orientation as in (a).[2]

Silicon nanowires can adopt several growth directions, all at different angles relative to the growth substrate. It should however be noted that epitaxial, as well as, non epitaxial growth has been observed for Si nanowires. For instance, nanowires grow epitaxially on Si substrates when the native oxide layer was removed. On the other hand, non-epitaxial growth was observed when an amorphous silicon oxide was present on the substrate. Early research by Wagner and Ellis[14] showed that nanowires with diameters greater than l00 nm and were

grown via a gold-mediated VLS, tended to grow in the <111> orientation. More recently, nanowire growth along the <112>, <110> and, in some rare cases, the <100> directions has been reported. Since we grow nanowires epitaxially on Si (111) substrates, it is relevant to examine and visualize the possible growth orientations relative to the substrate crystallographic orientation[Figure 1.8]. Looking perpendicularly at the substrate surface and parallel to the [111] direction, there are a total 4 equivalent <111> directions, 15 possible <112> directions and 9 possible <110> directions. Although 16 the directions are different relative to each other geometrically, families of <hkl> directions are indistinguishable in reality, and are physically and chemically equivalent.[2, 14]

So, Si nanowires can grow along any of the possible <110>, <111> or <112> directions as shown in Figure 1.8. This leads to the question of what factors govern the choice of growth direction and what distinguishes the nanowires that are grown in different directions. According to other researchers,[13, 14] the nanowire diameter is growth direction dependent. Large nanowires ($d > 40$ nm) prefer to grow along the <111> orientation, and small nanowires ($d < 15$ nm) choose to grow along the <110> orientation. For intermediate diameter ranges, <112> is the preferred growth orientation. Arguments were made based on free energies of the bounding facets and that of the growth interface. Consequently, certain growth directions minimize the energy of the system and hence are the preferred growth orientations.[14]

Another related phenomenon is that of kinking. In kinking, a nanowire growing in a well defined crystallographic direction abruptly changes its axial

growth direction. Earlier research attributed kinking to possible kinetic growth instability. More recently, Lugstein[12] et al, reported that higher gas pressures force the nanowires to kink towards the <112> growth orientation.[2, 14]

1.4 Plasma-Assisted Approaches in Nanostructure

1.4.1 Introduction into Plasmas

The concept ‘‘plasma’’ was first proposed by Irving Langmuir who described it as either a partially or fully ionized gas. Macroscopically, plasmas are electrically neutral, while on the molecular level they contain charged particles like electrons, cations, and in some cases anions.[15] Excited neutral species in the form of molecules, atoms, and radicals are also present. Compared to the ordinary solid, liquid, and gas phases, the species in plasma (at least part of) are in electronically excited states, resulting in a highly reactive environment for chemical reactions. Laboratory-scale plasmas for materials processing are usually generated by means of electromagnetic fields, most commonly by direct-current (DC), radio-frequency or microwave radiation, or electron cyclone resonance (ECR). [11, 15]

The electron density n_e and electron temperature T_e are important parameters to characterize plasmas. Both of these parameters can vary significantly, resulting in the broad spectrum of plasmas from neon tubes to plasma in fusion reactors. n_e describes the density of charged particles in the plasma, often referred to as the plasma density. Typical values of n_e are in the range of 109–1013 cm^{-3} in low-pressure plasmas and 1016 cm^{-3} in atmospheric

plasmas. The electron density in the positive column of DC glow discharge is typically 1011 cm^{-3}. Low-pressure (10^{-3}–1 Torr) capacitively coupled discharge typically gives n_e value in the range of 109 cm^{-3}. Inductively coupled plasma (ICP) sources enable a higher electron density of 1012 cm^{-3}. In high-density ICP and ECR plasma sources, an electron density of 1013 cm^{-3} is reached. The electron temperature, T_e, is a quantitative reflection of the degree of thermal motion of the electrons. For materials-processing plasmas in laboratory scale equipment, the electron temperature is typically on the order of 1–10 eV.[17] The heavy particle-like ions and neutrals have their own effective temperatures, which can be very different from T_e due to the different mobility. In the cases of much-lower ion temperatures, T_i, the electron temperatures are generally much greater and correspondingly indicate more energetically excitation. The heavy particles remain near room temperature. Such plasmas are known as cold plasmas or low-temperature plasmas. There is no significant heating effect of cold plasmas, while the energetically excited species still impart high chemical reactivity. [15, 16]

Thus, a unique property of cold plasmas is their high chemical reactivity under what would otherwise be mild conditions. This is very desirable for materials processing, especially for those sensitive to heat, such as organic materials, polymers, and biomaterials.[5, 11, 12] Low-temperature plasmas have broad applications in film deposition, etching, and surface modifications. Plasmas with comparable temperature of heavy particles to that of electrons, i.e., Te, Ti, are known as thermal plasmas. Except the high chemical reactivity, thermal plasmas exhibit very intense heat that is sufficient to melt and even vaporize most

materials. They are often used in high-temperature materials-processing applications such as melting of metals, ceramics sintering and evaporation, and as an ionization sources in chemical analysis such as atomic emission spectroscopy and mass spectrometry (MS).[17]

1.4.2 A Schematic of the Low-Pressure Cold-Plasma State

The most commonly encountered plasma in CVD applications is the capacitive or “RF diode” plasma. A simplified view of such a reactor might look like Figure 1.9. In this figure, $n_e = z_i \cdot n_i$ is the plasma density; typical values are around 10^8 to $10^{10}/cm^3$, compared to a neutral density of $3x10^{15}/cm^3$ at 100 mTorr. (The ion and electron densities are equal to maintain charge neutrality in the bulk plasma.)[17]

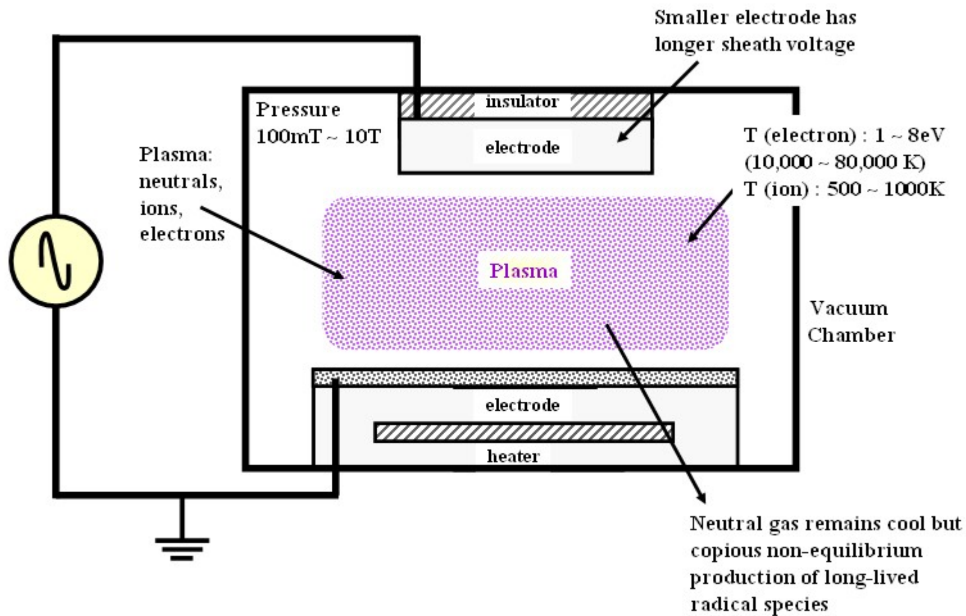


Figure 1.9 Simplified view of a generic catacitively-excited plasma.

The plasma is excited and sustained by applying a voltage typically AC or RF, 60 Hz to many MHz – between the two electrodes. The "capacitive" moniker arises from the nature of the coupling to the plasma. The plasma forms "sheaths", or regions of very low electron density, next to solid surfaces. The RF voltage appears mostly across these sheaths as if they were the dielectric region of a capacitor, with the electrode and the plasma forming the two plates. [16]

The system pressure for CVD applications is usually between about 100 mTorr and 10 Torr. The electrodes are typically cylindrical, with the separation between the two electrodes kept small compared to the electrode diameter. The electrode "gap" is an important parameter; it varies from about 0.5 cm to 10 cm, generally getting smaller for higher pressure operation. Typical gaps are a few hundred times the mean free path, so electrons undergo many collisions but do not have time to transfer their energy to the neutral gas. However, practical limitations on chamber size generally lead to increasing ratios, and "hotter" plasma, at higher pressure. Thus, a gap of 5 cm, which is very easy to build, corresponds to about 100 times the mean free path at 100 mTorr. On the other hand, to achieve the same relative separation at 10 Torr one would need to separate the electrodes by only 0.5 mm or 500 microns, which is a very challenging mechanical task if the diameter is comparable to the size of a wafer. Typical electron temperatures are around 5 eV. Electron temperature varies weakly with other parameters: it is dominated by the requirement that the electrons provide enough ions to sustain the plasma.[16, 18]

1.4.3 Classification of Plasma-Stimulated Nano-Fabrication

According to the processing method, plasma-assisted nanostructure fabrication approaches reported so far can be classified into the following four categories [Figure 1.10].[18]

i) PECVD (Figure 1a): Like in CVD processes, the reaction precursors are fed into the reactor in the form of gases. Plasma is introduced into the reaction zone to activate the precursors. The substrate can be deposited either in the plasma zone or outside the plasma region, to enhance or avoid some plasma effects such as ion bombardment. PECVD can operate in a broad range of temperature and pressure conditions, allowing for large freedom in preparation and property control. The precursors for PECVD have to be volatile, which put some limitations to the approach for some material systems.

ii) Thermal Plasma Processing with Liquid and Solid Precursors (Figure 1b): In this setup, the precursors can be liquids, solids, or solutions, which are injected directly into the high temperature plasma zone. Products are obtained after the transformation in the high-temperature plasma zone. This method provides large freedom of choice in starting materials. Nanostructures with a high degree of crystallinity are often obtained due to the strong heat effect.

iii) Thermal Plasma Evaporation and Condensation (Figure 1c): In this case, the starting materials are evaporated by the intense heating of

thermal plasma. After leaving the high temperature plasma zone, the vapors condense into nanostructures. Reactive gases can also be introduced into the plasma for chemical composition tuning.

iv) Plasma Treatment of Solid Phases (Fig. 1d): Here, the target material is prepared by simply exposing the solid precursor to plasmas through plasma–solid interaction. This configuration is simple and not complicated by the complexity of precursor introduction. In addition, the solid-phase conditions such as temperature and external bias can be well controlled in this configuration, which is suitable for plasma–solid interactions.

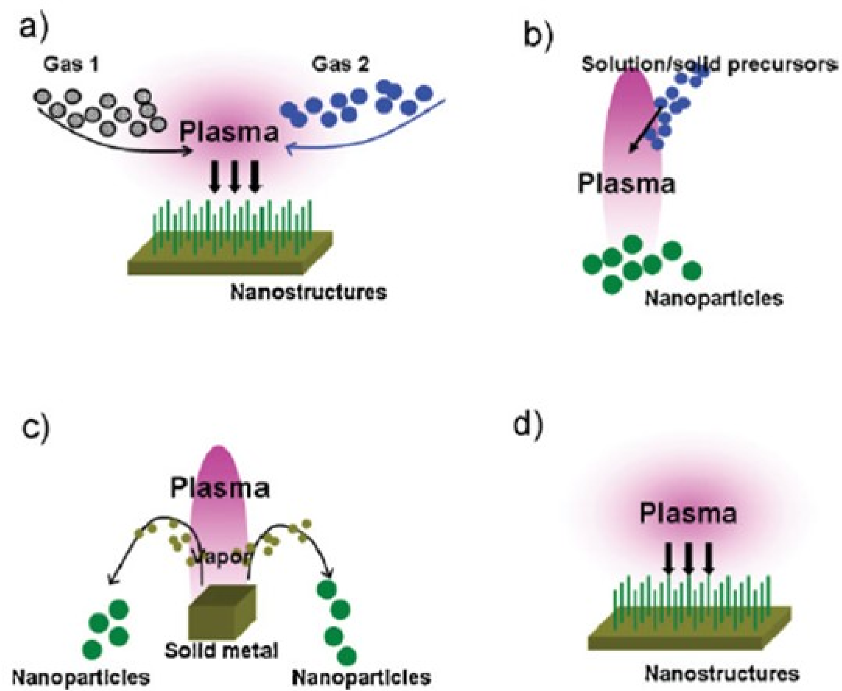


Figure 1.10 Schematic illustration of four plasma-assisted material preparation process; a) PECVD b) thermal plasma sintering c) thermal plasma evaporation and condensation, and d) plasma treatment of solid phases.[18]

1.5 Statement of Problem

A clear understanding of the silicon nanowire growth at low temperature is a key factor in providing insight into the kinetic processes involved. By using rf plasma excitation during thermal growth a new control parameter is introduced during nanowire growth to enhance the nanostructure grown at low temperature. Low temperature disilane plasma is expected to possibly develop various silicon nanostructures compared to thermal growth condition. Also, a comparison of the influence of different disilane pressures and plasma powers on the nanowire growth kinetic can provide the kinetics of VLS silicon nanowire growth at low temperature. Another potential advantage of rf plasma excitation is that it activates the mobility and diffusivity of Au catalysts in order to promote the nanowire growth.

In the present research work, a low power rf plasma (operating at 13.56 MHz) is utilized for low temperature growth of silicon nanowires. A qualitative and comprehensive comparison of the growth characteristics including nucleation, growth rates, orientations, morphologies between conventional thermal and plasma stimulated growth is carried out for better fundamental understanding of the structure and growth of nanowire. In addition, various nanostructures are studied based on their growth mechanism.

Chapter 2

Experimental Techniques

This chapter describes the deposition reactors and experimental procedures involved in the growth of Si nanowires. An ultra-high vacuum thermal evaporation system was used for depositing Au films onto clean Si substrates. The gold was transformed to nanodots via thermal annealing, which caused the film to morphologically destabilize due to reasons of surface thermodynamics. Subsequent nanowire growth was done in a quartz-lamp heated, low pressure chemical vapor deposition system to which an rf plasma generator was connected. *Ex-situ* characterization of the samples included scanning electron microscopy (SEM) for imaging the nanowires, transmission electron microscopy (TEM) for investigating the crystallinity and directionality of the grown nanowires, and Raman spectroscopy for analyzing the intrinsic strain of the curved silicon nanowires.

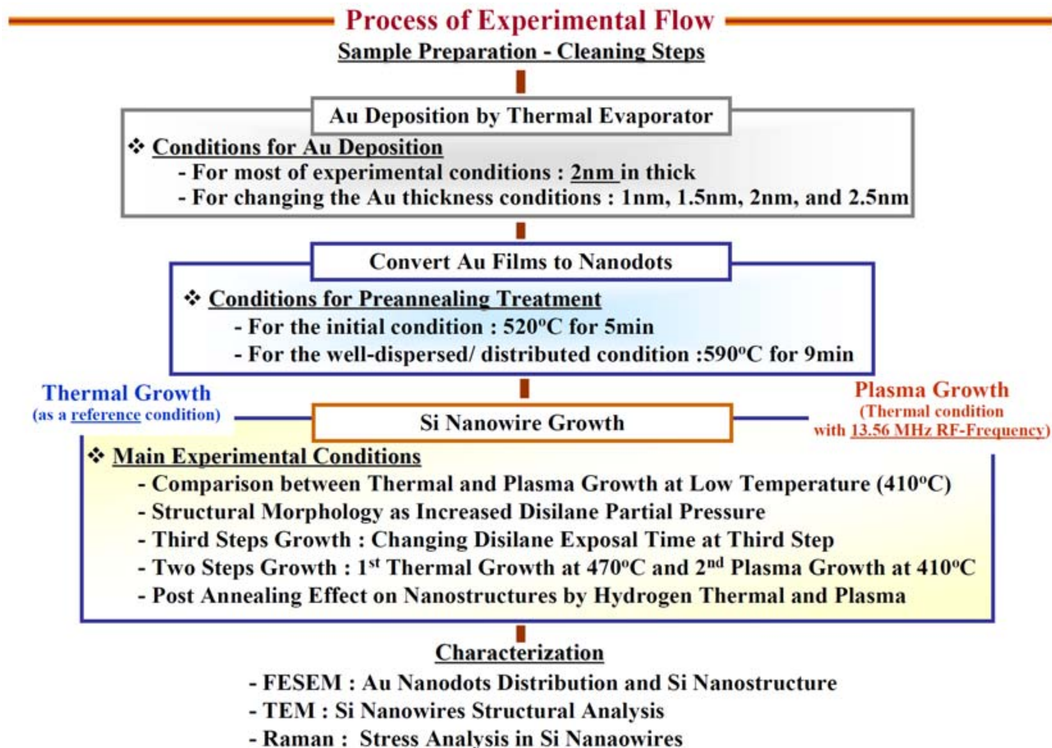


Table 2.1 Procedure of Thermally Grown and Plasma-enhanced Si Nanowires.

2.1 Wafer Preparation

Before describing the procedures for silicon nanowire growth, wafer preparation is described first. In most cases, low doped, <111> oriented substrates (about 1 cm on an edge) were cut from a 100 mm diameter silicon wafers. Prior to growth, the residual contamination of these wafers was reduced by a two-step wet chemical cleaning process. First, the necessary equipment was cleaned. For this purpose, a Teflon basket for the sample holder was placed inside a quartz bowl and carefully rinsed with deionized water. The quality of the epitaxial structure grown depended critically on the quality and cleanliness of the substrate. Silicon

(100) (or (111)) arsenide-doped n-type wafers (resistivity ~ 10^{-2} ohm-cm) were degreased by rinsing in acetone for 10 min followed by a methanol rinse for 10 min. The wafers were then etched in a piranha solution (H_2SO_4 : H_2O_2 = 3:1) to remove organic matter from the surface and rendering a super hydrophilic native oxide surface. The final cleaning step involved removing the native oxide surface by etching the wafers in 10:1 buffered 48% HF solution for 10 min. followed by drying under flowing nitrogen gas. This left a clean super-hydrophobic hydrogen-terminated surface. The substrates were immediately loaded into a high vacuum thermal evaporation chamber for Au film deposition.

2.2 High Vacuum Thermal Evaporation System

The vacuum thermal evaporation deposition technique consists of heating a source material to evaporate it into the gas phase. The vapor condenses to form a thin film on the cold substrate surface, as well as, on the vacuum chamber walls. Usually low pressures are used, about 10^{-6} or 10^{-5} Torr, to avoid vapor borne contamination. At these low pressures, the mean free path of vapor atoms is on the same order as the dimensions of the vacuum chamber (5×10^2 ~ 10^5 cm). Effectively, these particles travel in straight lines from the evaporation source towards the substrate. This resulted in a 'shadowing' phenomenon with 3D objects, especially in those regions not directly in line of sight of the evaporation source. With most thermal evaporation techniques, the average energy of vapor atoms reaching a substrate surface is generally quite low (on the order of a kT, i.e.,

tenths of an eV). The effect on the surface morphology of the films is often a porous and poorly adherent material.[19]

Substrate heating ameliorates the adhesion problem and produces gold surface structure appropriate for nanowire growth. The equipment available in the laboratory uses either resistance heating (Joule effect) or bombardment with a high energy electron beam, usually several keV, generated by an electron beam gun (electron beam heating). A schematic of the evaporator used is shown in Figure 2.1. Typically it consists of an evaporation source of the desired material. Substrates are located away at an appropriate distance facing the evaporation source. The substrate holder can be heated and/or electrically biased to a desired potential using a dc/rf power supply. The evaporated atoms undergo essentially collisionless line-of-sight transport to the substrate surface.[19]

A quartz crystal monitor located in the molecular beam path is used to precisely measure the thickness of the evaporated gold films.

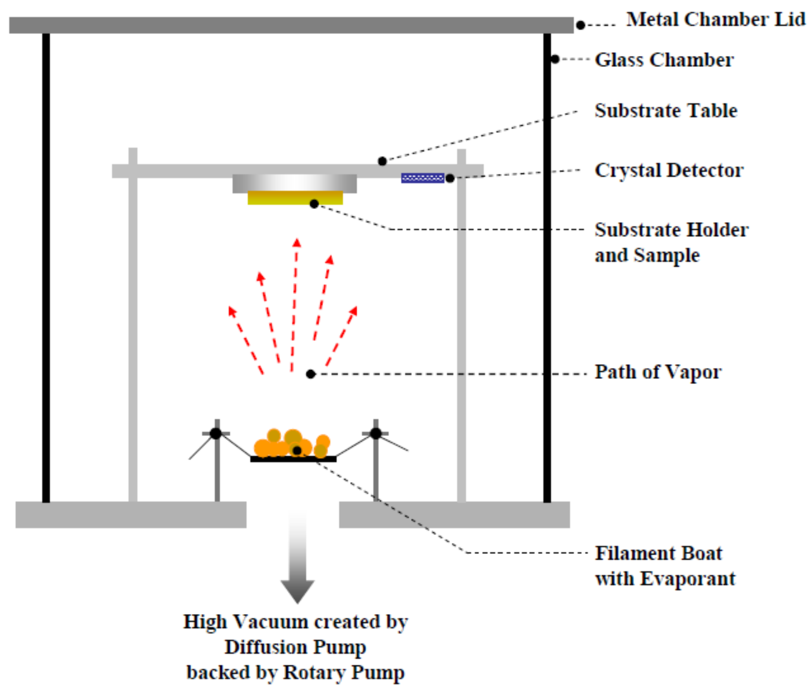


Figure 2.1 Schematic Diagram of High Vacuum Thermal Evaporator System[19]

2.3 Chemical Vapor Deposition of Nanowires

Silicon nanowires were grown by the VLS, gold actuated process using a quartz lamp heated, low pressure chemical vapor deposition (LPCVD) reactor as illustrated in Figure 2.5. A base pressure of 5 mTorr was used. The entire chamber was enclosed in a stainless steel cabinet and that was divided into three parts, namely, the pumping system, the gas cabinet and a quart tube reaction chamber.

The system was vacuum pumped by a roots blower backed by a mechanical pump as shown in Figure 2.2. This combination provided high capacity and low cost pumping. Roots pumps are single stage mechanical pumps

and capable of high gas throughputs. They contain two counter-rotating blades mounted on parallel shafts which rotate synchronously in opposite directions at speeds of 3000-3500 rpm. No oil is used to seal the gaps and they are thus referred as dry pumps. They substantially reduce oil contamination normally associated with rotatory pumps. The exhaust gas then passes through a water scrubber to remove gas borne particles and water soluble/reactive molecules.

The gas reactant delivery system consisted of gas cylinders and mass flow controllers (MFCs) [Figure 2.3 and Figure 2.4]. The operational principle of MFCs relies on the ability of a flowing gas to transfer heat. The mass flow meter consists of a large main gas flow tube in parallel with a small sensor.

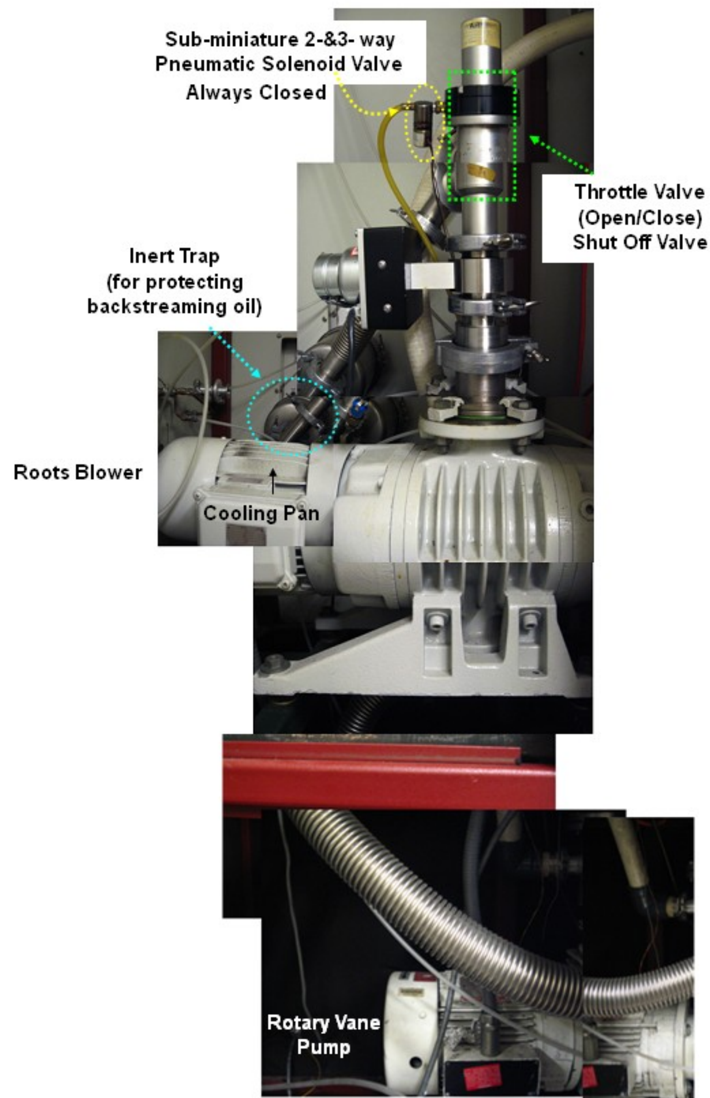


Figure 2.2 Vacuum Pumping System

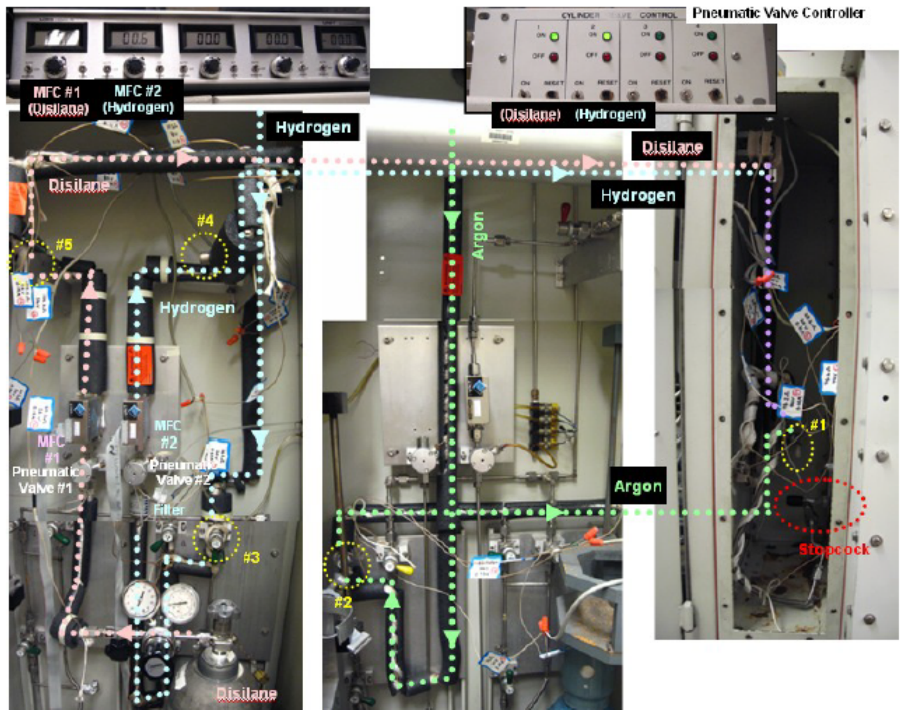


Figure 2.3 Gas Flow Control and Delivery System

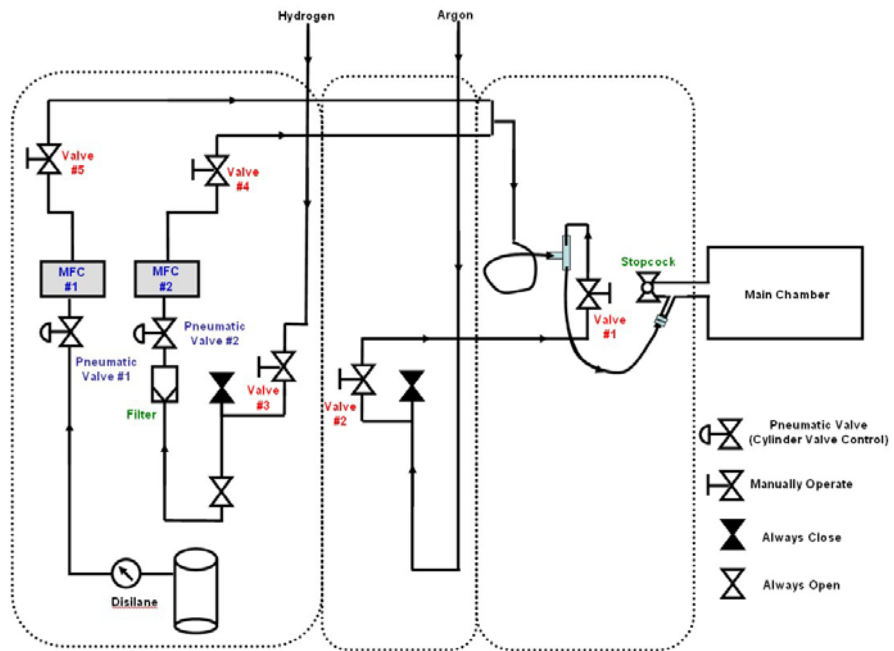


Figure 2.4 Schematic of Gas Flow System

A heating coil is wrapped around the sensor tube midway along its length, and temperature sensors (resistance thermometers) are located both upstream and downstream of the heated segment. When gas is not flowing, the temperatures at both sensors are equal. Flowing gas causes the temperature distribution in the sensor tube to change, as a result of the thermal transfer between a heated wall and the gas stream. The downstream temperature becomes greater than the upstream temperature since the flowing gas conducts heat away from the heated point. Each of the two resistance thermometers is connected to one arm of an unbalanced Wheatstone bridge, and the temperature differential is converted into a voltage signal. Calibration factors are used so that the voltage output derived from the sensor tube can express the gas flow in units of standard cubic centimeter per minute (sccm).

The CVD system has four thermal mass flow controllers (Unit 1660) calibrated to nitrogen with flow capacities of 200, 500 or 5000 sccm. Hydrogen gas was typically flowed in the range of 250 to 3000 sccm. Silane (diluted in hydrogen gas) was flowed in the range of 20 to 40 sccm.

All the gas lines were isolated to prevent premature mixing of reactants until they reached the reaction chamber. The pressure inside the reactor is measured using two Baratron capacitance manometers with ranges of 0-10 and 0-1000 Torr. They detect gas pressures independent of the gas species and provide absolute pressure measurement. They work by measuring changes in pressure that produce a displacement of a flexible diaphragm relative to that of a fixed plate.

The capacitance between the diaphragm and the fixed plate is measured and correlated with the diaphragm displacement and, thus, converted to pressure.

Sample heating was provided by 12 quartz lamps concentrically placed around the quartz reaction tube. The lamps were encompassed in a water-cooled gold-coated stainless steel shield to transmit the heat radially towards the reaction tube. Figure 2.5 is a schematic of the sample holder system, illustrating the location of the plasma glow. The Si substrates were supported by a SiC-coated graphite susceptor during growth. The maximum allowed sample size was $3.5 \times 3.5\ cm^2$. The sample temperature was measured by a pre-calibrated alumel-chromel (type K) thermocouple located on the back of the susceptor. For Si nanowire growth under plasma conditions, a 13.56 MHz RF power supply was employed, where the reaction chamber was one component of a tunable matching network. A stainless steel tube, attached to the backside of the sample holder, acted as an antenna for delivering the RF power.

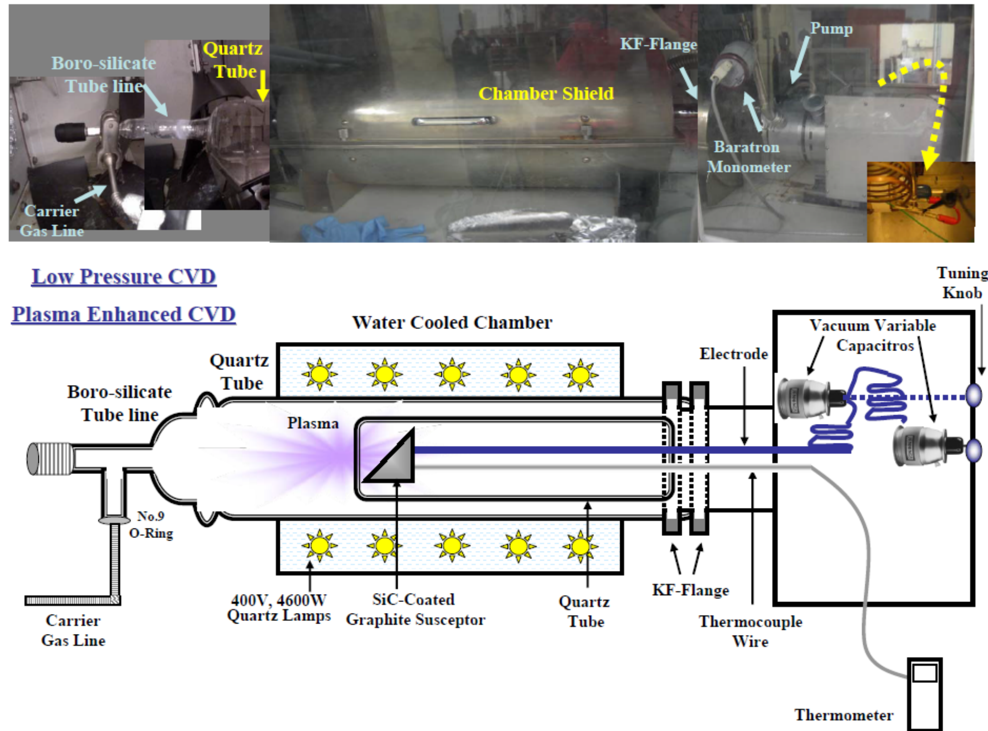


Figure 2.5 Schematic Diagram of Plasma-Enhanced Low-Pressure CVD

2.4 Silicon Nanowire Synthesis Procedures

As we discussed in previous sections, Si nanowire synthesis is done sequentially in the following steps:

1. Substrate cleaning to provide a clean oxide free surface;
2. Gold catalyst is applied by evaporation and annealed to form nanodot seeds; and
3. Growth of Si nanowires in LPCVD reactor.

The following steps are performed for growing Si nanowires on Au deposited Si (100) or (111) substrates:

1. The substrate is first dipped in 2 % HF diluted in de-ionized (DI) water for

10 sec to remove any surface oxides followed by 2 sec in DI water and blow dried with nitrogen;

2. The substrate is then immediately loaded into the CVD chamber which is under positive argon flow and then evacuated to base pressure of 5 mTorr;
3. Semiconductor research grade hydrogen is flowed at a flow rate of 3000 sccm for outgassing and substrate temperature is increased in steps of 100ºC per 10 minutes to 300ºC;
4. The substrate is then annealed at 520ºC for 5 minutes to promote the formation of a AuSi eutectic prior to the start of nanowire growth.
5. For growth using disilane as a source gas, a gas atmosphere of 10% Si_2H_6 diluted in H_2 gas was admitted at a flow rate of 200 sccm with the total pressure held at 0.154 Torr (or 0.256 Torr). Nanowires were grown at temperatures between 410 to 470ºC and in some cases the partial pressure of Si_2H_6 was adjusted to within the range of 6×10^{-3} mTorr to 25×10^{-3} mTorr.
6. For Si nanowire growth under plasma conditions an rf plasma (13.56 MHz) was used. The plasma power was varied from 1.5 to 3.5 W and the growth times were varied between 10 seconds to 5.5 minutes. Figure 2.6 shows the plasma glow when the disilane plasma was injected into the reactor.
7. For hydrogen post-annealing under plasma conditions, a plasma power of 2.3 W was typically used. The hydrogen total pressure was 0.154 mTorr.

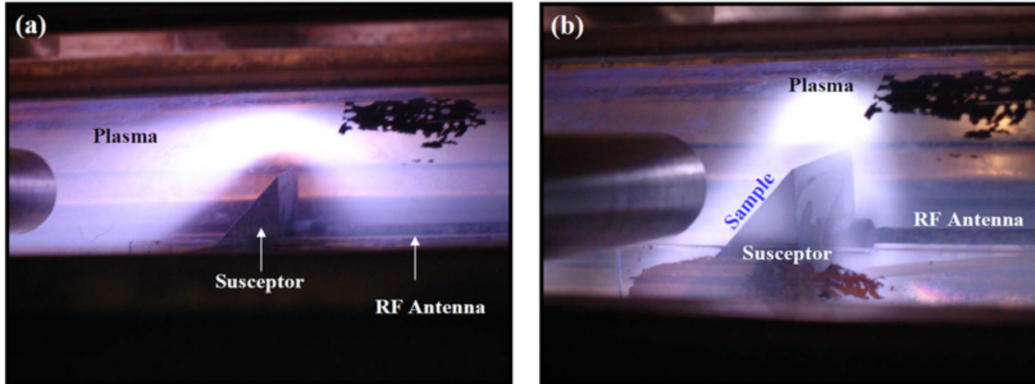


Figure 2.6 Plasma Glow near the Susceptor and RF Antenna in LP-CVD

The range of working parameters for nanowire growth used in this study is given in Table 2.2.

	Growth Step	Variations of Working Growth Parameters
Pre-annealing Condition	Single Step	• Pre-annealing at **520°C for 5mins and 590°C for 9mins** • Si nanowires growth at 410°C for 5'30" (P_{total}=0.154 Torr)
Thermal & Plasma Growth	Single Step	•**Thermal & Plasma Growth** (with 2.3 W) at 410°C for 5'30" • Disilane Partial Pressure Changes : **6x10^{-3} to 25x10^{-3} mTorr** :
Bending Nanowires	Three Steps	• First Step : Thermal Growth at 470°C for 5 mins • Second Step : Hydrogen Plasma (2.3 W) at 410°C for 5 mins • Third Step : Disilane Plasma at 410°C (with 2.3 W) for **10, 40, & 150 sec**
Branching Nanowire	Two Steps	• First Step : Thermal Growth at 470°C for 5 mins • Second Step : Disilane Plasma at 410°C for 2'30" mins with Plasma Powers **1.5 W, 2.6 W, & 3.5 W**
Post-annealing Treatment	Three Steps	• First Step : Thermal Growth at 470°C for 5 mins • Second Step : Hydrogen Thermal & Plasma (2.3 W) at 410°C for **5 and 15 mins**

Table 2.2 Range of Working Growth Parameters for Si Nanowire Growth in Low Temperature CVD System

2.5 Characterization Techniques

2.5.1 Electron Microscopy

Electron microscopy was routinely used to analyze the morphologies of the nanowires grown. The technique uses electrons to illuminate and image a specimen at great magnifications. Electron microscopes have much greater resolving power and greater magnifications than light microscopes, which is due to the small wavelength of the high energy electrons, its de Broglie wavelength, being much smaller than the visible spectrum. Two types of electron microscopes were routinely used in this work, namely, a Scanning Electron Microscope (SEM) and a Transmission Electron Microscope (TEM).[17]

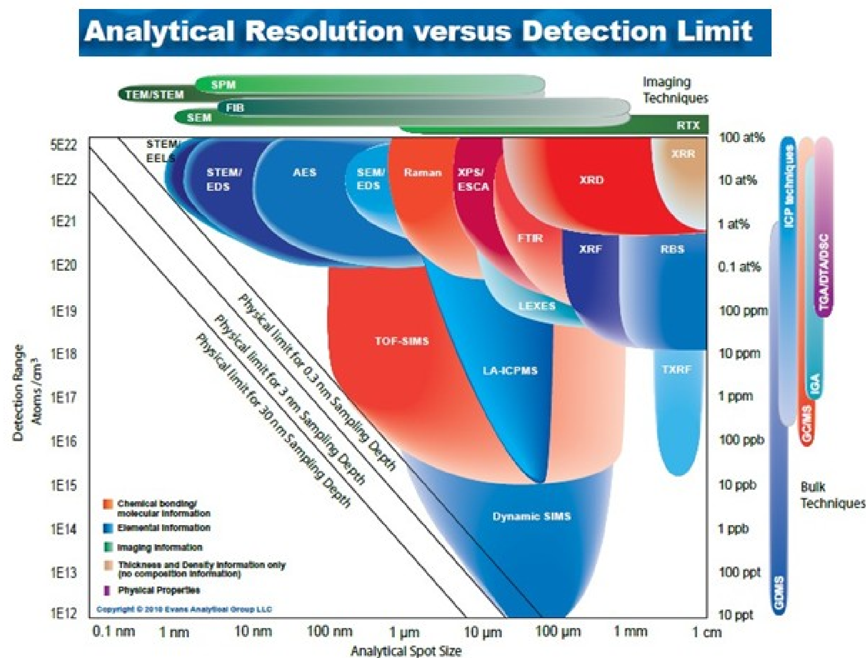


Figure 2.7 Analytical Resolutions versus Detection Limit[20]

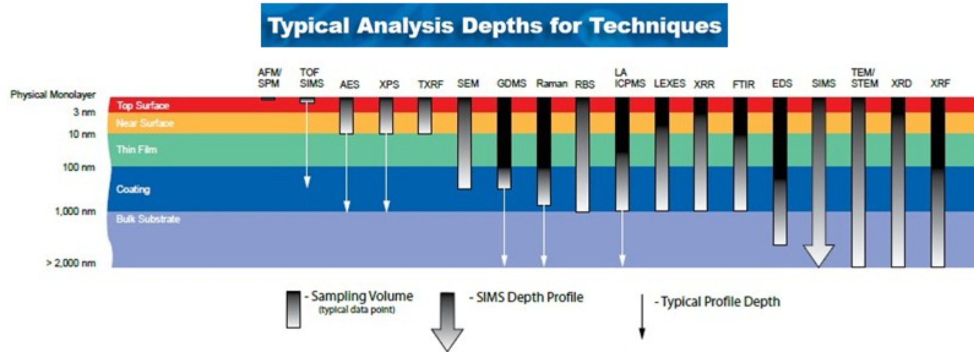


Figure 2.8 Typical Analysis Depths for Techniques[20]

2.5.1.1 Electron-Atom Interaction

Electron-atom interaction is what makes electron microscopy possible. Energetic electrons strike the sample and cause various collision reactions to take place as shown in Figure 2.9. At the top the diagram, various collision processes are shown corresponding to backscattered processes such as secondary electrons. Through the bottom various emissions are shown corresponding to transmitted processes. The sampling volumes for the different electron-atom interactions are illustrated in Figure 2.9b.[21]

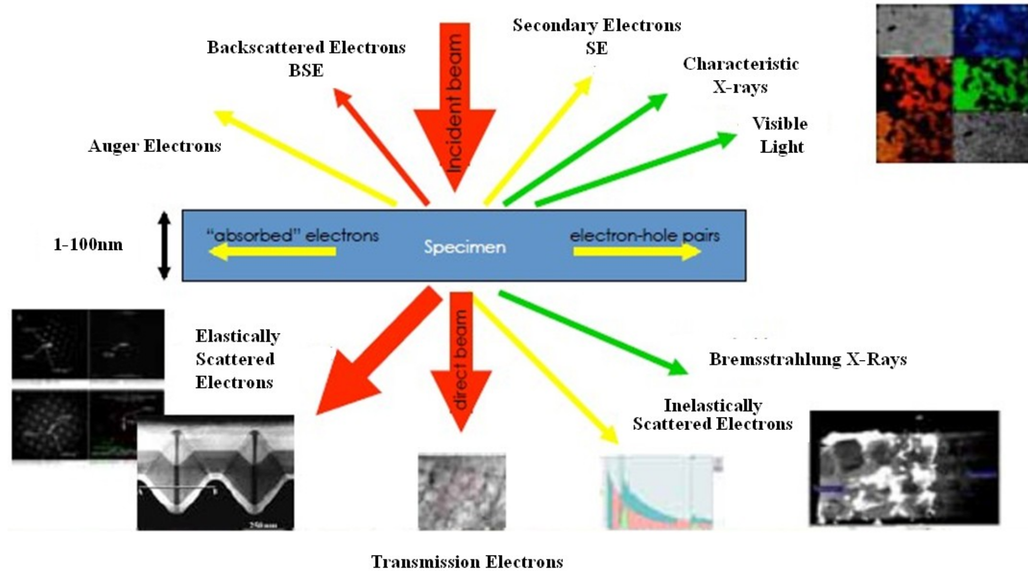


Figure 2.9 (a) Effects produced by electron bombardment of a material and their use in imaging; (b) Interaction volumes for various electron-atom interactions[21]

There are several specimen interactions pertinent to the sample characterization used in this study.[17, 21]

- Secondary electrons: When an incident electron passes near an atom in the specimen, it will impart some of its energy to a lower energy electron of the specimen, causing its ejection with a very small kinetic energy (5 eV). Production of secondary electrons is very topographically sensitive in nature. Due to their low energy, only secondary electrons very near the surface (<50 nm) can escape the sample and be collected for imaging.
- Backscattered electrons: When an incident electron collides with an atom in the specimen, and then is backscattered with efficiencies dependent on the atomic number of the scattering atoms. The production of these electrons varies directly with the specimen's average atomic number and

appears brighter for heavier atoms.

- X-rays: Caused by the de-energization of the specimen atom after a secondary electron is produced. X-rays emitted from the atom will have a characteristic energy which is unique to the element from which it originates.

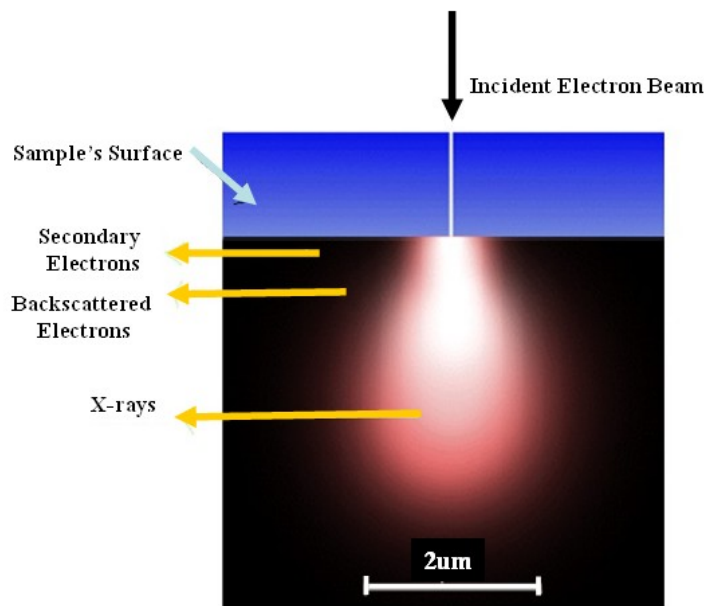


Figure 2.10 Schematic Bulk Specimen Interactions[21]

2.5.2 Scanning Electron Microscopy (SEM)

The scanning electron microscope (SEM) is a type of electron microscope capable of producing high resolution images of a sample surface. Due to the manner in which the image is created, SEM images have a characteristic three-dimensional appearance, because of a large depth of field. They are useful for judging the surface structure of the sample. SEM produces images by probing the

sample with an electron beam with an energy ranging from a few hundred eV to 40 keV. The electron beam is generated by an electron gun of three main types: Tungsten hairpin, LaB_6 and Field Emission Gun (FEG). The latter produces an electron beam with a significant brightness and small beam size. A filament (electron gun) used in scanning electron microscope generates a beam of electrons in a vacuum created inside the chamber where the samples are kept for analysis. That beam is collimated using electromagnetic condenser lenses, focused by an objective lens, and scanned across the surface of the sample by electromagnetic detection coils. The primary imaging method collects the secondary electrons that are released by the sample. The secondary electrons are detected by a scintillation detector that produces flashes of light from the impinging electrons. These light flashes are then amplified by a photomultiplier tube and counted. By correlating the sample scan position with the resultant signal, a black and white image is constructed similar to what would be seen through an optical microscope. The surface topography looks natural due to contrasting illumination and shadowing.

The general SEM instrument itself is very versatile, having many other imaging modes available to it. For instance, specimen current imaging uses the variation in electrical current to produce an image that is induced in the specimen by the illuminating electron beam. It can often be used to show subsurface defects. Another example is backscattered imaging, which uses high-energy electrons that emerge nearly 180 degrees from the incident beam. The backscatter electron yield is a function of the average atomic number of each point on the sample, and thus can give compositional information. Scanning electron microscopes are often

coupled with X-ray analyzers, e.g., energy dispersive X-ray spectrometer (EDS or EDX). When energetic electrons impact a sample, X-rays are generated that are characteristic of the elements present in the sample. These X-rays are collected by a detector, from which an image is constructed. Many other imaging modes are available that provide specialized information. A full detail of the SEM can be found elsewhere[18]. The tool model used is a Hitachi 4340 field emission SEM.

2.5.3 Transmission Electron Microscopy (TEM)

Transmission electron microscopy (TEM) is an imaging technique whereby a beam of electrons is focused onto a specimen causing an enlarged version to appear on a fluorescent screen or layer of photographic film, or to be detected by a CCD camera. The beam has enough energy for the electrons to transmit through the entire sample. This beam is greatly magnified by a series of electromagnetic lenses and observed in two ways. One is by electron diffraction and the other by direct electron imaging. Electron diffraction patterns are used to determine the crystallographic structure of the material. On the other hand, the microstructure, e.g. the grain size, and lattice defects are studied by use of the image mode. With scanning transmission electron microscopy (STEM), the electron beam is raster-scanned across the material.

Two working modes are used, namely, scanning TEM and diffraction modes. In the former, the electron beam is scanned over a defined area of the sample. At each point, the generated signal is simultaneously recorded by selected detectors, and an image is built.

In addition to various imaging modes, electron bombardment also produces a variety of electron and X-ray signals that may be used for compositional analysis. A 200 KeV TEM [JOEL 2010F] instrument was used in our project. A photograph of the facility is given below. A Phillips 2000 High Resolution Transmission Electron Microscope (HRTEM) of 300 KeV is also used for lattice imaging of the Si nanostructures.[17, 20]

2.5.4 Raman Spectroscopy

2.5.4.1 Raman Scattering

The basic features of Raman scattering from vibrational excitations in nano-structures are similar to those of the bulk and independent of the dimensionality of the system. This concerns the experimental techniques, the kind of selection rules, resonance phenomena and other properties. For this reason, discussion will be confined in this section mainly to a short summary of the technique's general properties. More detailed descriptions can be in several reviews dealing with bulk systems.[17, 22] We will point out adaptations applied for analyzing lower dimensional systems.

The main difference between Raman scattering from bulk samples and lower dimensional small-scale systems is that the latter have electronic states and vibration properties different from the bulk. While these differences do not cause any principal limitations, the small numbers of atoms present in the lower dimensional systems turn out to be the main experimental obstacle. As a result, the scattering intensities are low and the experiment needs to be carefully

designed. Besides standard optical measures such as high aperture, optimized collecting optics for the scattered light between the sample preparation chamber and the monochromator, it turns out that the main advantage comes from the exploitation of cross sectional resonance enhancements (Resonance Raman Scattering). For this reason, previous knowledge about the electronic band structure is extremely helpful and quite often the choice of photon energies is the decisive parameter for a successful experiment. *Vice versa*, the experiment, which first of all is supposed to determine vibrational properties, also allows information to be obtained about the electronic states by using different laser lines for excitation.

2.5.4.2 Experimental configurations of Raman Instruments

Different configurations allow for measurements on different spatial resolutions, that is, macro-, micro- and nano-Raman spectroscopy. Common to all resolution scales is the laser illumination and the spectrometer. By directing the laser light into different, parallel existing optical arrangements, the different spatial resolutions can be selected. The illumination source common for all set-ups is a yttrium aluminum garnet (YAG) laser with a very low beam divergence (0.5 mrad) emitting. It is further enhanced by expanding the beam and by applying spatial filtering. [23]

The spectrometer common to all three resolution configurations is a triple monochromator that can be operated in a single line scanning mode (added dispersion) and in a multichannel mode as a spectrograph. The scanning mode

provides higher contrast and resolution. In the multichannel mode, the first two monochromators operate in a subtractive mode, selecting the desired spectral region, which is subsequently analyzed by the spectrograph equipped with low noise, liquid-nitrogen cooled CCD (charge coupled detector).

The macro-Raman configuration is the standard Raman set-up used when experiments need long working distances. It allows only for small numerical apertures (NA = 0.1-0.2) as is often the case with *in-situ* measurements in ultrahigh vacuum chambers, cryostats or gas cells. The resolution is thus low around 10 − 100 μm. A micro-Raman configuration is based on a confocal microscope design that uses an objective lens with a very large numerical aperture (NA = 0.95) and a pinhole in the intermediate focal plane. The spatial resolution of this microscope is below 1 μm. In nano-Raman, where the optical near field is exploited, sampling resolutions below 100 nm are achieved. Independent of the desired resolution, it turns out to be extremely important in all measurements on nanostructures, to have nano-positioning capabilities (nanometric stages) for the sample, in order to be able to increase the optical signal.[17, 23]

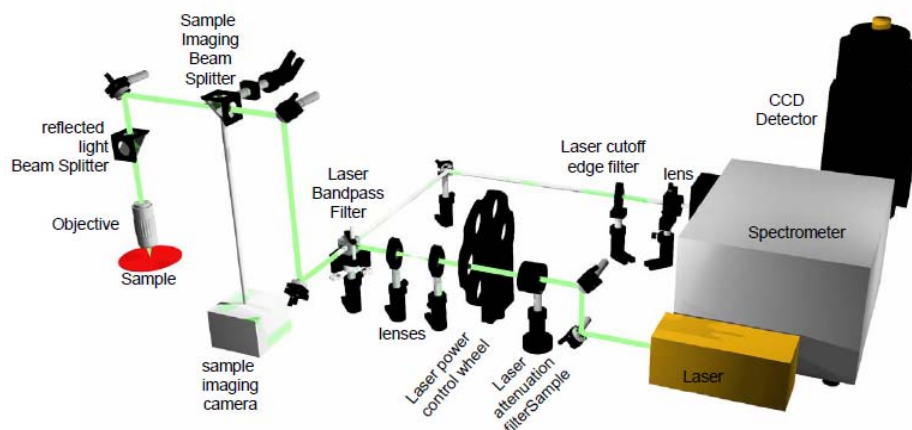


Figure 2.11 Schematic of Custom-built Raman System.[23]

Figure 2.11 shows schematically a custom-built Raman instrument used in this study. The characterization is performed by five operation processes as described following;

(1) The band pass filter sends the incident polarized light at 90° towards the microscope and removes the wavelength of the incident light from the light going straight through the cube.

(2) The laser cut-off filter removes all energies higher than 532 nm while allowing detection and measurement as low as 100 cm^{-1}

(3) Alignment of the solid state YAG laser with 532 nm wavelength and 100 mW maximum output power from coherent.

(4) Three grating, computerized turret provides large spectral range and dispersion

(5) Ultra long working distance Mitutoyo objective with effortless manual

sample height adjustment providing <5 μm resolution. (typically ~1 μm)

2.5.4.3 Raman Study of Silicon Nanowires

Raman spectroscopy is a nondestructive technique used to study the molecular/crystal structures of solids and bonding via their vibrational properties. For solids, examination of line shapes of Raman spectra give useful information of crystallinity, amorphicity, and dimensions of nanoscale silicon. Raman scattering of crystalline silicon in various forms, such as bulk, nanoparticles, and nanowires, has been investigated extensively.[22, 24]

Raman spectroscopy of amorphous and nanocrystalline R-Si:H films was also investigated. It was found that the second-order acoustic bands 2LA (longitudinal acoustic) and 2TA (transverse acoustic) do not seem to be influenced by confinement effects and are similar to those in the bulk. The second-order optic bands are broadened and shifted in comparison to those in the bulk. It has been known that, in addition to the first-order Raman scattering, higher order Raman scattering may also give important information of vibrational properties of nanocrystalline silicon and, therefore, attracted much attention from scientists in the past few years.[24-26]

Restricted to the Raman selections rule[25], only the transverse optical (TO) phonon mode is Raman active during the first order scattering process for silicon nanowires. The investigation of the temperature dependence of high-order Raman spectra, by considering the participation of other phonons in the scattering process, will help us to acquire information of vibrational properties and phonon related

interaction of silicon nanowires which cannot be obtained merely from the first-order Raman spectra.[27-29] Moreover, silicon is a semiconductor that has an indirect band gap with low light emission efficiency. So far, porous silicon and silicon nanocrystallities were found to have efficient photoluminescence covering almost the whole range from infrared to ultraviolet region. During the electron transition process for the materials with an indirect band gap, the participation of single phonon or multiphonon is inevitable. The study of electron-phonon and photon-phonon processes in the temperature-dependent Raman spectra is therefore useful for further investigation of the light emission of silicon nanowires.[25]

Chapter 3

Enhanced Nanowire Growth at Low Temperatures

3.1 Motivation of Research on Low Temperature Growth of Silicon Nanowires

In most processes that fabricate silicon nanowires, the growth temperatures have been greater than 900-1000˚C. For chemical vapor deposition (CVD), the growth temperatures could be lower than 900-1000˚C, but the crystalline quality of the silicon nanowires is often poor. Also, the aggregation of gold at elevated temperatures is a major problem when trying to control the diameter of Si nanowires. At one time, it was believed that the good crystalline silicon nanowires could not be achieved.[30, 31]

We have been performing research on the low-temperature decomposition of disilane to grow Si nanowires. The synthesis from disilane has been reported at temperatures above 500˚C,[32] however, these studies yielded diameters that were generally large and uncontrolled due to the agglomeration of the Au catalyst. To reduce wire diameters and increase their uniformity, more controllable lower temperature growth processes needed to be developed.[33-37]

We have conducted a study of the growth conditions aimed at optimizing and enhancing the Si structures produced at low temperatures. Our initial study began with finding an appropriate low temperature to characterize the nanostructures grown by both solely thermal and combined thermal and disilane plasma activation. For the purposes of this dissertation, a reference to disilane plasma activation implies that the plasma is imposed on top of the same

deposition conditions as used for thermal activation. This was then followed by identifying and standardizing the preparation of the silicon nanowires prior to the deposition anneals. This included not only working out the cleaning and depositing films of the gold catalyst, but in identifying a consistent preannealling procedure for converting the gold film into distinctive arrays of gold nanodots, or seeds, under which the nanowires would grow.[38] That preparatory work is reported in this chapter.

3.2 Nanowire Nucleation at Low Temperature

From the Au–Si phase diagram (Figure 1.5), it is apparent that the growth temperature must exceed the eutectic temperature of 365˚C for the VLS growth. We were interested in examining the deposition behavior both above and below this temperature so as to elucidate reaction behavior and to target an appropriate temperature for future studies.[33] Thus, we studied nanowire growth between 340 and 410˚C. Syntheses by thermal CVD were performed on Si (111) oriented substrates. The plasma power was set at a constant 2.3 watts. The Au nanodots were formed by thermally depositing 2 nm Au films, followed by preannealing at 520˚C for 5 minutes. Disilane flow was set at 6.825 sccm and the partial pressure of disilane was 14.9 mTorr. The deposition time was 5 minutes.

In both cases, early stages of pregrowth (before nanowire elongation) nucleation of crystalline Si in the form of nanobuds were progressively apparent. Figure 3.1 shows the morphologies of deposited nanowires by both thermal (a, c, e) and plasma (b. d. f) deposition at 340˚C (a, b), 380˚C (c, d) and 410˚C (e, f),

respectively. At 340˚C, some Si nanowires barely nucleated and failed to grow from the 2 nm Au seeds under thermal only conditions.[33, 35] However, plasma stimulation revealed some formation and growth of wires with small diameters (149 nm) and short lengths (0.48 μm). This is because of the likely present of solid alloy, rather than liquid allow, which allowed only slow decomposition rates of disilane gas and the diffusion rate of Si (across the vapor/solid (or liquid) interface of the alloy catalyst) that were insufficient to support nanowire growth.

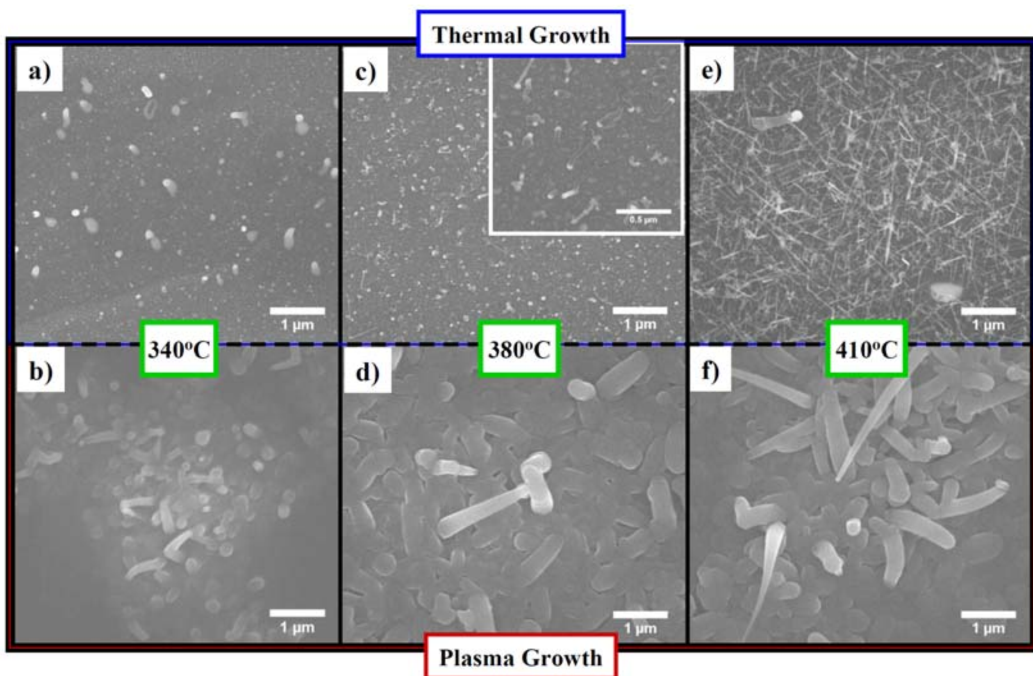


Figure 3.1 FE-SEM images of synthesized Si nanowires at various low growth temperatures: (a, b) 340˚C, (c, d) 380˚C (e, f) 410˚C by thermal (top) and plasma (bottom) growth, respectively. All growth processes are after preannealing at 520˚C for 5 minutes.

At a higher temperature 380˚C, nanowires started to grow as shown in Figure 3.1 (c, d).[33, 35] For thermally grown nanowires (Figure 3.1 c), the nanowires were generally short (0.243 µm), thin (<50 nm) and sparsely dispersed. On the other hand, worm-like shapes were observed for plasma grown wires as seen in Figure 3.1 d. The dimensions were 1.07 µm in length and 408 nm in diameter. For thermally grown nanowires at 410˚C (Figure 3.1.e), axial growth (elongation) took place favorably yielding dense and straight nanowires of high aspect ratios and with uniform diameters (32 nm) along their lengths (1.57 µm). Under plasma enhanced conditions at 410˚C, the nanowires grew longer (1.92 µm) and thicker (421 nm) compared to nanowires grown thermally. It was observed that the catalyst gradually disappeared during growth, resulting in strongly tapered shapes.[31, 35, 39] The nanowires were much broader at their bases than for thermally grown nanowires indicating that lateral, or radial, growth was substantial. [26]

Figure 3.2 describes the measured diameter and length of nanowires grown by both thermal CVD and disilane plasma CVD. Thermally grown Si nanowires obtained by using Au and disilane were usually only very slightly tapered. This indicated that radial growth was very slow compared to axial growth. Compared to the thermal growth condition, greater increases of both diameter and length were seen in nanowires grown in a disilane plasma. In other words, the increased nanowire growth rate due to the plasma was markedly greater than for thermally grown nanowires,[40] that is, 10 times faster for axial growth and 1.2 times faster for radial growth.

For pure thermal activation, disilane physically absorbs onto the eutectic Au-Si surface and then decomposed through subsequent hydrogen dissociation. However, faster and more efficient growth rate under plasma conditions could be explained in terms of the effect of the plasma on forming disilane radicals in the gas phase. These radicals increased the net conversion of gaseous disilane to Si atoms on the liquid Au-Si catalyst surface. Also, these radicals strongly adsorb onto the surface, thus, promoting faster incorporation of Si into the droplet and accelerating nucleation times and growth at the silicon nanowire tip.[10]

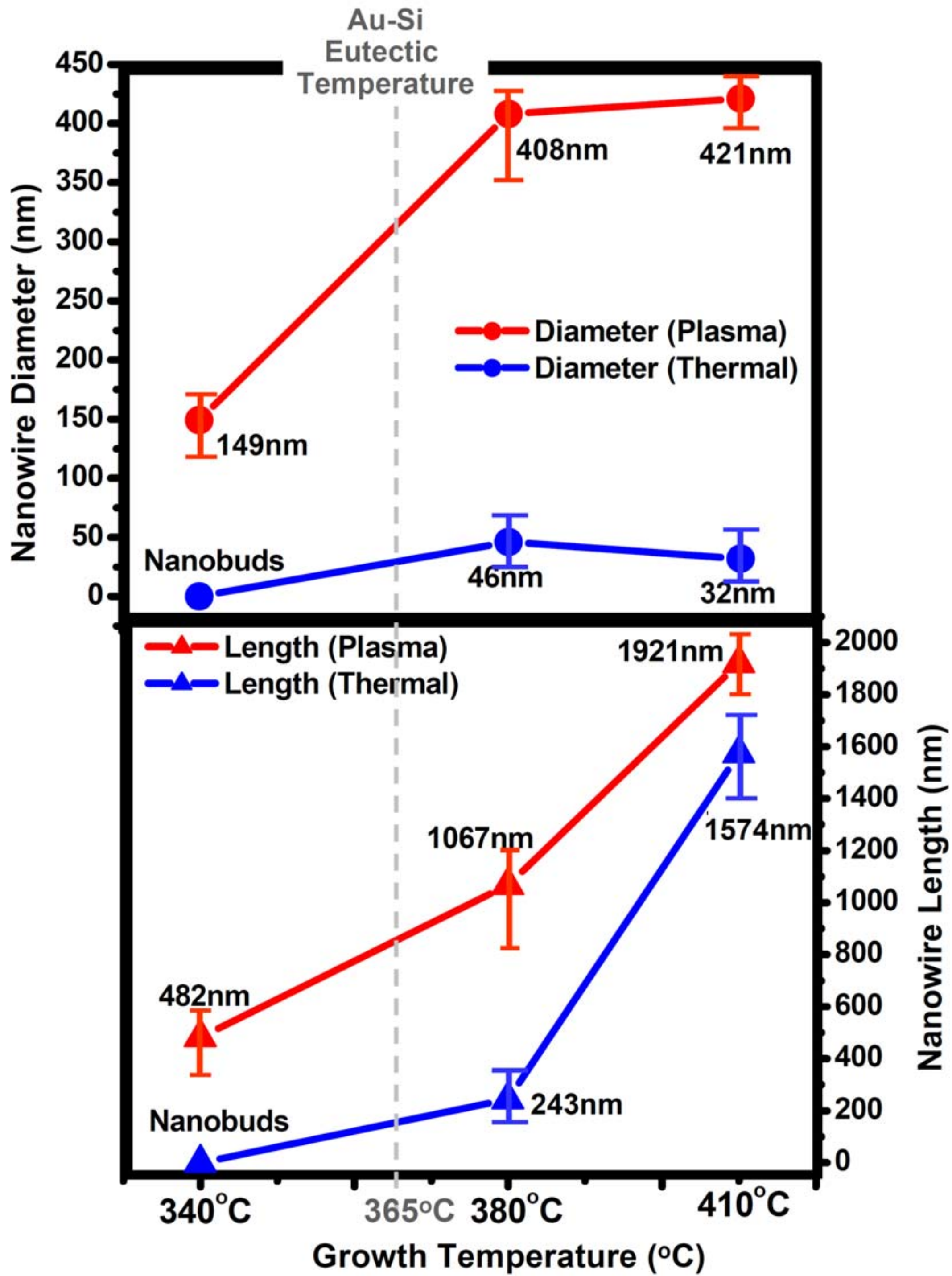


Figure 3.2 Average diameter and length of silicon nanowires grown after 5 minutes as a function of the growth temperature.

3.3 Effect of Preannealing Treatment on Silicon Nanowire Growth

The effect of the morphologies of the Au thin films on the resultant silicon nanowire morphologies and dimensions were also studied as a function of the conditions for annealing the gold films and their subsequent conversion to a nanodot array.[13] When a 2 nm-thick Au film was deposited onto a Si (111) wafer and heated to 520˚C for 5 min, the Au layer partially broke up by "de-wetting", and forming Au-Si nano droplets on an otherwise smooth, but thinner, Au nano layer. In fact, the Au-Si phase diagram has the eutectic point at 363˚C (18.6 at. % of Au), and upon solidification of Au-Si droplets under the eutectic temperature, phase separation occurred between Au and Si.[4, 10, 41]

The droplets coarsened by a ripening process via surface diffusion to create larger hemispherical clusters.[41] The distribution of Au nanodots is shown in Figure 3.3 (a1). The characteristics of their sizes, shape and distribution are also shown to be very un-uniform. The sizes of Au nanodots vary between 0.1 μm up to 1.1 μm. Each nanodot was typically separated from one another by 3.5 μm to 5.6 μm in distance. Figure 3.3 (b1) and (c1) shows FE-SEM plan-view and cross-sectional view images of thermally grown Si nanowires after preannealing treatment at 520˚C for 5 minutes. The images confirm that thermally grown Si nanowires are much thinner and shorter compared to the plasma grown nanowires. However, under plasma growth conditions, the irregular and un-uniformed distribution of Au nanodots results in a random distribution of Si nanowires as shown in Figure 3.3 (d1) and (e1). Because the Si growth rate is faster under plasma conditions, Si nanowires are randomly grown.[30, 42] However, thermally

grown Si nanowires have much slower growth rates compared to the plasma condition. Thus, thin and short Si nanowire can be grown uniformly along the entire substrate as Au diffuses to the surface gradually.[40]

To solve the random distribution under plasma growth condition, we controlled the preannealing condition as follows. Gold thin films were annealed at a higher temperature, 590˚C and for a longer time, 9 minutes. This higher preannealing temperature and longer time brought about a more distinct coalescence of Au nanodots, presumably without an intermediate residual surface layer of gold on the silicon substrate. In fact, the higher preannealing temperature and longer time allowed more diffusion of Au nanodots to take place, leading to larger diameter clusters.[38] Thus, these modest changes compared to the conditions at 520˚C and for 5 minutes produced more reproducible results.

With this new preannealing treatment at 590˚C for 9 minutes, the distribution of Au nanodots is shown in Figure 3.3 (a2). The size of nanodots is between 0.14 μm and 0.32 μm, which indicate that the size range of nanodots is smaller than by the previous preannealing treatment. The gold nanodots are separated by 1.5 μm to 3.2 μm in distance.

With these well-distributed Au nanodots, Si nanowires can grow more uniformly on the entire substrate by either thermal or disilane plasma growth conditions. Figure 3.3 (b1) and (c1) show in plan and cross-sectional views FE-SEM images of Si nanowires that were thermally grown. Significant changes in morphologies are shown for the Si nanowires by plasma-enhanced condition in Figure 3.3 (d1) and (e1). Unlike the randomly distributed nanowires for the pre-

520˚C for 5 minute preannealing treatment, the new pre-annealing treatment contributes to enhanced uniformity.

A comparison was also done on the effect of different substrate orientations and resistivivities on nanowire growth. For this, the substrate pre-annealing treatment at 590˚C for 5 minutes was used. Nanowires were grown simultaneously on side-by-side substrates corresponding to the following orientation and resistivity combinations: Si(100) (0.001~0.003 Ωcm), Si(100) (5 Ωcm), and Si(111) (0.001~0.003 Ωcm). This allowed for a qualitative examination of to be made directly.

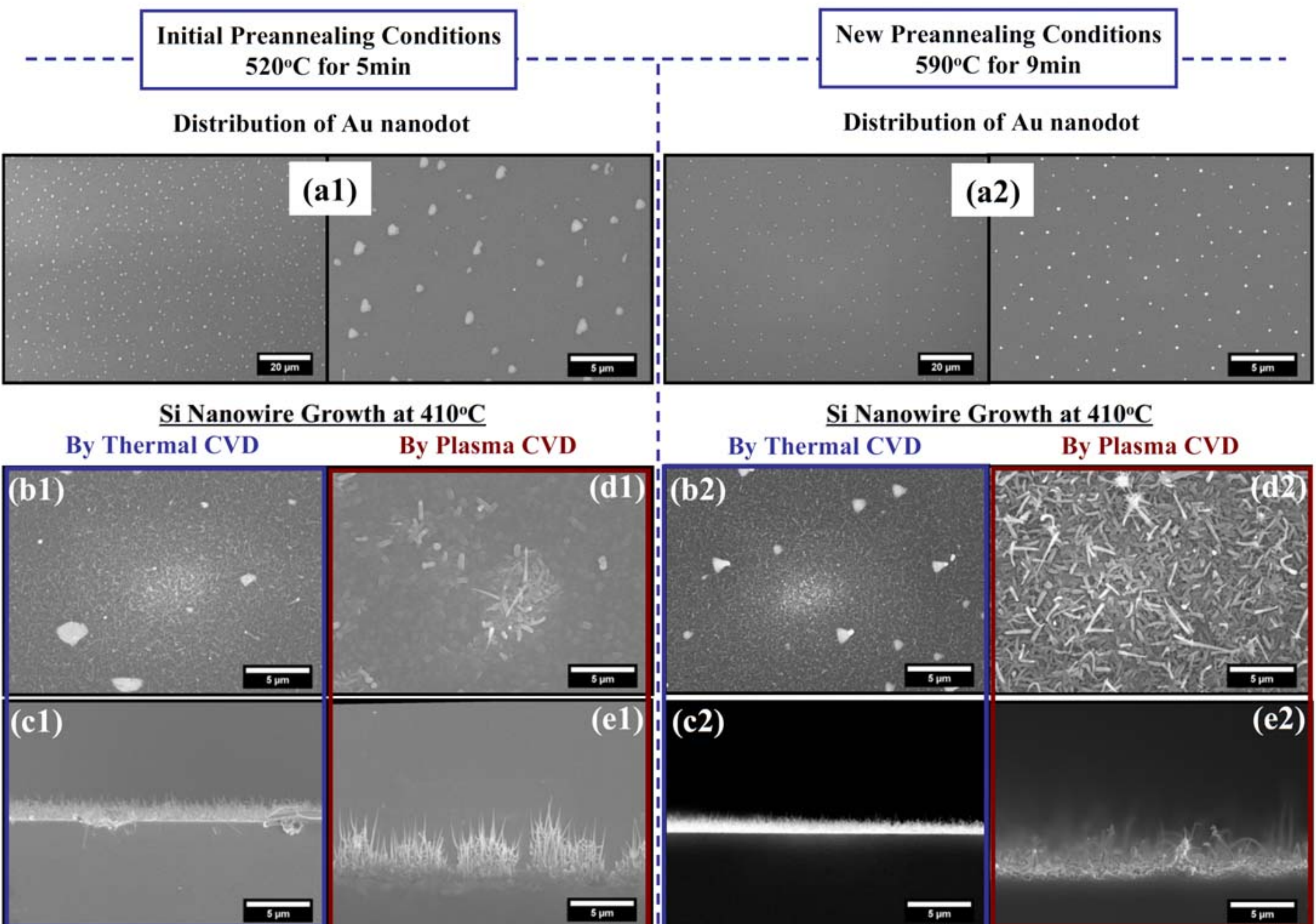


Figure 3.3 Preannealing Effect on Au distribution and Si Nanowire Growth

The FE-SEM micrographs shown in Figure 3.4 show the results of nanowires grown on the different substrates and for two different preanneal conditions. Nanowire growth on Si (111) substrates receiving a 5 minute preanneal treatment at 520˚C exhibited a dense forest of nanowires that were localized into domains. These domains were separated by what was otherwise clear areas of silicon substrate [Figure 3.4(a)]. Moreover, “tree-like” formations grew at the center of these domains, with nanowires branching first laterally and then turning upward. Some of the nanowires still had gold beads at their tips, but most did not. All of the nanowires were significantly tapered indicating that radial growth was significant in addition to the axial growth at the individual tips.[10]

Nanowires grown on the substrates receiving the 590˚C preanneal treatment were more uniformly distributed, without the clustering into domains [Figure 3.4 (b, c, d)]. The nanowires were thicker and longer and partially collapsed into mattes similar to that to be discussed in Chapter 5. Regardless of wafer orientation and intrinsic substrate resistivities, FE-SEM images showed uniform coverage. A comparison between the different substrates indicated a couple of significant differences.[18, 33] Growth on the Si (111) low resistivity substrate produced thick and well tapered nanowires, and some branching at critical lengths. Growth on the Si (100) low resistivity substrate produced much finer nanowires with a, more-or-less, even mix of vertically oriented nanowires versus curved nanowires. On the other hand, growth on the Si (100) high

resistivity substrate exhibited thick nanowires, almost all of which are significantly curved. This influence on curvature is the subject discussed in Chapter 4.4.

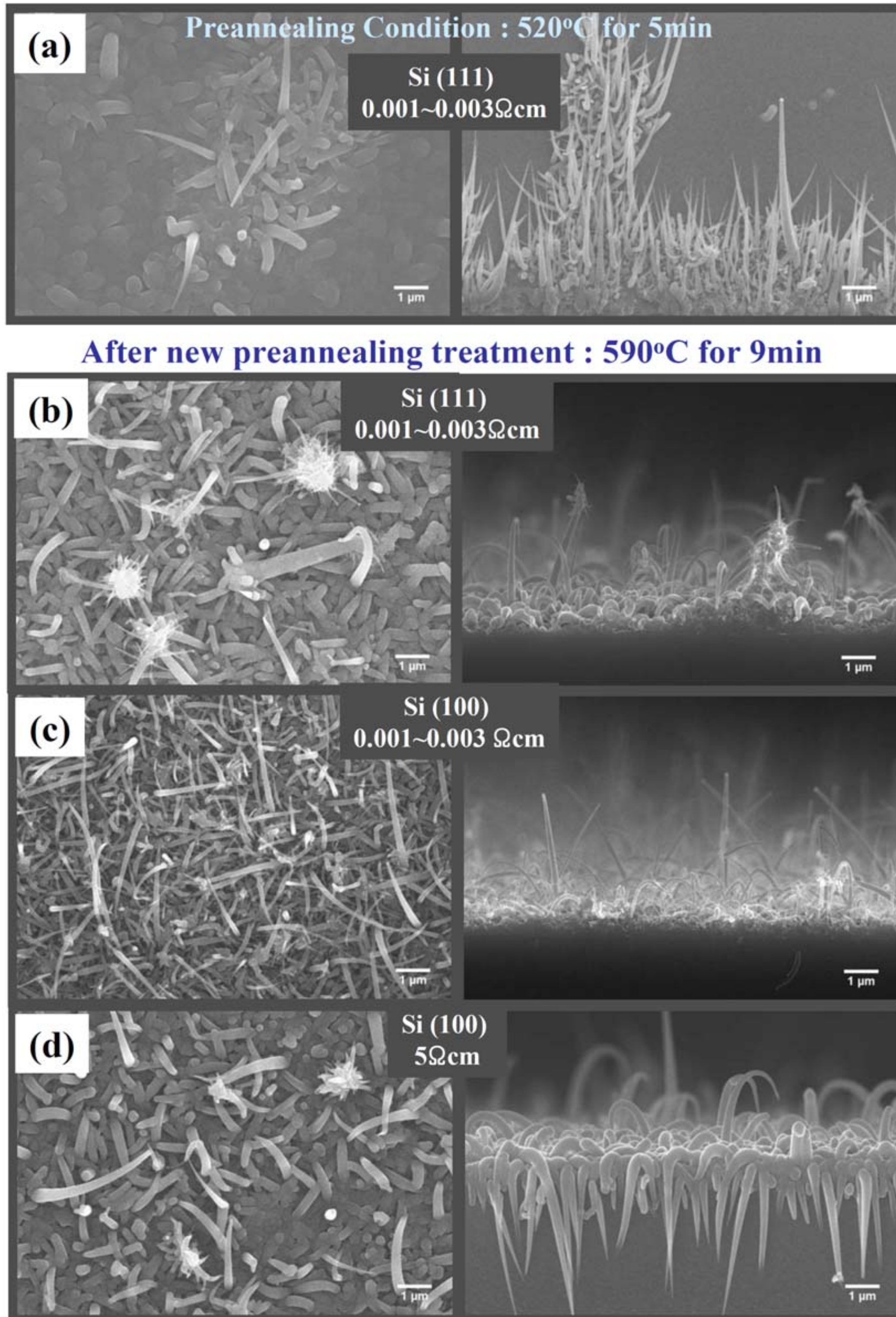


Figure 3.4 FE-SEM images of Si nanowires grown at 410˚C on substrates thermally pre-treated in hydrogen at (a) 520˚C for 5 min on Si (111) 0.001~0.003

Ωcm wafer, and grown on substrates similarly treated at 590˚C for 9min, (b) on Si (111) 0.001~0.003 Ωcm, (c) on Si (100) with 0.001~0.003 Ωcm, and (d) on Si (111) 5 Ωcm.

3.4 Conclusion

A series of preliminary studies were conducted to determine the standard experimental conditions to be used throughout the later studies described in this dissertation. Nanowire growth in disilane plasmas was studied as a function of temperature, spanning from below, to just above, the eutectic temperature for the Si-Au system (363˚C).[37] In addition, a series of experiments were conducted on gold-coated silicon substrates with (111) and (100) orientations and having received either 520 or 590˚C thermal treatments in hydrogen in preparation for the deposition runs.[40]

Below the eutectic temperature, nanowire growth was not sufficient to produce anything worthy of study. However, the morphological variations for nanowires grown at 410˚C were complex and sensitive to the plasma power. This temperature was selected as the target temperature for nanowire growth for most of the rest of the work reported here.[38, 40]

With respect to the substrate preparation, thermal preanneals at 590˚C for 9 minutes generally led to more uniform distribution of nanowires subsequently grown at 410˚C by plasma-enhanced CVD. This was associated with the redistribution of gold on the silicon substrates.[32] Nanowires grown under these

conditions were also found to have high aspect ratios that were thicker and longer. Consequently, the 590˚C 9 minute preanneal treatment was adopted as a standard treatment of substrates.

Chapter 4

Comparative Study of Nanowire Morphology Between Thermal and Plasma-assisted CVD

In Chapter 3, we first carried out some preliminary experiments for the purpose of identifying the important preparatory procedures for nanowire growth by thermally and plasma-stimulated CVD at low temperatures. After selecting an appropriate target temperature of 410˚C to grow Si nanowires, we also selected a procedure for pre-annealing (at 590˚C for 9 minutes) the gold-coated substrates. This optimized the distribution of gold beads on the substrate that would later catalyze the nanowire growth via the vapor-liquid-solid (VLS) mechanism.

In this chapter, a more detailed comparative study is described on the nanowire morphologies after growth by simple thermal and by plasma-assisted activation of the gas phase reactions. Unlike the straight shapes of thermally grown Si nanowire, curved nanowires are common when grown in a disilane plasma at low temperatures. This is unlike at higher temperatures above about 500˚C where the nanowires are typically straight regardless of whether they were by either process.[10] Thus, the focus will be on the nanostructural characteristics and differences as characterized by the nanowire growth direction, diameter, length, and surface morphology. The effect of disilane partial gas pressure is also examined towards the end of the chapter. Bending tends to be more pronounced with an increase in disilane partial pressure.

The characteristic of bending nanowires is studied in terms of their bending curvatures and geometrically calculated strains. Raman Spectroscopy is used as an experimental method for characterizing bending nanocrystallinity due to the measured curvature by geometrical method.

4.1 Effect of Wafer Orientation on Silicon Nanowire Orientations under Thermal Growth Conditions

Electron (SEM) micrographs are shown in Figure 4.1 of epitaxial <111> and <110> oriented nanowires thermally grown on Si(100) and Si(111) substrates. When grown on Si (100) substrates and when seen in plan-view, (Figure 4.1a and Figure 4.1b), the orthographic projections of <111> nanowires are oriented at 90º angles with respect to one another. These are coplanar with the four fixed <111> directions of the silicon substrate.[2] Epitaxial <110> oriented nanowires are also shown in plan-view projection in these same figures. They are oriented at 45º angles to the <111> nanowires and to the edges of the micrographs. When viewed from the side, Figure 4.1c, the azimuth angles formed between each set of nanowires and the substrate surface are shown, in good agreement with the crystallographic directions of the substrate.[43]

The orthographic projections of <111> and <110> nanowires are seen to form rectangular networks as illustrated in Figure 4.1b on a Si (100) substrate. Under this condition, the nanowire diameters are between 22-32 nm and 28-49 nm ranges for <111> and <110> nanowires, respectively. Also, the average length is approximately 909.67 nm.

A similar comparison is given of nanowires grown by thermal CVD onto Si (111) substrates in the sequence of micrographs given in Figure 4.1.d, 4.1.e and 4.1f. Here, the equivalent [111] and [110] directions correspond to the trigonal symmetry of the substrate, whose projections form 120˚ angles in the plane of the micrograph. A fourth direction is pointed directly out of the page, normal to the substrate surface. When viewed from the side, the <111> oriented nanowires.[43] These latter nanowires are seen as bright spots on the plan-view image due to the gold beads at the tips.

Figure 4.1.f is a side view SEM image showing azimuthal angles of the nanowires thermally grown on Si (111). It shows make an angle of 19.4º with the substrate, while the fourth [111] direction is perpendicular. The diameter range is 26-52 nm and 1.67 µm in length is observed.[49]

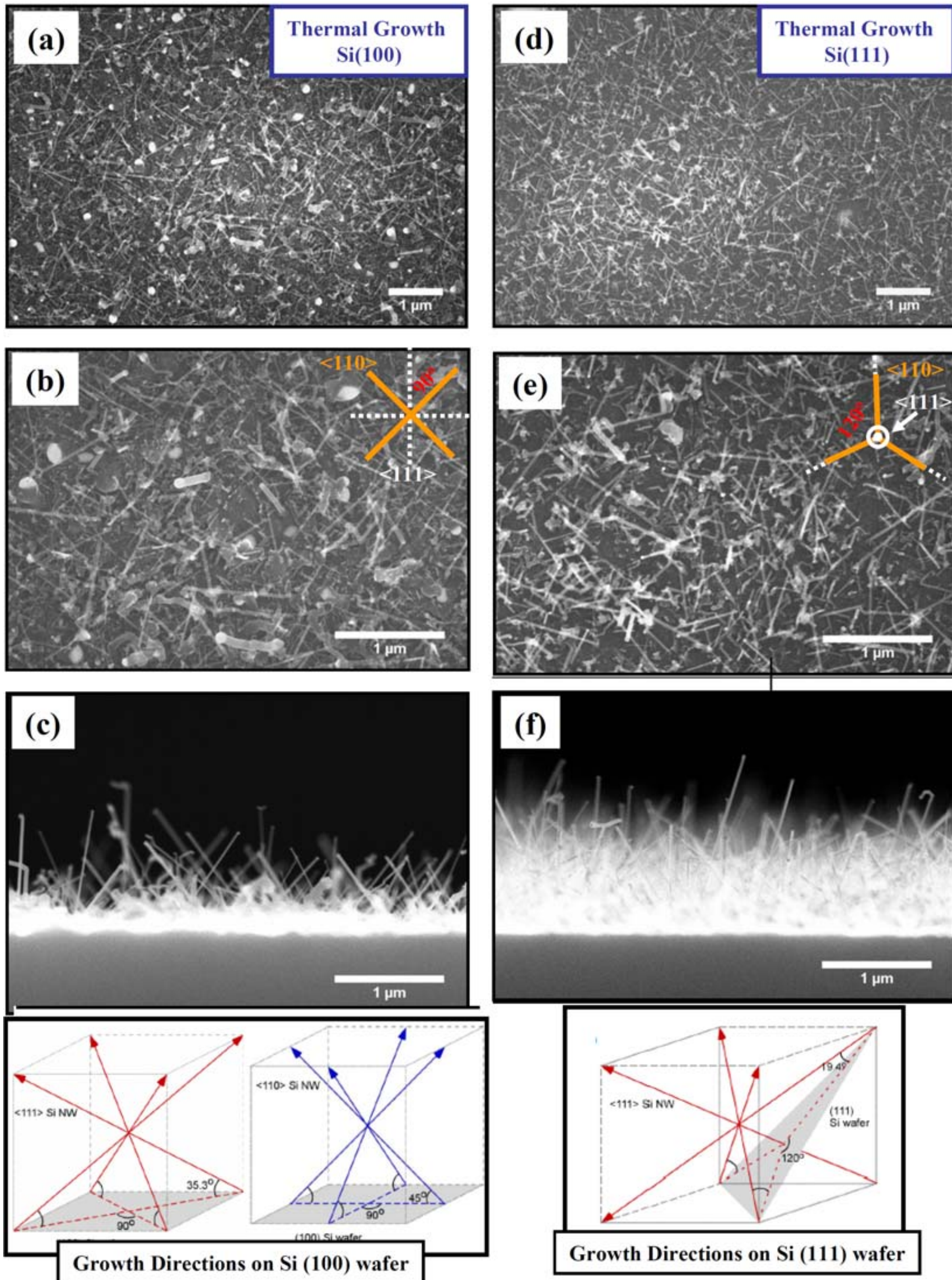


Figure 4.1 a, b) Plan view SEM images c) Cross-sectional view of Si nanowires grown on Si (100) substrate d, e) Plan view SEM images f) Cross-sectional view

of Si nanowires frown on Si (111) substrate at 410ºC, 154 mTorr growth pressure, and 5 min growth time

4.2 Influence of RF Plasma on Si Nanowires Growth at Low Temperature

Plasma-enhanced synthesis is shown to significantly alter the nucleation rate and activation energy for vapor-liquid-solid (VLS) silicon nanowire growth compared to thermal growth,[10] providing new control over nanowire morphologies and new insight into the rate-limiting mechanisms of VLS growth. Low power RF plasma excitation can be used not only to pre-ionize the gas making it more reactive, but also to accelerate surface mobility on condensed phase surfaces.[40]

Unlike thermally grown VLS, plasma-stimulated Si nanowires dramatically increase growth in the lateral directions. Regardless of the wafer orientation, Si nanowires grow thicker and longer than for thermal only conditions. They often develop a taper, being thickest at the base where it is exposed longest to the depositing gases. The increased growth rate under plasma conditions can be understood in terms of the effect it has on forming silane radicals.[44] These radicals in turn increase the net rate of hydrogen dissociation from Si atoms adsorbed on the liquid AuSi catalyst surface.[44, 45]

The effect of plasma enhancement on nanowire nucleation and growth is even more dramatic at low temperatures where thermal processes are slower. Figure 4.2 shows FE-SEM images of a, b) plan and c) cross-sectional view of Si nanowires grown on Si (100) substrates, and d, e) plan and f) cross-sectional view

of Si nanowire grown on Si (100) substrates at 410ºC, 154 mTorr growth pressure, and 5 min growth time. From all FE-SEM images, it confirms that some nanowires grow linearly and the others are bent. The mechanism of bending nanowires is discussed in Chapter 5.

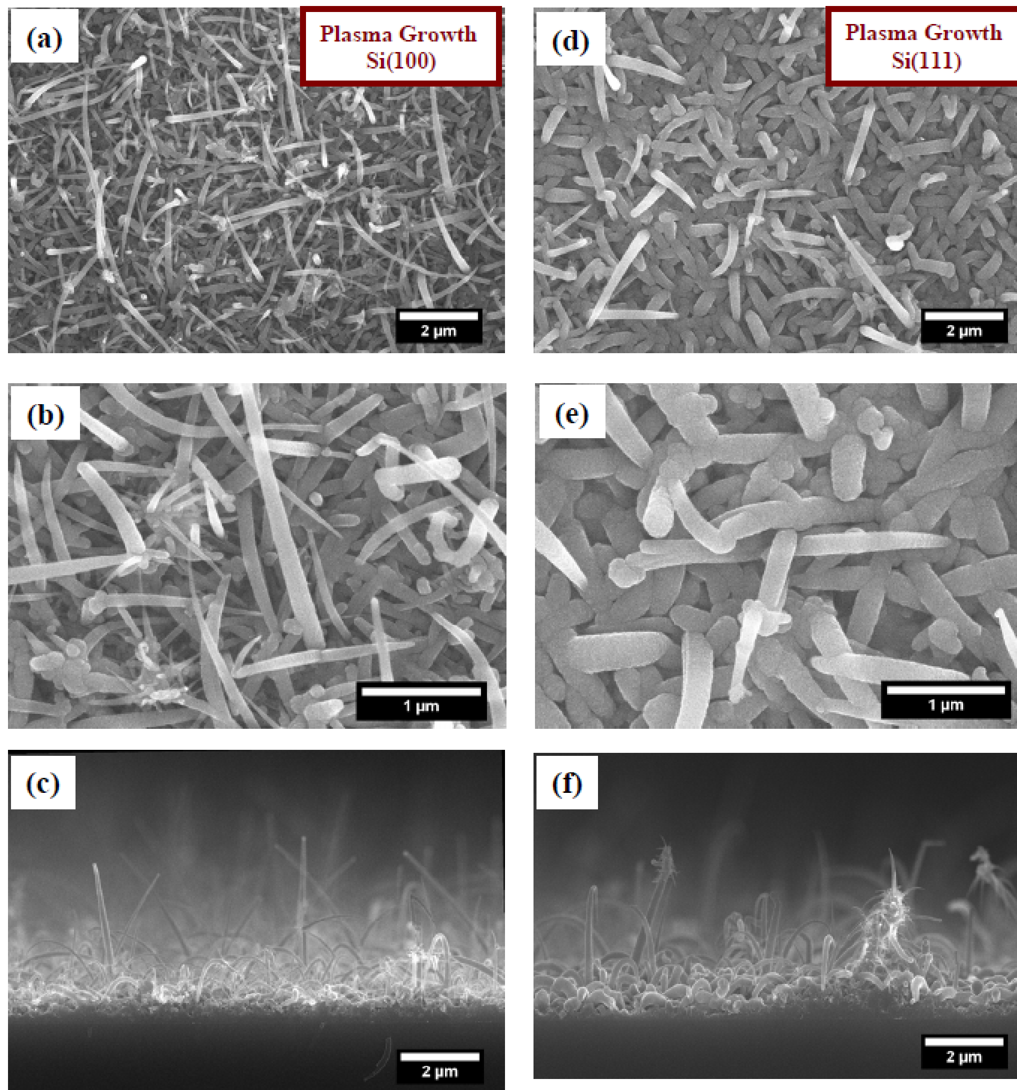


Figure 4.2 Plasma enhanced growth at 410ºC, 154 mTorr growth pressure, and 5 min growth time; a, b) plan view SEM images c) cross-sectional view of Si nanowire grown on Si (100) substrate d, e) plan view SEM images f) Cross-sectional view of Si nanowire grown on Si (100) substrate

4.3 Comparison of Thermal Growth and Plasma Growth of Silicon Nanostructure

Based upon the results illustrated in Figures 4.1 and 4.2, Figure 4.3 directly compares the nanostructural differences of surface morphology of Si nanowires grown by simple thermal activation and then assisted by plasma-stimulation. The structural differences of the nanowires are considered in terms of their orientations relative to the wafer, growth directions, diameters, lengths, and distributions over the surface.[10]

Compared to thermally grown nanowires, plasma stimulates the nanowires' properties to become thicker, longer, and to more densely cover the substrate surfaces.[10, 40] This trend is seen for growth on both Si (100) and (111) substrates.[40] Another significant difference is that nanowires are often bent when grown by the combination of disilane plasma, whereas the nanowires are linearly when grown thermally. It is interesting to note here that nanowires grown in disilane plasmas at higher temperatures are typically straight as is also typical in "silane"-hydrogen plasmas.[40, 42]

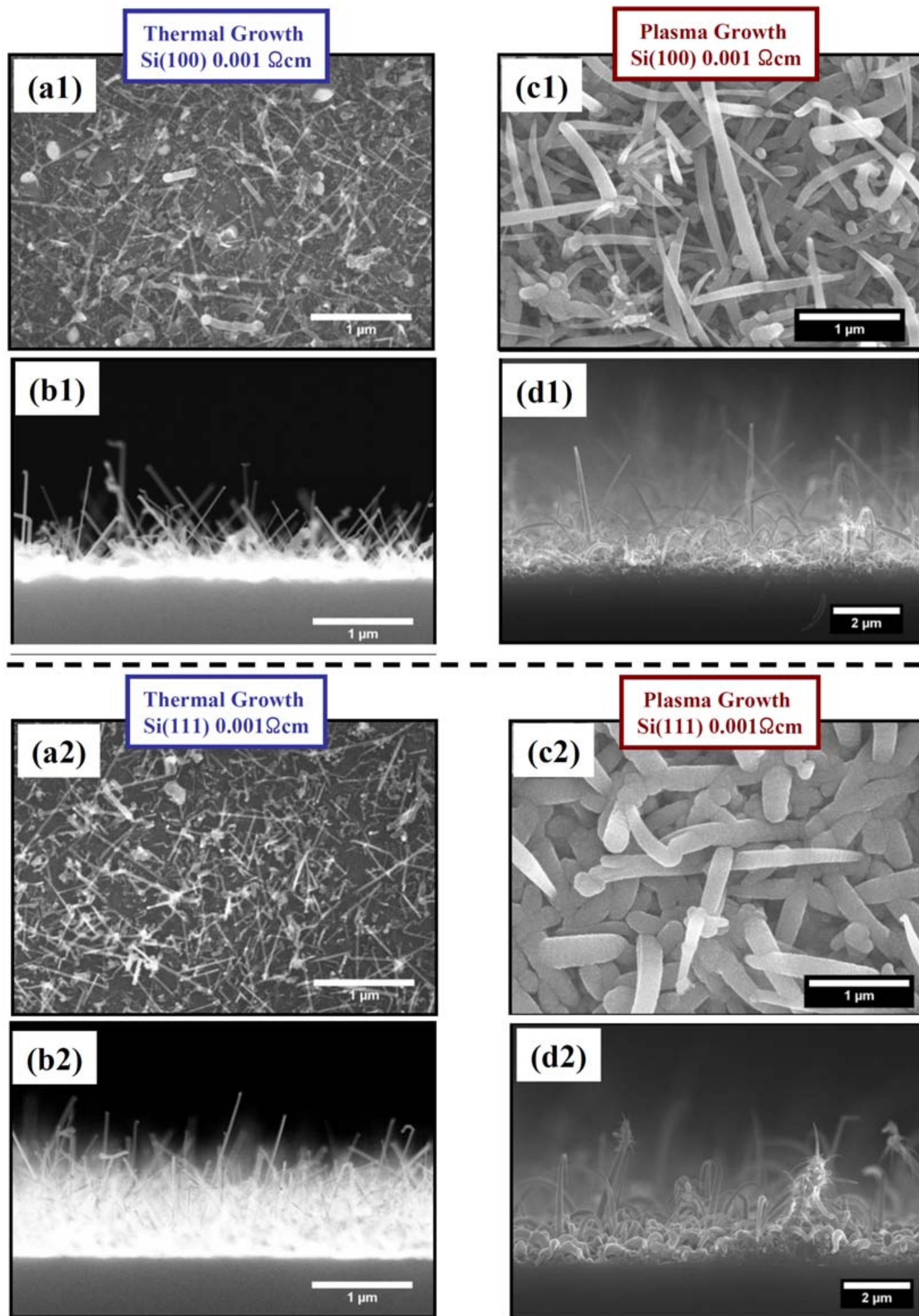


Figure 4.3 Comparisons of Thermal Growth and Plasma Growth of Si Nanostructure Grown on Si (100) Wafer (Top) and Si (111) Wafer (Bottom)

4.4 Influence of Disilane Partial Pressure on Silicon Nanowire Growth

The effect of disilane partial pressure on the morphology of silicon nanowire growth in plasmas is described in this section. A series of experiments of nanowires grown on substrates with 2 nm Au films were conducted using three disilane partial pressures within the range of $6x10^{-3}$ mTorr to $25x10^{-3}$ mTorr. The plasma power was fixed at 2.3 W. Figures 4.4 and 4.5 present collages of micrographs corresponding to nanowires grown on Si(100) and Si(111), respectively, as a function of both disilane partial pressure and total pressure. The differences in pressure are due to the hydrogen carrier gas.

For Si nanowires grown on (100) Si wafers in $6x10^{-3}$ mTorr disilane , shown in Figure 4.4, the nanowire morphology is typically thin, linear and densely distributed. The majority of nanowires are grown grow straight, with only a few nanowires gently bent. A similar morphology is seen for nanowires grown on Si (111), although a larger fraction of the nanowires appear to be bent than for those on Si (100). For nanostructure grown on Si (100), the nanowires were on average 110 nm in diameter and 2.84 µm in length, most of which grew in the <111> direction. The growth orientations of nanowires relative to the Si<110> substrate orientation could not be as easily identified. The growth orientations of the bent nanowire could not be identified, neither. More bent nanowires were seen in growth on Si (111) wafers compared to the (100) wafer. The diameters and lengths of nanowires grown under this condition were 190 nm and 2.83 µm,

respectively. For nanowires grown on both substrates, nanowires grown in the <110> growth direction were not identified.

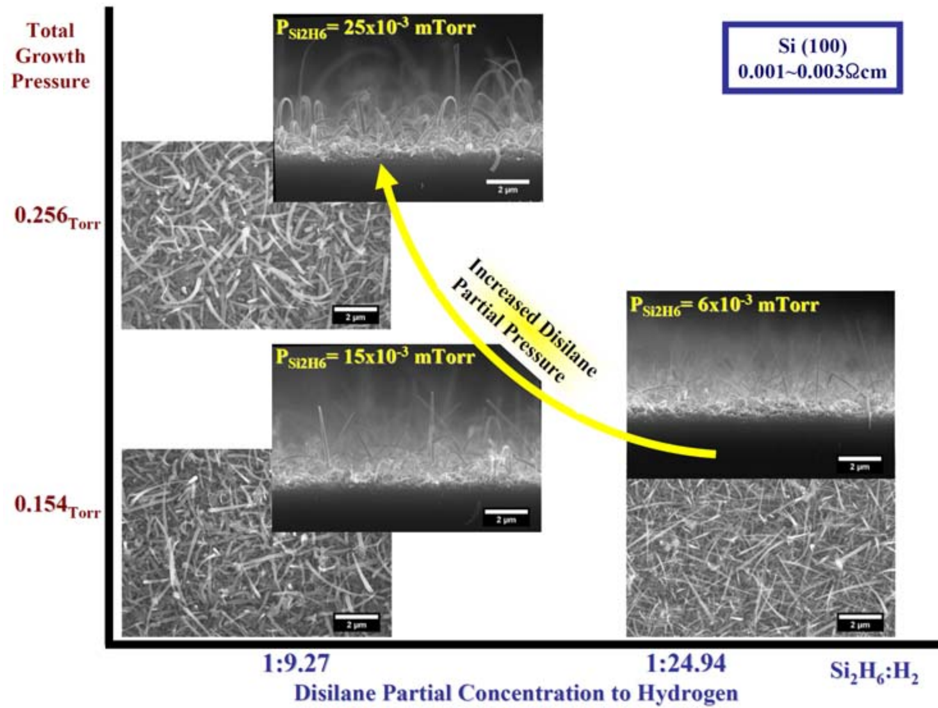


Figure 4.4 Influence of Disilane Pressure (as a Function of Total Pressure, and Disilane Partial Pressure Ratio to Hydrogen, and Disilane Partial Pressure) on Silicon Nanowire Growth on Si (100) Substrate. The plasma power was 2.3 W.

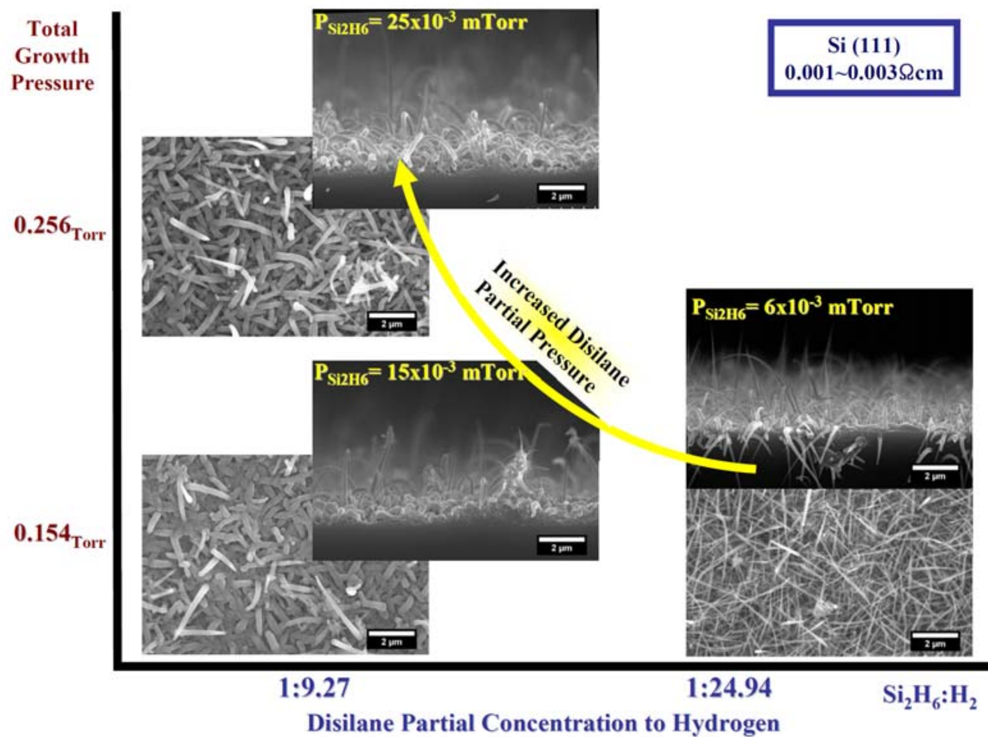


Figure 4.5 Influence of Disilane Pressure (as a Function of Total Pressure, and Disilane Partial Pressure Ratio to Hydrogen, and Disilane Partial Pressure) on Silicon Nanowire Growth on Si (111) Substrate. The plasma power was 2.3 W.

Silicon nanostructure at the higher disilane partial pressure of 15×10^{-3} mTor, is also shown in Figure 4.4 for nanowires grown on Si (100) wafer and Figure 4.5 for nanowires grown on Si (111) wafer. Compared to their growth at lower disilane partial pressure, 15×10^{-3} mTorr, more bending was observed for both substrates. The density of straight nanowires was less reduced, and the density of bent nanowires was greater compared to those grown at lower pressures. Also, the average diameters (120 nm for Si (100) and 270 nm grown on Si (111)

wafers) and lengths (2.88 μm for Si (100) and 3.28 μm grown on Si (111) wafers) all increased relative to the lower pressure.

At the highest disilane partial gas pressure, $15x10^{-3}$ mTorr, all nanowires grown on both Si (100) and (111) substrates were severely bent and appeared as if they collapsed into a dense matte. There was also very significant tapering. The diameters were also the largest observed for this series being 230 nm for nanowires grown on Si (100) wafer and 290 nm on Si (111) wafer. These nanowires were also longest being 5.1 μm and 5.36 μm for nanowires grown on Si (100) and Si (111) substrates.

By increasing the disilane partial pressure, the nanowire morphology shows obvious dimensional changes, which are plotted in Figure 4.6. They are longer and thicker nanowires. Their density of coverage density also increases with partial pressure. It is not surprising that the greater concentration of disilane that comes with increasing partial pressure increases the rate of deposition and, therefore, results an overall increase in all of the nanowire dimensions and densities.[46, 47]

It is interesting to note though, that while the lengths of nanowires grown on Si (111) and Si (100) are basically the same, regardless of pressure, their diameters are quite different. Generally, those grown on Si (111) are much thicker in diameter. The presumption here is that gold beads were typically larger when formed on the Si (111) substrates.

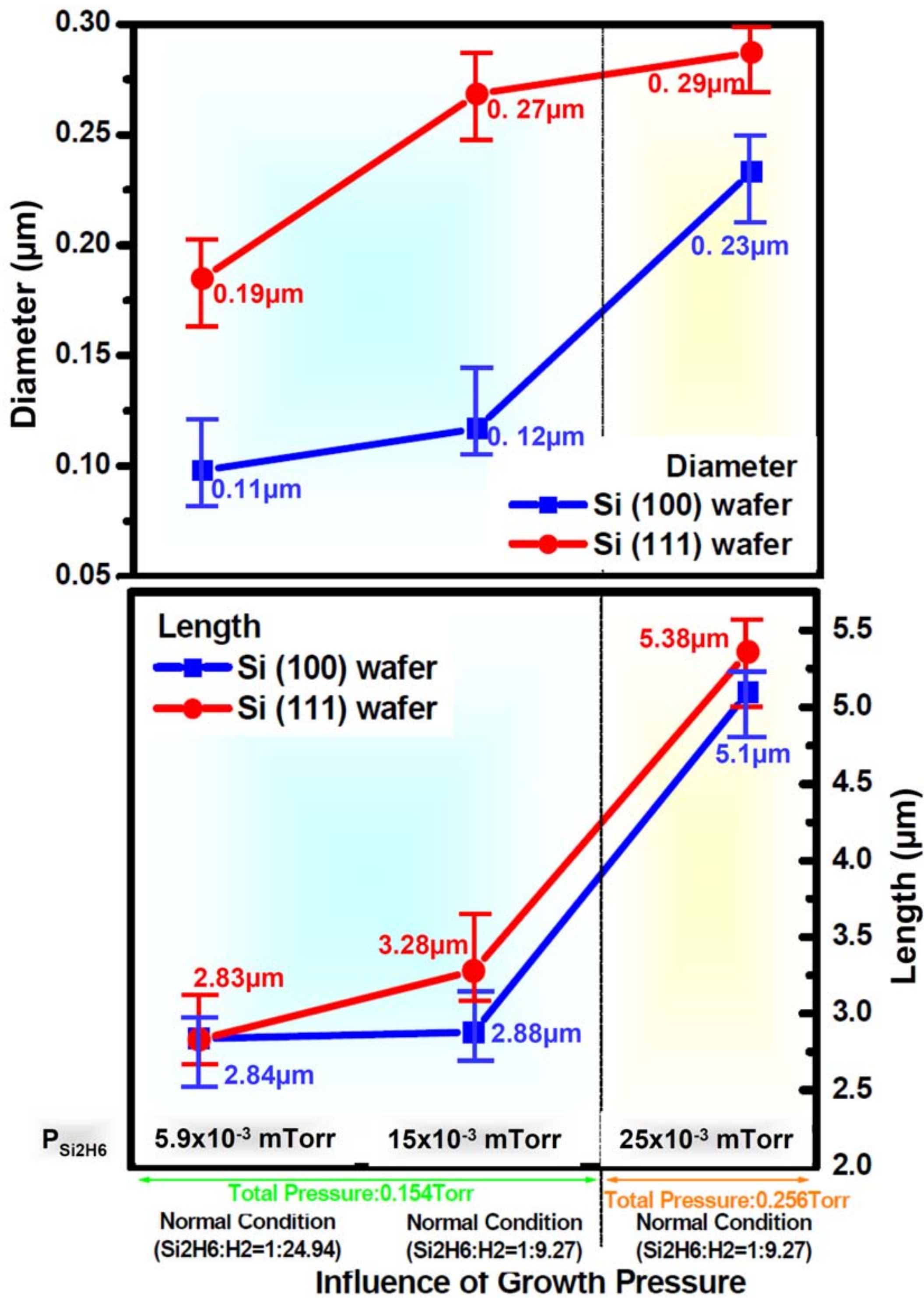


Figure 4.6 Comparisons of Nanowires Diameter and Length Dependent on the Gas Pressure Influence

4.5 Characteristic of Bending Nanowire

4.5.1 Bending Morphology of Si Nanowires

The curvature of Si nanowires grown under different disilane gas pressures is illustrated in the micrographs of Figure 4.7 corresponding to those grown on Si (100) and (111) wafer orientations. For P_{Si2H6} of $6x10^{-3}$ mTorr, more than 70% of the nanowires remained straight, whereas only 4 or 5 nanowires within the field of view were bent for either Si (100) and (111) substrates. At the higher disilane partial pressure of $15x10^{-3}$ mTorr, [Figure 4.7 (b)], fewer straight wires were seen, where only 2 or 3 linear nanowires were observed in the micrograph. For the highest disilane partial pressure of $25x10^{-3}$ mTorr growth condition as seen in Figure 4.7 (c), all nanowires were curved regardless of Si wafer orientation. Their curvatures for those grown on Si (111) appear more bent than nanowires on Si (100) substrate, which is related to their greater thickness. This latter point is a discussed in a later chapter.

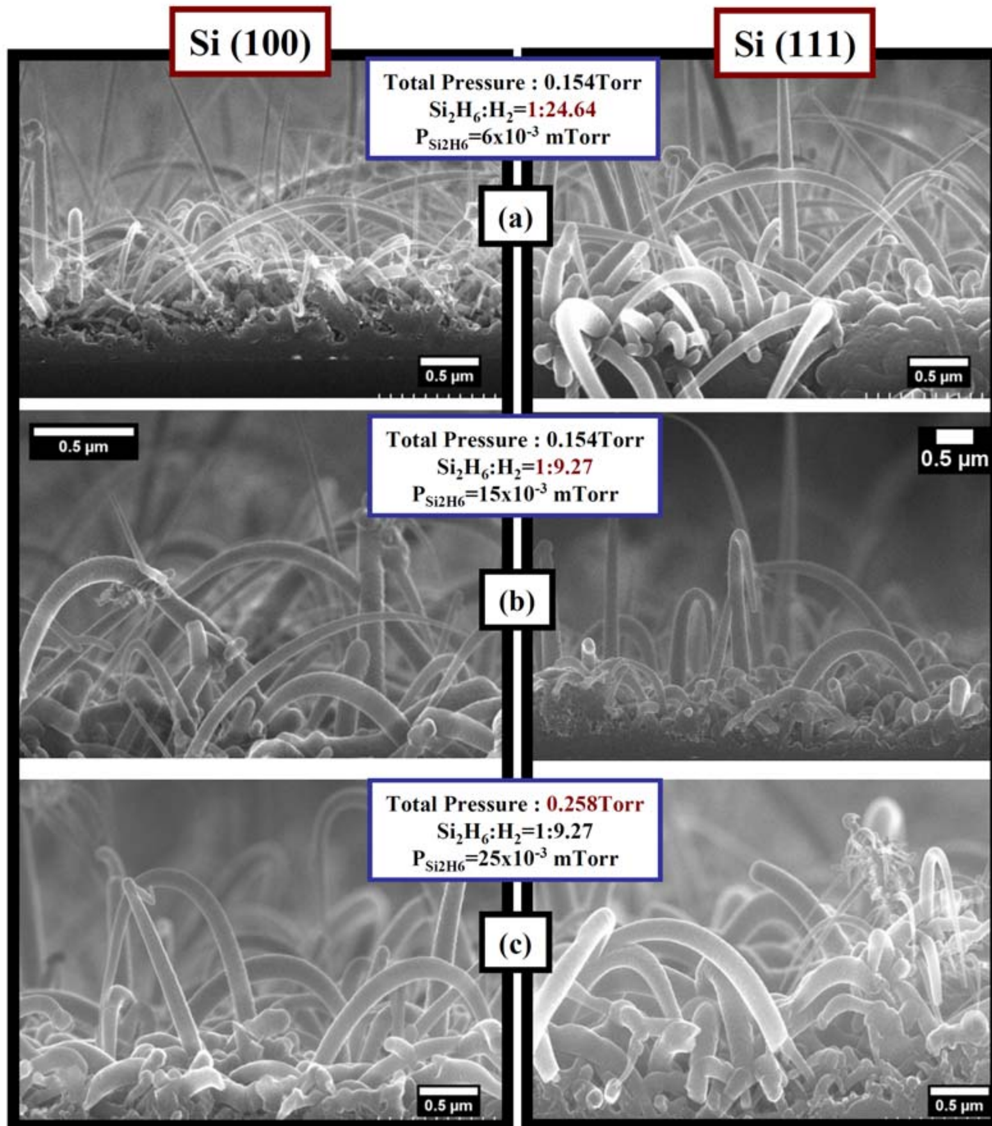


Figure 4.7 Bending Structures of Si Nanowires on Different Si Wafer Orientation under Plasma Growth Conditions with Different Gas Pressure

4.5.2 Geometrical Approach for Understanding Bending Nanostructures

With the common observation of bent, or curved, morphologies seen in Figure 4.7, bending structures of nanowires grown under different disilane partial pressure was characterized quantitatively by measuring the geometrical curvature. This was done using the procedure described by the Damon A. Smith research group.[48, 49] They assumed that a nanowire is semicircular. Thus, geometrically the radius of curvature, R, and the angle of curvature, α, can be related to the buckling cord length, L, as described in the inset of Figure 4.8. The bending curvatures (k) could then be estimated based on the measured radius of curvature (R) according to the equation $k(curvature) = 1/R(radius)$. Figure 4.8 plots the average curvatures observed as a function of nanowires grown under the different disilane partial pressures in the previous sections. For the Si nanowires grown at a disilane partial pressure of $6x10^{-3}$ mTorr, the radii of curvatures were large, thus implying relatively small curvatures of 1.46 μm^{-1} and 1.76 μm^{-1} for Si (100) and (111) substrates, respectively. At $15x10^{-3}$ mTorr disilane partial pressure, the curvatures were 2.31 μm^{-1} for Si (100) and 3.04 μm^{-1} for Si (111) substrates. The greatest curvatures were observed for nanowires grown at the highest disilane partial pressure of $25x10^{-3}$ mTorr, being 2.81 μm^{-1} and 3.13 μm^{-1} for Si (100) and (111) substrates, respectively.

In combining all of these observations of curvatures, the trends in nanowire growth in disilane plasmas indicate that the faster nanowires grow, the more likely they are to curve and with greater curvatures (smaller radii of curvatures). Coincident with this is that the nanowires are generally thicker. A

comparison between nanowires grown on Si (100) and Si (111) substrates indicates that the nanowires of the latter are generally thicker and more curved. Considering the controlling growth variables, then it can be expected that more curved nanowires would grow under conditions of higher plasma powers, high disilane partial pressures and on Si (111) substrates

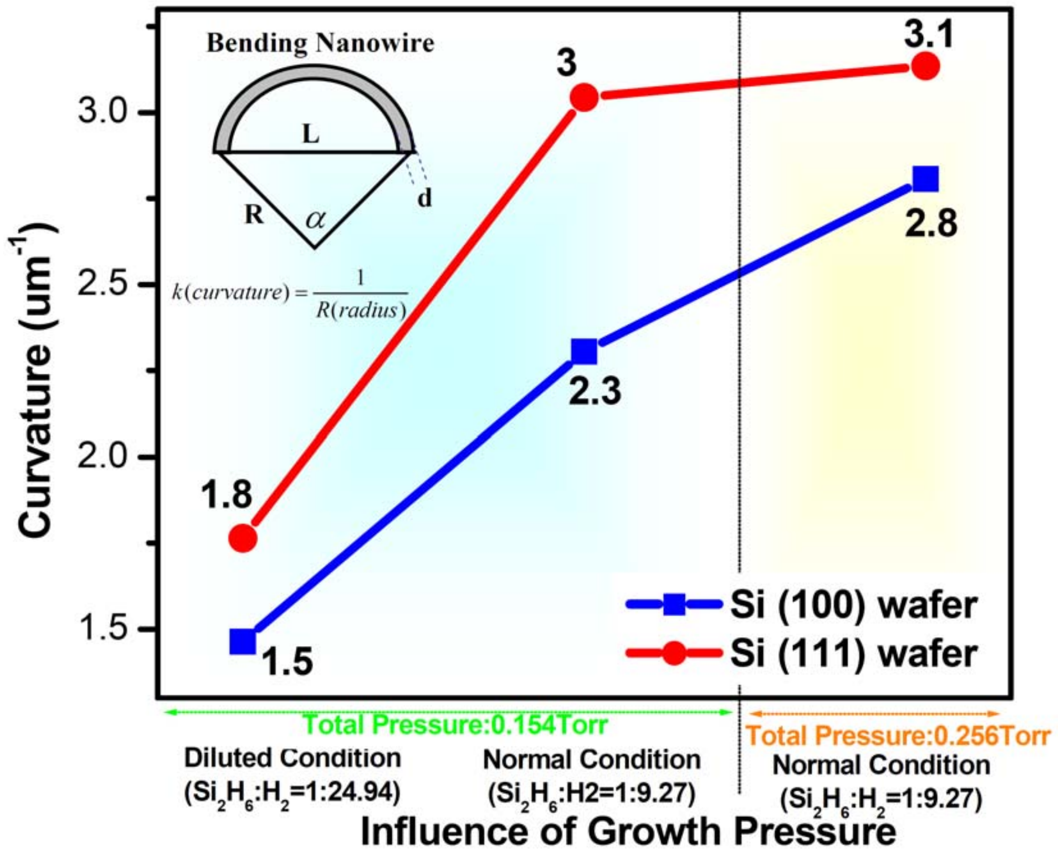


Figure 4.8 Calculated curvatures for Si bending nanowires grown on Si (100) and (111) substrates with varying gas pressures.

4.5.3 Experimental Approach for Measuring Bending Strain of Si Nanowires

One means of characterizing the materials effects due to bending is provided by Raman spectroscopy. Such measurements were performed using a YAG laser (532 nm) and at low excitation powers (5 mW). Low powers were used to avoid heating the nanowires, which can cause asymmetric broadening and a downshift of the Raman peaks. Figure 4.9 shows the Raman spectra of a bare Si (111) wafer, Si nanowires thermally grown at 410°C, and plasma-enhanced grown Si nanowires (grown 15×10^{-3} mTorr and 25×10^{-3} mTorr disilane partial gas pressures).

In Figure 4.9, the blue-colored peak at 520.48 cm^{-1} corresponds to transverse optic (TO)/ longitudinal optic (LO) mode of a bare Si (111) substrate. The Raman peaks for Si nanowires grown by thermal and plasma CVD conditions are all down-shifted. For thermally grown Si nanowires, shown as black in Figure 4.9, the peak is only slightly shifted to 517.92 cm^{-1}. On the other hand, the peak shift is much greater (to 496.22 cm^{-1}) for plasma grown nanowires at 15×10^{-3} mTorr disilane partial gas pressure as plotted in red. For nanowires grown at even higher disilane partial pressure to 25×10^{-3} mTorr, the main peak shift is even larger to 493.62 cm^{-1} as shown in Raman green.

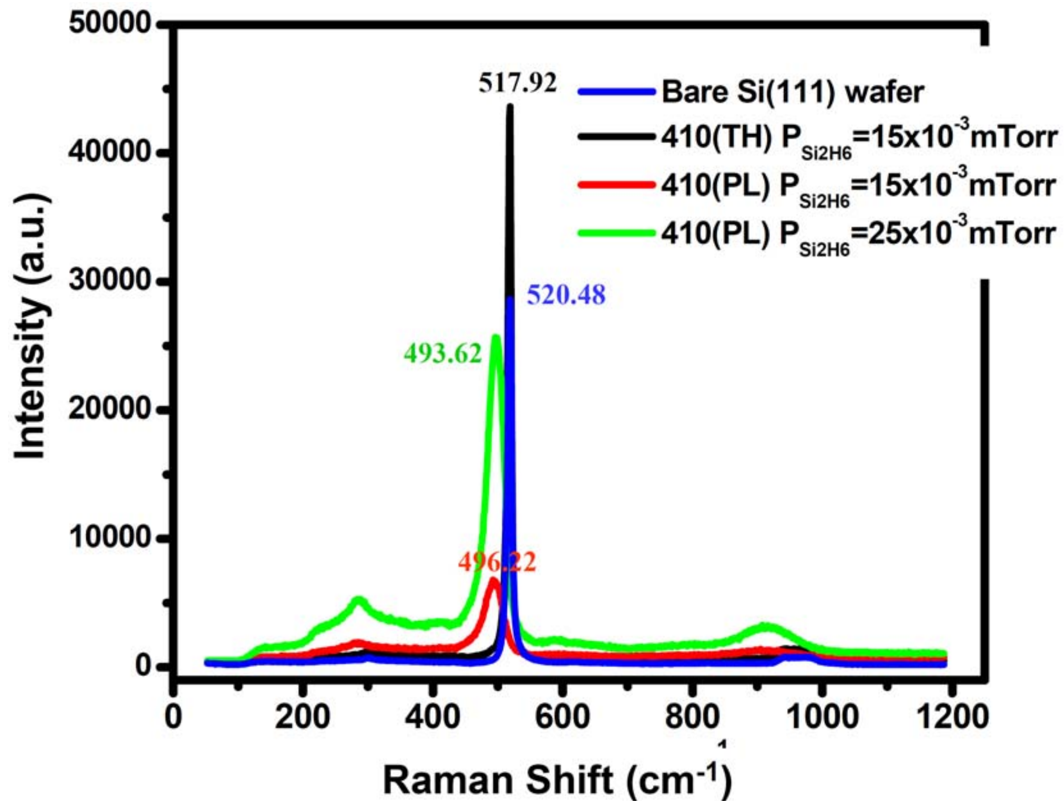


Figure 4.9 Raman Spectrum of the Bare Si (111) Wafer, Si nanowires thermally grown at 410°C with $15x10^{-3}$ mTorr disilane partial gas pressure, Si nanowires at 410°C by plasma-enhanced growth with $15x10^{-3}$ mTorr, and $25x10^{-3}$ mTorr disilane partial gas pressure.

Another appropriate characteristic for comparison is the full peak width at half maximum (FWHM) of the main Raman peaks for all samples. Generally, the intensity becomes broader with increasing disilane partial pressure for Si nanowires growth under plasma condition compared to a bare Si (111) wafer and thermally grown Si nanowires. Table 4.1 gives the details of the peak positions and peak widths.

The reason for the shifts and increasing widths of the main Raman peaks can be associated with the disorder and size effect that accompanies phonon confinement.[50] There has been significant research on the Raman spectroscopy of solid silicon as it is affected by the degree of crystallinity and particle/grain size. The main Raman band at 521 cm^{-1} corresponds to pure crystalline silicon in bulk form, and is also relatively narrow. At the other extreme of amorphous silicon, the main band appears at 480 cm^{-1} and is quite broad.[51, 52] Thus, in applying this to the Raman spectrum of curved nanowires, it can be conclude that the silicon in the nanowires themselves are nanocrystalline and highly disordered. The degree to which this happens clearly can be associated with the curvature and, in turn, the growth conditions. TEM studies report in Chapter 6 clearly confirm these observations, where it is that smaller nanocrystalline domains are a characteristic of the convex side of the nanowire, where it must grow fastest compared to the concave side. Therefore, the wires showing the greatest curvature and thickness would be expected to exhibit the highly disordered smaller nanocrystalline and, thereby, the greatest Raman peak shift and width. Thus, we can confirm that the nanowires grown at low temperature plasma conditions and under $25x10^{-3}$ mTorr disilane partial pressure will exhibit the greatest curvature.

Growth Condition	Si (111) bare wafer	410°C Thermal P_{Si2H6} = $15X10^{-3}$ mTorr	410°C Plasma P_{Si2H6} = $15X10^{-3}$ mTorr	410°C Plasma P_{Si2H6} = $25X10^{-3}$ mTorr
Nano-structure	-	VLS NWs (short length)	Semi-curly (short length)	Semi-curly (thick & medium length)
Peak Position	520.48	517.92	496.22	493.62
Peak Height	-	15634	1495.7	4927.3
FWHM	4.7	6.40393	25.726	29.216

Table 4.1 Summary of Measured Raman Spectrum Data

4.6 Conclusion

To characterize Si nanowires grown at low temperature, syntheses were performed by thermal and plasma enhanced CVD methods. Morphological differences of the nanowires were studied and compared in terms of their diameter, length, growth directions, density, and distribution. Under plasma-enhanced conditions, nanowires grew thicker, longer, and denser than thermally grown nanowires. Moreover, the nanowires tended to grow in a bent configuration, whereas nanowires grow linearly when thermally grown.

The characteristic of nanowires growing in bent, or curved, configurations was studied as a function of growth conditions, namely, disilane partial gas pressure under low temperature plasma conditions. As increase disilane partial pressure, more nanowires with greater curvatures (smaller radii of curvatures) were observed. The associated bending morphology was measured by both

geometrical measurement and Raman spectroscopy. In general, the greater the curvature was associated with the highly disordered smaller nanocrystallines. This was correlated with the growth conditions. In effect, the faster the growth rate under plasma-enhanced growth conditions, the nanowires were more curved and more strained. This correlated with higher disilane partial pressures and growth on Si (111), as opposed to growth on Si (100) at low disilane pressures. The mechanism for nanowires bending is discussed in Chapter 5.

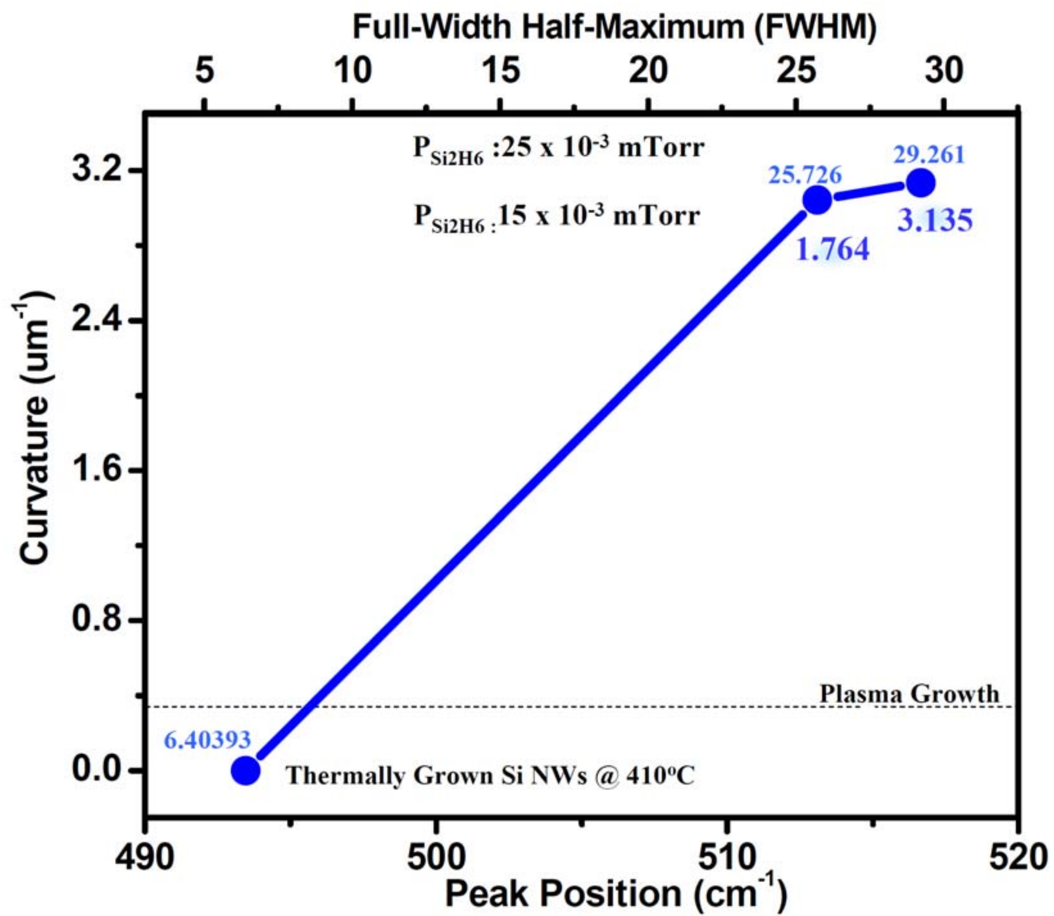


Figure 4.10 Correlations of Geometrically Measured Curvature and Raman Spectrum in Bending Nanowires Grown under Different Disilane Partial Pressures.

Chapter 5

Bending Mechanism of Si Nanowires Grown at Low Temperature

Based on the vapor-liquid-solid (VLS) mechanism, Si nanowires grow linearly underneath catalyzed Au nanodots that float on the top of the nanowire tip. Such morphologies are mostly seen for thermally grown Si nanowires at high temperature[11] and at low temperatures under conditions as discussed in Section 4.1. Plasma-enhanced Si nanowires at high temperature[10] also exhibit linear morphologies, although, as discussed in Section 4.2, bending is routinely observed for plasma-enhanced CVD at low temperatures (410°C) using disilane as a silicon source. To understand the bending mechanism, a three-step growth protocol was selectively performed to elucidate different aspects of the process. This involved manipulating the exposure time to a disilane plasma and examining the resulting wire morphology. A hypothesis was proposed and examined to explain the bending mechanism.

5.1 General Approach for Strain-Induced Bending Mechanism

In general, bulk silicon is brittle at relatively low temperatures due to its high energy for nucleating dislocations and its high Peierls stress for activating dislocation motion. Only at an appreciable fraction of its melting point can dislocations be activated and silicon can exhibit some level of ductility. The temperature necessary for triggering plasticity in bulk Si under stress is at least

400 °C.[53] For very fine silicon particles, the defect-free structure normally found is very resistant to fracture, requiring a high critical resolved shear stress to initiate dislocation motion. The fracture and deformation character are often significantly different from their bulk. In this study, we discovered that Si nanowires are bent during growth under low temperature plasma-stimulated conditions. Unlike VLS mechanism under purely thermal conditions, Si nanowires appear to naturally grow as curves in plasma for certain conditions.[54]

Compared to conventional VLS, a schematic of plasma grown Si nanowires is shown in Figure 5.1 (a). Bending can be explained by a differential growth rate, where growth is faster on one side of the nanowire compared to the diametrically opposite position. The driving force, however, is unclear. One explanation might be associated with a lateral stress acting on the nanowire tip and perhaps between nanowires.[55] Both electrostatic or Van der Waals forces might reasonably be suspected.[56-58] With respect to electrostatic forces that might arise in a plasma, the Debye length in a glow discharge should be at least on the order of 100 μm or greater, and the nanowires are located well within the high-field space of the discharge. Consequently, a significant electrostatic attractive force is exerted on the nanowires. The electrostatic attractive force (F) in Figure 5.1 (b) produces a tensile stress where the growth rate is faster, and correspondingly, a compressive stress is applied where the growth rate is slower.[56, 58]

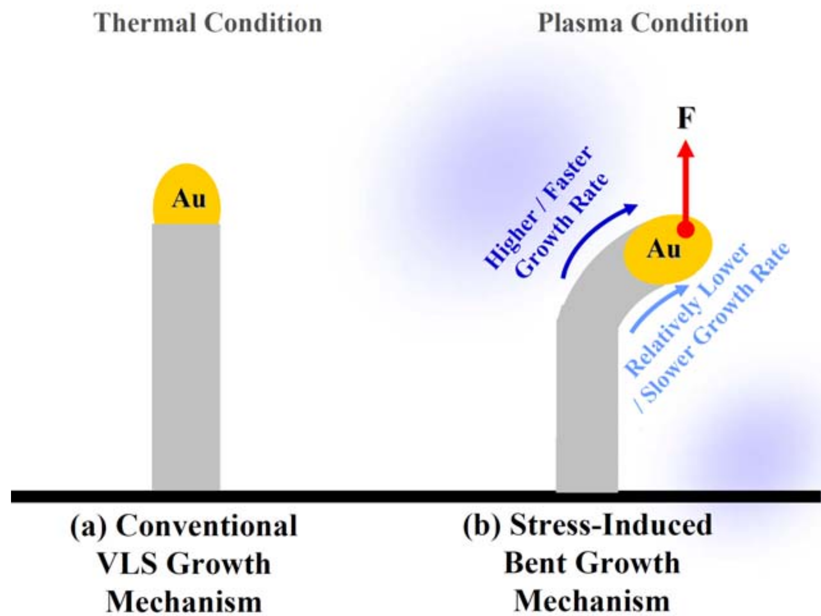


Figure 5.1 Different Growth Mechanism for Si Nanowires (a) Conventional VLS Growth Mechanism (b) Stress-Induced Bent Growth Mechanism

5.2 Disilane Plasma Effect on Si Bending Nanostructure

In the previous chapter, we confirmed that nanowire bending occured only under plasma-stimulated conditions at low temperature, and especially when disilane was involved as the silicon source. The effect was experimentally investigated using a three-step growth process as shown in Figure 5.2. After a preanneal treatment at 590˚C, the Si nanowires were thermally grown at 470˚C. Next, the nanowires were exposed to a hydrogen plasma for 5 minutes at 410˚C, followed with exposure to a disilane plasma at 410˚C. Both hydrogen and disilane plasmas were generated by 2.3 W rf power. The time of exposure in the latter step was varied between 10, 40, and 150 seconds as shown. The resulting growth morphologies are shown in Figure 5.2 (b), (c), and (d), respectively.

Thermally grown Si nanostructures at 470˚C, after only the hydrogen plasma treatment (step 2), are shown in Figure 5.3 (a) plan view and (e) cross-sectional view. The nanowires appear straight and very fine as is characteristic of thermally grown wires. On the other hand, the sequence of exposure to hydrogen plasma with disilane reveals a rather rapid and dramatic change. After a 10 second exposure (Figure 5.3 (b) and (f)), a thickening and more obvious curving is beginning to appear at the tips. Lengthening is apparent, indicating that the VLS mechanism is still acting even in the absence of an external silicon source.

Mechanism of Nanostructure Transformation

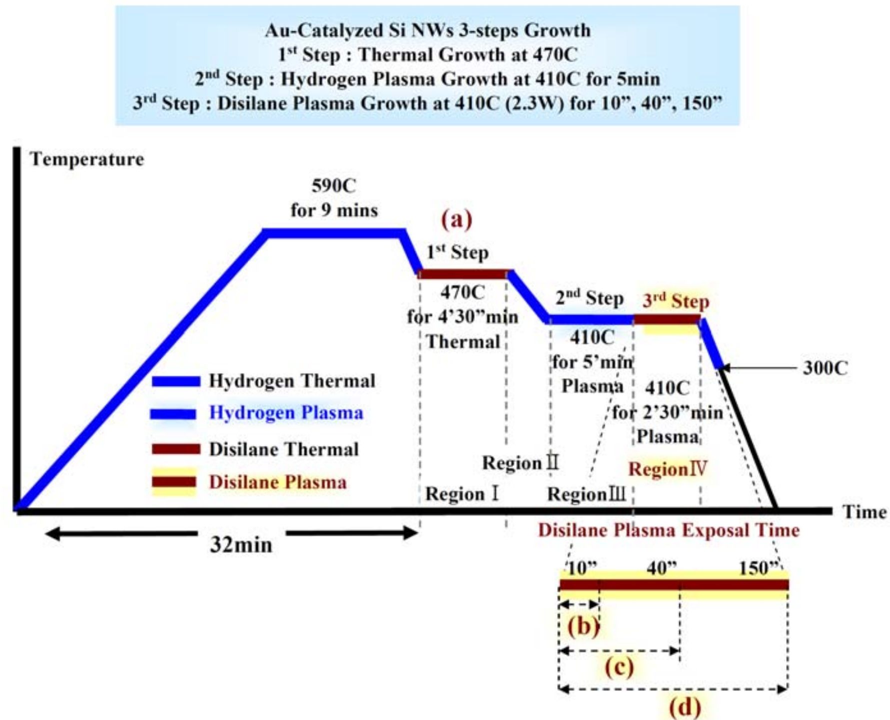


Figure 5.2 Experimental Approaches for Bending Nanostructure

After 40 seconds plasma anneal, more distinct bending is observed [Figure 5.3 (c) plan view and (g) cross-sectional view]. Nanowire bending starts more from the middle of the nanowires in this case compared to the shorter times. This behavior can be explained by the irregularity of the individual nanowires as well as van der Waals attraction between nanowires. According to the typical formation mechanism of Si nanowires reported[57], if the shape of nanowires is irregular, the centre of gravity of each individual nanowire is not aligned with those of other nanowires.[58]

For longer, 150 second, exposures to a disilane plasma, the longer nanowires appear to be significantly bent, curving in a semicircle and back towards the substrate. Eventually this leads to entanglement and matting of nanowires as their lengths become too long as shown in Figure 5.3 (d) and (h). The density of the Si nanowires is also quite high.

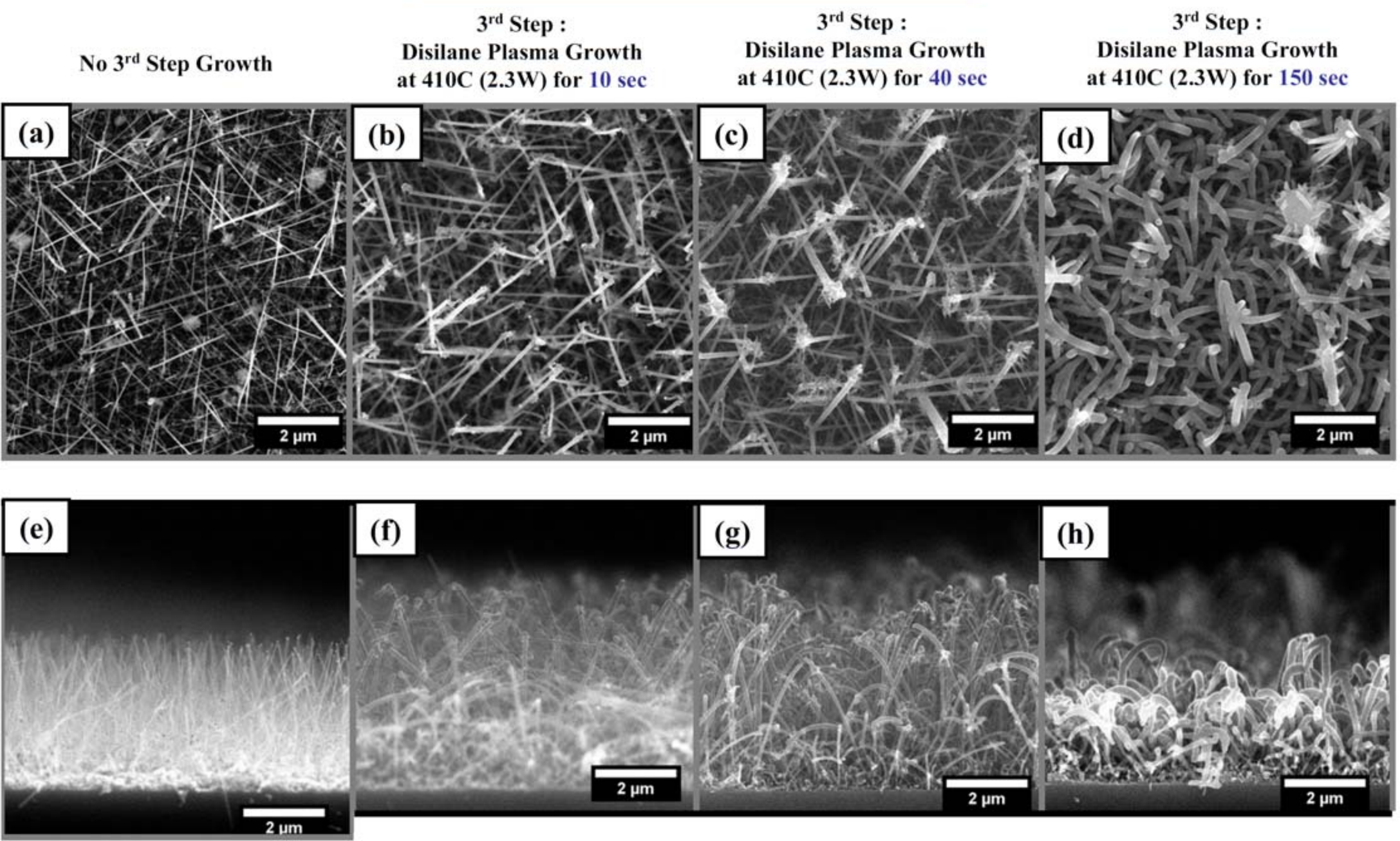


Figure 5.3 Effect of Disilane Plasma on Si Nanowires' Morphology

5.3 Kinetic Approach for Bending Mechanism

Based on the experimental results just described, an hypothesis of the bending mechanism can be formulated based upon differential growth kinetics at different surface locations dependent on the degree of exposure to the plasma. Figure 5.4 presents a schematic describing this model. The starting points for all experiments just before the application of the plasma were the thermally grown Si nanowires on Si (111) wafer. The nanowires had either of two dominant growth directions relative to the substrate, namely, <111> and <110>.

When exposed to the disilane plasma stage at 410°C, the surfaces of the nanowires grown in the <110> direction are unevenly exposed to disilane plasma on all sides, unlike Si nanowire starting in the <111> growth direction. In other words, the outer surface of a <110> nanowire is more exposed to the disilane plasma relative to inner surface facing the substrate surface [Figure 5.4 (a)]. Because an <110> nanowire is unequally influenced by plasma on all sides, the diffusion of gold along the same surfaces are uneven due to a difference in the line-of-sight bombardment by the plasma electrons. This means gold surface diffusion at outer side is more accelerated and more heavily distributed [Figure 5.4 (b)]. In turn, a faster deposition reaction occurs at the outer wall rather than inner wall [Figure 5.4 (c)]. Thus, a differential growth deposition rate between outer and inner walls induces curving.

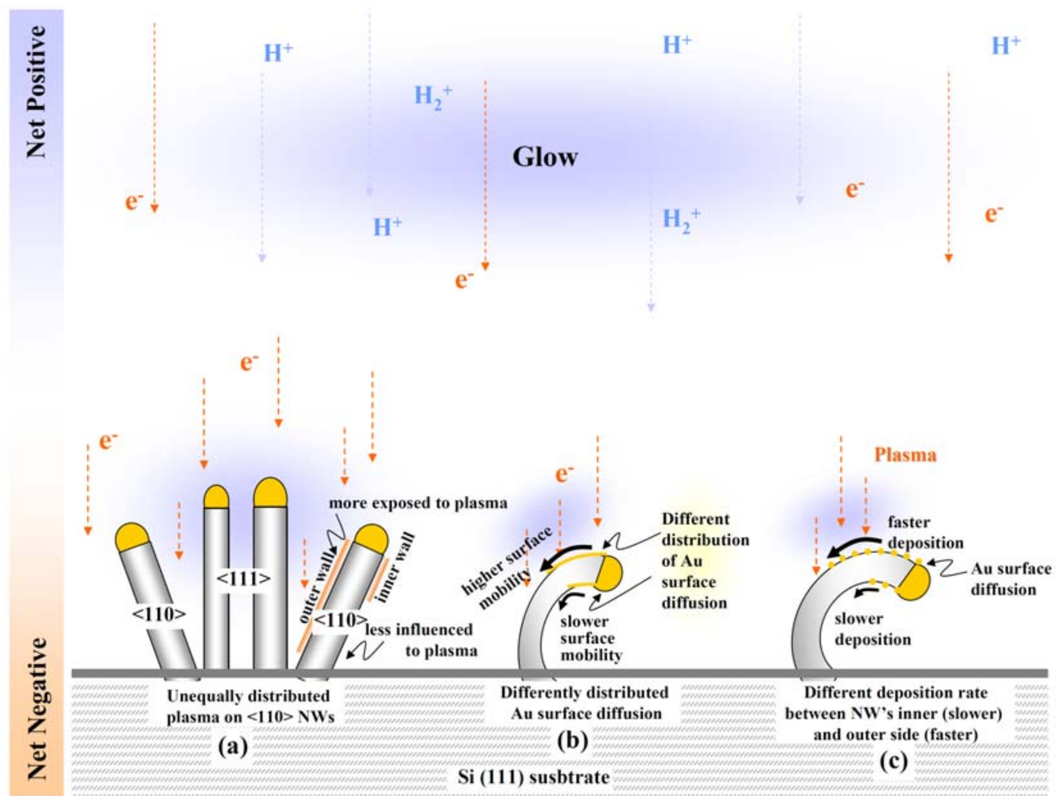


Figure 5.4 Schematic of a hypothesis for a differential deposition kinetic mechanism for explaining curved nanowire growth in a hydrogen-disilane plasma.

5.4 Conclusion

For low temperature growth conditions, Si nanowires grown in a hydrogen-disilane plasma tended to curve during growth near the Au bead at the nanowire tip. A three-step growth process was used to elucidate some of the growth details. Nanowires exposed longer to disilane plasmas at 410°C, tended to be more bent.

To explain the process, a hypothesis was formulated whereby the nanowires curved due to differential growth rates at diametrically opposite sides of the nanowires. At those surfaces more openly exposed to the plasma, the growth rate tended to be faster than the surfaces that were more in the shadow of the nanowire. It was also hypothesized that the surfaces where the growth rates were greatest also possessed more surface gold that had diffused out from the gold bead tip due to greater stimulation of surface mobility due to plasma particle bombardment.

A secondary hypothesis was discussed that raised the prospect of electrostatics and Van der Waals forces acting on the nanowire tips to accelerate bending during growth.[57, 58] When nanowires are exposed to a hydrogen-disilane plasma, the Au beads become more negative charged than the plasma itself and quite possibly more negative than the silicon substrate [as shown in Figure 5.5 (a)]. A repulsive force arises between adjacent Au beads [Figure 5.5 (b)]. Once bend begins, nanowire tip is increasingly attracted to substrate surface [Figure 5.5 (c)].

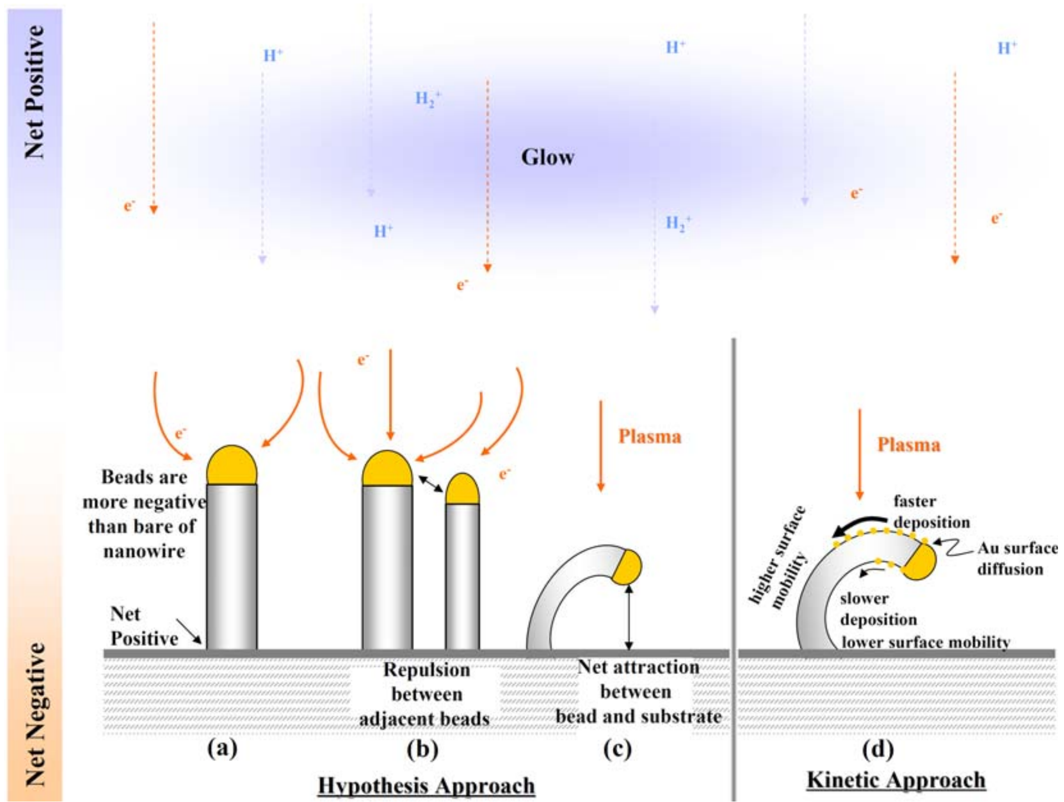


Figure 5.5 Hypothesis (a, b, & c) and Kinetic Approach (d) for Bending Mechanism

Chapter 6

Effect of Disilane Plasma on Nanowire Branching

6.1 Introduction to Branching Nanostructures

Controlling the branching of silicon nanowires as they grow presents an opportunity to construct *in-situ* networks of silicon devices that already have inter-connections in place. The higher complexity of such structures increases the potential for new applications by increasing the number of connection points and providing parallel connectivity to functional elements.[59] For this project, a survey of the experimental conditions leading to branching was undertaken, with the purpose of directing new studies that world focus on identifying a mechanism that could selectively trigger and suppress branching.[60]

The observation of homo- and hetero-branching and multibranching nanowire structures has been demonstrated by various methods, introducing the possibility of fabricating hierarchical nanostructures of increased complexity and functionality.[59, 61] Up to now, most strategies for inducing branching involve a second seeding step to place metal catalyst particles on to the primary nanowire ‘‘trunk’’. Generally, this involves removing the initial structure from the growth reactor in order to deposit the secondary catalyst before returning to the reactor.[59-63] In this chapter, we present an alternative approach where branching is done *in situ*, facilitated by the interaction of the plasma with the liquid Au–Si alloy. In effect, the plasma influences surface migration of the alloy during disilane plasma

growth. The result is the fabrication of densely branched Si nanowires. A modest degree of control is demonstrated in branching from primary to secondary nanowire without the need for *ex situ* seeding.

The conditions for branching and systematic trends in branch morphology are described here for the low temperature growth of silicon nanowires under thermal and RF plasma activation. Silicon nanowire branching is thought to be facilitated by the surface migration of liquid Au-Si alloy catalyst from the nanowire tips.[62]

6.2 Branching Nanowire Morphologies

Gold films, 2 nm thick were thermally evaporated onto hydrogen terminated Si (111) substrates in a thermal evaporator. The primary silicon nanowires were thermally grown in a low pressure chemical vapor deposition (LP-CVD) system by the catalytic vapor-liquid-solid (VLS) technique using 9.267% disilane (Si_2H_6) diluted in hydrogen (H_2) at 470°C. The secondary and tertiary silicon nanowires were synthesized by disilane plasma-stimulated chemical vapor deposition (PE-CVD) at 410°C, using RF plasma powers of 1.5 W, 2.6 W, and 3.5 W at a frequency of 13.56 MHz.

In our method, the primary nanowire trunks have grown first under large diameter growth conditions and at relatively high temperatures. Without breaking vacuum, the growth conditions were then changed within the same run to a low temperature so as to favor the growth of smaller diameter nanowires off the walls of the primary nanowires. It is assumed that the gold diffused from the tips along

the trunk sidewalls due to plasma enhanced mobility. This then facilitated branching.

Figures 6.1 (a) and (b) show typical FE-SEM plan and cross-sectional views of the branching grown under a 1.5 W plasma. The primary nanowire grows from bottom-to-top almost linearly. Secondary branching grows with six to eight long thin arms sprouting from the top of the primary nanowire in all directions. These branches typically curved slightly downward as they grew. The primary nanowire's length is 6.13 μm and the diameter is 189 nm. The branches are typically 1.3 μm in length and 121 nm in diameter.

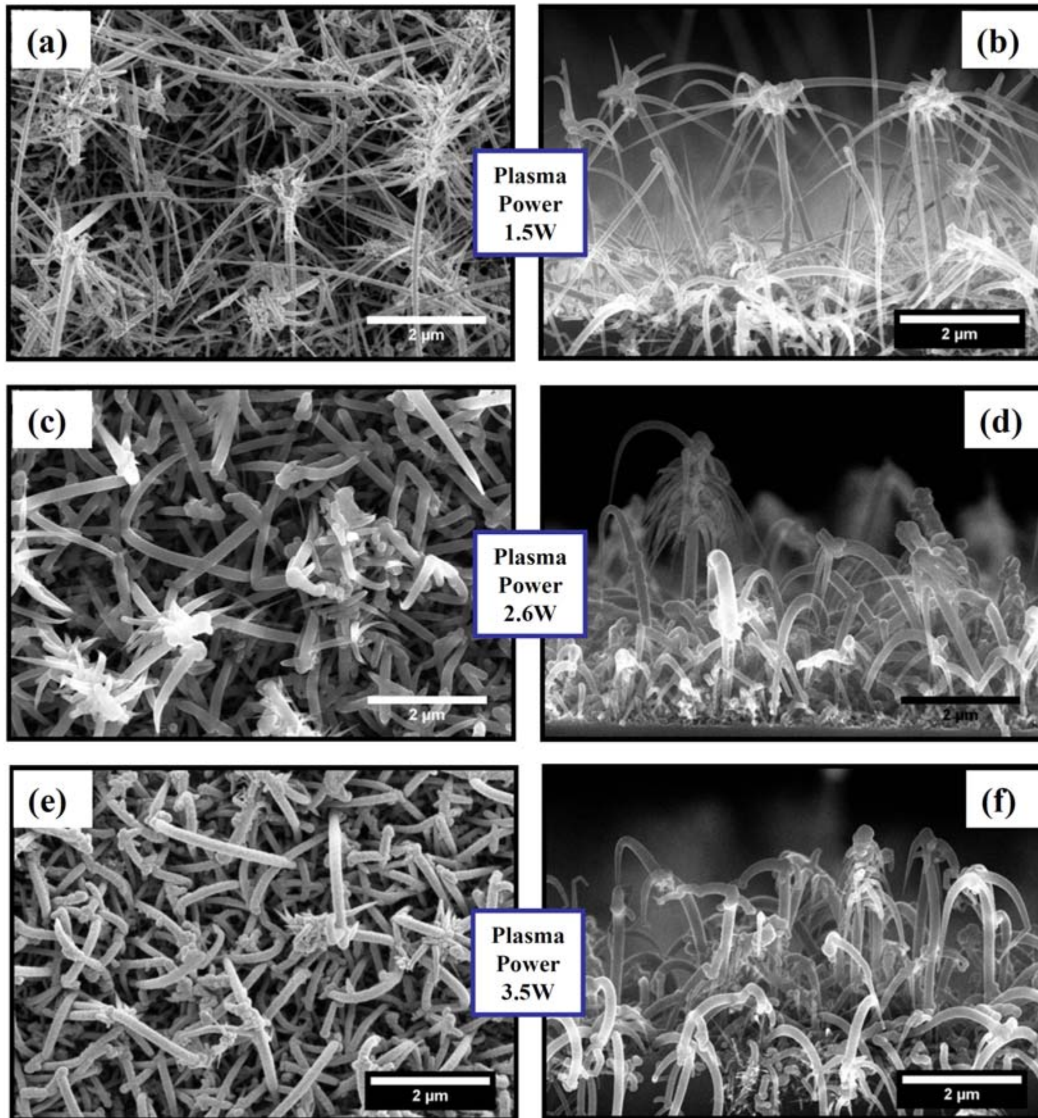


Figure 6.1 FE-SEM images of branching nanowires (a) plan view, and (b) cross-sectional views grown under a plasma power of 1.5 W; (c) plan view, and (d) cross-sectional views grown under a plasma power of 2.6 W; (e) plan view, and (f) cross-sectional views grown under a plasma power of 3.5 W

Many branches exhibit a metal bead at their tips indicative of VLS growth. At a larger plasma power of 2.6 W, the primary nanowire itself curves down toward the substrate as it grows [Figure 6.1 (c) and (d)]. The nanowire has a 136 μm diameter and 0.7 μm length. Compared to the 1.5 W, the branching diameters are thicker and the lengths are shorter. Unlike, the branching structures at 1.5 W, the catalyst at the tips for the 2.5 W nanowires are mostly invisible. FE-SEM images in Figure 6.1 suggest that the gold from the Au-Si bead migrates possibly over the nanowire surface, distributing as an invisible layer. At the highest plasma power of 3.5 W, the primary nanowire trunk bends even more as shown in Figure 6.1 (e) and (f). The branches tend to be thicker (154 nm diameter) and shorter (0.2 μm length) than either prior experiment.

In Figure 6.2, the diameters and length of the nanowire branches are plotted as a function of plasma power. The trend clearly shows that increasing plasma power produces shorter but thicker nanowires. The highest power shows branching to produce only stubs, whereas the long and slender branches are seen at the lowest power. Increasing the plasma power also affects the density of branches. Effectively, it decreases from 62 counts of branching nanowires under 1.5 W plasma power to 7 counts per 447 μm^2 (that was the field of view) under 3.5 W plasma power [Figure 6.3].

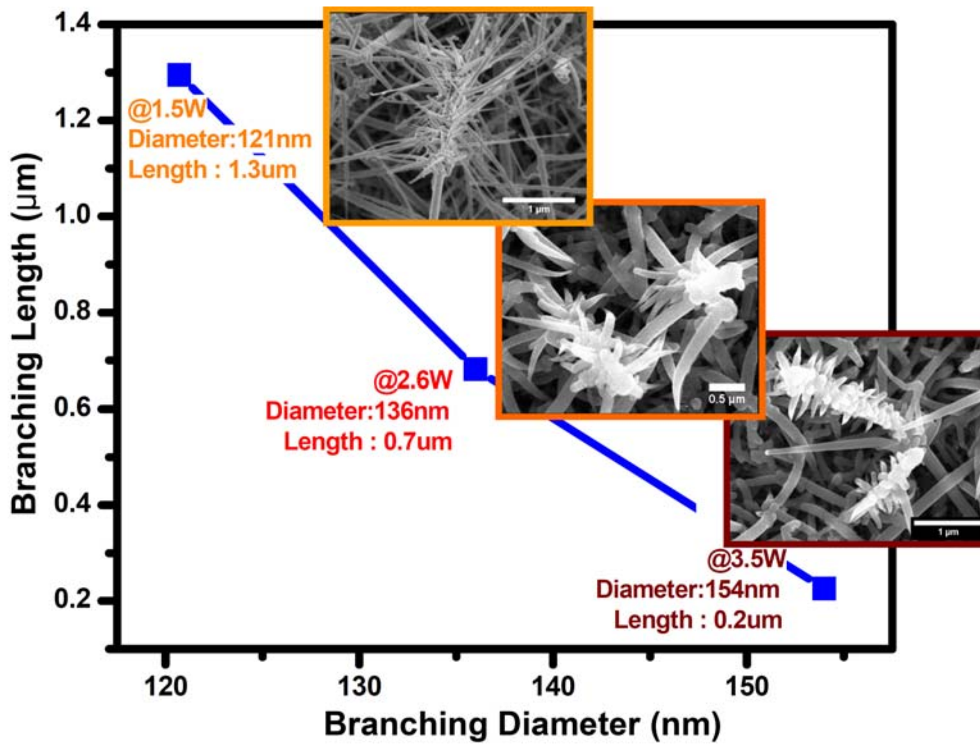


Figure 6.2 Branch Diameters and Lengths with Plasma Power

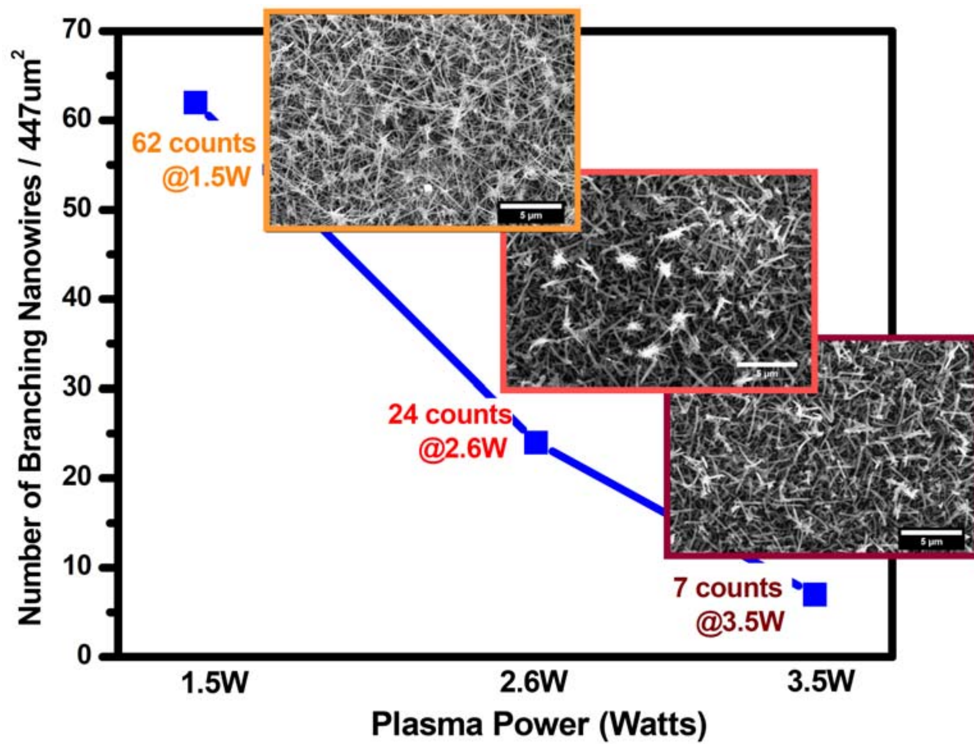


Figure 6.3 Density of Branches as a function of Plasma Power

6.3 Influence of Au Diffusion on Nanowire Branching

The branching of nanowires during growth can be explained by the gold catalyst diffusing along the silicon surface. For the growth step at 470°C [Region Ⅰ of the temperature profile in Figure 6.4], the gold catalyst remains at the tip of the nanowires. This is shown in micrographs at the bottom of Figure 6.4 including (a) a plan view of the nanowire morphology and (c) a cross-sectional view. When the disilane source has been stopped after the thermal growth step, the temperature is cooled corresponding to RegionⅡ. At this point, different processes can happen: (i) the nanowires continue to grow by decomposing residual disilane, and growth also occurs by coarsening processes, incorporating residual excess Si present in the catalyst; (ii) gold from the catalyst begins diffusing over the surface of the nanowires; and, (iii) gold forms critical single-clusters at the same surfaces. The average coverage of gold is assumed to approximate one monolayer, however, it is thought that gold clusters form as the temperature decreases further.[45, 62, 64-66]

Assuming this to be the case, it has the potential to nucleate nanowire that branches outward, consistent with what was observed only at the lower temperatures. Thus, when there is source of gold alloy, the model assumes that gold migrates down the nanowire sidewalls and recrystallizes into smaller seed crystals at the lowest temperatures.

Subsequently, branching is initiated when disilane is again introduced under plasma conditions at 410°C [Region Ⅲ in Figure 6.4]. The effect of disilane

plasma at low temperature drives the structural changes that are now familiar, namely, increased branching, thickening diameter, lengthening diameters, and accelerating gold diffusion.

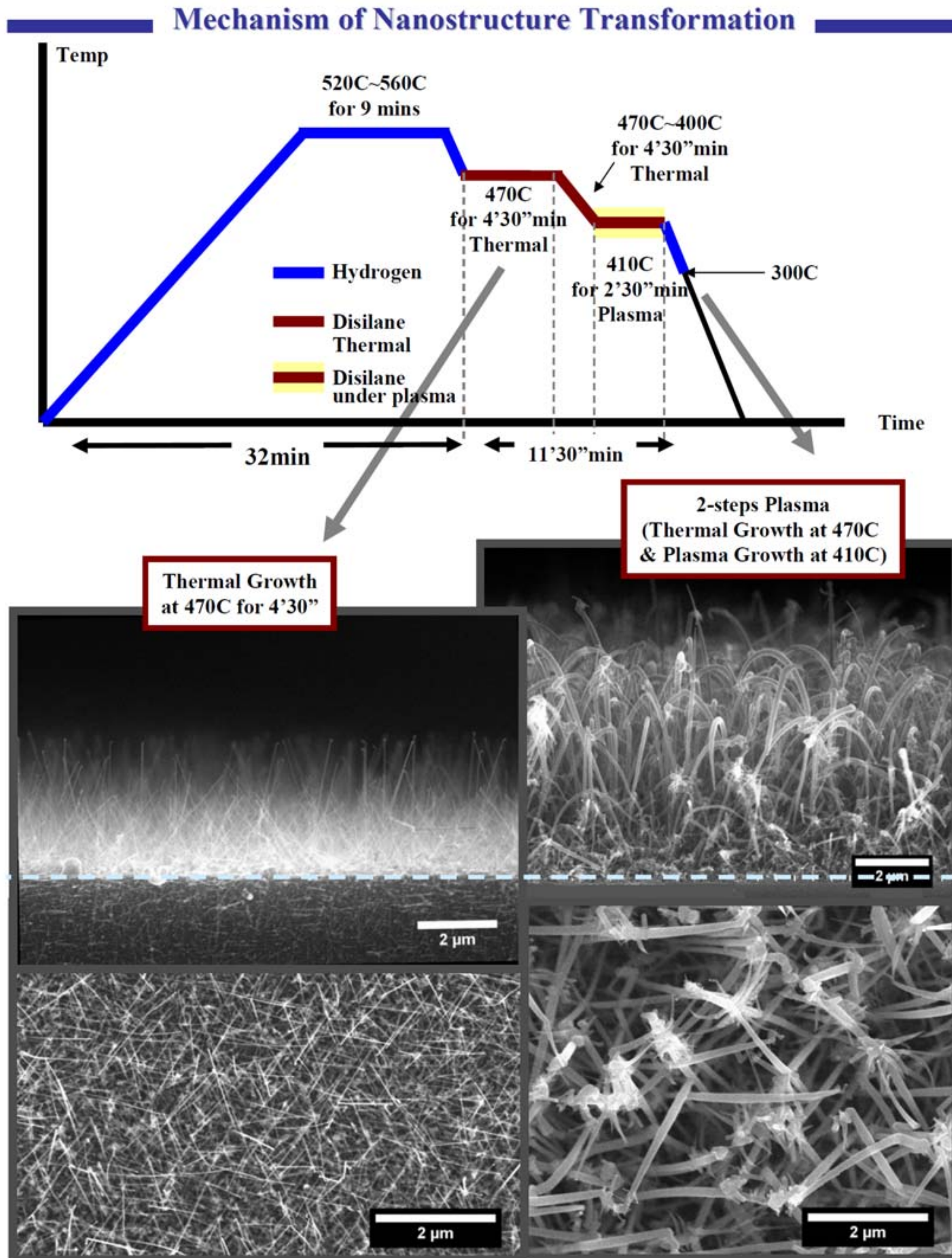


Figure 6.4 Thermal sequence and microstructure evolution leading to branching.

6.4 Size Effects on Branching Nanowires Induced by Different Plasma Power

The crystallinity of the branching nanowires was studied by Raman spectroscopy using 532 nm primary laser radiation. Figure 6.5 shows the Raman spectrum of a Si (111) wafer without Si nanowires, with Si nanowires thermally grown at 470°C, and with silicon nanowires grown under different plasma powers (1.5 W, 2.6 W, and 3.5 W). There is a very strong match in the primary peaks for bulk Si (111) wafer and thermally grown nanowires, which are predominantly straight. The primary peak for bulk Si (111) centers on the 519.73 cm^{-1} phonon band. The same peak for thermally grown Si nanowires is only slightly shifted to 518.86 cm^{-1} which is presumably due to a small size effect due to the narrow cylindrical radius.[29, 38, 67]

All plasma grown samples exhibited downshifted resonances relative to bulk Si (111) and thermally grown Si nanowires, as shown in Figure 6.5. The peak positions for 1.5 W, 2.6 W, and 3.5 W appeared at 501.51 cm^{-1}, 495.47 cm^{-1}, and 489.34 cm^{-1}, respectively. This trend agrees with the behavior shown in Figure 4.9 that correlated curvature with nanosize crystallinity. The peaks also show the asymmetric broadening in intensity. It is attributed to the different domain size distributions in branching nanostructure. As discussed in Chapter 4.5.3, the branch's peak position tends to downshift more when the branch structure becomes more amorphous-like nanostructure. A more detailed study of the the size distribution of nanocrystallines is described in next sectionon TEM characterization.

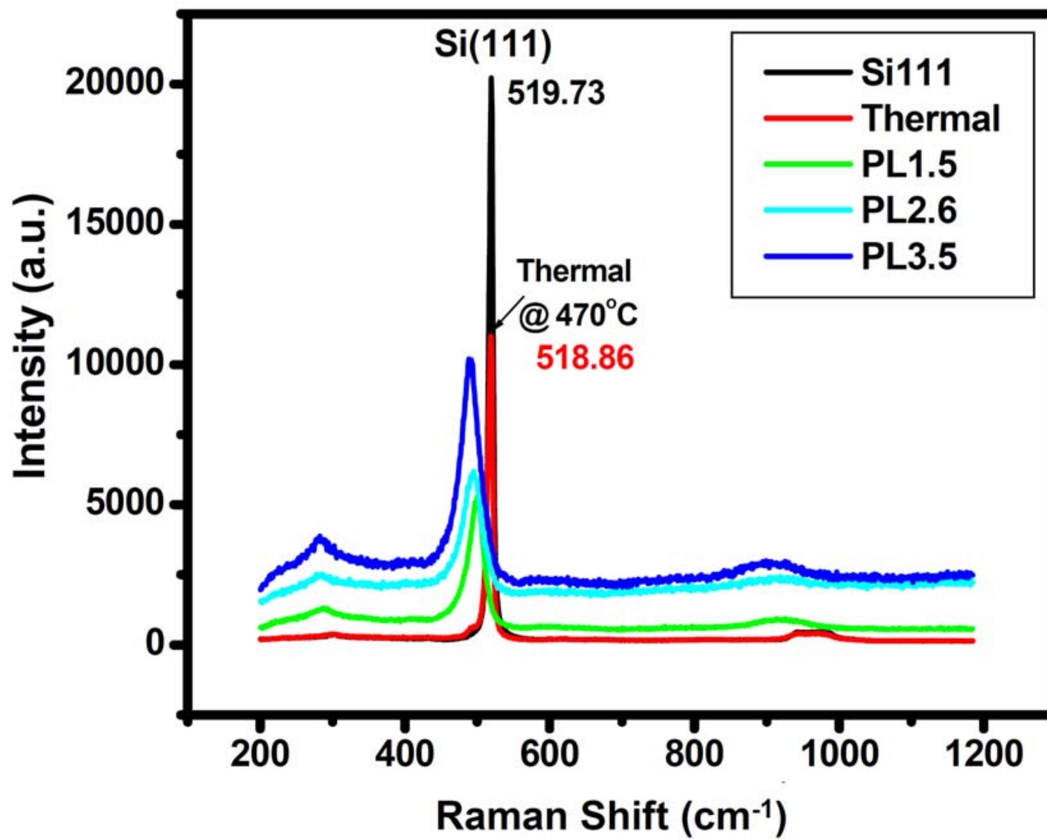


Figure 6.5 Comparison of Raman Spectra of a bare silicon (111) wafer without Si nanowires, 470°C thermally grown Si nanowires, and branching silicon nanowires grown at different plasma powers (1.5 W, 2.6 W, and 3.5 W).

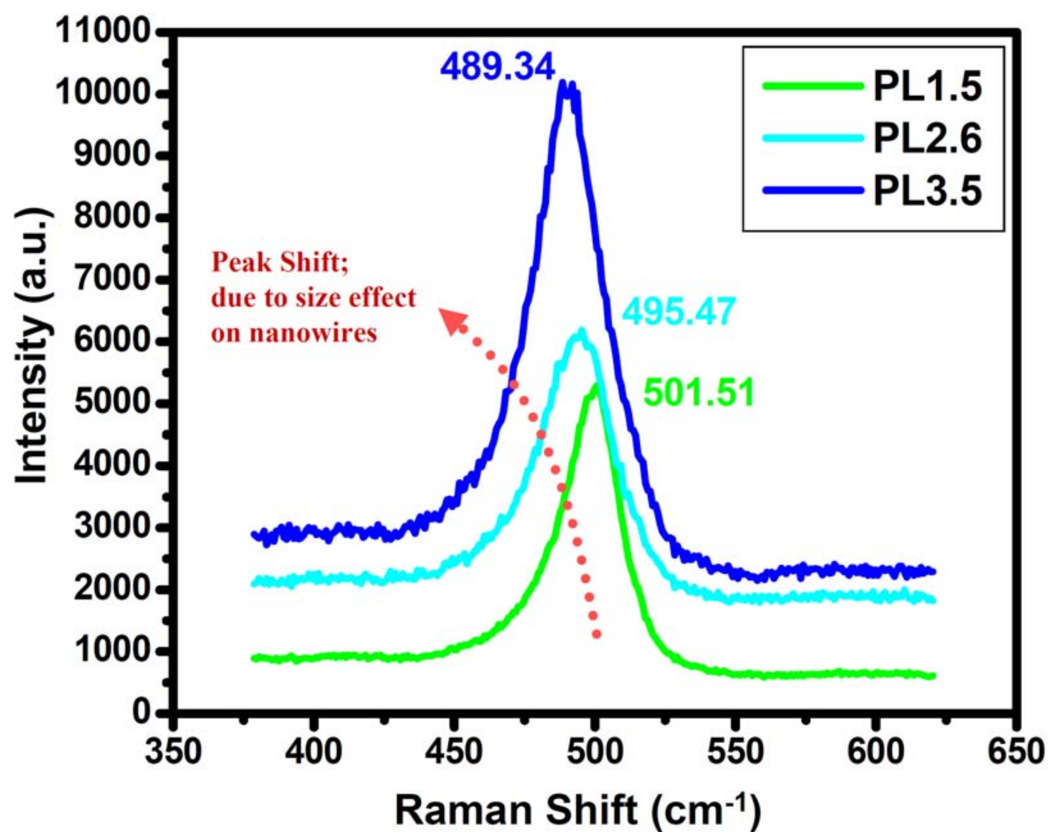


Figure 6.6 Shifting Raman peak positions of branching nanowires after growth under different plasma powers.

6.5 TEM Studies of Curved Nanowires and Branches

The structures of the primary nanowires and its branches were examined by transmission electron microscopy. Figure 6.7 shows a high-resolution (HR) composite image of a representative branching nanowire. It shows a low magnification image (a), and a high magnification image of a primary nanowire (b), and the junctions leading to a branching nanowire (c). In all cases, the polycrystalline nature of the nanowire is evident. Lattice imaging in various locations correspond to interplanar lattice spacing of 0.192 nm, 0.23 nm, 0.29 nm, 0.31 nm, and 0.38 nm for Si (220), (211), (111), and (110), respectively.[36] This confirms that the structure of both the primary nanowire and the branching nanowires are essentially polycrystalline.

It should also be emphasized that the branching occurs after the two-step growth process and supports the proposed mechanism. This is the migration of Au along the nanowire surface leads to the formation of small Au-Si particles on the sidewalls of the nanowires.[45, 64] These particles are distributed over the surface of the Si nanowires during intermediate cooling stage between the initial thermal and the plasma growth steps. However, Au-Si particles remain catalytically inactive due to insufficient supply of the Si source. Under the subsequent step of disilane plasma growth, branching occurs form these secondary gold seeds on the sidewalls of the primary nanowire.

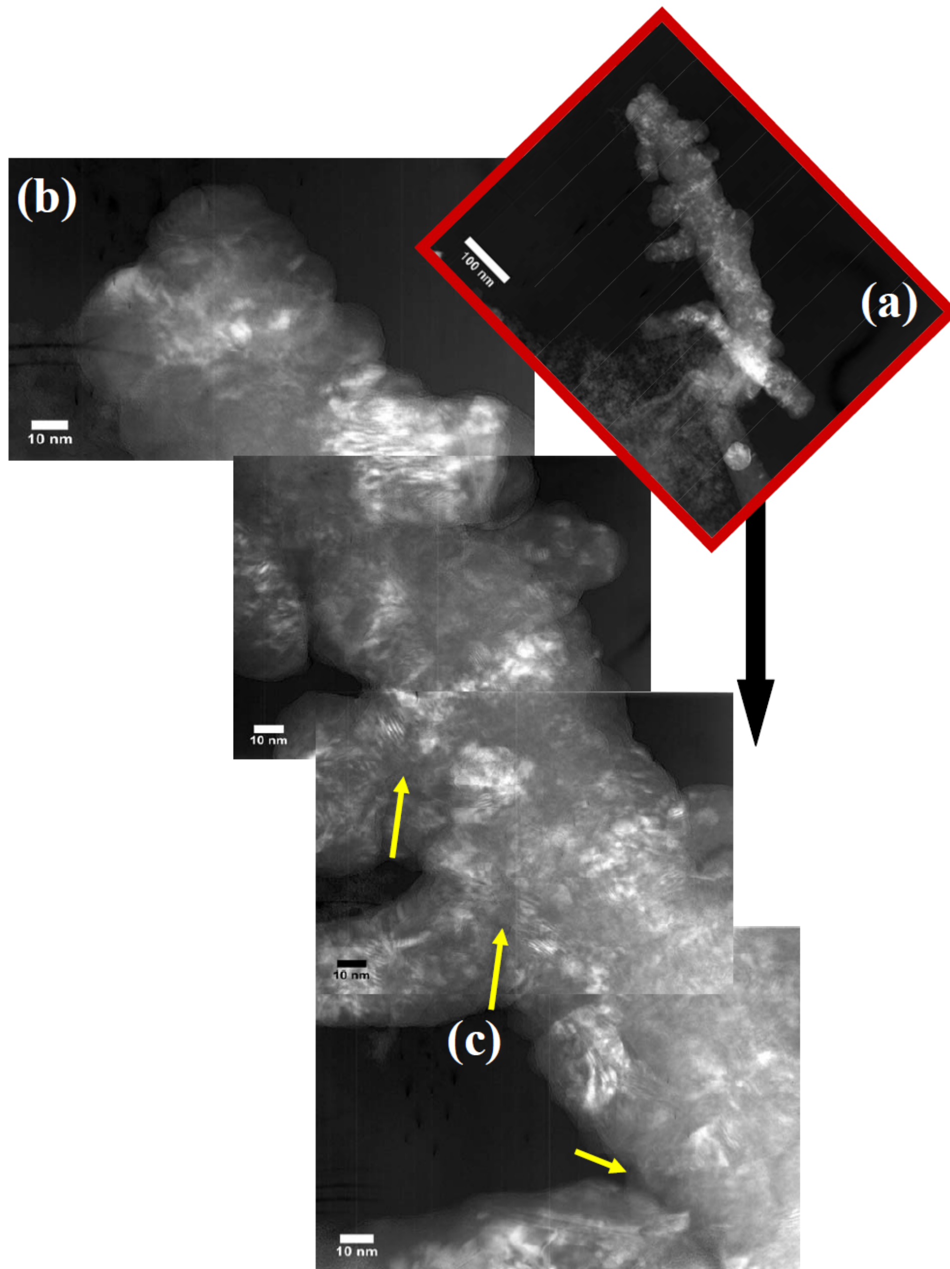


Figure 6.7 High-Resolution TEM Image of Branching Nanowires (a) Inset shows a low magnification image (b) High magnification of branching nanowires, and (c) the junction between the primary nanowire and a branching nanowire.

The curved nanostructure resulting from the two-step growth process is shown in Figure 6.8. As we discussed in Chapter 4.6, bending is mainly related to the strain in nanowire during its growth.[37, 68, 69] The diameter of the nanowire in Figure 6.8 varies along its length. In effect, it is thickest (112.74 nm) where the curvature is also greatest and thinnest (88.13 nm) near the gold tip where it is also relative straight. This is explained further by the structural analysis presented in Figure 6.9.

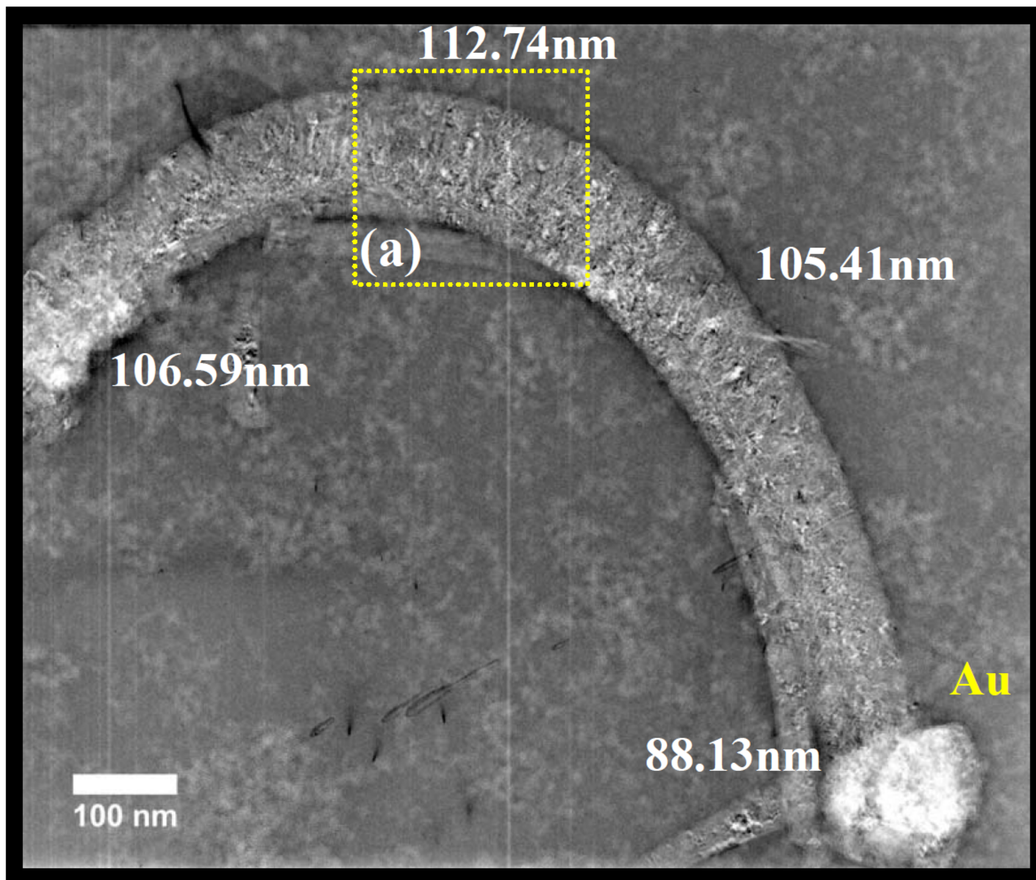


Figure 6.8 Dark-Field High-Resolution TEM (HRTEM) image of bending nanowire with gold on the tip. (Each number indicates the diameter at that

location.)

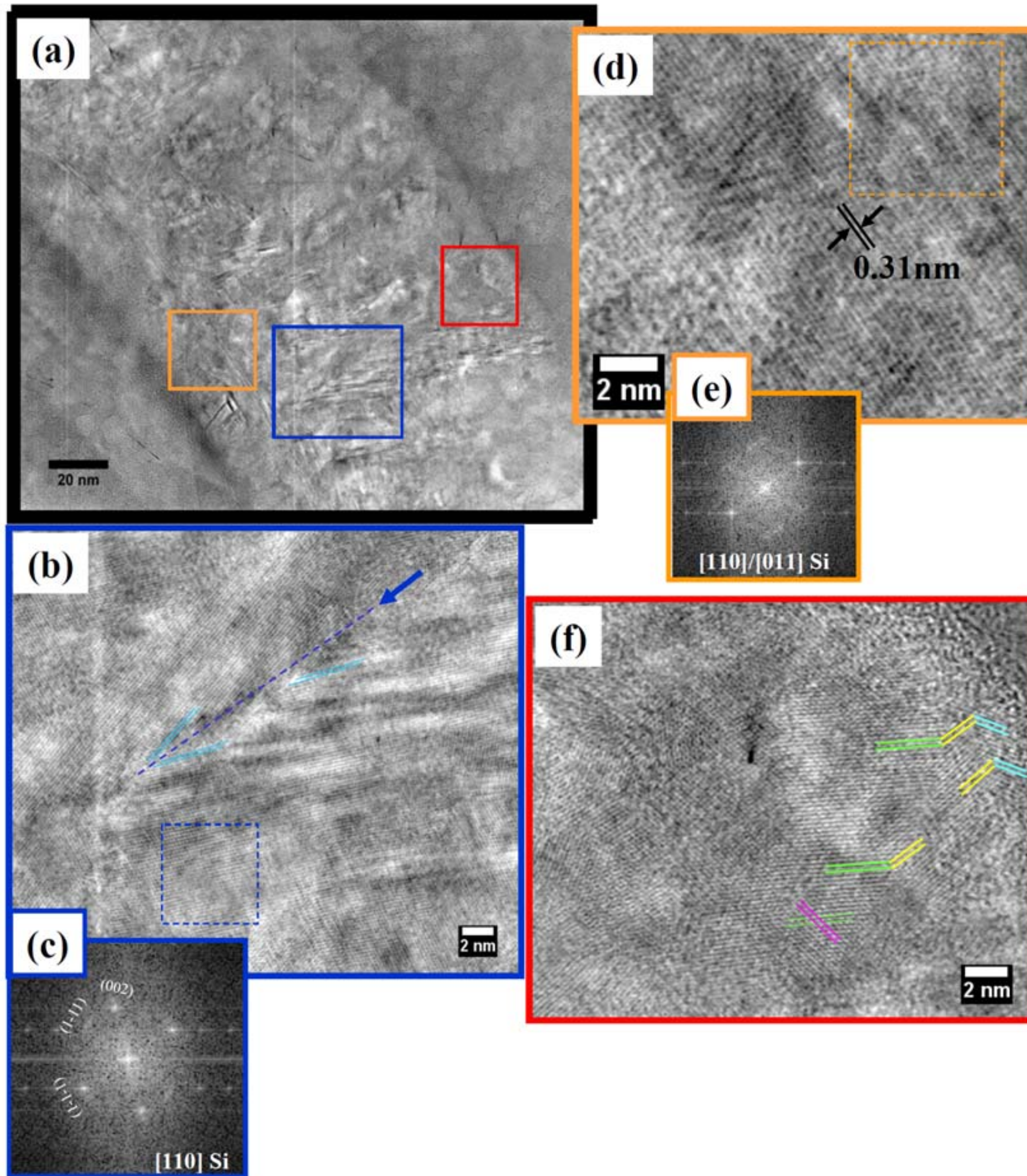


Figure 6.9 (a) HRTEM image of the high curvature region of the nanowire shown in Figure 6.8, (b) an even higher magnification image of middle region corresponding to the blue box in (a), (c) a power spectrum (fast Fourier transform,

FFT) of the blue dash box region in (b), (d) HRTEM image at bottom region of bending nanowire marked in orange box, (e) an FFT of the orange dash box region in (e), and (f) HRTEM image of top region of bending nanowire in red box of (a)

Figure 6.9 is a high resolution image of the nanowire in Figure 6.8. It provides a number of clues as to how the nanowire grew in the vicinity of the area of greatest curvature. A general characteristic of the bending nanowires is that they are thicker in diameter where they also have the greatest curvature. A detailed look at the top (convex) side of the nanowire the silicon is relatively, disordered and poorly crystalline. On the concave side, the silicon is still polycrystalline but comprises larger grains of well-defined lattice planes. These two sides represent the areas of greatest tensile and compressive strains, characteristic of plastic deformation in a wire while being bent.[48-50, 70]

At the axial center of the nanowire, Figure 6.9 (b) shows a twin plane, perpendicular to the axis, and the accommodating strain distortions that bridges the convex side that possesses the extra material and the concave side that has a relative deficiency of material. The power spectrum FFT (Figure 6.9 (c)) shows the growth direction along the [1-11], particularly in blue dash box. The twin boundary is marked by the blue arrow in Figure 6.9(b). Figure 6.9 (d) is shown the interplanar spacing of 0.31nm, corresponding to the Si (111) plane. The long periodic lattices/planes are observed at the region where the less intrinsic strain exists, which the less bending is occurred.

These observations indicate that the nanowire curved during growth due to relative differences in growth rates. On the outside of the curve, growth was more rapid than at the inside surface. The low crystallinity of the outside is believed to be due to the greater deposition rate and relatively little time for the crystal structure to reorganize and conform to the surrounding material. At the other side, the relatively slow growth rate allows more time for a stable microstructure to form. Here, crystallinity is better defined. Where the nanowire is thickest corresponds to where the greatest differential growth rate would occur, and hence, the greatest curvature.

6.6 Conclusion

The conditions for branching and branching morphology are described for the low temperature growth of silicon nanowires under thermal and RF plasma activation. Using a two-step growth process, the primary nanowire trunks were first made under large diameter growth conditions and at a relatively high temperature (470°C). Secondary and tertiary nanowire branching are observed and isolated for varying thermal and plasma power sequences.

Field emission SEM (FE-SEM) studies where used to determine the density, size and shapes of the branching nanostructures. The trend clearly shows that increasing plasma power produces shorter but thicker nanowires. In addition, increasing the plasma power also affects the density of branches, which decreases at higher plasma powers.

The nanocrystallinity of the branches was investigated by Raman

Spectroscopy and high-resolution TEM studies. From both characterizations, greater structural disorder in the form nanocrystallinity and even amorphous atom packing was observed for nanowires grown at higher plasma powers. The primary peak shift was shown in nanowires grown by higher plasma power supply. Branching structure was clearly shown in HR-TEM image, as well as, the curved nanostructure. In curved nanowire, the more curvature with thicker diameter was observed at the convex side relative to the concave side due to the highly disordered nanocrystallinity. Also, it was shown that the crystallinity also varied from very poor at the convex side to a more ordered and arranged polycrystalline structure at the concave side because of the differential growth rate (faster at convex and slower at concave). This observation explains previous observations reported in Chapter 5 concerning the bending mechanism.

Chapter 7

Post-annealing Effect on Si Nanowire Morphologies after Thermal Hydrogen and Plasma Hydrogen Treatments

7.1 Introduction

The effect of post-annealing treatment on Si nanowire structures was investigated by a two-step anneal process. For the first step, Si nanowires were thermally grown on Si (111) wafers at 470°C as seen in Figure 7.1(a). Next, the temperature was decreased to 410°C while in a pure hydrogen without disilane. The total gas pressure was maintained at 154 mTorr. Thermal post-annealing in hydrogen was conducted for between 5 and 15 minutes. A second series of experiments were conducted in a 2.3 W RF hydrogen plasma at different powers for the same range of times. The changes in nanowire morphologies were compared. The results confirm our previous observations that the phenomenon of curving nanowires is caused by the combination of plasma excitation and disilane, and not by either alone.

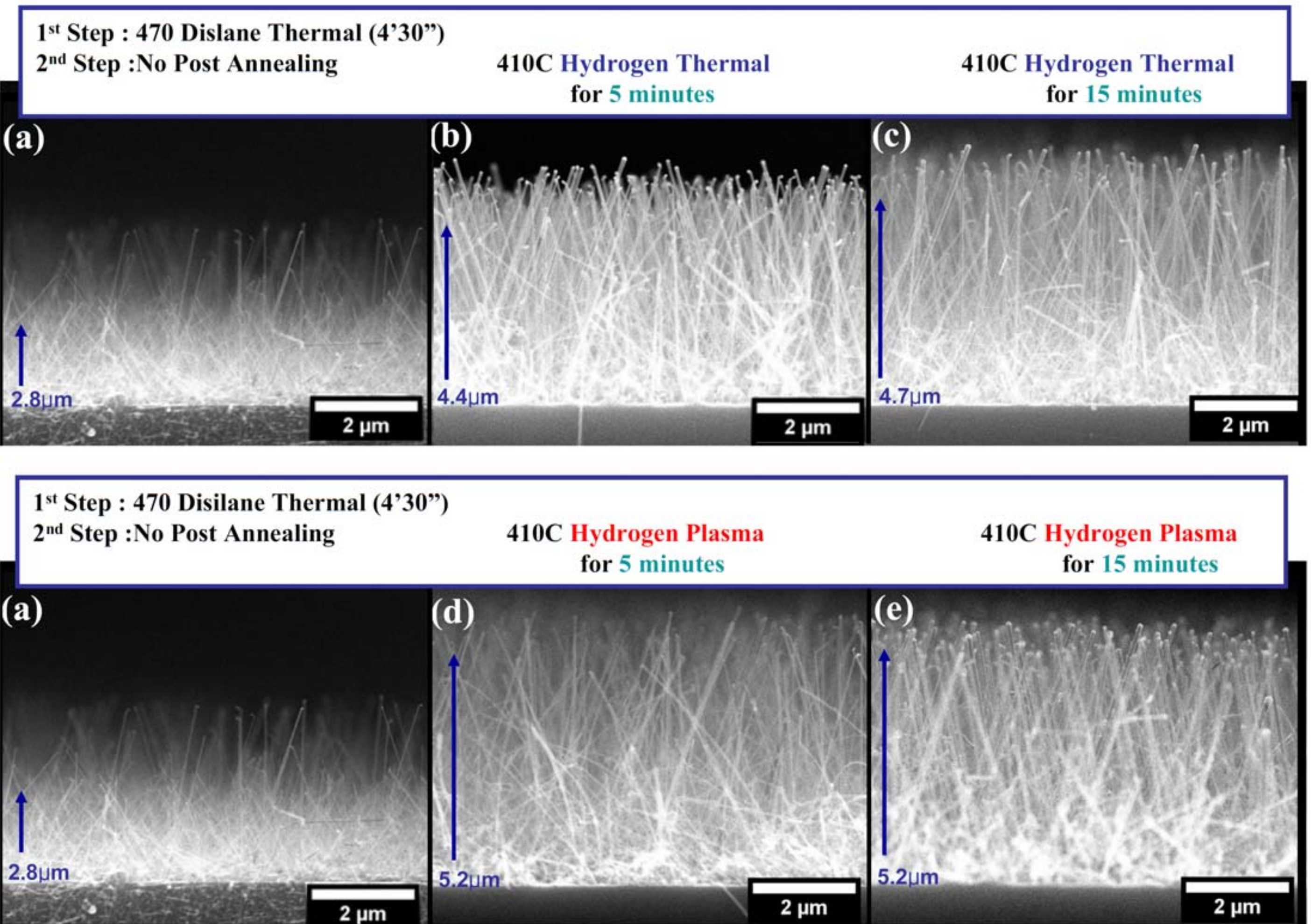
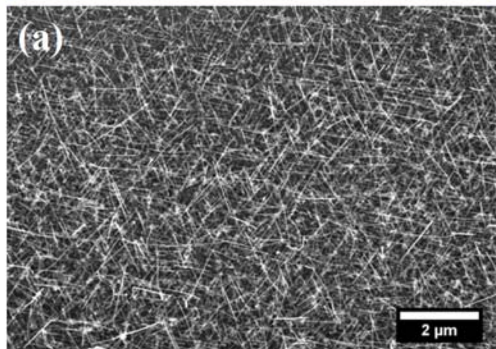


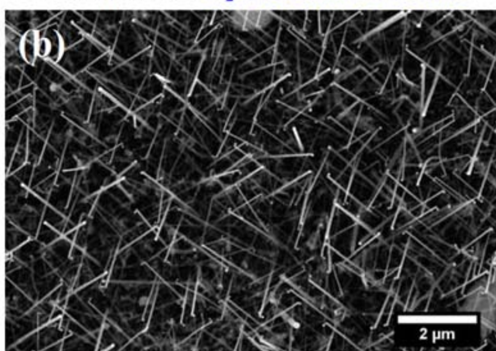
Figure 7.1 Effect of Post-annealing Treatment on Si Nanowires' Morphology

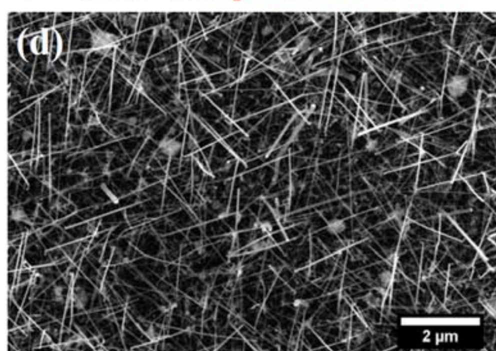
7.2 Nanowire Morphologies after Post-annealing Treatment

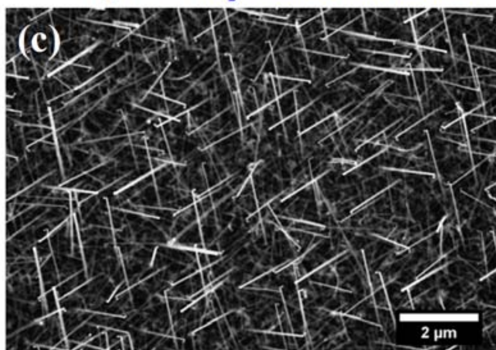
As previously mentioned, thermally grown Si nanowires at 470°C show [111] and [110] growth orientations [Figure 7.1 (a)].[2] Figure 4.7 (b) and (c) show the nanowire growth habits after thermal annealing in hydrogen for 5 and 15 minutes, respectively. In general, the nanowires lengthen and thicken. From an initial 2.8 μm length for thermally grown wires at 470°C, the Si nanowires grow to 4.4 μm for the 5 minute anneal and 4.7 μm for the 15 minute anneal. Without the presence of disilane as a Si source, the nanowires grow gradually during thermal hydrogen post-annealing by a coarsening process.[71, 72] In addition to axial growth, the nanowires thicken in their diameters as shown in Figure 7.2 (b). The diameters were 33 nm for the 5 minute anneal and (c) 47 nm for the 15minute anneal. This compares 16 nm diameter for the unannealled wires in Figure 7.2 (a).

Compared to the hydrogen thermal post-anneal, the nanowires after the plasma treatment were longer and thicker, but less dense, as shown in Figure 7.1 (d) for the 5 minutes and 15 minutes (e). The lengths were 5.21 μm and 5.24 μm, respectively, and the diameters increased to 64 nm and 109 nm as shown in Figure 7.2 (d) and (e).









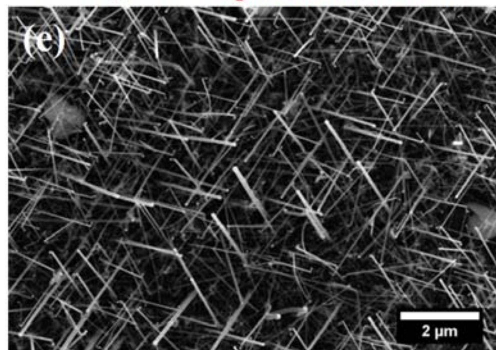


Figure 7.2 FE-SEM plan view images of post-annealing effect on Si nanowires (a) thermally as-grown Si nanowires at 470°C, (b) after post-annealing in hydrogen

thermal treatment for the 5 minutes (c) 15 minutes; (d) after post-annealing in hydrogen plasma for the 5 minutes (d) 15 minutes

7.3 Density of Nanowires after Hydrogen Post-Annealing

In the previous section, it was shown that hydrogen post-annealing altered the morphologies of Si nanowires in both diameter and length. Post-annealing in hydrogen plasma produced even greater changes. The question that arises is what the source of silicon that feeds the growth of the nanowires in the post treatments is. To address this, analysis of the net volume changes of the silicon nanowires was done.

Figure 7.3 illustrates the density of nanowires grown at 470°C by both thermal and plasma post-annealing treatments. Initially, without any post-treatment, 614 nanowires were counted in a 6 µm x 6 µm area. After 5 and 15 minutes thermal post-anneal, the number of nanowires decreased to 101 counts and 69 counts, respectively, [Figure 7.3 (b) and (c)]. Similar decreases were observed for the plasma treated material.

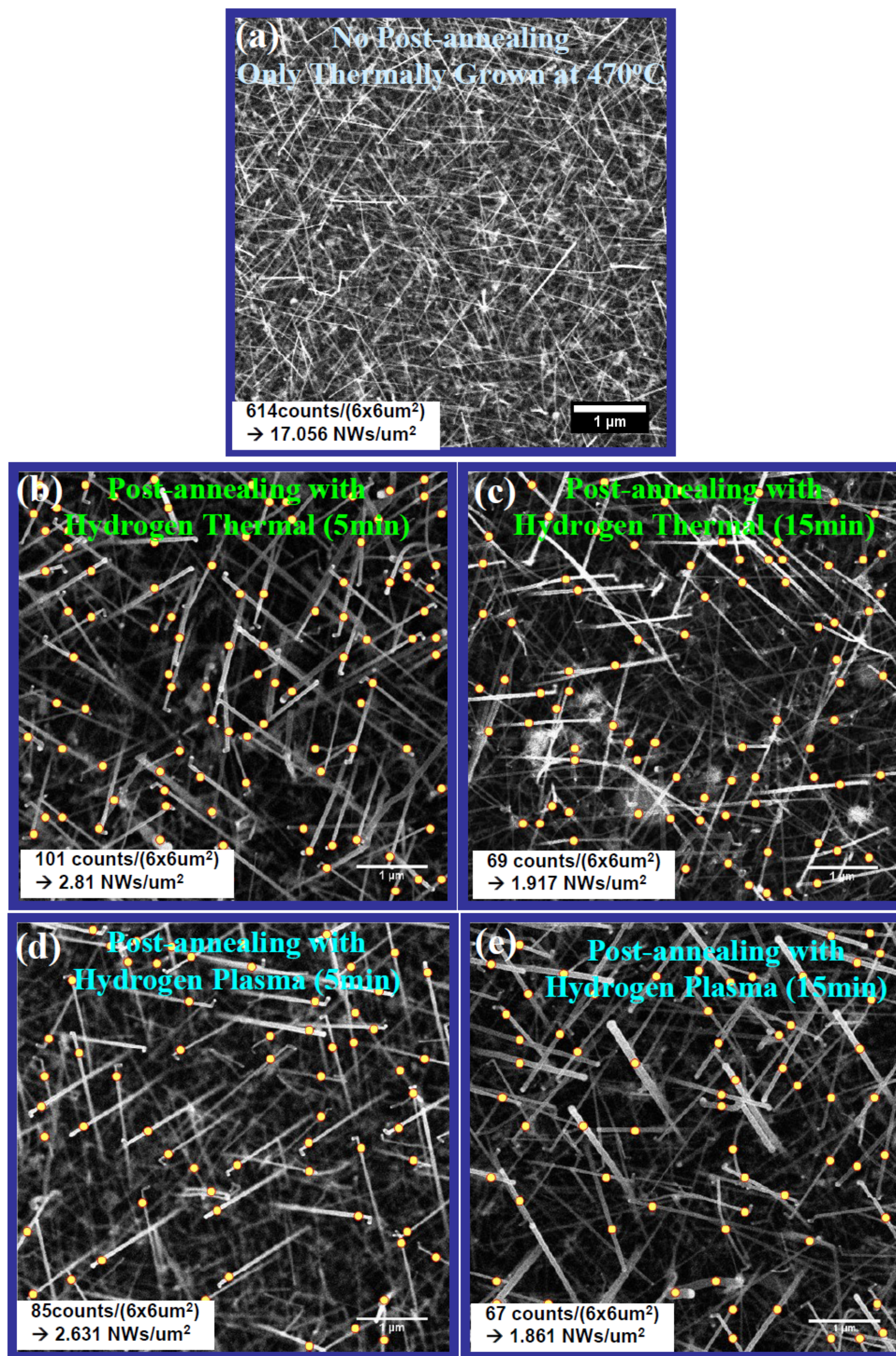


Figure 7.3 Density of Nanowires (a) Thermally Grown at 470°C without Post-annealing (b) Thermal Hydrogen Post-annealing for 5 minutes (c) 15 minutes and

Post-annealing by Hydrogen Plasma for (d) 5 minutes (e) 15 minutes (yellow dots were used to locate nanowire tips to assist in the nanowire counting.)

Figure 7.3 (d) and (e) shows that the density reduces to 85 counts for 5 minutes and 67 counts for 15 minutes after annealed by hydrogen plasma.

Figure 7.4 plots the average length, diameter, and density as a function of post-anneal time. Compared to the number density (614 per 36 μm^2 area) of Si nanowire at the beginning of each post-anneal treatment, the densities decreased as a function post-anneal time. Correspondingly, the larger nanowires grew at the expense of smaller nanowires. In effect, some of the narrow nanowires served as the source of silicon for the thickening nanowires.

This same effect was also observed with the plasma annealed samples, except the morphological changes were more pronounced. That is to say, the plasma annealed nanowires were thicker and somewhat longer than for the thermal annealed samples. It is interesting to note, however, that the biggest differences are seen in the nanowire diameters. The number density and lengths of the thermal and plasma treated samples were very similar to one another.

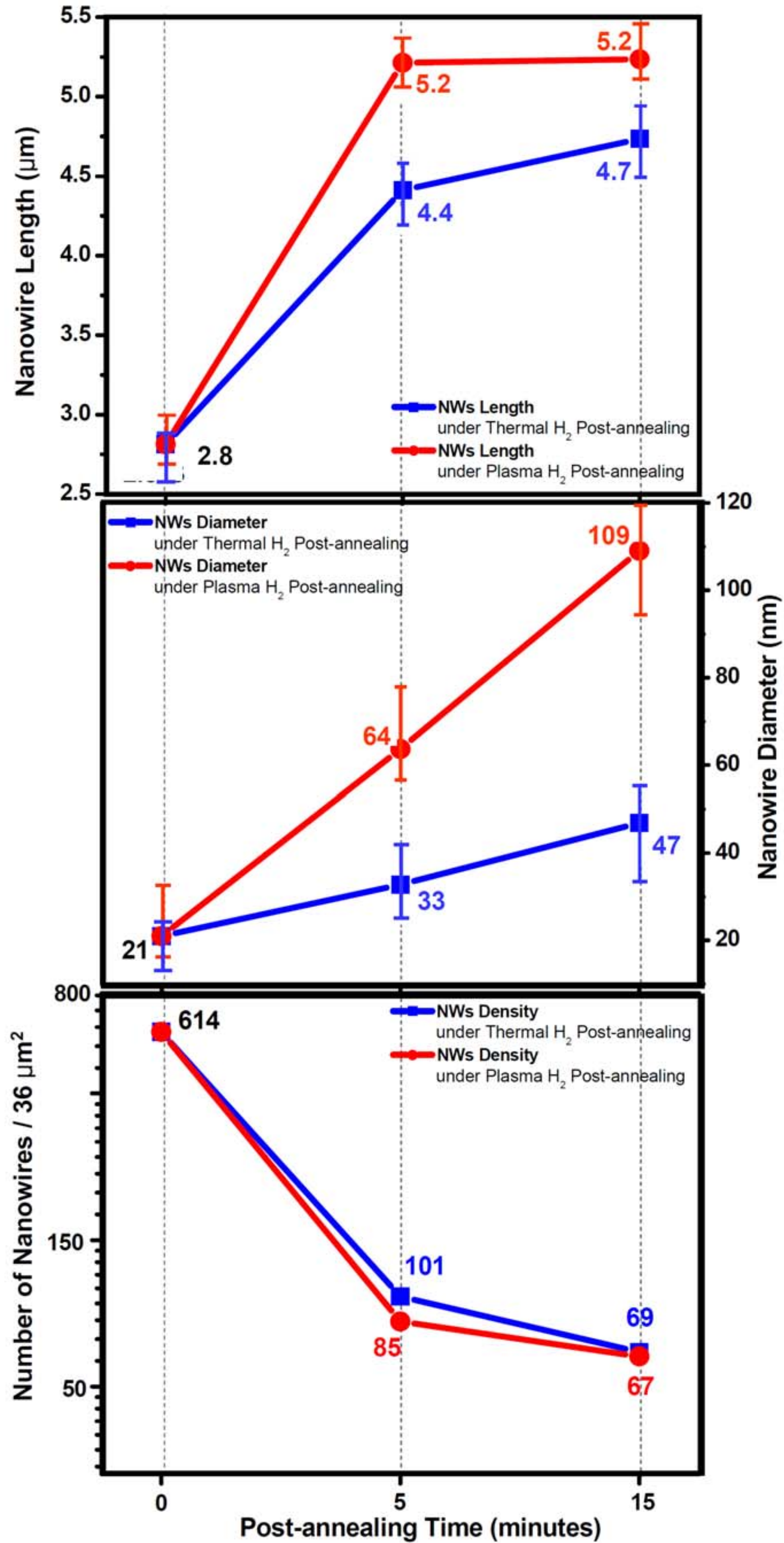

Nanowire Length (μm)
5.5
5.0
4.5
4.0
3.5
3.0
2.5
5.2
5.2
4.4
4.7
2.8
NWs Length
under Thermal H2 Post-annealing
NWs Length
under Plasma H2 Post-annealing
NWs Diameter
under Thermal H2 Post-annealing
NWs Diameter
under Plasma H2 Post-annealing
Nanowire Diameter (nm)
120
100
80
60
40
20
109
64
47
33
21
Number of Nanowires / 36 μm2
800
150
50
614
NWs Density
under Thermal H2 Post-annealing
NWs Density
under Plasma H2 Post-annealing
101
85
69
67
0
5
15
Post-annealing Time (minutes)

Figure 7.4 Comparison of Si nanowires by thermal hydrogen post-annealing and plasma hydrogen post-annealing in terms of their length (top), diameter (middle), and density (bottom)

7.4 Growth Mechanism of Si Nanowire Growth by Post-anneal Process

The nanostructural changes discussed above can be explained by Ostwald ripening.[71-73] Ostwald ripening is driven by the greater stability of larger diameter nanowires in comparison to thin wires and associated fractional contributions of area and curvature of the nanowire surfaces. In effect, a system will drive itself to reduce its overall surface energy, relative to its volume, by reducing its surface area and curvature. Thermal and plasma treatments serve to accelerate the mobility of silicon species on the nanowire surfaces and in the gas phase towards that end.

Figure 7.5 schematically presents a hypothesis of what is thought to be occurring during the post-anneal treatments, and which explain the observations of why thicker nanowires get thicker and thinner nanowires become much thinner. Thre are three processes envisaged including (1) surface diffusion, (2) gas diffusion, and (3) etching and deposition.[73, 74]

As discussed earlier about gold diffusion's role in nanowire branching in chapter 6.3, gold migrates along the Si nanowire's sidewalls, especially after the gas bearing silicon source was stopped.[45, 66, 75] As post-annealing time is increased, more gold is allowed to diffuse along the sidewalls by either thermally or plasma-

stimulated hydrogen. Because hydrogen plasma more actively stimulates surface mobility than simple thermal activation more dramatic shifts in mass should be expected for the plasma treated cases.[4] The same effect should also be seen on the mobility of silicon.

During hydrogen post-anneal process, and even when disilane gas is not present, it is expected that the gas phase will form relatively small concentrations of silicon bearing species in the form of SiH, SiH_2, and SiH_3 (g)). It is expected that gas phase mobilities in both thermal and plasma-enhanced hydrogen. However, the effect of the plasma particles bombarding the silicon surfaces, it is expected that more of the silicon gas species will be generated.[74] With such greater concentrations, it is expected that the coarsening is faster in the plasma than for the simple thermal anneal.[71, 72, 76]

Another contributing factor to coarsening relates to the various degrees of unequal rates of etching and deposition rate for the thermal and plasma-stimulated processes. With respect to etching, hydrogen molecules and radicals bombarded Si nanowire and Si substrate surfaces to remove a silicon.[74, 77] These form various silanes Si_nH_{2n+2} and in turn re-dissociate and deposit Si atoms. In a hydrogen plasma post-anneal treatment, these actions are much faster than in the thermal post-anneal. This would explain why the coarsening processes are so different between the two types of treatments.

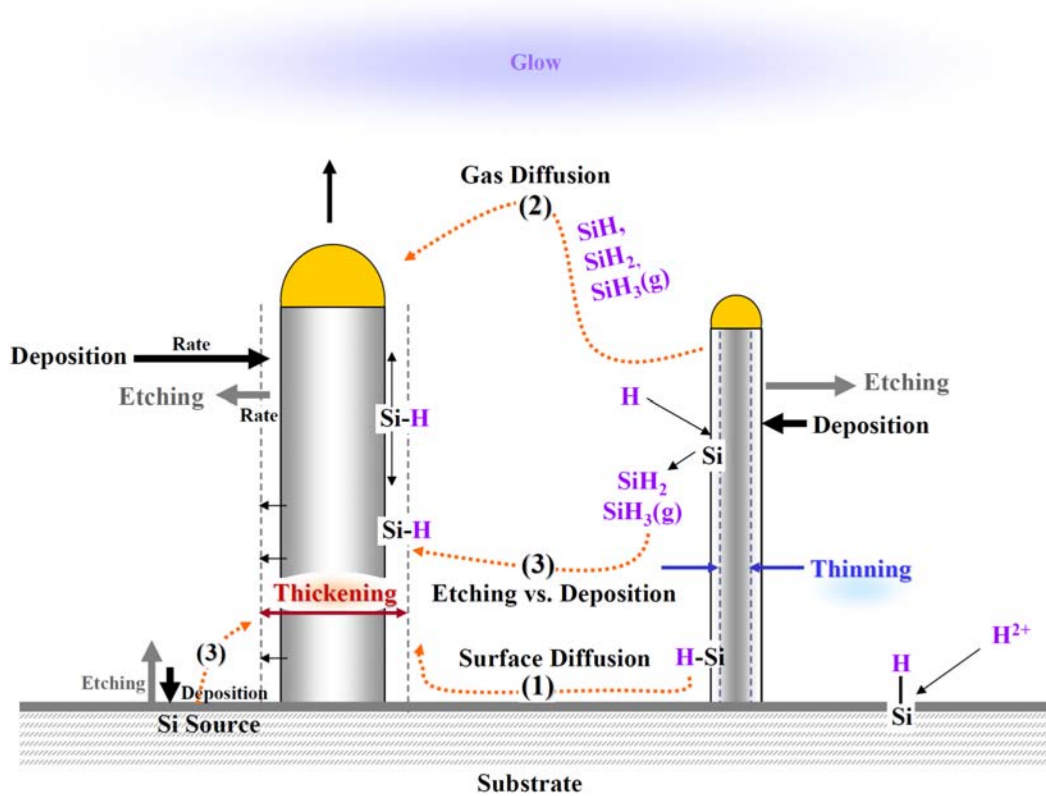


Figure 7.5 Hypothesis Approach of Si Nanowire Growth Mechanism by Post-annealing Based on Three Processes; (1) Surface Diffusion, (2) Gas Diffusion, and (3) Etching and Deposition

7.5 Conclusion

Growth of Si nanowires by a two-step experimental treatment (initially thermal disilane growth at 470°C followed by a hydrogen post-annealing treatment at 410°C without disilane) was characterized in this chapter. One result was that nanowires continued to grow longer and thicker in both treatments despite the fact that an external source of silicon had been stopped. As the anneal time increased, longer and thicker nanowires grew. However, the number densities of nanowires decreased. This can be explained by a Ostwald Ripening Effect, where thicker nanowires grow at the expense of thinner nanowires. The mechanism of coarsening was hypothesized to involve two parallel contributions, namely, by surface diffusion and by gas diffusion. The latter involves the combination of etching and deposition. In a hydrogen plasma, the surface diffusion rate is much faster than for simple thermal annealing. Similarly, the rates of gas-solid reactions (etching and re-deposition) are also accelerated in plasma. The net effect is that nanowire coarsening and elongation will be more pronounced for plasma treated nanowires than for simply thermally treated nanowires.

Hypothesis Growth Mechanisms			
	Hydrogen Thermal Post-annealing		Hydrogen Plasma Post-annealing
Surface Diffusion	$Rate_{thermal}$	$<$	$Rate_{plasma}$
Gas Diffusion	$Rate_{thermal}$	$\approx$	$Rate_{plasma}$
Etching Process vs. Deposition Process	Faster Etching Si source		Faster Deposition From Si Source

Table 7.1 Summarized Comparison of Hypothesis Growth Mechanism by Hydrogen Thermal and Plasma Post-annealing

CHAPTER 8

Conclusions

Silicon nanowires were grown epitaxially on Si (100) and (111) surfaces under both thermal and plasma enhanced growth conditions using the Vapor-Liquid-solid (VLS) mechanism. Nanowire growth in disilane plasmas was studied as a function of temperature, time, disilane partial pressure and substrate preparation. Below the eutectic temperature Si-Au system (363˚C), VLS growth was insufficient to produce any nanowires. However, the morphological variations for nanowires grown at 410˚C were complex and sensitive to the plasma power. In addition, under the substrate preparation by thermal preanneal treatment at 590˚C for 9 minutes, it generally led to more uniform distribution of nanowires subsequently grown at 410˚C by plasma-enhanced CVD. This was associated with the redistribution of gold on the silicon substrates. Nanowires grown under these conditions were also found to have high aspect ratios that were thicker and longer.

Silicon nanowires synthesized by low temperature plasma conditions grew thicker, longer, and denser than thermally grown nanowires. Moreover, the nanowires tended to grow in a bent configuration compared to the linear nanowires grown under thermal conditions. The nanowires tended to bend more with increasing disilane partial pressure up to 25 x 10^{-3} mTorr. At higher disilane partial pressures, more nanowires with greater curvatures (smaller radii of

curvatures) were observed. The nanowire curvature measured geometrically is correlated with the shift of the main silicon peak obtained in Raman spectroscopy (nominally the 519 cm^{-1} band for bulk silicon). The greater curvatures were associated with the greater the greater downshifts. This was attributed to the polycrystalline nature of the nanowires when they grew in a curved morphology. Whereas straight nanowires that obtained from thermal CVD or high temperature plasma CVD where single crystals, and where main Raman band were essentially that of bulk silicon, the curved nanowires exhibited shifts own to below 489 cm-1. This was attributed to the size effect due the nanocrystalline structure of the curved nanowires on the phonon behavior that Raman spectroscopy detects.

A hypothesis was formulated whereby the nanowires curved due to differential growth rates at diametrically opposite sides of the nanowires. The growth rate of those surfaces that were more exposed to the plasma tended to be faster than the surfaces that were more in the shadow of the nanowire. It was also hypothesized that the surfaces where the growth rates were greatest also possessed more surface gold that had diffused out from the gold bead tip due to greater stimulation of surface mobility due to plasma particle bombardment. A secondary hypothesis was discussed that raised the prospect of electrostatics and Van der Waals forces acting on the nanowire tips to accelerate bending during growth. Deduced from a systematic variation of a three-step experimental protocol, the mechanism for bending was associated with asymmetric deposition rate along the outer and inner wall of nanowire.

The conditions for branching and branching morphology are described for

the low temperature growth of silicon nanowires under thermal and RF plasma activation. Using a two-step growth process, the primary nanowire trunks were first made under large diameter growth conditions and at a relatively high temperature (470°C). Secondary and tertiary nanowire branching are observed and isolated for varying thermal and plasma power sequences. The trend clearly shows that increasing plasma power produces shorter but thicker nanowires. In addition, increasing the plasma power (up to 3.5 W) also affects the density of branches, which decreases at higher plasma powers. From both Raman Spectroscopy and high-resolution TEM characterizations, highly disordered smaller nanocrystalline was observed for nanowires grown at higher plasma powers.

Post-annealing thermal and plasma-assisted treatments in hydrogen were compared to understand the influences in the absence of an external silicon source (otherwise supplied by disilane). Longer and thicker nanowires were associated with longer annealing times due to an Ostwald-like ripening effect. The mechanism of coarsening was hypothesized to involve two parallel contributions, namely, by surface diffusion and by gas diffusion. The latter involves the combination of etching and deposition. In hydrogen plasmas, the surface diffusion rate is much faster than for simple thermal annealing. Similarly, the rates of gas-solid reactions (etching and re-deposition) are also accelerated in plasma. The net effect is that nanowire coarsening and elongation will be more pronounced for plasma treated nanowires than for simply thermally treated nanowires.

Using growth methods that combine thermal with plasma-stimulated

growth conditions, we have observed significant nanostructural modification and variation in terms of nanowires' diameter, length, density, and distribution, as compared to simple thermally grown nanowires. The bending of nanowires during growth was commonly observed, which presents the opportunity to controllably produce curved or even semi-circular nanowires that might find utility in the construction of electronic nanodevices. This study identified plasma conditions under which curved nanowires would form. Basically, nanowire curving was observed when grown under the combination of high growth rates associated with the use of disilane with low temperature rf plasmas. The temperatures were not so low, however, as to render the gold-silicon alloy catalyst as solid, and it appeared necessary to maintain a liquid alloy above the Si-Au eutectic temperature of 365˚C.

Post-growth annealing treatments were found to be useful in making relatively minor adjustments in the nanowire morphology. Under such conditions, nanowires were observed to coarsen and elongate via a ripening process that consumed thinner nanowires in order that thicker nanowires would grow.

Finally, the measurement of nanocrystallinity in curved nanowires was examined systematically as a function of the nanowire curvature. Where straight nanowires exhibited little or no strain, and were single crystalline, the bent nanowires were characteristically highly polycrystalline, if not amorphous. High resolution imaging correlated the curvature with the nanowire thickness, i.e., the curvature was greatest where the nanowire was thickest. This supported the model that curvature was caused by differential growth rates across the nanowire,

which was significantly enhanced under plasma conditions. The growth rate was greatest for nanowire surfaces directly exposed to the plasma and slowest where the surfaces were in shadows of the plasma.

REFERENCES

1. Johannes V. Barth, G. C. a. K. K. *Nature* **2005,** 437, (29), 671.
2. Volker Schmidt; Stephan Senz; Gosele, U. *Nano letters* **2005,** 5, (5), 931-935.
3. Lieber, W. L. a. C. M. *JOURNAL OF PHYSICS D: APPLIED PHYSICS* **2006,** 39, R387–R406.
4. Griffiths, H.; Xu, C.; Barrass, T.; Cooke, M.; Iacopi, F.; Vereecken, P.; Esconjauregui, S. *Surface and Coatings Technology* **2007,** 201, (22-23), 9215-9220.
5. Laurent Pichon, R. R., Anne-Claire Salaun. *Project Presentation* **2010**.
6. Bhushan, B. *Handbook of nanotechnology, Springer* **2007**.
7. Julia W.P. Hsu, T. J. C. *SANDIA REPORT* **2007,** SAND2007-6795.
8. Picraux, S. T. *Project Presentation, Los Alamos and Sandia Nanotial Laboratories* **2010**.
9. Kazumasa Yoshida, K. M., Tatsuo Oguchi, Kenichi Tonokura, and; Koshi, M. *Journal of Physics Chemistry A* **2006,** 110, 4726-4731.
10. Pavan Aella, S. I., William T. Petuskey, and S. Tom Picraux. *Advanced Materials* **2007,** 19, 2603-2607.
11. V. Schmidt, J. V. W., and U. Go¨sele. *Chemical Reviews* **2010,** 110, 361-388.
12. J Tang, P. P., A Tserepi and D Tsoukalas. *Nanotechnology* **2011,** 22, 235306.
13. A. Lugstein; M. Steinmair; Y. J. Hyun; G. Hauer; Pongratz. *Nano Letters* **2008,** 8, (8), 2310-2314.

14. J. Cervenka; M. Ledinsky; H. Stuchlikova; J. Stuchlik; Z. Vyborny; J. Holovsky; K. Hruska; A. Fejfar; Kocka, J. *Physica status solidi. PSS-RRL. Rapid research letters* **2010,** 4, (1-2), 37-39.

15. Ostrikov, K. *Plasma Nanoscience, Wiley-VCH* **2005**.

16. Zuraw, D. M. D. a. M. K. *Principles of Chemical Vapor Deposition, Kluwer AcademicPublishers* **2003**.

17. Joseph Goldstein, D. N. *Scanning Electrom Microscopy and X-ray Microanalysis, Kluwer Academic/Plenum Publishers* **2000**.

18. Zheng, J.; Yang, R.; Xie, L.; Qu, J.; Liu, Y.; Li, X. *Advanced Materials* **2010,** 22, (13), 1451-1473.

19. Bashar, S. A. *Ph.D thesis* **1998**.

20. Group, E. A. http://www.eaglabs.com/techniques/analytical_techniques/.

21. Hessler-Wyser, D. A. *Presentation for Electron-matter interaction* **2009**.

22. L. Andrew Lyon, C. D. K., Audrey P. Fox, Bonnie E. Baker, Lin He, Sheila R. Nicewarner, Shawn P. Mulvaney, and Michael J. Natan. *Analytical Chemistry* **1998,** 70, 341R-361R.

23. Science, L. E. C. f. S. S. http://le-csss.asu.edu/raman.

24. Piscanec, S.; Ferrari, A. C.; Cantoro, M.; Hofmann, S.; Zapien, J. A.; Lifshitz, Y.; Lee, S. T.; Robertson, J. *Materials Science and Engineering: C* **2003,** 23, (6-8), 931-934.

25. Fukata, N.; Oshima, T.; Murakami, K.; Kizuka, T.; Tsurui, T.; Ito, S. *Applied Physics Letters* **2005,** 86, (21), 213112.

26. Li, C.; Fang, G.; Sheng, S.; Chen, Z.; Wang, J.; Ma, S.; Zhao, X. *Physica E: Low-dimensional Systems and Nanostructures* **2005,** 30, (1-2), 169-173.

27. Somnath Bhattacharyya; Dmitry Churochkin; Erasmus, R. M. *Applied Physics Letters* **2010,** 97, 141912.

28. J. D. Prades; J. Arbiol; A. Cirera; Morante, J. R. *Applied Physics Letters* **2007,** 91, 123107.

29. Piscanec, S.; Cantoro, M.; Ferrari, A. C.; Zapien, J. A.; Lifshitz, Y.; Lee, S. T.; Hofmann, S.; Robertson, J. *Physical Review B* **2003,** 68, (24), 241312.

30. Min-Sung Jeon, Y. T., Minoru Aoyagi, and Koichi Kamisako *Jpn. J. Appl. Phys.* **2009,** 48, (1), 015002.

31. Niu, J.; Sha, J.; Wang, L.; Ji, Y.; Yang, D. *Physica E: Low-dimensional Systems and Nanostructures* **2005,** 27, (3), 309-313.

32. Linwei Yu, P.-J. A., Gennaro Picardi, Isabelle Maurin and Pere Roca i Cabarrocas. *Nanotechnology* **2008,** 19, (48), 485605.

33. Jeon, M.; Kamisako, K. *Journal of Alloys and Compounds* **2009,** 476, (1-2), 84-88.

34. Mbenkum, B. N.; Schneider, A. S.; Schultz, G.; Xu, C.; Richter, G.; van Aken, P. A.; Majer, G. n.; Spatz, J. P. *ACS Nano* **2010,** 4, (4), 1805-1812.

35. Pengfei, Q.; William, S. W.; Huaizhou, Z.; Dunwei, W. *Applied Physics Letters* **2008,** 93, (16), 163101.

36. Lai, Y.-S.; Wang, J.-L.; Liou, S.-C.; Tu, C.-H. *Applied Physics A: Materials Science & Processing* **2009,** 94, (2), 357-363.

37. Massimo Cuscuna, A. C., Luigi Mariucci, Guglielmo Fortuanto, Laura Felisari, Giuseppe Nicotra, Corrado Spinella, Alessandro Pecora, and Faustino Martelli. *Nanotechnology* **2010,** 21, 255601.

38. A. Colli; S. Hofmann; A. Fasoli; A. C. Ferrari; C. Ducati; R. E. Dunin-Borkowski; Robertson, J. *Applied Physics A: Materials Science & Processing* **2006,** 85, 247-253.

39. K. E. Moselund; H. Ghoneim; H. Schmid; M. T Björk, E. L.; S. Karg; G. Signorello; D .Webb; M. Tschudy; Riel, R. B. a. H. *Nanotechnology* **2010,** 21, (43), 435202.

40. Saeed Akhtar; A. Tanaka; K. Usami; Y. Tsuchiya; Oda, S. *Thin Solid Films* **2008,** 517, 317-319.

41. F. Ruffino; A. Canino; M. G. Grimaldi; F. Giannazzo; F. Roccaforte; Raneri, a. V. *Journal of Applied Physics* **2008,** 104, 024310.

42. Cantoro, M.; Hofmann, S.; Pisana, S.; Ducati, C.; Parvez, A.; Ferrari, A. C.; Robertson, J. *Diamond and Related Materials* **2006,** 15, (4-8), 1029-1035.

43. C. X. Wang; Masahiro Hirano; Hosono, H. *Nano letters* **2006,** 6, (7), 1552-1555.

44. Nobuhiko Ozaki; Yutaka Ohno; Jun Kikkawa; Takeda, S. *Journal of Electron Microscopy* **2005,** 54, i25-i29.

45. Woo-Jung Lee; Jinwon Ma; Jungmin Bae; Mann-Ho Cho; Ahn, J. P. *Cryst. Eng. Comm.* **2011,** 13, 690-696.

46. W. H. Chen; R. Larde; E. Cadel; T. Xu; B. Grandidier; Nys, J. P. *Journal of Applied Physics* **2010,** 107, 084902.

47. Ying Xiang; Linyou Cao; Sonia Conesa-Boj; Sonia Estrade; Jordi Arbiol; Francesca

Peiro; Martin Heiß; I. Zardo; Joan R. Morante; Mark L. Brongersma; Morral, A. F. i. *Nanotechnology* **2009,** 20, (24), 245608.

48. Smith, D. A.; Holmberg, V. C.; Korgel, B. A. *ACS Nano* **2010,** 4, (4), 2356-2362.

49. Cheng-Lun Hsin, W. M., Yudong Gu, Yifan Gao, Chi-Te Huang, Yuzi Liu,; Lih-Juann Chen, a. Z.-L. W. *Advanced Materials* **2008,** 20, 3919–3923.

50. Chen, J.; Conache, G.; Pistol, M.-E.; Gray, S. M.; Borgstrom, M. T.; Xu, H.; Xu, H. Q.; Samuelson, L.; H kanson, U. *Nano Letters* **2010,** 10, (4), 1280-1286.

51. Giri, S. D. a. P. *Nano Express* **2011,** 6, 320.

52. Nemanich, S. A. L. a. R. J. *Physica* **1983,** 117B & 118B, 871-873.

53. Matthew T. McDowell; Austin M Leach; Gall, K. *Modelling Simul. Mater. Sci. Eng* **2008,** 16, (4), 045003.

54. Merkulov, V. I.; Melechko, A. V.; Guillorn, M. A.; Lowndes, D. H.; Simpson, M. L. *Applied Physics Letters* **2001,** 79, (18), 2970.

55. Prokes, S. M.; Arnold, S. *Applied Physics Letters* **2005,** 86, (19), 193105.

56. Chen, X.; Xing, Y.; Xu, J.; Xiang, J.; Yu, D. *Chemical Physics Letters* **2003,** 374, (5-6), 626-630.

57. T. Qiu; X. L. Wu; J. C. Shen; Peter C. T. Ha; Chu, P. K. *Nanotechnology* **2006,** 17, (23), 5769-5772.

58. Kumar, D.; Srivastava, S.; Singh, P.; Sood, K.; Singh, V.; Dilawar, N.; Husain, M. *Journal of Nanoparticle Research* **2010,** 12, (6), 2267-2276.

59. Mattew J. Bierman; Jin, S. *Energy & Environmental Science* **2008,** 2, 1050-1059.

60. Gregory S. Doerk; Velimir Radmilovic; Maboudian, R. *Applied Physics Letters* **2010,** 96, 123117.

61. Wu, Z. H.; Mei, X.; Kim, D.; Blumin, M.; Ruda, H. F.; Liu, J.; Kavanagh, K. L. *Applied Physics Letters* **2003,** 83, (16), 3368.

62. Gregory S. Doerk; Nicola Ferralis; Carlo Carraro; Maboudian, R. *Journal of Materials Chemistry* **2008,** 18, 5376-5381.

63. Maoqi He; Mohammad, S. N. *J. Vac. Sci. Technol. B* **2007,** 25, (6), 1909.

64. Eric Dailey; Prashanth Madras; Drucker, J. *Journal of Applied Physics* **2010,** 108, 064320.

65. Yuting Wan; Yewu Wang; Bo Chen; Yanjun Fang; Sha, J. *Phys. Status. Solidi C* **2009,** 6, (3), 687-689.

66. Martien I. den Hertog; Jean-Luc Rouviere; Florian Dhalluin; Pierre J. Desre; Pascal Gentile; Pierre Ferret; Fabrice Oehler; Baron, T. *Nano letters* **2008,** 8, (5), 1544-1550.

67. Z. X. Su; J. Sha; J. J. Niu; J. X. LIu; Yang, D. R. *Physica Status Solidi (a)* **2006,** 203, (4), 792-801.

68. Rong-ping Wang; Guang-wen Zhou; Yu-long Liu; Sha-hua Pan; Hong-zhou Zhang; Da-peng Yu; Zhang, Z. *Physical Review B* **2000,** 61, (24), 16827.

69. I. Zardo; S. Conesa-Boj; S. Estrade; L. Yu; F. Peiro; P. Roca i Cabarrocas; J. R. Morante; J. Arbiol; Morral, A. F. i. *Applied Physics A: Materials Science & Processing* **2010,** 100, (287-296).

70. Vladimir I. Merkulov, A. V. M., Michael A. Guillorn, Douglas H. Lowndes, and

Michael L. Simpson. *Applied Physcis Letters* **2001,** 79, 2970.

71. V. A. Sivakov, R. S., F. Syrowatka, F. Falk, U. Gösele and S. H. Christiansen. *Nanotechnology* **2009,** 20, (40), 405607

72. Nagashima, K.; Yanagida, T.; Oka, K.; Tanaka, H.; Kawai, T. *Applied Physics Letters* **2008,** 93, (15), 153103.

73. K. W. Adu; H. R. Gutierrez; U. J. Kim; G. U. Sumanasekera; Eklund, P. C. *Nano Letters* **2005,** 5, (3), 409-414.

74. Dzbanovsky, N. N.; Dvorkin, V. V.; Pirogov, V. G.; Suetin, N. V. *Microelectronics Journal* **2005,** 36, (7), 634-638.

75. Kodambaka, S.; Tersoff, J.; Reuter, M. C.; Ross, F. M. *Physical Review Letters* **2006,** 96, (9), 096105.

76. Billel Kalache, P. R. i. C., and Anna Fontcuberta i Morral. *Japanese journal of applied physics* **2006,** 45, (No. 7), L190-L193.

77. Ming-Che Yang, J. S., Tsung-Shine Ko, Hsuen-Li Chen and Tieh-Chi Chu. *Japanese journal of applied physics* **2005,** 44, (no. 7b), 5791.