Temperature Compensated, High Common Mode Range, Cu-Trace Based Current Shunt Monitors Design and Analysis

by

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ABSTRACT

Sensing and controlling current flow is a fundamental requirement for many electronic systems, including power management (DC-DC converters and LDOs), battery chargers, electric vehicles, solenoid positioning, motor control, and power monitoring. Current Shunt Monitor (CSM) systems have various applications for precise current monitoring of those aforementioned applications. CSMs enable current measurement across an external sense resistor (R_S) in series to current flow. Two different types of CSMs designed and characterized in this paper. First design used direct current reading method and the other design used indirect current reading method. Proposed CSM systems can sense power supply current ranging from 1mA to 200mA for the direct current reading topology and from 1mA to 500mA for the indirect current reading topology across a typical board Cu-trace resistance of 1 Ω with less than 10 µV input-referred offset, 0.3 µV/°C offset drift and 0.1% accuracy for both topologies. Proposed systems avoid using a costly zero-temperature coefficient (TC) sense resistor that is normally used in typical CSM systems. Instead, both of the designs used existing Cu-trace on the printed circuit board (PCB) in place of the costly resistor. The systems use chopper stabilization at the front-end amplifier signal path to suppress input-referred offset down to less than 10 µV. Switching current-mode (SI) FIR filtering technique is used at the instrumentation amplifier output to filter out the chopping ripple caused by input offset and flicker noise by averaging half of the phase 1 signal and the other half of the phase 2 signal. In addition, residual offset mainly caused by clock feed-through and charge injection of the chopper switches at the

chopping frequency and its multiple frequencies notched out by the since response of the SI-FIR filter. A frequency domain Sigma Delta (ΣΔFD) ADC which is used for the indirect current reading type design enables a digital interface to processor applications with minimally added circuitries to build a simple 1st order ΣΔ ADC. The CSMs are fabricated on a 0.7µm CMOS process with 3 levels of metal, with maximum V_{ds} tolerance of 8V and operates across a common mode range of 0 to 26V for the direct current reading type and of 0 to 30V for the indirect current reading type achieving less than 10nV/$\sqrt{\boldsymbol{Hz}}$ of flicker noise at 100 Hz for both approaches. By using a semi-digital SI-FIR filter, residual chopper offset is suppressed down to 0.5mV_{pp} from a baseline of 8mV_{pp}, which is equivalent to 25dB suppression.

To My Wife Jiyeon, my son Damin and Parents

ACKNOWLEDGMENTS

First of all, I would like to thank God for preserving every step of my path from the beginning of my first breath or even before that. Looking back the time when I decided to quitting my job and pursuing a PhD degree, I was filled with half of hope and the other half of worries. Even though there could be some other choices regarding selecting schools and pursuing a new degree as other usual stuffs in my life, I'm very sure that the choice of school and meeting with my academic advisor and the research opportunity granted from him have been the best and lucky chance that I have ever been given.

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1 INTRODUCTION

As electronic devices are becoming more versatile by converging many functions and independent devices into one compact form, designing power hungry portable devices with longer operation time is becoming more important than ever. Not only building long-lasting power management system is important, but also using it more efficiently is becoming essential in recent electronics applications. As a consequence, sensing and controlling current flow from energy sources is a fundamental requirement for several electronic systems [1]-[5], including power management (DC-DC converters and LDOs) [1], [6]-[7], battery chargers [8]-[9], electric vehicles [10]-[11], solenoid positioning [12]-[13], motor control [14], and power monitoring [15]. Current Shunt Monitors (CSMs) are part of the instrumentation amplifier family, which is dedicated to precise sensing of system current for industrial and consumer applications [16]-[18]. In many system applications, sensing of supply current with less than 1% error across the power source common-mode voltage range is required. Most practical way of sensing the current is measuring voltage drop across a current sensing resistor (R_S) [19], which requires reading out of voltages ranging from 10mV to hundreds of mV in typical applications [20]. Fig. 1.1 shows a concept of how current sensing can be completed through a dedicated sense resistor which placed in series with the current path.

Sensing of weak supply current by monitoring voltage drop across current sensing resistor in the presence of high common mode range input signal (0V up to 30V in case of the proposed designs) is a challenging design task.

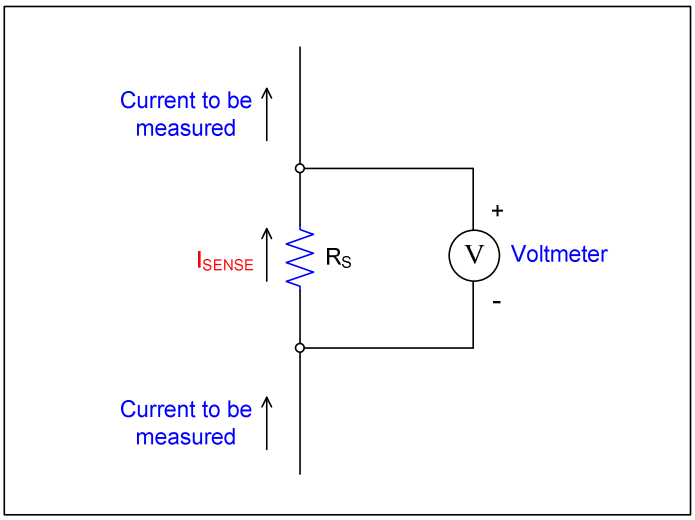


Fig. 1.1 Sensing of current through a series connected sense resistor R_S

To sense the typical range of the voltage drop, input referred offset floor of the input front-end pre-amplifier should be well below tens of micro volt (μV) range [21]. To obtain low input referred offset, auto-zeroing and chopping is widely used in current shunt monitors. While each approach has its own strengths and trade-offs, due to noise folding problem associated with auto-zeroing [22], chopping has been the preferred method for instrumentation applications [23]-[26].

Although chopping can effectively suppress input referred DC offset by modulating it to the chopping frequency, the up-converted DC offsets and flicker noise can cause considerable ripple at the chopping frequency [27]. Mismatches, clock feed-through, and charge injection of the first chopping switches can also cause residual offset at the amplifier input, which is amplified by the amplifier gain and modulated to the odd multiples of the chopping frequency.

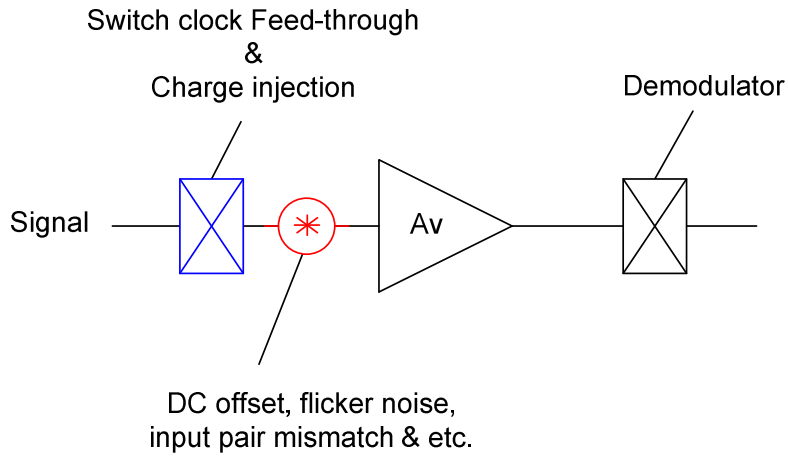


Fig. 1.2 Sources of noise in chopper amplifier system

Fig. 1.2 shows the sources of noise that contributed to the final amplifier output after demodulation in general chopping amplifier systems. To obtain the required input referred offset level, 10μV, with other specification targets listed in the following chapters, two different types of CSMs have been designed and presented in this dissertation. First type of design adopted direct current reading topology which takes some portion of the current to be measured into the CSM loop to read the precise amount of current flowing while the second design adopted indirect current reading topology which converts the sensed input voltage drop corresponding to the amount of the current flowing through a sense resistor (R_S) back into current by using a gain boosted Gm stage inside CSM system. Both of the proposed designs implement ripple reduction scheme that uses a second order current mode semi-digital FIR filter. The current mode second order semi-digital FIR filter provides a notch filter at the integer harmonics of the chopping

frequency to notch out the chopping ripple and residual offset at the multiples of the chopping clock frequency and current domain operation removes the need for current to voltage conversion, which eliminating a possible step of generating noise. Fig. 1.3 shows the typical form of a notch filter response.

Furthermore, the indirect current reading type CSM embedded all digital frequency-domain ADC. Sigma-Delta Frequency to Digitization (ΣΔFD) block that requires only two D flip-flops (DFFs) and one XOR gate has been designed to build the required first order ΣΔ ADC. This added function with minimal power dissipation enables digital output, which makes the system possible to interface with other digital systems.

While a wide variety of applications benefit from the ability to measure current flow, current sensing has been primarily for circuit protection and reporting. However, as technology advances, current sensing is becoming more important as a way to monitor performance and ultimately enhance it [28].

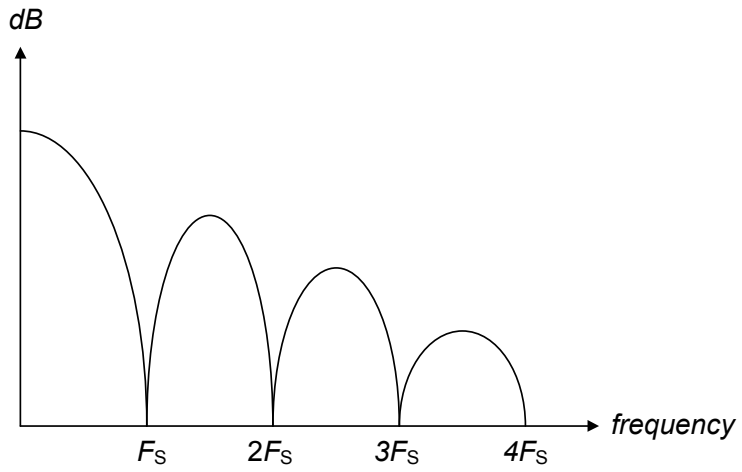


Fig. 1.3 A general form of notch filter response

Some applications that benefit from current sensing can be:

- Over-current protection and supervising circuits

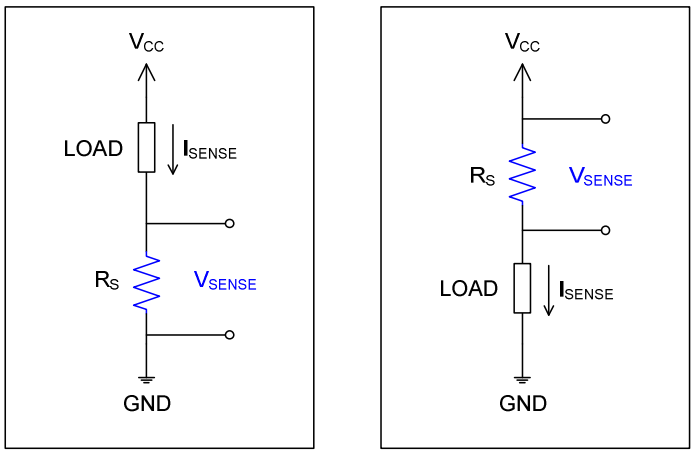
  (enhancing battery life for mobile application and Hybrid vehicles)
- Programmable current sources
- Linear and switch-mode power supplies
- Battery chargers
- Battery-operated circuits for which the ratio of current flow into and out of a rechargeable battery should be known
- Proprotional solenoid control (current control)

The paper is organized as follows. In chapter 2, different current sensing techniques (methods), definition and types of current shunt monitors followed by explanation of related prior works are discussed. Basic principles of chopper stabilization technique including analyzing noise entailed due to chopping and some techniques to reduce residual offset are discussed in chapter 3. Chapter 4 introduces the proposed current shunt monitor design, which contains two different type of design, one with using direct current reading topology and the other is using indirect current sensing method. Detailed architecture and circuit level design of the proposed current sensing systems and measurement results for both of approaches will be following in the same chapter. Finally, the conclusion is drawn in chapter 5.

2 CURRENT SENSING TECHNIQUES

2.1 Different Current Sensing Methods

Current sensors are electronic circuits that monitor the current flow by measuring voltage drop across a resistor (R_S) placed in-line with the current path. The outputs of the current sensor can be either a voltage or a current that is proportional to the current through the measured path. Unlike voltage monitoring, which can be performed with a high degree of precision while introducing virtually no losses into the measurement system, current sensing requires sacrificing DC precision for low insertion loss or suffering high insertion loss for greater DC precision depends on the magnitude of the inserted sensing resistor (R_S) [29]. Current sensing can be performed either at the low side or the high side of the load. Low side current sensing can be performed by connecting a current sensing element between the load and the ground as shown in Fig. 2.1 (a). Current is measured by looking at the voltage drop across a resistor (R_S) placed between the load and ground. Some of the advantages of low side current sensing technique are that it is straight forward, easy, and rarely requires more than an op-amp to implement, and is inexpensive and precise [17]. However, addition of undesirable resistance in the ground path may cause ground noise which cannot be tolerated in most high accuracy system applications. In a similar manner, high side current sensing requires connecting a current sensor between the supply and the load as shown in Fig. 2.1 (b). Current is measured by looking at the voltage drop across a resistor (R_S) placed between the supply and the load. Some of the advantages of high side current sensing technique are as following.



(a) (b)

Fig. 2.1 (a) Low side and (b) high side current sensing

Since a current sensor connected directly to the power source, it can detect any downstream failure and trigger appropriate corrective action. Also, it won't create an extra ground disturbance that comes with a low side current sensing design [29].

While introducing no ground disturbance as in low side current sensing, high side current sensing approach must withstand switching wide common-mode range voltages, which may be outside the limits of the supply rails of the amplifiers being used [28]. Also, high side current sensing technique requires very careful resistor matching in order to obtain an acceptable common mode rejection ratio (CMRR). The results of inaccuracy due to the resistor mismatching are [29]:

- A 0.01% deviation in any resistor value lowers the CMRR to 86dB

- A 0.1% deviation lowers it to 66dB
- A 1% deviation lowers it to 46dB

A conceptual view of a conventional in-line current sensing signal chain is shown in Fig. 2.2. Both the low side and high side sensing concept are depicted in a single drawing for simplicity. Both of the techniques require insertion of a resistor in series with the load. Although reduction of such resistor would bring down the amount of the power dissipated by the component, the measured voltage generated by the current of interest also gets reduced, which results in increased errors for the input sensing amplifier. Also, such a resistor typically requires high precision over the entire operating temperature variation, which also increase the overall system cost. Therefore low insertion loss input current sensing component with high precision sensing instrumentation amplifier that has less than 10μV input referred offset is crucial for this design.

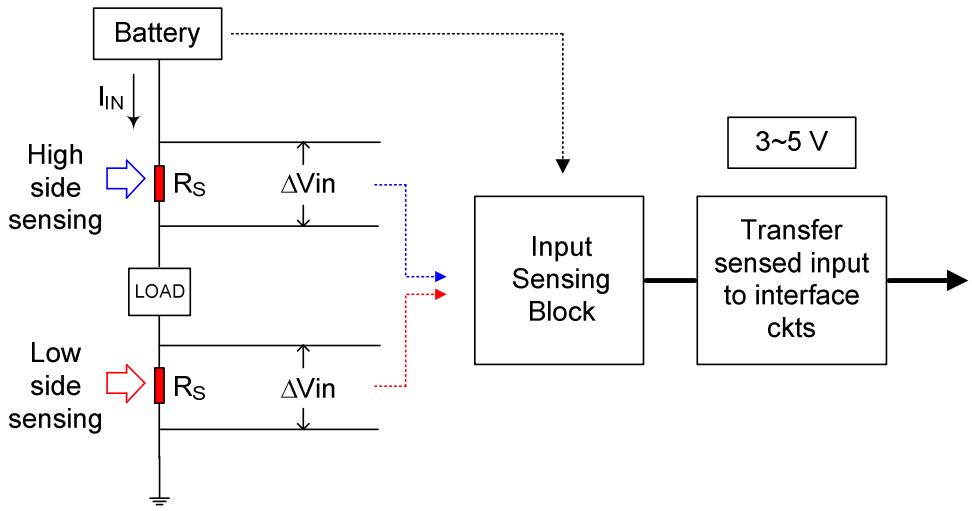


Fig. 2.2 Conventional Low and High side in-line current sensing signal chain

2.2 Definition and Types of Current Shunt Monitors

CSMs are unique new amplifier family that is solely dedicated to high side current sensing applications, and contains all the necessary functions needed to perform the measurement easily and economically [17]. Figure 2.3 shows an example of test set-up (signal chain) by using a conventional CSM.

There are two main approaches of sensing current that can fulfill the aforementioned requirements. First method is to sense the current directly by the CSM [19]. In this approach, two resistors of R_S and R_G designed ratiometrically sense a portion of the current directly into the CSM system as depicted in Fig. 2.4(a). The voltage drop with respect to the current ratio set by the size of the R_S and R_G across the final load resistance (R_L) can be measured as follows.

$$V_o = I_{IN} R_S \left(\frac{R_L}{R_G}\right) \tag{2.1}$$

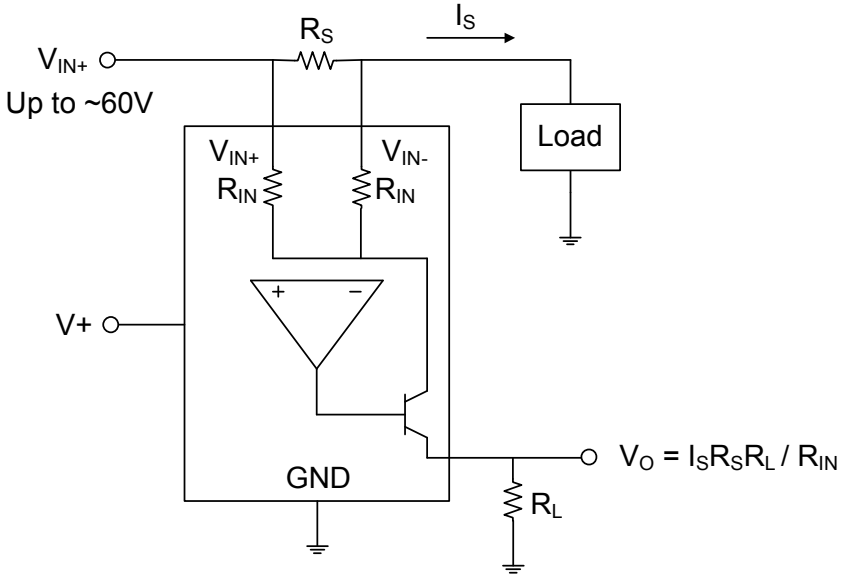
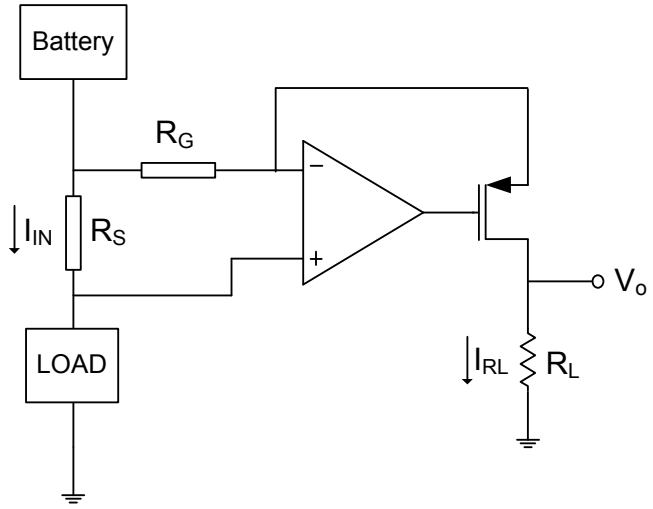
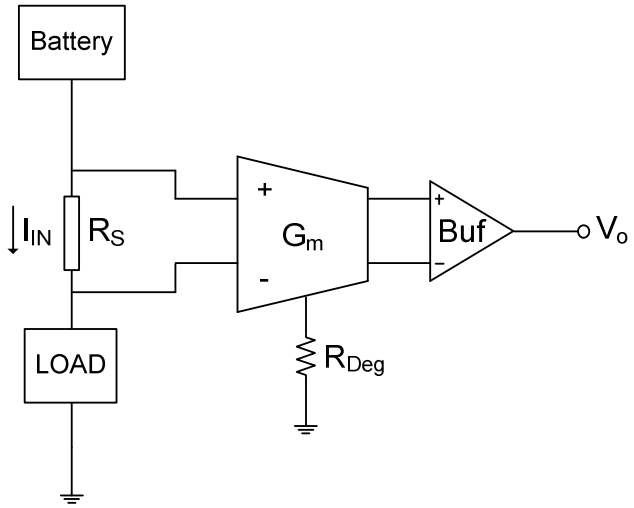


Fig. 2.3 A signal chain of current sensing by using a conventional CSM



(a)



(b)

Fig. 2.4 (a) Direct and (b) Indirect current reading topology

Interestingly, the ratio of R_G and R_S has important roles in terms of how much of the input referred offset would affect the final value of the CSM noise. Shown in Fig. 2.5. is calculation of the relationship among R_S, R_G and DC input offset in terms of contribution of the input offset to the final noise level.

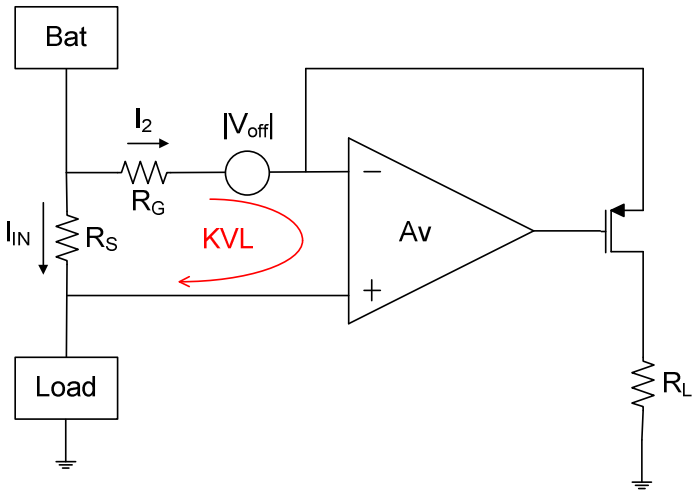


Fig. 2.5 Input referred offset contribution with respect to the ratio of R_G/R_S

Applying KVL in the loop will result in:

$$I_{IN}R_S - R_G I_2 + |V_{off}| = 0 \tag{2.2}$$

Solving equation (2.2) with respect to the input current to the system, I_2 will result in:

$$I_2 = I_{IN}\left(\frac{R_S}{R_G}\right) + \frac{V_{off}}{R_G} \tag{2.3}$$

The equation (2.3) clearly shows that the input referred DC offset is inversely proportional to the magnitude of gain resistance (R_G). Therefore, increasing the ratio of R_G/R_S is desirable in typical CSM application.

The second method is reading the current indirectly by using input transconductance (gm) stages [30]. As shown in Fig. 2.4(b), by maintaining the effective gm of the input stage constant, current proportional to the product of gm and sensed input voltage across a sensing resistor can be measured as in the following equation.

$$I_{sense} = G_{meff}V_{sense} \quad where, \quad G_{meff} = \frac{1}{R_{Deg}} \tag{2.4}$$

However, the effective input transconductance (Gm) value of source degenerated transconductance stage is not linear over the entire operation range unless the gm value of input transistor pair is huge enough to be ignored with respect to the magnitude of degeneration resistance, R_{Deg} as shown in the following equation.

$$G_m \cong \frac{1}{R_{Deg}+\frac{1}{g_m}} \tag{2.5}$$

Therefore, a crucial challenge of designing a current shunt monitor based on this topology is how to increase the effective transconductance value of Gm over the entire operation (input common mode) range.

2.3 Prior Work Analysis

As briefly mentioned in earlier chapter, the residual offset occurred by the chopper stabilization needs to be canceled out through a following circuit chain in CSM systems. Designing CSMs with less noise and possible reduction of cost has been actively performed. There are several prior works that can be related to CSM designs. Since chopping technique was used for all the works due to the superiority compared with other offset cancelling techniques, namely auto-zeroing, and correlated doubling sampling [27], the prior works inevitably have residual offset and entail offset cancelling mechanism. Most of the prior arts fall into one of the subcategories as following; ripple reduction loop based low pass filter technique [19], band pass filter based ripple reduction technique [31], and nested chopper based ripple reduction [22]. In general, each different method was

designed to have lower comparable residual ripple while each approach has its own shortcoming. The following prior works that represents each one of the aforementioned approach is discussed in this chapter.

2.3.1 A Current-Feedback Instrumentation Amplifier with 5μV Offset for Bidirectional High Side Current Sensing

Shown in Fig. 2.6 is a simplified signal chain of the presented prior art. This architecture uses a ripple reduction loop based low pass filter technique for residual offset cancellation. Basic operation principle can be found through the following:

$$I_1 = G_1 \times V_{in} \tag{2.6}$$

$$I_2 = G_2 \times V_{fb} \tag{2.7}$$

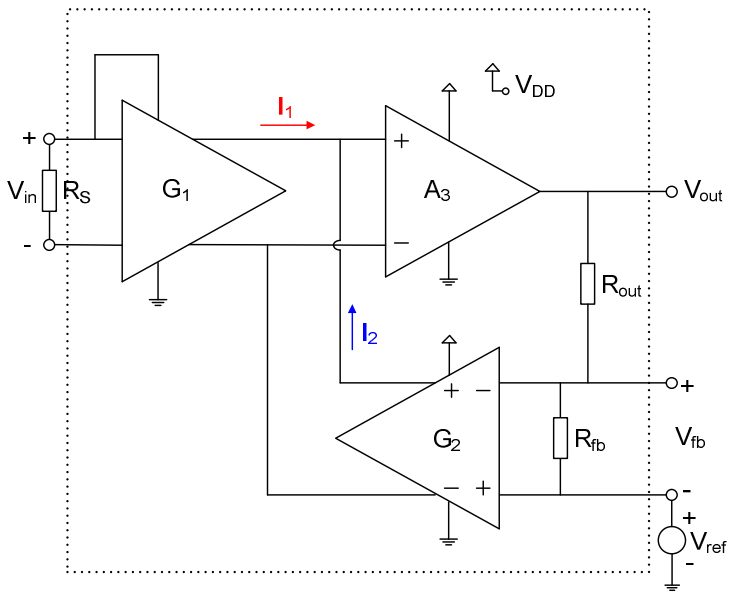


Fig. 2.6 An indirect current-feedback instrumentation amp

By equating equation (2.6) and (2.7), we get the following:

$$I_2 = G_2 \times \frac{R_{fb}}{R_{out}+R_{fb}}\left(V_{out} - V_{ref}\right) \tag{2.8}$$

Now, let $I_1 = I_2$,

$$\frac{\left(V_{out} - V_{ref}\right)}{V_{in}} = \frac{R_{out} + R_{fb}}{F_{fb}}\left(\frac{G_1}{G_2}\right) \tag{2.9}$$

Some of the advantages of this approach are including isolation of input and output CM (Common-mode) voltages, which implies that the input CM voltage can be lower than the output CM voltage and handling of bidirectional currents. However, a shortcoming of the topology could be that its offset is the sum of the offsets of both G_1 and G_2. Also, high complexity of chopping and auto-zero paths with nested miller compensated op-amp blocks and not covering the lower rail around 0V are some of the potential problems of this topology.

2.3.2 A CMOS Instrumentation Amplifier with 600nV Offset, 8.5nV/$\sqrt{Hz}$ Noise and 150dB CMRR

Shown in Fig. 2.7 is a simplified signal chain of the presented prior art. In this design is used a band pass filter based residual ripple reduction technique. The following equation (2.10) shows the optimal Q factor for the designed band pass filter (BPF).

$$Q_{opt} = \sqrt{\frac{1}{8\varepsilon}} \quad , \varepsilon = \frac{f_{chop}-f_0}{f_0} \tag{2.10}$$

where f_0 is BPF center frequency.

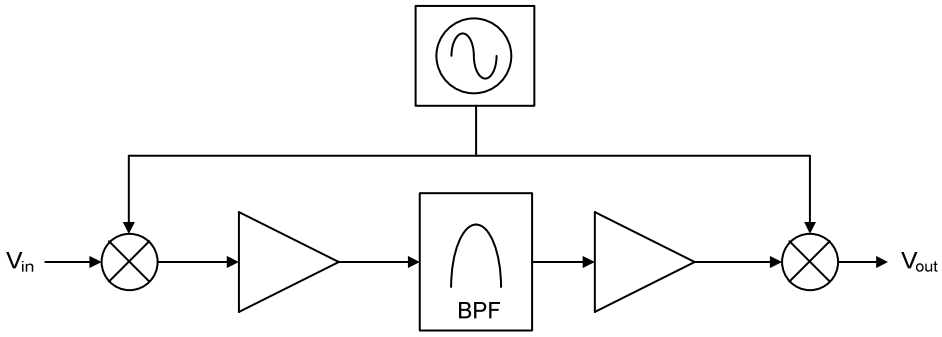


Fig. 2.7 Block diagram of the instrumentation amp

Cancellation of the residual ripple at every ripple frequency can be directly performed by applying a BPF. However, the required high Q of the BPF introduces gain inaccuracies if there is a mismatch between f_{chop} and the center frequency, ω_o, of the BPF. Also, it does not function over the input rail-to-rail operation which in many cases is a requirement of applications.

2.3.3 A CMOS Nested-Chopper Instrumentation Amplifier with 100-nV Offset

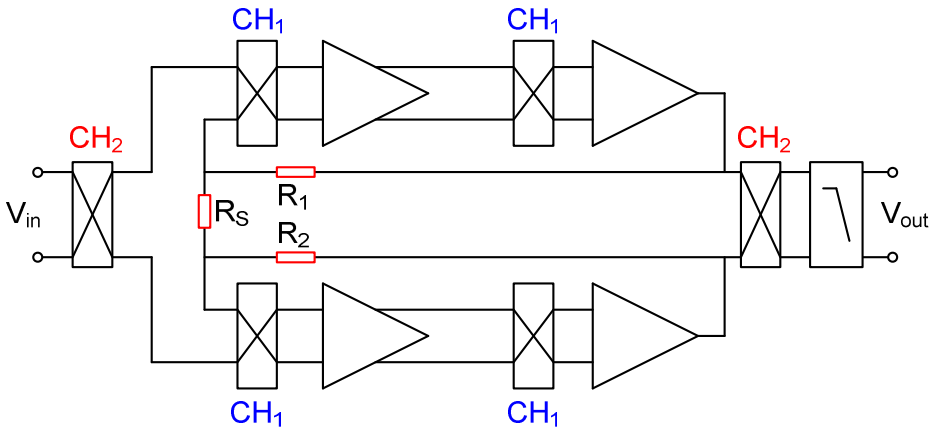
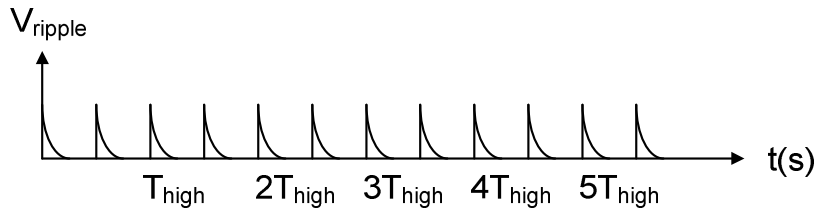
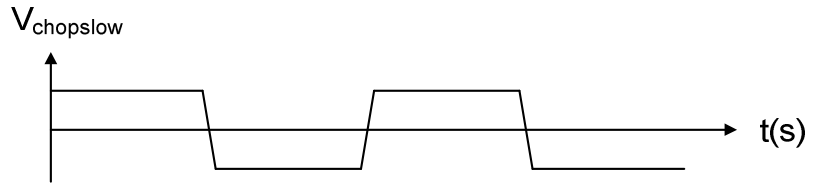


Fig. 2.8 Nested chopper instrumentation amp

Shown in Fig. 2.8 is a signal chain of the nested chopper based chopping ripple reduction technique. The architecture embedded two sets of choppers; one inside and the other surrounding the pairs from the outside. This technique can reduce down the fast clocking chopping (CH_1) ripple by averaging it with slower clocking chopping (CH_2) modulator signal.



(a)



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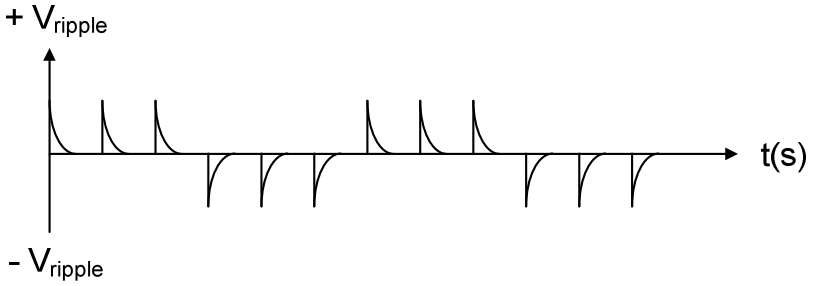


(c)

Fig. 2.9 (a) Residual offset of faster chopper (CH_1) (b) wave form of slower chopper (CH_2) and (c) modulated residual ripple after passing through both CH_1 and CH_2

Fig. 2.9 shows the mechanism and the resulting waveforms at each stage of nested chopping residual ripple reduction technique accordingly. One set of choppers (CH_1) is clocking faster than the other set (CH_2). The faster clocking sets of chopper modulate and demodulate the input dc-offset such as flicker noise as normal sets of choppers are operating. The Additional sets of outside chopper that have slower chopping frequency ($f_{chopslow}$) cancel out the ripples occurring from the original fast chopper by alternating the insider chopper's ripple as shown in clock sequence on Fig. 2.9 (b). However, a possible shortcoming of this topology is that the maximum input signal frequency is limited to half of $f_{chopslow}$.

3 BASIC PRINCIPLE OF CHOPPER STABILIZATION

Chopper stabilization (CHS) is a modulation technique that can be used to reduce the effects of op amp imperfections such as noise (mainly due to flicker and thermal noise of input devices, input pair mismatch, and etc.) and input referred dc offset voltage. This technique was first developed by Edwin A. Goldberg in 1949. There are other techniques that can reduce the input referred offset such as auto-zeroing (AZ), and correlated double sampling (CDS) which can be regarded as a particular case of AZ. While AZ uses sampling technique for operation, CHS employs modulation base operation technique. Since AZ and CDS suffer from noise folding issue due to its sampling nature, CHS does not suffer from the issue, which results in better performance in terms of in referred offset level.

3.1 Basic Theory

The CHS technique uses an AC carrier to get an AC signal from DC by modulating the input signal. Fig. 3.1 shows the principle of chopper amplification. The clock signals $m_1(t)$ and $m_2(t)$ in the figure are modulating and demodulating carriers (clock signal for the transmission switches) with period $T=1/f_{chop}$, which in other words is the chopper frequency. V_{OS} and V_N denote deterministic dc offset and noise (mainly flicker), respectively. In this configuration is assumed that the input signal is band-limited to half of the chopper frequency (f_{chop}), hence no signal aliasing is occurring. Chopper frequency (f_{chop}) is normally selected at significantly higher frequencies where there is no 1/f noise.

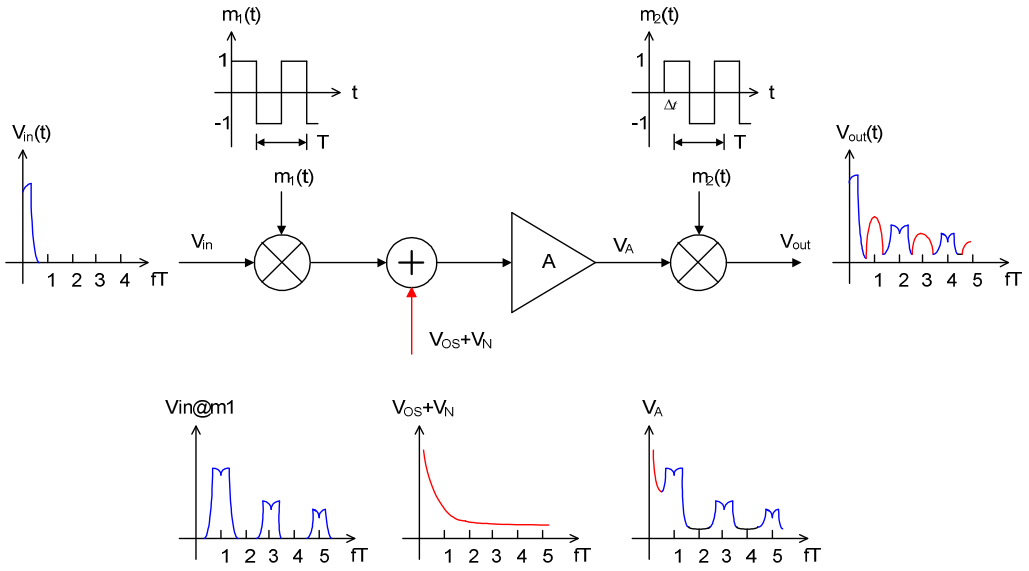


Fig. 3.1 Principle of chopper amplification

Amplitude modulation is performed by using a square wave signal (carrier) which transposes the signal and the noise to the each multiple sets (even and odd multiples) of chopper frequency. For the periodic carrier with a period of T and 50% duty cycle, its Fourier representation is [32]:

$$m(t) = 2\sum_{k=1}^{\infty} \frac{sin\left(\frac{k\pi}{2}\right)}{\left(\frac{k\pi}{2}\right)} \cos\left(2\pi f_{chop} kt\right) \tag{3.1}$$

Since the k-th Fourier-coefficients, M_k of the above equation 3.1 has the following property as

$$M_0 = M_{\pm 2} = M_{\pm 4\ldots} = 0 \tag{3.2}$$

The resulting modulated signal that is shown as V_{in} at m_1 (t) in Fig. 3.1 is transposed to the odd harmonic frequencies of the modulating signal. Once modulation and amplification are done, the signal is then demodulated by multiplying m_2 (t) to obtaining the following:

$$V_d(t) = 4AV_{in}(t)\sum_{k=1}^{\infty}\frac{sin\left(\frac{k\pi}{2}\right)}{\left(\frac{k\pi}{2}\right)}\cos\left(2\pi f_{chop}kt\right)\sum_{l=1}^{\infty}\frac{sin\left(\frac{l\pi}{2}\right)}{\left(\frac{l\pi}{2}\right)}\cos\left(2\pi f_{chop}lt\right) \quad (3.3)$$

Since the signal obtained through the equation (3.3) contains harmonic contents at multiple chopper frequencies as shown in Fig. 3.2, the demodulated signal is generally applied to a low pass filter with a cut-off frequency slightly above the input signal bandwidth to recover the original signal in amplified form. Shown in Fig. 3.2 is the Fourier transform of the noiseless demodulated output signal with loss pass filter signal applied on top of the demodulated signal at half of the chopper frequency. While the input signal is being modulated and demodulated accordingly, noise and offset are modulated only once. If $S_N(f)$ denotes the power spectral density (PSD) of the noise and offset, then the PSD of $(V_{OS} + V_N)m_2(t)$ is [33]

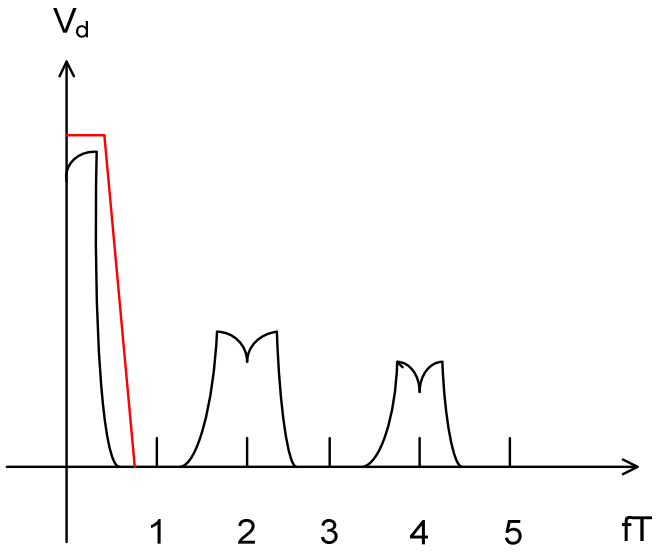
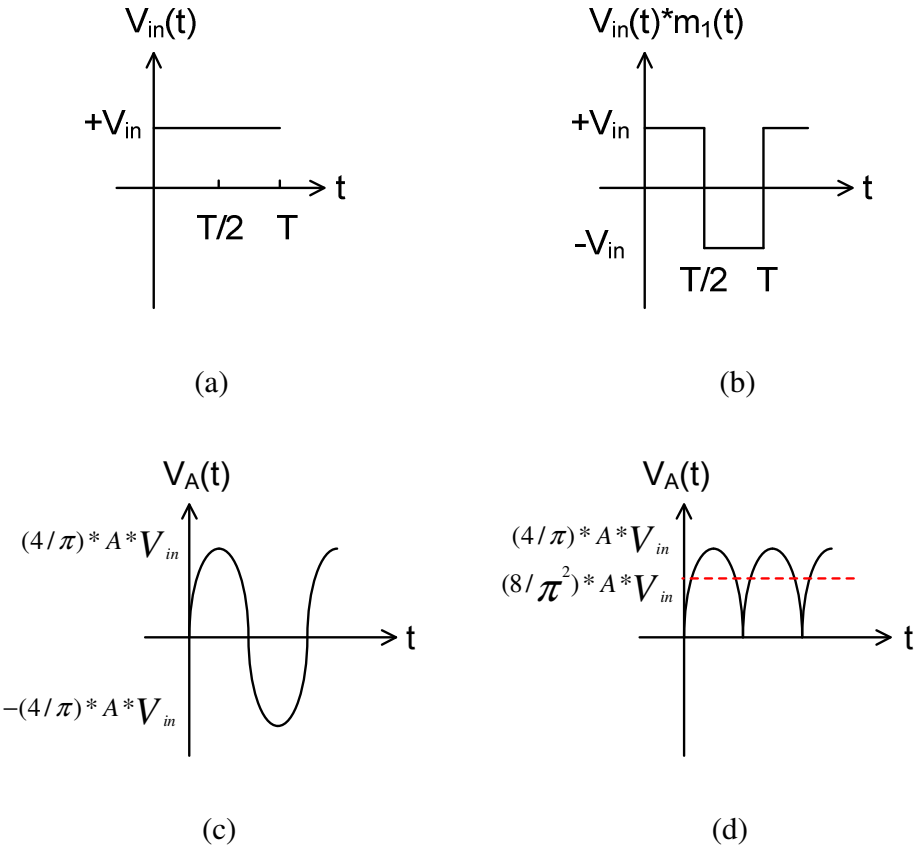


Fig. 3.2 Fourier transform of the ideal noiseless output signal with a low pass filter

$$S_{CS}(f) = \sum_{k=-\infty}^{\infty} |M_{2k+1}|^2 S_N\left(f - \frac{2k+1}{T}\right)$$

$$= \left(\frac{\pi}{2}\right)^2 \sum_{k=-\infty}^{\infty} \frac{1}{(2k+1)^2} S_N\left(f - \frac{2k+1}{T}\right) \quad (3.4)$$

Therefore it is clear that noise and offset are transposed to the odd harmonic frequencies of the modulating signal as shown in the equation (3.4), which is leaving the chopper amplifier ideally without any offset or low-frequency (flicker) noise.



(a) (b)

(c) (d)

Fig. 3.3 Effect of limited bandwidth of the amplifier on (a) a dc input signal, (b) modulation signal, (c) amplified signal after modulation, and (d) low pass filtered output signal after demodulation

Assuming the input signal V_{in} is a dc (at a frequency much lower than the chopper frequency) signal, if the amplifier is ideal that in other words means infinite gain bandwidth with no delay, the signal V_A is simply the square wave with an amplitude $A \cdot V_{in}$ and the signal after demodulation is also a dc signal as $A \cdot V_{in}$. In reality, the amplifier would normally have limited bandwidth and propagation delay. Assuming the amplifier has a bandwidth of twice of the chopper frequency with a constant gain of A and zero elsewhere (ideal low pass), the amplifier output signal $V_A(t)$ is now a sine wave corresponding to the fundamental component of the chopped dc signal with an amplitude $(4/\pi)(A \cdot V_{in})$ [27] as shown in Fig. 3.3. Consequently, the output V_{out} as depicted in Fig. 3.3(d) of the demodulator is a rectified sine wave containing even-order harmonic frequency components [34]. Again, the output should be low pass filtered to recover the desired amplified signal.

Finally, delay introduced by the main amplifier could also degrade overall dc gain. Assuming the amplifier has an infinite bandwidth but introduces a constant delay of T/4 while the input and output modulators are in phase, the output signal would be a chopped cosine wave without a dc component and containing only odd harmonics. Therefore, the overall dc gain of the chopper stabilized amplifier would be zero. If there is the same constant delay between the input and output modulators, i.e., Δt in Fig. 3.1 equals to T/4, the output signal is a rectified sine wave. In conclusion, the phase shift between the two modulators needs to match precisely with the phase shift introduced by the main amplifier in order to maximize the dc gain of the chopper amplifier [27].

3.2 Noise Analysis due to Chopping

Generally, there are two types of noise sources that corrupt analog signals processed by integrated circuits. One is device electronic noise and the other is environmental noise. The environmental noise in other words refers to random disturbances that a circuit experiences through the supply or ground lines or through the substrate in practical system applications [35]. On the other hands, electronic noise refers more to the intrinsic noise that is mainly occurring due to the characteristics of the material [36]. More specifically, the electronic noise can be divided into two parts: thermal and flicker noises. While each noise source shows different characteristics over frequency, the effect of chopping on both thermal (white) noise and flicker noise is analyzed in the following section.

3.2.1 Chopping Noise Effect on Amplifier

Shown in Fig. 3.4 is the plot of power spectral density (PSD) for both flicker and thermal (white) noise on the same axes.

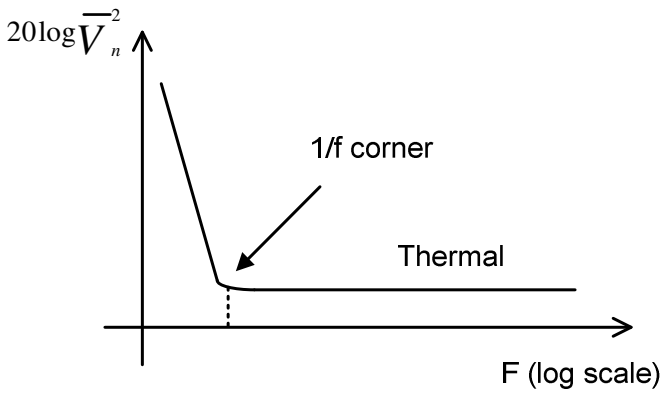


Fig. 3.4 Concept of flicker noise corner frequency

Let f_c be the cut-off frequency of the main amplifier drawn in Fig. 3.1. The corner frequency depicted in the figure serves as a measure of what part of the band is mostly corrupted by flicker noise [37].

In general, the definition of cut-off frequency widely used is the frequency for which the transfer function magnitude is decreased by the factor of $1/\sqrt{2}$ from its maximum value [38]. More precisely, the 1/f noise corner, f_c, of the output current can be determined as

$$4kT\left(\frac{2}{3}gm\right) = \frac{K}{C_{ox}WL}\cdot\frac{1}{f_c}\cdot {g_m}^2 \tag{3.5}$$

that is,

$$f_C = \frac{K}{C_{ox}WL}g_m\frac{3}{8kT} \tag{3.6}$$

The effect of the chopper modulation on the amplifier noise can be analyzed as in Fig.3.5 where $V_N(t)$ is the noise and m(t) the carrier signal. The bilateral PSD of the chopped output signal $V_{CS}(t)$ is given as

$$S_{CS}(f) = \left(\frac{\pi}{2}\right)^2 \sum_{\substack{n=-\infty \\ n\,odd}}^{+\infty}\frac{1}{n^2}S_N\left(f-\frac{n}{T}\right) \tag{3.7}$$

In baseband ($|f| \le 0.5f_{chop}$), S_{CS} in equation 3.4 can be approximated by a white noise PSD as in the following:

$$S_{CS-white}(f) = S_{CS-white}(f=0) = S_0\left[1-\frac{\tanh\left(\frac{\pi}{2}f_cT\right)}{\frac{\pi}{2}f_cT}\right] \tag{3.8}$$

Assuming an amplifier cut-off frequency f_c equal to five times the chopper frequency 1/T, and for $f_c >> f_{chop}$, $S_{CS\text{-}white}$ can be further approximated to

$$S_{CS-white}(f) \cong S_0 \quad for \quad |f| \le 0.5f_{chop} \; and \; f_c \gg f_{chop} \tag{3.9}$$

Therefore it is possible to say that the baseband PSD of the noise is nearly

constant for large f_c of the amplifier. Unlike auto-zeroing (AZ) technique, the chopper modulation does not introduce aliasing of the broadband noise, which for AZ causes the PSD in the baseband to increase proportionally with the ratio of the noise bandwidth and the sampling frequency [39].

As shown in equation (3.8), the baseband PSD resulting from the chopper modulation is nearly constant, and it tends to be same as the value of the input white noise S_0 for a large f_cT. This is because of that the noise is not sampled nor held, just periodically inverted without changing the general properties of the noise in the time domain. Although the chopper modulator output PSD results from a summation as for a sample and hold (S/H) process, in the chopper modulation the replicas are multiplied by $1/n^2$, making their contribution to the baseband decrease very rapidly [27].

For 1/f noise, the input PSD can be described as

$$S_{N-\frac{1}{f}}(f) = S_0 \frac{f_k}{|f|} \tag{3.10}$$

where f_k is the amplifier corner frequency. Substituting the PSD in eq. 3.10 into eq. 3.2, the low frequency noise is translated into higher frequencies, which in other words means that the 1/f noise pole disappears from the baseband.

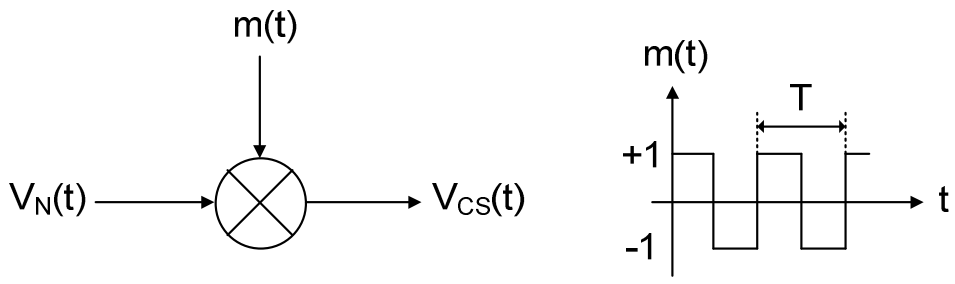


Fig.3.5 Chopper modulation

Simulation shows that the chopped 1/f noise PSD in baseband can be approximated by [27]

$$S_{CS-\frac{1}{f}}(f) = 0.8525 S_0 f_k T \tag{3.11}$$

Finally, the total input-referred residual noise in the baseband for a typical amplifier can now be defined by summing the equation (3.9) and (3.11).

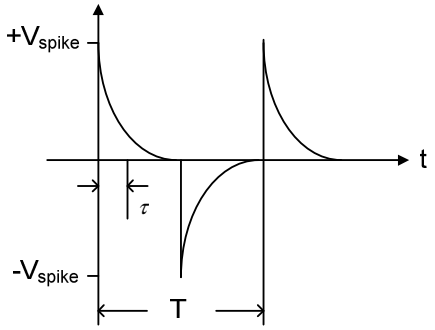
$$S_{CS}(f) = S_0(1 + 0.8525 f_k T) \;\; for \;\; |f| \leq 0.5 f_{chop} \;\; and \;\; f_c \gg f_{chop} \tag{3.12}$$

Therefore, it is reasonable to choose the chopper frequency (f_{chop}) equal to the amplifier corner frequency (f_k). The resulting noise PSD increase is less than 6dB [27].

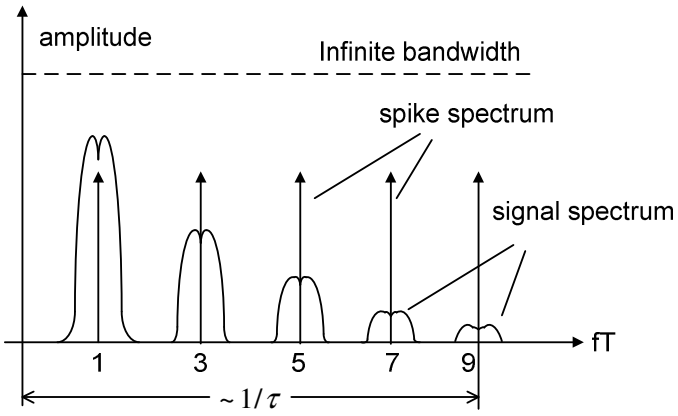
3.2.2 Chopping Noise Effect on Residual Offset

Since the modulators are realized with MOS switches in most of the cases, it suffers from both charge injection and clock feed-through. Charge injection is known as that the remaining charges exit through the source and drain terminals every time the switch turns off. Clock feed-through is occurring due to the result of the coupling between control signals on the analog switch and analog signal passing through the switch. Such coupling happens because of the gate-to-source capacitance, interconnects parasitic capacitance or because of the substrate coupling [27]. The non-idealities cause spikes at the input of the main amplifier. The spikes (residual offset voltage) being located input of the amplifier will be amplified then modulated by the output modulator. Shown in Fig. 3.6(a) is a typical spike signal in time domain where τ represents the time constant of the generated (parasitic) spikes, T is the chopper clock period. Since only the odd

harmonics of the chopper frequency contributes to the final residual offset as explained in earlier chapter, the spike signal has an odd symmetry. Since the time constant τ normally has much smaller value than the half of the chopper clock period T/2, the energy of the spike signal tend to be concentrated at frequencies higher than the chopper frequency. Shown in Fig. 3.6(b) are the spectra of the spikes and the chopper-modulated signal that are located at the input of the main amplifier.



(a)



(b)

Fig. 3.6 (a) Spike signal at the input of the amplifier (b) spectra of spike signal of chopper modulated signal with amplifier bandwidth characteristics

The input-referred offset from the spectra can be calculated as following [27].

$$V_{OS} \cong \frac{2\tau}{T} V_{spike} \tag{3.13}$$

As discussed in the earlier section, a maximum dc gain A_V can be achieved by using an amplifier with a bandwidth much higher than the chopper frequency, f_{chop}. However, using a wide bandwidth amplifier also results in a maximum output offset voltage because almost all of the spectral components of the spike signal will also contribute by transferring through the wide bandwidth amplifier. Therefore, a good design compromise is to limit the bandwidth of the amplifier to twice the chopper frequency. The overall dc gain resulted will be

$$(8/\pi^2) \cdot A_V = 0.81 A_V \tag{3.14}$$

The equation shows only 19% degradation of dc gain while the offset voltage is reduced drastically as [27]

$$V_{OS} \cong \left(\frac{2\tau}{T}\right)^2 V_{spike} \tag{3.15}$$

3.3 Techniques to Reduce Residual Offset

As mentioned in previous section, residual offset mainly caused by charge injection of MOS switches. On top of the channel charge injection, the most important factors affecting residual offset are the following:

- clock feed-through
- sampled noise
- leakage current

Channel charge injection and clock feed-through related residual offset cancelling approaches will be discussed in this section. Fig. 3.7 shows a cross-section of a transistor. As shown in the figure, when the transistor is on, charge forms under the gate to create a channel for current (I_d) to flow. When the transistor turns off, this charge has to go somewhere.

In general, defining where the charge goes (how it divides between the two sides of the transistor) is an extremely complex function of the relative impedances on either side of the switch, the transistor type, the relative voltage levels on either side of the switch and the fall time of the gate voltage. In general, since $\Delta V = \Delta q/C$, using a small switch and a larger capacitance will help.

However, if the switch is too small and the capacitor is too large, the required charge transfer will not have time to complete. Also, more power is required to drive large capacitance as well. A simple MOS switch can be drawn as in Fig. 3.8. C_h corresponds to the total capacitance at the switch drain (the hold capacitor) and C_p corresponds to the total parasitic capacitance at the source.

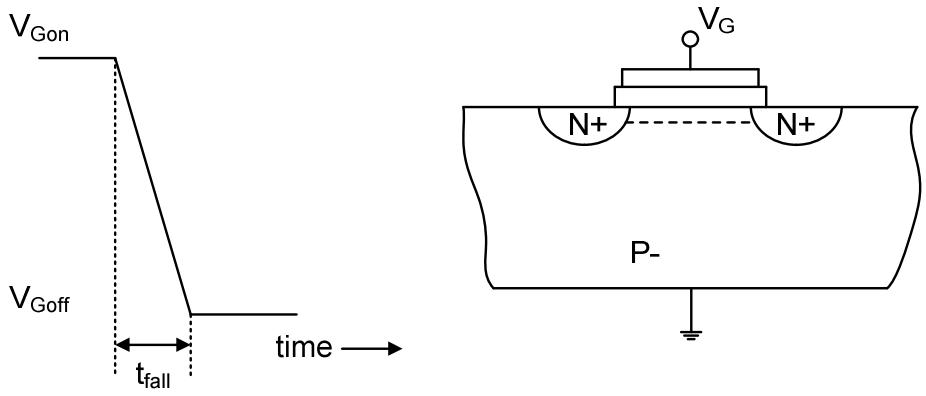


Fig. 3.7 A cross-section of a MOSFET transistor

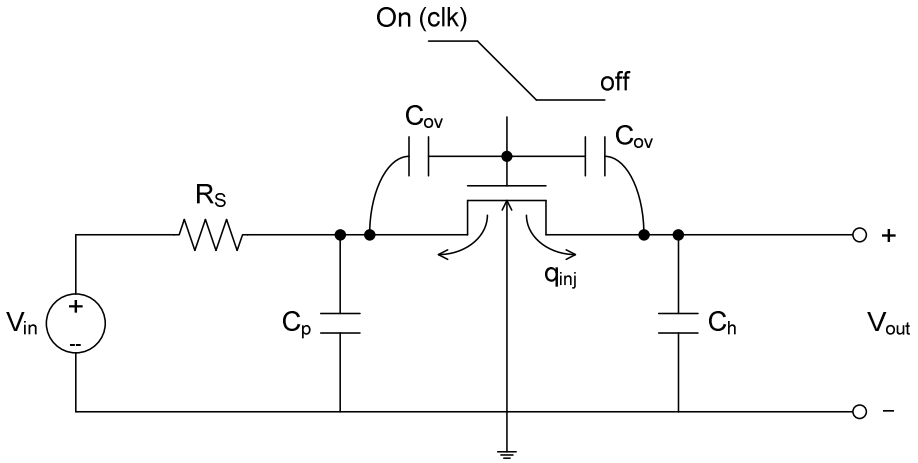


Fig.3.8 Basic MOS switch

Although it is a complex function to solve where the charge ends up distributed, whichever say the charge goes, some of it ends up on C_h and causes an error in the voltage that has been sampled on to C_h.

Besides increasing the size of hold capacitance and minimize the size of the MOSFET switch, there are many well known techniques of reducing residual offset caused by charge injection. Some of the basic approaches will be discussed in the following sub-sections.

3.3.1 Using Complementary Switches

One of the simplest conventional approaches is to use complementary switches instead of using a single type of MOSFET switch. The basic theory of this approach is that the charges released by one switch are absorbed by the complementary switch to build its channel. In reality, it is difficult to match precisely channel charges of an n-MOSFET device and a p-MOSFET device.

Therefore insertion of a half sized dummy switch between the drain of the switch and the hold capacitance, C_h would help to recover the net charge transfer as zero. However, phase jitter between the two complementary clocks further degrades the charge mismatch [27].

3.3.2 Using Larger Capacitance

Another efficient way of reducing the charge injection is to make C_p (total parasitic capacitance at the source side) much larger than C_h (total capacitance at the switch drain side) and choose a slow clock transition. Most of the channel charges will be attracted to the larger capacitor C_p, leaving almost zero charges to C_h on the output side. A main drawback of this approach is that it sets a limit on the maximum clock frequency [27].

3.3.3 Fully Differential Structure

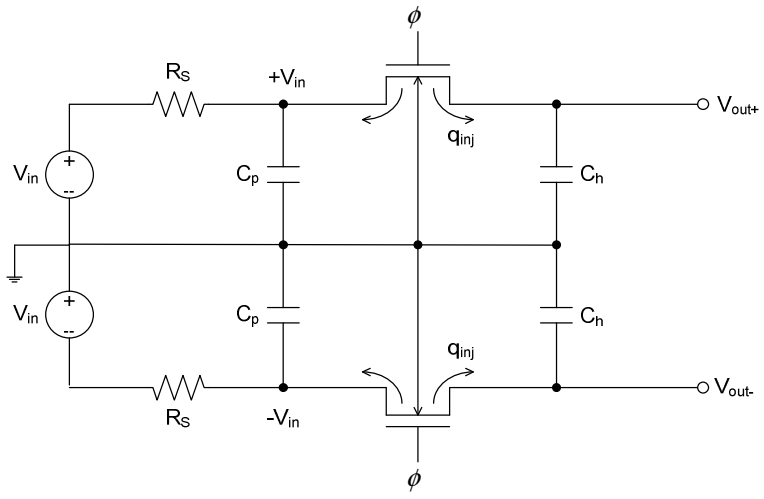


Fig.3.9 Fully differential structure

By purposely setting $C_p = C_h$, which in other words means that the injected charges to the differential capacitors are matched, the resulting voltage appears as a common-mode voltage and is rejected. Shown in Fig. 3.9 is an example of a fully differential structure. This technique usually requires the generation of delayed-cutoff clock phases [27].

3.3.4 Using Multistage Cascading

Another conventional approach of reducing the offset caused by switch charge injection is cascading several single-stage amplifiers to achieve high gain and speed. Shown in Fig. 3.10 is a sample circuit of cascading stages with corresponding switches. In the offset sampling phase, the negative inputs of all the simplifiers are connected to ground. Switch S1 is opened first to inject some charge into capacitor C_1, which results in an error voltage appearing at the negative input of the second amplifier. This error voltage can be viewed as a change in the input-referred offset voltage of the second amplifier. This offset ends up being cancelled along with V_{OS2}. Switches S_1, S_2, …, S_N are opened successively. The effective offset voltage is only determined by charge injection of switch S_N into capacitor C_N in the last stage because the offset voltages at earlier stages get cancelled.

The equivalent input-referred offset is [27]

$$V_{OS} = \frac{1}{A_1 A_2 \ldots A_N} \cdot \frac{q_{inj-N}}{C_N} \tag{3.16}$$

where q_{inj} is the injected charge. This offset voltage is much smaller than that obtained for a single-stage low-gain amplifier.

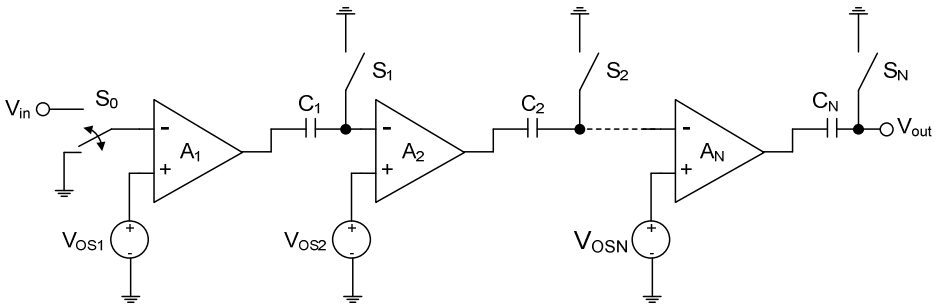
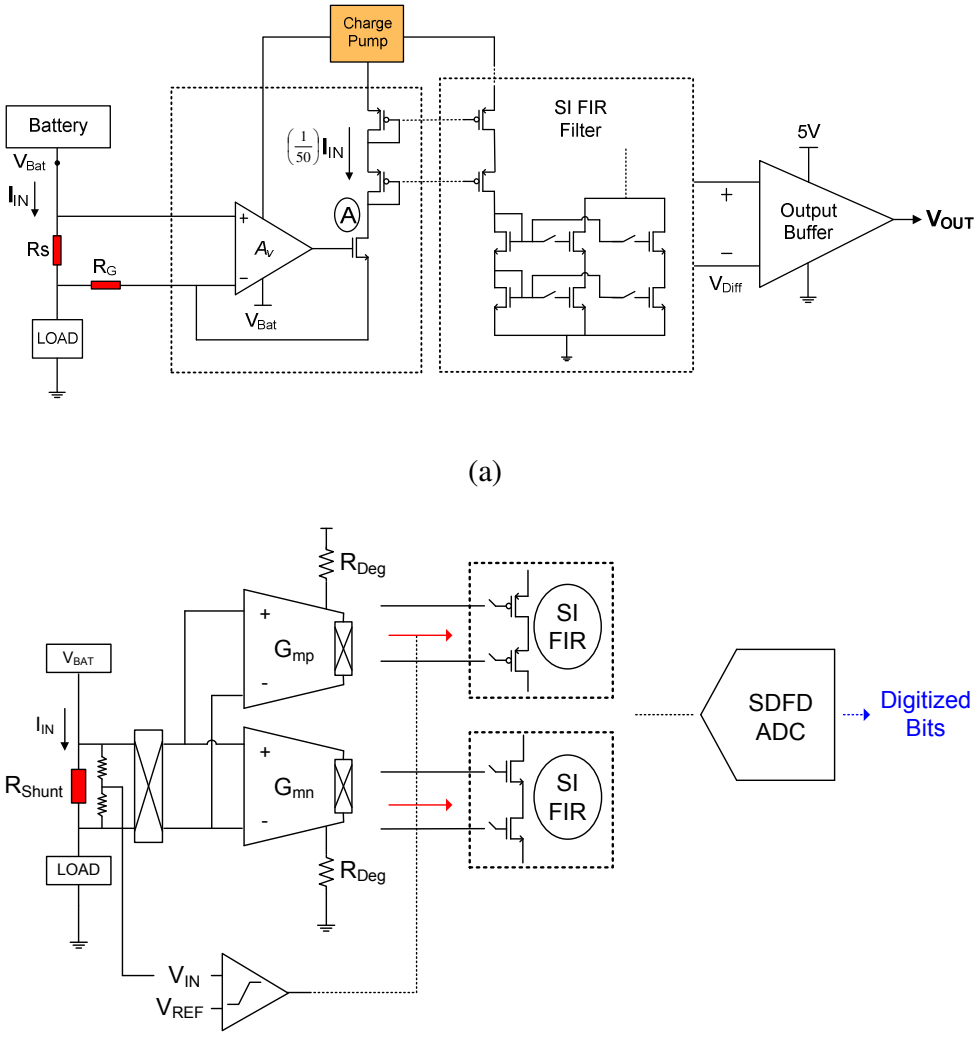


Fig.3.10 Multistage offset cancellation circuit

4 CURRENT SHUNT MONITOR DESIGN

As mentioned earlier, two current shunt monitors (CSMs) shown in Fig. 4.1 based on different topologies have designed and fully characterized through the following chapters.



(a)

(b)

Fig. 4.1 (a) Direct current reading method and (b) Indirect voltage to current conversion method

First topology depicted in Fig. 4.1(a) is based on direct current reading method which intakes a portion set by the ratio of R_S and R_G of the sensed input current to read the actual sensed amount. Second topology depicted in Fig. 4.1(b) is based on indirect current reading method which converts sensed input voltage drop that is proportional to the sensed input current through a source degenerated transconductance (gm) stage.

The design target is specified in TABLE 4.1.

TABLE 4.1

Design Target Specifications

	Input			Output			Power
Parameter	ICMR	CMRR	Offset	Gain	Gain Error	Non-linearity Error	Current
Condition				V_{sense} = 1mV to 200mV			Quiescent
Target (Max)	0~26 V	120dB	±10μV	250 V/V	±2%	±0.1%	~300uA

4.1 Direct Current Reading Method

Shown in Fig. 4.2 is the completed design and signal flow of the proposed direct current reading CSM. In the proposed approach, voltage drop corresponding to the current flowing through the input sensing resistor (R_S) will be measured by the front-end instrumentation pre-amplifier. A ratio set by R_S/R_G will determine the amount of the current flowing into the CSM block.

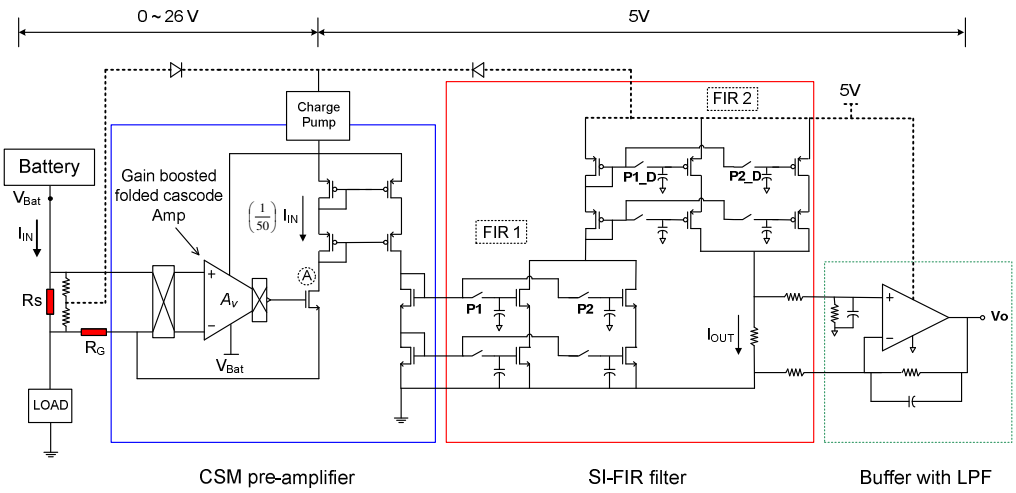


Fig. 4.2 Architecture and completed signal chain of the direct current reading CSM

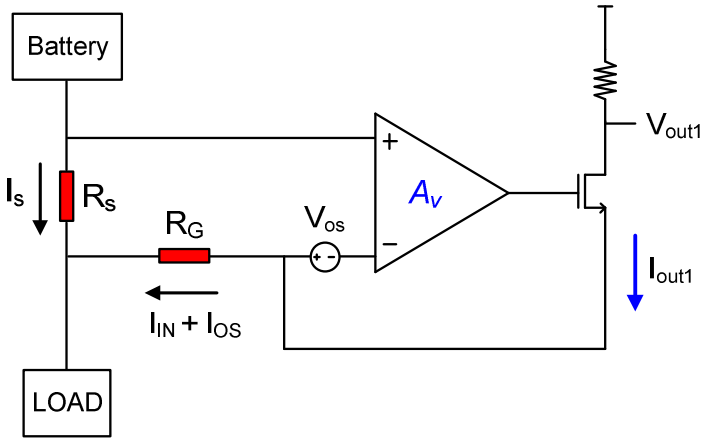
In order to suppress input-referred flicker noise and DC offset, the pre-amplifier uses chopper stabilization at a frequency of 150KHZ which is significantly higher than the flicker noise corner frequency (f_C). Fig. 4.3 shows the concept of how cancellation of the input referred DC offset is performed by applied chopper stabilization. Averaging the output current of phase1 and phase2 cancels the effect of the offset, V_{OS} as

$$I_{out1} = \frac{I_s \cdot R_s}{R_{in}} + \frac{V_{os}}{R_{in}} \tag{4.1}$$

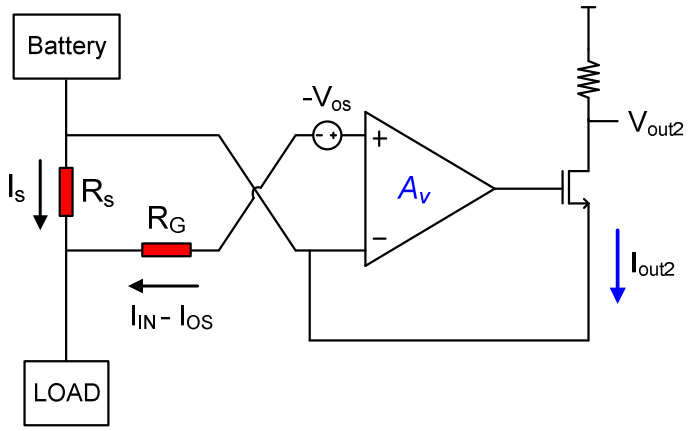
$$I_{out2} = \frac{I_s \cdot R_s}{R_{in}} + \frac{(-V_{os})}{R_{in}} \tag{4.2}$$

By equating equation (4.1) and (4.2), the following will result.

$$I_{avg} = \frac{I_{out1} + I_{out2}}{2} \tag{4.3}$$



(a)



(b)

Fig. 4.3 Showing the concept of cancelling DC offset by two phases (a), and (b) of signals

Shown in Fig. 4.4 is a simulation result that shows plots of the power spectral density (PSD) of the selected process, AMIS I2T100. The plot showing that the flicker domain noise has been lowered after chopping is applied (yellow line labeled as “Chopped”).

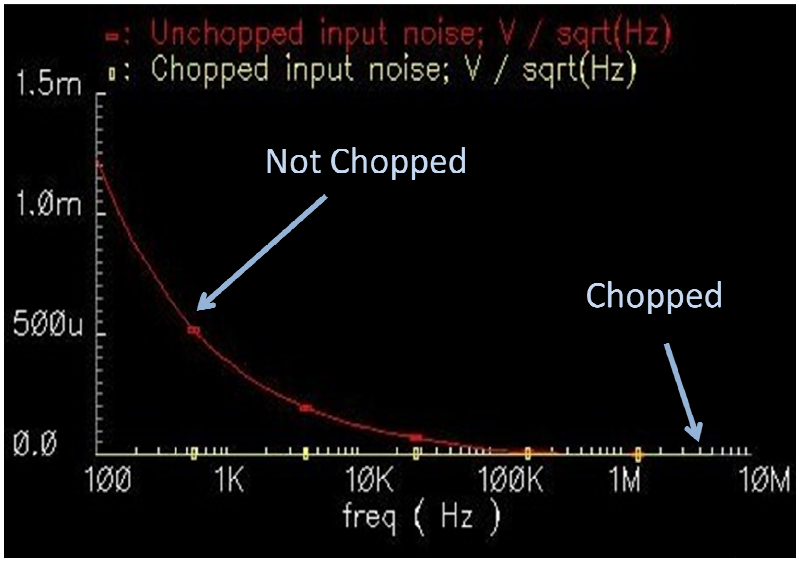


Fig. 4.4 Suppression of flicker noise resulting from chopping

Since the chopped signal has ripples due to input offset and flicker noise, and residual offset due to switch clock feed-through and charge injection that cause amplified spikes at the output of the front-end amplifier at chopping frequency as shown in Fig. 4.5, a switching current mode FIR filter is used in the following stage to suppress the output ripple and residual ripple caused by clock feed-through of the switching Mosfet by taking the average of the two different phases of chopped signal at the chopping frequency.

While averaging performs effective filtering of the chopped ripple signals, in the frequency domain, this is equivalent to notch filtering at integer multiples of chopping frequency, which notches out the harmonic contents of ripples and residue. Fig. 4.6 shows the sequential signal flow and resulting offset and chopping ripple cancellation of the proposed design in both frequency and time domain.

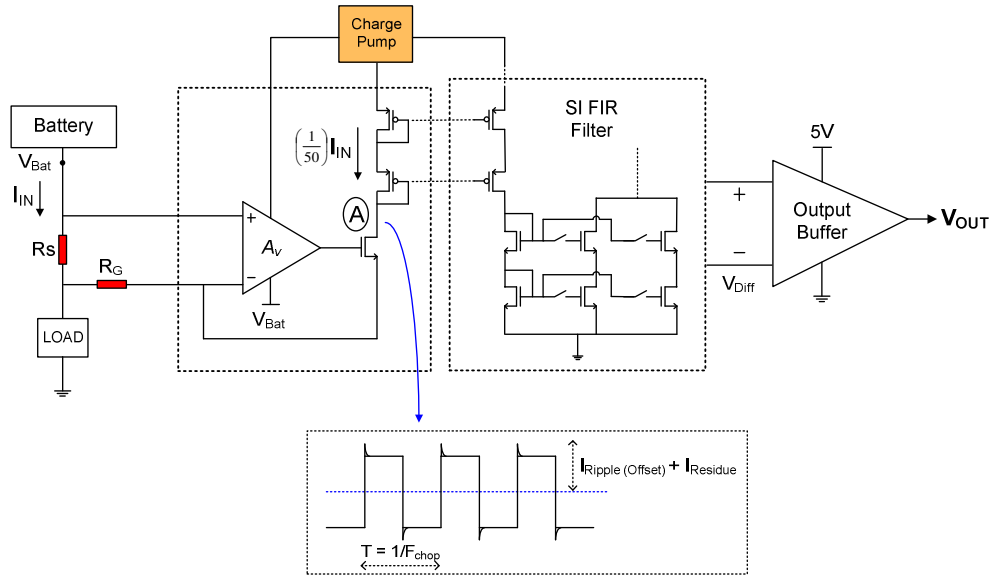


Fig. 4.5 Current ripple (offset) and residual offset after chopping

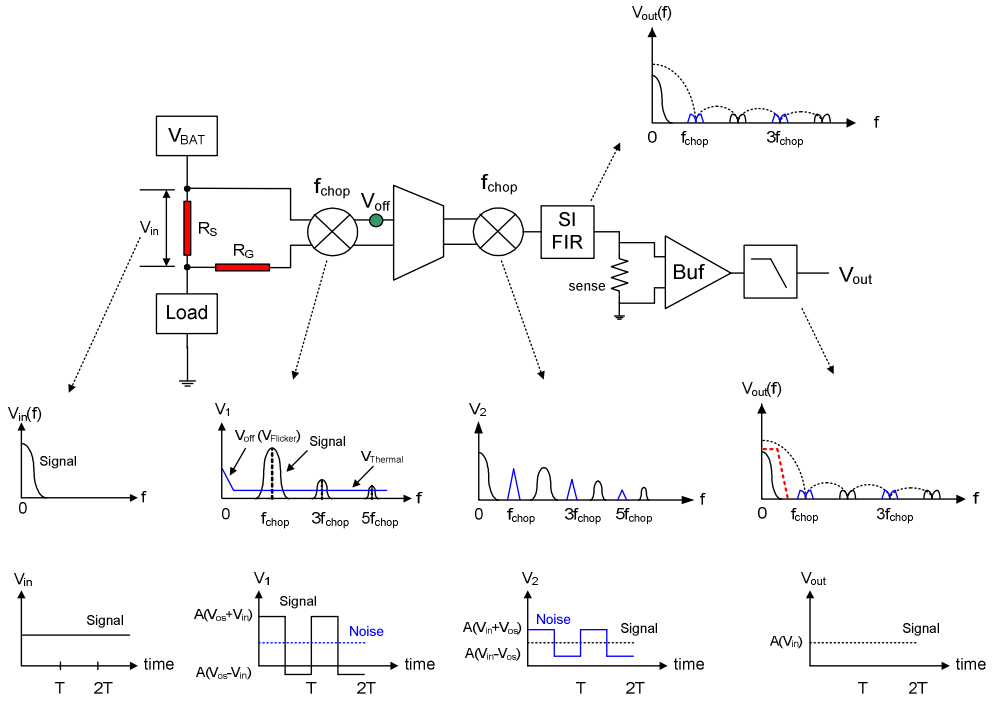


Fig. 4.6 Signal flow of the proposed design in frequency and time domain

4.1.1 Building Block Analysis

Each building blocks of the first architecture (direct current reading CSM) is described in detail through the following sections.

4.1.1.1 Matched PCB Cu-Trace Design

In a conventional CSM design, use of an external R_S increases the system cost, and matching of the external R_S to the gain resistor (R_G) as depicted in Fig. 4.1 can cause gain error.

Especially, current sensing in power supplies and motor controls demands the use of a very low value resistor [40]. Instead of using external resistors, the proposed design uses existing PCB Cu-trace in place of the external R_S and R_G in the current path, which leads to elimination of external components as shown in Fig. 4.7. The Cu-trace resistance built as serpent shape to achieve the ratio of R_G/R_S as 50.

The resistance for a piece of metal is given by the equation as a function of temperature [40]:

$$R(T) = \frac{S(T) \cdot L}{a} \tag{4.4}$$

where the units are

R = Resistance, Ω

$S(T)$ = Resistivity, Ω-cm

L = Length, cm

a = Area, cm^2

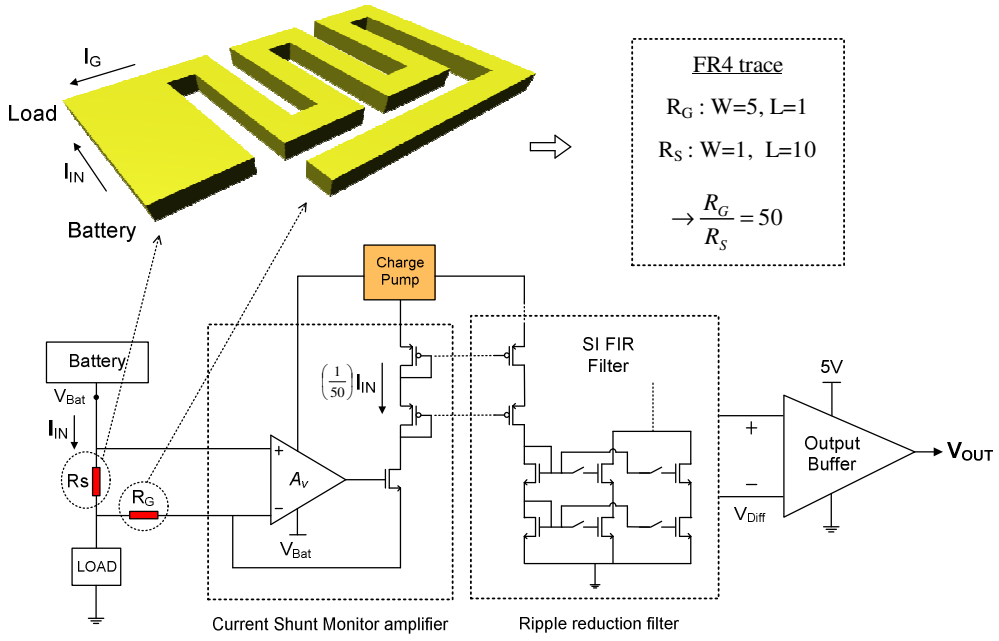


Fig. 4.7 Concept of building two matched Cu-trace resistance on an FR4 board

Electrical resistivity can be defined as

$1.7241 \cdot 10^{-6}\Omega$-cm @ 20°C

Temperature Coefficient of Resistivity is

+0.0039 per °C

in typical case of 99.5% pure Cu.

Finally, the resistivity of copper, as a function of temperature, can be defined as

$S(T)=1.7241 \cdot 10\text{-}6 \cdot [1+0.0039 \cdot (T\text{-}20)]\ \Omega$-cm

where T is the copper temperature in °C. Table 4.2 provides the required dimensions for a 1oz PCB copper resistor given a maximum current and desired voltage drop [40]. Fig. 4.8 shows the actual realization of the resistance on an FR4 PCB. Although the variation of the resistance over temperature is critical for

PCB Cu-trace resistance, the effect of absolute variation is minimal in direct current reading topology because it can be eliminated by using two matched Cu-trace based resistors.

TABLE 4.2

DIMENSION SOLVER FOR GIVEN CURRENT AND DESIRED VOLTAGE DROP FOR 90°C MAXIMUM COPPER TEMPERATURE

AMPS	Desired Voltage Drop			Width [in]
	10mV	25mV	50mV	
	PCB Etch Length [in]			
1	0.162	0.405	0.810	0.010
2	0.243	0.608	1.215	0.015
3	0.405	1.013	2.025	0.025
4	0.648	1.620	3.240	0.040
5	0.891	2.228	4.456	0.055
6	1.053	2.633	5.266	0.065
7	1.377	3.443	6.886	0.085
8	1.701	4.253	8.506	0.105
9	2.025	5.063	10.126	0.125
10	2.430	6.076	12.152	0.150
11	2.754	6.886	13.772	0.170
12	3.078	7.696	15.392	0.190

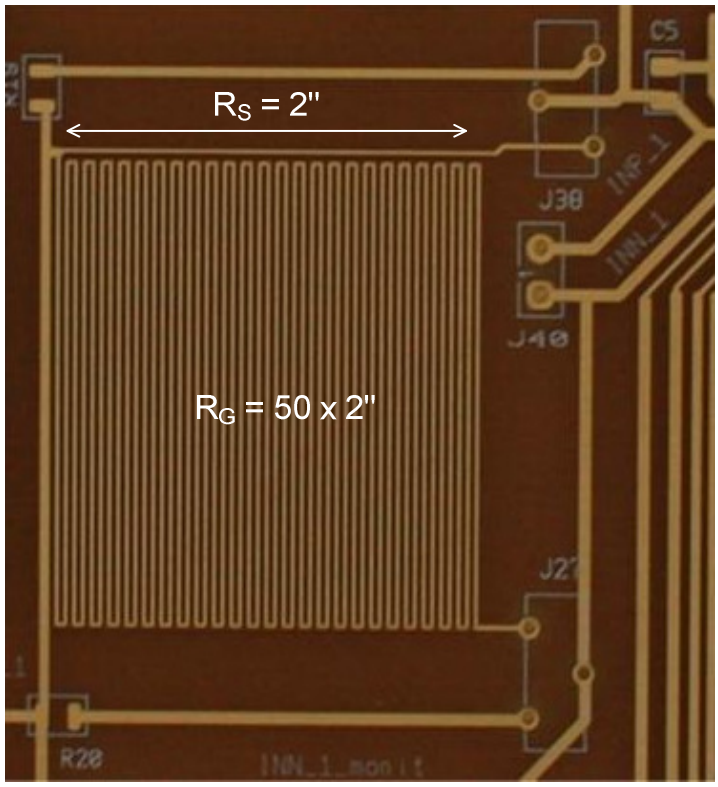


Fig. 4.8 Cu-trace resistance on an FR4 board

In the proposed approach, the input sensing and gain resistors are designed in ratio such that R_G/R_S = 50 by using Cu-traces. Unit length of 2 inches with unit width of 0.9 mils, and thickness of 1.5 mils can yield a unit resistance of 1.08 Ω at 40 °C for R_S as shown in the Fig. 4.8.

The following equation shows an example of how the 1.08 Ω resistance was achieved.

$$The\ resistnace\ at\ 40\ °C = R(40)$$

$$= \frac{1.7241 \cdot 10^{-6}[1 + 0.0039 \cdot (40 - 20)]\left[\frac{\Omega - cm}{°C}\right] \cdot \frac{1000\ mils}{2.54\ cm} \cdot 2000\ mils}{0.9\ mils \cdot 1.5\ mils}$$

$$= 1.08\ \Omega$$

4.1.1.2 Input Instrumentation Amplifier Design

To achieve less than ±1% gain error in the current readout path, the input front-end amplifier uses a gain boosted folded-cascode amplifier with the internal boosting amplifiers also utilizing folded-cascode amplifiers [41]-[42]. Modulation chopper is located at the input of the instrumentation amplifier and demodulation choppers are inserted inside each output current branch of the amplifier as described in Fig. 4.9. The demodulation chopper switches are inserted at the selected nodes because the nodes are low swing nodes. By keeping the ripple cancellation outside the main amplifier loop while achieving a DC gain of 110dB from a gain boosted folded-cascode amplifier, there is no need of using higher order amplifier systems, typically used in CSM applications.

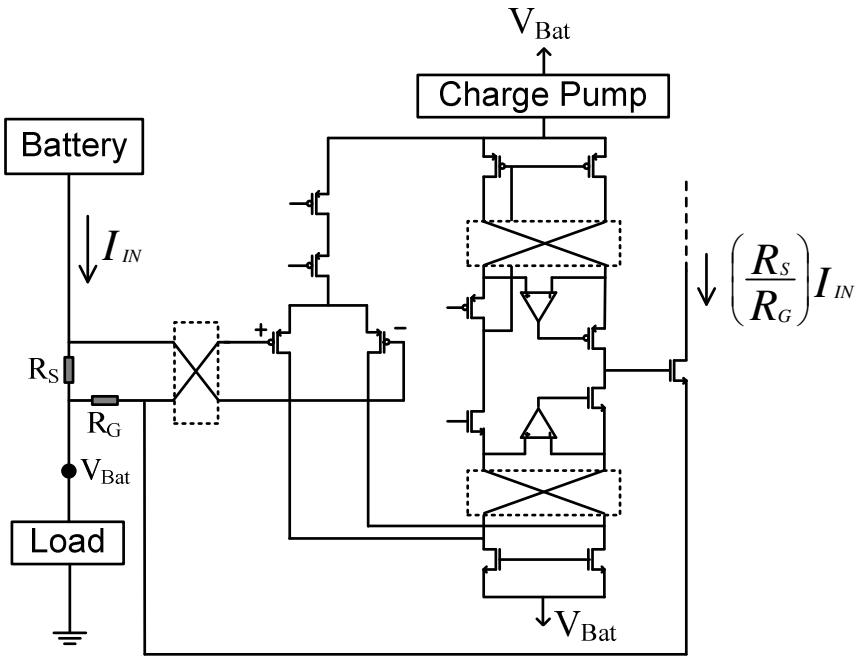


Fig. 4.9 Insertion of the choppers into the signal path

With the use of a single gain boosted amplifier, nested Miller compensation is avoided and the system can achieve a unity gain bandwidth of 300 KHz with a quiescent current consumption of 100μA.

4.1.1.3 Intermediate Amplifier Supply Design

To enable the system operate over the entire common mode input range from 0 to 26V with a single PMOS input paired Operational Transconductance Amplifier (OTA), the system uses a charge pump that boosts sensed input voltage to around 4V above the input voltage. This intermediate rail (boosted voltage) is used as a power supply for front-end amplifier and the incoming common mode voltage (V_{Bat}) used as a ground return path for this front-end stage.

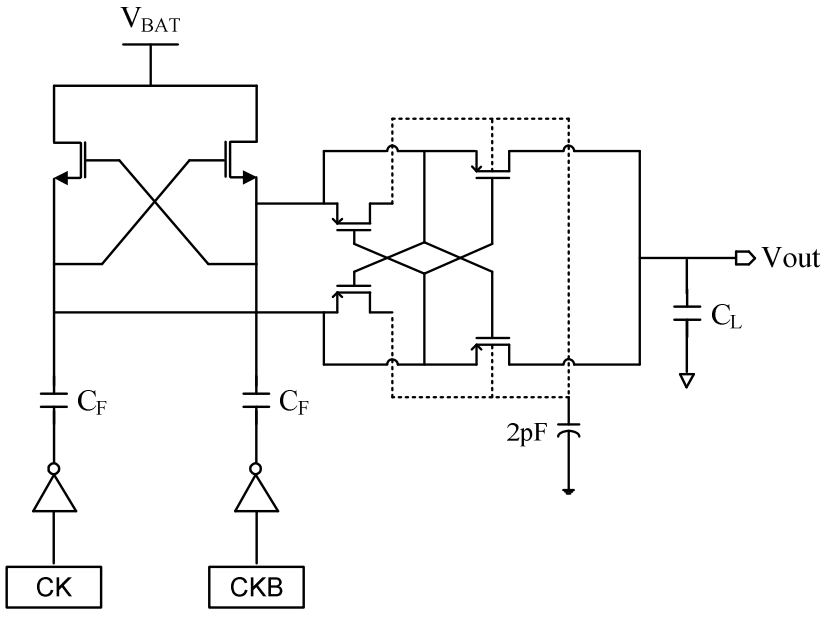


Fig. 4.10 Charge pump to generate the sense amplifier supply voltage

Since the charge pump only needs to maintain approximated voltage around 4V that can keep the front-end amplifier in saturation range and the well characterized load (small current in the range of 100uA) associated with the error amplifier, instead of using fully regulated charge pump topology, the design adopted a simple Dickson charge pump to minimize design complexity and size overhead as depicted in Fig. 4.10 [43]-[44]. Shown in Fig. 4.11 is the conceptual view of the role of the charge pump. Since the power supply ripple (V_R) associated with the charge pump is inversely proportional to the size of the load capacitance C_L, as in

$$V_R = \frac{I_{pump}}{f_{osc} \times C_L} \tag{4.5}$$

where I_{pump} is the pumping current into the flying capacitor (C_F), which is equal to I_{out} in a steady stage [45], the optimal sizes of the passive elements can be resulted as following.

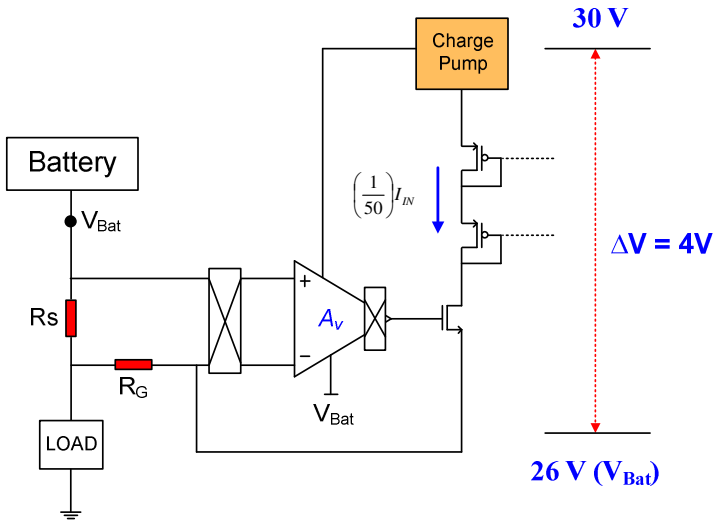


Fig. 4.11 Voltage boosting from the input common mode voltage

Assuming I_{out} equals to 400µA (The amount of current needed to operate the front-end input sensing amplifier stage), charge pump oscillation clock frequency (f_{osc}) at 10MHz with the load capacitance size of 10nF, the resulting voltage ripple at the output of the charge pump will be approximately 2mV as shown in Fig. 4.12.

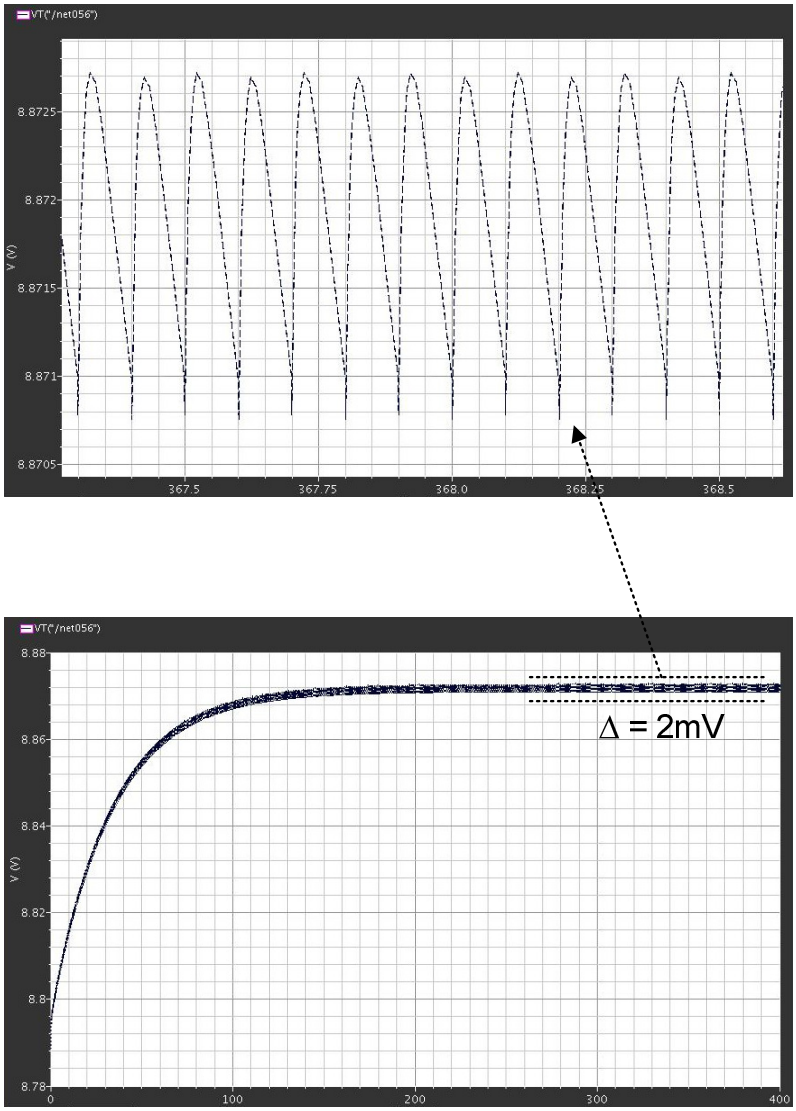
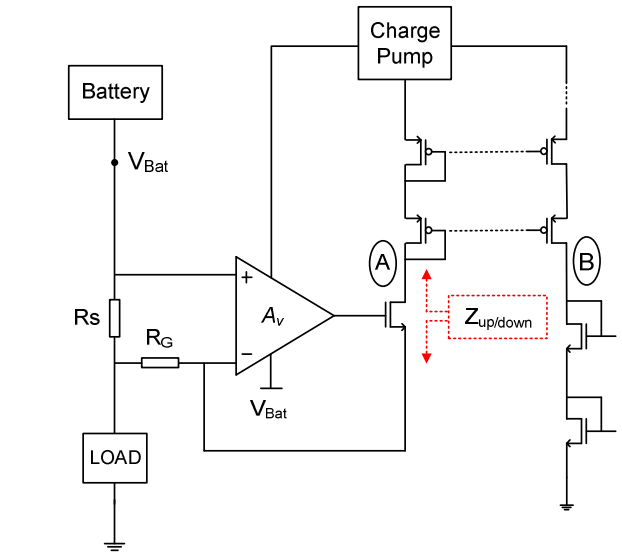
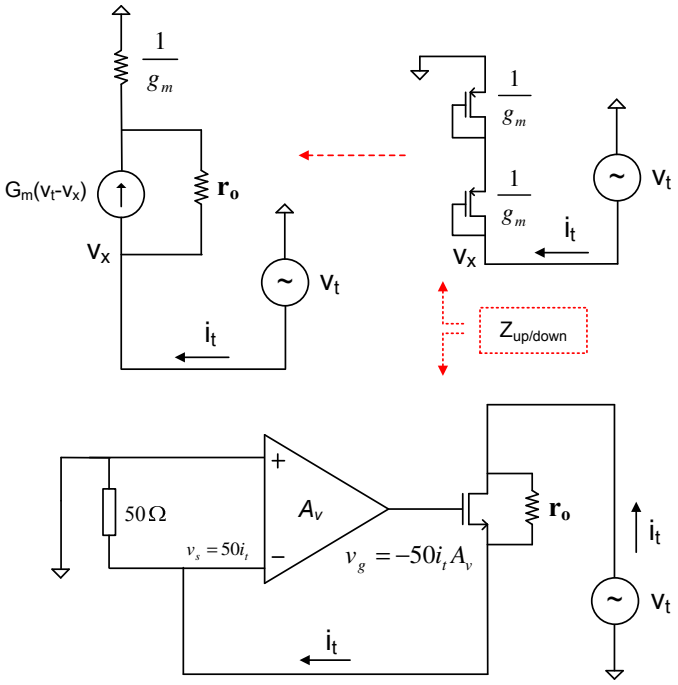


Fig. 4.12 Charge pump voltage fluctuation (ripple)



(a)



(b)

Fig. 4.13 Supply ripple rejection analysis (a) showing the impedance dividing point, and (b) simplified small signal equivalent impedance analysis

Also, the amount of charge injected to the load C_L in one pumping clock cycle can be calculated by the following equation where V_{in2} implying the voltage loss due to the channel resistance of the charge pump switching transistors.

$$Q_{inj} = C_f[V_{in1} - V_{in2}] = C_f[V_{in1} - I_{ch} \times R_{ch}] \quad (4.6)$$

The amount of voltage ripple (noise) due to the charge pump switching as in the equation (4.5) can be effectively reduced down by the resistor divider effect of the proposed architecture as described in Fig. 4.13. Small signal impedance looking down from the point A, represented by Z_{down} is

$$Z_{down} = \frac{v_t}{i_t} = r_o + 50 + 50 g_m r_o A_v \cong 400M\Omega \quad (4.7)$$

In the same manner, the following approach can be used to calculate impedance looking up (Z_{up}).

$$z_{up} = \frac{v_t}{i_t} = \frac{2}{g_m + g_o} \cong \frac{2}{g_m} \cong 20K\Omega \quad (4.8)$$

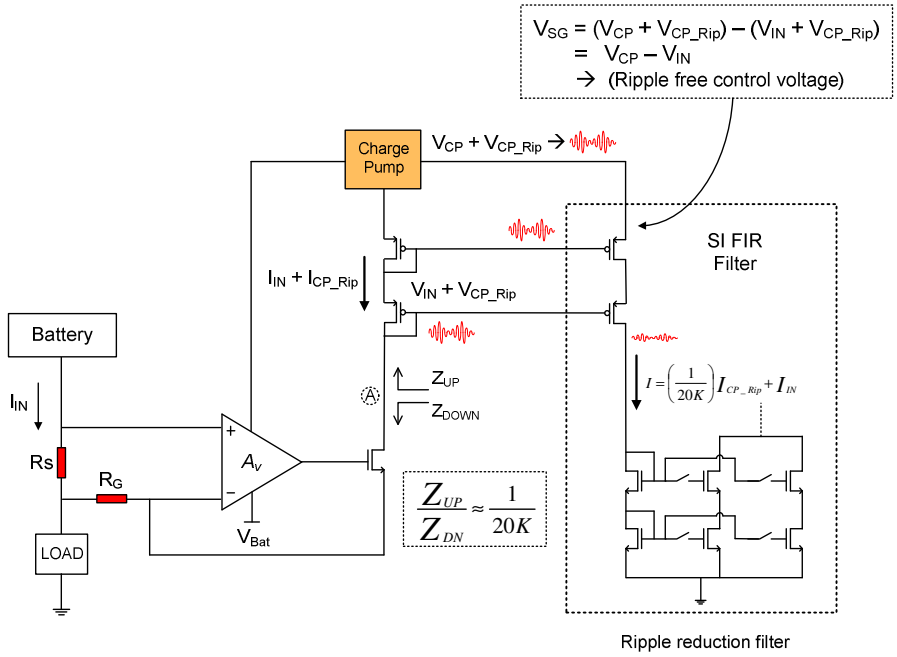


Fig. 4.14 CP ripple suppression by impedance dividing effect

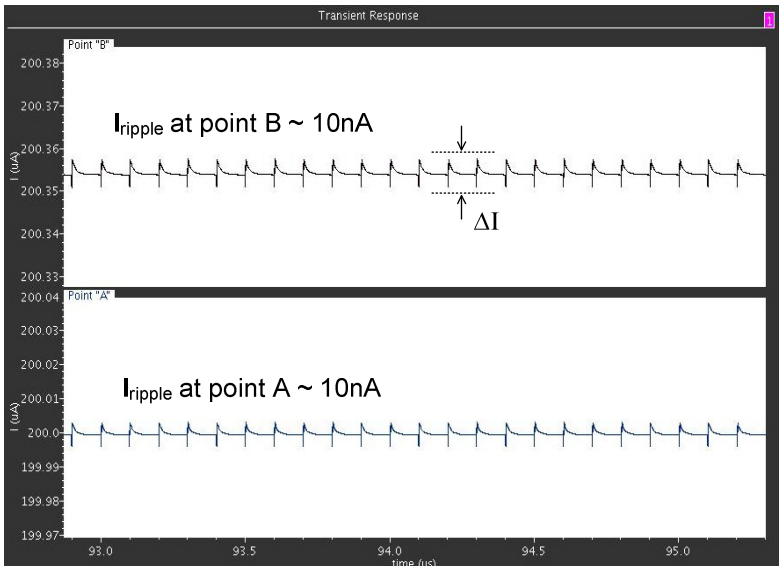


Fig. 4.15 Current at node A and B in Fig. 4.13 with respect to the amount of charge pump voltage ripple

The ratio of Z_{down} vs. Z_{up} (~20,000:1) would reflect the same amount and phase of the power supply ripple on the point A in the Fig. 4.14, and the current ripple reflected on the point B due to the power supply voltage ripple will be suppressed down by this ratio.

The simulation result in Fig. 4.15 shows that the current ripple at node B in Fig. 4.14 which is replica of the sensed current at node A. The amount of current change due to the voltage ripple (V_R) is 10nA, which is about 0.005% error with respect to the desired sensed current signal that is 200uA. This result is equivalent to achieving 85dB ripple suppression. The charge pump ripple reduction corresponding to different sensed input current is shown in Table 4.3. Since the front-end preamplifier of the CSM maintains minimum headroom for operation by using the power supply (battery) as its ground return and boosted

supply as its new power supply, most of the high voltage sensing front-end amplifier could be built by using low voltage core transistors without using any dedicated high voltage compliant transistors. The flying capacitance (C_F) of 100pF is integrated inside the chip while the load capacitance (C_L) is located outside of the chip to provide current of 400μA.

TABLE 4.3

Charge Pump Ripple Reduction with Respect to Different Sensed Input Current

Sensed Input (mA)	Charge Pump (CP) Ripple (mV)	Output change due to CP ripple (uV)	Suppression (dB)
5	4.032	0.397	80.13
10	5.054	0.503	80.04
15	6.047	0.597	80.11
20	7.011	0.713	79.86

4.1.1.4 Switching Current Mode FIR Filter Design

As discussed in earlier chapter, the two main chopping ripple noise sources are generated by the modulation switch and the amplifier input referred noise (ex. flicker, input pair mismatch, and etc.) as in Fig. 4.16. The spike signals generated by the clock feed-through of the modulation MOSFET switches are amplified by the gain A of the amplifier before being demodulated back to the DC level and its even harmonic terms. Therefore, the harmonic tones of the induced residual offset are located at even harmonics of chopping frequency with the input

signal. In the meantime, the input referred dc offsets and flicker noise terms are being transposed to the odd harmonics of the chopping clock frequency, which eventually separates the dc-offset (such as flicker, and etc.) from the incoming input signal. Depicted in Fig. 4.17 are the noisy spike signals that are mainly caused by the clock feed-through and charge injection of the Mosfet switches.

As discussed earlier, chopping results in chopping ripple and residual offset at the chopping frequency due to up-converted DC offsets, flicker noise, switching clock feed-through and charge injection [27]. The resulting signal at the point A of the signal path after chopping was previously depicted in Fig. 4.5. The Fig. 4.18 conceptually shows how SI FIR filter average out the chopped ripple signal and the residual offset. The proposed design implements ripple reduction scheme that uses a second order current mode semi-digital current-mode FIR filter as previously shown in Fig. 4.2.

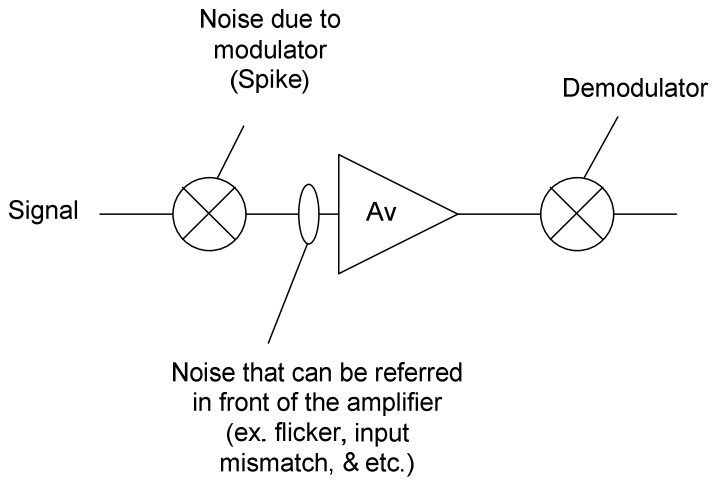
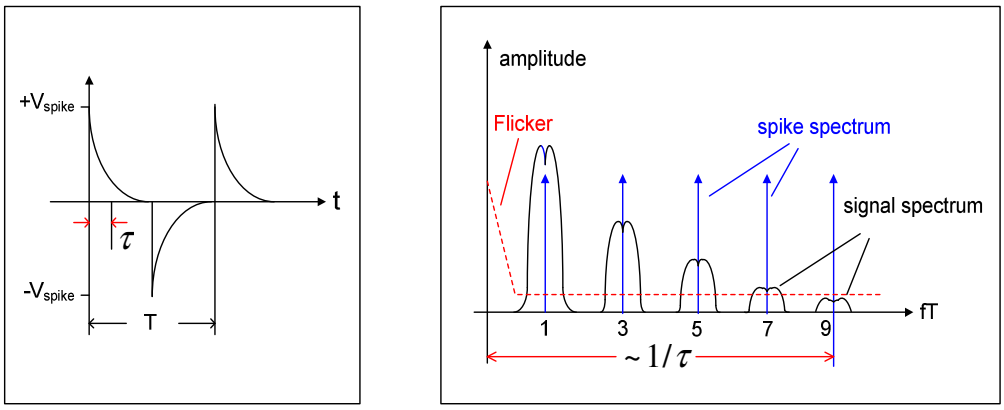


Fig. 4.16 Two main sources of noise contributing to output in chopper amplifier system



(a) (b)

Fig. 4.17 (a) Spike signal occurred by clock feed-through in time domain. (b) spectrums of different noise sources in frequency domain

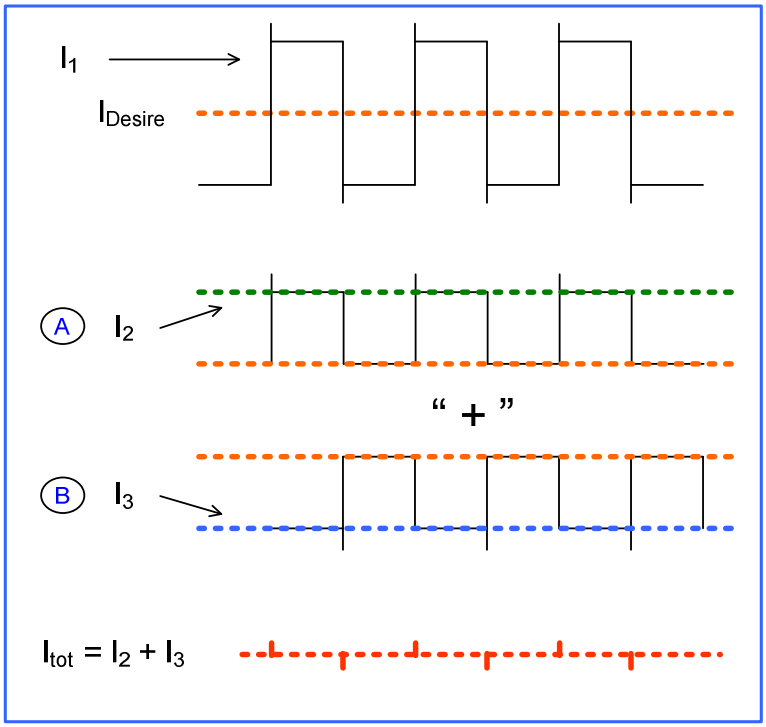


Fig. 4.18 Cancellation of chopping ripple by averaging

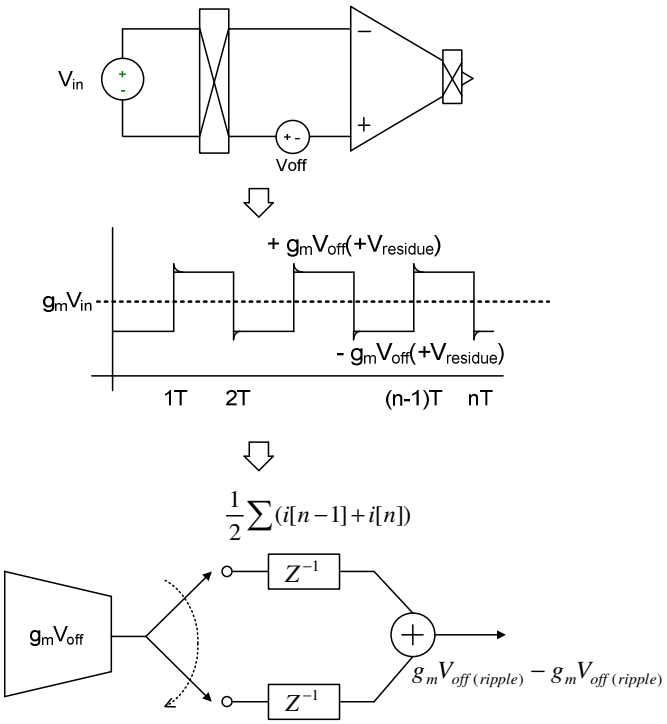


Fig. 4.19 Cancellation of the offset by chopping and notching out of the resulting ripple by following SI FIR filter in time domain analysis

The Switching Current mode (SI) FIR filter will average out the ripples by track and hold the incoming current domain signal during clock phases of ø1 and ø2 as described in Fig. 4.19. In frequency domain, the current mode second order semi-digital FIR filter also provides a notch filtering at the integer harmonics of the chopping frequency [46]-[48]. While the SI FIR filter is averaging out the chopping ripple caused by the input offset and flicker noise, its *sinc* response also notches out the residual ripples caused by the switching clock feed-through and charge injection. Since the residual offset caused by the first chopper switches will be amplified and modulated by the second chopper switches, only odd harmonics of the chopper frequency contributes to the residual offset, therefore

the spike signal has an odd symmetry. Since the time constant τ in Fig. 4.17(a) in general is much smaller than T/2, the energy of the spike signal concentrates at frequencies higher than the chopper frequency [27]. The spectra of the spikes and the chopper-modulated signal at the input of the amplifier are shown in Fig 4.17(b). Mathematically, a sample and hold operation can be expressed as following.

$$f_{s/h}(t) = \sum_{n=0}^{\infty} f(nT)[u(t-nT) - u(t-nT-T)] \tag{4.6}$$

where u(t) = $\begin{cases} 0 & t < 0 \\ 1 & t \geq 0 \end{cases}$

Taking Laplace Transform of above equation will result in the following equations.

$$f_s(s) = \left[\frac{1-e^{-sT}}{s}\right] \sum_{n=0}^{\infty} e^{-snT} f(nT) \tag{4.7}$$

$$\left|H_{s/h}\, f\right| = \left|\frac{1-e^{-sT}}{s}\right| = T \frac{\left|sin\left(\frac{\omega T}{2}\right)\right|}{\left|\frac{\omega T}{2}\right|} \tag{4.8}$$

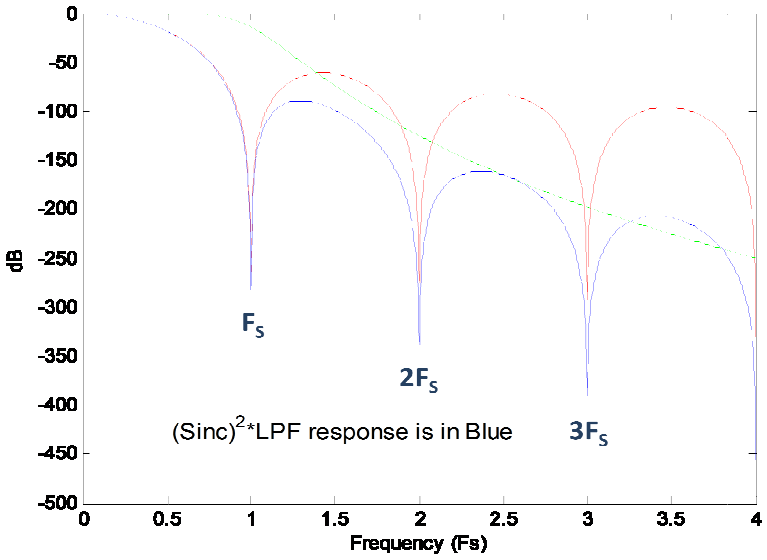
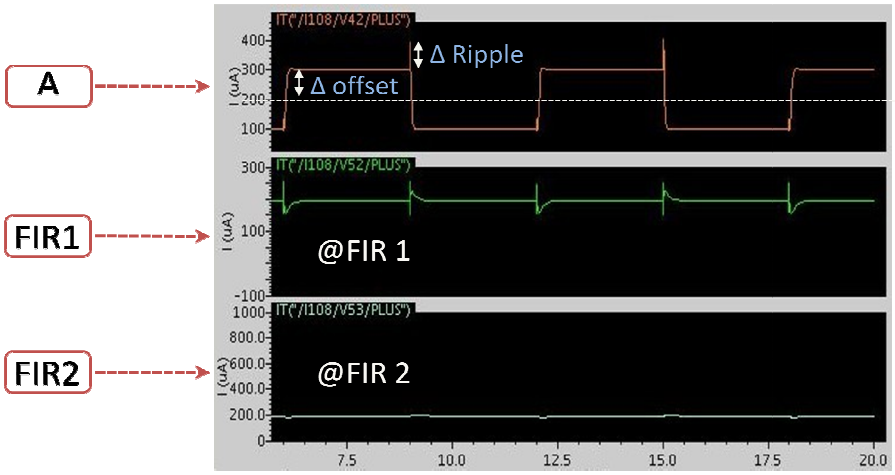
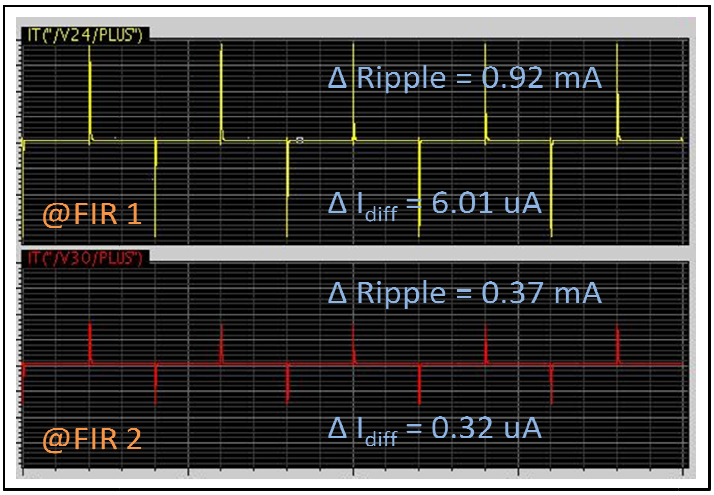


Fig. 4.20 Filter response FIR1, FIR2 and LPF in frequency domain



(a)



(b)

Fig. 4.21 Transient simulation results showing chopping ripple reduction comparison of FIR1 vs. FIR2

The equation (4.8) shows that the *sinc* response of the switching current mode FIR filter effectively suppresses down the switching and its harmonics of the chopper [49]. To achieve a wider band notch around the chopping frequency harmonics, two first-order hold *sinc* FIR filters are cascaded, achieving a $sinc^2$ response as shown in Fig. 4.20.

The second order *sinc*^{2} filter reduced residual ripple by more than 7.5mV$_{pp}$ from a baseline of 8mV$_{pp}$ ripple. The Fig. 4.21 shows a comparison of sinc filter notch effect as the order of the general sinc filter is increased in time domain analysis.

The final stage of the system includes buffers embedded with a first order passive LPF that can sense the output of the SI FIR filter differentially and convert the final difference to single-ended output. As shown in Fig. 4.2, the final buffer stage filters out remaining ripples outside the bandwidth of the LPF cutoff frequency in the signal after passing through the SI FIR filter stage.

4.1.1.5 Implementation of High Voltage Chopper Modulation Switches

Since the front end input amplifier stage uses incoming voltage as its own power, the input stage is facing wide range of voltages, namely 0V to 26V for this application. Fig. 4.22 describes the case when the incoming voltage is in excess of the compliant gate to source voltage, V$_{gs}$ for the front end modulation switches.

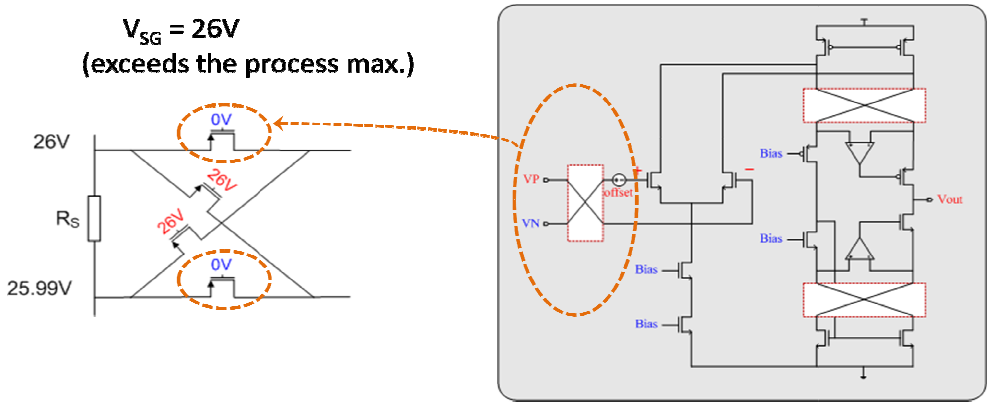


Fig. 4.22 Incoming voltage in excess of Vgs process compliance

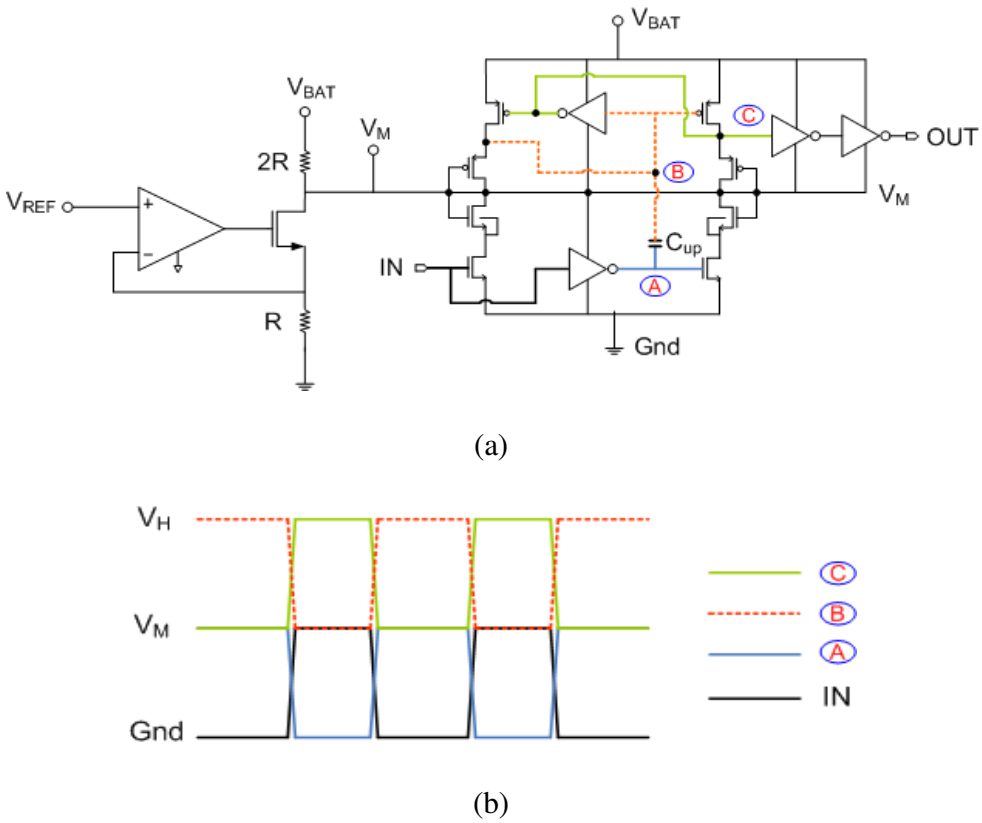


Fig. 4.23 (a) Level shifting circuit for input modulator protection (b) output waveform of the level shifter

Although high voltage compliance drain extended MOSFET can sustain maximum voltage drop up to 40V over drain to source (V_{ds}), the voltage drop over gate to source (V_{gs}) and gate to drain (V_{gd}) is limited to 8V to protect from gate oxide breakdown for the selected process.

For example, when the incoming voltage is 26V a pair of p-MOSFET switch is supposed to be on while the other set is to be off as in Fig. 4.22. Since the maximum voltage compliance of V_{gs} is only 8V for the chosen process, one set of the two pairs of switches are always facing into excess voltage.

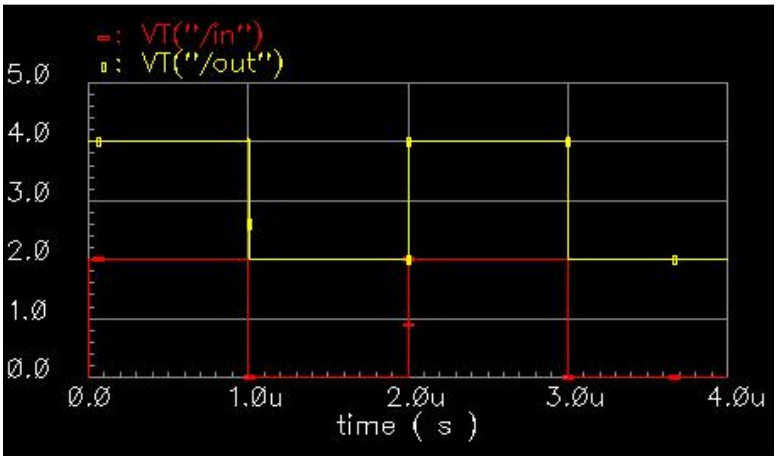


Fig. 4.24 Level shifted output wave form with respect to the middle voltage V_M

Therefore, special protection for the front end stage transmission gates is needed not to face into voltage drop over the maximum in case the incoming common mode voltage is exceeding the maximum voltage rating for V_{gs}. Shown in Fig. 4.23 are the level shifting circuit and its output. The incoming clock signal is level shifted with respect to the voltage V_M. Fig. 4.24 shows a simulated level shifted output waveform.

4.1.2 Measurements

Fig. 4.25 shows measurement results showing the filtering effect in time domain at the input of the pre-amplifier, output of the first order filter (FIR 1), second order filter (FIR 2) and the final output after buffer with first order RC filter, respectively. The measurement results show that the unfiltered chopped signal contains both offset and switching ripple and the chopping ripple reduced more effectively as the order of the semi-digital *sinc* filter increased.

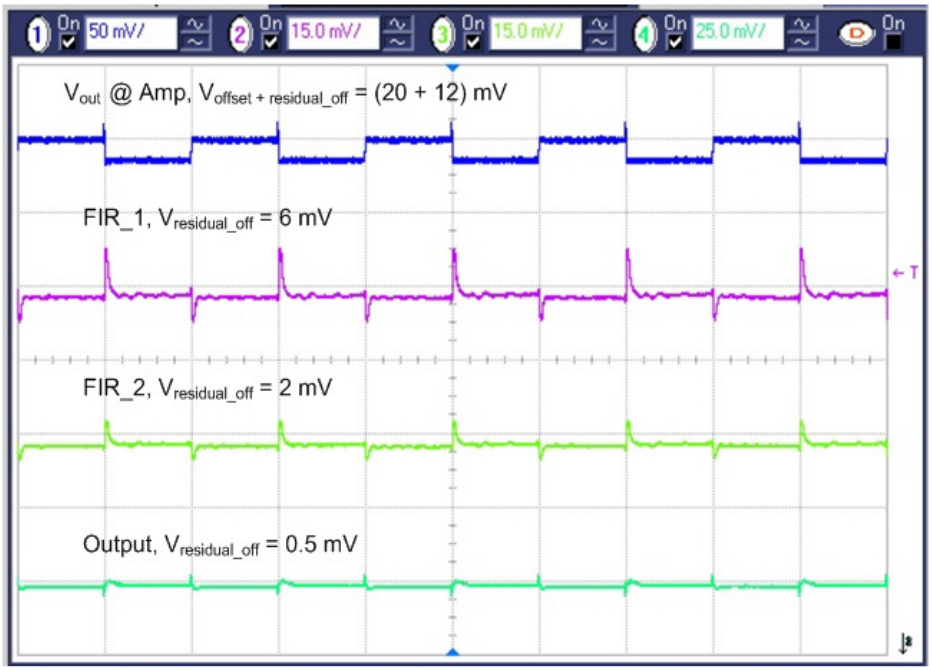
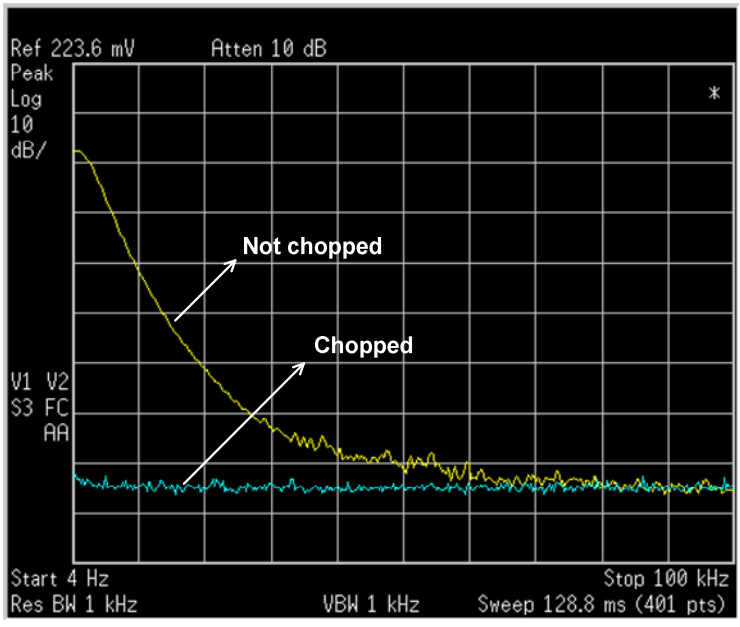
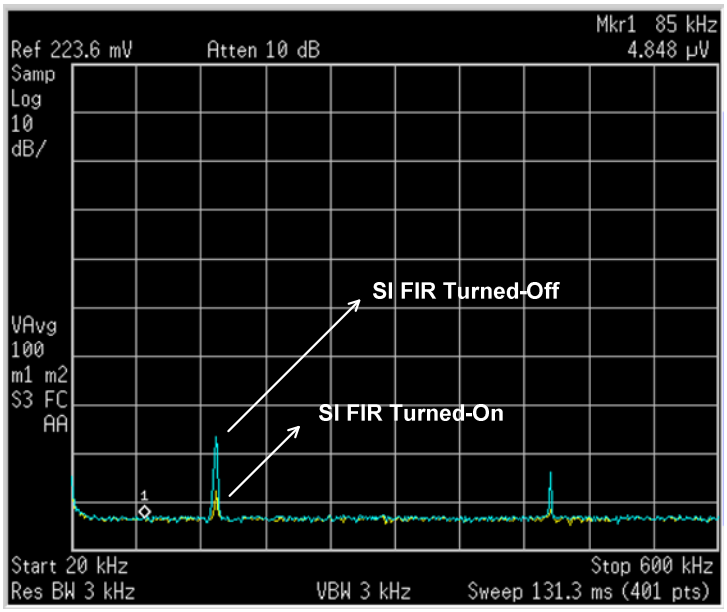


Fig. 4.25 Measured time domain SI FIR filter transient response



(a)



(b)

Fig. 4.26 (a) Measured output Power Spectral Density (PSD) plot with and without chopping from 0 to 100KHz and (b) Measured output PSD plot with and without ripple reduction filtering

Fig. 4.26(a) shows the measured power spectral density (PSD) plot of the given process with and without chopping up to frequency of 100 KHz. Shown in Fig. 4.26(b) are the measured output responses of PSD and reduction of chopping ripple at a frequency of 150KHz and their harmonics at every odd multiples of the chopping frequency by semi-digital *sinc* filter in frequency domain. This measurement result also shows that the chopping ripple and its odd harmonics at multiples of chopping clock frequency have been removed by the designed $sinc^2$ filter and the floor of the input-referred noise density of the overall system is $10\text{nV}/\sqrt{Hz}$.

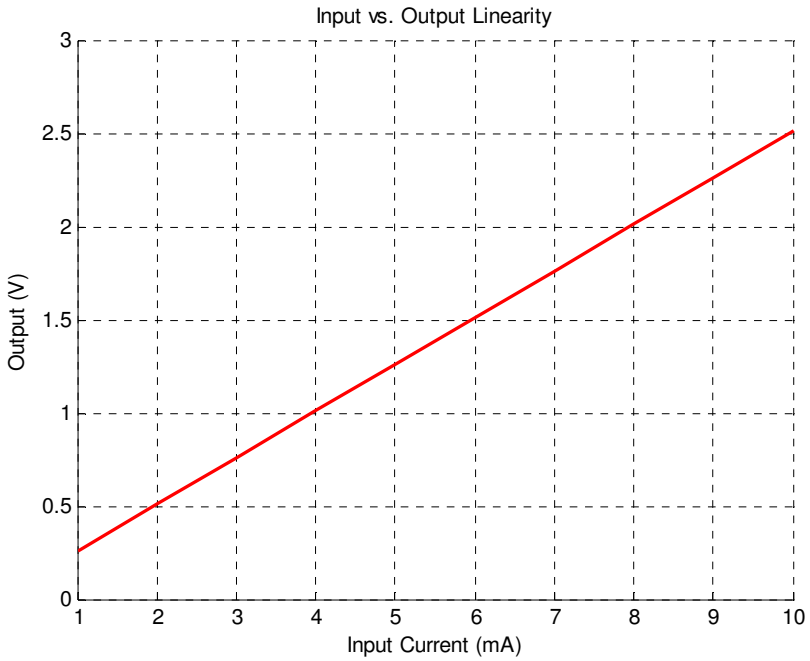


Fig. 4.27 Plot for linearity vs. sensed input current

Fig. 4.27 and Table 4.4 show that input vs. output linearity plot over the wide range of input current at a common mode input voltage of 3V. The linearity plot in manuscript shows how low the current shunt monitor system can sense the input voltage drop without degrading the accuracy of input sensing (performance).

The linearity plot is obtained by measuring the sensing accuracy below the target specification level, 10mV. Since the current that needs to be measured turns into voltage over the sense resistor (R_S), precise readout of the voltage drop at the sense resistor (R_S) over the entire input common mode range (0V-26V) is important. Shown in Table 4.5 are the design parameters of the selected process, AMIS I2T100.

TABLE 4.4

INPUT VS. OUTPUT LINEARITY

Input (mA)	Output (mV)	Linearity error (%) $\left[\frac{(D_n - D_{n-1}) - 250}{250}\right] \times 100$
1	263.87	
2	513.75	0.07
3	763.15	0.08
4	1013.8	0.08
5	1263.75	0.1
6	1513.8	0.1
7	1763.81	0.08
8	2013.79	0.09
9	2263.8	0.07
10	2513.8	0.07

In addition, reducing the amount of voltage drop over the input sense resistor (R_S) is also important because the critical shortcoming of high side current sensing system is that the amount of power dissipated by the current sensing element (R_S) could take the head room needed for the operation of main battery powered load (system). Since reduction of the size of the resistor (R_S) will result in increased errors for the input sensing amplifier due to the reduced voltage generated by the current of interest, more accurate sensing mechanism is needed for the main amplifier in case of reduced magnitude of R_S.

TABLE 4.5

PROCESS PARAMETERS

Process	AMIS I2T100			
General Info.	Substrate	Geometry	HV Operation (V_{ds})	Well Formation
	P-sub	0.7 µm	Up to 100 V	Twin-well
Capacitors	Poly0/Poly1 capacitor (360 pF/mm^2) Metal1/Poly/Metal2 sandwich (75 pF/mm^2)			
B (µA/V^2)	680 (NDMOS, W=40, L=3) 190 (PDMOS, W=40, L=4)			
$V_{th}(0)$	0.8 V (max., NDMOS) -1.2 V (min., PDMOS)			
V_{gs} max	~12 V (Depends on the type and the V_{ds} voltage range of the DMOS)			

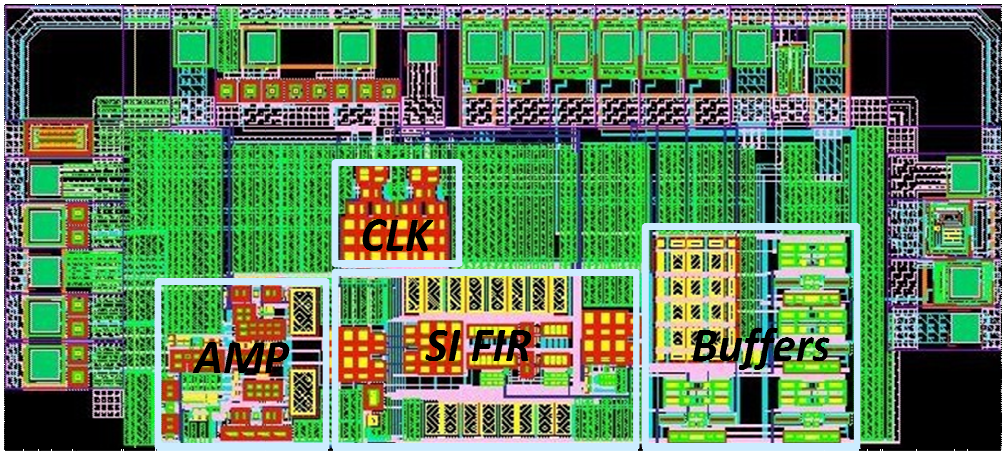


Fig. 4.28 Layout of the proposed direct current reading CSM

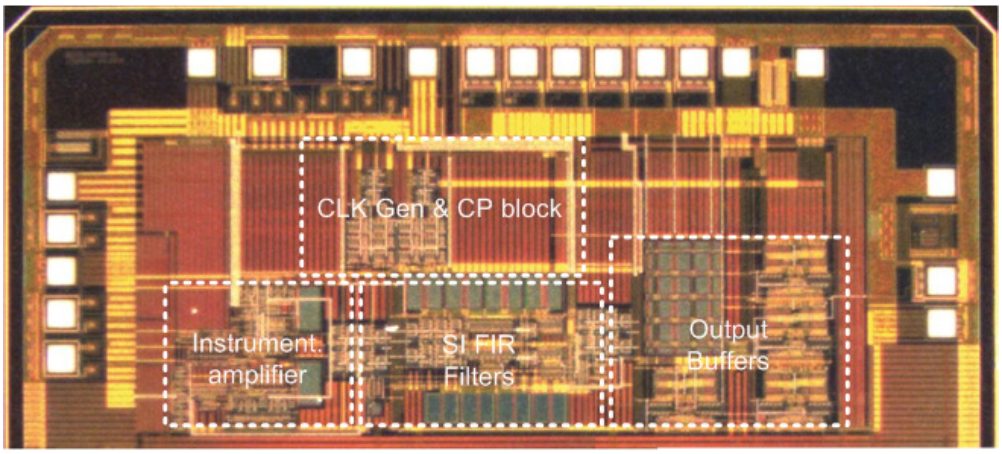


Fig. 4.29 Plot for Die photograph of the proposed CSM

TABLE 4.6

FINAL PERFORMANCE SUMMARY AND COMPARISON

	This work	[15]	[16]	[19]
Year	2010	2007	2008	2009
ICMR (Input CM)	0 to 26V	4 to 60V	1.9 to 30V	-
Floor noise ($nV/\sqrt{Hz}$)	10	-	-	15
Offset (Input Referred)	10 µV	10 µV	5 µV	5 µV
CMRR (DC)	>120 dB	-	-	>120dB
Current draw (I_{supply})	300 µA	420 µA	650 µA	230 µA
Chopping Frequency	150 KHz	-	-	40, 510 KHz
BW	300 KHz	-	-	800 KHZ

The device is fabricated on a 0.7µm AMIS I2T100 CMOS technology with 3 metal layers, and occupies a core area of 2.1 mm^2. Shown in Fig. 4.28 is the final layout of the designed direct current reading CSM. The die photograph of the fabricated current shunt monitor is depicted in Fig. 4.29. Overall system operates with 1.5mW power consumption. The final performance and comparisons with other chopper amplifiers are summarized in Table 4.6.

4.1.3 Conclusion

A current shunt monitor (CSM) system that can sense typical current range of 1mA to 200mA across a Cu board trace of 1Ω over the entire common mode range of 0 to 26 volts is presented. Direct current reading topology with high side current sensing is selected for the design. The proposed CSM can operate rail to rail with reduced number of high-voltage compliant drain-extended transistors being used by maintaining minimum operational voltage for the front-end input stages. The CSM achieves less than 10µV input-referred offset noise floor and DC CMRR of 120dB with the flicker noise of 10nV/$\sqrt{Hz}$ at 100Hz by using chopping and SI FIR notch filter with a gain boosted instrumentation amplifier. As discussed earlier, this system can be used for many industrial current sensing applications with minimal tuning of the proposed design.

4.2 Indirect Current Reading Method

As shown in Fig. 4.30, the voltage drop corresponding to the current flowing through the input sensing resistor (R_S) will be measured by the input gm

stages. In order to suppress input-referred flicker noise and DC offset, the input gm stage uses chopper stabilization at a frequency of 150 KHz which is significantly higher than the flicker noise corner frequency (f_C). Cancellation of the input DC offset and flicker noise with the selected indirect current reading topology can be described in Fig. 4.31. The figure shows that the input referred offset can be removed by averaging the sensed signal (I_{out1} and I_{out2}) of chopping phase 1 and 2.

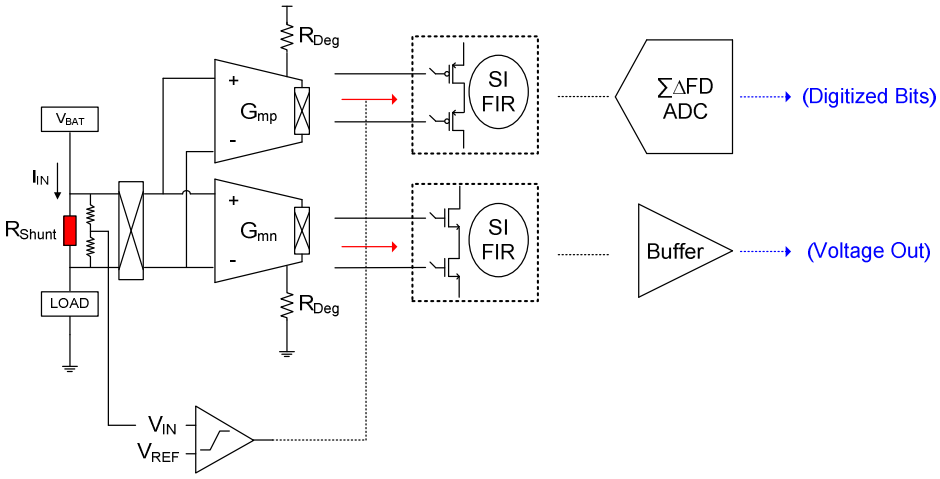
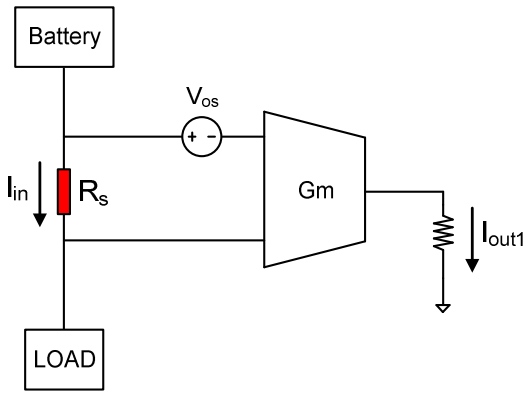
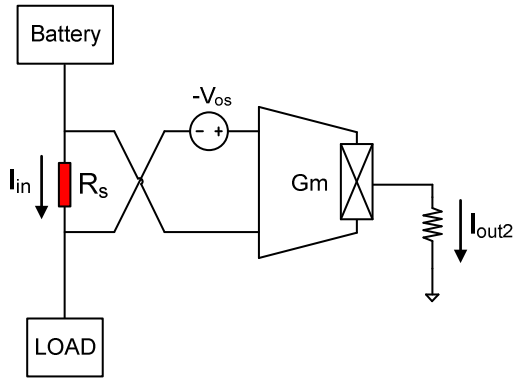


Fig. 4.30 Signal chain of the proposed indirect current reading CSM



(a)



(b)

Fig. 4.31 Cancellation of input referred offset with chopper stabilization

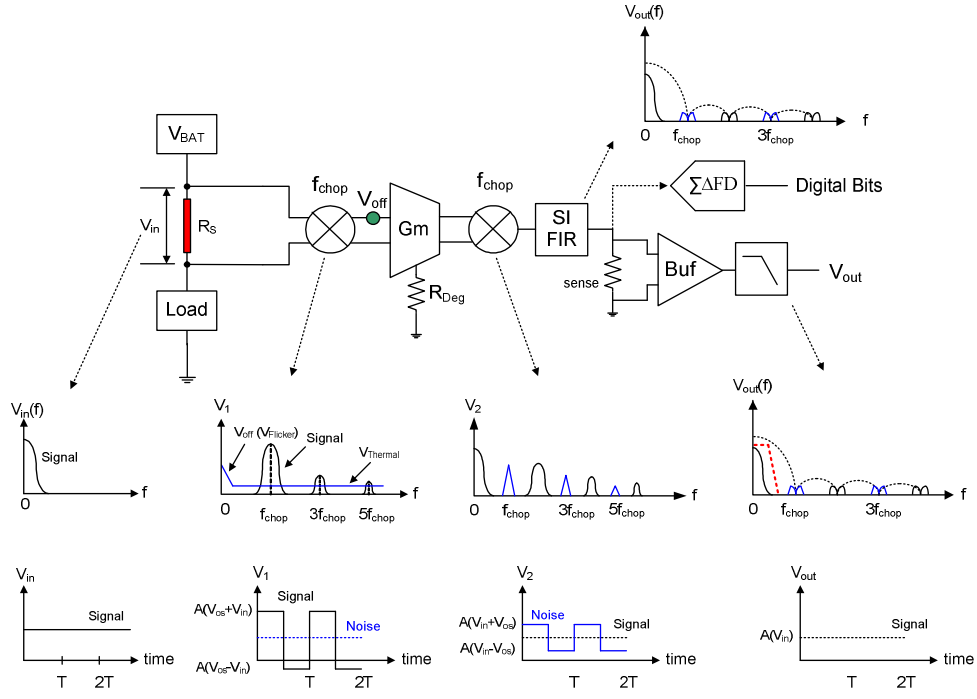


Fig. 4.32 Signal flow of the proposed design in frequency and time domain

Since the chopped signal has ripples due to input offset and flicker noise, and residual offset due to switch clock feed-through and charge injection that cause spikes in front of the front-end amplifier at chopping frequency, following

switching current mode (SI) FIR filter is used to suppress the output ripple and residue at the chopping frequency by notching out the ripple through its sinc filter response at multiples of chopping clock frequency. Fig. 4.32 shows the signal flow and resulting offset and chopping ripple cancellation of the proposed design in both frequency and time domain.

4.2.1 Building Block Analysis

As described earlier, in a conventional CSM design, use of an external sense resistor (R_S) increases the system cost. Also, such a resistor is typically required to be precise enough to put the overall system error within 1% over the entire operational temperature range normally from -40 to 85 °C. Therefore, it is highly desirable to measure the current by simply using the voltage drop across existing Cu-traces on a PCB board in place of a dedicated external sensing resistor, which leads to elimination of external components. Also, the variation of the resistance over temperature is cancelled out at the following frequency domain ADC block, which generates the frequency modulated reference level using an identical path as the sensed input signal path. By sampling the sensed frequency-modulated input signal generated from the Cu-trace path with a frequency-modulated reference signal generated from the identically duplicated Cu-trace path, the temperature variation of the Cu-trace resistance will be cancelled. Also, interdigitation layout helps to reduce the mismatch between the two different current paths. More detailed analysis of the ΣΔFD block will be followed in the upcoming sections.

4.2.1.1 Input Sensing Gm-Block Design

The proposed design adopted indirect current reading topology [30] having two gm-boosted PMOS and NMOS input pairs as depicted in Fig. 4.33.

To cover the entire input common mode range of 30 volts, lower side of input rail is sensed by the p-side gm block while the rest of the input is sensed by the n-side gm block. Selection of the input gm-stage is determined by a simple comparator which has programmable threshold value being changed according to the input common mode level.

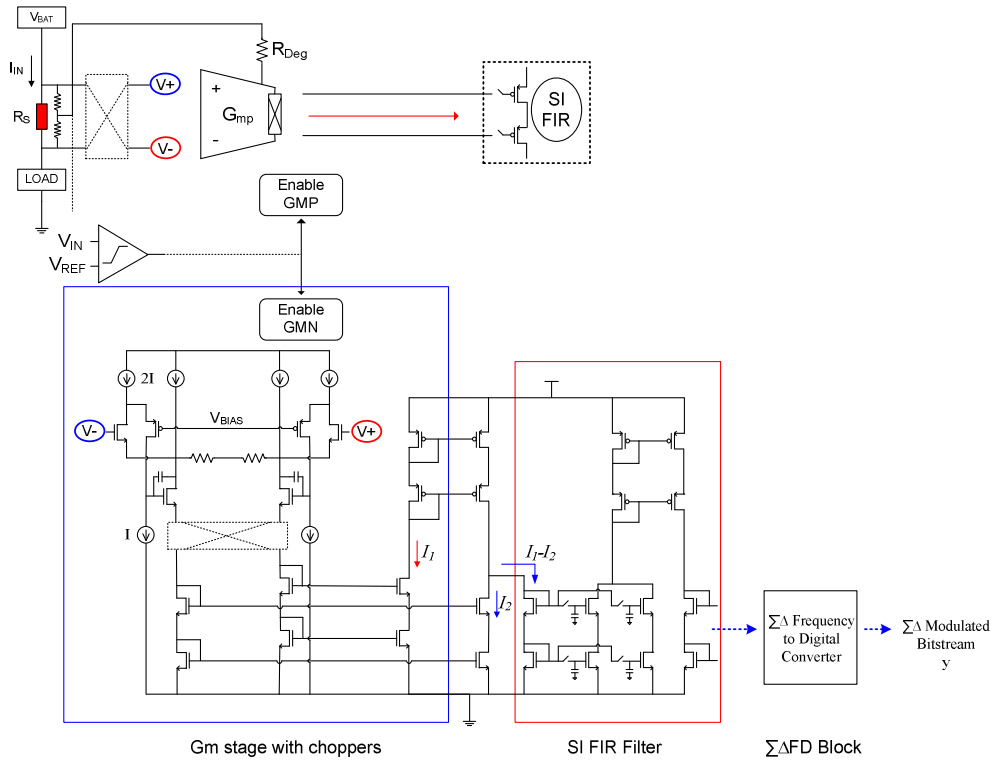


Fig. 4.33 Detailed schematic level design showing input sense resistor (R_S), two chopper stabilized gm stages followed by SI FIR filter, and ΣΔFD block

It is well known that the transconductance (gm) value of a source-degenerated input stage is inversely proportional to the magnitude of the degeneration resistor (R_{Deg}) as long as the magnitude of the effective input gm is comparably large enough to be ignored with respect to R_{Deg} as shown in equation (4.9).

$$G_{meff} = \frac{1}{R_{Deg}+\frac{1}{gm}} \cong \frac{1}{R_{Deg}} \tag{4.9}$$

Since the magnitude of the sensed input voltage drop is inversely proportional to the magnitude of R_{Deg}, the value of the resistance cannot be set up too high. Therefore, increasing the magnitude of input gm stage rather than that of R_{Deg} is necessary. Shown in Fig. 4.34 is an input gm boosting approach [42] which leads into new boosted transconductance (g'_m) value as described in the following equation.

$$g'_m = \frac{I_{OUT}}{V_{IN}} = \frac{V_X}{V_{IN}} \cdot \frac{V_Y}{V_X} \cdot \frac{I_{OUT}}{V_Y} \tag{4.10}$$

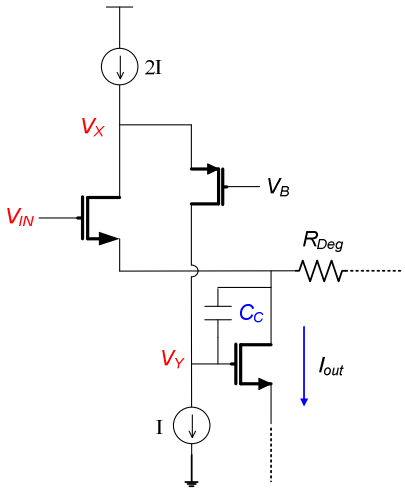


Fig. 4.34 Effective gm-boosting scheme

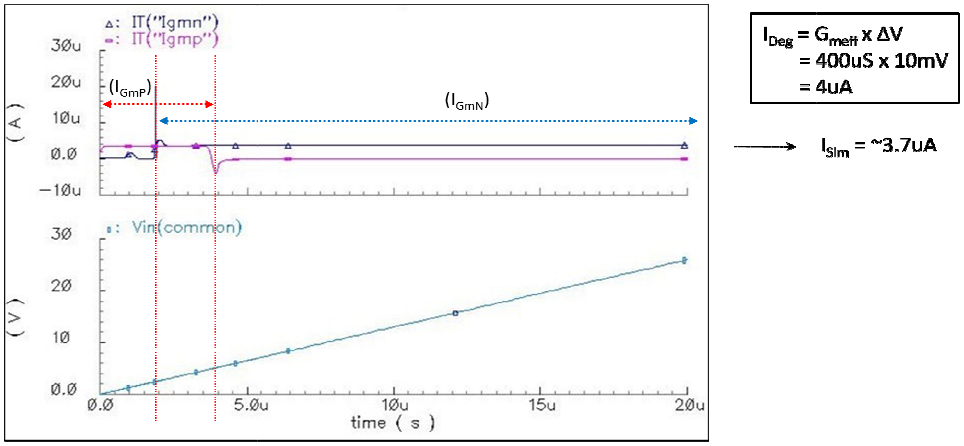


Fig. 4.35 Typical 10mV input over the entire common mode voltage range (0~30V) showing the linear response of the system

The above equation (4.9) is equivalent to the following equation which clearly shows that the new transconductance is boosted by the gain of multiple stages.

$$g'_m = (-g_{m1}r_o) \cdot (g_{m2}r_o) \cdot g_{m3} \tag{4.11}$$

The Miller compensation capacitor (*Cc*) is inserted for loop stability.

4.2.1.2 ΣΔ Frequency Discrimination ADC

The proposed CSM architecture enables digital interface, by using a frequency-domain digitizer using frequency discriminator (ΣΔFD) at the output of the SI FIR filter. The ΣΔFD is composed of a current controlled oscillator (ICO) followed by first-order sigma delta frequency to digital converter, which consists of two D-Flip-Flops (DFFs) and an XOR gate as in Fig. 4.36. This ΣΔFD block accomplishes all three functions of integration, quantization, and differentiation just like a typical analog input ΣΔ modulator.

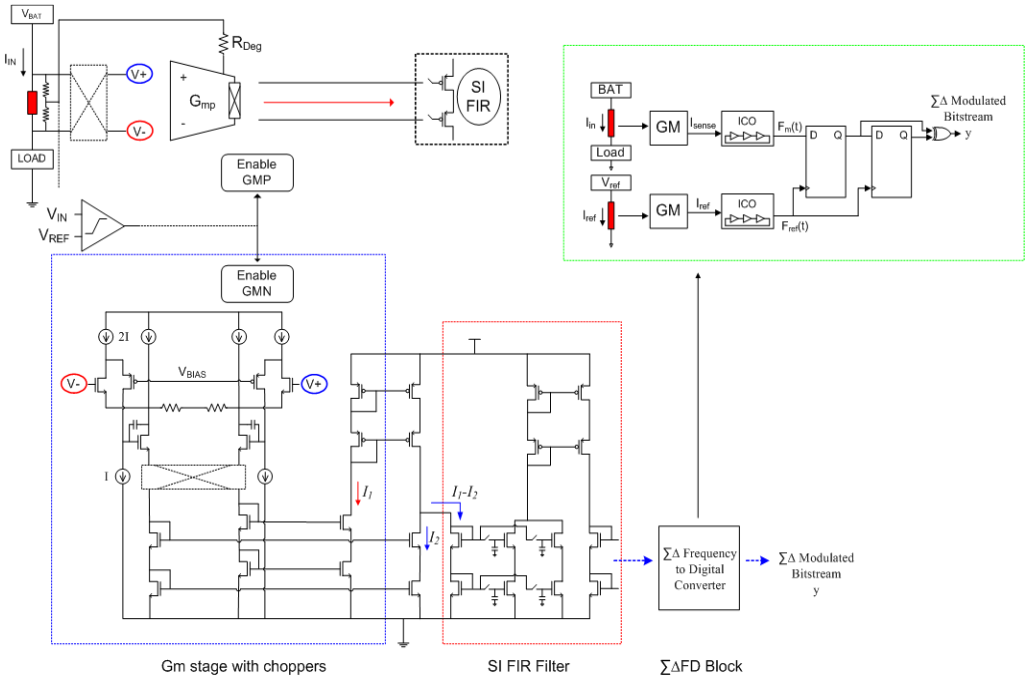


Fig. 4.36 Overall signal chain

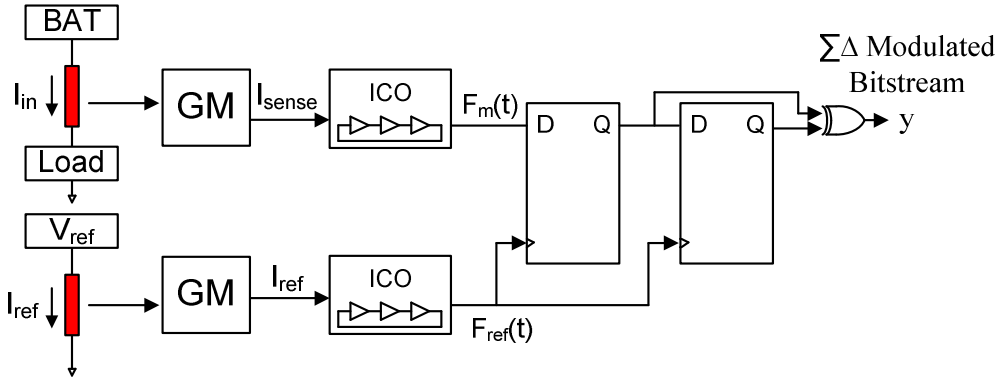


Fig. 4.37 Diagram of the proposed ΣΔFD block

As a consequence of using reduced complexity digital circuits in comparison to analog digitization techniques, such as windowed, successive approximation or pipeline ADCs, it consumes lower power [50]. Operation of the

ΣΔFD block is as follows. The output current of the SI FIR can be used as a control signal for the current controlled oscillator (ICO) block. This produces a frequency modulated input signal. Another frequency modulated clock signal that is generated from an identical Cu-Trace and the following gm block is used for sampling the frequency modulated input signal in the ΣΔFD ADC.

Since both the sensed input and the generated clock signals contain the same temperature variation of the Cu-trace resistance, their temperature variation can be cancelled at the digitization stage, hence, produces final temperature compensated ΣΔ frequency modulated digital bit-streams at the output of the ΣΔFD ADC.

4.2.2 Measurements

Fig. 4.38 shows measurement results showing the filtering effect in time domain at the output of the gm block which containing square wave ripple and residual offset, the first order filter (FIR 1), second order filter (FIR 2) and the final buffer with first order RC filter, respectively. The measurement results show that the unfiltered chopped signal contains both offset and switching ripple and the chopping ripple reduced more effectively as the order of the semi-digital *sinc* filter increased. Fig. 4.39 shows the Power Spectral Density (PSD) plot of the given process with and without chopping up to frequency of 100 KHz.

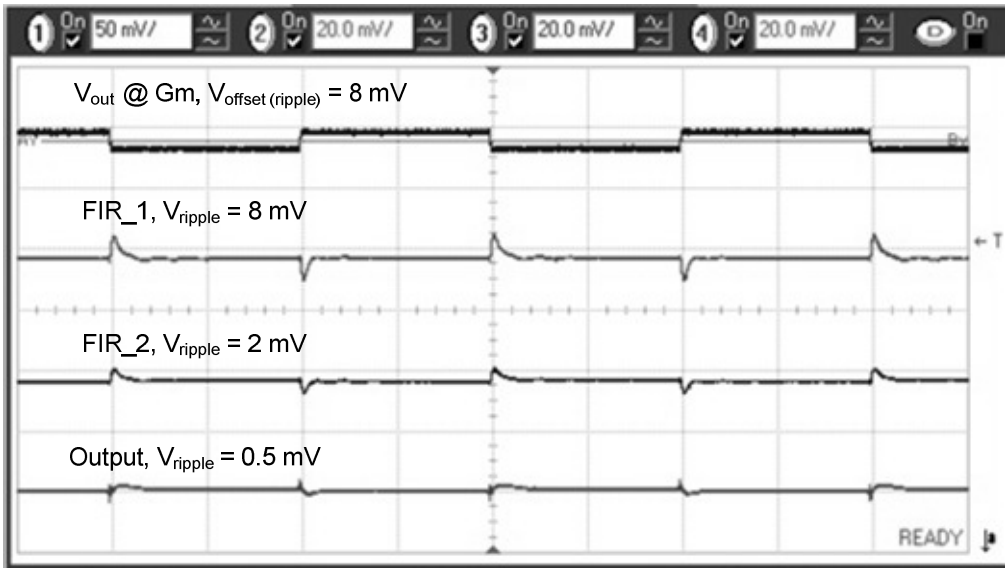


Fig. 4.38 Measured time domain SI FIR filter transient response

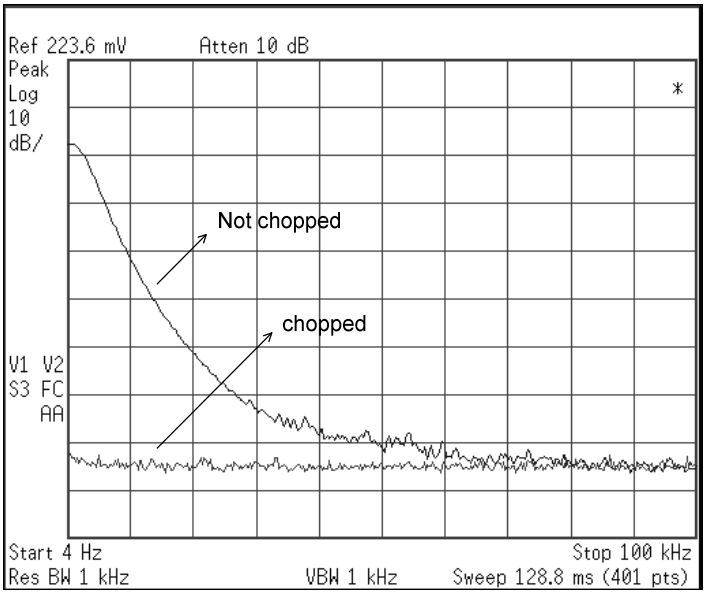


Fig. 4.39 Measured output Power Spectral Density (PSD) plot with and without chopping from 0 to 100 KHz

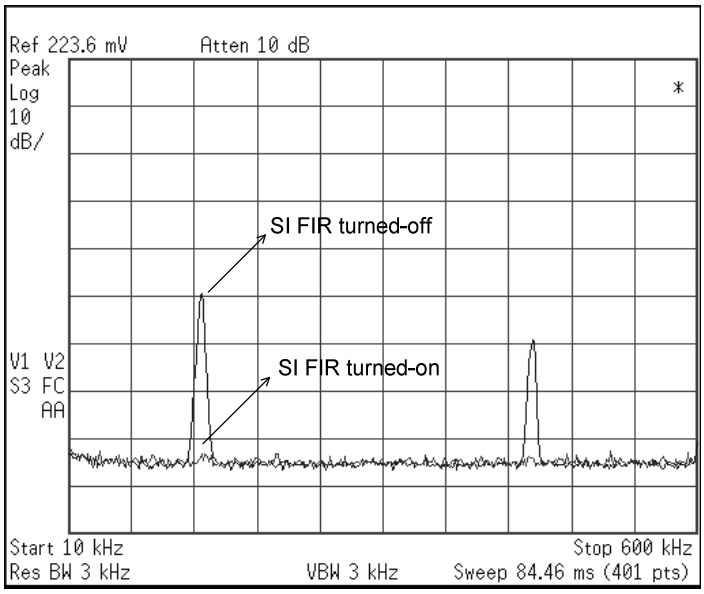


Fig. 4.40 Measured output PSD plot with and without ripple reduction filtering

Shown in Fig. 4.40 are the output responses of PSD and reduction of chopping ripple at a frequency of 150 KHz and their harmonics at odd multiples of the chopping frequency by semi-digital *sinc* filter in frequency domain. This measurement result also shows that the chopping ripple and its odd harmonics at every multiple of chopping clock frequency have been removed by the designed $sinc^2$ filter and the floor of the input referred noise density of the overall system is $10\text{nV}/\sqrt{Hz}$. Fig. 4.41 and Table 4.7 show that input vs. output linearity plot over the wide range of input current at a common mode input voltage of 2V at the ADC output.

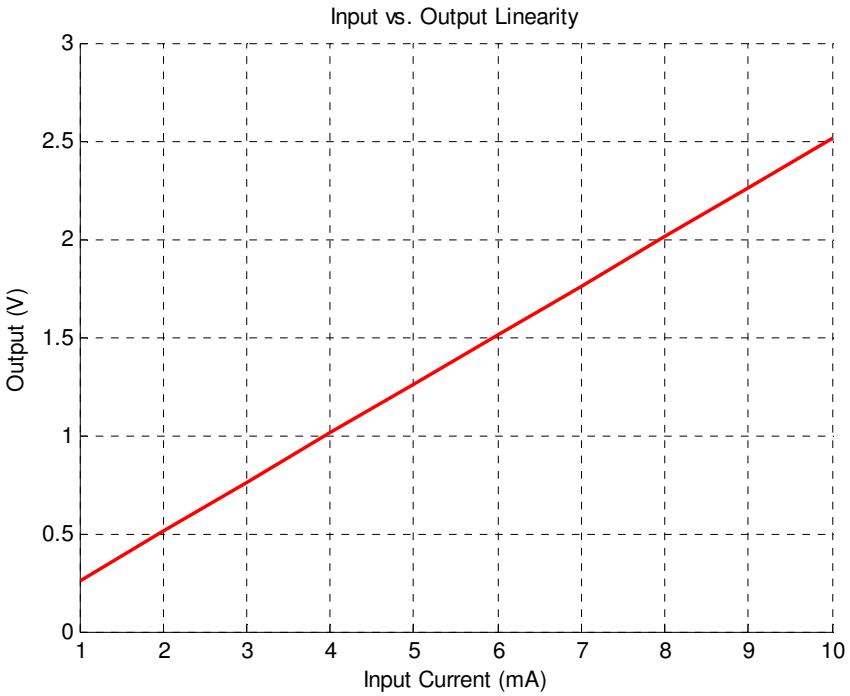


Fig. 4.41 Plot for linearity vs. sensed input current

As it was done for the case of direct current reading based CSM in the previous chapter, the linearity plot shows that how low the current shunt monitor system can sense the input voltage drop without degrading the accuracy of input sensing (performance). The linearity plot is obtained by measuring the sensing accuracy below our target specification level, 10mV. The design efforts that are attributed to the obtained linearity are as following.

TABLE 4.7

INPUT VS. OUTPUT LINEARITY

Input (mA)	Output (mV)	Linearity error (%) $\left[\frac{(D_n - D_{n-1}) - 250}{250}\right] \times 100$
1	264.88	
2	514.76	0.07
3	764.16	0.08
4	1014.9	0.08
5	1264.85	0.1
6	1514.9	0.1
7	1764.91	0.08
8	2014.89	0.09
9	2264.9	0.07
10	2514.9	0.07

Using board Cu-trace as a sensing method which brings down the size of sense resistor to typical range of 1Ω, input stage Gm-boosting scheme which helps increasing linearity of the source degenerated input stage, interdigitated layout of the degeneration resistors for better matching and chopping technique with appropriate FIR filtering. Overall system operates with 1mW power consumption. The final performance and comparison are summarized in Table 4.8.

TABLE 4.8

FINAL PERFORMANCE SUMMARY AND COMPARISON

Design Parameters	This work	[15]	[16]	[19]
Year	2010	2007	2008	2009
ICMR (Input CM)	0 to 26V	4 to 60V	1.9 to 30V	-
Floor noise (nV/$\sqrt{Hz}$)	10	-	-	15
Offset (Input Referred)	10 µV	10 µV	5 µV	5 µV
CMRR (DC)	140 dB	-	143 dB	>120dB
Offset drift	± 75nV/°C	± 50nV//°C		
Chopping Frequency	150 KHz	-	-	40, 510 KHz
Current draw (I_{supply})	200 µA	420 µA	650 µA	230 µA

As shown in the provided table, the most significant performance of the proposed design is that it can cover the entire input rail to rail common range including ground level input while achieving minimal power consumption.

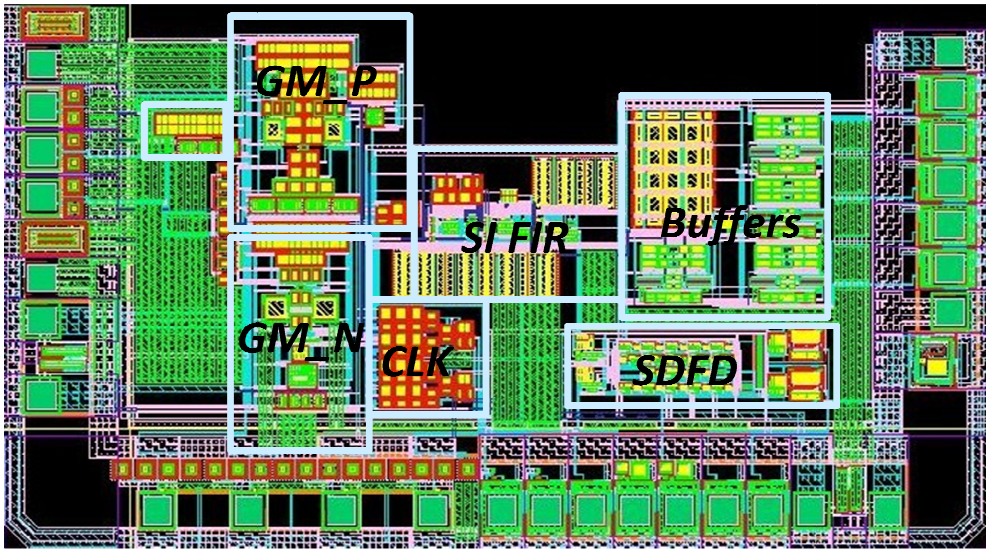


Fig. 4.42 Final layout of the proposed indirect current reading CSM

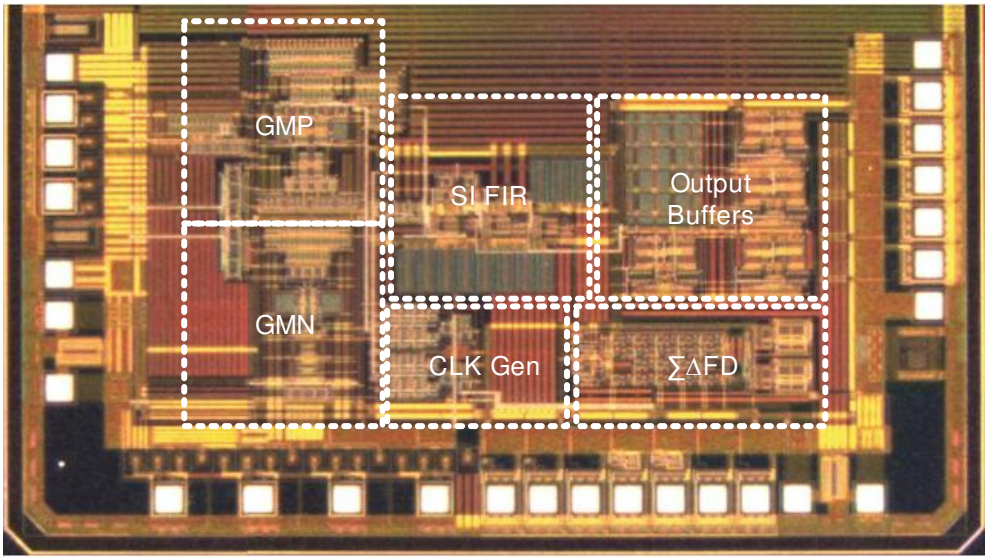
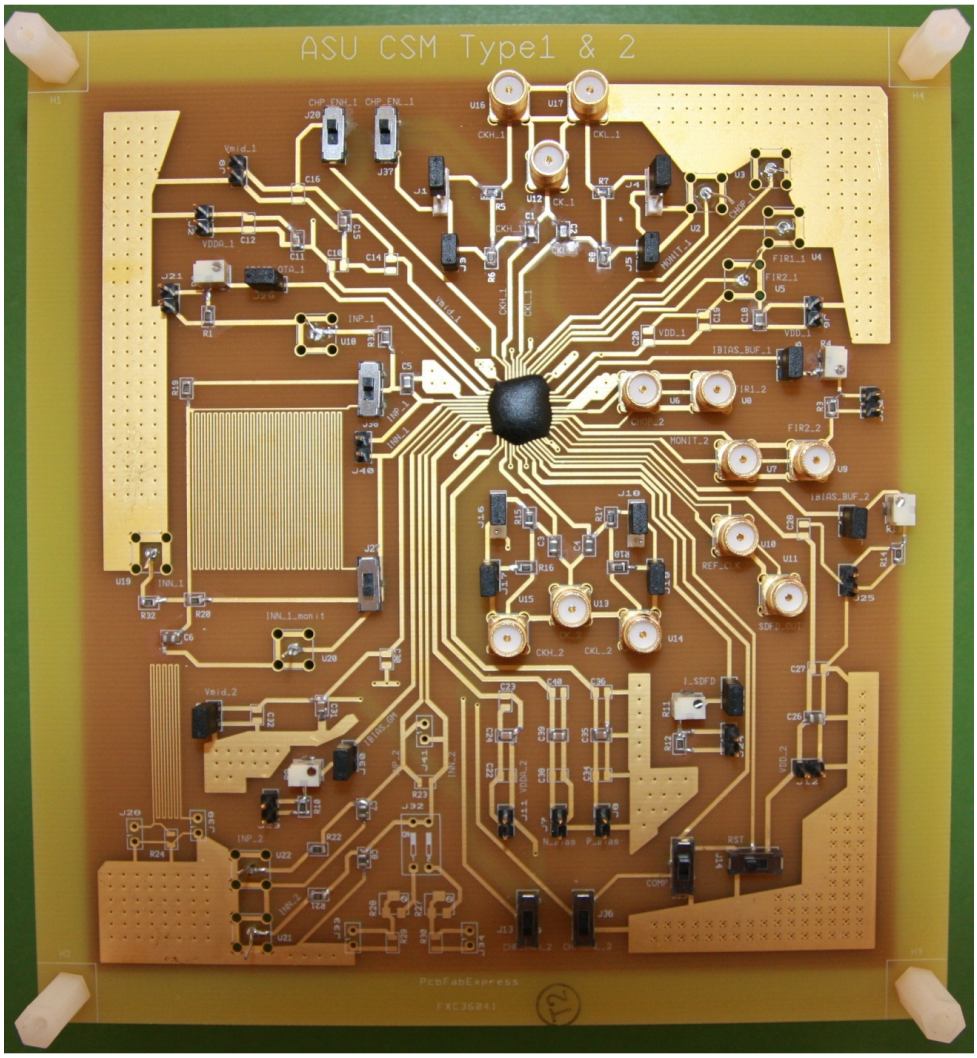


Fig. 4.43 Plot for Die photograph of the proposed CSM

The device is fabricated on a 0.7µm AMIS I2T100 CMOS technology with 3 metal layers, and occupies a core area of 2.3 mm^2. Shown in Fig. 4.42 is

the final layout of the designed indirect current reading CSM. The die photograph of the fabricated current shunt monitor is depicted in Fig. 4.43. Shown in Fig. 4.44 is the picture of the final test board that is used for both types of the proposed designs.



4.44 Picture of the final testing board

4.2.3 Conclusion

A current shunt monitor system that can sense typical current range of 1mA to 500mA across a Cu board trace of 1Ω over the entire common mode range of 0 to 30 volts is presented. Indirect current reading topology with high side current sensing is selected for the design. The proposed CSM can operate over entire input rail to rail common mode range by switching from p-side gm stage to n-side gm stage accordingly.

Some of the highlights of this approach include use of existing PCB Cu trace resistance for input current sensing method, which reduces the cost of mass production by eliminating dedicated external sense resistor component. Second, this work can cover entire input rail to rail from 0V to 30V, which includes absolute ground level input. Third, the switching current mode FIR filter notches out the chopping ripple at multiples of chopping frequency, which can only be possible through higher order filter with sharp 3dB pass band very close to the baseband frequency. This conventional analog filtering technique may induce significant loss of signal due to the reduced pass bandwidth of the signal while the sample domain filter can notch out the ripple with no significant impact on the baseband signal. Finally, there is an optional direct digital interface with micro-controllers by using a built-in ΣΔ ADC block. Since the frequency modulated input signal is available by feeding the sensed input signal thorough a current controlled oscillator (ICO) chain, a first order digital ΣΔ ADC can be implemented at the output of the signal chain with minimally added gate counts (Two digital FFs and one XOR gate) and power consumption.

The CSM achieves less than 10μV input-referred offset and DC CMRR of 120dB with the flicker noise of 10nV/$\sqrt{Hz}$ at 100Hz by using chopping and SI FIR notch filter. ΣΔ modulated bit stream output makes the designed CSM system possible to communicate with other digital systems directly without using any additional interconnecting circuitry.

5 CONCLUSIONS

Those noise sources that are originated from amplification of the clock feed through of the modulation switches reflected as residual ripples at the final output of the amplifier. Moreover, in addition to the ripple occurring at chopping frequency, its harmonic terms located at every multiple of chopping clock frequency contribute to the DC offset.

Many prior works tried to minimize the residual ripple in different ways. Most of the prior arts fall into one of the subcategories as following; ripple reduction loop based low pass filter technique, band pass filter based ripple reduction technique, and nested chopper based ripple reduction. In general, each different method was designed to have lower comparable residual ripple while each approach has its own shortcoming.

First of all, the low pass filter based approach needs to have a lot higher order and runs at the risk of impacting DC measurement accuracy to have an equivalent performance to our proposed sinc filter based design. Also, the additional Gm stages for ripple reduction loop can be added noise source of DC offset at a lot complicated design effort due to higher order amplifier loop compensation and added Gm stages. The band filter pass based ripple reduction loop also achieves low offset at the potential risk of increased noise when there is mismatch between the center frequency of the band pass filter and the frequency of the chopper. Finally, the nested chopper technique runs at the limitation of that the input signal frequency is reduced to half of slower chopper frequency. Consequently, the most important point that all the previous approaches could not

efficiently overcome was that the harmonic contents of the chopping ripples could not be removed effectively. The significance of the presented discrete time switching current mode FIR filter approach is that it can remove all the harmonic contents of the chopping ripples located at every multiple of chopping clock frequency by its natural zero order hold sinc response. Also, the fact that the signal filtering is carried over the current domain can also remove a potential risk of the sensed signal being corrupted by unnecessary noise addition generated from the current to voltage conversion process that should be entailed in typical voltage domain filter stage.

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