Aging Predictive Models

and Simulation Methods

for Analog and Mixed-Signal Circuits

by

Rui Zheng

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Graduate Supervisory Committee:

Yu Cao, Chair
Hongyu Yu
Bertan Bakkaloglu

ARIZONA STATE UNIVERSITY

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ABSTRACT

Negative bias temperature instability (NBTI) and channel hot carrier (CHC) are important reliability issues impacting analog circuit performance and lifetime. Compact reliability models and efficient simulation methods are essential for circuit level reliability prediction. This work proposes a set of compact models of NBTI and CHC effects for analog and mixed-signal circuit, and a direct prediction method which is different from conventional simulation methods. This method is applied in circuit benchmarks and evaluated. This work helps with improving efficiency and accuracy of circuit aging prediction.

DEDICATION

To my family

ACKNOWLEDGMENTS

I would like to express my sincere gratitude and respect to my advisor and mentor Dr. Yu Cao, for his continuous support and invaluable guidance, during the course of the work, without which this work would not have been possible. His trust in my capabilities and his patience in discussion have been the motivating force for this work.

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CHAPTER 1

INTRODUCTION

1.1 Overview of Circuit Reliability

Moore in 1965 predicted that the number of transistors that can be placed on an integrated circuit will be approximately doubled every two years [1]. Although it was initially an observation or forecast, the prediction has turned into a 'self fulfilling prophecy' rather than a law. Moore's law has turned into the driving force for technological advancement in the semiconductor industry. The increased transistor count has directly led to improved capabilities in the digital devices such as processing speed, power, memory capacity etc.

Scaling of CMOS technology will continually drive the evolution of electronics, and the total number of devices per chip will keep increasing. Certain problems emerge as technology advances. Circuit performance degrades over time and this is called circuit aging. Cost effectively designing and manufacturing electronic systems become more and more challenging due to the presence of multiple variability and reliability issues, such as negative bias temperature instability (NBTI)[2][3], channel hot carrier (CHC), time dependent dielectric breakdown (TDDB) etc. These mechanisms have been known to affect the transistors since the 1970s but have become more pronounced in the nano-scale regime when processing and scaling changes are introduced to improve device and circuit performance [4]. The situation is further complicated by real-time

uncertainties in workload and ambient conditions, which dynamically influence the rate of temporal degradation. The result of these aging mechanisms is the degradation in the circuit characteristics such as drain current which ultimately may lead to logic failure and reduce lifetime of a device.

In today's microprocessors, scaling of power supply (V_{dd}) is done but the threshold voltage (V_{th}) does not scale any more. Lower V_{dd} and constant V_{th} greatly increase the vertical and lateral electric field, which exacerbate CHC and NBTI effects. Both CHC and NBTI result in poor drive current, lower noise margin and shorter device lifetime.[5]

1.2 Concerns with Reliability Analysis

While technology improvement is the main focus in traditional research, ignoring these aging effects in the design process leads to an excessive amount of over-margining. As the reliability concerns become more severe with continuous scaling, it is critical to understand, simulate, and mitigate their impact during the design stage. Design for reliability requires predictive design tools, which has to fulfill the following requirements: integrating the key degradation mechanisms; analyzing their impact on the operation, identifying critical functional units; and evaluating the tradeoff among different performance metrics. The simulation and analysis of circuit aging are fundamentally difficult, since the degradation rate depends on both process and operation conditions, such as supply voltage, temperature, duty cycle, and input patterns. These conditions change significantly from gate to gate and from time to time, rising a dramatic challenge to efficient and accurate reliability analysis of IC designs. To improve design predictability and support robust design it is necessary to develop methods that are able to predict the circuit aging efficiently.

1.3 Aging Prediction in Analog and Mixed-Signal Circuits

There has been intensive work in device-level reliability modeling [4][6][7]. However, the area of reliability simulation for analog and digital circuits requires significant attention. Traditional methods of reliability simulation are still based on transient circuit analysis [8], which are expensive in computation and result in overly pessimistic lifetime prediction.

Different operating conditions in analog and digital circuits lead to different approaches in modeling and simulation. Although it is feasible to develop a unified reliability model at the device level, reliability simulation methods for different type of circuits should be treated differently. As shown in Fig.1.1, digital signals are usually defined by clock cycle T_{clk} (equivalent to frequency) and duty factor α and the rail to rail voltage; however in analog circuits, the voltage has a large signal DC value and a small signal AC value, resulting in a more complicated situation. Such characteristics in circuit operation and topology will lead to a dramatically different stress history and thus, various amounts of degradation.

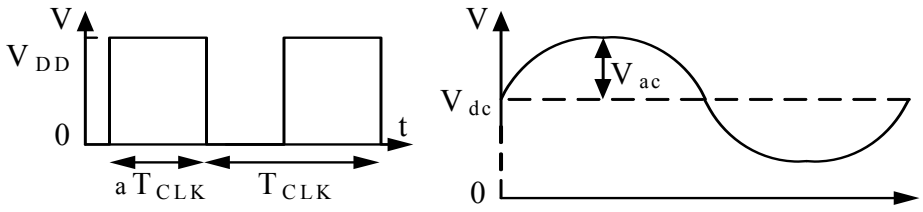

Figure 1.1: Typical operating patterns of digital and analog. Digital signals (left) are usually rail-to-rail square waves, while analog or mixed signals compose of DC and AC components (right).

A most challenging situation in analog circuits is that the degradation is highly sensitive to the DC biases applied to the transistors. In multiple stage circuits, the degradation of the present state is dependent on the degradation of the previous state, demanding an iterative flow that updates the DC biases of each transistor after an appropriate amount of time.

1.4 Contribution of This Work

This work proposes a suite of compact models and simulation methods to predict circuit aging in analog designs. It is compatible with other simulation and has better accuracy and efficiency. It starts from an integrated model for the leading aging mechanisms, NBTI and CHC, and then propagates the degradation of device parameters into circuit performance analysis. Distinct from previous efforts in this area [8][9][10][11], instead of application of extrapolation, the new solutions leverage *long-term predictive models* that recognize the unique stress patterns, directly calculate the degradation at a given point of time, and customize the simulation method to achieve the best efficiency and accuracy. Such solutions are compatible with today's analog design flows. They seamlessly close the gap between the underlying reliability physics and circuit/system analysis.

1.5 Thesis Outline and Organization

The organization of the thesis is as follows: Chapter 2 provides the background of NBTI and CHC effects; Chapter 3 introduces the static DC models of NBTI and CHC; Chapter 4 presents the long-term models of NBTI and CHC for analog/mixed-signal circuits; Chapter 5 briefly overviews current aging simulators and then describes the our simulation flow and demonstrates two circuit benchmarks; Chapter 6 summarizes the contributions of this thesis.

CHAPTER 2

NBTI AND CHC DEGRADATION

2.1 Introduction

Negative bias temperature instability (NBTI, in PMOS devices) and channel hot carrier (CHC, in NMOS devices) are two major reliability concerns in nanoscale regime. Both NBTI and CHC occur when a high voltage is applied at the gate of either NMOS or PMOS at elevated temperature. A unified approach based on the reaction-diffusion mechanism is used to explain both effects.

In NBTI, when a high negative electrical stress is applied at the gate of PMOS, interface traps are generated at the Si-SiO_2 interface [12]. NBTI manifests itself as an increase in threshold voltage V_{th}. When the stress is removed some of the interface traps are annealed, leading to partial recovery [13].

When the gate of NMOS switches, CHC occurs due to the generated of interface at the Si-SiO_2 interface only at the drain end. It also results in an increase in the absolute value of V_{th}. CHC is a permanent effect which is not recoverable, in contrast to the partially recoverable NBTI originated degradation.

In this chapter, the reaction-diffusion (R-D) model is presented to explain both NBTI and CHC effects. The predictive aging models due to NBTI and CHC developed based on R-D model under the simplest condition are then discussed.

2.2 Impact of CHC and NBTI

At the device level, the primary and major impact of NBTI and CHC is the increase in the absolute value of threshold voltage as shown in Fig.2.1. Mobility is also affected due to the longer column scattering and sub-threshold slope is increased due to aging. The impact of aging on threshold voltage gets significant with scaling due to thinner oxide thickness.

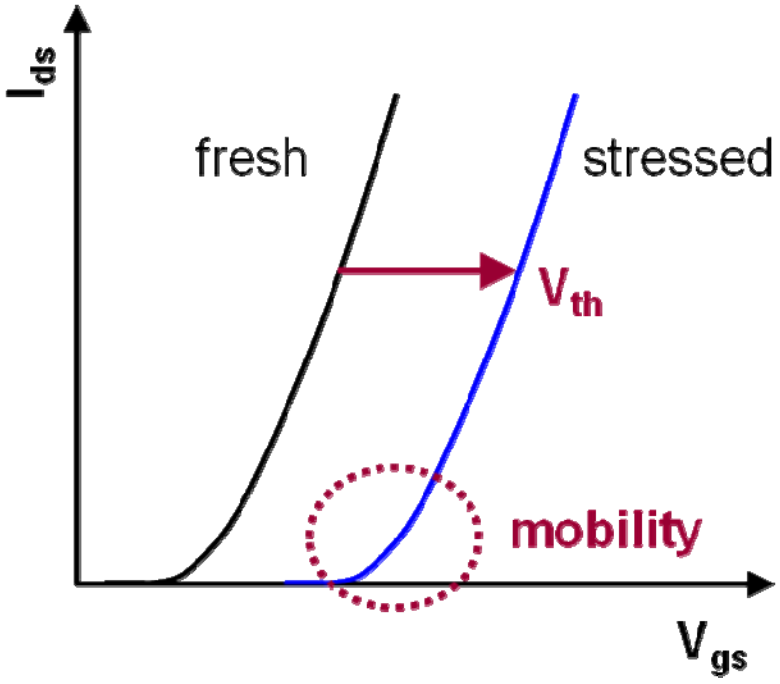

Figure 2.1: Impact of aging due to NBTI and CHC

At the circuit level, NBTI and CHC affect both analog and digital circuits. In digital design, aging impacts speed, power, noise margin, data stability and lifetime [14]. For analog circuits, the DC bias voltage and current will be changed, leading to change of circuit performance. In Fig.2.2 it is illustrated that

larger amount of electrical stress applied at the gate worsens the degradation, leading to a greater increase in V_{th}. The experiments were conducted on 65nm ring oscillator, where the shift of frequency is proportional to ΔV_{th}.[15]

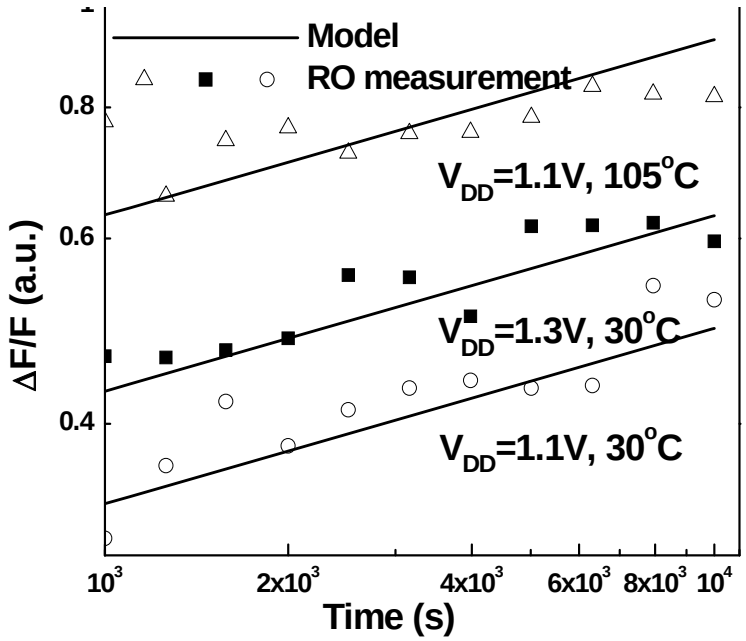

Figure 2.2: Aging of 65nm ROs under various temperatures and V_{DD}.[15]

2.3 Reaction-Diffusion Mechanism

Till date, the reaction-diffusion (R-D) model is the only model that successfully explains the power-law dependence of shift in the threshold voltage due to both NBTI and CHC. Both NBTI and CHC can be physically described as the generation of interface traps (charges) at the Si-SiO_2 interface. Based on this common theoretical framework, R-D model was proposed. This model assumes that when a gate voltage is applied, it initiates a field dependent reaction at the Si-SiO_2 interface that generates interface traps by breaking the passivated Si-H bonds. Fig.2.3 shows the cross-section of a transistor to illustrate R-D model.[16]

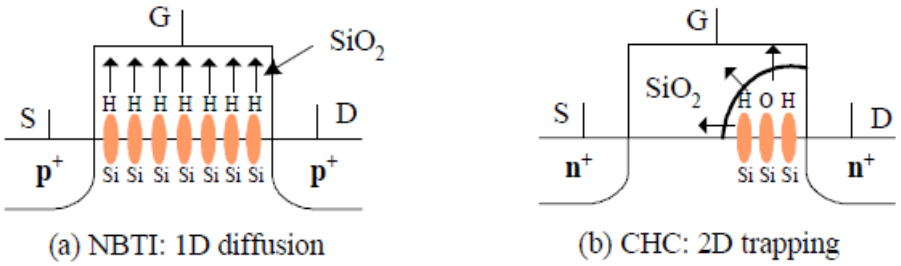

Figure 2.3: The reaction-diffusion mechanism (a) NBTI: 1D hydrogen species diffusion (b) CHC: 2D hot carriers trapping

There are two critical phases described in RD model:

1. Reaction. Under electrical stress, some Si-H or Si-O bonds at the substrate/gate oxide interface are broken [17]. In NBTI, it is the positive holes that trigger such reactions while in CHC it is the hot electrons [18]. Consequently, the interface charges are induced, causing increase of V_{th}. Given

the initial concentration of the Si-H bonds (N_o) and the concentration of inversion carriers (P), the generation rate of interface traps, N_{IT} is given by

$$\frac{dN_{IT}}{dt} = k_F(N_0 - N_{IT})P - k_R N_H N_{IT} \tag{2.1}$$

Where k_F and k_R are the reaction rates of forward and reverse reactions, N_0 is the hydrogen concentration [19]. The generation rate is an exponential function of electric field and temperature. And it is also proportional to the density of reaction species, namely holes and electrons [20].

2. Diffusion. The reaction generated interface charges diffuse away from the interface toward the gate, driven by the gradient of density. While NBTI happens uniformly in the channel, CHC impacts primarily the drain end, as shown in Fig.2.3. The process influences the balance of reaction and is governed by

$$\frac{dN_H}{dt} = D_H \frac{d^2 N_H}{dx^2} \tag{2.2}$$

The solution of equations (2.1) and (2.2) exhibits a power-law dependence on the time [5]. The exact value of the power-law index indicates the type of diffusion species [2].

CHAPTER 3

STATIC DEGRADATION MODELS OF NBTI AND CHC

3.1 NBTI Static Degradation Model

Negative bias temperature instability (NBTI) affects the drain current, V_{th}, etc., of the PMOS transistors. Due to the difference in flat band voltage, the NMOS transistor has a negligible level of holes in the channel and thus, does not suffer from NBTI degradation.

For a PMOS transistor, there are two phases of NBTI depending upon the bias condition of the gate. During the phase 1 when V_g=0 (i.e., V_{gs}=-V_{dd}), interface traps are generated diffusing the hydrogen atoms broken from Si-H bonds towards the gate. This phase is referred as “stress” or “static NBTI”. In phase 2, when V_g=V_{dd} (i.e., V_{gs}=0), the PMOS device is under pure recovery as hydrogen atoms closer to the interface diffuse back to the interface and anneal the broken Si-H bonds. This phase is referred as “recovery” and has a significant impact on the estimation of NBTI during the dynamic switching in digital operations. However in analog applications recovery is unlikely to happen as the transistors are always undergoing stress when operating.

Based on this reaction-diffusion model and considering the simplest case, in which the gate is under a constant stress with a DC voltage, the shift of threshold voltage can be given by:

$$\Delta V_{th} = \left(K_v^{\,2} t \right)^n \tag{3.1}$$

where n is the time exponent for NBTI which indicates the degradation rate. For a H_2 based diffusion model, n=1/6 and for a H based model, n=1/4. K_v has an exponential dependence on temperature (T) and electric field in the dielectric and this is called the static model.

$$K_v = \left(qt_{ox} / \varepsilon_{ox}\right)^3 K^2 C_{ox}(V_{gs} - V_{th})\sqrt{C}\exp\left(2E_{ox} / E_0\right) \tag{3.2}$$

where q is the electron charge, k is the Boltzmann constant, C_{ox} is the oxide capacitance per unit area, E_{ox} is the vertical electric field across the oxide and t_{ox} is the oxide thickness.[16]

3.2 CHC Static Degradation Model

Channel hot carrier (CHC) is another major degradation mechanism observed in MOSFETs. The main source of the hot carriers is the heating inside the channel of MOSFET during the circuit operation. These energetic carriers can lead to impact ionization within the substrate and the generated hot electrons or holes inside the channel or the heated carriers themselves can be injected in to the gate oxide.

NBTI occurs in standby mode, while hot carrier stress conditions are inherent in CMOS circuit operation. The diffusion occurs in right triangular prism fashion, while for CHC, it occurs in conical fashion as the traps are generated only at the drain end.

Based on this analysis, the threshold voltage shift due to CHC is given by

$$\Delta V_{th} = \frac{q}{C_{ox}} K_2 \sqrt{Q_i} e^{E_{ox}/E_{o2}} e^{-\varphi_{it}/q\lambda_f E_m} t^{n'} . \tag{3.3}$$

where Q_i is inversion charge, and time exponent n'=0.45.[16]

Table 3.1: Summary of NBTI and CHC static models.

$\Delta V_{th}(t)$	**NBTI**	$(K_v{}^2 t)^n$
	CHC	$\frac{q}{C_{ox}} K_2 \sqrt{Q_i} \exp(\frac{E_{ox}}{E_{o2}}) \exp(-\frac{\varphi_{it}}{q\lambda E_m}) t^{n'}$

K_v	$\left(\frac{qt_{ox}}{\varepsilon_{ox}}\right)^3 K_1{}^2 C_{ox}(V_{gs}-V_{th})\sqrt{C} \exp\left(\frac{2E_{ox}}{E_0}\right)$
Q_i	$C_{ox}(V_{gs}-V_{th})$
E_{ox}	$(V_{gs}-V_{th})/t_{ox}$

3.3 Model Verification

With the DC degradation model the performance of transistors under NBTI and CHC stress is predicted directly. Fig.3.1 shows a set of IV curves of single transistors after stress. Fig.3.2 further evaluates transconductance Gm of single transistors after stress. The models well predicts the degradation.

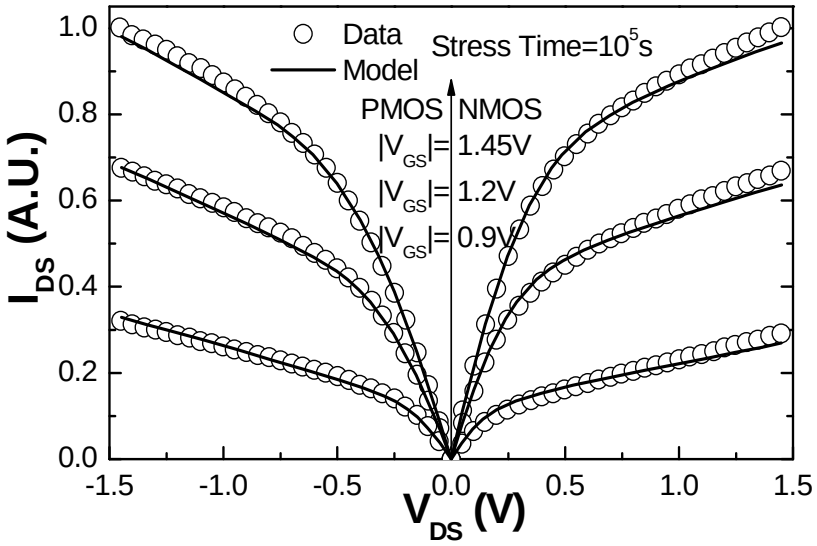

Figure 3.1: Performance degradation prediction of 65nm NMOS and PMOS IV characteristics.[16]

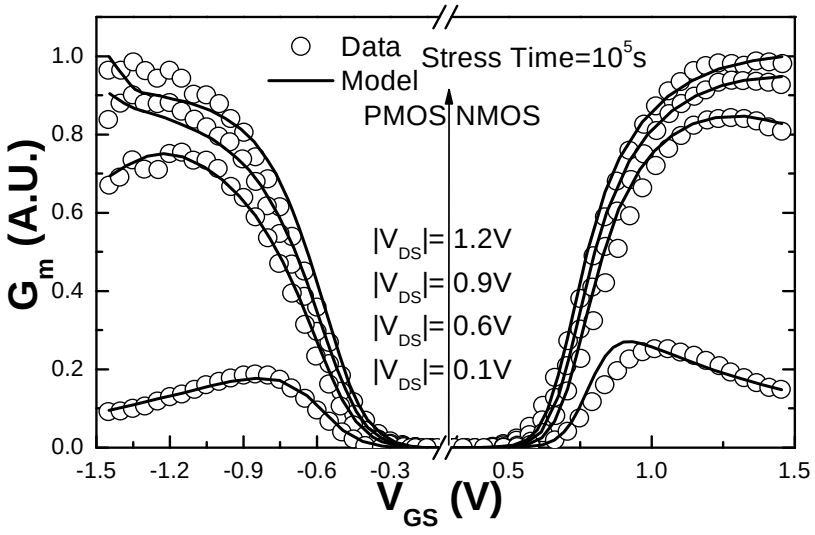

Figure 3.2: Performance degradation prediction of 65nm NMOS and PMOS transconductance characteristics.[16]

CHAPTER 4

LONG-TERM DEGRADATION MODELS FOR ANALOG/MIXED-SIGNAL CIRCUITS

4.1 Concerns and Requirement for Models Used in Analog/Mixed-Signal Circuits

Analog circuits have a wide range of input patterns unlike digital circuits. Analog inputs can be small signal sinusoidal voltage superimposed over a large signal DC typical in operational transconductance amplifiers (OTA) and large signal DC voltages, typical in comparators. Thus the models need to have both large signal DC component and small signal AC components as inputs.

Although it is possible to use the DC model to simulate the aging process, this kind of simulation requires the bias conditions frequently updated. To achieve enough accuracy the updating interval must be much smaller than signal period and this is called “real-time simulation”. For a typical analog signal with frequencies not lower than 100KHz such simulation cost too much and it is impossible to be applied in life-time simulation which considers a time scale of several years. Thus a long-term model is needed to handle the simulation.

The long-term model is supposed to be applied in predicting the device degradation over a large time scale rather than the detailed aging status within each period, which is impractical to collect. Considering a periodical wave form, the final status at the end of each period is much more than necessary. To improve efficiency the long-term models target at close forms of degradation behaviors.

With appropriate approximation a long-term model can achieve enough accuracy while at the same time keeps a simple form which consumes much less computing resources than real-time simulation.

4.2 NBTI Long-Term Model

Starting from static model with a constant gate stress from Eq.(3.1),

$$\Delta V_{th} = \left[\left(B \exp\left(2(V_{gs} - V_{th}) / E_0 t_{ox} \right) \right)^2 t \right]^n , \tag{4.1}$$

$$B = \left(q t_{ox} / \varepsilon_{ox} \right)^3 K_1^{\,2} C_{ox} \left(V_{gs} - V_{th} \right) \exp\left(-E_a / 2kT \right) / \sqrt{T_0} , \tag{4.2}$$

where B is proportional to V_{gs}-V_{th} Since the gate voltage changes with time continually,

$$d\left(V_{th}^{\,1/n} \right) = \left(B(V_{gs}) \exp\left(2(V_{gs} - V_{th}) / E_0 t_{ox} \right) \right)^2 dt , \tag{4.3}$$

$$V_{th}^{\,1/n} = \int_0^t \left(B(V_{gs}) \exp\left(2(V_{gs} - V_{th}) / E_0 t_{ox} \right) \right)^2 dt , \tag{4.4}$$

Therefore for any two time instants t_n and t_{n-1} (t_n>t_{n-1}), the degradation in V_{th} at time t_n is given by

$$\Delta V_{th}\left(t_n \right) = \left\{ \left(\Delta V_{th}\left(t_{n-1} \right) \right)^{1/n} + \left[B\left(V_{gs} \right) \mathrm{e}^{\frac{2\left(V_{gs} - V_{th} \right)}{E_{o1} t_{ox}}} \right]^2 \left(t_n - t_{n-1} \right) \right\}^n , \tag{4.5}$$

where $\Delta V_{th}(t_n)$ and $\Delta V_{th}(t_{n-1})$ are the degradations in threshold voltage at time instants t_n and t_{n-1} due to the applied DC+AC stress at the gate of a PMOS. However, to predict the degradation in long-term, it is impractical to predict ΔV_{th} for small intervals and keep updating. We show that it is possible to obtain a closed form solution for long-term as a function of $V_{gs,dc}$, $V_{gs,ac}$ and t.

$$\Delta V_{th}^{\,1/n} \approx \left[B\left(V_{gs,dc} \right) \mathrm{e}^{\frac{-2V_{th}}{E_{o1} t_{ox}}} \right]^2 \int_0^t \mathrm{e}^{\frac{4V_{gs}}{E_{o1} t_{ox}}} dt , \tag{4.6}$$

Since V_{gs} has both DC and AC components, it can be expressed as

$$V_{gs} = V_{gs,dc} + V_{gs,ac} \sin \omega t \,, \tag{4.7}$$

Substituting Eq.(4.6) into Eq.(4.7) and direct integrating will leads to Bessel Functions of the first kind. Without losing accuracy, Expanding the exponential term in Eq. (4.6) using the Taylor series at $V_{gs,dc}$ instead and noticing that when t is large enough, the trigonometric functions are of little significance, finally we have

$$\Delta V_{th} \approx \left[B\left(V_{gs,dc}\right) \mathrm{e}^{\frac{2\left(V_{gs,dc}-V_{th}\right)}{E_{o1}t_{ox}}} \right]^{2n} \left[t + \frac{1}{2}\left(\frac{4V_{gs,ac}}{E_{o1}t_{ox}}\right)^2 \frac{t}{2} + \frac{1}{24}\left(\frac{4V_{gs,ac}}{E_{o1}t_{ox}}\right)^4 \frac{3}{8}t \right]^n . \tag{4.8}$$

$V_{gs,ac}$ is the amplitude of the AC signal amplitude above the DC bias. Eq. (4.8) predicts the degradation in threshold voltage after a time t due to NBTI when a DC+AC gate stress is applied. It can be seen from the equation that the degradation is independent of the frequency of AC signal after a long time. This is consistent with the frequency independent behavior in digital operations [15][22].

4.3 CHC Long-Term Model

As in typical analog operation all NMOS transistors are in strong inversion, substitute $Q_i=C_{ox}(V_{gs}-V_{th})$, $E_{ox}=(V_{gs}-V_{th})/C_{ox}$ and $E_m=(V_{ds}-V_{dsat})/l_p$ into Eq.(3.3) we have:

$$d\Delta V_{th}^{1/n'} = \left[\frac{q}{C_{ox}} K_2 \sqrt{C_{ox}\left(V_{gs}-V_{th}\right)}\, \mathrm{e}^{\frac{V_{gs}-V_{th}}{t_{ox}E_{o2}} - \frac{\varphi_{it} l_p}{q\lambda_f (V_{ds}-V_{Dsat})}} \right]^{1/n'} dt\,, \tag{4.9}$$

Following similar procedure as in NBTI, and consider

$$V_{ds} = V_{ds,dc} + V_{ds,ac}\sin\omega' t$$

we have

$$\Delta V_{th}^{1/n'} \approx \left[\frac{q}{C_{ox}} K_2 \sqrt{C_{ox}\left(V_{gs,dc}-V_{th}\right)}\, \mathrm{e}^{\frac{V_{gs,dc}-V_{th}}{t_{ox}E_{o2}} - \frac{\varphi_{it} l_p}{q\lambda_f (V_{ds,dc}-V_{Dsat})}} \right]^{1/n'} F_2(t)\,, \tag{4.10}$$

where $F_2(t)$ is a linear function of time,

$$F_2(t) \approx t + \left[\left(b^2-2b\right)\frac{c^2}{2} + abc + \frac{a^2}{2} \right]\frac{t}{2}\,, \tag{4.11}$$

and a, b and c are dimensionless intermediate parameters decided by operating conditions.

$$a = \frac{V_{gs,ac}}{n' t_{ox} E_{o2}}, b = \frac{\varphi_{it} l_p}{n' q\lambda_f \left(V_{ds,dc}-V_{Dsat}\right)}, c = \frac{V_{ds,ac}}{V_{ds,dc}-V_{Dsat}}\,. \tag{4.12}$$

4.4 Long-Term Model Verifications

Fig.4.1 compares the NBTI degradation details within a wave period obtained from real-time simulation to the prediction by the long-term model results. The real-time simulation uses the static model and updates parameters at very short intervals. Two real-time simulation were run at different frequencies. The curve is by using long-term model and the symbols are from real-time simulation. According to the long-term model the difference in frequency will not lead to different result. As can be seen in the plot, although at the beginning the long-term model prediction varies from the real-time simulation, they finally converge after several cycles.

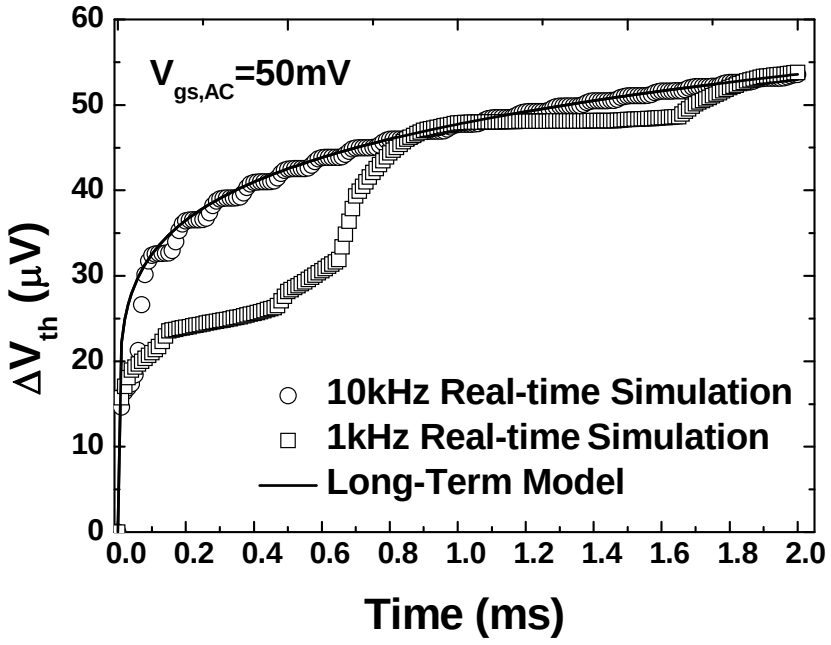

Figure 4.1: Comparison of ΔV_{th} degradation with small time scale.

Fig.4.2 further compares the ΔV_{th} degradation after a short time of stress at various stress conditions. The curve is by using long-term model and the symbols are from real-time simulation. The model is capable of various stress conditions.

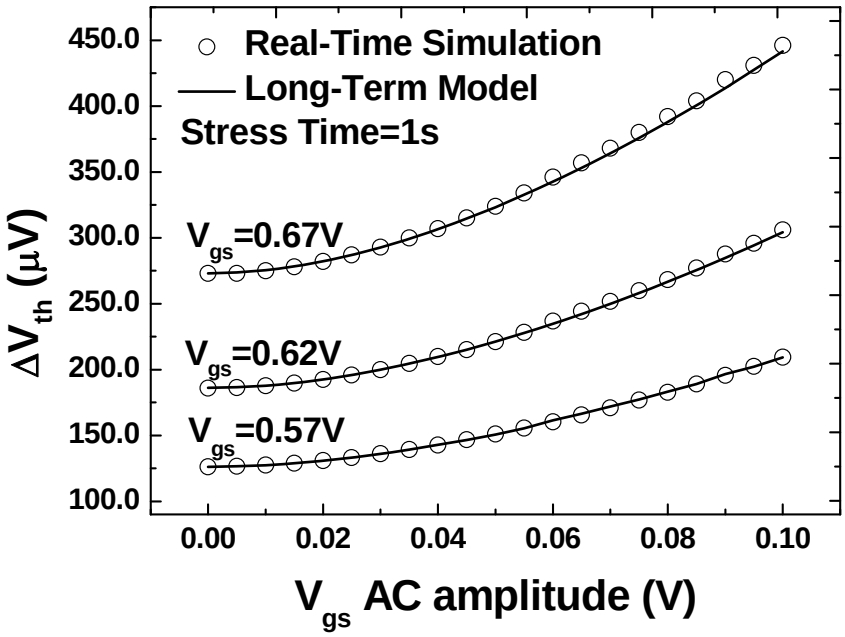

Figure 4.2: Comparison of ΔV_{th} at various stress conditions.

The simplification in the derivation of long-term models introduces errors. The long-term models are then compared with real-time simulation. The real-time simulation uses the DC model but updates parameters with fine step size which is much smaller than the periods of the AC signals.

As shown in Fig.4.3, larger small signal (AC signal) leads to larger error, which mainly stems from the approximations where $V \approx V_{dc}$, e.g. in Eq.(4.6) where $B\left(V_{gs}\right) \approx B\left(V_{gs,dc}\right)$ thus it can be taken out of the integration, simplifying the derivation. This is more notable for CHC model as it considers two AC values.

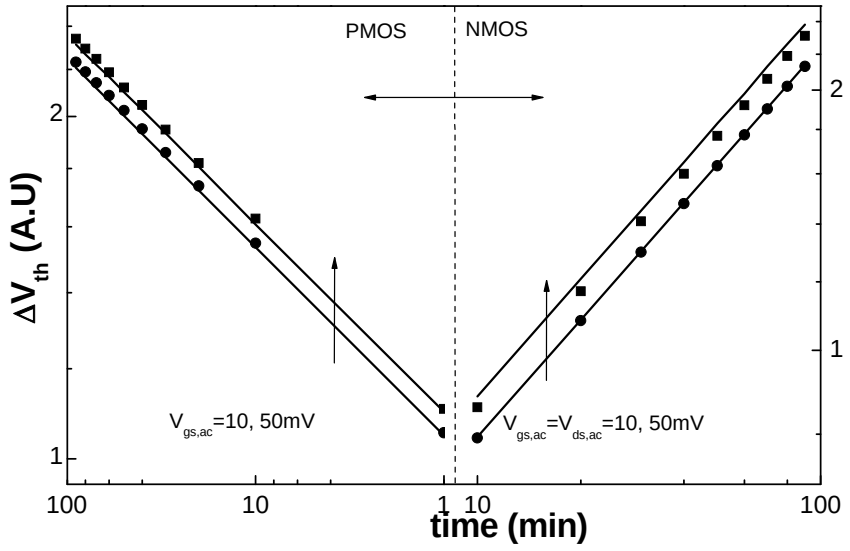

Figure 4.3: Long-term NBTI and CHC model validation. Axis are in lognormal.

As one can expect, the errors in long-term models accumulate over time for the distinct reason that the model requires V_{th} and operating voltages as its inputs which are all changing. This situation in circuit level is similar but more complicated with much more parameters gradually changing. To minimize the accumulated error, one can update the V_{th} value after a certain time step. Fig.4.4 shows that by updating the parameters, the accumulated error can be limited.

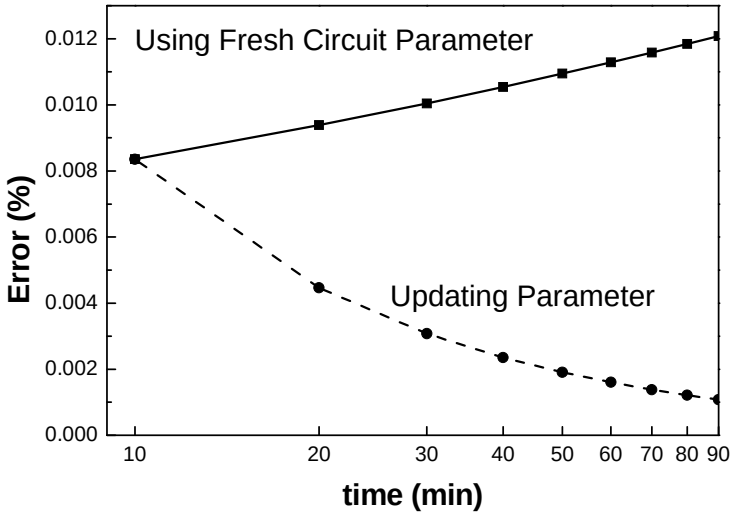

Figure 4.4: Long-term model error comparison. Using fresh device parameter values and using updated values lead to different trend in error accumulation.

For life-time prediction, deciding the step size plays an important role. Small step size can be more accurate but results in long simulation time, while large step size risks loss of accuracy. Some simulation tools changes step size dynamically based on degradation rate. However, with the long-term model, one can set the step size to a large constant value without losing much accuracy. Fig.4.5 shows the relative prediction error at life time=10years for different step size, comparing to one second step size. The error is very small that it is safe to set step size to 3 or 6 month in circuit level simulation, which will boost the simulation efficiency greatly.

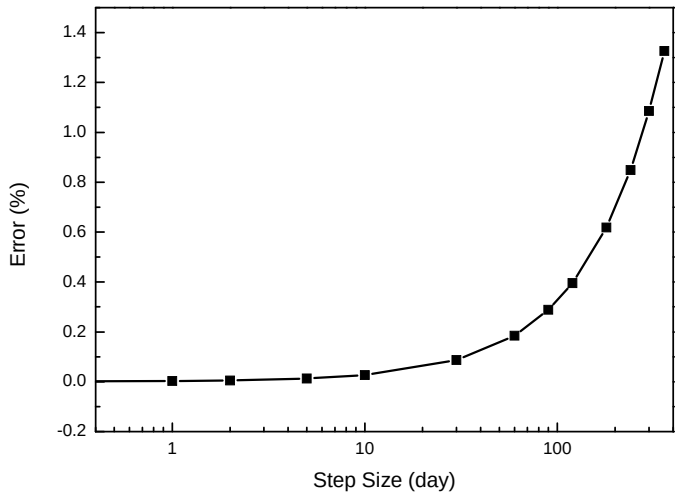

Figure 4.5: Trend of error versus step size.

4.5 Summary of Long-Term Models

Finally, the long-term model is summarized in Table 4.1. Unlisted parameters are the same as in [16].

Table 4.1: Summary of NBTI and CHC long-term models for analog.

NBTI	$\Delta V_{th} \approx \left[B\left(V_{gs,dc}\right) \mathrm{e}^{\frac{2\left(V_{gs,dc}-V_{th}\right)}{E_{o1}t_{ox}}} \right]^{2n} \left[t + \frac{1}{2}\left(\frac{4V_{gs,ac}}{E_{o1}t_{ox}}\right)^2 \frac{t}{2} + \frac{1}{24}\left(\frac{4V_{gs,ac}}{E_{o1}t_{ox}}\right)^4 \frac{3}{8}t \right]^n$
	$B = \left(qt_{ox}/\varepsilon_{ox}\right)^3 K_1^2 C_{ox}\left(V_{gs,dc}-V_{th}\right)\exp\left(-E_a/2kT\right)/\sqrt{T_0}$
CHC	$\Delta V_{th} \approx \frac{q}{C_{ox}} K_2 \sqrt{C_{ox}\left(V_{gs,dc}-V_{th}\right)}\, \mathrm{e}^{\frac{V_{gs,dc}-V_{th}}{t_{ox}E_{o2}} \frac{\varphi_{it} l_p}{q\lambda_f\left(V_{ds,dc}-V_{Dsat}\right)}} \left[F_2(t)\right]^{n'}$
	$F_2(t) \approx t + \left[\left(b^2-2b\right)\frac{c^2}{2} + abc + \frac{a^2}{2} \right] \frac{t}{2}$
	$a = \frac{V_{gs,ac}}{n' t_{ox} E_{o2}}, b = \frac{\varphi_{it} l_p}{n' q \lambda_f \left(V_{ds,dc}-V_{Dsat}\right)}, c = \frac{V_{ds,ac}}{V_{ds,dc}-V_{Dsat}}$

CHAPTER 5

SIMULATION METHOD

5.1 Concerns about Aging Prediction in Analog/Mixed-Signal Applications

Different operating conditions in analog and digital circuits lead to different approaches in modeling and simulation. The main circuit operation parameters defined in an analog circuit are large signal DC bias, small signal amplitude and small signal frequency that define the amount of stress on device.

One major concern in analog circuits is they are sensitive to DC biases applied to the transistors unlike the rail-to-rail signals in digital circuits. The degradation in one transistor affects the DC biases of other transistors in the next stage, changing its operation region and the amount of stress in that region. Thus the degradation of transistors in second stage is dependent on the degradation of transistors in the first stage. Also the effect of AC signal should be taken into account to help evaluate the degradation rate.

Another major concern is the potential time-dependent shift of circuit bias conditions. As the transistors undergo stress during operation, their performances changes over time. This changes circuit bias conditions naturally and the degradation rate is again dependent on the new bias conditions. Without updating bias conditions the error will accumulate over time and lead to huge difference in life-time prediction.

5.2 Brief Overview of Current Aging Simulators

Several simulators have been developed to perform aging analysis on the circuits. Most of them rely on transient simulation for a short time length and then obtain long-term prediction through extrapolation. In the following three of these simulators will be discussed.

5.2.1 Berkeley Reliability Tool (BERT)[23]

BERT is a reliability simulator developed in University of California, Berkeley.

The organization of BERT is as shown in Figure 5.1. In the first step, the pre-processor generated the intermediate files by running a transient simulation with SPICE. Then it passes the original SPICE deck to the circuit simulator and passes the node waveforms to the postprocessor. With these waveforms the post-processor calculates the amount of degradation each device undergoes depending on bias conditions and time. These degradation data are written into the Agetable file. Then pre-processor generates new SPICE model parameters for each stressed device according to the Agetable. A second SPICE simulation is run with the aged circuit.

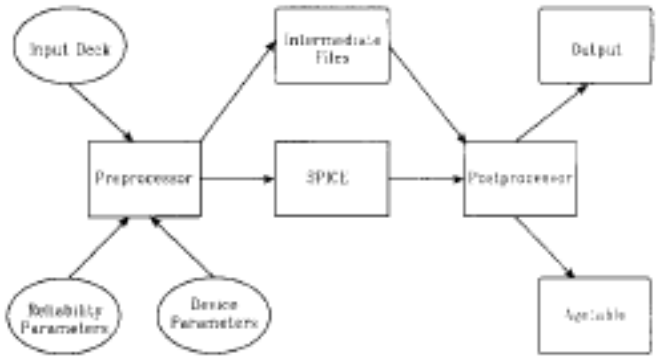

Figure 5.1: Organization of BERT [23].

The BERT does not consider the bias shift during the aging process and its final result relies on extrapolation. These drawbacks may lead to errors accumulated by time.

5.2.2 RelXpert [24][25]

RelXpert is the reliability simulator from Cadence Design Systems.

RelXpert uses a similar reliability analysis methodology close to the BERT simulator. SPICE simulations are run with the fresh model card. Using the currents obtained from the simulation, other reliability parameters and user defined reliability models, the Age of the device is calculated. Using this Age either the device degradation in a given time or the lifetime of the device for a set level of degradation can be determined. The final step is the AgeMOS extraction which simulates the behavior of the aged circuit.

The fundamental drawback of RelXpert is its reliance on extrapolation.

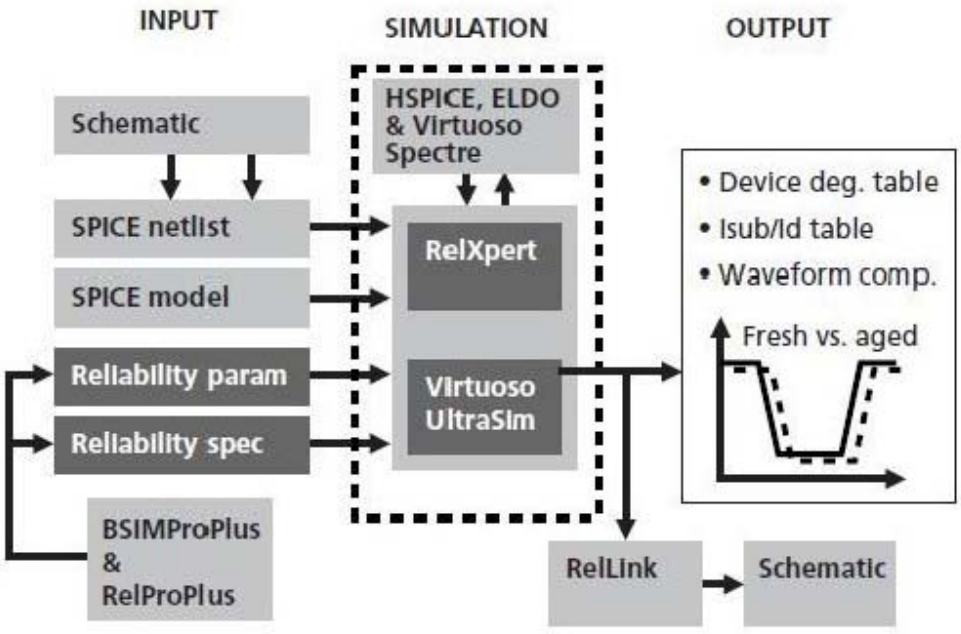

Figure5.2: Reliability simulation flow chart using RelXpert.

5.2.3 ELDO Aging Simulator [26]

The ELDO is a simulator from Mentor Graphics.

In ELDO the stress on each transistor over a transient time is determined. And then it is extrapolated to get the degradation over the total time. This degradation data is then used to update the model parameters in the model card which can be user defined. A simulation is run with the new model card and gives the aged circuit behavior.

In ELDO one can divide the total time into several segments and run iterative step simulation at the end of each the model parameters are updated. Thus it takes into account the time dependent bias shift during aging process. However, within each time interval it still relies on extrapolation.

5.3 Improved Simulation Flow for Analog/Mixed-Signal Aging Prediction

As discussed above, current simulation methods have two major drawbacks which limit the simulation accuracy:

1) The potential time dependent shift of bias condition and device parameters is not considered,
2) The calculation of degradation more or less relies on extrapolation from a short transient simulation.

To overcome the drawbacks we propose an improved simulation flow based on the long-term aging models discussed in last chapter. In this method an iterative flow is used that updates the DC biases after an appropriate amount of time, and during each time interval the long-term model is used to determined the degradation.

In analog circuits, each transistor node is subjected to any arbitrary voltage and since the degradation is exponentially dependent on electrical stress as shown in Eq.(1), the exact voltages at every node of the transistor have to be considered. This requires that before running an aging analysis, a circuit simulation is needed to obtain the operating points of all the nodes in the circuit. Contrary to current aging methodologies the simulation can either be a transient simulation or an AC/DC simulation. However, in some circuits, such as the A2D converter, transient simulations are very time consuming and thus for such circuits an AC/DC simulation can be done in order to determine the voltages on the nodes. In order to account for the changing bias points due to the degradation an iterative

simulation strategy is adopted where the biases are updated after an appropriate amount of time. The iterative aging simulation is performed by replacing the transistors with the aging sub-circuit as shown in Fig.5.4.

The stress conditions are applied to the netlist and the DC operating points and the stress voltages are obtained through AC/DC and transient simulation. With the stress voltage, aging analysis is performed using verilog-A module. To obtain accurate results, several iterations are run in appropriately smaller time steps. This means that to determine the degradation after time T years, we will need to run N simulations such that each step is t_{step}=T/N. After each step, the new bias points are determined and the stress conditions are updated in the netlist externally using perl scripts and the simulation is rerun. At the final stage, the circuit characteristics at the final stress time (T years) are obtained.

For comparison, current simulation methodology can be summarized into a flow as in Fig.5.3, though some vary in detail. And our improved approach is highlighted in parallel. It is compatible with current methods and overcomes their drawbacks, improving accuracy and efficiency of circuit level aging prediction.

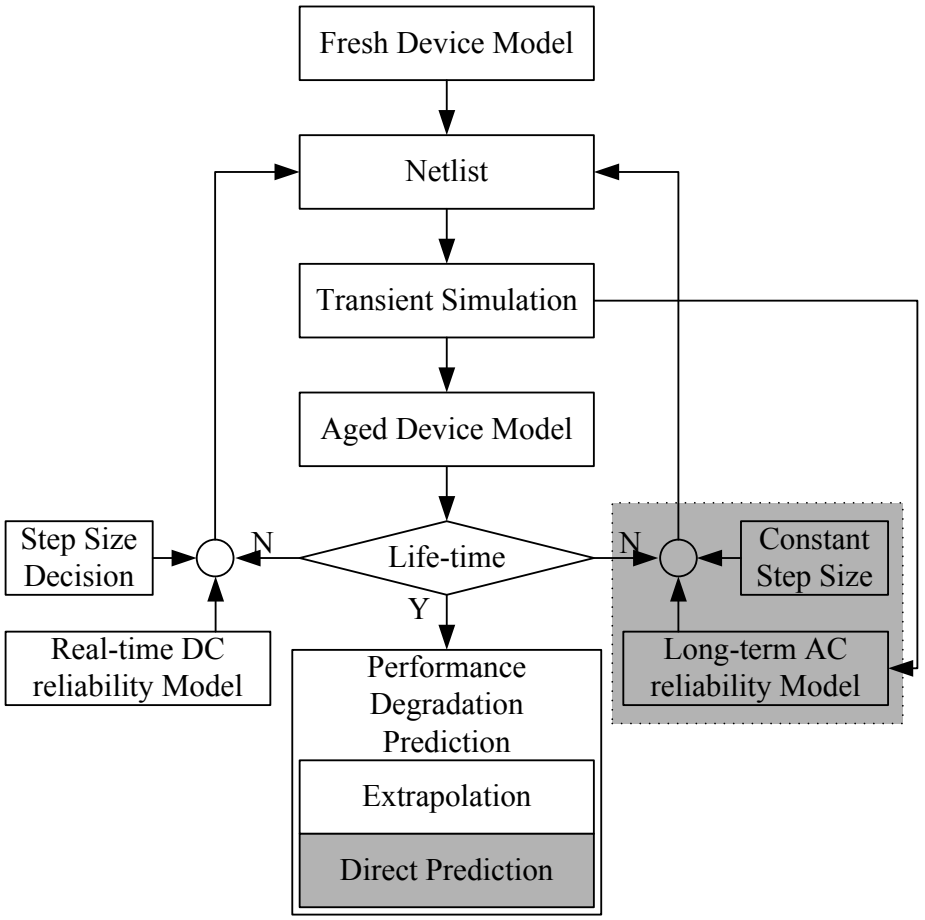

Figure 5.3: Simulation flow comparison. The contribution of our approach is highlighted.

5.4 Model Implementation

For the SPICE level implementation, an aging sub-circuit for MOSFET is defined as shown in Fig.5.4 where every transistor in the design will be replaced with this sub-circuit. The change in V_{th} due to NBTI or CHC degradation is calculated using the long term models implemented in Verilog-A module and is applied as an additional gate voltage in order to update the effective V_{th} of the device [27]. Simulation of the circuit using this sub-circuit with aging turned on simulates the circuit as it would at time T years. And the effect of the degradation on the circuit parameters like node voltages can be determined by measurement command.

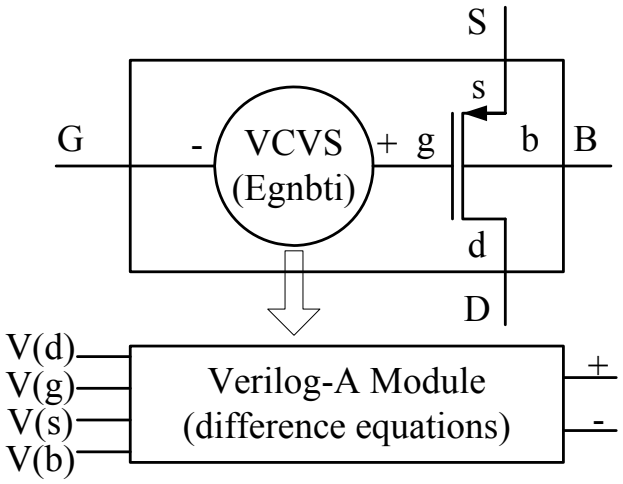

Figure 5.4: Spice model implementation.

5.5 Circuit Benchmark

5.5.1 PMOS Comparator

The NBTI aging analysis is demonstrated on a PMOS input comparator with 65nm technology node as shown in Fig.5.5. The comparator is used to measure the difference between the input signals and the reference signals. When the input signals match the reference signals the v_{o+}- v_{o-} offset is zero and when they do not match the offset is non-zero. In the zero offset case, that is when the input signals match the reference signals the two legs of comparator undergo equal stresses and thus there will not be any affect of degradation on the offset. However when the input signals do not match the reference signals there will be unequal stresses on the transistors thereby causing the offset to be non-zero even when matching signals are applied.

The prediction of mismatch in the time scale of 10 years is shown in Fig.5.6. The result is compared with one time prediction using the long-term model and fresh circuit parameters. The finite step method leads to a more optimistic prediction. Also the model continuity is shown.

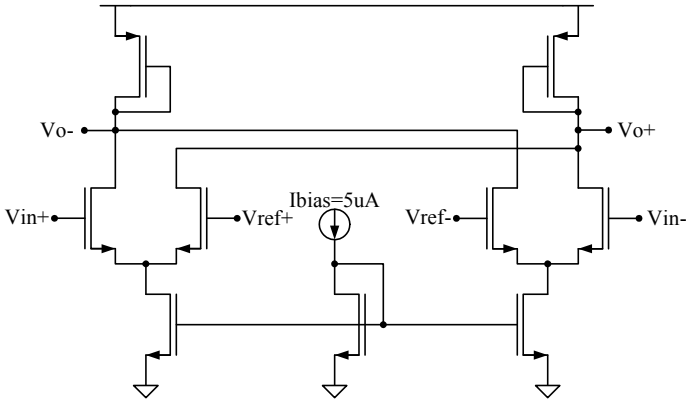

Figure 5.5: PMOS comparator schematic.

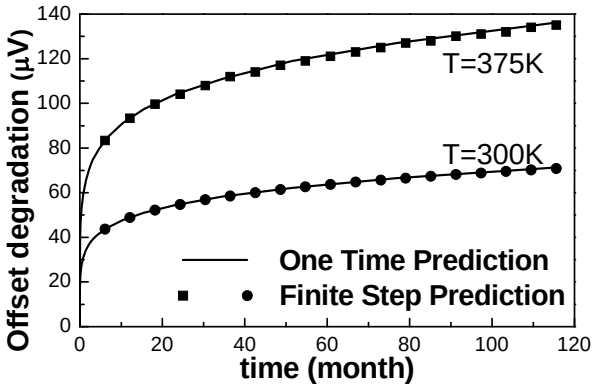

Figure 5.6: PMOS comparator simulation result. Curves are prediction using long-term model with only one calculation. Symbols are finite step simulation with updated parameters and multiple calculation.

5.5.2 NMOS Mixer

We evaluated the proposed model on the front end of a RF frequency wideband direct-conversion receiver in 0.18um CMOS. The schematic is shown in Fig.5.7. Bias circuit is not drawn. The receiver front end consists of a source degenerated cascade LNA and a doubly balanced Gilbert mixer and operates at frequencies between 2GHz and 3.2GHz. The LNA circuit amplifies the incoming RF signal with a very low noise injection to achieve the highest SNR (signal to noise ratio) possible, while the mixer down-converts the amplified RF signal to baseband. Conversion gain of the receiver is 21dB at the center frequency, while input (s11) and output (s22) matching are below -10db. Noise figure of the receiver chain is 4dB and power dissipation is 24mW with a 1.8V supply. 1dB compression point and input referred third order intercept point are -25 dBm and -15dBm respectively.

Fig.5.8 shows the performance degradation using direct prediction. Although the degradation value is small, it is demonstrated that this method is efficient.

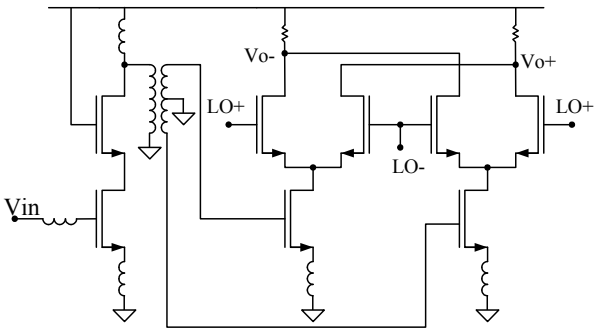

Figure 5.7: Schematic of the LNA and mixer. LO+ and LO- are generated by bias circuit which is not included in this schematic. Vo+ and Vo- are the differential output.

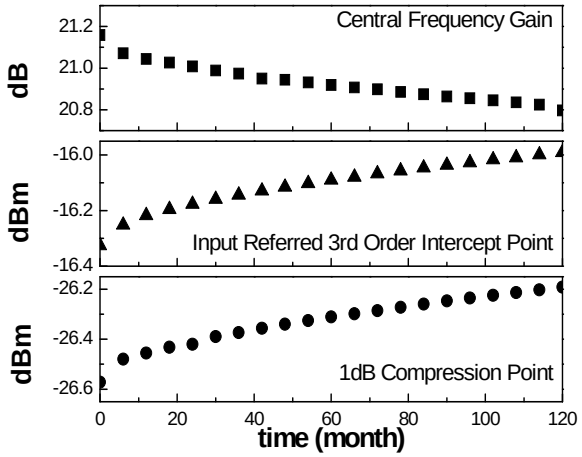

Figure 5.8. Mixer performance degradation prediction result for time=10 years.

CHAPTER 6

SUMMARY

6.1 Thesis Conclusions

This thesis is a study of device degradation models of NBTI and CHC effects and circuit level aging simulation in analog/mixed-signal circuits. The specific contributions of this thesis include:

6.2 Future Work

The models and simulation methods proposed in this work provide a new approach for analog/mixed-signal circuit aging analysis. However this work requires additional work to be a comprehensive and accurate reliability tool. A few suggestions for future work are as follows:

1) There are many physical mechanisms other than NBTI and CHC that also lead to circuit reliability problems. Current simulation flows may need add-ons to incorporate other mechanisms and their effects.
2) The set of models and simulation method can help circuit designers improve their designs if they are implemented into industrial tools.

REFERENCES

[1] G. E. Moore, “Cramming more components onto integrated circuits,” Electronics, vol. 38, no. 8, Apr. 1965.

[2] S. Bhardwaj, W. Wang, R. Vattikonda, Y. Cao, and S. Vrudhula, “Predictive modeling of the NBTI effect for reliable design,” CICC, pp. 189–192, Sept. 2006.

[3] D. K. Schroder and J. A. Babcock, “Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing,” Journal of Applied Physics, vol. 94, no. 1, pp. 1–18, Jul. 2003.

[4] M. A. Alam and S. Mahapatra, “A comprehensive model of PMOS NBTI degradation,” Microelectronics Reliability, vol. 45, pp. 71–81, Aug. 2005.

[5] R. Vattikonda, W. Wang, and Y. Cao, “Modeling and minimization of PMOS NBTI modeling and the impact of input vector control on performance degradation”, *Design, Automation and Test in Europe Conference and Exhibition*, pages 1–6, April 2007.

[6] S. Bhardwaj, W. Wang, R. Vattikonda, Y. Cao, and S. Vrudhula, “Predictive modeling of the NBTI effect for reliable design,” CICC, pp. 189–192, Sept. 2006.

[7] V. Reddy, A. T. Krishnan, A. Marshall, J. Rodriguez, S. Natarajan, T. Rost, and S. Krishnan, “Impact of negative bias temperature instability on digital circuit reliability,” IRPS, pp. 248–254, Apr. 2002.

[8] R. H. Tu, et al.,“Reliability effects on MOS transistors due to hot-carrier injection,” IEEE Transactions onComputer Aided Design of Integrated Circuits and Systems, vol. 12, no. 10, pp. 1524–1534, Oct. 1993.

[9] E. Maricau and G. Gielen, “Reliability simulation of analog ICs under time varying stress innanoscale CMOS,” IEEE Workshop on Design for Reliability and Variability, 2008.

[10] E. Maricau, P. D. Wit, and G. Gielen, “An analytical model for hot carrier degradation in nanoscale CMOS suitable for the simulation of degradation in analog IC applications,” Microelectronics Reliability, vol. 48, no. 8-9, pp. 1576–1580, Aug/Sept 2008.

[11] X. Li, J. Qin, B. Huang, X. Zhang, and J. B. Bernstein, “A new SPICE reliability simulation method for deep submicron CMOS VLSI circuits,” TDMR, 2006.

[12] S. Ogawa and N. Shiono, “Generalized diffusion-reaction model for the low-field charge build up instability at the Si-SiO2 interface”, *Physical Review*, 51(7):4218–4230, Feb. 1995.

[13] S. Mahapatra, D. Saha, D. Varghese, and P. B. Kumar, “On the generation and recovery of interface traps in mosfets subjected to nbti, fn, and hci stress”, *IEEE Tran. on Electron Devices*, 53(7):1583–1592, Jul. 2006.

[14] S. Chakravarthi, A. T. Krishnan, V. Reddy, C. F. Machala, and S. Krishnan, “A comprehensive framework for predictive modeling of negative bias temperature instability”, *IEEE International Reliability Physics Symposium*, pages 273–282, 2004.

[15] R. Zheng, et al., “Circuit aging prediction for low-power operation”, *Customs Integrated Circuits Conference*, pp. 427-430, 2009.

[16] W. Wang, V. Reddy, A. T. Krishnan, R. Vattikonda, S. Krishnan and Y. Cao, “Compact modeling and simulation of circuit relaibility for 65nm CMOS technology”, *IEEE Transactions on Device and Materials Reliability*, vol. 7,no. 4, pp. 509-517, 2007.

[17] S. Mahapatra, P. B. Kumar, and M. A. Alam, “Investigation and modeling of interface and bulk trap generation during negative bias temperature instability of p-mosfets”, *IEEE Tran. on Electron Devices*, 51(9):1371–1379, Sep. 2004.

[18] K. Chen, S. A. Saller, I. A. Groves, and D. B. Scott, “Reliability effects on mos transistors due to hot-carrier injection”, *IEEE Tran. on Electron Devices*, 32(2):386–393, Feb.1985.

[19] W. Wang, V. Reddy, A. T. Krishnan, R. Vattikonda, S. Krishnan, and Y. Cao, “An integrated modeling paradigm of circuit reliability for 65nm CMOS technology,” CICC, pp. 511–514, 2007

[20] M. A. Alam, “On the reliability of micro-electronic devices: An introductory lecture on negative bias temperature instability”, *Nanotechnology 501 Lecture Series*, Sep. 2005.

[21]

[22] W. Wang, et. al., “The impact of NBTI on the performance of combinational and sequential circuits,” DAC, pp. 364–369,Jun. 2007

[23] R.T. Hu, et. al., “Berkeley Reliability Tools-BERT”, *IEEE Tran. On Computer Aided Design of Integrated Circuits and Systems*, vol. 12, no. 10, 1993.

[24] “Virtuoso relxpert reliability simulator user guide, Product version 7.0.1,” June 2008.

[25] “Reliability simulation in integrated circuit design,” available at: http://www.cadence.com/.

[26] “Eldo UDRM user’s manual, Release AMS 2009.1.”

[27] R. Vattikonda, et al.,“A new simulation method for NBTI analysis in SPICE environment,” International Symposium on Quality Electronic Design, pp. 41–46, 2007.

APPENDIX A

VERILOG A CODE FOR LONG-TERM NBTI

```
`include "disciplines.vams"
`include "constants.vams"
 module nbti_lt(ng,ns,pos,neg);
parameter real Eah2=0.49;
parameter real E0 = 0.08;
 parameter real q=1.6e-19;
 parameter real eox=3.4515e-20;
 parameter real T0=1e-8;
 parameter real K=7.5;
 parameter real KT=32.634e-3;
 parameter real B=exp(-Eah2/KT);
 parameter real C=B/T0;
 parameter real n=0.1666666667;
 parameter real Vgs=1.6;
 parameter real stress_time=0 from [0:100000000];
 parameter real eps1=0.9;
 parameter real eps2=0.5;
  parameter real tclk=0.01;
 parameter real alpha= 0.5;
 parameter real t_one=1e-5;
 parameter real Tox=2.2;
parameter real Vth=0.18;
```

```
//*********Variables**********//
real Eox;
real Cox;
real alpha_tclk;
real alpha_prime;
real Kv;
real i;
real year;
real T;
real t;
real te;
real beta;
real Dvth;
real D;
real t0;
// real Vgs;
real del_Vth;
real vth_shift;
real vth_shift_recovery;
real V1;
real V2;
input ng,ns;
```

```
output pos,neg;
electrical pos,neg,ng,ns;
analog
begin
 V2=V(ns);
V1=V(ng);
 Eox=(Vgs-Vth)/Tox;
Cox=eox/Tox;
alpha_tclk=alpha*tclk;
alpha_prime=(1-alpha)*tclk;
Kv = pow(((q * Tox) / eox), 3) * (pow(K, 2) * Cox * (Vgs - Vth) * pow((exp(Eox
/ E0)),2) * sqrt(C));
//if(t-t0>t_one)
//begin
//te=Tox;
//end
//else
//begin
//te=Tox*sqrt((t-t0)/t_one)-sqrt(eps2*C*(t-t0)/eps1);
//end
//if (Vgs>Vth)
//begin
```

```
//vth_shift=pow((Kv*pow((t-t0),0.5)+pow(del_Vth,1/(2*n))),(2*n));
///end
//else
//begin
////vth_shift=del_Vth*(1-((2*eps1*te+sqrt(eps2*C*(t-t0)))/(2*Tox+sqrt(C*t))));
 // vth_shift=del_Vth*(1-((2*eps1*te+sqrt(eps2*C*(t-t0)))/(2*Tox+sqrt(C*t))));
//end
//del_Vth=vth_shift;
//$display("change in Vth=%g",del_Vth);
///$display("Vgs=%g",Vgs);
// V(pos,neg) <+ del_Vth;
//t0=t;
 //end
 if (Vgs>Vth)
 begin
  vth_shift = pow((Kv*sqrt(stress_time)),2*n);
 end
  //$display("Vgs=%g, vth_shift=%g, stresstime=%g,
kv=%g",Vgs,vth_shift,stress_time,Kv);
 V(pos,neg)<+ vth_shift;
 end
endmodule
```

APPENDIX B

VERILOG A CODE FOR LONG-TERM CHC

```
include "disciplines.vams"
`include "constants.vams"
module chc_lt(ng,nd,ns,pos,neg);
 //************  Constant parameters  **************//
  parameter real K = 1.95e8;                        // unit is nm C^(-0.5) //
  parameter real E0 = 0.8;                         // unit is V/nm //
  parameter real q = 1.6e-19;                       // unit is Coul //
  parameter real eox = 3.4515e-20;                    //3.9*(8.85*10^(-21)), unit is
F/nm //
  parameter real Vt = 0.0259;                       // unit is eV, 0.0259 is for T=300K
//
//  parameter real Esat = 0.011;                      // unit is V/nm
  parameter real l = 17;                           // unit is nm //
  parameter real phi = 5.92e-19;                     // 3.7*1.6e-19 unit is J //
  parameter real Lambda = 7.8;                       // unit is nm //
//  parameter real Abulk = 0.62;                      // no unit was=0.005 //
  parameter real n = 0.45;                         // no unit //
  parameter real n1 = 1/n;                         // no unit //
//*******Technology parameters   (65nm)**********//
  parameter real Tox = 2.2;                         // unit is nm //
  parameter real Vth = 0.38;                        // unit is V //
  parameter real Cox = eox/Tox;                      // unit is F/nm^2 //
```

```
 parameter real Leff = 35;                    // unit is nm //
 parameter real vsat = 1.3e14;                  // unit is nm/s //
 parameter real theta = 0.95;                  // unit is V^-1 //
 parameter real u0 = 235e14;                    // unit is nm^2/Vs //
//*****************************************//
 parameter real Vsupply = 1.5 from [0.8:1.8];
parameter real VGS=1.6 from [0.3:1.8];
 parameter real VDS=1.6 from [0.3:1.8];
 parameter real stress_time=0 from [0:31536000];
//************** variables*******************//
 real current_time;
 real prev_time;
 real delta_t;
 real vth_shift;
 real Vgs1;
 real Vds1;
 real Eox;
 real Vdsat;
 real Em;
 real delta_vth0;
 real term1;
 real A;
```

```
 real B;
 real term3;
 real ueff;
 real Esat;
  real V1;
 real V2;
//  real stress_time;
 // real VGS;
 input ng,nd,ns;
 output pos,neg;
 electrical pos,neg,ns,ng,nd;
 analog
 begin
  V1=V(ng);
 V2=V(ns);
  // VGS = V(ng)-V(ns);                  // instantaneous value of Vgs
 //     Vds1 = V(nd)-V(ns);                  // instantaneous value of Vds
//      stress_time=$abstime;
//      delta_t = stress_time - prev_time;
            if(VGS > Vth)  // Vgs > Vthn then nmos is strong inversion region
      begin
              ueff = u0/(1+(theta*(VGS-Vth)));
```

```
        Esat = 2*vsat/ueff;
        Vdsat = (Esat *Leff*(VGS-Vth))/((Esat*Leff)+(VGS-Vth));
        if(VDS > Vdsat)
        begin
//          if(Vds1 > Vsupply) // HACK! Ignore overshoot in output until I figure
out how to fix it in the simulator.
//            begin
 //             Vds1 = Vsupply;
  //          end
          Em = (VDS-Vdsat)/l;
                  Eox = (VGS-Vth)/Tox;                  // unit is V/nm //
                  // term1 = Cox*delta_vth0/q;
         B=exp(-phi/(q*Lambda*Em));
          A = K * sqrt(Cox*(VGS-Vth)) * exp(Eox/E0) *B;
          //term3 = pow(term1,n1) + (pow(A,n1) * delta_t);
          term3=A*pow(stress_time,n);
                        // vth_shift = q/Cox * pow(term3,n);
                  vth_shift= q/Cox*term3;
                end
       end
     //  $display("A=%g, term3=%g, stresstime=%g, vth_shift=%g",A, term3,
stress_time,vth_shift);
```

```
        //$display("VGS=%g, Vdsat=%g Vg=%g Vs =%g B=%g A=%g",VGS,
Vdsat, V1, V2, B, A);
        // delta_vth0 = vth_shift;
        // prev_time = stress_time;
        $display("VGS=%g, vth_shift=%g,
stresstime=%g",VGS,vth_shift,stress_time);
         V(pos,neg) <+ vth_shift;
    end
endmodule
```

APPENDIX C

PERL SCRIPT FOR AGING ANALYSIS SIMULATION

```
#!/usr/bin/perl

# Runs the psuedoreal analysis on a given input netlist.

$start = time();

$start_time = localtime($start);

print "\n\nStart Time is $start_time\n\n";

#input arguments

if ($#ARGV == -1) {

  print "syntax : aging_analysis.pl -i <input filename> -s <stress interval> -t <total

stress time> -c <temp>\n";

  print "          -i : input spice filename\n";

  print "          -s : stress interval used in the psuedo long term analysis\n";

  print "          -t : total stress time\n";

  print "          -c : simulation temperature in Celsius\n";

  print "          -h : print help\n";

  die "no arguments given : $!";

}

elsif(($#ARGV == 0) && shift(@ARGV) =~ /-h/){

  print "syntax : aging_analysis.pl -i <input filename> -s <stress interval> -t <total

stress time> -c <temp>\n";

  print "          -i : input spice filename\n";

  print "          -s : stress interval used in the psuedo long term analysis\n";

  print "          -t : total stress time\n";
```

```
  print "            -c : simulation temperature in Celsius\n";
  print "            -h : print help\n";
  die "print help end\n";
}
elsif($#ARGV != 7){
  print "syntax : aging_analysis.pl -i <input filename> -s <stress interval> -t <total
stress time> -c <temp>\n";
  print "            -i : input spice filename\n";
  print "            -s : stress interval used in the psuedo long term analysis\n";
  print "            -t : total stress time\n";
  print "            -c : simulation temperature in Celsius\n";
  print "            -h : print help\n";
  die "Arguments missing : $!";
}
else {
  while ($#ARGV >= 0){
    $compare = shift(@ARGV);
    if($compare =~ /-i/){
      $input_file = shift(@ARGV);
    }
    elsif($compare =~ /-s/){
      $stress_interval = shift(@ARGV);
```

```
    }
    elsif($compare =~ /-t/){
      $stress = shift(@ARGV);
    }
    elsif($compare =~ /-c/){
      $temp = shift(@ARGV);
    }
    else{
      print "syntax : aging_analysis.pl -i <input filename> -s <stress interval> -t
<total stress time> -c <temp>\n";
      print "          -i : input spice filename\n";
      print "          -s : stress interval used in the psuedo long term analysis\n";
      print "          -t : total stress time\n";
      print "          -c : simulation temperature in Celsius\n";
      print "          -h : print help\n";
      die "Wrong Arguments : $!";
    }
  }
}
#parse through the spice file to get the transistor names used in the design
@transistor_list = "NULL";
@aging_mechanism = "NULL";
```

```
$sub_name_found = 0;
open (FH_sp, "<$input_file") or die "can't open $input_file: $!";
while(my $line = readline(*FH_sp)){
  @line_split = split(' ', $line);
  if(@line_split[0] =~ /xs/){
    @line_split[0] =~ s/xs//;
    push(@transistor_list, @line_split[0]);
    if(@line_split[5] =~ /pnbti/ || @line_split[5] =~ /nchc/){
      push(@aging_mechanism,@line_split[5]);
    }
    else {
      die "Unknown Looking for pnbti or nchc. Found @line_split[5] ";
    }
  }
  elsif(@line_split[0] =~ /subckt/){
    $sub_name = @line_split[1];
    $sub_name_found = 1;
  }
  elsif($sub_name_found == 1 && $line =~ /$sub_name/){
    $sub_num = @line_split[0];
  }
}
```

```
shift(@transistor_list); #shift out the NULL which is the first element of the array
shift(@aging_mechanism); #shift out the NULL which is the first element of the
array
$num = @transistor_list;
#print "\n\ntransistor list = @transistor_list , number = $num sub=$sub_num\n\n";
close FH_sp or die "can't close $input_file: $!";
# writing the initial values for the degraded parameters used in the simulation
# setting the degraded vth (delvth) and the initial operating points used in the
# degradation calculation to 0.
$op_file = "parameter_op.sp";
$delvth_file = "parameter_delvth.sp";
$aging_file = "parameter_aging.sp";
print "\n\n********** Writing initial parameter_op_psuedo.sp
**********\n";
open (FH_param, ">$op_file") or die "can't open $op_file: $!";
print FH_param "*This file is generated by the script aging_analysis.pl\n\n";
for($j=0;$j<$num;$j++){
  $param = "vgdc"."@transistor_list[$j]";
  print FH_param ".param $param=0\n";
  $param = "vgac"."@transistor_list[$j]";
  print FH_param ".param $param=0\n";
  $param = "vddc"."@transistor_list[$j]";
```

```
  print FH_param ".param $param=0\n";
  $param = "vdac"."@transistor_list[$j]";
  print FH_param ".param $param=0\n";
}
close FH_param or die "can't close $parameter_file: $!";

print "\n\n**************** Writing initial parameter_delvth.sp ****************\n";
open (FH_delvth, ">$delvth_file") or die "can't open $delvth_file: $!";
print FH_delvth "*This file is generated by the script aging_analysis.pl\n\n";
@delvth_array = "NULL";
@delvth_val = "NULL";
for($j=0;$j<$num;$j++){
  $param = "delvth"."@transistor_list[$j]";
  push(@delvth_array,$param);
  push(@delvth_val,0);
  print FH_delvth ".param $param=0\n";
}
shift(@delvth_array);
shift(@delvth_val);
close FH_delvth or die "can't close $delvth_file: $!";
# creating the output files
```

```
$temp_file = $input_file;
$temp_file =~ s/.sp//;
$degrad_file = "output/"."$temp_file"."_degrad.dat";
open (FH_degrad, ">$degrad_file") or die "can't open $degrad_file: $!";
print FH_degrad "#This file is generated by the script aging_analysis.pl\n\n";
print FH_degrad "Time(sec)\t\t\t\t@delvth_array\n";
# Measuring the output parameters at time=0
$temp_file = $input_file;
$temp_file =~ s/.sp//;
$measure_file = "$temp_file"."_measure.sp";
# NBTI Analysis begins...
$time=$stress_interval;
for($i=0;$i<$stress;$i=$i+$stress_interval){
  # Stressing the circuit and determining the operating points for this stressed
  # condition
  $temp_file = $input_file;
  $temp_file =~ s/.sp//;
  $stress_file = "$temp_file"."_stress.sp";
  #print "\n\nstress file = $stress_file\n\n";
  open (FH_aging, ">$aging_file") or die "can't open $aging_file: $!";
  print FH_aging "*This file is generated by the script aging_analysis.pl\n\n";
  print FH_aging ".param stresstime=0\n";
```

```
  print FH_aging ".param temperature=$temp\n";
  print FH_aging ".include '$stress_file'\n";
  print FH_aging ".hdl nbti_l_analog.va\n";
  print FH_aging ".hdl chc_l_analog.va\n";
  close FH_aging or die "can't close $aging_file: $!";
  print "\n\n***************Running Circuit Simulation Under Stress Conditions ***************\n";
  system("hspice -i $input_file -o output/out_stress");
  print "\n\n***************Extracting Operating Points***************\n";
  system("./operating_points.pl -i output/out_stress.lis");
  # Measuring the degraded vth
  open (FH_aging, ">$aging_file") or die "can't open $aging_file: $!";
  print FH_aging "*This file is generated by the script aging_analysis.pl\n\n";
  print FH_aging ".param stresstime=$stress_interval\n";
  print FH_aging ".param temperature=$temp\n";
  print FH_aging ".include '$measure_file'\n";
  print FH_aging ".hdl nbti_l_analog.va\n";
  print FH_aging ".hdl chc_l_analog.va\n";
  close FH_aging or die "can't close $aging_file: $!";
  print "\n\n***************Running Circuit Simulation under Measurement Conditions ***************\n";
  system("hspice -i $input_file -o output/out_measure");
```

```
# Updating the Vth values in the spice file
print "\n\n***************Updating Vth values ***************\n";
open (FH_lis, "<output/out_measure.lis") or die "can't open output/out_measure.lis: $!";
open (FH_delvth, ">$delvth_file") or die "can't open $delvth_file: $!";
print FH_delvth "*This file is generated by the script aging_analysis.pl\n\n";
@delvth_val = "NULL";
while(my $line = readline(*FH_lis)){
  if($line =~ /.pos/){
    for($j=0;$j<$num;$j++){
      $search_string = "xs"."$transistor_list[$j]".".pos";
      if($line =~ /$search_string/){
        $line = readline(*FH_lis);
        @line_split = split(' ', $line);
        @line_split[1] =~ s/m/E-3/;
        @line_split[1] =~ s/u/E-6/;
        @line_split[1] =~ s/n/E-9/;
        @line_split[1] =~ s/p/E-12/;
        @line_split[1] =~ s/f/E-15/;
        @line_split[1] =~ s/a/E-18/;
        if(@aging_mechanism[$j] =~ /pnbti/){
          print FH_delvth ".param delvth$transistor_list[$j]=-@line_split[1]\n";
```

```
        }
        elsif(@aging_mechanism[$j] =~ /nchc/) {
          print FH_delvth ".param delvth$transistor_list[$j]=@line_split[1]\n";
        }
        push(@delvth_val,@line_split[1]);
      }
    }
  }
  shift(@delvth_val);
  close FH_lis or die "can't close output/out_measure.lis: $!";
  close FH_delvth or die "can't close $delvth_file: $!";
  # Measuring the offset degradation using the degraded Vth and "stress time = 0".
  # Measuring the offset along with the deltaVth measurement (stress time != 0)
  # causes an extra Vth to be added to the transistor and thus incorrect offset
  # data. Thus we separate the measurements.
  print FH_degrad "$time\t\t\t\t@delvth_val\n";
  $time+=$stress_interval;

}
#close FH_offset or die "can't close $offset_file: $!";
#close FH_result or die "can't close $result_file: $!";
```

```
close FH_degrad or die "can't close $degrad_file: $!";

$end = time();

$endtime = localtime($end);

print "\n\nEnd Time is $endtime\n\n";

$sim_time = $end - $start;

print "\n\nTotal Simulation time is $sim_time sec\n\n";
```