A CMOS Analog Front-End IC for Gas Sensors

by

Hyun Tae Kim

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Graduate Supervisory Committee:

Bertan Bakkaloglu
Bert Vermeire
Andreas Spanias
Trevor Thornton

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ABSTRACT

This thesis presents a gas sensor readout IC for amperometric and conductometric electrochemical sensors. The Analog Front-End (AFE) readout circuit enables tracking long term exposure to hazardous gas fumes in diesel and gasoline equipments, which may be correlated to diseases. Thus, the detection and discrimination of gases using microelectronic gas sensor system is required. This thesis describes the research, development, implementation and test of a small and portable based prototype platform for chemical gas sensors to enable a low-power and low noise gas detection system. The AFE reads out the outputs of eight conductometric sensor array and eight amperometric sensor arrays. The IC consists of a low noise potentiostat, and associated 9bit current-steering DAC for sensor stimulus, followed by the first order nested chopped ΣΔ ADC. The conductometric sensor uses a current driven approach for extracting conductance of the sensor depending on gas concentration. The amperometric sensor uses a potentiostat to apply constant voltage to the sensors and an I/V converter to measure current out of the sensor. The core area for the AFE is 2.65x0.95 mm^2. The proposed system achieves 91 dB SNR at 1.32 mW quiescent power consumption per channel. With digital offset storage and nested chopping, the readout chain achieves 500 μV input referred offset.

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CHAPTER 1

INTRODUCTION

Diesel and gasoline engines produce combustion gases and exhaust fumes, which contain a complex mixture of over one hundred types of gases and fine particles. The widespread and growing use of diesel and gasoline powered equipment has raised concern due to several links associated with human exposure to the diesel exhaust and lung diseases [1], [2]. High accuracy and sensitivity measurement and analysis of exposure are critical in correlating diseases to certain chemicals. The detection and discrimination of gases using a microelectronic gas sensor system is required in various industry and domestic applications such as automobiles, safety, indoor air quality, and medicine and food industries. As such, since the beginning of the twentieth century many biologists, chemists and electrochemists have been trying to characterize the electrical activity that results in chemical reactions in the different types of bio-chemical sensor systems that have excitable membranes or layers. The reason that this is important is because it helps biologists, scientists and engineers understand how the bio gas sensors work with harmful chemical particles, how the use of artificial engines create more harmful particles, and how the gas-controller or agent controls can remove exhaust gases. Furthermore, it helps us to diagnose and treat the respiratory nervous system of not only children exposed to exhaust from gasoline or diesel buses and cars but also workers in the manufacturing environment [1], [2]. In particular, chemical/biological sensors agents have attracted attention from both academia and industry because of their application,

efficiency and performance. Several types of chemical sensors have been introduced in the past that can sense fatal chemical/biological agents even in harsh environments.

One of the powerful approaches to the characterization of respiratory ailments is analysis of electrical data from gas sensors. Depending on the research goals, scientists, medical doctors, or engineers who wish to protect human health may decide to perform the analysis of chemical effects of humans and living things due to a hazardous environment by using a diesel and gasoline power system [2]. The electrical data captured from gas exhaust provides the medical doctors with the ability to study respiratory diseases, determine how the gases affect the human body, and evaluate responses to external stimuli gases. To provide the information for medical doctors or clinical instructors, use of specific gases and chemical sensors simplify the collection and analysis of data. A typical gas sample is composed of nitrogen dioxide (NO_2), carbon dioxide (CO_2), and hydrogen sulfide (HS) which are found in hazardous environments such as automobile engines and manufacturing environments containing handing and washing chemicals. Without the rest of the other gases, like oxygen, hydrogen, and nitrogen, present it is possible to stimulate the exhaust gas sensor detection system electrically or chemically and determine how it reacts with their equivalent electrical model. This is an important tool in the creation of electrical models of gases. One common application of the system of extracted gases is to gather information about the characteristics of reduction and oxidation channels. The collection of gas characteristics from the gas detection system provides the

ability to determine how a gas sensor behaves and which sensor reactions are more sensitive when exposed to certain dangerous gases.

The objective of this research is to provide improvements in the sensors and microelectronics used for performing exhausted gas detection in automobiles or manufacturing machines. This thesis describes the research, development, implementation and testing of a small, portable prototype platform for chemical gas sensors to enable a low-power and low-noise gas detection system. The following requirements for this li-ion battery operated chemical sensor system must be satisfied: weight, size, lifetime, and performance. Before delineating the specification for the low-power, low-noise and mobile chemical microelectronics with both conductometric sensor (single wall carbon nanotube sensor) and amperometric sensor, different types of sensors were studied. An analysis and comparison of conductometric, amperometric and other chemical sensors such as capacitive or huge resistance sensors was also performed and is described in this thesis.

Electrically gathering chemical sensor data is a form of measurement, and all measurement systems contain imperfections. By minimizing these imperfections, the quality of the sensor output results can be maximized. The electrical information measured from the gas sensor systems consists mainly of DC or low-frequency signals. The amplifiers and integrators used in the systems are generally CMOS based. It is well-known that CMOS circuits are an enormous producer of flicker noise (*1/f*), a noise process that produces increasing noise as the frequency is reduced. To reduce this noise problem, design engineers use

transistors with large width and length or employed filtering. Although lager transistors reduce *1/f* noise, they also take up a huge space which limits fabrication cost and the number of sensor interface channels that can be used simultaneously. Applying filtering can cause a loss of sensor measurement data in addition to taking up extra space in fabrication. Instead of conventional approaches, the approach proposed in this thesis is to use the well-known nested chopper modulation technique to reduce the effects of low-frequency noise, such as dc offsets, flicker noise and residue offset, generated by the input stages of the CMOS amplifiers, switched capacitor switches and chopper switches. This approach provides a significant reduction in the required noise and offsets. The smaller core size and footprint reduces die area; as a result, more channels can be used in the electrochemical systems.

The novel contribution of this thesis includes demonstration of the nested chopper stabilized technique, shows suppression of flicker *(1/f)* noise as well as DC offset and noise of integrator, and applies the chopper stabilized technique to conventional switched capacitor sigma delta ($\Sigma\Delta$) analog to digital converter (ADC).

In the next chapter, background information is provided on the conductometric sensor based on single wall nanotubes (SWNT) and the amperometric sensor based on planar microelectrodes. This thesis proposes a low-residue offset, low-power and mobile-based CMOS interface circuitry for conductometric and amperometric gas-chemical sensors. A desirable platform system should be battery operated and as small as a wearable badge. To satisfy

the size and power consumption requirements of the system, an integrated gas readout IC, data acquisition, and data signal processing module was developed.

This thesis is organized as follows and focuses on the low-noise, low-offset and low- voltage analog front-end interface circuitry used in mobile based gas detection applications, which require small physical area and low noise. Chapter 2 presents the background information for the basic electrochemical sensors and previous works. Also, it describes the flicker (1/*f*) noise and dc offset noise as well as their reduction techniques. Chapter 3 introduces sigma delta ADC theory and operation as well as decimation theory and operation. Chapter 4 discusses architecture of CMOS interface circuitry, the simulation of each circuit block and presents simulation results. In chapter 5, transistor level implementation and post-layout simulation results will be shown. Chapter 6 discusses the chip measurement results and tests the designed portable platform. The designed interface will be connected to the electrochemical sensor arrays, and the performance of the full system will be described. Chapter 7 consists of the conclusions and accomplishments.

CHAPTER 2

REVIEW BIOSENSORS AND PREVIOUS WORKS

2.1 SENSORS, BIOSENSORS, TRANSDUCERS AND ACTUATORS

According to etymology, the word transducer is derived from the Latin verb “transducere-traducere” which means “to transfer-to translate” [3]. Therefore, a device that transfers or translates energy from one kind of system to another form is termed a transducer. In the instrumentation environment, a transducer is used to indicate a device whose input and output belonging to the same signal domain can be identified as a transistor.

A sensor may be defined as a transducer that converts a signal of some specific form into an electrical signal like current and voltage. An actuator, on the other hand, can be defined as a transducer that converts an electrical signal or energy into a signal of another form, usually a mechanical signal of another form or a mechanical signal for motors and switches [3].

Examples of sensors as transducer are pressure sensors, pH sensors and phototransistors. Examples of actuators are solenoids, piezoelectric devices and laser diodes. An electrode at which hydrogen or oxygen is generated by applying a potential is an example of a chemical actuator. A display is a special kind of transducer that converts an electrical signal into a display like LED or LCD to readout the electrical signal.

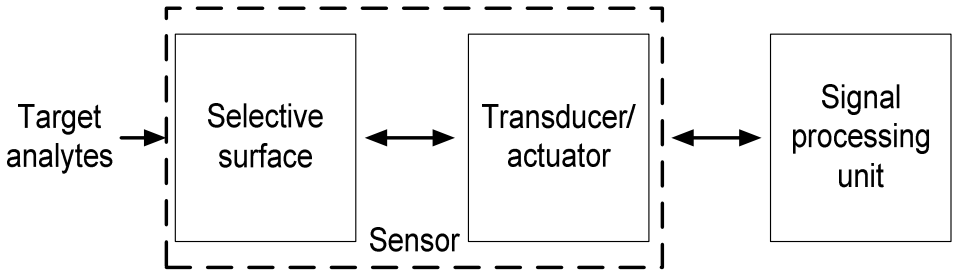


Figure 2.1 General features of a chemical sensor.

2.2 FEATURES OF CHEMICAL SENSOR

Three general features can be identified that make up a chemical sensor [3], [6]. These include a selective surface, a transducer, and a processor as depicted in Fig. 2.1 below. The selective surface allows for a specific interaction with the garget analyte, where analyte refers to be compound whose composition or presence is being sought. The surface can be modified by the addition of ligands or catalysts that provide specific recognition features. The transducer tracks the association of the surface with the analyte. For example, the transducer may be a polymerie material that changes its electrical resistance with the incorporation of the analyte. Alternatively, the transducer may change color or modify the transmittance of light passing through it. Some signal detection, processing, and amplification are carried out to generate a practical output signal used by the process controller. The final signal coming from the sensor is electronic so that it can be interfaced to standard controllers or data loggers.

The main limitations of many chemical sensors are associated with the selectivity of the response to the target analyte compared with the response seen for potential background or contaminating compounds [6]. In a constant

background there is little need for selectivity, but in a more typical sensing situation the background concentration changes in unknown ways due to the presence of similar chemical components or “active” species as well as temperature and pressure fluctuations. A typical interference in many gases sensing situation is the background moisture or humidity level that is constantly undergoing variations.

The main types of chemical sensors developed to date rely on electrical or optical transduction technologies [6]. To a lesser degree, physical transduction processes such as displacement tracking, due to pressure or temperature mediated effects, may also be used, but it is often the case that the operation of such devices rely on electrical or optical signal modulation. Within the electrical transducers, it is convenient to divide them into amperometric, potentiometric or conductimetric sensors depending on whether the measured signal is the current, voltage or conductance, respectively. Optical sensors include those that monitor the light absorption, refractive index, polarization, or fluorescence of a transducer, perhaps at many different wavelengths and using continuous or variable light input schemes.

The main work in the development of sensors is on designing, finding or fabricating new materials. The following discussion will focus mainly on the chemical sensor technologies. Broadly speaking, the chemical sensors can be categorized as either resistive or capacitive. As the name suggests, a resistive sensor changes resistance when exposed to a chemical of interest, whereas a capacitive sensor changes capacitance when exposed to a chemical of interest.

Table 2.1. Electrochemical Sensor Transduction Mechanisms [6]

Transducer	Mechanism	Signal	Example Sensor
Amperometric	Electron charge transfer reaction (Faraday's law)	Current: due to production or consumption of electroactive species	Oxygen, some hydrocarbons, hydrogen peroxide, fuel cells
Potentiometric	Multiphase equilibrium (Nernst Equation)	Potential: due to distribution of ionic species	Glass pH electrode, ion selective electrode
Conductomeric	Variation of resistance with composition	Conductance or resistance: due to change in resistive elements	Metal-oxide-semiconductor gas and humidity sensor, the oxide gas sensors

Electrochemical sensors include the familiar wired or printed electrodes as well as metal oxide semiconducting devices, devices, fuel cells, ion-selective field transistors (ISFETs), interdigitating electrodes, high-temperature solid-electrolyte systems, and chemi-resistors [3], [6]. A current trend in many chemical sensors is toward miniaturization and micro fabrication that can impart novel properties to sensors, thereby affecting their selectivity, sensitivity, and stability. This thesis does not explore all the latest research variations and innovations but focuses on devices that are commercial or near commercial. Recent research results can be found in specialized journals devoted to chemical sensing and analytical chemistry.

2.2.1 Electrochemical sensors:

Table 2.1 lists the three main types of electrochemical sensors. They are explored in separate sections below, with specific examples that illustrate the

important features [6]. Not all sensors can be exactly categorized in this way since they represent only limiting behaviors. Nevertheless, such distinctions are routinely used and widely adopted in the chemical sensor literature.

2.2.1.1 *Amperometric sensing*

An amperometric chemical sensor is composed, at a minimum, of two metal electrodes maintained at a constant potential (voltage) difference. The current flowing in a closed circuit (which is established and monitored by suitable electronics) through the two electrodes is measured and indicates the presence of electroactive species. The relationship between the moles, N, of electroactive species reacted (either oxidized or reduced) and the charge passed through the sensor, Q, is known as Faradays's law

$$N = \frac{Q}{nF} \tag{2.1}$$

where n is the number of electrons transferred per mole and F is the Faraday constant (F=96487 *C/mol*). By monitoring the charge over time, which is the current, the amount of electroactive compounds can be deduced. To operate as a true sensor, however, some selectivity is required, and this can be achieved by the choice of a suitable electrical potential, by the introduction of a catalytic reaction step, and/or through perm selective membranes. For examples, a common method for the detection of dissolved oxygen in liquids is through the use of a so-called polarographic electrode. In this chemical sensor, the reduction of oxygen is followed at constant potential by monitoring the current passing between a working platinum (Pt) electrode and a silver/silver chloride (Ag/Cl) reference

electrode. At steady state, the current is proportional to the dissolved oxygen concentration. This is often reported as an equivalent particle pressure corresponding to the oxygen concentration and is a gas phase that would be in equilibrium with the actual liquid-phase concentration.

2.2.1.2 *Potentiometric sensing*

A potentiometric chemical sensor is composed of many of the same parts as an amperometric sensor, except that voltage is measured under conditions of a small, often negligible current. The most important feature in a potentiometric measurement is that equilibrium conditions are established between electroactive species in solution and at the electrode. This is in contrast to the diffusion-limited condition just discussed for amperometric measurements and leads to relations between voltage and concentration that are logarithmic rather than linear.

2.2.1.3 *Conductometric sensing*

The electrical resistance change that accompanies the interaction of a target analyte with a conductive layer (typically a polymer or ceramic) held between two electrodes can also be used to construct a sensor. Such devices are generally known as conductometric or resistive sensors. These sensors are one of the simplest types of sensor to construct and have been widely used in gas sensing applications. At the same time, however, they are among the least understood in terms of their selectivity properties. For this reason, many of the applications have been discovered by empirical modifications to various selective layers and to electrode physical design. The result is that conductometric sensors often require detailed calibration with a variety of potential interferents in order to carefully

define the selectivity and be commercially useful. Nevertheless, these sensors are generally inexpensive and the perceived disadvantages are easily outweighed.

The electrodes in a conductimeric sensing circuit contact the resistive element in such a way that direct current or alternating current measurements can be taken with the resistive layer exposed to the sensing fluid. Absorption of the analyte occurs both at the surface and within the bulk of the material, which leads to changes in the electrical resistance. Such measurements can usually be done very accurately using two particular types of layers: metal oxide semiconductors and conducting polymers.

2.3 CONDUCTOMETIRIC (RESISTIVE) CHEMICAL SESNORS

Resistive chemical sensors form another generally used type of sensors [4], [5]. The basic mechanism of resistive sensors may vary from one sensor to another, but the first principle behind the mechanism is either chemical reaction or polarization. In Ion-Sensitive FETs (ISFET) sensors like a transistor, a CMOS-like structure is used as a sensor [71]. The difference between the CMOS and ISFET is that the gate of ISFET is coated with a polarized material that reacts with or attracts the interesting chemicals in a solution. When the chemical exists on the gate of the structure, the amount of inversion in the channel of the device changes due to the change in effective gate potential. In fact, this results in the change of resistance after chemical reaction. In non-transistor-like resistive sensors, the chemical of interest directly forms a bond with the sensor, which

triggers a transfer of excess charge carrier into the sensor. Such a transfer results in the change of resistance.

The sensitivity of resistive sensors may vary a lot from sensor to sensor, but the sensitivity can be partical per trillion (ppt) [2] when they are heated or are activated. Because the statistical information on many sensors is not available in most papers, an accurate performance characterization of sensors is not easy to conduct. The response time is usually longer than that of the capacitive sensors because the sensor has to react with the chemical. In most cases, the reaction time is around 1 millisecond to 10 minutes, but this can also be reduced through heating and chemical coating.

A drawback of general resistive sensors is that their base resistance is hard to control. For example, in carbon nanowire sensor case, the base resistance can change from 1 MΩ to 1 GΩ [4], [5]. Given the necessary signal to activate the sensor, and the fact that base resistance change, ΔR, is proportional to the base resistance R, the dynamic range of the sensor interface would have to be large wide. A fair comparison among the sensor is very difficult to conduct because of limited information provided by the published results. In the following section, conductometric sensor based carbon nanotube sensors is studied specifically in the context of building a low- noise, low-offset and low-power chemical sensor system.

Resistive chemical sensors are used because of their advantages: good sensitivity to relevant gases, low production costs, and small size. Thus, it is convenient to design miniature gas detection system with these sensors [6]. The

mechanism of resistive sensors may vary from one sensor to another, but the main principle is a change in resistance according to a chemical reaction or polarization. In fact, they react to the presence of the gases by varying the conductivity; therefore, they can be considered resistive sensors. To interface with such sensors, which can have resistance values varying from tens of kΩ to tens of GΩ, different coating solutions have been developed. In general, the sensitivity of resistive sensors may vary significantly from sensor to sensor but the sensitivity can be high with prolonged exposure to hazardous gases.

One of the disadvantages in resistive sensors is the response time. Generally, the response time of the resistive sensor is longer than that of the capacitive sensors. The other drawback of resistive sensors is that the sensor's base resistance is hard to control. Since the dynamic range of the sensor interface is large power dissipation is required. Furthermore, general resistive sensor applications need to reduce offset and noise at low frequency because the sensor signal is very low frequency.

2.3.1 Carbon Nanotube (CNT) Chemical Sensor

The discovery of carbon nanotubes (CNTs) has generated and kept interest in developing CNT-based sensors for many applications [7]. The CNTs ability to sense chemicals was first demonstrated in [10]. Much research and results were published on CNT sensors based on a bare CNT, a CNT transistor, and a film of CNTs [4]. The application of CNTs in next-generation sensors has the potential of revolutionizing the sensor industry due to their inherent properties such as small

size, high strength and high electrical and thermal conductivity. The CNTs were shown to be one of strong candidates for the next-generation chemical sensor, first introduced in the pioneering work by Kong et al [10].

As mentioned before, each type of CNT sensors has its own advantages, such as easier fabrication steps, high selectivity, high sensitivity, and high yield. Single-wall carbon nanotube (SWNT) sensors are an especially popular CNT sensor. This gas detective sensor has chosen a SWNT instead of multi-wall carbon nanotube because of simple structure to sense the gas chemicals.

A bare carbon nanotube can sense NH_3 and NO_2 as shown in Fig. 2.2 and 2.3. If the gate voltage is fixed V_{gs} (4V) as shown in Fig. 2.2, the CNTs

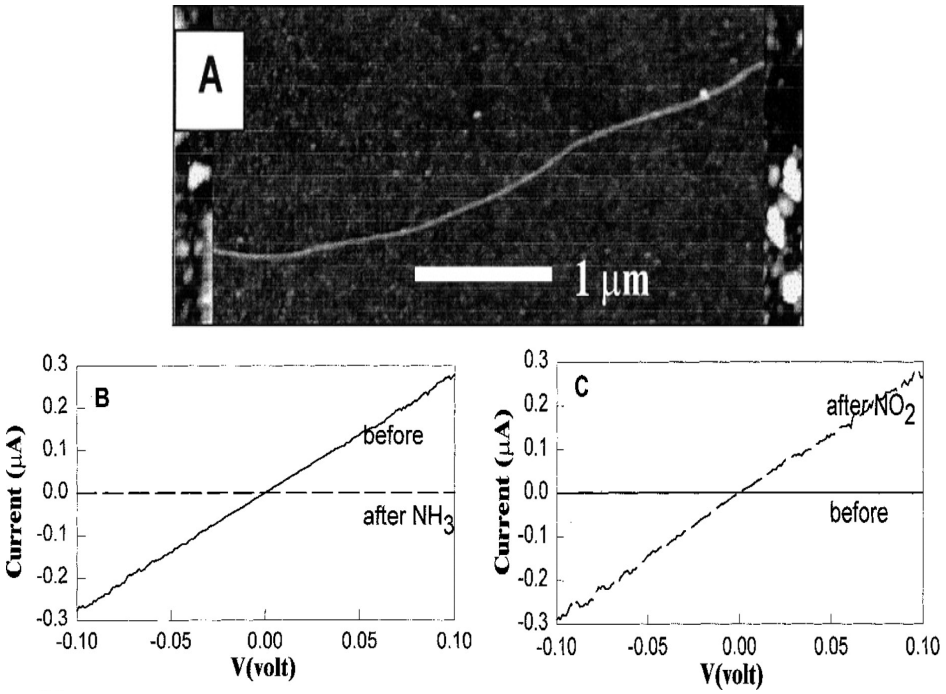


Figure 2.2 Changes of electrical characteristics of a SWNT in exposed NO_2 and NH_2 (a) Nanotube diameter is ~1.8 nm. (b) I-V curve before and after exposure to NH_3. (c) I-V before and after NO_2 exposure. J. Kong et al [10].

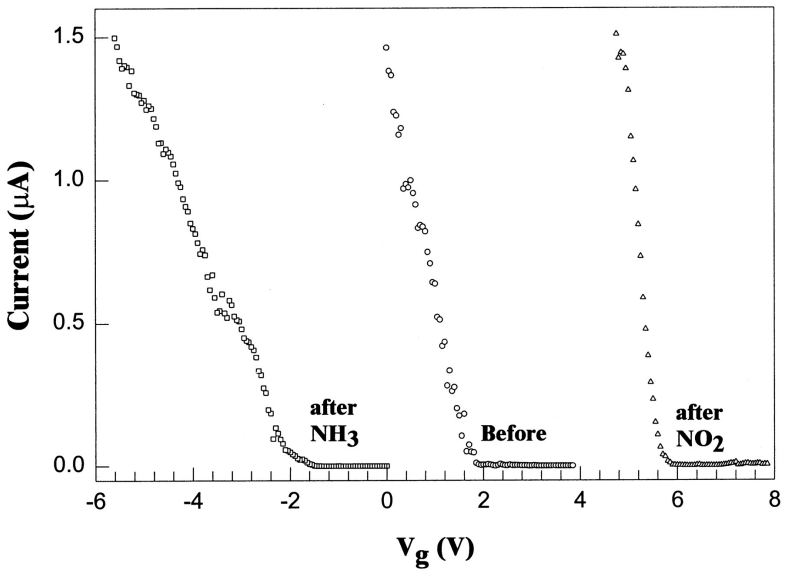


Figure 2.3 I-V_{gs} curve for NO Current NO_2 (circles) and NH_3 (squares) exposures.

response to the exposure of chemicals could effectively be interpreted as the resistance change of CNTs. Therefore, by reading out the resistance value of CNTs at a fixed gate bias, the concentration of specific gas could be inferred. Fig. 2.3 shows a CNT device is a P-type with negative threshold voltage, and the shift of the voltage curve is the shift in the threshold voltage of the device. However, CNTs take more than 500 seconds to fully react with the chemicals in air at that concentration. When the concentration of gas increases, the response time decreases. The response time can actually be decreased by structure on surface of the CNT. The coating increases the bonding sites for more chemical atoms, which in turn decreases the response time from 5 second to 10 seconds [4].

The SWNTs (single wall cabonanotubes-COOH 80 ~ 90% purity) were obtained from Carbon Solution, Inc. (Riverside, CA). Works introduced in the

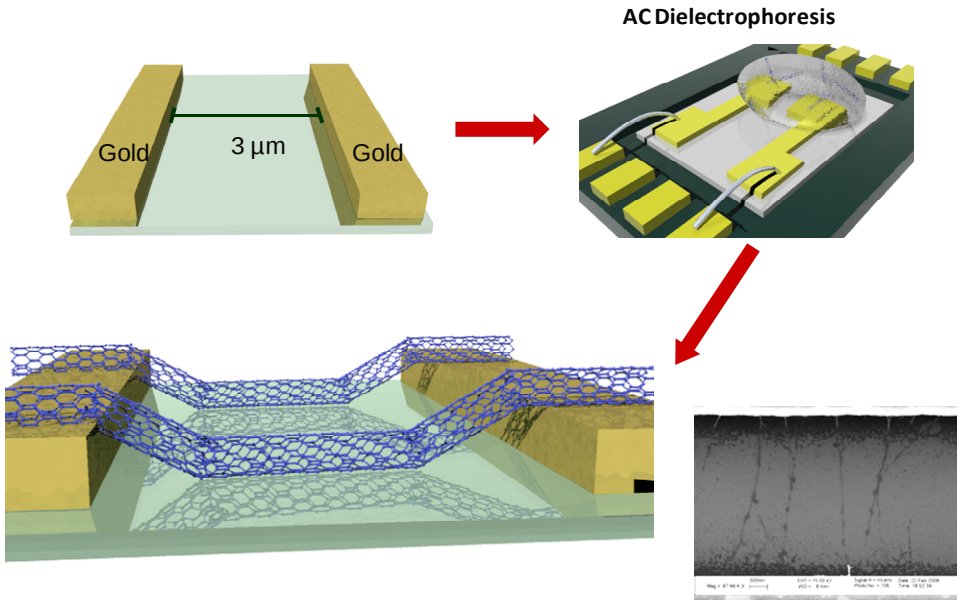


Figure 2.4 SWNT fabrication process

following fabrication for this sensor are built by biochemical lab at University of California, Riverside. The fabrication process is shown in Fig. 2.4.

The nanotubes (10 $\mu g/ml$) were ultrasonically dispersed in N, N-dimethylformamide (DMF) and the suspension was centrifuged at 31,000 G's for 90 min to remove the non-soluble fraction and aggregates. Preparation of the SWNT solution is depicted in Fig. 2.4. The SiO_2 film with the thickness of 300 nm was deposited on highly doped p-type Si substrates using the thermal Chemical Vapor Decomposition (CVD) deposition technique. The Cr/Au (20/180 *nm*) electrodes were subsequently e-beam evaporated on SiO2/Si substrates. The gap between two electrodes and the length were 3 μm and 200 μm, respectively. For randomly oriented SWNTs, 0.1 μl of SWNTs suspended in DMF was placed on top of electrodes using micro syringe or inker.

Sensor resistance was controlled by drop size and SWNTs solution concentration. For aligned SWNTs, 0.2 μl of SWNTs suspended solution was placed on top of gold electrodes applying 0.36 VRMS at 4 MHz frequency. Sensor resistance was adjusted by deposition time. Resistance increases with the decrease in deposition time. To reduce the contact resistance between electrodes and SWNTs and remove solution residues, the assembled sensors were annealed at 300 °C for 1 hr under the reducing environment of 5% H_2 in N_2.

2.4 AMPEROMETRIC SENSOR

The following sections describe aspects of electrochemical and electro-analytical chemistry. Amperometry is a special form of voltammetery, because the potential is kept constant and the current is the sensor output signal which is recorded as a function of time. In other words, voltammetery is the measurement of the current which flows at an electrode as a function of the potential applied to the electrode. As a result of a voltammetric experiment, the current-potential curve is recorded for chemical reactions like oxidation and reduction (redox).

2.4.1 Faradaic Current

Under equilibrium, and in the absence of an externally applied voltage, a single polarizable electrode resting in solution will develop a potential based on the ratio of the solution's chemical species [8]. When a voltage sufficiently larger than this equilibrium potential (an over potential) is applied to the electrode, the

system is forced out of equilibrium and results in a reduction/oxidation (redox) reaction of the form:

$$O + ne^{-} \leftrightarrow R \tag{2.2}$$

where O is the oxidized form of the species, n is the number of electrons per molecule oxidized or reduced, e^{-} is an electron, and R is the reduced form of the species. For every reduction or oxidation, electrons are transferred from solution to electrode or vice versa. This results in a faradaic current at the electrode surface. Among other parameters, the faradaic current is a function of the concentration of the oxidized species and the electrode area. Thus, the measured faradaic current corresponds to a specific ion concentration.

2.4.2 Amperometric Sensor

Single electrode systems are operationally impractical because of there are no electrical signal paths. A typical sensor configuration is the three-electrode amperometric cell. The three electrodes are the count electrode (CE), the reference electrode (RE), and the working electrode (WE), as shown in Fig. 2.5.

On all boundaries between electrodes and solution there exists double layer capacitor, $C_{dl.}$ This capacitor will be discussed later. The faradaic reaction of interest occurs at the WE. The RE, which ideally draws zero current, is a non-polarizable electrode that tracks the solution potential. Consequently, the potential between the electrode and solution which induces the faradaic reaction is given by:

$$V_{WE} - V_{RE} \cong V_{CELL} \tag{2.3}$$

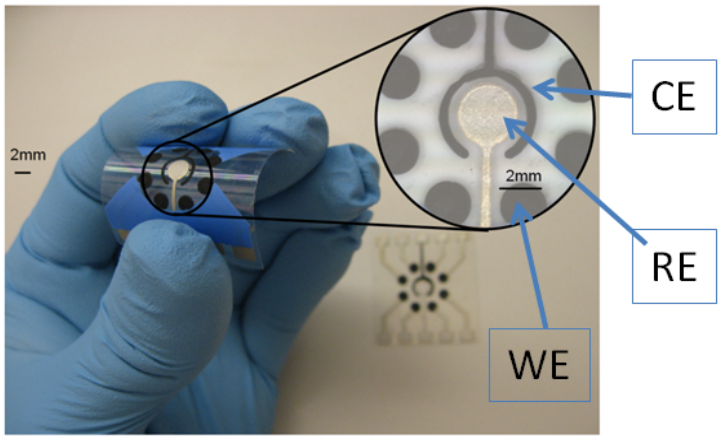
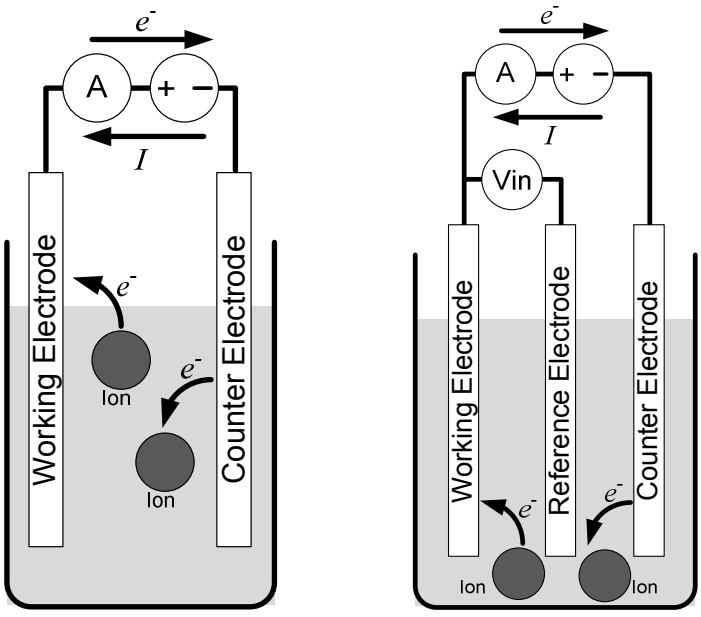


Figure 2.5 Amperometric Sensor Symble by using Flexible-Wearable Screen printed Electrode (SPE).

The amperometric cell's potential is defined by (2.3). The CE enables the potential of the solution to be set via secondary redox reactions and sources the current necessary for the faradic reaction. To keep constant voltage between WE and RE, a potentiostat is used. The potentiostat can be defined as a direct analytical application of the Nernst equation [71] through measurement of the potential of non-polarized electrodes under conditions of zero current. The measurement is thought to be performed in thermodynamic equilibrium. Since only the potential of the half-reaction is of interest, a reference electrode is necessary. Reference electrodes are therefore of special importance for electrochemical experiments. Without a stable reference electrode, no reliable electrochemical sensor can be made. Reference electrodes are also based on the principles of the Nernst equation. The normal hydrogen electrode (NHE), the calomel and the Ag/AgCl electrode are detailed in [71].

Research articles on CMOS interfaces to amperometric gas sensors have also been published in the past. Two different electrode configurations are shown in Fig. 2.6 (a) the two-electrode system consists of a reference electrode (RE) and a working electrode (WE). A potential is applied to this electrochemical cell and the current is recorded as a function of this potential. However, the drawback of this two electrode system is that the electrode will polarize and over-potential will occur while the reference electrode carries current. Thus, the potential at the WE is unknown. This polarization can be avoided by the use of a very large reference electrode and a small working electrode. In this way, the current density will be low enough to prevent polarization of the electrode. The other problem in two electrode systems is the material consumption in the reference electrode. A good



(a) (b)

Figure 2.6 (a) Two electrodes potentiostat (b) three electrodes potentiostat.

example of this problem is an oxygen sensor consisting of an Au working electrode and an Ag/AgCl reference electrode. To reduce the oxygen at the WE, oxidation of Ag to AgCl will take place at the RE. If all Ag in the RE is consumed, the RE will not function properly and the potential at the WE will be unknown. To avoid this problem, large electrodes are used for the RE and small working electrode. A better approach is the use of a three electrode system and a potentiostat, instead of a two electrode system [3]. Besides the WE and RE, the counter electrode (CE) is introduced in Fig. 2.6 (b). The RE in the two electrode system is split into two electrodes for the three electrode system: the true RE for controlling the potential and the CE for current injection in the electrolyte. In fact, in three electrode systems, the potentiostat controls the current at the CE as a function of the potential. Based on this, the work by Zhang achieves the detection current range of 10 pA to 10 μA by controlling the gain in the amplifier stage with the amperometric sensor [12]. It consists of a potentiostat biasing structure and a single channel switched capacitor current readout circuit.

The amperometric sensor is fabricated using the following procedure. The sensor used in this thesis design was made by biochemical lab at University of San Diego, CA. A semi-automatic screen printer (Model TF 100; MPM, Franklin, MA) was used for printing the thick film carbon (working and counter) and Ag/AgCl (pseudo reference) electrodes. The carbon [G-449(I), Ercon, Wareham, MA] and silver ink [R-414(DPM-68) 1.25 Ag/AgCl ink, Ercon] were printed through a patterned stencil on 10 cm × 10 cm ceramic plates containing 30 strips (3.3 cm × 1.0 cm each). Both printed Ag/AgCl and carbon thick film electrodes

were cured at 120^{o}C for 20 minutes. An insulating ink (E6165-116, Blue Insulator, Ercon) was subsequently printed on a portion of the plate, leaving exposed sections of the electrode and silver-contact areas on both ends, including a 6 mm x 2 mm carbon working electrode. The insulating layer was cured at 120°C for 30 minutes.

2.5 PLANAR MICROELECTRODES

Thomas and others introduced the concept of planar microelectrodes in 1972 [13]. A planar microelectrode is a thin-film deposit of gold or platinum on a glass substrate. The planar microelectrode is enclosed in a Petri dish or a glass chamber of some sort. The container is filled with microelectrodes which are implemented in arrays. Planar microelectrodes are non-invasive, can accommodate large numbers of cells, and are simple to implement.

A metal electrode is not generally inert to the electrolyte medium into which it is immersed [17]. There is generally an electrochemical reaction between the electrode and electrolyte [8], [9]. When an unbiased metal item is dipped into an electrolyte, several chemical reactions start between the metal and the liquid. One of these reactions is oxidation, where the metal with donors gives out an electron and an acceptor, which are metal ions. This reaction is shown in (2.4).

$$A \leftrightarrow A^{+} + e^{-} \tag{2.4}$$

In equation (2.4), donor A gives out an acceptor, A^{+} and an electron, e^{-}. An electrolyte and the sample is then placed upon the electrode, generally planar at the interface. Donated electrons will accumulate at the edge of the metal, because

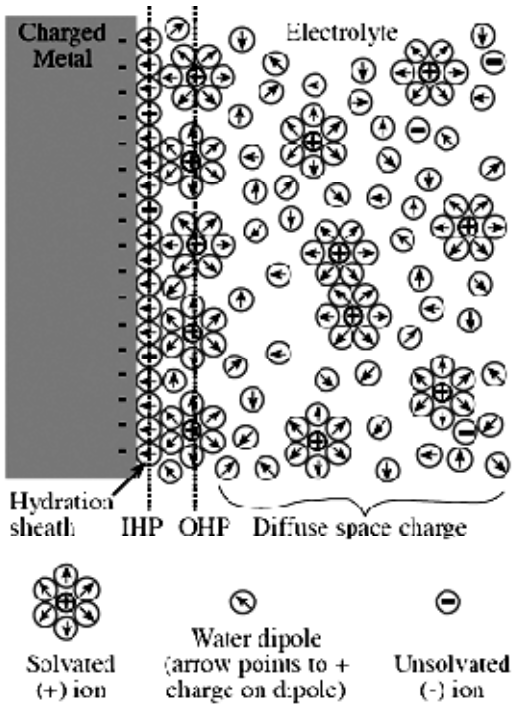


Figure 2.7 Structure of double Layer in boundary.

electrons repel each other and are attracted to the metal surface. The ions in the electrolyte will align themselves by forming a double layer called as inner Helmholtz plane (IHP) and outer Helmholtz plane (OHP) as seen in Fig. 2.7.

The space charge layer formed in this equilibrium is usually modeled as a capacitance, known as the “interfacial capacitance.” There is equal current flow in both directions which results in zero net current. If a DC voltage is applied across the interface, there will be a current flow across the plate [10], [11] so a resistive path needs to be added to the model. If the potential difference is relatively small, the current flow will be linearly related to the voltage. The equivalent resistance is called “charge transfer resistance (R_{ct}).” The solution resistance shown as R_s in

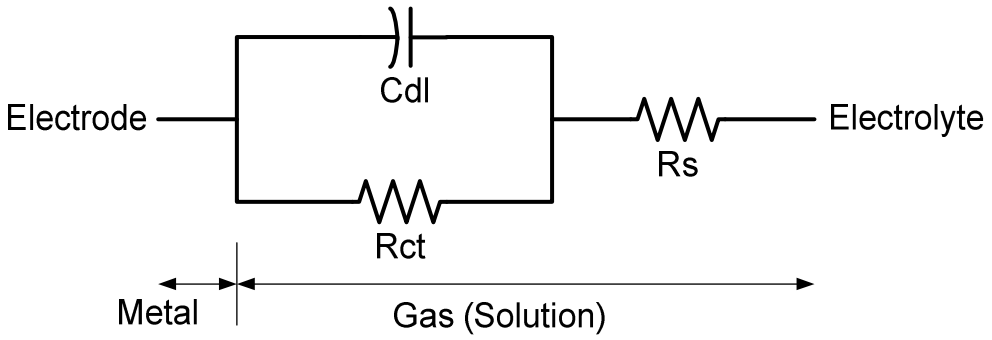


Figure 2.8 Equivalent electrical model of metal-electrode interface.

Fig. 2.8 is modeled for the current that flows outward from the electrode into the chemical solution.

In general, its value depends on the shape of the electrode and conductivity of the electrolyte. In fact, the equivalent circuit model for an amperometric sensor in the electrode-electrolyte interface is given in Fig. 2.8. Planar microelectrode arrays have been used extensively by many scientists for all kinds of current and voltage measurements.

2.6 LOW FREQUENCY NOISE SOURCES

The analog sensor signals usually have a bandwidth between DC and a few kilohertz. In the low frequency range problems that have little effect in high frequency circuits start to become important. In this thesis these noise sources will be identified and explained. Methods of low frequency noise reduction techniques will be presented and some implementation issues will be addressed.

2.6.1 Flicker Noise and Thermal Noise

Flicker noise is a low-frequency noise and is probably the most important and most misunderstood noise source in CMOS circuit design [31]. Flicker noise is known as pink noise or 1/*f* noise because its PSD is inversely proportional to frequency. Flicker noise originates in the amplifier and is a significant noise source for low-frequency applications. The most significant contributors of this type of noise are the input transistors because the noise generated by them is directly added to the signal and amplified by the following stages.

A simple method of reducing 1/*f* noise is to increase device geometry and add a special process. In CMOS process the input referred noise of the transistor is described using a well-known equation, as shown below [58]:

$$S_n(f) = 4kT\frac{\gamma}{g_m} + \frac{K_p}{WLC_{ox}f} \tag{2.5}$$

where *k* is Boltzmann's constant (1.38×10-23 J/K), *T* is absolute temperature (*K*), γ is a noise excess coefficient, g_m is transconductance of the transistor, K_p is a process dependent constant on the order of 10^{-25} V^2F, *WL* is the product of the transistor's width and length, and C_{ox} is oxide capacitance. From (2.5), the first term of the left side represents the thermal noise, and the second term is 1/*f* noise. Fig. 2.9 above shows the noise spectrum. The flicker noise corner frequency (f_c) is given by:

$$f_c = \frac{K}{WLC_{ox}f}\frac{g_m}{4kt\gamma} \tag{2.6}$$

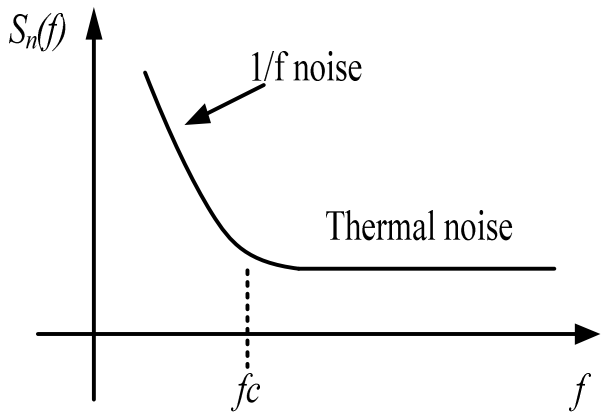


Figure 2.9 Noise spectrum of CMOS transistor.

This equation implies that f_c generally depends on device dimension and bias current. Nonetheless, since the dependence is relatively weak for a given L, the 1/*f* noise corner is relatively constant, falling in the vicinity of 100 kHz to 1 MHz for submicron transistors.

A challenging research question for analog circuit designers is how to reduce 1/*f* noise. There are several methods to minimize 1/*f* noise. One approach is to use large input device geometries. As seen in (2.6), 1/*f* noise is the inversely proportional to the area of the transistor. Using large device geometries reduces 1/*f* noise associated with these devices. However, this technique costs large parasitic capacitances and die area.

A second approach involves adding a special process step while manufacturing devices to produce a buried channel into the device. Any 1/*f* noise is due to trapping and de-trapping carriers (electrons and holes) on the channel surface when the channel is formed in operation condition [14]. Since the channel is built at the interface between silicon and the gate oxide, carriers flow at the

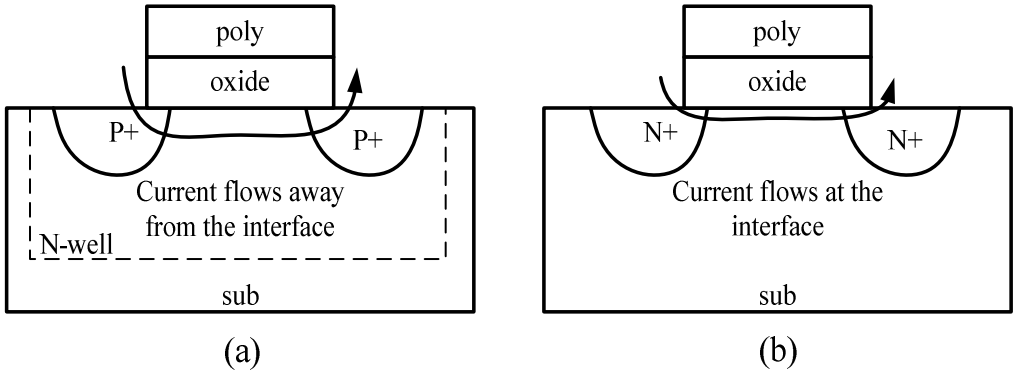


Figure 2.10 (a) p-channel MOS vs. (b) n-channel MOSFET.

interface and could be easily trapped and de-trapped. In the case of a buried channel device, the channel could be built deeply, as seen Fig. 2.10.

Therefore, the carrier could flow away from the interface and the flicker noise performance of the buried channel device is similar to a bipolar junction transistor (BJT) with very low flicker noise.

2.6.2 DC Offset

In general, the differential outputs of an amplifier should be zero when its differential inputs are also zero, but generally, there is an offset voltage between the outputs of the amplifier. This DC offset may be a result of the improper design of the circuit but is usually caused by mismatches in the circuit. The DC offset seen at the output of an amplifier will decrease the dynamic range of the circuit. This offset voltage can usually be compensated by introducing an offset at the input. This offset is referred to as the amplifier's input offset voltage. Fig. 2.11 shows this voltage.

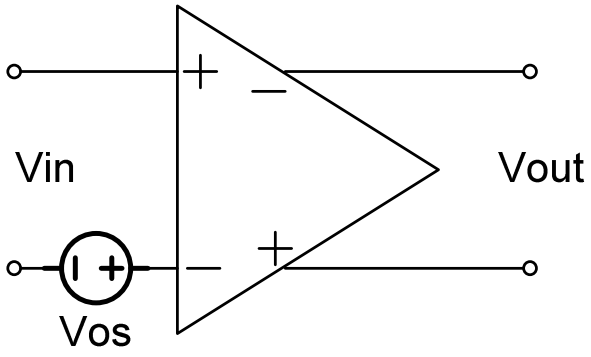


Figure 2.11 DC Offset.

2.6.3 Channel Charge Injection and Clock Feed through

Every time a MOS switch is turned off, as shown in Fig. 2.12, some fraction of the charge that is stored in its channel is injected into the line. These unwanted charge transfers affects system precision and linearity. This results in a DC offset at the amplifier's output and MOS switch, which is called residual offset. Here an important trade-off comes into effect. If the main amplifier's bandwidth is much larger than the chopper frequency, it will result in an increase in the gain as mentioned in previous chapters. However, this will also cause

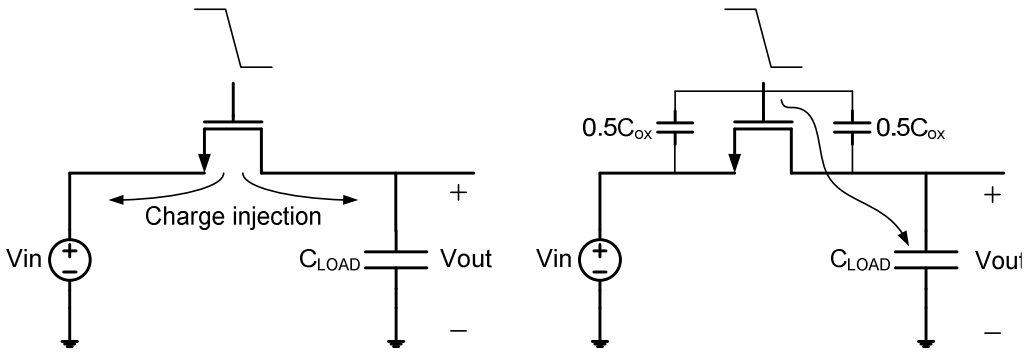


Figure 2.12 An MOS switch to show charge injection and clock feed through.

the residual offset voltage to increase because more spectral components of the spikes will be added to the signal and amplified. When choosing the amplifier's bandwidth this trade-off must be taken into consideration.

2.6.4 Other Noise Sources

There are some other noise sources that are specific to the materials and manufacturing processes chosen. In the case of metal electrodes, the resistive elements between metal-electrolyte interfaces create additional thermal noise which will degrade system quality. This noise, especially which created by the spreading resistance *(R_s)*, limits the size and the shape of the electrode, adding another constraint to the recording system design [15], [16]. Another noise source is the random baseline drift, which is reported to be very slow and therefore relevant. This drift is usually around 100mV at a frequency of less than a couple of hertz [18]. Designers usually remove this noise with a high-pass filter which has a low cutoff frequency. It is reported that this noise only applies to metal electrodes and does not appear on neuron-transistor based systems [15].

Another noise source that limits the system's performance is Electro-Magnetic Interference or (EMI) [15]. Any wire that passes a current can be a source of EMI. One of the problematic manifestations of EMI is the 60 Hz noise that is caused by electric lines. Many designers add a notch filter to attenuate this type of noise.

Crosstalk between adjacent lines that connect to measure the sensor signal can cause problems. If a large signal is passed through one of these wires, artifacts

may appear on the adjacent lines. This is often a problem when one of the lines connects to a test chip while the other carries a measuring sensor signal.

2.7 Noise Cancellation Techniques

DC Offset and 1/*f* noise in CMOS system are constraints on the obtainable accuracy and dynamic range of CMOS amplifiers. There are several ways to reduce offset and low frequency noise based on sampling or modulation. The autozero technique and correlated double sampling technique (CDS) are methods of reducing *1/f* noise and offset based on sampling. In the next section, the two methods and dummy switch are considered and their advantages and drawbacks are discussed.

2.7.1 Dummy Switch

One way to reduce this injected noise is to use half-sized dummy

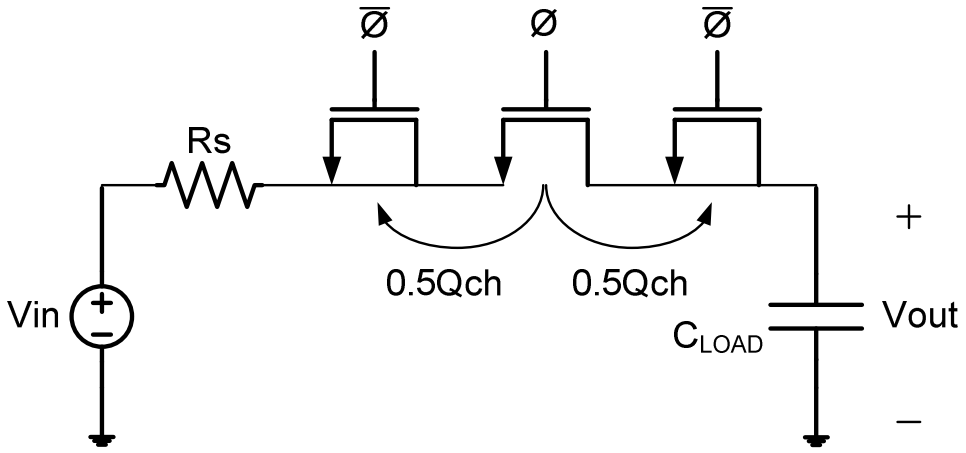


Figure 2.13 An MOS switch to show charge injection and clock feed through.

transistors as seen in Fig. 2.13 [34]. The built up charge on the switch will equally split between source and drain and be compensated by these dummy switches. However, this requires that dummy switching is the complement of the signal controlling MOS switch should also be slightly delayed. When MOS turns off, half of the channel charge is injected toward the dummy switch. However, it is difficult to fabricate exactly half of the channel of MOS switch for the dummy switch.

2.7.2 Auto-Zero Technique

The auto-zero technique reduces the offset and low frequency noise based on sampling methods [18]. This method has been extensively used in the past for offset reduction in comparators and amplifiers. Most of the current A/D

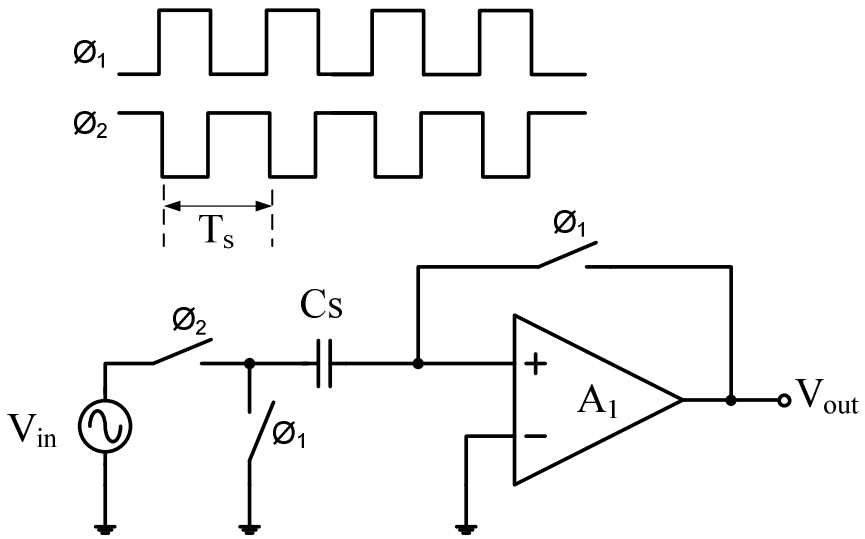


Figure 2.14 Auto-zero technique.

converters with offset cancellation make use of auto-zeroed comparators. Fig. 2.14 illustrates the principle of auto-zero amplifiers.

The auto-zero process requires at least two phases. In the first phase of the clock, the sampling phase, the offset and the flicker noise of the amplifier configured as a buffer is sampled on the capacitor Cs. The output $V_{out}(t)$ is actually the offset voltage V_{os} as long as the open loop gain of the amplifier A_{OL} is large:

$$V_{out}(t) = -\frac{1}{1-\frac{1}{A_{OL}}} V_{os} \approx -V_{os} \tag{2.7}$$

In the second phase of the clock, the amplification phase, the input signal $V_{in}(t)$ is sampled and amplified. The offset and 1/*f* noise is removed from the output by subtracting the value sampled on the capacitor from its actual output:

$$V_{out}(t) = A_{OL}\left(Vin(t) - \frac{V_{OS}}{A_{OL}}\right) \tag{2.8}$$

The equivalent input offset is reduced by a factor equal to the amplifier open loop gain. The reduction of 1/*f* noise is based on the high correlation between the 1/ *f* noise samples. The charge injected from the switch produces residual offset which is not cancelled by the auto-zero mechanism.

To show the auto-zero effect, consider a stationary random process *n(t)* which can be white noise or flicker noise generated by the amplifier A_1 from Fig. 2.14. For simplicity, the amplifier is assumed to have an infinite bandwidth, unity

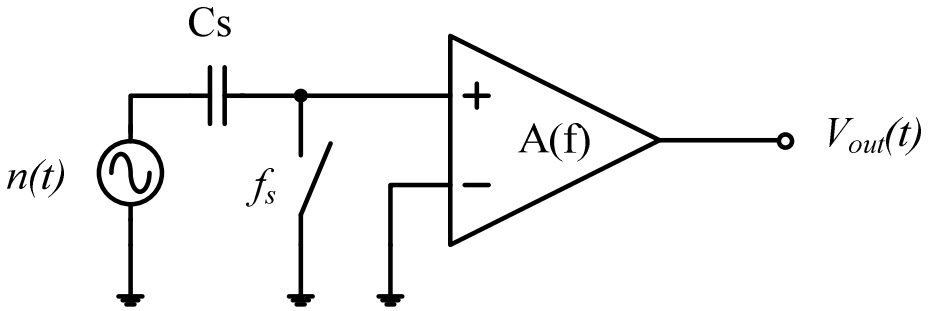


Figure 2.15 Noise sampling in auto-zero amplifiers.

gain, A=1, and the input signal is $V_{in}(t)$=0. The equivalent circuit for the noise sampling is shown in Fig. 2.15.

Assuming the switch is ideal, the voltage on the capacitor Cs is an ideal sample and hold signal. If kT_s are sampling time instants, $h(t)$ the hold function, the voltage on the capacitor Cs is:

$$V_{cs}(t) = \sum_{k=-\infty}^{\infty} n(kT_s)h(t - kT_s) \tag{2.9}$$

At the output of the amplifier we have a signal $V_{out}(t)$:

$$V_{out}(t) = n(t) - \sum_{k=-\infty}^{\infty} n(kT_s)h(t - kT_s) \tag{2.10}$$

Given the sample and hold of the noise and/or offset on the capacitor Cs the output spectrum is found to be:

$$V_{out}(f) = N(f) - sinc(\pi f T_s)\exp(-j\pi f T_s)\sum_{k=-\infty}^{\infty} N\left(f - \frac{k}{T_s}\right) \tag{2.11}$$

The output noise spectrum is a sequence of spectra shifted at multiples of the sampling frequency T_s. The transfer function for every harmonic $H_k(f)$ has a value of:

$$H_k(f) = \begin{cases} 1 - sinc(\pi f T_s)\exp(\pi f T_s) & k = 0 \\ sinc(\pi f T_s)\exp(\pi f T_s) & k \neq 0 \end{cases} \quad (2.12)$$

The transfer function for *k=0* has a zero at the origin and acts like a differentiator. Therefore, any DC component of the random process *n(t)* is cancelled out, which is why this technique is called auto-zero. The power spectral density of the output noise is found in equation (2.13)

$$S_{yy}(f) = |H_o(f)|2S_{xx}(f) + sinc^2(\pi f T_s)\sum_{k=-\infty}^{\infty} S_{xx}\left(f - \frac{k}{T_s}\right) \quad (2.13)$$

If the random process *n(t)* is white noise the second term from (2.13) introduces fold over components in the baseband. The first term takes care of 1/*f* noise and offset reduction. In conclusion, auto-zero amplifiers will reduce the offset and 1/*f* noise by using sampling techniques at the expense of increasing the white noise in the baseband.

2.7.3 Correlated Double Sampling (CDS) Technique

Correlated double sampling (CDS) is another technique for offset and noise reduction [19]. This CDS technique is a particular case of the auto-zero process. The main difference between auto-zero and CDS techniques is the way the signal is delivered to the output. In CDS methods, there are two sampling times, a sampling time for noise only and a second sampling time for noise and signal with opposite signs. In CDS the output is a sampled and hold signal whereas for auto-zero, the output is a continuous time output. Fig. 2.16 shows the CDS technique realization.

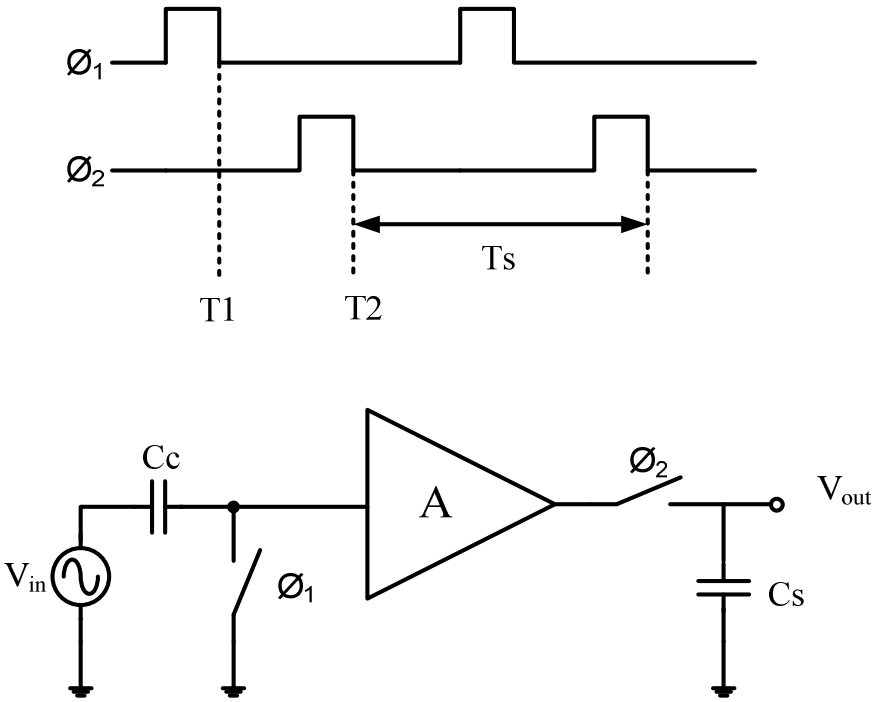


Fig. 2.16 Correlated double sampling technique.

The CDS operation is performed in two phases: 1) clamp, sampling of a reference value and noise at T1, and 2) sampling of disturbed signal with the clamped value subtracted at T2. If the noise of the clamp and sampling time is correlated, this signal-processing scheme results in an effective noise reduction.

CDS is used in sampled-data systems and particularly in SC circuits. Although the signal at the output of a circuit using CDS is now S/H, the effect of CDS on the amplifier offset and noise is very similar to that of the auto-zero process. The baseband transfer function still imposes a zero at the origin of frequency that cancels any offset and strongly reduces the 1/ *f* noise in the same way the auto-zero technique does. On the other hand, although the transfer functions for $k \neq 0$ are different from those obtained for the auto-zero process, the

fold over component due to aliasing is comparable since the wideband noise has already been sampled once. Therefore, the CDS technique also has the disadvantage of aliasing white noise in the baseband.

2.7.4 Chopper Modulation

The chopper technique is used to reduce the effects of flicker noise and DC offset in amplification systems. This method does not decrease either types of noise, it simply isolates the noise from the signal in the frequency domain so that the noise can be easily removed without affecting the signal.

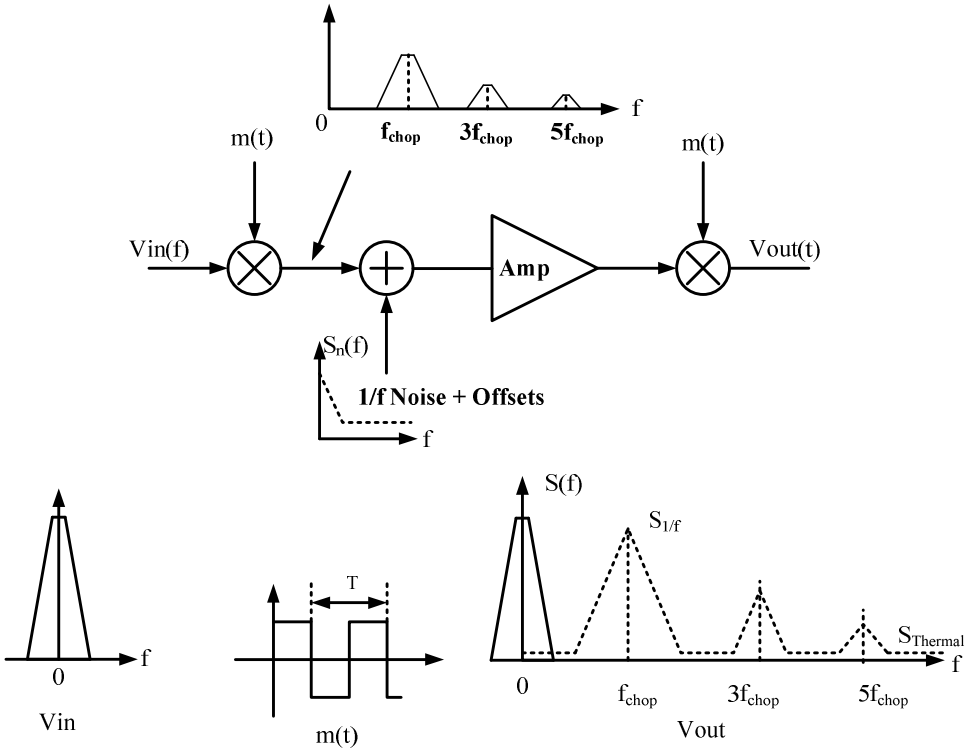


Figure 2.17 Chopper stabilization technique.

In this technique, as seen in Fig 2.17, the input signal is pushed to higher frequencies, specifically the odd harmonics of the chopper frequency where the flicker noise has an insignificant value. The converted signal is amplified and afterwards a second chopper modulator brings the signal back to its original band. The result is that the amplified signal does not contain a significant flicker noise component.

If the amplifier has an infinite bandwidth, the amplified signal can be recovered in its full strength since demodulation, which in this case is exactly the same as modulation, will collect the signal from all of the harmonics which modulated in previous stage. However, all amplifiers have a limited bandwidth so complete recovery is not possible [20]. As an example, if a V_{in} signal is used with an amplifier which has bandwidth of $2 \times f_{chop}$, where f_{chop} is the chopper frequency, and a gain of A, the recovered signal's amplitude would be $0.8 \times A \times V_{in}$ [21]. The chopper frequency, amplifier bandwidth or signal bandwidth can be chosen as seen in (2.14), provided that they can be changed by the designer. This equation assumes that the signal bandwidth is f_{signal}, amplifier bandwidth is f_{amp} and the chopper modulator is a square wave signal with a frequency f_{chop}.

$$f_{corner} + f_{signal} < f_{chop} < f_{amp} - f_{signal} \tag{2.14}$$

This equation implies that the smallest value of f_{chop} should at least be able to separate the flicker noise from the signal, and the highest value should not push the signals main harmonic out of the amplifier's passband.

The amplitude of the modulation signal decreases with $1/n$ where n is the harmonic number. Offset and $1/f$ noise are modulated at odd harmonics leaving

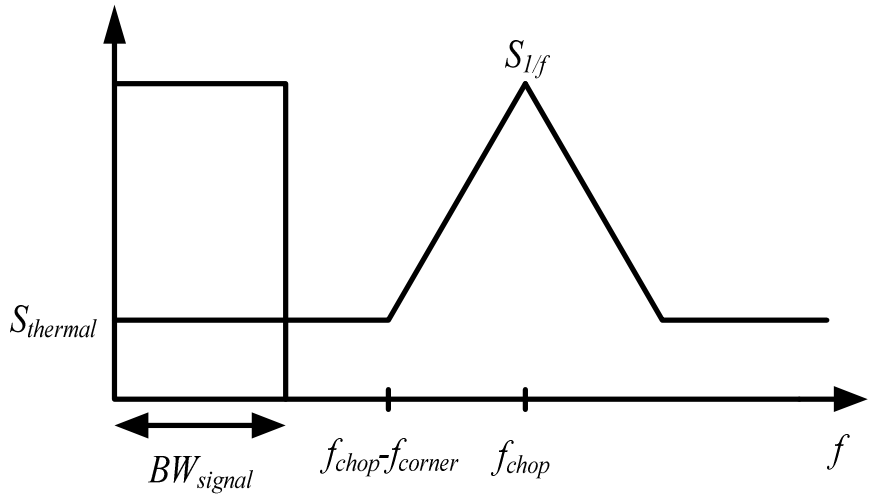


Figure 2.18 The baseband spectrum.

the baseband free of 1/*f* noise. In the ideal chopping case the bandwidth of the amplifier should be infinity. If this is true, multiplying the signal twice with *m(t)* will reconstruct the input signal. If the bandwidth of the amplifier is limited the result is a high frequency residue centered around the even harmonics, and the signal in the baseband is attenuated. To recover the signal the output should be low-pass filtered, as shown in Fig 2.18.

Given the corner frequency of the 1/*f* noise f_{corner} and the cutoff frequency of the low-pass filter at the output and BW_{signal}, the necessary condition to have complete reduction of the flicker noise in the baseband is found from using the following equation [22]:

$$f_{chop} \geq BW_{signal} + f_{corner} \tag{2.15}$$

To analyze the effect of chopping on the offset of the amplifier the offset has been represented in Fig. 2.17 at the input of the amplifier (Amp). As long as the frequency response of the amplifier is flat the output voltage $V_{out}(f)$ is found from the following equation:

$$V_{out}(f) = AV_{os} \otimes \frac{2}{j\pi} \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{1}{n} \delta\left(f - \frac{n}{T} \right) \tag{2.16}$$

This sequence of Dirac pulses has no DC component, and the offset at the output has a theoretical value of 0 V. It is clear that any temperature drift of the offset voltage is also cancelled out after chopper modulation.

The effect of the chopper modulation on the amplifier noise can be analyzed from Fig. 2.19 where $V_N(t)$ is the noise and $m(t)$ is the carrier signal. The PSD (power spectrum density) of the chopper output signal $V_{CS}(t)$ is given by:

$$S_{cs}(f) = \left(\frac{2}{\pi} \right)^2 \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{1}{n^2} S_N\left(f - \frac{n}{T} \right) \tag{2.17}$$

Eq. (2.16) can be approximated in the baseband ($|fT| \leq 0.5$) by a white noise PSD given by:

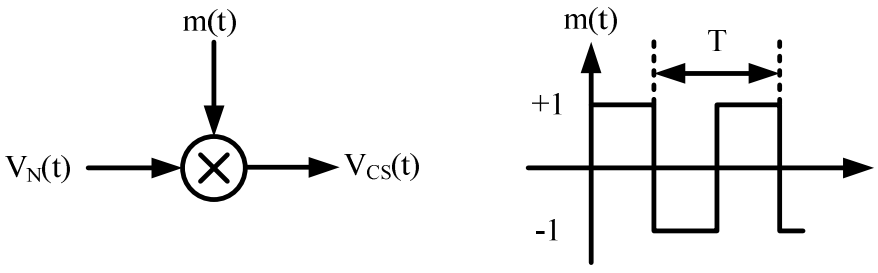


Figure 2.19 Chopper modulation.

$$S_{N,white}(f) = S_{N,white}(f=0) = S_o\left[1 - \frac{\tanh\left(\frac{\pi}{2} f_c T\right)}{\frac{\pi}{2} f_c T}\right] \tag{2.18}$$

which for $f_cT >>1$ can further approximated by:

$$S_{N,white}(f) = S_o \text{ , } for \left|fT\right| \le 0.5 \, and \;\; f_c T >> 1 \tag{2.19}$$

Unlike the auto-zero technique, the chopper modulation does not introduce aliasing of the broadband noise, which for auto-zero causes the PSD in the baseband to increase proportionally with the ratio of the noise bandwidth and the sampling frequency. As seen by (2.17), the baseband PSD resulting from chopper modulation is nearly constant (white noise), and it approaches to the value of the input white noise S_0 when f_cT is large.

The effect of the chopper modulation on the 1/*f* noise can also be analyzed assuming a cutoff frequency much larger than the chopper frequency and an input PSD given by,

$$S_{1/f}(f) = S_0 \frac{f_k}{f} = S_0 \frac{f_k T}{fT} \tag{2.20}$$

where S_0 is the white noise, T is the period of the modulation signal (*m(t)*), and f_k is the cutoff frequency. From (2.20), 1/*f* noise is transposed to $\pm 1/T$ and is applied to the odd harmonics of the chopper frequency. It also shows that the chopped 1/f noise PSD can be approximated in the baseband by a white noise component [26]:

$$S_{CS\_1/f}(f) = 0.8525 \, S_0 \, f_k T \tag{2.21}$$

Therefore, total noise in the baseband for a typical amplifier is given by:

$$S_{CS}(f) = S_0\left(1 + 0.8525 f_k T\right) \tag{2.22}$$

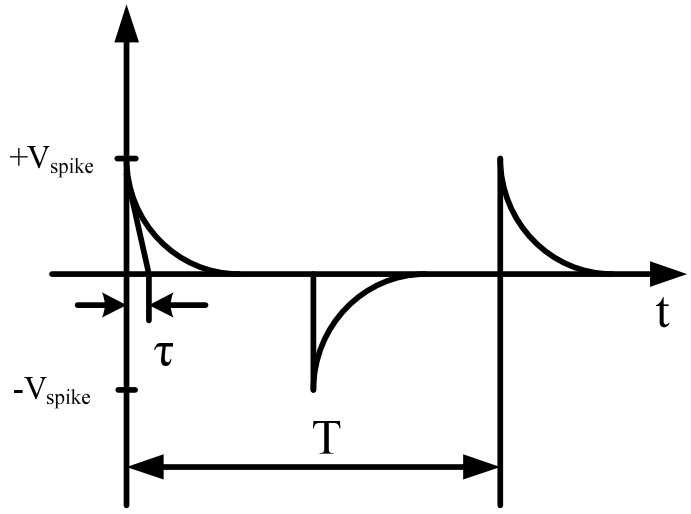


Figure 2.20 Spike signal at the amplifier input.

As seen by (2.22), the chopper stabilization technique does not affect the white noise and unlike an auto-zero technique, it transposes 1/*f* noise to a chopper frequency.

As mentioned above, residual offset is mainly due to clock feedthrough and charge injection in the input modulator. More generally, any spikes caused by the modulator non-idealities and appearing at the amplifier input will be amplified and demodulated by the output modulator, giving rise to a residual dc component. Since only the odd harmonics of the chopper frequency will contribute to the residual offset, the positive and negative spikes will have an odd symmetry in Fig. 2.20.

Using an amplifier with a bandwidth much larger than the chopper frequency results in a maximum gain but leads to a maximum output offset voltage since almost all of the spectral components of the spike signal will contribute. The input referred offset can be calculated assuming that $\tau << T/2$:

$$V_{os} \approx \frac{2\tau}{T} V_{spike} \tag{2.23}$$

where τ is a settling time constant of spike signal. Keeping the same gain A in the passband but limiting the bandwidth to twice the chopper frequency slightly lowers the overall DC gain to $(8/\pi^2)A=0.81A$, but greatly reduces the offset voltage referred to the input. The offset voltage is given by,

$$V_{os} \approx \left(\frac{2\tau}{T}\right)^2 V_{spike} \tag{2.24}$$

As seen in (2.24), if τ is much smaller than *T/2*, the offset voltage can be reduced sufficiently by limiting the amplifier bandwidth to twice the chopper frequency.

2.7.5 Nested-Chopper Modulation

In the low frequency band, the increase in flicker noise is proportional to the decrease in frequency. In the relative-low frequency band, the offset will dominate the noise, especially in sensor interface circuits, where system performance is limited. The chopper stabilized technique with conventional op-amps has been shown to have

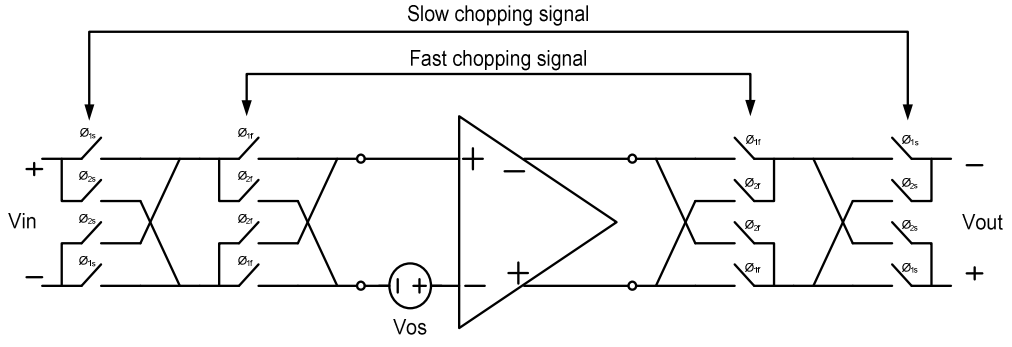


Figure 2.21 Nested-chopper modulation [23].

better immunity to low frequency noise. Unfortunately, the chopping approach also generates residue noise, which comes from the charge-injection mismatch between the switches during the operation of the chopper. One approach of dealing with this problem is proposed in [23]. This idea is depicted in Fig. 2.21.

In this technique another chopper pair operating at much lower frequencies than the first chopper pair is included in the circuit. The spikes, which were originally caused by the first chopper modulator, will be inverted by the second chopper modulator resulting in zero offset. The outer pair will still introduce an offset but since they operate at much lower frequencies it will be much lower than that of the version without the second pair. Using this technique 100 nV offset has been achieved by the authors.

CHAPTER 3

SIGNAM DELTA ANALOG TO DIGITAL CONVERTER AND DIGITAL TO ANALOG CONVERTER

Sigma delta Analog-Digital Converters (ΣΔ A/D) have been known for nearly thirty years, but only recently has the high-density digital VLSI existed to manufacture them as inexpensive integrated circuits [31]. Now, they are used in many applications where a low-cost, low-bandwidth, low-power, and high-resolution ADC is required. Thus, ΣΔ ADC can be used in biosensor applications with low power and low noise. The ΣΔ A/D combine the over sampling analog sigma delta modulators with digital decimation filters to achieve high precision and cost effective A/D conversion solutions. This type of converter is used to implement high-precision and low-power A/D converters for applications such as sensor interfaces and audio processing.

The demand of powerful digital signal processors implemented in CMOS technologies raises the need for robust, high-resolution analog-to-digital (ADC) and digital-to-analog converters (DAC). Converters should be integrated on the same substrate with the digital circuitry and provide high performance functionality. This requirement is met by oversampling analog-to-digital and digital –to-analog converters which are also the most suitable converters for both low frequency and high resolution applications. However, while ΣΔ modulators gain accuracy when utilized in precision analog circuits, implementation is difficult. Furthermore, proper implementation requires a small signal bandwidth [26], [27]. Nowadays, low-cost and small footprint gas chemical sensor with low

noise, low offset, high resolution, and low power consumption are required in a vast number of applications ranging from portable apparatus for hazardous gases in automobiles.

In this chapter, a CMOS first-order ΣΔ modulator for the readout of the conductometric sensor and amperometric sensor is presented. The interface IC is based on a front-end programmable switched capacitor ΣΔ modulator. This architecture decouples the two types of gas sensor from the optimized performance ΣΔ modulator.

3.1 ANALOG TO DIGITAL CONVERSION THEORY

Analog to digital conversion (ADC) is the process of sampling a continuous analog signal and converting the signal into a quantized representation of the signal in the digital domain. There are many different ADC architectures, such as successive approximation ADC, sigma delta ADC, flash ADC, and pipeline ADC, used to convert analog signals into digital signal representations. The conventional ADC transforms an analog input signal X(t) into a sequence of digital codes X(nT) at a sampling rate of $f_S = 1/T$, where T denotes the sampling interval or period and n is integer number. The sampling function is equivalent to modulating the input signal by a carrier signal. The sampled signal is represented as the signal frequency modulated by integer multiples of the sampling frequency and the summation of the original signal contents. Thus, any signal information about the Nyquist frequency in the input signal is seldom properly sampled because the signals will get folded into the base band signal in the sampled signal

which was not present in the original input signal. This non-linear behavior in sampling signal and folding or signal distortion is referred to aliasing. Therefore, to avoid this, anti-aliasing filters are required to prevent or reduce these aliasing artifacts. Successive approximation registers (SAR) and flash converters among many A/D converters work at the Nyquist rate (f_N). These converters sample the analog input signal according to a sample frequency (f_S) which is almost twice the maximum frequency of the input signal. A Nyquist rate ADC converts the analog signal into an n-bit representation depending on the Nyquist sample time. Since the Nyquist rate is two times the input frequency of the sample pass band of interest, an anti-aliasing filter is required to make the limitation in the maximum input frequency for the A/D converter.

3.2 SIGMA DELTA ANALOG TO DIGITAL CONVERTER

Analog-to-digital converters can be categorized into two types depending on the sampling rate [28]. As mentioned previously, the first group samples the analog input at the Nyquist frequency f_N such that $f_S = f_N = 2f_B$, where f_S is the sampling frequency and f_B is the bandwidth of the input signal. The second type of ADCs samples the analog input at much higher frequencies than the Nyquist frequency, and are called oversampling ADCs [29]. A sigma delta (ΣΔ) ADC can be under this second category. In ΣΔ ADC, the input signal is sampled at oversampling frequency $f_s = OSR \times 2f_b$ where OSR is defined as the oversampling ratio and is given by:

$$OSR = \frac{f_s}{2 f_b} \tag{3.1}$$

Sigma delta analog-to-digital converters do not instantly digitize the analog signal into a digital sample of n-bit precision at the Nyquist frequency. Instead, a sigma delta ADC over samples the analog signal by an over sample ratio of *OSR* resulting in $f_N << f_S$ in equation 3.1 shown. The over sampling A/D conversion is performed at a lower precision with a coarser quantization. In fact, many ΣΔ ADCs have a 1-bit quantizer normally. As shown in Fig. 3.1, the output of the 1-bit ADC is a bit stream with the one's density of the stream proportional to the magnitude of the sine wave input. The 1 -ADC stream that is generated at the f_S sampling frequency can be digitally filtered out and decimated back down to a Nyquist rate of n-bit precision samples.

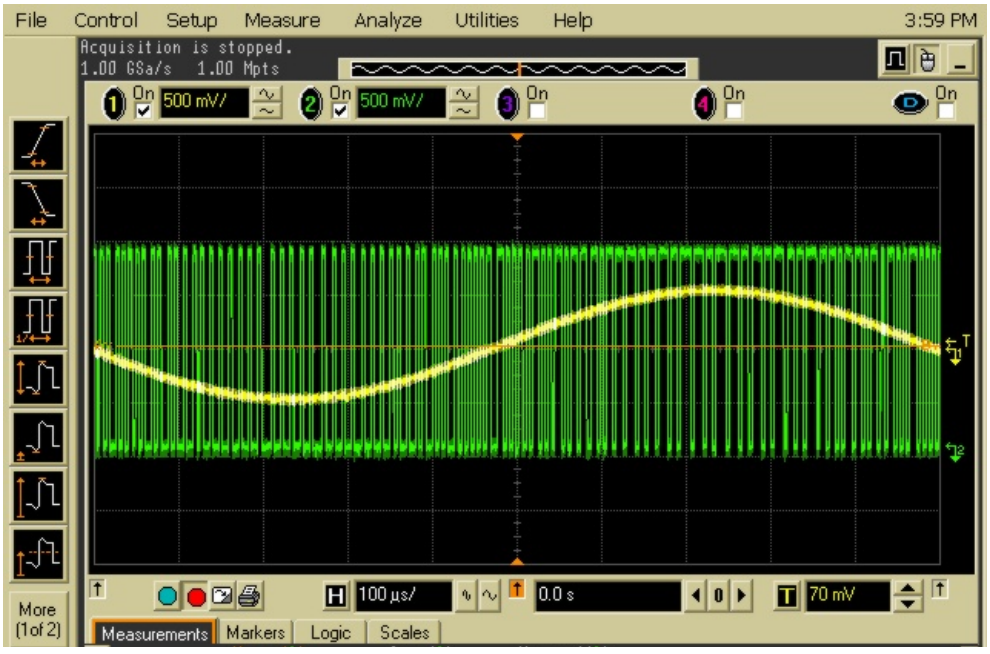


Figure 3.1 ΣΔ modulator output with a 1 kHz sine wave input.

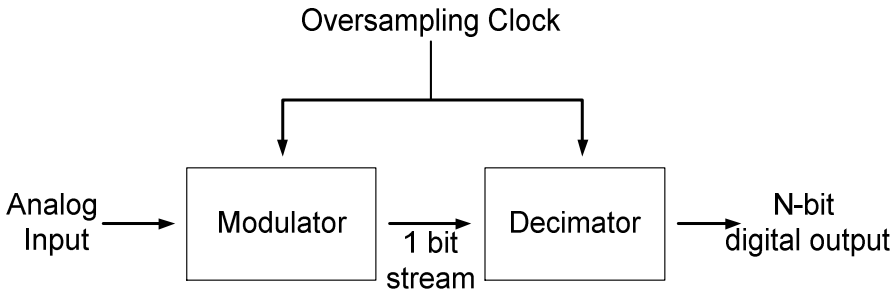


Figure 3.2 Block diagram of a ΣΔ ADC.

The block diagram of a sigma-delta ADC is shown in Fig. 3.2. The modulator samples the analog input signal at much higher frequencies by the oversampling ratio and converts the analog input signal into a pulse density modulated digital signal containing both the original input signal and the unwanted out of band noise [30]. A decimation filter following the modulator filters out the out-of-band noise. Both the modulator and the decimator are operated with the same oversampling clock. As shown in Fig. 3.2, the modulator is the first order with a 1-bit quantizer and generates a 1-bit output. The output of the decimator is also shown as n-bit digital data: n-bit is the output resolution of the ADC and is dependent on the oversampling ratio, *OSR*. The order of the decimator depends on the order of the modulator. Usually the order of the decimator is one more than the order of the modulator [32].

In fact, the 1-bit stream of ADC is digitally filtered to obtain an n-bit representation of the analog input. The 1-bit ADC stream is accumulated until sampling cycles reach OSR and divided by ADC resolution n - bit. This procedure

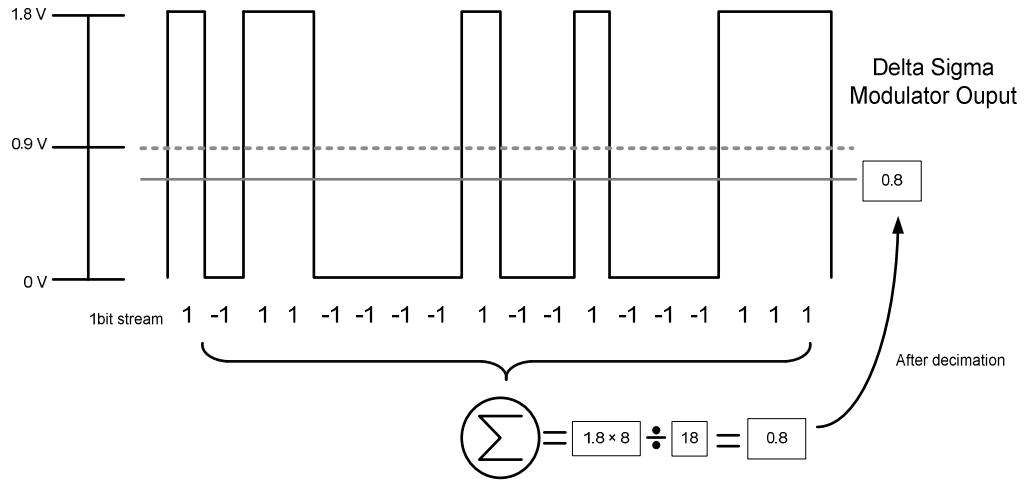


Figure 3.3 ΣΔ A/D stream accumulated and decimated to represent an n-bit value of the input.

yields a decimated value which is the average value of the bit stream from the modulator as shown in Fig. 3.3. Decimation filters will be discussed in next section.

In addition to anti-aliasing, a Nyquist rate ADC also requires a precise sample and hold analog circuit [33]. The circuit holds continuous amplitude, discrete time samples of the analog waveform stable while the converter performs the quantization. The sample and hold output is compared to a set of reference levels within the ADC. The quality and precision of these reference levels is a limiting factor for high resolution A/D converters. For instance, a 16-bit ADC requires 2^{16} (=65535) different reference levels. A typical converter may span a 1.8V input range. The spacing between any adjunct two levels is only 27.5 μV. This type of matching is difficult to achieve on a normal Nyquist integrated circuit without the use of expensive and complicated trimming techniques.

One of the major advantages of ΣΔ ADCs over a conventional parallel or Nyquist ADC is the relaxation of the requirements for the anti-aliasing filter. As mentioned above, the requirement of an anti-aliasing filter for a Nyquist rate ADC is a sharp transition from the pass band (f_B) to stop band ($fs/2$) as mentioned before. The anti-aliasing filter for a conventional ADC needs to be flat through the pass band and attenuate signals above the stop band by an attenuation factor greater than the dynamic range of the ADC [33].

An over sampling A/D converter moves the sampling frequency (f_S) much farther away from the original sampling frequency with a Nyquist rate converter by an oversampling ratio. Since the complexity of an anti-aliasing filter is proportional to the ratio of the width of the transition band to the width of the pass band, over sampled converters require far simpler anti-aliasing filters than Nyquist rate converters with similar performance. What has been a complex filter requiring significant component matching in the Nyquist rate converter can be replaced by a simple RC filter in an oversampled converter [32].

3.3 FISRT ORDER MODULATOR

The modulator is the analog part of a sigma-delta ADC as shown Fig. 3.2. The final resolution of the ADC is dependent on both the order of the modulator and the oversampling ratio at the modulator stage. Since the modulator uses the principle of oversampling, the critical need for an anti-aliasing filter may be eliminated and the analog input signal can directly be sampled using the oversampling ratio [34]. Due to oversampling of the analog signal, the accuracy

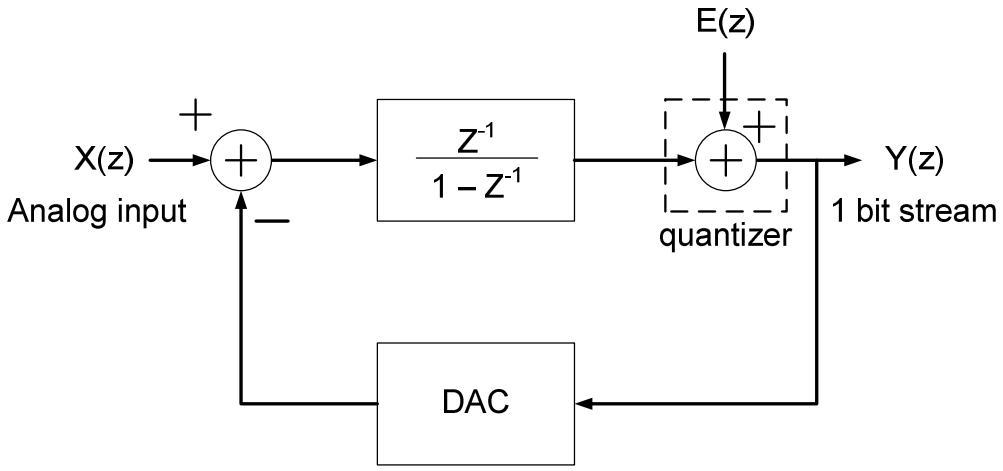


Figure 3.4 Block diagram of a first-order modulator.

of the analog circuitry can be compromised with the speed. The modulator shapes the quantization noise to higher frequencies, which can be filtered out by using a digital low pass filter at the decimation stage. The modulator outputs a 1-bit digital data, which is applied as an input to the decimator stage with low pass filtering. The basic block diagram of the first order modulator design is shown in Fig. 3.4. The difference between the analog input and the output of a digital-to-analog converter (DAC) is applied to an integrator, which is quantized to generate a pulse density modulated (PDM) 1-bit digital stream output.

For the case of a 1-level quantizer, the ADC and DAC reduce to a simple clocked comparator with a direct feedback connection. To develop a linear presentation for the modulator and characterize the spectral response of the quantization noise, the following assumptions (Bennett's criteria) are made concerning the input signal [32], [34]:

- The modulator's input signal falls within the DAC's output levels (reference level). Hence, no saturation of the digital output code occurs. In other words, exceeding the normal operating range of the ΣΔ ADC affects the quantization noise spectrum by adding spurs (tones) or spikes to the output spectrum.
- The modulator's least significant bit (LSB) is much smaller than the input signal amplitude. Otherwise, the output of the modulator can look like square wave which results in tonal output spectral. However, adding or subtracting a feedback signal based on the expected or past quantization noise helps to avoid these spurs.
- The input signal is busy or unpredicted with no DC or very low-frequency components. In other words, no two consecutive outputs of the modulator have the same digital code. In first order sigma delta ADC case, adding a high frequency dither signal or pseudo-random noise to the input helps to make the input signal randomized and suppress the tones. This high-frequency noise is eventually filtered by a digital filter or an output reconstruction filter.

With these assumptions, the operation of the modulator can be better understood from the linear quantizer model of Fig. 3.5, in which the quantizer is replaced by an additive quantization error source, Q[n]. In this model, the input signal, X[n], is a busy signal and the quantization error values resemble uncorrelated samples with a flat frequency spectrum.

In Figure 3.5, the summation takes the difference between the input signal and the feedback signal from DAC. The integrator accumulates this difference

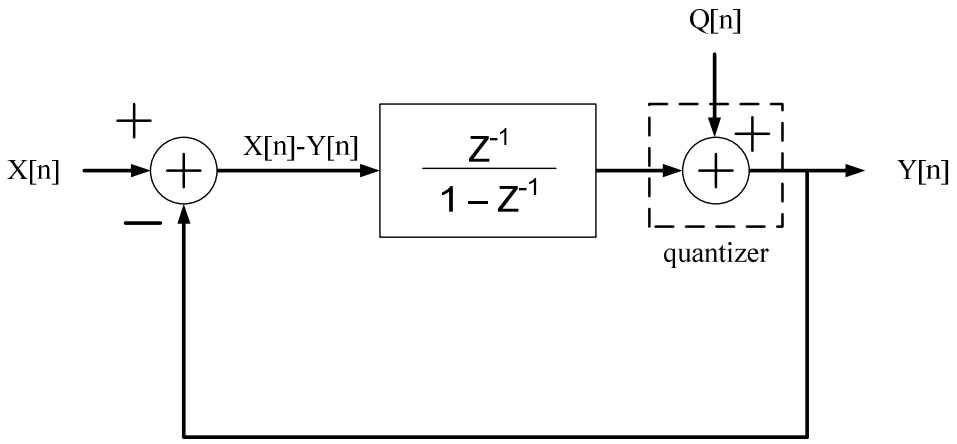


Figure 3.5 Linear model of a first order sigma delta modulator with 1-bit DAC.

(X[n]-Y[n]) and feeds the result back to the summation node through the quantizer. This process explains the output of the modulator to track the average value of the input. When quantization error is positive, the feedback signal is greater than the input, otherwise it is smaller than the input signal. Sometimes, the average feedback signal should ideally be the same as the input signal if no quantization error exists. One of the oversampling converters are ΣΔ modulators, which means that the quantization noise power is spread over the sampling frequency range and small parts of it fall in the signal band width. As defined previously, the ratio of the sampling frequency over the Nyquist rate (twice of the signal bandwidth of f_B) is the oversampling ratio (*OSR*). The quantization noise in the signal band is more suppressed by the loop filter gain. Fig 3.5 shows that the input signal simply passing through the modulator with a delay unit while the quantization noise is differentiated and pushed to higher frequencies. The output is equal to:

$$Y(Z) = H(Z)X(Z) + H(Z)Q(Z) = Z^{-1}X(Z) + (1 - Z^{-1})Q(Z) \tag{3.2}$$

The magnitude of the quantization noise transfer function *H(Z)* is found as below [32]:

$$NTF\ \ H(e^{sT_s}) = \left(1 - e^{sT_s}\right) = (1 - e^{-jwT_s})\frac{2j}{2j}\frac{e^{\frac{j\pi f}{f_s}}}{\frac{ej\pi f}{f_s}} = \left(\frac{e^{j\pi f/f_s} - e^{-j\pi f/f_s}}{2j}\right)2je^{j\pi f/f_s}$$

$$NTF\ \left|1 - z^{-1}\right| = \left(1 - e^{sT_s}\right) = (2\sin \pi f T_s) \approx 2\pi f T_s = \frac{\pi}{OSR} \tag{3.3}$$

for frequencies which satisfy f<<1, $\left|NTF\right|^2 \approx \left(2\pi f / f_s\right)^2$. It is a high pass response, which suppresses the quantization noise at and near DC and amplifies it out of band at $f_s/2$. This noise- shaping action is the key to the effectiveness of ΣΔ modulation.

In Fig. 3.5, the quantization noise model is linear white noise model. This simplifies the analysis of an ADC system, because a deterministic nonlinear system is replaced by a stochastic linear one, i.e. the quantization error becomes a

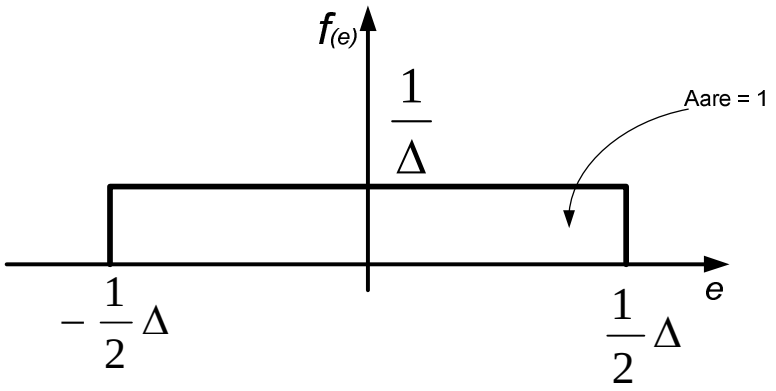


Figure 3.6 Probability density (PDF) of the quantization error.

quantization noise. The LSB between positive and negative reference is defined by Δ. The noise generated by a quantizer with two levels equally spaced by Δ is uncorrelated and has equal probability of laying anywhere in between ±0.5Δ in Fig. 3.6. As shown in Fig. 3.6, the probability density function (PDF) of this error is1/Δ. The average power and the power spectral density of this quantization noise are calculated as:

$$S_Q(e) = \int_{-\infty}^{\infty} e^2 f(e) de = \frac{\Delta^2}{12} \tag{3.4}$$

It should be noted at this point that the total quantization noise power is independent of the sampling frequency and is only determined by the quantizer resolution. Since the signals at the quantizer are sampled signals, all the quantization noise power is folded into the frequency range [-f_s/2, f_s/2]. Thus, with the white noise approximation in Fig. 3.7, the power spectral density of the quantization noise is:

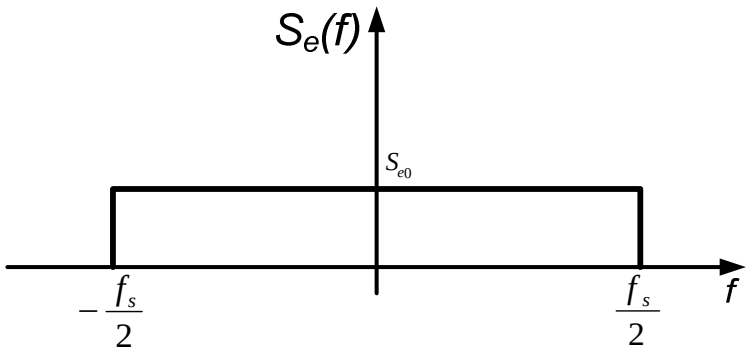


Figure 3.7 Power spectrum density (PSD) of the quantization error.

$$S_e(f) = \int_{-\frac{fs}{2}}^{\frac{fs}{2}} S_Q(e)df = \frac{\Delta^2}{12}\frac{1}{f_s} \tag{3.5}$$

The in-band quantization noise power over the sampling frequency band of $-f_s$ to f_s is equal to

$$PQ = \int_{-f_B}^{f_B} S_Q(e)\left|H(NTF)\right|^2 df = \int_{-f_B}^{f_B} \frac{\Delta^2}{12}\frac{1}{f_s}\left\{\frac{2\pi f}{f_s}\right\}^2 df$$

$$= \int_{-f_B}^{f_B} \frac{\Delta^2}{12}\frac{1}{f_s}\left\{\frac{2\pi f}{f_s}\right\}^2 df = \frac{\Delta^2}{12}\frac{1}{f_s}\frac{\pi^2}{3}\left\{\frac{2f}{f_s}\right\}^3 = \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3, \; if\ OSR >> 1 \tag{3.6}$$

Because of the oversampling, the signal bandwidth is much smaller than the sampling frequency (i.e. OSR>>1) and the following approximation is valid. One can assume the input signal is a sinusoidal wave between positive reference voltage ($+V_{REF}$) and negative reference voltage ($-V_{REF}$) and its root mean square power is $V_{REF}^2/8$. The signal-to-noise ratio (SNR) for an n-bit A/D converter with quantization level of $\Delta = 2 \times V_{REF}/2^N$ is defined by

$$SNR = 10\log\frac{\left(\frac{1}{2}\frac{V_{ref}^{\ 2}}{4}\right)}{\left(\frac{\Delta^2}{12}\right)} = 10\log\frac{\left(\frac{V_{ref}^{\ 2}}{8}\right)}{\left(\frac{\frac{2V_{REF}^{\ 2}}{2^N}}{12}\right)} = 6.02N + 1.76\ [dB] \tag{3.7}$$

If the same input power is used in the 1st order ΣΔ modulator, the SNR by the modulator's quantization noise is

$$SNR = 10\log\frac{\left(\frac{1}{2}\frac{V_{ref}{}^2}{4}\right)}{\left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{2f_B}{f_s}\right)^3} = 6.02 + 1.76 - 10\log\left(\frac{\pi^2}{3}\right) + 10\log(OSR)^3$$

$$= 6.02N + 1.76 - 5.17 + 30\log OSR \tag{3.8}$$

The equation (3.8) can predict an increase of *OSR* in the *SNR* of an oversampling modulator. In other words, (3.8) corresponds to 1.5 bit increase in resolution for a doubling in the OSR. Thus, it is evident that a combination of noise shaping and oversampling is a favorable concept for achieving high resolution ADC. For example, when an input signal has 1 kHz bandwidth and the sampling frequency is 1 MHz, the *OSR* is 500 as equation (3.1). This *OSR* results in a remarkable increase of 80.96 dB in SNR. By using (3.8), the overall SNR in 1st order ΣΔ ADC is then equal to:

$$SNR = 6.02 + 1.76 - 5.17 + 30\log 500 = 83.58 \text{ dB} \tag{3.9}$$

Thus, the resolution will be 14 bit.

A main drawback of the first-order ΣΔ modulator described above is the generation of tones and pattern noise appearing in the output [32], which is in strong disagreement with the theoretical behavior following the linearized model in Fig. 3.5. This is due to the assumption of the lack of a correlation between the quantizer input signal and the quantization error Q[n] in Bennett's theorems in previous section. Thus, when the input to the quantizer is not a random signal, the quantization noise will no longer be white. Especially, in a first order modulator, the input signal and the quantizer input are strongly correlated, while the output

contains strong in-band frequency tones. This is worse, if an additional dc signal is applied. For dc input signals the first order ΣΔ modulator runs into repetitive patterns, trying to equal the input level on average.

A possible solution to this problem is to include a pseudorandom noise (PRN) source at the quantizer input in order to add some nonperiodic signals which are called dither. Therewith a partial correlation of the quantization error from the input signal can be achieved in low-order modulators. The implementation of this PRN with linear feedback shift registers will be discussed in chapter 5.

3.4 DECIMATOR

The process of converting the sampling rate of a signal from a given higher rate f_S to a lower rate f_N is called decimation [34], [36]. Decimation in the dictionary means reduction by 10 percent, but in signal processing decimation means a reduction in sampling rate by any factor (integer number) as shown Fig. 3.3.

Basically a decimator is a digital low-pass filter which performs the operation of sample rate reduction. The sigma-delta modulator pushes quantization noise to higher frequencies so that the decimation stage after the modulator output should filter this noise out above the cutoff frequency, *fs/2*.

The band limited signal can then be re-sampled by discarding K samples out of every K samples, where K being the oversampling ratio. By averaging every K samples out of the quantized sigma delta output, the decimation filter

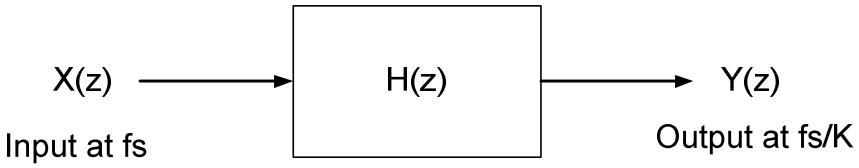


Figure 3.8 Basic block diagrammatic representation of the decimator.

achieves a high output resolution and the frequency of the output data is at twice the input signal bandwidth which is the Nyquist rate.

3.4.1 Decimator Theory

Decimation is the processes of lowering the word rate of a digitally encoded signal. It is usually carried out to increase the resolution of an oversampled signal and to remove the out-of-band noise. In a sigma delta ADC, oversampling the analog input signal by the modulator does not lower the quantization noise. In fact, the modulator just pushes the noise to high frequency. The ADC should employ an averaging filter, which works as a decimator to remove the noise and to achieve higher resolutions. A basic block diagrammatic representation of the decimator is shown in Fig. 3.8.

The decimator is a combination of a low pass filter and a down sampler. In Fig. 3.8 the transfer function, H(z) is representative of performing both the operations. The output word rate of the decimator is down sampled by the factor K, where K is the oversampling ratio. The function of low-pass filtering and down sampling can be carried out using an averaging circuit. The transfer function of

the averaging circuit is given by equation (3.12). It establishes a relation between the input and output functions [34].

$$H(Z) = \frac{Y(Z)}{X(Z)} = \frac{1}{K}\sum_{x=0}^{k-1} Z^{-x} \tag{3.11}$$

$$H(Z) = \frac{1}{K}\frac{1-Z^{-k}}{1-Z^{-1}} \tag{3.12}$$

The averaging circuit defined by the equation (3.12) averages every K samples. By converting the z-domain transfer function into the frequency domain with $Z = e^{sT_s}$, the characteristics of the circuit can be plotted in Fig. 3.9. The frequency response of the decimator is given by equation (3.13) [36].

$$H(f) = \frac{1}{K}\frac{1-e^{-sT_s k}}{1-e^{-sT_s}} = \frac{\sin c\left(\frac{K\pi f}{fs}\right)}{K\sin c\left(\frac{\pi f}{fs}\right)} \tag{3.13}$$

The frequency response of the averaging circuit, which is used as a decimator, is similar to that of a sync filter as a digital low pass filter [32]. The sync filter can be used to filter out the high frequency noise from the modulated input signal. The signal band is the range of frequencies from zero to the signal bandwidth *fs/2K* in main lobe. The sync filter attenuates any signal above the Nyquist rate *fs/K, 2fs/K and Nfs/K* to remove the out-of-band noise. In order to satisfy the digital low-pass filter characteristics, the attenuation in the stop band should be high. In designing a decimation filter, the ratio of the main lobe to the side lobe forms a critical factor. The filter characteristics can be improved to have

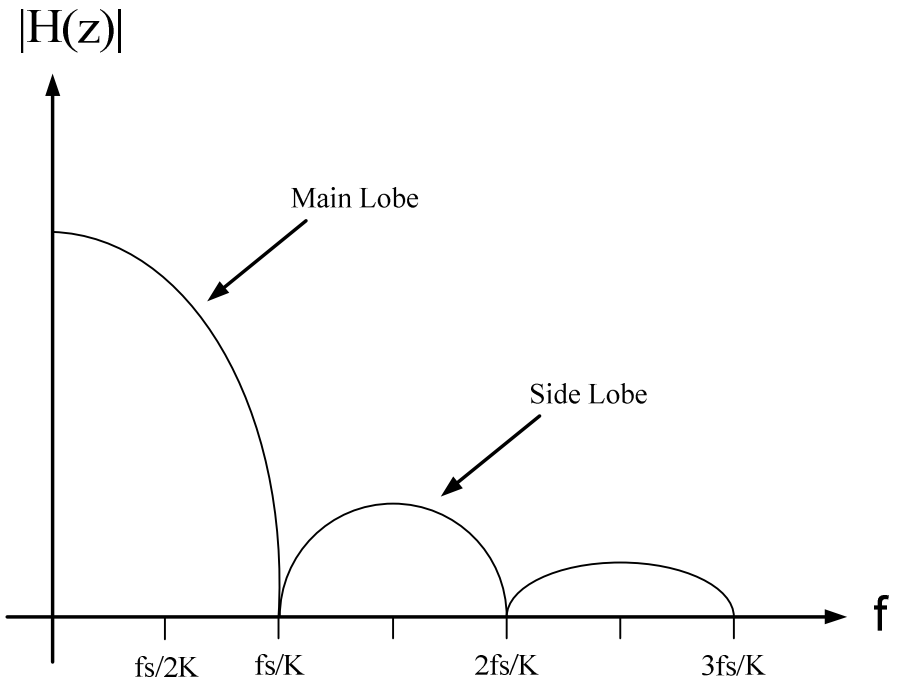


Figure 3.9 Frequency response of a sync averaging filter

a sharp transition between the pass band and the stop band in addition to good attenuation in the stop band by cascading the decimation stages. In Fig. 3.9, the gain of the filter is the value *K*. Increasing the value of *K* means increasing the final output resolution and has no direct significance on the frequency response. The decimator averages every *K* samples. In fact, the variable K is the oversampling ratio and since the output occurs at every K^{th} sample, the output rate of the decimator is *fs/K*. The input to a decimator is the sequence of bits of 1's and 0's because of ΣΔ modulator output. Since the averaging operation involves the addition of these input bits, the output resolution increases due to the addition of every K number of bits. The relation between the number of bits increased to the

oversampling ratio K for a first order sigma-delta ADC is given by equation (3.14) [32].

$$6.02N + 1.76 = 6.02 + 1.76 - 5.17 + 30\log K$$

$$N = \frac{30\log K - 5.17}{6.02} + 1 \tag{3.14}$$

The final output resolution of the decimator not only depends on the oversampling ratio but also on the input resolution as 1 in shown (3.14). The output of the modulator is applied as an input to the decimator, but the output resolution of the modulator depends on the quantizer level in the modulator designed (or the order of modulator). In this work, a first order modulator is considered; therefore, the output of the modulator is a 1-bit digital data.

In the present work, the decimator is designed to form a ΣΔ ADC by cascading it with an already-designed modulator. The designed modulator is the first order and based on the following equation (3.15). As a result, the order of the decimator has to be two [32].

$$L = 1 + M \tag{3.15}$$

In equation (3.15), L is the order of the decimator and M is the order of the modulator. The complete transfer function of the decimator of order L is given in equation (3.16).

$$H(Z) = \left(\frac{1}{K} \frac{1 - Z^{-k}}{1 - Z^{-1}} \right)^{L} \tag{3.16}$$

From this equation, higher order decimator filters can be designed by cascading single stage decimation stage. Thus, for the first order ΣΔ modulator, a second order decimator will be suitable to achieved filter characteristics.

3.4.2 Cascaded Integrator Comb (CIC) Filter Theory

The cascaded integrator combo (CIC) filter is a combination of digital integrator and differentiator stages in series which performs the decimation and low pass filtering in Fig. 3.10. The CIC filters do not require any multiplier circuits. Therefore, they are very economical for implementation in hardware. Generally, the problems in a filter design implemented by an accumulate-and-dump circuit are overcome with the CIC design. Equation (3.17) gives the transfer function of the CIC filter in z-domain and it is similar to equation (3.16) except the numerator term and the denominator terms are separated [32].

The numerator represents the transfer function of a differentiator and the denominator indicates that of an integrator.

$$H(Z) = \left(1 - Z^{-k}\right)^{L} \left(\frac{1}{K}\right)^{L} \left(\frac{1}{1 - Z^{-1}}\right)^{L} \tag{3.17}$$

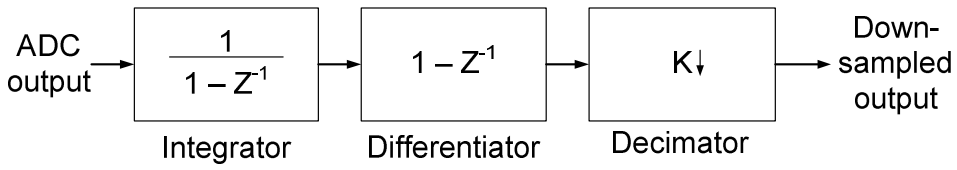


Figure 3.10 First order CIC decimation filter

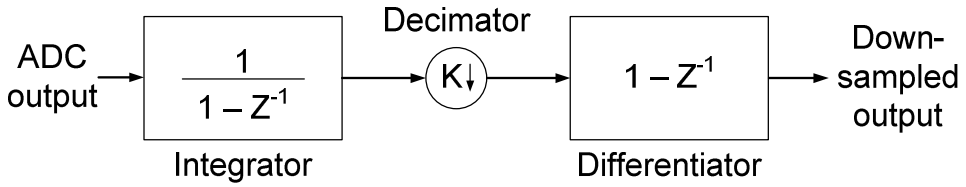


Figure 3.11 Equivalent block diagram for first order CIC decimation filter

The transfer function of both the CIC filter and the filter with an accumulator-and-dump circuit are similar, but the way the circuits are implemented is different. The CIC filter first performs the averaging operation and then follows it with the decimation not like in the accumulate-and-dump circuit where the averaging and decimation operations occur at the same time. A simple block diagram of a first order CIC filter is shown in Fig. 3.11. The unit needed to implement the CIC filter shown in Fig. 3.8 is very significant because of the delay elements that are used in the differentiator stage. It can be seen that the differentiator circuit needs K delay elements. The delays are implemented using registers in the hardware circuit. As the oversampling ratio increases, the number of delay elements also increases as well as the number of register bits that are used to store the data. The above design also requires another decimation circuit for decreasing the data rate, which requires additional hardware. Hence it becomes very cumbersome to design the differentiator with many delay elements. Because of the problem with the area, most decimation filter can be implemented in software like MatLab or LabView. Also, in hardware implementation, a clock

divider circuit in-between the integrator and differentiator stages is used to reduce area. The clock divider circuit divides the oversampling clock signal by the oversampling ratio K. By dividing the clock frequency by K the number of delay elements used in the differentiator can be reduced to just one. In Fig. 3.11, the integrator operates at the sampling clock frequency *fs* while the differentiator operates at down sampled clock frequency of *fs/K*. By operating the differentiator at lower frequencies, a reduction in the power consumption is achieved. In this research, the CIC filter based on this model has been designed. In this work, CIC is implemented in software to reduce area and substrate coupling noise as well as reduce the many sensor channels, interface circuitry and ADC occupied in analog front-end (AFE). The following sections discuss the integrator and differentiator.

3.4.3 Digital Integrator

The digital integrator is similar to an accumulator which is used to store or accumulate the sum of the input data. It is a single-pole Infinite Impulse Response (IIR) filter with a filter coefficient factor of one. The transfer function of the integrator is shown in equation (3.18) [32].

$$Y[nT_s] = X[nT_s] + Y[(n+1)T_s]$$

$$\frac{Y}{X}(Z) = H(Z) = \frac{1}{1 - Z^{-1}} \tag{3.18}$$

The output of the integrator is the sum of the input and the delayed output. This procedure can be observed from the time domain representation equation (3.18). Based on equation (3.18), a block diagram of the digital integrator can be

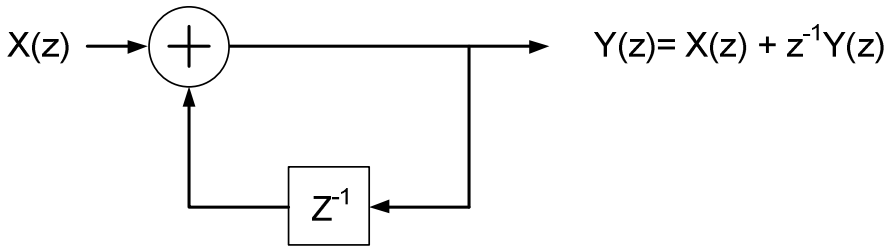


Figure 3.12 Block diagram of digital integrator

modeled and is shown in Fig. 3.12. The delay unit is used to delay the output signal by one clock period and can be implemented in hardware design using a memory element such as a simple register. The transfer function (3.18) in z-domain representation can be converted into a frequency domain by substituting Z with e^{sTs}. The magnitude response of the integrator is given by equation (3.19)

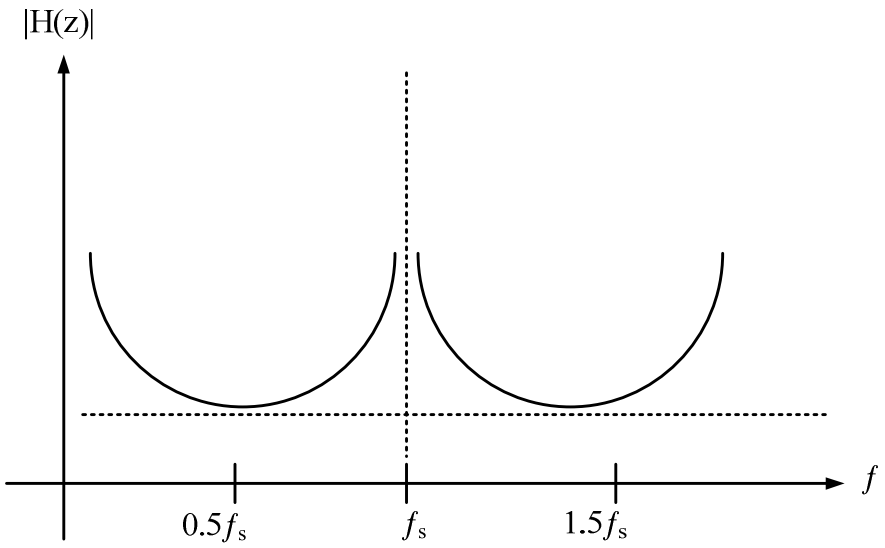


Figure 3.13 Frequency response of digital integrator.

and the plot showing the magnitude response of the integrator is shown in Fig 3.13 [32].

$$H(f) = \frac{1}{1 - e^{-sTs}} = \frac{1}{1 - e^{-j2\pi f / fs}}$$

$$\left|H(f)\right| = \frac{1}{\sqrt{2\left(1 - \cos\left(2\pi \frac{f}{f_s}\right)\right)}} \tag{3.19}$$

In equation (3.19), the integrator has an infinite gain at DC and at multiples of the sampling frequency (*fs*). The integrator has a minimum value of 0.5, but the frequency of operation that is of interest is at *fs*. Since the gain is infinite at DC and at *fs*, hardware design should take into account that the gain might cause the integrator to become unstable and there is every chance that the register used in the delay element could overflow causing data loss. In order to avoid problems with register overflow, the two's complement coding scheme is needed. By using the two's complement method of coding, the data will not be lost even when the register overflow occurs. In accumulate-and-dump circuits, an accumulator is an integrator, and since binary form is used, data loss could be possible [34]. This is another advantage of the CIC filter as it avoids the data loss due to register overflow. Here, N is the number of input bits to that particular integrator stage. Each integrator achieves an increase in resolution by log_2K bits. The input size of an integrator to avoid data loss is given by equation (3.20) [34].

$$\text{Register size M (in bits)} = \log_2 K + N \tag{3.20}$$

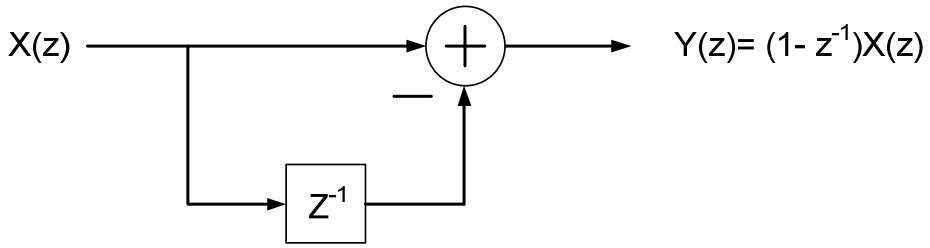


Figure 3.14 Block diagram of digital differentiator.

In order to boost the word size to that shown in equation (3.20) each integrator is preceded with a coder circuit.

3.4.4 Digital Differentiator

A differentiator circuit, also called a comb filter, is a Finite Impulse Response (FIR) filter. A comb filter is a digital low pass filter. The time domain expression and the transfer function of the differentiator are given in equation (3.21). From the time domain representation it is explained that the output of the differentiator is the difference between the present input and the past input.

$$Y[nT_s] = X[nT_s] - X[(n-1)T_s]$$

$$\frac{Y}{X}(Z) = H(Z) = 1 - Z^{-1} \tag{3.21}$$

The block diagram of the differentiator is modeled in Fig. 3.14. The transfer function (3.21) is converted into the frequency response and the expression for the magnitude response is given by equation (3.22) [32]. The plot

of magnitude response of the differentiator is shown in Fig. 3.15. The two's complement output of the integrator is applied as the input to the differentiator, and so the differentiator also uses the two's complement scheme of coding.

$$H(f) = 1 - e^{-sTs} = 1 - e^{-j2\pi f / fs}$$

$$|H(f)| = \sqrt{2\left(1 - \cos\left(2\pi \frac{f}{f_s}\right)\right)} \tag{3.22}$$

The final output of the decimator is the output of the differentiator and the output is in binary form; thus, the two's complement output is converted back to the binary form. It should be noted that the differentiator operates at a different clock frequency compared to the clock frequency of the integrator as explained above. Because of this, both the circuits act as individual blocks and can be used for cascading in order to form a cascaded integrator comb filter.

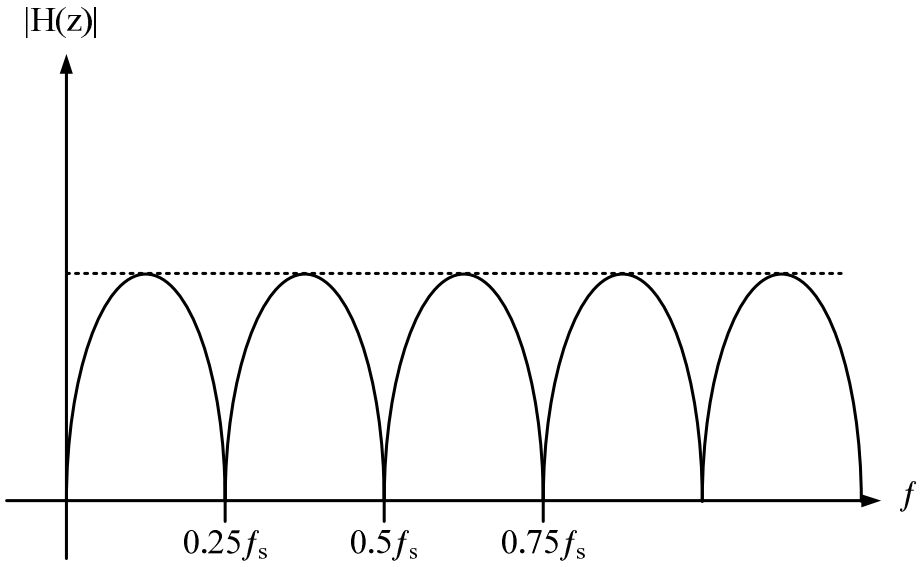


Figure 3.15 Frequency response for digital differentiator.

3.5 CURRENT-STEERING DIGITAL TO ANALOG (DAC) CONVERTER

Despite the widespread use of digital electronics, the real world is still analog. As a result, digital-to-analog converters (DACs) are needed as interfaces between digital and analog circuit sections. Moreover, due to the fast increasing demand for IC technology, high-speed DACs are needed in many applications. In particular, current-steering converters have shown to be suitable candidates for applications requiring high speed and high resolution. Indeed, they exhibit an inherent speed potential, since no output buffer is needed to drive the load [37], [38].

In conventional current-steering DACs the current switch is usually implemented using a differential pair [37]. The use of this circuit, besides allowing differential output, is mandatory in order to prevent the current source from completely switching off. As such, output glitches are reduced.

Although a full thermometer-coded DAC gives the best performance, it is unpractical for exclusive use due to its complexity. Currently, high-performance DACs are implemented using a segmented architecture, consisting of a binary-weighted and a thermometer-coded sub-DAC for the least significant bits (LSBs) and the most significant bits (MSBs), respectively.

Basically, a current-steering converter is made up of an array of weighted current sources that are switched to the output by current-steering switches controlled by the input bits. Current sources must be well matched in order to guarantee good static linearity performance. According to the weight assigned to

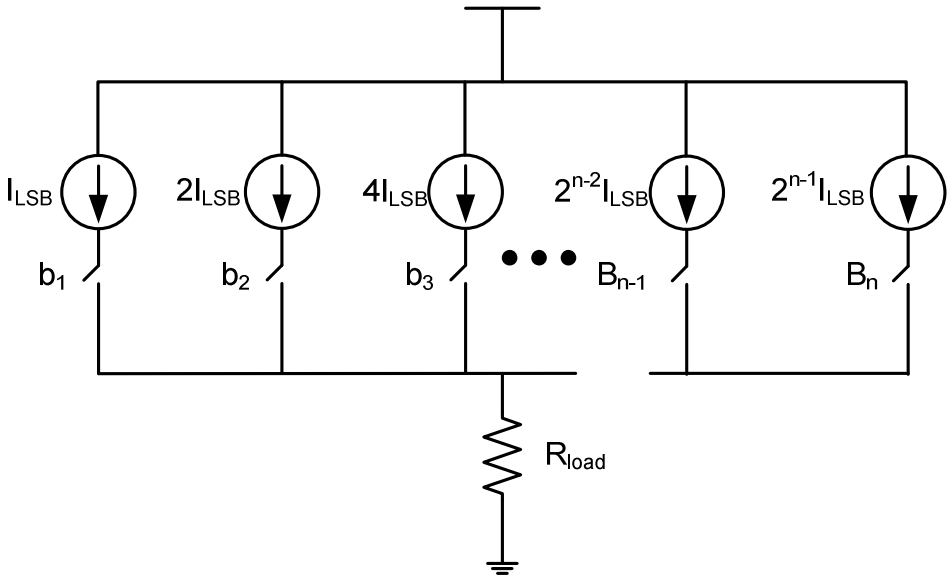


Figure 3.16 A Binary-weighted Current Steering DAC.

each current source of the array, we obtain different architectures as briefly discussed below.

3.5.1 Binary weighted Architectures

As no decoding logic is required, a binary-weighted DAC as shown Fig. 3.16 has higher conversion speed, offers simplicity in routing and has low power consumption. However, this structure has major drawbacks on both static and dynamic performance. These drawbacks are all associated with major transitions of the DAC. The severity of the problem is proportional to the weight of the bit. The worst case occurs at the middle-code transition when the MSB current source of the binary-weighted array is being turned on and all the other current sources are being turned off. Therefore, this architecture is not guaranteed to be monotonic and may result in large differential nonlinearity (DNL) error.

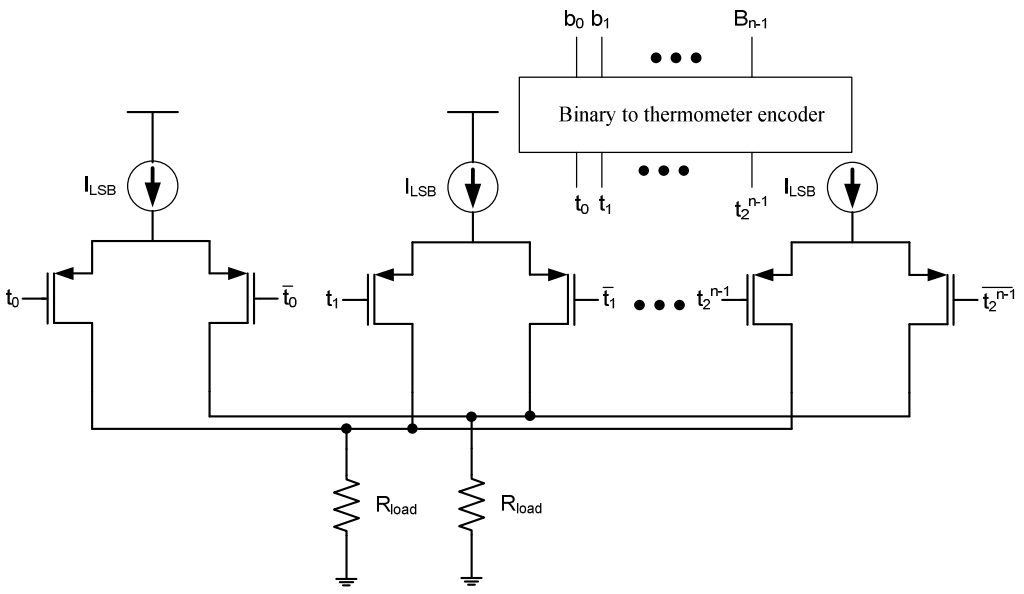


Figure 3.17 Thermometer coded Current Steering DAC.

3.5.2 Thermometer-coded Architectures

In thermometer decoding, a digital decoder is required to convert the binary input values to a thermometer-coded equivalent in Fig. 3.17. In thermometer coding, an additional output on the decoder is selected for every increase in the binary input code. Therefore, advantages of thermometer-code based architectures are that they offer guaranteed monotonic outputs, low DNL errors and reduced glitch noise. The major drawback of thermometer-code based architecture is that it requires a decoder which draws extra power and takes additional area to implement. To represent 2^n different digital values, the thermometer code requires 2^{n-1} levels. Therefore, for higher n values, the decoding logic can introduce large decoding delay and could take a lot of real

estate on silicon. Also, for high speed DAC design, the decoder design is not trivial.

3.5.3 Segmented Architectures

The widely used segmented DACs utilize the advantages of binary-weighted and thermometer-coded architectures. Generally, a certain number of most significant bits are implemented in thermometer-coded architecture and the rest of the least significant bits are realized in binary-weighted fashion. This, in addition to using binary-weighted architecture in places where the overall DNL is least affected, allows the low DNL of thermometer-coded architecture to be exploited in order to achieve better overall DNL performance while reducing the decoder logic. Using this concept, segmented current steering DAC is applied to produce the constant current for the conductometric sensor arrays.

Thermometer-coded-architectures of current-steering DACs have guaranteed monotonicity. Also, the matching requirement is significantly less, as 50% matching of the unit current source results in a DNL of under 0.5 LSB. Also, glitches do not contribute to non-linearity in thermometer-coded case because the size of the glitch in thermometer-coded DACs is proportional to the number of switches that switch at a given sample time. However, the major drawback of thermometer-coded architecture is that as the number of bits increases, the area increases significantly. On the other hand, in binary architecture, the output can change by substantially more than 1 LSB, causing a potentially substantial glitch created by the MSB source varying in one direction and the LSB sources varying

in another direction during mid-code transitions. Also, the severity of the matching problem is determined by the weight of the bit. Therefore, the matching of the MSB current source transistor must be extremely accurate. Still, for high bit resolution, binary architecture requires significantly less area than thermometer architecture. In this way, there are many trade-offs between thermometer-coded and binary weighted architectures. In this work, segmented current steering DAC is selected because less glitch power and less area are required instead of both binary weighted DAC and thermometer-coded DAC.

In this thesis, an optimum segmentation current steering DAC is designed by combining using both the binary weighted and thermometer-coded types in order to have the minimum area requirement and maintain INL < 1.0 LSB, and DNL < 0.5 LSB. Also, the thermometer-coded bits are split into two groups to reduce area requirement in Fig. 3.18. In this design, the current source dimensions are designed taking all these process mismatches into consideration. A major problem associated with current steering architecture is that if the current required is large, the dimension of switches A and B in Fig 3.18 becomes so large that a glitch of significant height occurs. Charge feed through of the switches is the one of caution of glitches. To reduce the glitch power, each switch circuit is modified with dummy switches as presented by cascade type switches. It will be discussed in chapter 5.

Based on the architecture above, the advantage of sourcing current to the conductometric sensor is that the current can be controlled directly and can improve dynamic range in analog front-end circuitry. The current through the

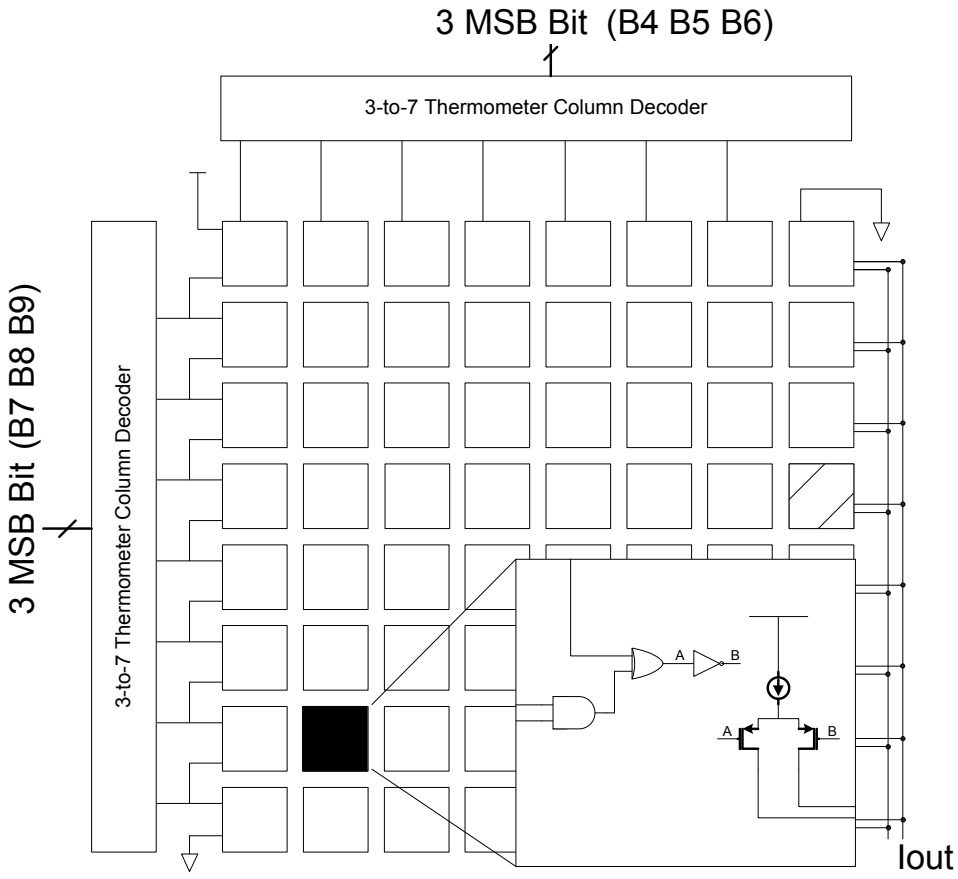


Figure 3.18 A Current Steering DAC with Thermometer-coded with for more matching.

current steering DAC can be limited to less than 60 μA because of the maximum current derived in conductometric sensor array. The allowable maximum current from the DAC is 51.1 μA. The specification and implementation of this DAC will be presented later.

3.6 LOW VOLTAGE SWITCHED CAPACITOR CIRCUITS

Low voltage switched capacitor circuits are considered a specific class of circuits often employed in analog signal processing as switched capacitor [61].

Switched capacitor circuits find widespread use because of their robustness, inherent linearity and implementation efficiency. For example, the cutoff frequencies of switched capacitor filters depend on the capacitor ratio instead of RC time constants as in continuous time filters. In monolithic circuits, capacitor ratios are easier to control and implement than RC time constants. As the name suggests, an important element in this case of circuits is the switch. In a low voltage environment, the switch implemented with a NMOS or PMOS suffers from a low overdrive voltage. Low overdrive voltage equates to low conductance as seen in the follow equations for channel conductance of a CMOS switch.

$$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_n \left(V_{dd} - V_{in} - V_{thn}\right) \tag{3.23}$$

$$g_p = \mu_p C_{ox}\left(\frac{W}{L}\right)_p \left(V_{in} - \left|V_{thp}\right|\right) \tag{3.24}$$

$$g_m = g_{mn} + g_{mp}$$

$$= \begin{Bmatrix} g_m & V_{in} < \left|V_{tp}\right| \\ g_m + g_p & \left|V_{tp}\right| \le Vin \le V_{dd} - V_{tn} \\ g_p & V_{dd} - V_{tn} < V_{in} \end{Bmatrix} \tag{3.25}$$

As is apparent from (3.25), if V_{dd} is less than the sum of the threshold voltages (V_{tn} + V_{tp}), a region exists in which the switch does not conduct. Fig. 3.19 graphically depicts the relationship between the operating regions. Even when the supply voltage becomes comparable to the sum of the threshold voltages, the switch conductance varies greatly over the input range, leading to excessive harmonic distortion. Settling requirements demand that the switch resistance be less than a certain value. A widely varying resistance over the signal

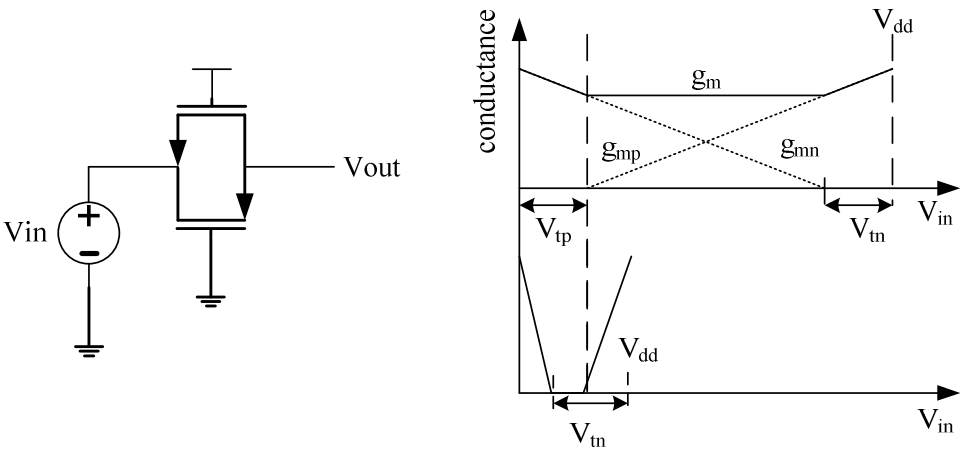


Figure 3.19 Conductance of CMOS switch operation with respect to supply voltage.

range would also lead to an inefficient design in terms of area.

The following recent designs employ several techniques to overcome the low voltage switch conductance problem described above: low threshold transistor option, supply or clock voltage multiplication, gate-voltage bootstrapping and switched operational amplifier. Fig. 3.19 suggests that reducing the threshold voltage will extend the region of conductance for the CMOS switch. A reported ΣΔ D/A converter operates down to a supply voltage of 1.5 V by employing 0.3V threshold transistor [39]. However, the low threshold voltage of the transistor increases processing cost and reduces circuit robustness due to greater leakage currents. As a result, bootstrapping techniques have been developed to remove the need for lower threshold voltages. Although increasing the transistor length in a deep submicron process reduces the threshold voltage,

the switch conductance is proportional to W/L. Increasing W to compensate for longer channels would increase switch capacitance, thereby increasing clock feed through and charge injection. Therefore, the dependence of charge injection according to the input level trades the switch width and the sampling capacitor in switched capacitance. In this work, one of the methods of cancelling the effect of charge injection is chopper stabilization technique as explained in chapter 2.

CHAPTER 4

ARCHITECTURE OF ANALOG FRONT-END CIRCUITRY FOR CONDUCTOMETRIC AND AMPEROMETRIC SENSORS

A desirable system should be as small as a badge and battery operated, similar to radiation counters. To satisfy the size, low noise and low power consumption requirements, an integrated readout interface circuit, data collection and a signal processing module are required. The complete system diagram is illustrated in Fig. 4.1. In the conductometric sensor case, a large variation of resistance from the single-wall carbon nanotube (SWNT) base resistance and the minimum resolvable resistance change depending on gas concentration translate into a wide dynamic range specification for the CMOS analog front-end (AFE) interface circuitry. Also, the current change in amperometric sensor depends on gas concentration and will translate into a wide range specification for AFE

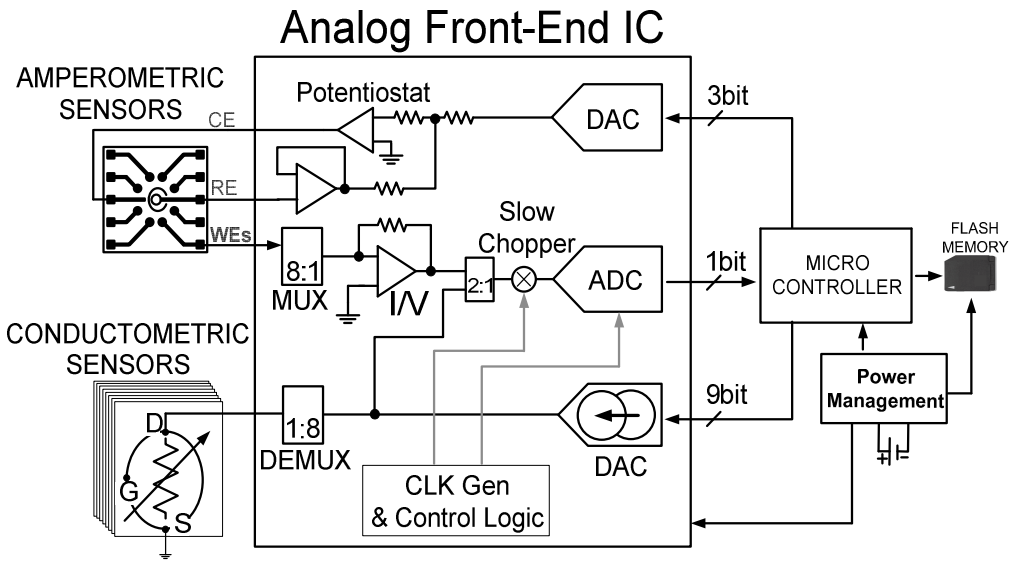


Figure 4.1 Block diagram of exhaust gas detection microelectronics.

interface circuitry. The AFE combines both conductometric and amperometric sensor channels along with the shared ADC to reduce a physical system size.

The conductometric and amperometric sensors are characterized to define an adequate specification for the CMOS, analog front-end interface. In this chapter, both conductometric sensor and amperometric characteristics will be analyzed to formally define an adequate specification for the CMOS interface. Also, the flow of the following block diagram will be explained.

4.1 CONDUCTOMETRIC SENSOR INTERFACE SPECIFICATIONS

From the conductometric sensor characteristics, a number of specifications for the interface circuitry can be determined. When exposed to a reasonable concentration of chemicals as 100 particles per million (ppm), the minimum resistance change in conductometric sensor is roughly 1% from the base resistance [4]. By being able to resolve a 1% change in conductance, the effective chemical concentration can be inferred to resolve a 1% change in conductance, and the effective chemical concentration can be inferred from the conductometric conductance or resistance measurements. If the base resistance in conductometric sensor arrays and its own resistance of sensors do not vary much from channel to channel, the minimum resolution requirement on the interface would be about to 7 bits. However, due to poor fabrication steps or poor environmental conditions when building the conductometric sensors, the base resistance actually varies from 10 kΩ to 10 MΩ.

To determine the effective dynamic range in analog front-end (AFE) circuitry for conductometric sensor arrays, the smallest resistance change that needs to be resolved from base resistance variation is to be considered. The smallest change could be 100 Ω when a 10 kΩ base resistance reacts with the gas chemicals. In fact, the dynamic range requirement in AFE circuitry translates into 17 bits because of 1% change detection and base resistance variation. Thus, when 100 Ω is considered as the LSB of the sensor resistance output, 10 MΩ will become 10^5 times greater than 100 Ω. It is interesting to notice that while the dynamic range requirement is 17 bits, the resolution requirement is only seven bits per 1% resistance change at each base resistance channel because the minimum resistance change in the conductometric sensor by electrochemical reaction is around 1%.

The sensitivity and the maximum drive current characteristics can be different for each channel in a similar mode because a conductometric sensor exhibits a statistical variation in its characteristics such as base resistance. From averaging theory with large numbers, by increasing the number of sensor channels, the reliability of the sensor system may be enhanced. Thus, the AFE interface IC that accommodates an array of the sensor should be developed with dynamic range and accuracy. The ability to accommodate sensor arrays should not come at a large overhead on the interface side. The reusable functionality of the AFE may apply to many sensors such as fuel cell, temperature, pH sensor or pressure sensors. Therefore, the interface is designed to time-multiplex the existing AFE resources. This may increase the readout rate requirement on the interface, but

such an increase in the readout rate is tolerable since the reaction rate for each sensor is very slow [5].

Another restriction on the interface circuitry of the conductometric sensor is the maximum current through the sensor channels. The single wall carbon nanotube (SWNT) as represented by the conductometric sensor can withstand up to 60 - 70 μA of current [40]. In the case of double wall carbon nanotubes, the current-carrying capacity is above 70 μA. The single wall tube normally breaks or loses its characteristics over 60 μA. Since the entire conductometric sensor arrays will be composed of a SWNT, the maximum current supplied to each sensor cell is constrained to be less than 60 μA.

Based on these requirements for the conductometric sensors, the limited noise allocated to a sensor system should be taken into account when designing the interface. The noise analysis will be discussed later. These specifications are summarized below in Table 4.1 below.

Table 4.1 Required Specifications for the Interface Circuitry for conductometric sensor

Resolution	17 bits for detection < 1% change
Dynamic Range	10kΩ ~ 10MΩ
Readout Rate	< 16 sec / channel
Maximum Current	< 70 μA / sensor
Number of Sensors on a System	More than 8 sensors

4.2 SPECIFICATIONS FOR AMPEROMETRIC SENSOR

In constructing a system for an electrochemical gas sensor arrays, the composition of the system is determined by the physical and electrical requirements associated with the corresponding gas interfaces that continuously monitors the physical and electrical activity. Several gas classes are good candidates for miniaturized electrochemical sensors. A key challenge in gas detector sensor development is assembling interfaces that simultaneously immobilize the gases on the electrodes during chemical reaction and allow the gas activity to be measured. A variety of electrochemical methods can be utilized to monitor hazardous activity including voltammetry and impedance spectroscopy. For amperometric sensor array, several voltammetry techniques can be used which require a transducer system composed of a reference electrode (RE), a counter electrode (CE), and an array of working electrodes (WE). To complete the electrochemical measurement system, the instrumentation electronics should incorporate amperometric readout circuit, electrode bias and control circuits.

While applying constant voltage between the RE and the WE reduction-oxidation reactions occur in the sensor cell and the Faradic I_f current generated by the sensor can be estimated by

$$I_f = AnF\Gamma T \tag{4.1}$$

where A is the electrode area, n is the number of electrons involved in the reaction, F is Faraday's constant, Γ is the surface coverage density of the gas, and T is the turnover rate [41]. To support micrometer-sized, off-chip electrodes relative to gasoline and diesel gases, the University of San Diego performed wet bench

Table 4.2 Required Specifications for the Interface Circuitry with amperometric sensor

Resolution	10 bits
Current Range	10 nA~ 100 μA
Readout Rate	< 16 sec / channel
Maximum Current	< 100 μA / sensor
Number of Sensors on a System	More than 8 sensors

testing and determined that the maximum current could reach from 10 nA to 100 μA depending on gas concentration and types. Thus, the readout circuit must support a wide input current range from 10 nA to 100 μA. It is typically difficult to precisely control the density and types of gas concentrations on each electrode; thus, calibration would be needed for individual electrodes. These specifications are summarized in Table 4.2.

A typical amperometric sensor configuration consists of three electrodes consisting of a CE, RE, and a WE. The target in this AFE design is to be able to detect chemical sensing signals using either amperometric sensors as planar electrodes or platinum microelectrodes. These amperometric sensor structures can detect quanta release of oxidization transmitters, such as the catecholamines, epinephrine and norepinephrine [42], using a carbon fiber or a platinum microelectrode that is positioned close to the cell surface and held at a potential that is sufficiently high enough to oxidize the released molecules. Upon release from a vesicle, the catecholamine molecules that diffuse to the surface of the electrode are rapidly oxidized, resulting in the transfer of two electrons to the

electrode [43]. To detect the different gas types by chemical reaction, the voltage levels for the power signals can be as low as 1V to make stimulus for only oxidation and the bandwidth no more than 1 kHz for 8 channels or more.

One of the problems with using low frequency signals from both a conductometric sensor and an amperometric sensor is that low frequency noise can interfere with the sensor signals in the overall system. The flicker noise and the DC offset of the CMOS amplifiers can be a problem since their effects increase with the decrease in frequency. In amperometric sensor system, potentiostat and current-to-voltage converters are usually used in CMOS amplifier designs for their proper operation. Furthermore, in the case of using planar or impaled electrodes, the output impedance is roughly higher than 2 kΩ. Thus, the output impedance of the AFE device is a significant factor in determining the specification of the sensor output impedance. The current to voltage converter should have a high input impedance to transfer most of the sensor signal. This is usually not hard to achieve because at low frequencies the input impedance of a CMOS-based amplifier is generally high.

The goal of AFE system for both types of sensors is to operate at low noise, low offset, and low power in a portable unit. The AFE circuitry could deliver an overall offset suppression up to 500 μV because all sensor signals work at very low frequencies and DC. In this chapter, a low-noise and high-resolvable architecture for both sensors that is based on the sensors' specifications and that accommodates both wide dynamic range and low noise will be proposed. The

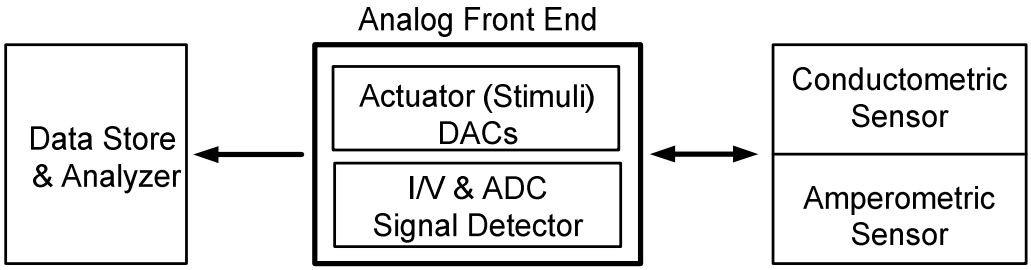


Figure 4.2 General concept of a sensor interface circuitry.

following section discusses the proposed architecture to achieve the specifications of the AFE mentioned above.

4.3 PROPOSED ARCHITECTURE

The primary function of sensor interface circuitry is to read and amplify transducer output signals. Generally, most sensor interface circuitry should have an actuator or stimuli to excite the sensor to be reacted, a signal detector to detect the signal from sensors after a chemical reaction, and a data analyzer to analyze and store the signal in the detector. A block diagram including all the components is shown in Fig. 4.2. In fact, the interface introduced actuates the sensor with a voltage source, then converts and measures the voltage signal at amperometric sensor output node. On the other hand, the same interface actuates with predetermined current sources into the conductometric sensor and measures the voltage signal at the sensor output node. In fact, in the interface design, it had been tried to actuate directly with a variable current sources and constant voltage, and then measure the voltage from the both sensors.

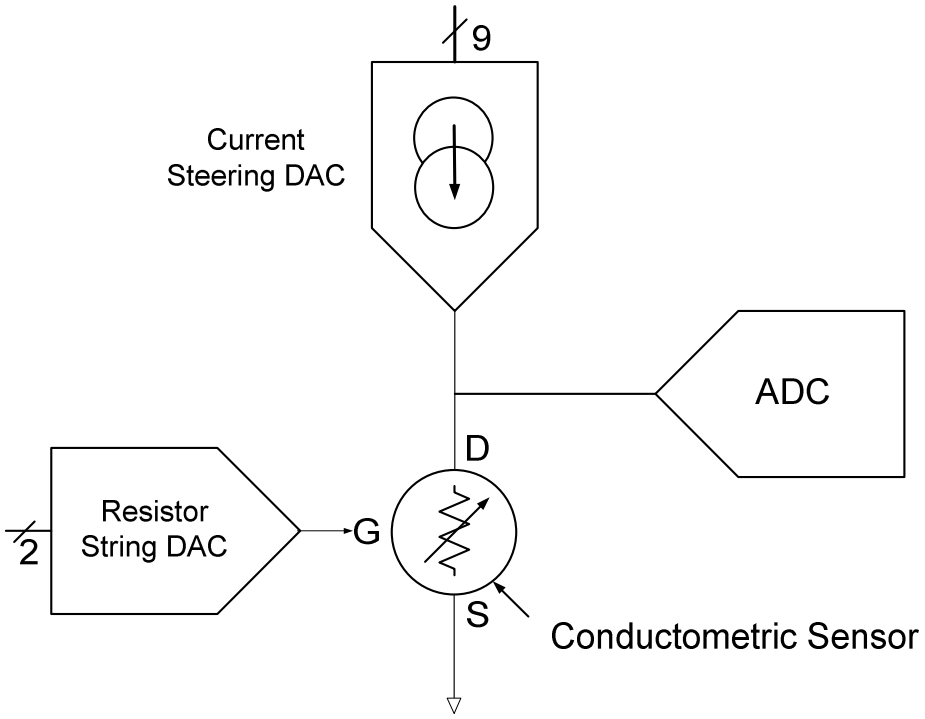


Figure 4.3 Analog front-end circuit for a conductometric sensor.

4.3.1 Sensor Analog Front-End Circuit for a Conductometric Sensor

The main idea for the proposed architecture is that the interface can trigger the sensor with a current source and measure the voltage to detect the resistance change of the sensors, as shown in Fig. 4.3. From this idea, the requirement for an amplifier to generate a virtual ground as well as the need for an amplifier to generate a stimulus across the sensor can be eliminated. This idea satisfies the requirement of having a 17-bit dynamic range with analog blocks smaller than the current dynamic range shown in Table 4.3. This idea can provide a coarse absolute resolution in the high-resistance range and a fine absolute resolution in the low resistance range. Since the resistance change in the conductometric sensor is proportional to sensor voltage and inversely proportional to the current being

Table 4.3 Current Specifications for conductometric sensor

Contents	Value	Unit		Value	Unit	Rsensor range
1% change of 10kohm	100	ohm				**10kΩ~24 kΩ**
Start resistance 100ohm stage1	**50**µ	A		**50**µ	A	
maxdetection R with this current	24k	ohm				
1% change of 24kohm	240	ohm				**24kΩ~57.6kΩ**
with resistance 24kohm stage2	**20.8**µ	A		**20.8**µ	A	
max detetion R with this current	57.6k	ohm				
1% change of 57.6kohm	576	ohm				**56.7kΩ~138 kΩ**
with resistance 24kohm stage3	**8.68**µ	A		**8.6**µ	A	
max detetion R with this current	138k	ohm				
1% change of 138kohm	1.38k	ohm				**138kΩ~332 kΩ**
with resistance 24kohm stage4	**3.62**µ	A		**3.6**µ	A	
max detetion R with this current	332k	ohm				
1% change of 332kohm	3.32k	ohm				**332kΩ~796 kΩ**
with resistance 24kohm stage5	**1.51**µ	A		**1.5**µ	A	
max detetion R with this current	796k	ohm				
1% change of 796kohm	7.96k	ohm				**796kΩ~1.91 MΩ**
with resistance 24kohm stage6	**628**n	A		**600n**	A	
max detetion R with this current	1.91M	ohm				
1% change of 1.91Mohm	19.1k	ohm				**1.91MΩ~ 4.59 MΩ**
with resistance 24kohm stage7	**262**n	A		**300n**	A	
max detetion R with this current	4.59M	ohm				
1% change of 4.59Mohm	45.9k	ohm				**4.59MΩ~ 11 MΩ**
with resistance 24kohm stage8	**109**n	A		**100n**	A	
max detetion R with this current	11M	ohm				

pushed through the current source, the minimum resolvable resistance change may decrease as the current is increased. However, the current through the sensor cannot be increased in order to keep the output voltage below the supply. There is a maximum current that can be supplied to a minimum detectable resistance of

conductometric sensor array. In fact, the maximum value is small for large resistors and large for small resistors, which results in the varying absolute resolution feature described.

In general, a sensor input voltage/current span seldom equals the DAC/actuator interface or the output voltage/current span. The DAC output voltage span must match the actuator input voltage span to achieve maximum performance. The procedure for matching the DAC output span to the actuator input span can be quite different from the procedure for matching the sensor output span to the ADC input span. Sensor outputs are usually low-level signals, thus care must be taken to preserve their signal-to-noise ratio. Actuator input signals may require significant power, thus robust op-amps are required to drive some actuators. To resolve these problems in actuator/DAC, the idea of using a current steering DAC can provide a solution.

The interface should be designed such that the 7-bit resolution is required to detect a 1% change in resistance. This requirement should be met across the whole dynamic range. In effect, the current sources should be set to detect the minimum resolvable resistance in the operating range of the interface circuitry. As shown in Fig. 4.3, analog blocks in the interface operate at the supply voltage of 1.8V and the sensor signal processing chain operates at 1V. The current source in this system can be implemented as a current-steering digital-to-analog converter (CSDAC). The input word for the DAC is a digital representation to choose the current sources, and the input is controlled by a microcontroller. The minimum current source cell for 1 LSB in the DAC is 100 nA to detect 10 MΩ or higher

resistance. Furthermore, in this work, the readout system may require 16-bit resolution when 1 LSB current source is applied as well as when an unknown sensor is tested. To digitize the analog sensor signal and store the signal into a flash memory, an ADC is implemented with a 1^{st} order sigma delta modulator, which has a good resolution and moderate speed applications [44]. The analog front-end IC employs 8 conductometric sensor cells. The 3-bit resistor string DAC with a class AB buffer is used to bias the back gate. The output of the DAC can be used to apply a static voltage to the back-gate of the conductometric sensor array, modulating the sensor sensitivity. In this work, current stimuli using current steering DAC is applied to the sensor directly and then the voltage signal at sensor output node is digitized by first order sigma delta ADC.

4.3.2 Sensor Analog Front-End Circuit for an Amperometric Sensor

This section describes the operation of the potentiostat in detail and discusses the sensor interface circuitry for an amperometric sensor. The potentiostat is normally used for amperometric sensors. The analog front-end interface for amperometric sensor contains the integrated control-loop-amplifiers which drive the on-chip counter electrodes and an off-chip reference electrode. This, along with the working electrodes, forms a standard potentiostat that can be used to perform classical electrochemical measurements such as cyclic voltammetry (CV) and electrochemical impedance spectroscopy (EIS) [45]. From Fig. 4.4 it can be seen that a potentiostat is a feedback control system used to apply a desired potential to an electrochemical cell and to measure the movement

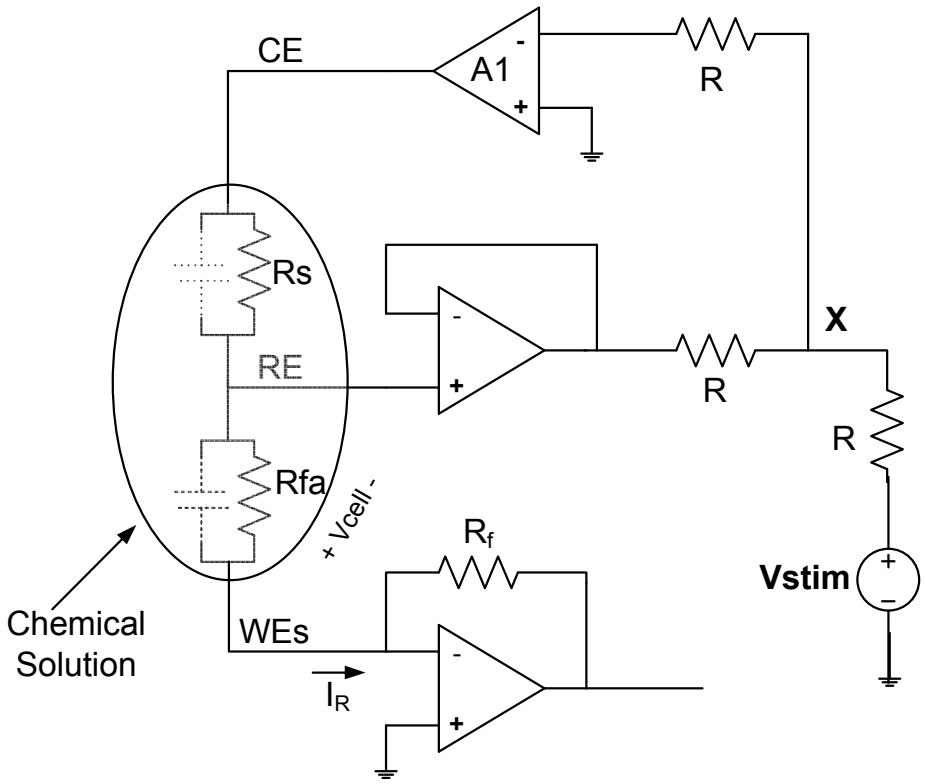


Figure 4.4 Potentiostat operation.

of charge through the sensor cell that accompanies electrochemical reactions occurring at an electro-electrolyte interface. A standard potentiostat is used in a typical electrochemical setup. The potentiostat consists of three electrodes immersed in an electrolyte as gas solution: a working electrode (WE) where the reaction of interest occurs, a reference electrode (RE) to hold the electrolyte at a known potential, and a counter electrode (CE). A primary function of the potentiostat is to ensure that V_{cell} tracks an applied source voltage (V_{stim}) under varying current-loading conditions. The negative feedback around I/V converter op-amp creates a virtual ground at the WE. Thus, assuming an ideal op-amp, V_{CELL} is given by:

$$V_{cell} = V_{WE} - V_{RE} \tag{4.2}$$

When a working electrode noise is considered as a virtual ground, equation (4.2) can be solved by:

$$V_{RE} = \frac{R_{fb}}{R_b + R_{fb}} A_1 (-V_{RE} + V_{stim})$$

$$\frac{V_{RE}}{V_{stim}} = \frac{A_1 R_{fa}}{A_1 R_{fa} + R_s + R_{fa}} \tag{4.3}$$

The RE's potential is buffered by a source follower (unit gain buffer) to ensure that no current is drawn through the RE. The negative feedback around amplifier A_1, which is connected via the amperometric sensor cell, forces node X to ground. The voltage seen at the X node is 1/2 of the sum of V_{stim} and V_{RE}. It follows that X node is only equal to zero (ground) when V_{stim} is equal to $-V_{RE}$ or by (4.2), when V_{stim} is equal to V_{cell}. Thus, the negative feedback of the potentiostat ensures that V_{cell} tracks V_{stim}.

Since WE is held at virtual ground because of feedback, the value of V_{cell} can only be altered by changing the potential at CE. The voltage swing of this architecture V_{cell_SWING}, assuming amplifier A_1 has rail-to-rail output, is defined by the voltage swing at CE.

$$V_{cell\_SWING} = (V_{dd} - V_{ss}) \frac{R_s}{R_s + R_{fa}} \tag{4.4}$$

where V_{dd} is the positive supply voltage and V_{ss} is the negative supply voltage. The rail-to-rail Amplifiers at A_1 and A_2 will be presented and implemented in next chapter.

The potentiostat amplifies the sensor's faradaic current from electrochemical reaction. The current is accomplished with an I/V converter for input at ADC. The sensor's output current flows through the feedback resistor R_f which is referenced to virtual ground to provide an amplified current-to-voltage conversion such that

$$V_{out} = -I_f R_f \tag{4.5}$$

In summary, the potentiostat for the amperometric sensor reaction keeps the voltage from applied voltage and measures the current signal from the sensor by using current to voltage converter as shown in Fig. 4.5. The interface circuit

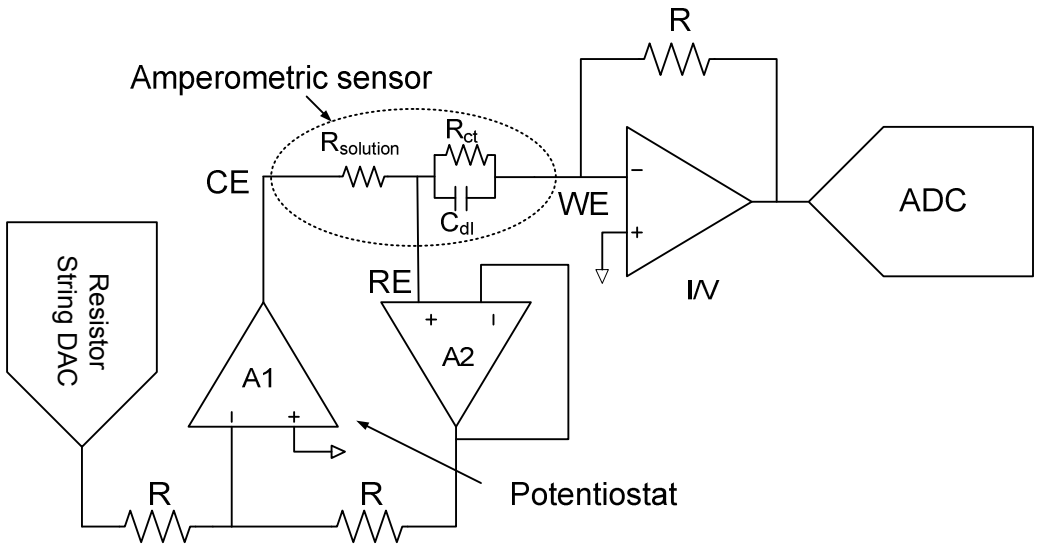
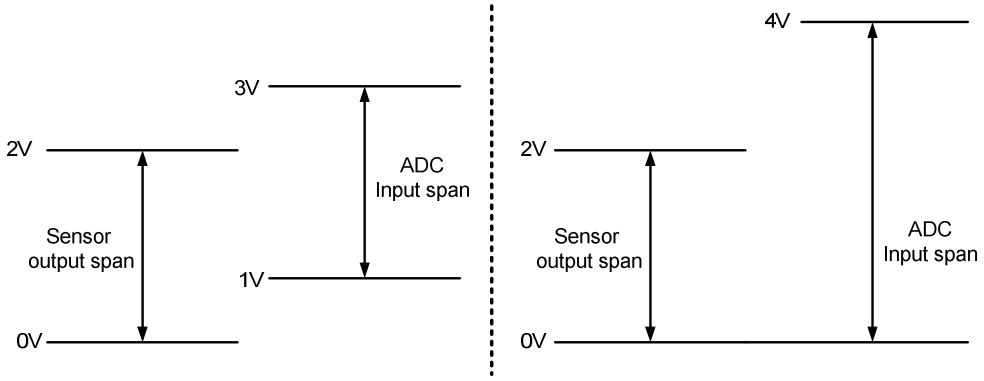


Figure 4.5 Analog front-end circuit for an amperometric sensor.

actuates the sensor with a voltage source from a programmable 3-bit DAC, and then measures the current signal from the sensor to maintain a stable oxidation-reduction reaction in the electrochemical cell. After I/V converter, the faradaic current become voltage at the ADC input. This output voltage will be digitized by the 1st ΣΔ ADC in Fig. 4.5.

4.4. FIRST ORDER SIGMA DELTA (ΣΔ) ADC WITH CHOPPER STABILIZATION

The sensor output voltage span seldom equals the ADC input voltage span. Sensor data is lost and/or ADC dynamic range is not fully utilized because the spans are unequal, start at different DC voltages, or both [11]. In Fig. 4.6(a) the spans are equal but offset. This situation requires level shifting to move the sensor output voltage up by one volt so that the spans match. In Fig. 4.6(b) the spans are unequal, but no offset exists. This situation requires amplification of



(a) same spans (b) different spans

Figure 4.6 Sensor span and ADC span for same and different spans.

the sensor output to match the spans. When the spans are unequal and offset, level shifting and amplification are required to match the spans. The spans should be matched to achieve optimum performance because mismatched spans lose sensor data or require an expensive increase in ADC dynamic range. The amplifier is the best analog circuit available for matching the spans because it level shifts and amplifies the input voltage to make the spans equal. The op-amp is so versatile that it level shifts and amplifies the input signal simultaneously. To achieve optimum performance, all significant signal chain spans are equal with the sensor actuator, the AFE, and the ADC [46].

Depending on an $\Sigma\Delta$ modulator loop, it is possible to build up the noise-shaping filter as a discrete time (DT) or a continuous time (CT) circuit[47]. The DT $\Sigma\Delta$ modulators are implemented using the switched-capacitor (SC) circuit technique. In SC circuits, amplifiers with high gain bandwidth product (GBW) satisfy the settling requirements. Typically, the GBW is seven times higher than the sampling frequency. By nature, CT $\Sigma\Delta$ modulators are not sensitive to settling behavior. As a result, CT $\Sigma\Delta$ modulators can potentially operate at higher clock frequency and/or with less power consumption. In a CT $\Sigma\Delta$ modulator, the loop filter provides additional anti-aliasing filtering, which is beneficial when having to handle large interface. In SC circuits, the in-band noise is bounded by the capacitor size. Consequently, CT modulators have smaller power and consume less silicon area than the DT counterparts. Contrary to a CT modulator, in a DT modulator large glitches appear on the op-amp virtual ground node of the

RC integrators due to switching transient. Therefore, a CT modulator achieves better linearity performance. However, it is well known that the clock jitter of the feedback DAC is critical in the SNR degradation of a CT single-bit feedback DAC. Some solutions should exist to circumvent the jitter effect. For example, going to an N-bit $\Sigma\Delta$ ADC will reduce the quantization step by 2^N-1. Consequently, the DAC charge transfer fluctuation per clock period due to jitter will also decrease by 2^N-1. However, this solution could be chip area consuming.

A more interesting solution consists of implementing the DT modulator as an SC DAC while keeping a continuous-time loop filter. As demonstrated in [49], because of a return-to-zero clock scheme configuration, a settling time constant of the SC DAC would be eight times smaller than the clock period and the jitter sensitivity would decrease by 4 dB. This latter solution is preferred for wireless applications that do not require more than 5 MHz conversion bandwidth because it optimally trades off the CT and DT advantages. In a DT modulator the variation in time constant is determined ratio of the capacitors. This enables excellent matching in the time constant of the noise shaping filter. However, this is not the case in CT modulators where the time constant's variation is between 25% to 30% due to R and C spreads. This variation can seriously degrade the SNR performance. Thus, a DT modulator is selected in this thesis for higher accuracy and better matching.

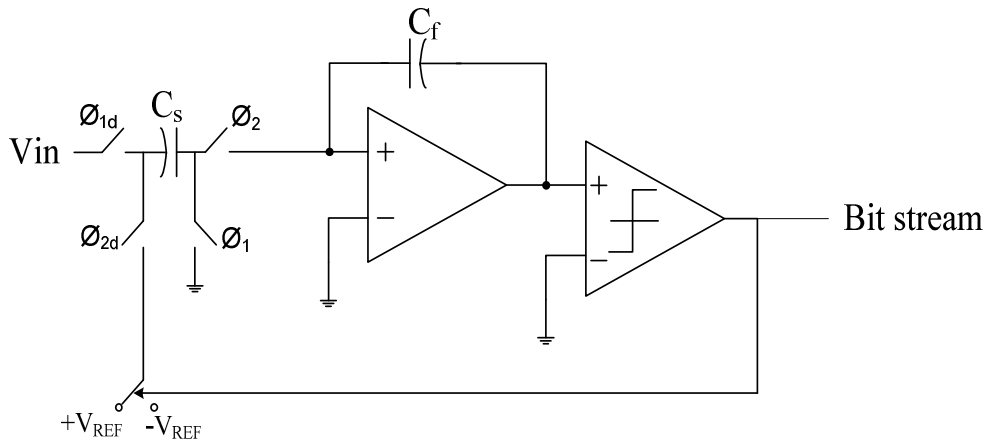


Figure 4.7 Simplified diagram of the first order SD modulator.

The basic block diagram of a first order sigma delta modulator is shown in Fig. 4.7, which consists of an integrator and a comparator, which acts as an ADC and 1-bit DAC, which is placed in the feedback loop. The name first order is derived from the information showing that there is only one integrator in the circuit, placed in the forward path. When the output of the integrator is positive, the comparator feeds back a positive reference signal that is subtracted from the input signal of the integrator.

Similarly, when the integrator output is negative, the comparator feeds back a negative signal that is added to the incoming signal. The integrator therefore accumulates the difference between the input and quantized output signals from the DAC output, which is in feedback loop, and then makes the integrator output around zero. A zero integrator output implies that the difference between the input signal and the quantized output is zero [50].

Low noise, low 1/f noise and reusable ADC is one of the most important blocks for the developed interface system. ADC can perform the function of

signal detector in the interface model introduced in a sensor interface chip diagram. While the conversion rate is not critical, the low dc offset noise and 1/f noise from AFE affect the sensor signal chain at low frequency. As introduced in chapter 2, the nested sigma delta scheme was chosen in this requirement because the nested chopper scheme is one of the most efficient noise suppression techniques for the CMOS amplifier and the mixed signal chain.

The $\Sigma\Delta$ ADC with chopper stabilization technique is applied to digitize the electrochemical measured voltages which is obtained from the amperometric sensor and the conductometric sensor. The complete signal flow diagram for the ADC with cascaded integrate comb (CIC) filters are shown in Figure 4.8(a). The outputs of both amperometric sensors and conductometric sensors are applied to the ADC. Two nested choppers modulate the output signal from the sensor. One is a low frequency and the other one has a high frequency inner side of the ADC. Figure 4.8(b) and Figure 4.8(c) show the frequency spectrum for nodes W, X, Y, and Z in Figure 4.8(a).

The slow chopper is applied to decrease the mismatch related residual offsets in the switched-capacitor (SC) circuit at slow chopper frequency [24], [25]. After the external slow chopper modulates the input signal, the first order ADC digitizes the significant signal at the slow chopper frequency and offset the DC at node W as shown in Figure 4.8(a), which is still within the flat-band of the quantization noise for the ADC as shown in Figure 4.8(b). Inner fast chopper pair removes *1/f* noise and the DC offset of the ADC integrator.

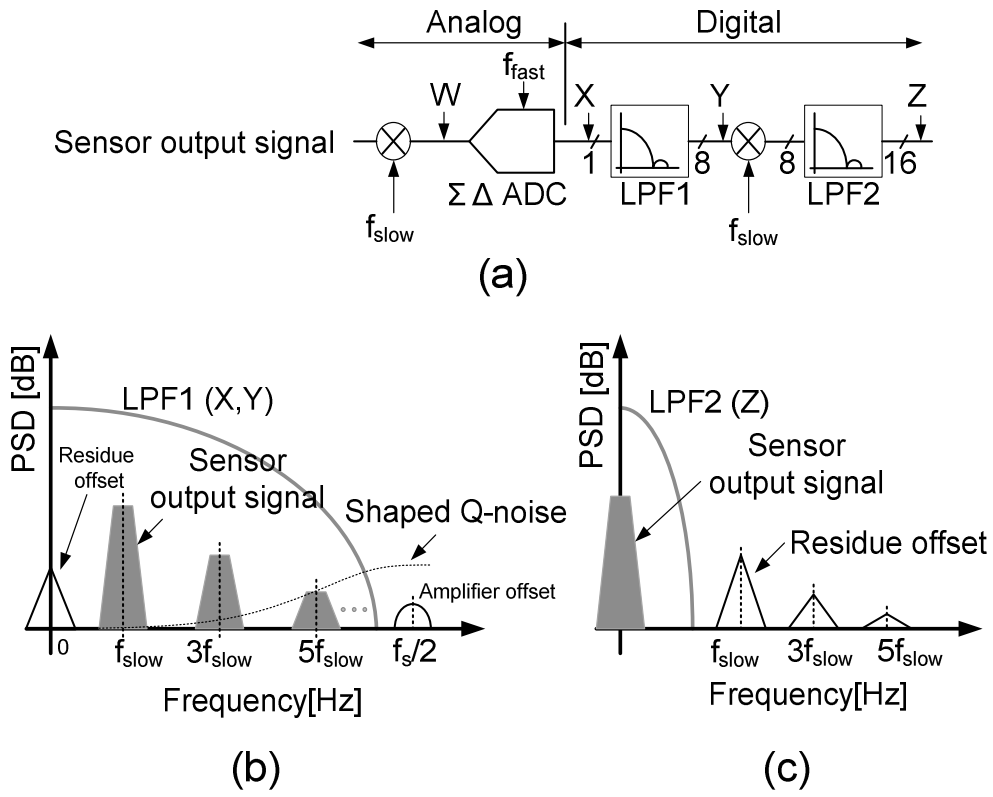


Figure 4.8 The complete signal flow diagram and frequency spectrum for ΣΔ ADC with decimation filters.

In addition to this, the ADC architecture in Fig 4.8 relates to chopper circuitry for reducing residual noise caused by a mismatch between the input chopper switches and the switched capacitor modulator. The performance of the delta sigma modulator is sensitive to input noise, which is caused by switches, operational amplifiers, and digital circuits. Such noise will degrade the dynamic range of the input signal. In the low frequency band, the increase in flicker noise is proportion to the decrease in frequency. In the relative-low frequency band, the offset will dominate the noise. In sensor interface circuits, system performance is limited. As mentioned in the previous chapter, correlated double sampling, self-

calibrating operational amplifiers, and chopper stabilization techniques are used to deal with this type of noise. The chopper stabilized delta sigma modulator with conventional op-amps has been shown to have better immunity from low frequency noise [51], [53]. Unfortunately, the chopping approach also generated residual noise, which switches during the operation of the chopper as well as the 1-bit feedback DAC switch. The ON and OFF of the switch induce the spikes into the input end of the delta sigma modulator. These high frequency switching noises will track the input signal and get injected into the modulator thereby degrading the resolution and SNDR of the system. To resolve this problem, a nested chopper amplifier is used to reduce the residual noise that was mentioned earlier. However, the front-end of the modulator will suffer from high-frequency noise caused by the mismatch between sampling switches and microcontroller [53], [54].

After the interested signal goes through all the analog components in Fig 4.8, the demodulation of the input signal occurs after the first digital low pass filter in digital area. The cutoff frequency of the first set of CIC filter should be higher than the chopper frequency to eliminate the risk of high frequency noise demodulation. In fact, the first filter should pass the odd harmonics of signal at odd chopper frequencies because the signal should be reconstructed with low distortion. After the digital demodulator with slow chopper frequency, the signal at the slow chopper frequency is down-converted in the original signal band by the chopper switches in the module. Finally, the low frequency drift at slow

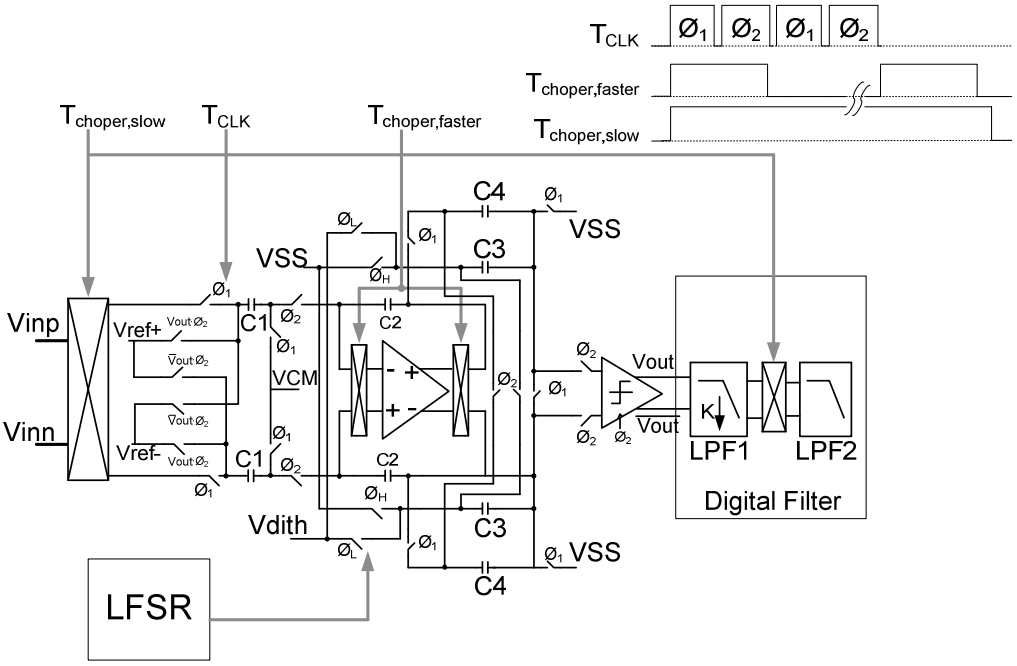


Figure 4.9 Proposed the first order ΣΔ ADC with chopper switches and dither circuit.

chopper frequency is eliminated by the second digital low-pass filter as shown in Fig. 4.8(c).

Based on the signal chain in ADC block diagram, the present proposed architecture for SC $\Sigma\Delta$ ADC is shown in Fig. 4.9. The proposed ADC consists of an OTA, a comparator, chopper switches, a digital filter, and dither circuitry with a linear feedback shift register (LFSR).

The micro instrument integrates a shared 1st order $\Sigma\Delta$ ADC to reduce chip size and power consumption. The single slope ADC is more susceptible to substrate noise [53]. Because of this limitation, the secondary converter could be useful for measuring noise transmission in this mixed-signal environment. The

step voltage for the converter is generated by supplying a fixed current, derived from 3-bit resistor string DAC to an off-chip resistor.

Both sensors are needed to digitize their sensor signal depending on gas concentration to store them into a flash memory because this module will be used to portable gas detection platform.

4.5 EQUVLAENT CIRCUIT MODEL FOR AMPEROMETRIC SENSOR

Before attaching the real amperometric sensor to analog front-end circuitry, an equivalent circuit model needs to be simulated to verify the proper functionality of the proposed module. Figure 4.10 shows an electrical equivalent model for a three electrode chemical sensors including noise source [55], [56].

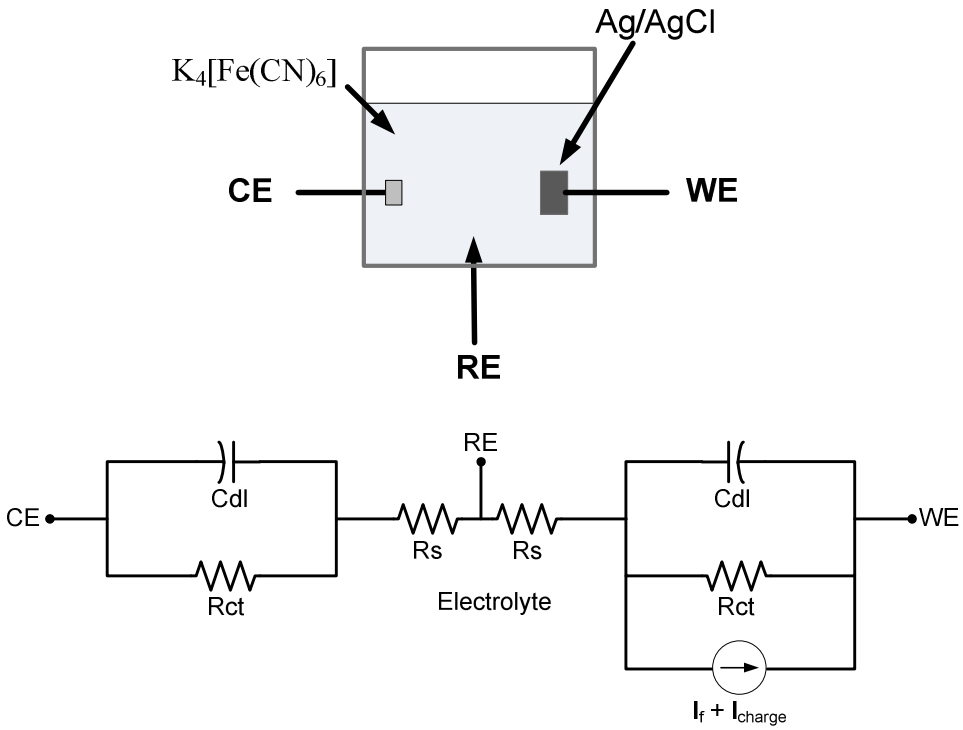


Figure 4.10 An equivalent circuit model for amperometric sensor.

Each of these electrodes introduces parasitic capacitance into the electrochemical cell. These parasitics can be adequately modeled using linear electrical components as shown Fig. 4.10. The double layer capacitance of both CE and WE is represented

by C_{dl} and is given by:

$$C_{dl} = 20 \cdot A\left(\mu F / cm^2\right) \tag{4.6}$$

Rs represent the gas solution resistance between the various electrodes and are given by:

$$R_S = A\frac{d}{k} \tag{4.7}$$

where d is the distance between the two electrodes and k is the gas conductivity. The charge transfer resistance at CE and WE, R_{CT} is given by:

$$R_{CT} = \frac{1}{i_o nF \cdot A} \tag{4.8}$$

where i_o is the equilibrium current density, n is the number of electrons, and F is Faraday's constant [56]. Of the parasitics, C_{dl} is of utmost concern since any current needed to charge/discharge the double layer capacitance is summed with the concentration dependent faradaic current. Large charging currents mask the desired reduction/oxidation (redox) current and lead to poor detection limits. Equations (4.6) to (4.8) demonstrate that the parasitics have dependencies on the areas of the electrodes and their separations. Furthermore, the relationships between the various parasitics and their areas create trade-offs in electrode sizing.

Noise in the electrochemical cell is generated both from the faradaic current,i_{faradaic} and from the parasitics. Similar to any resistor, the solution resistance and charge transfer resistance produce a thermal current noise given by:

$$\overline{i_{thermal,noise}^2} \approx \frac{4kT}{R_s} \tag{4.9}$$

where k is the Boltzmann constant, T is temperature, and R_s is the resistance of gas. Additional noise in the form of shot noise arises from the discrete electron transfer from ions in the solution to electrode and is given by:

$$\overline{i_{thermal,noise}^2} \approx 2q\left(i_{faradaic} + i_{charge}\right) \tag{4.10}$$

where q is the charge of an electron and i_{charge} is the charging current. In the electrical model, these noise sources can be added in parallel with their respective sources. Since the magnitudes of R_s, $i_{faradaic}$ and i_{chage} are dependent on area, electrode dimensions directly affect the total noise generated in the system.

4.6 EQUVLAENT CIRCUIT MODEL FOR CONDUCTOMETRIC SENSOR

Fig. 4.11 shows an equivalent circuit of a carbon nanotube (CNT) as a conductometric sensor trapped between two electrodes. Although only one CNT is depicted in the Fig. 4.8, this circuit is equivalent to all of the conductometric sensor channels connected in parallel in the microelectrode gap [57]. The electrode and gas contact is formed at the both ends of the CNT side. The total resistance of the gas sensor R_T is given by:

$$R_T = R_c + R_s + R_C \tag{4.11}$$

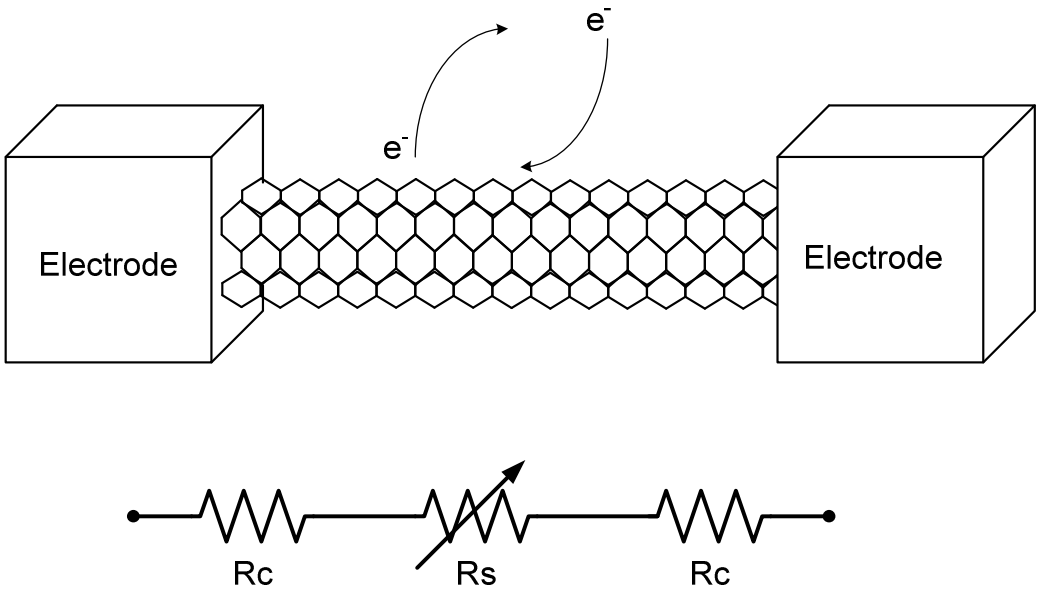


Figure 4.11 An equivalent circuit model for conductometric sensor.

where R_S is solution resistance from the CNT resistance when chemical reaction is activated, and R_C is the charge transfer resistance between the two electrodes and CNT contacts respectively.

As shown in Fig. 4.11, after the gas adsorption (electron), the Schottky barrier and the resistance R_C become higher according to the chemical reaction mechanism. The idea is that the conductometric sensor response can be expressed as a superposition of the Schottky contact resistance (R_C) and the CNT resistance (R_S), which are differently influenced by the gas adsorption and contribute to the overall sensor response. For example, when the sensor is exposed to NO_2 gas, the NO_2 molecules are adsorbed on the CNT surface and attract electrons in the CNT due to high electron affinity. As a result, the positive hole density in the p-type semiconducting CNT increases so that the CNT resistance R_S decreases from the

base resistance value. The resistance exponentially decreases as the number of adsorbed NO_2 molecules increases with elapsed time according to an adsorption scheme such as a Langmuir-model. In fact, *Rs* can be changed by gas concentration.

It is possible that measuring equipment and the environment may contribute to the conductometric sensor output noise. To investigate the noise contributed to the sensor, the same experiment is repeated but the CNT sensors are replaced with a carbon film resistor with similar resistance [57]. The paper has found out that the noise of this carbon film resistor is 0.01 – 0.02% which is an order lower than the CNT noise. Hence, it can be concluded that most of the noise in the CNTs sensor is inherent noise (noise that exists in the CNTs) rather than noise coming from measurement. Theoretically, resistors only have thermal noise. Thermal noise can be formulated by [58]:

$$\overline{V_{thermal,noise}^{2}} = 4kTR_{s}\Delta f \tag{4.12}$$

where Δf is the measuring bandwidth, T is the temperature, and k is the Boltzmann constant.

4.7. SYSTEM SIMULATION

This section discusses the simulation for the first order sigma delta modulator with chopper stabilization. System stability and performance were analyzed and determined using MatLab Simulink simulation. Each block in the architecture was modeled according to the previous discussions. Fig. 4.12 shows the block diagram of the simulation schematic used in Simulink. The advantages

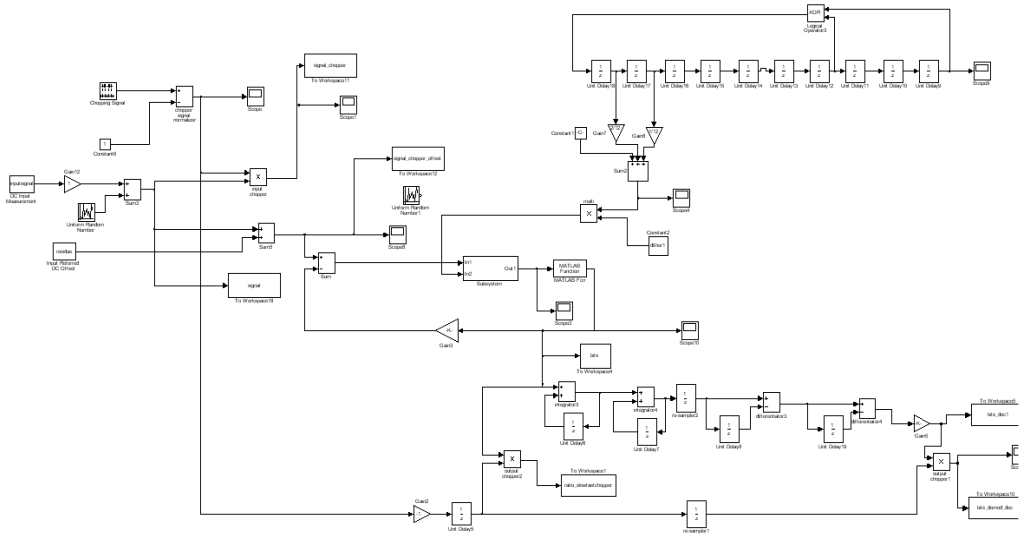


Figure 4.12 MatLab first order sigma delta modulator with chopper stabilization system simulation.

of modeling simulations are speed and ease of use based on the chopper stabilization technique and the 1st order sigma delta ADC. Sensitivity analysis was performed by degrading finite amplifier gain and mismatch in sense capacitance. Other analog non-idealities, such as amplifier thermal noise and *kT/C* noise, were included in the MatLab simulation.

The AFE circuitry performance under non-ideal conditions is presented in Fig. 4.13. The noise is shaped 20dB per decade or by first order shaping due to the interface integrator. This noise shaping would not be present if an amplifier was implemented instead of an integrator. Given one input signal and a sample rate of 262.144 kHz, the simulated Signal-to-Noise Ratio (SNR) is 60.27 dB for a signal bandwidth of 1 kHz. In Fig. 4.13, the SC switch residue offset and the chopper switches offset appear at DC while the sensor signal is at slow chopper

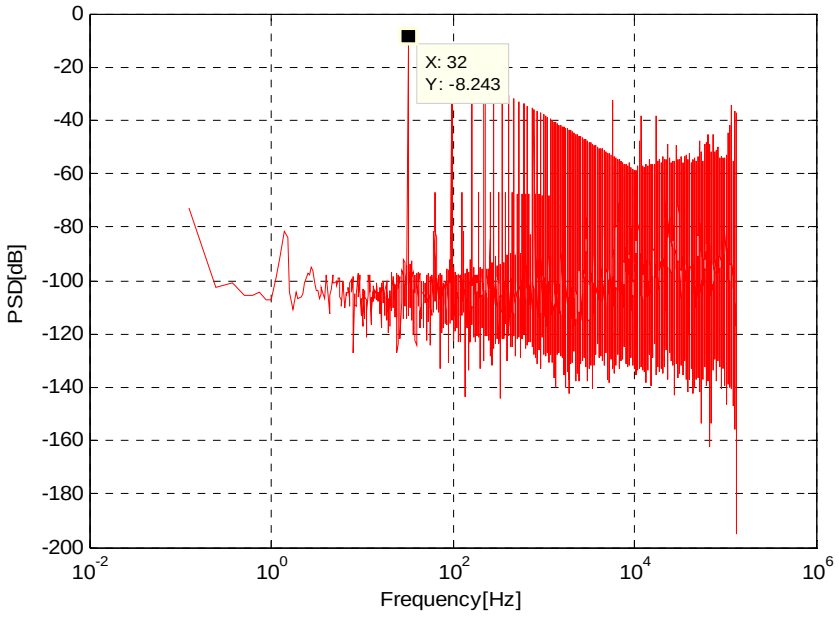


Figure 4.13 AFE circuit system simulation.

frequency. The amplifier DC offset was pushed to high frequency. In this MatLab simulation, 32 Hz frequency is used for the slow chopper frequency and 131 kHz is used for the fast chopper frequency. In the first order modulator, the input signal and the quantizer input are strongly correlated while the output contains strong in-band frequency tones. This is even worse if an additional dc signal is applied.

For DC input signals, the first-order ΣΔ ADC modulator runs in repetitive pattern trying to equal the input level on average. A possible solution to this problem is to include a random noise source at the quantizer input (or at the modulator input) in order to add non-periodic and random signals called dither. In Fig. 4.12, a sequence of delay blocks in simulink presents a linear feedback shift

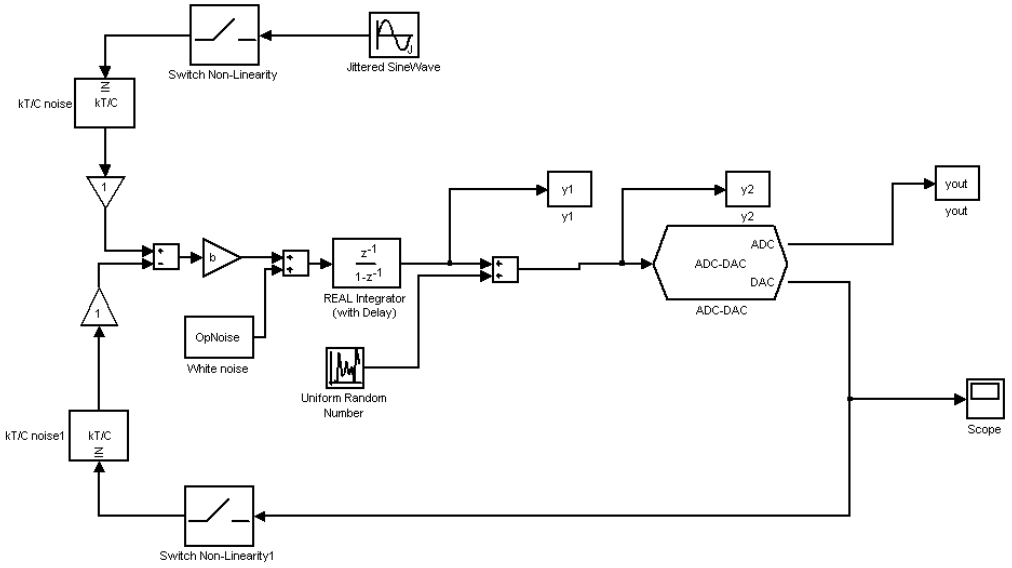


Figure 4.14 Simulink schematic with amplifier thermal noise for ADC.

register (LFSR) and then this LFSR makes uniformly random noise signal to reduce pattern noise.

In Fig. 4.12, the ADC block consists of the lower level Simulink block diagrams with the amplifier thermal noise injected in the summing node of the integrator in Fig 4.14. This Simulink simulation technique was presented by P. Malcovati for modeling amplifier non-idealities [21].

Fig 4.15 shows that the noise floor has increased from an ideal system of -120dB to a system with amplifier thermal noise of -100dB. The thermal noise injected into the system was 1m Vrms. A sampling capacitor C_S of 12.5pF was chosen. The circuit was simulated with the sampling frequency *Fs* equal to 262.144 kHz (a jitter of 1‰ of the clock period) with an oversampling ratio (OSR) of 128.

Fig. 4.15 shows the case where the AFE system is simulated with 1mV residual offset and 5mV signal from the sensors. Fig. 4.15 shows the PSD of input

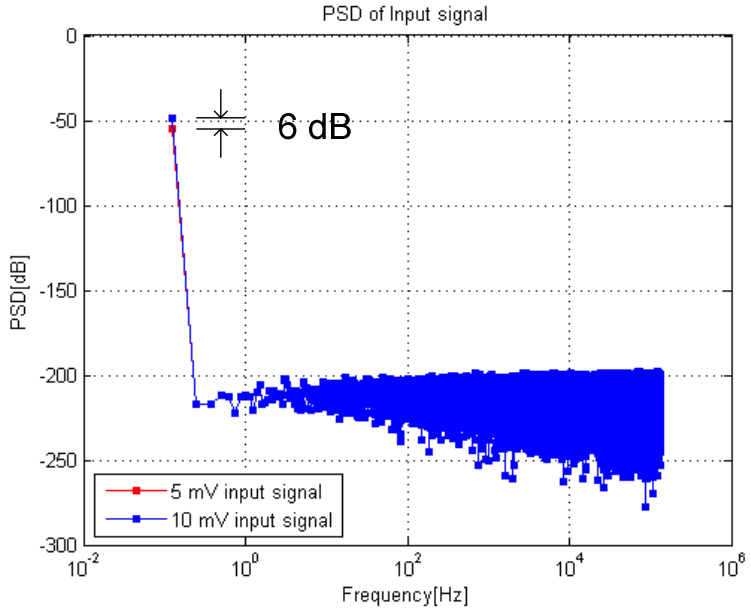


Figure 4.15 Power spectral density of the 5 mV and 10 mV input signals.

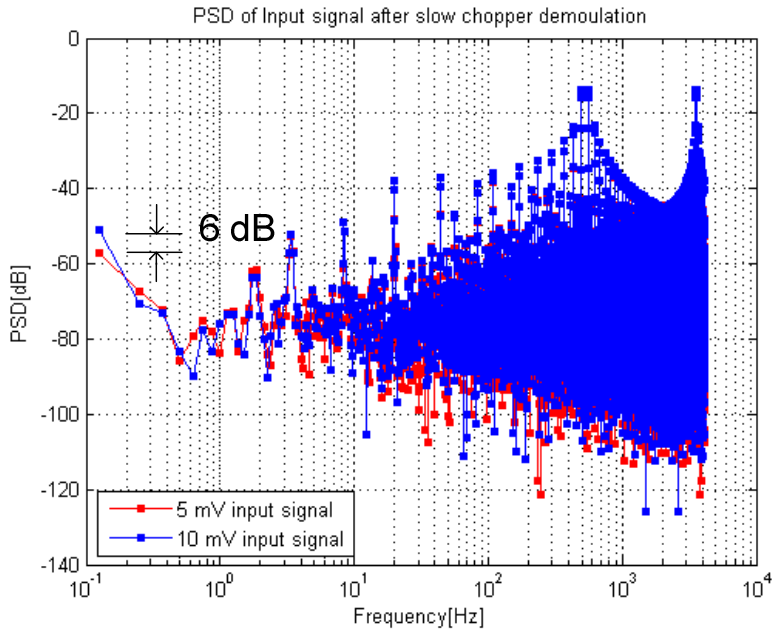


Figure 4.16 Output signals at slow chopper frequency of 32 Hz after the first decimation filter.

signal and Fig. 4.16 shows the PSD of the ADC output after the digital slow chopper demodulation and the first decimation filter. As shown in this simulation, the input signal that comes from the sensors is replicated at the ADC output without any gain error tracking the input signals dB-per-dB at the lowest signal levels.

Chapter 5

IMPLEMETATION CMOS INTERFACE CIRCUITRY FOR GAS SENSORS

An analog front-end (AFE) can provide the interface between a transducer and a digital processing part. AFE contain circuitry for sensor output, which include conversion of the sensor output to more useful electric signals, low-noise delivery and amplification, and data conversion. As presented in Chapter 4, the AFE presents practical implementations of the gas detection system in this chapter. The potentiostat consists of operational amplifiers and resistors which, through feedback, regulate the voltage across the reference and working electrodes independent of the current through the chemical cell. To achieve high swing, these operational amplifiers should have rail-to-rail outputs and the operational amplifiers should drive the large double-layer capacitor of the CE and WE. Based on these requirements, the operational amplifiers were implemented using the architecture with rail-to-rail input, folded cascade, and class AB output stages.

In Section 5.1, the implemented rail-to-rail operational amplifier will be presented for a potentiostat and buffer. In Section 5.2, a resistor string DAC with class a AB buffer will be implemented. In Section 5.3 the current steering DAC with a segmented current source cell will be introduced and its performance will be characterized. In Section 5.4, the on-resistance of the analog multiplexer and chopper switches should be minimized to get a good linearity for the sensor signal channel in the developed sensor array interface. In section 5.5, a scheme of a nested chopper ADC will be discussed and the performance will be characterized.

5.1 RAIL-TO-RAIL OPERATIONAL AMPLIFIER WITH 0.18 μm PROCESS

This section describes the first of two low-voltage rail-to-rail operational amplifiers for a potentiostat, a buffer and a current-to-voltage converter. The primary objective of this design was the development of a standalone rail-to-rail CMOS operational amplifier or op-amp. Standalone refers to a circuit that is packaged separately to be used as a discrete component in a larger system. Such general purpose circuitry requires specifications depending on managing driving and loading conditions.

5.1.1 Target Specifications

Table 5.1 lists the target specifications for the 1.8V operational amplifiers. For similar reasons mentioned in the previous chapter for rail-to-rail input, a rail-to-rail output voltage range increases the dynamic range for a potentiostat and a DAC buffer.

5.1.2 Design Methodology

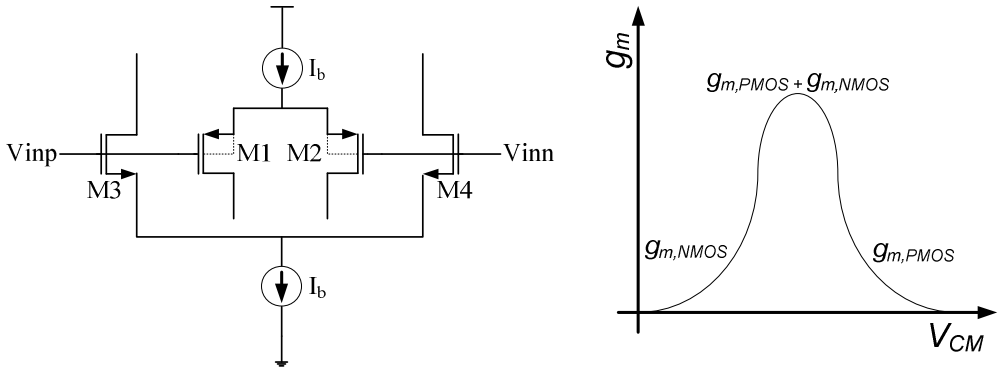
The research has developed and continues to develop rail-to-rail op-amps which are intended to be used in an integrated application where the driving and loading conditions are known. The op-amp design discussed herein is a modification of one of the topologies [60].

In the op-amp design, input referred noise e_n and I_{dc} are assumed to be the most challenging to meet in Table 5.1. Therefore, the design process focused on transistor sizing and rationing to reduce noise and control all static current paths.

Transistor sizes in the input stage are determined by minimizing the input-referred voltage noise. The output stage has little effect on input noise, but requires most of the supply current budget to guarantee stable operation; a class AB output stage minimizes bias current while providing relatively large current drive.

Table 5.1 Folded cascade op-amp specification

Symbol	Parameter	Conditions	Value
$\mathbf{V_{os}}$	Offset voltage		<1 mV
PSRR	Power supply rejection ratio		> 80 dB
CMRR	Common mode rejection ratio		> 80 dB
$\mathbf{A_{dc}}$	Open loop gain		> 100 dB
SR	Slow rate		> 1 V/μs
$\mathbf{f_u}$	Unit gain bandwidth		3 MHz
$\mathbf{I_{dc}}$	Bias current		30 μA
PM	Phase Margin	C_L=50 pF	81.23
$\mathbf{e_n}$	Input referred noise	<1 kHz	300 nV/√Hz
$\mathbf{V_{dd}}$	Supply voltage range		1.6 V to 2.0 V
Temperature	Temperature range		-40 to 85C



(a) (b)

Figure 5.1 Rail-to-rail input pairs.

5.1.3 Circuit Design

This section represents the design methodology and presents the key circuit diagrams in previous chapter. Without compensation, rail-to-rail input stages exhibit transconductance variation over the input common mode range. This characteristic leads to deficiencies in performance which are discussed later. The section continues with a discussion of the input and output stages and the bias current circuit for the op-amp.

Fig. 5.1(a) shows a common method to increase the input common mode range of the classic op-amps. At low common mode voltages inputs, the PMOS input pair as M1 and M2 conducts current whereas M3 and M4 as NMOS pair operate at high common mode voltages. For mid-range common-mode voltage, both NMOS pair and PMOS pair work. Thus, the total transconductance, g_m, is defined by

$$g_m = g_{m,NMOS} + g_{m,PMOS} \tag{5.1}$$

where $g_{m,NMOS}$ and $g_{m,PMOS}$ are the transconductances of M1,2 and M3,4 respectively. Fig. 5.1(b) shows the plot of the g_m as a function of common mode voltage. In the middle of the range, g_m is twice the value at either low or high input common mode. The g_m variation may lead to distortion and inefficient frequency compensation [61]. Another drawback of the dual differential pairs is the minimum CMRR when the input CMR is near the middle since the offsets from each input pair are different. The input stage described circuitry to maintain a constant g_m over the entire input CMR.

Fig. 5.2 is the schematic of the class AB op-amp used in AFE. Transistors M1 to M4 form the dual differential pairs. M5-M12 transistors constitute a low-voltage folded cascade load for the differential pair biased with the floating current source as presented by M23 and M25. M17 through M26 provide class AB control for the output stage consisting of M13 and M14. Finally, BP1 and

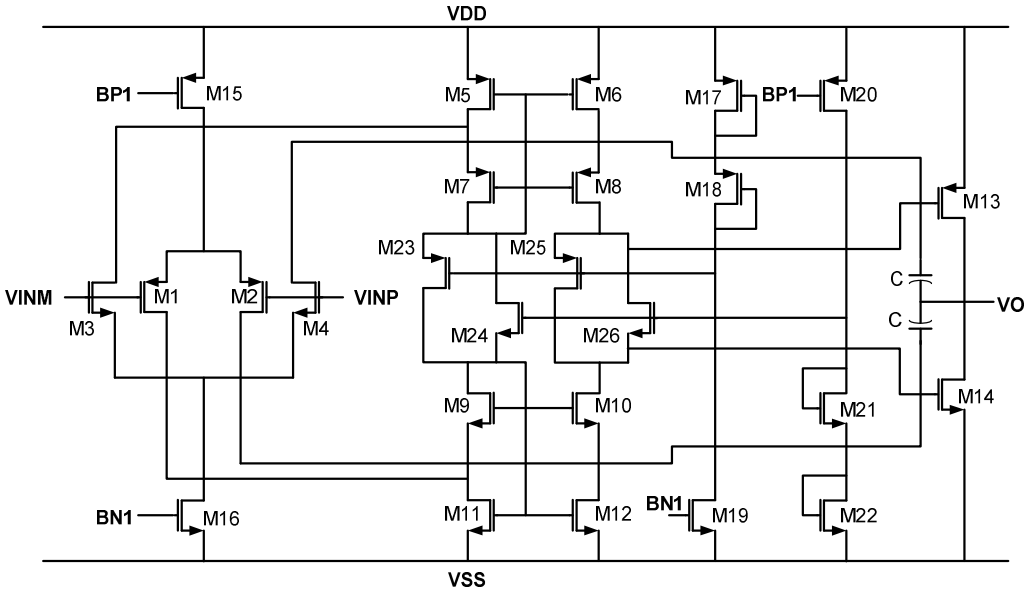


Figure 5.2 The single ended rail-to-rail class AB op-amp.

BN1 maintain constant g_m across the CMR by controlling the tail currents flowing through each differential pair.

The method for reducing the g_m variation across the input CMR depends on the region of the operation of the differential pairs. The input transistors are biased in weak inversion to reduce the input offset voltage and input referred noise [61]. However, in the weak inversion region, the current source mismatch is bigger than the saturation region. Thus, the input transistor should be biased in strong inversion to reduce mismatch at DC or low frequency. In strong inversion, g_m, depends only on the bias current I_d and V_{ov} (= $V_{\mathrm{ds,sat}}$) and is given by:

$$g_m = \frac{2I_d}{V_{ov}} \tag{5.2}$$

Applying (5.2) and assuming all coefficients are identical for the PMOS and NMOS pair:

$$g_m = \frac{2\left(I_{d1,2} + I_{d3,4}\right)}{V_{ov}} \tag{5.3}$$

where $I_{d1}$and I_{d2} are the bias currents for the PMOS and NMOS. Therefore, g_m is constant if the sum of the bias current sources M15 and M16 is constant. At low common-mode input, the PMOS pair receives all of I_{tail} of M15 whereas the NMOS pair sees all of I_{tail} of M16 curing high common-mode voltage excursions. In general, the assumption made is that some variance of g_m occurs even with perfect control of the currents.

Due to the gain of the first stage only a few transistors contribute substantially to the total noise and offset: M1-M4, M11-M12 and M17-18. The

equivalent input noise voltage spectral desist of a MOSFET biased in strong inversion with width *W*, length *L* and oxide capacitance per unit area is C_{ox} given by:

$$\frac{\overline{v_n^2}}{\Delta f} = 4kT\left(\frac{2}{3}\frac{1}{g_m}\right) + \frac{K}{WLC_{ox}f} \tag{5.4}$$

where *k* is Boltzmann's constant, *T* is the Kelvin temperature, *f* is the frequency, and *K* is flicker noise constant. The first term results from the random thermal noise and the second term is caused by traps and de-traps associated with poor fabrication and contamination as flicker or *1/f* noise.

Applying a voltage noise source with noise spectral density given in (5.4) at the gate of each transistor in the deal differential input pair and referring the noise back to the input of the op-amp results in the voltage noise spectral density contribution of M1-M4 given by:

$$\frac{\overline{v_{n,M1-M4}^2}}{\Delta f} = \frac{1}{\left(g_{m1,2}+g_{m3,4}\right)^2}\sum_{n=1}^{4}\left(g_{m1,2}+g_{m3,4}\right)^2\left(4kT\left(\frac{2}{3}\frac{1}{g_m}\right)_n + \left(\frac{K}{WLC_{ox}f_c}\right)\right)_n$$

$$= \frac{1}{4}\left(2kT\left(\frac{2}{3}\frac{1}{g_m}\right)_{1,2} + 2\left(\frac{K_p}{(WL)_{1,2}C_{ox}f_c}\right)_{1,2} + 2kT\left(\frac{2}{3}\frac{1}{g_m}\right)_{3,4} + 2\left(\frac{K_n}{(WL)_{3,4}C_{ox}f_c}\right)\right)_{3,4}$$

$$= kT\left(\frac{2}{3}\frac{1}{g_m}\right)_{1,2,3,4} + \frac{1}{2}\left(\frac{\mu_n K_p + \mu_p K_n}{(WL)_{1,2}C_{ox}f_c}\right) \tag{5.5}$$

where μ is the mobility and the subscripts p and n refer to PMOS and NMOS transistors. The derivation assumes $g_{m1,2} = g_{m3,4}$, $L_{1,2} = L_{3,4}$ and $\mu_p W_{1,2} = \mu_n W_{3,4}$. Note that (5.5) is valid only for the middle of the CMR when both input pairs are

equally active. Similarly, applying (5.4), the noise contribution from the current source transistors given by the following derivation:

$$\frac{\overline{v_{n,M\,5,6\,and\,11,12}^2}}{\Delta f} = 2kT\left(\frac{2}{3}\frac{g_{m5,6}}{g^2{}_{m1,2,3,4}}\right) + 2\left(\frac{K_p}{(WL)_{5,6}C_{ox}f_c}\right)\frac{g^2{}_{m5,6}}{4g^2{}_{m1,2,3,4}}$$

$$+ 2kT\left(\frac{2}{3}\frac{g_{m11,12}}{g^2{}_{m1,2,3,4}}\right) + 2\left(\frac{K_n}{(WL)_{11,12}C_{ox}f_c}\right)\frac{g^2{}_{m11,12}}{4g^2{}_{m1,2,3,4}}$$

$$= 2kT\left(\frac{2}{3}\frac{g_{m5,6}}{g^2{}_{m1,2,3,4}} + \frac{2}{3}\frac{g_{m11,12}}{g^2{}_{m1,2,3,4}}\right)$$

$$+ \left(\frac{1}{2C_{ox}f(WL)_{11,12}}\right)\left(\frac{1}{g^2{}_{m1,2,3,4}}\right)\left(K_n + \frac{\mu_n}{\mu_p}K_p\right)\left(g^2{}_{m5,6} + g^2{}_{m11,12}\right) \quad (5.6)$$

The combination of (5.5) and (5.6) result in the total input-referred voltage noise spectral density for the input common-mode voltage at the middle of the CMR. Table 5.2 summarized methods and associated costs for reducing the noise.

Table 5.2 Noise reduction and associated cost

Technique	**Cost**
Increase size of input differential pairs	Area
Increase g_m	Power
Increase I_{BIAS}	Power
Increase $L_{11,12}$ and $L_{17,18}$	Area and bandwidth

In addition to providing gain, the output stage drives signals rail-to-rail and ensures stability for the unity-gain configuration. Some applications require the output stage to have low output resistance to efficiently drive low resistance loads. The voltage follower configuration, where the sources of the output transistors connect to the output, has a low output resistance but restricts the output from swinging within a drain-source saturation voltage and a gate-source voltage to both supply rails. To facilitate the rail-to-rail operation, however, the drains not the sources of the output transistors connect to the output node in Fig. 5.2. While this topology increases the output swing, the output resistance suffers. Typically, large output resistance is not a problem for on-chip applications when the amplifier drives loads that are predominantly capacitive.

As mentioned earlier, the class AB output stage in the amplifier consumes most of the current budget. To estimate the required current, the frequency characteristics of the output stage are examined. The output stage adds a second pole to the frequency characteristics of the amplifier. Although non-dominant, this pole affects the parse margin. Assuming relatively large compensation capacitors and load capacitance, C_L, the second pole resides at frequency f_{bw} [58] given by:

$$f_{bw} \approx \frac{g_{mab}}{2\pi C_L} \tag{5.7}$$

where g_{mab} is the transconductance of the output stage which is equal to the sum of g_{m13} and g_{m14}. To be a stable operational amplifier, f_{bw} should be at least three times the unity gain frequency, f_u to guarantee phase margin (PM) 60^o over. If

g_{m13} and g_{m14} are equal, substituting (5.7) into (5.2) results in the following equation for the required quiescent current in the output stage:

$$I_{d,ab} = 3\pi V_{ov} C_L f_{bw} \tag{5.8}$$

At room temperature, the output stage consumes nearly three quarter of the power.

Class AB control provided by trans-linear loops sets the quiescent current level in the output transistors. Trans-linear loops were originally developed in the context of a sum of based-emitter voltages in (5.9), but the concept can also be applied to gate-source voltages.

$$V_{SG,17} + V_{SG,18} = V_{SG,25} + V_{SG,13} \tag{5.9}$$

The trans-linear loop controls the biasing of M25 in Fig. 5.2 where M25 conducts half of M19, I_{d18} is equal to I_d of M19, and it is assumed that $(W/L)_{18}= 2(W/L)_{23}$ and $Vsg_{23}=Vsg_{18}$. Therefore, (5.9) implies that $V_{sg17}=V_{sg13}$ and that the following relationship can be derived:

$$I_{d,AB} = I_{d,19} \frac{(W/L)_{13}}{(W/L)_{17}} \tag{5.10}$$

Since M13 is biased in strong inversion as well as M17. A similar equation (5.11) results for the quiescent current in M14 controlled by the trans-linear loop consisting of M14, M21, M22 and M26.

$$I_{d,AB} = I_{d,20} \frac{(W/L)_{14}}{(W/L)_{22}} \tag{5.11}$$

Equations (5.10) and (5.11) imply that M13, M14, M19 and M20 should be sized such that $I_{d,13}$ is equal to $I_{d,14}$ Based on this equation and the simulated transistor level, the ac response results show in Fig. 5.3.

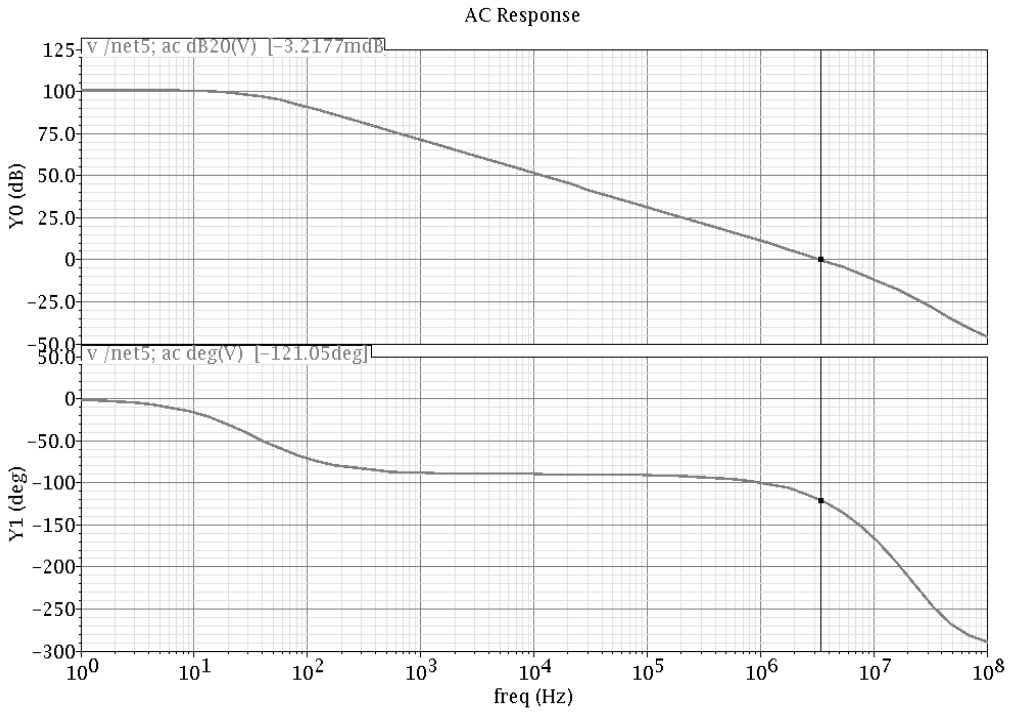


Figure 5.3 AC response of Chopper Amplifier.

5.2 RESISTOR STRING DAC

In this section, the implementation of the resistor string DAC will be presented. This DAC is based on a decoder. The typical DAC consists of a resistor string acting as a voltage divider that provides taps for the different voltage levels to perform digital-to-analog data conversion. One of these voltage taps is selected by a decoder to connect the appropriated voltage tap to the output node. A 3-bit DAC is shown in Fig. 5.4.

The decoder in Fig. 5.4 consists of a number of transmission gates that form a switching network. The switches are connected in the form of a tree; only one low impedance path connecting one of the resistor string voltage tap points to

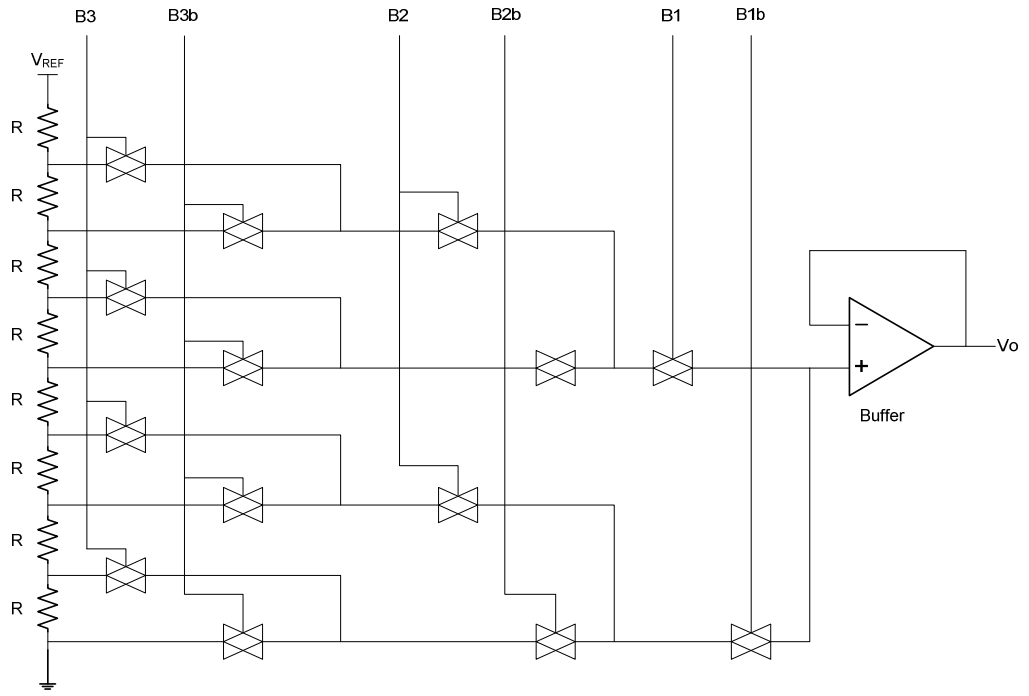


Figure 5.4 A 3 bit resistor string DAC using transmission gate.

the output node exists. The advantage of using a transmission gate switch is that the output voltage will operate close to the power supply voltage levels.

Instead of transmission gates, a NMOS transistor based decoder may be used. This results in a reduced value of the voltage swing at the output node. However, the speed of operation may not be severely diminished because of reduced amount of source and drain capacitance and the absence of the PMOS transistors. This reduced capacitance can offset for the increased resistance due to the absence of the PMOS transistors of the transmission gates.

The resistor string tap points ensure that monotonicity is maintained in the tapped voltage and therefore for the DAC. The accuracy of the DAC depends on the matching of these resistors. The delay through the decoder determines the data

conversion speed of the DAC. Each of the transmission gates adds to the resistance of the decoding path. The low impedance path will have three transmission gates with ON resistance. The capacitive load consists of at the source and drain capacitances of nearly 9 transistors in Fig. 5.4. Generally, 2N from the transistors comprise transmission gates and source/drain capacitance of non-N-switching transistors of the high impedance paths.

To make a low impedance node at the DAC output and isolate the DAC output and potentiostat input, a class AB buffer stage is used. The buffer amplifier is shown in Fig. 5.2 which is used to generate voltage output. The amplifier also works as a rail-to-rail amplifier to stimuli chemical reactions like oxidation/reduction. The advantages of string DACs are low cost and guaranteed monotonicity due to the string architecture. An important aspect of string DACs is it offers low power and small die area which allow for small packages and makes them desirable in portable applications. Another advantage is that the output buffer is already included which eliminates the need for an additional external component on the board. Furthermore, the output buffer isolates the internal resistors and the analogue circuitry from the outside world. This is quite helpful in low-impedance circuitry. Many applications require low-glitch energy, which is another benefit of string architecture. Of course buffer amplifiers have offset and this can cause non-monotonicity in a buffered resistor string DAC.

5.3 CURRENT STEERING DIGITAL-TO-ANALOG CONVERTER

Segmented DACs are a hybrid between the binary weighted and the thermometer decoded topologies. This mix proved to be the fastest and most precise topology at the expense of die area. The major advantage of sourcing current to the conductometric sensor array is that the current through the sensors can be controlled by digital input. This is a very importance issue because the maximum current drive for conductometric sensor may be limited to less than 60μA. Thus, the maximum current from the DAC is 51.1 μA

The DAC operates from a 1.2V power supply and results in limited voltage headroom for each DAC cell. In many current steering DACs, the limited

Table 5.3 Binary to thermometer code

B3	B2	B1	D7	D6	D5	D4	D3	D2	D1
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	1
0	1	1	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1	1
1	0	1	0	0	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

voltage headroom and the finite output resistance of DAC cells leads to nonlinear characteristics. The voltage headroom concern is somewhat relieved for this application; however, because the DAC cells operate in the strong inversion region, 1LSB as a unit current is only 100 nA.

The segmented DAC consists of a 3-bit binary weighted DAC and 6-bit unit element DAC. The six most significant bits (MSB) of the DAC select the 6-bit unit element DAC. The 6-bit unit element architecture consists of 64 unit array current sources arranged in an 8 x 8 matrix. The matrix is logically seen as being composed of 8 x 8 arrays oriented side-by-side as in Fig. 5.5. The thermometer decoder is a two-stage decoder reproduced two times. There is a 3 to 7 bit

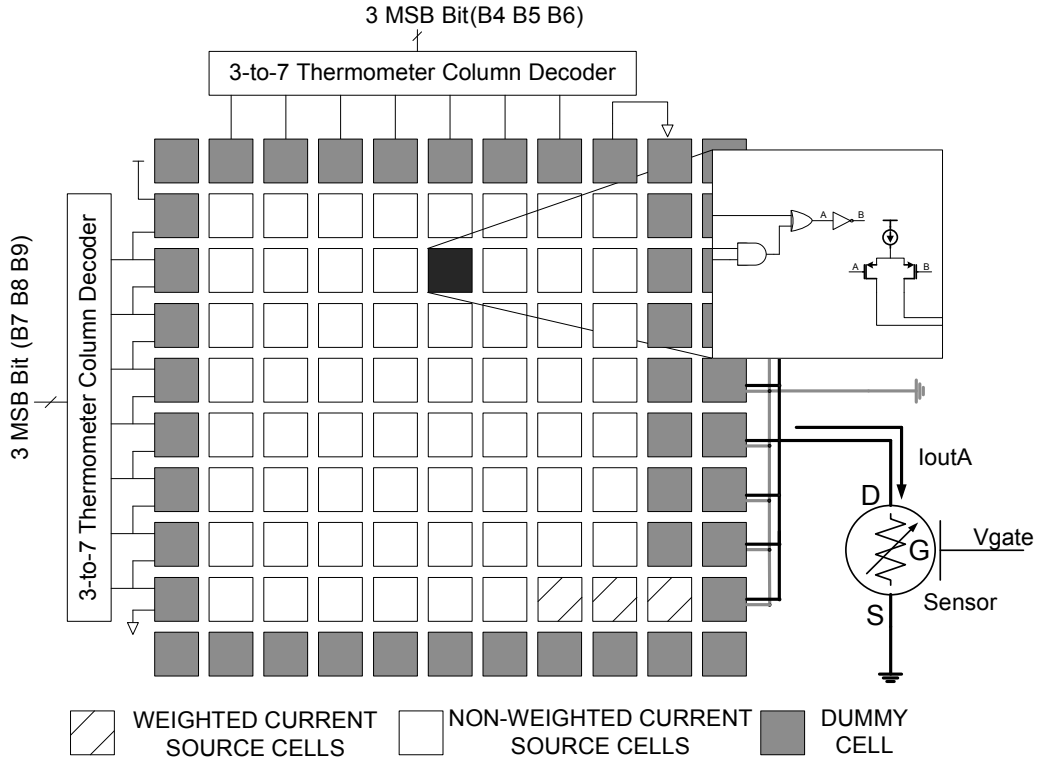


Figure 5.5 Current steering DAC for the conductometric sensor.

thermometer row decoder and a 3 to 7 bit (Table 5.3) thermometer decoder. A row-column decoder of six bits requires only AND and OR gates with at most three inputs.

The remaining binary weighted four LSB select a simple PMOS 3-bit current divider. These current sources will be placed in two columns next to the matrix. The 3-bit current divider generates the currents I_{LSB}, $2I_{LSB}$, and $4I_{LSB}$. The first three currents are each switched by a two way switch to I_{outA} or I_{outB}.

Typical sources of systematic process related MOS transistor mismatch are variations in the gate dimensions, wafer gradients in the gate-oxide thickness and in the channel doping, photolithographic and etching effect and asymmetry. To reduce these effects, the device should have the same shape and size. In addition, matching devices should be at minimum distance. Also, devices should have the same current orientation. To avoid gradient effects, common centroid geometry and interdigitated geometry are used. However, for transistors with large *W/L*, a simple rectangular geometry becomes impractical, because the aspect ratio strongly devices from one, and introduces transistors with large *W/L* ratios are used, the layout style may have an influence on the matching performance. The avoid systematic variations in the transistor drain current, duet to electrical, thermal or process gradients and point symmetric structures are recommended. To keep the transistor aspect ratio close to one, finger structures are the preferred layout method.

In Fig. 5.6, there is a basic current source and switching transistors. As discussed in the previous chapter, the current source has to be rather big for better

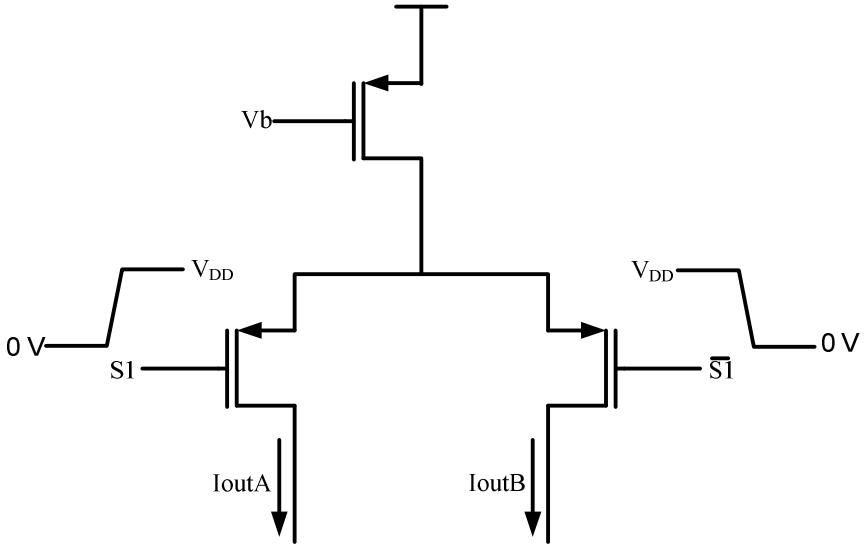


Figure 5.6 An unit cell of current steering DAC of the conductometric sensor.

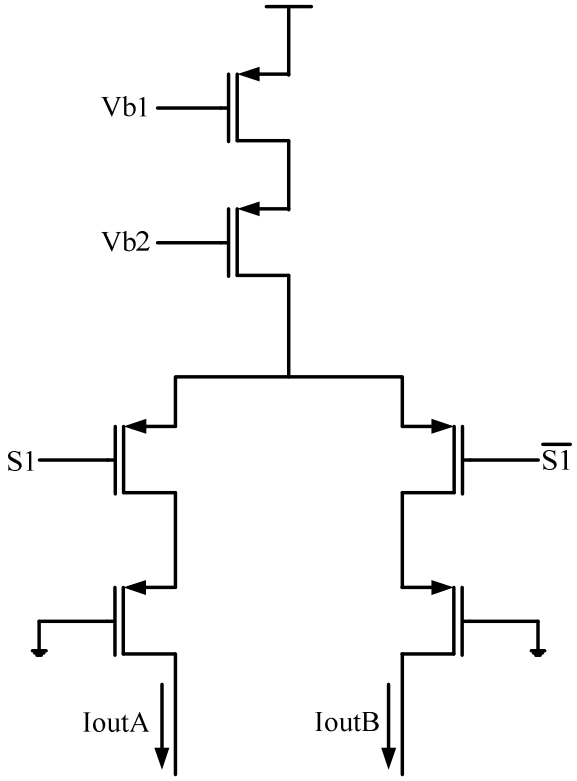


Figure 5.7 A modified unit cell of current steering DAC.

matching and for better linearity. The currents are each switched by a two-way switch to I_{outA} or I_{outB}. To reduce the glitch energy, the control signals for the switches come from thermometer code shown in Table 5.3.

Charge feed through is the one of caution of glitches. To reduce the glitch power, the switch circuit is modified in Fig. 5.7. An extra cascade transistor is added to provide the necessary high output impedance and a dummy transistor is inserted to partially compensate for the charge feed through.

5.4 ANALOG MULTIPLEXER

The analog multiplexer allow the use of a single amplifier to service multiple gas sensor channels. One possible candidate of a multiplexer is the tree-

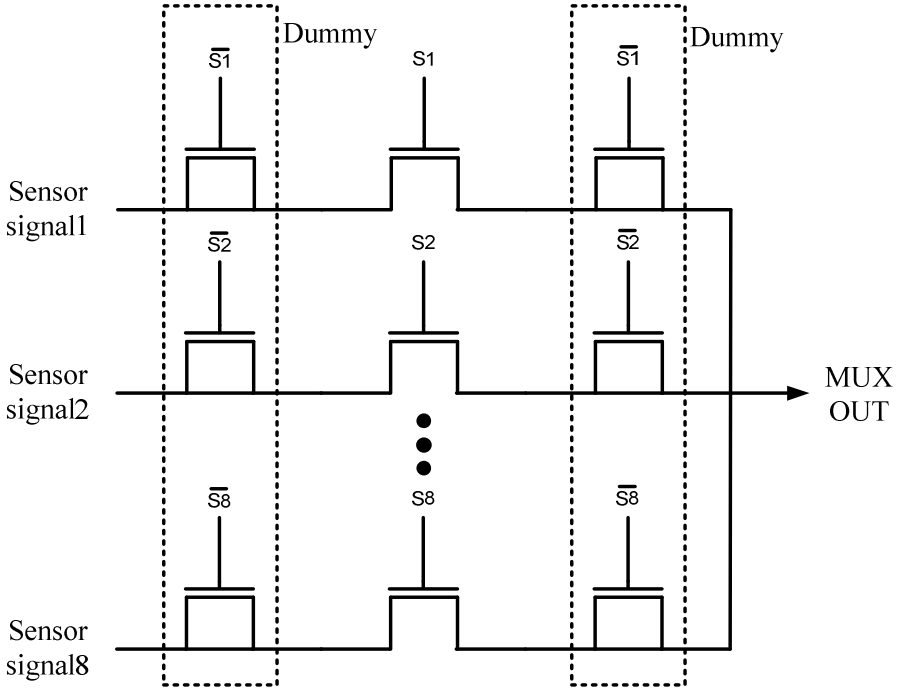


Figure 5.8 8-Channels analog multiplexer.

structured transmission gate. By organizing the transmission gates in a tree-structure, a separate decoder is not needed. The circuit details for a part of the 8-channel analog multiplexer possessed by each gas sensor are shown in Fig. 5.8. The input and select signals will be labeled sensor signal1 through sensor signal8 and S1 through S8 respectively. The select digital input signals go off-chip allowing user control. The multiplexers are simply transmission gates that pass the signal when their gates are turned on and become high-impedance when their gates are turned off. Charge injection cancellation is achieved by inserting dummy switches which are driven by complementary select signals [31]. The dummy switches are also inserted between the channel and main switches to isolate the effect of charge feed through from the original sensor output signal.

The problem of having a tree-structured transmission gate multiplexer is that the on resistance is be too large, and that the resistance is actually nonlinearly dependent on the input voltage. The maximum on-resistance of the transmission gate is at least 10 kΩ with minimum channel length and the value of the resistance may vary as the input voltage varies. The various on-resistances exist because neither NMOS nor PMOS are strongly turned on around low input signal and high input signal.

To gain lower on-resistance regardless of input signal, the width of the transmission gates should be increased. However, the width of the transistors cannot be increased indefinitely because the large gate capacitance may require the drivers to turn on and off the transistor. This causes not only the increase in energy dissipated from charging and discharging the large gate capacitance, but

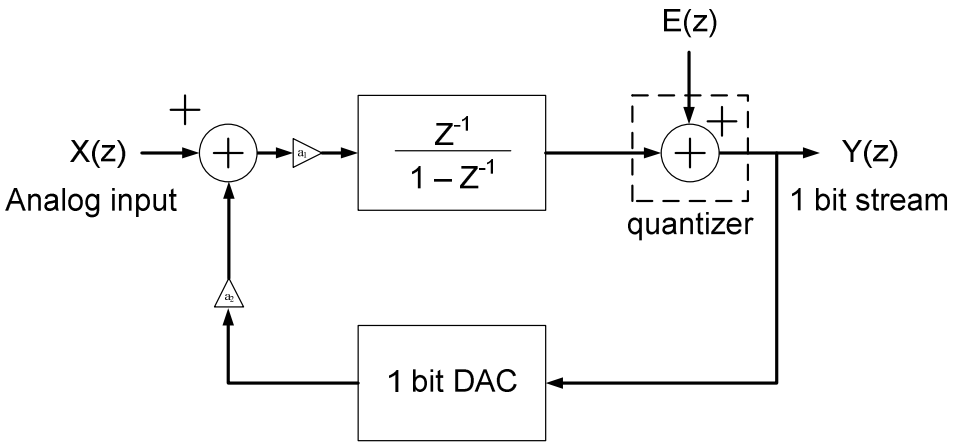


Figure 5.9 Block diagram of the 1st order ΣΔ modulator

also to turn on and off the large drivers. Thus, multiplexor trade-offs between transistor size, power consumption and parasitic capacitor should be considered.

5.5 FIRST ORDER NESTED CHOPPED SIGMA DELTA (ΣΔ) MODULATOR

5.5.1 First Order ΣΔ Modulator

Recall from chapter 3, the block diagram of a first order sigma delta modulator is shown in Fig. 5.9, which consists of an integrator, a comparator and 1-bit DAC. The target application for this converter is gas chemical sensor with two types of sensors. Typically, applications involving chemical transducers require low bandwidth like a low Hz, but high resolution. The name first order is derived from the information that there is only one integrator in the circuit placed in the forward path. When the output of the integrator is positive, the comparator feeds back a positive reference signal that is subtracted from the input signal of the integrator. Similarly, when the integrator output is negative, the comparator

Table 5.4 Target specification for first order ADC

Parameter	Specification
Supply voltage	1.8 V
Power	< 100 μW
Input signal bandwidth	< 32Hz
Dynamic range	91 dB
Oversampling ratio	4096

feeds back a negative signal that is added to the incoming signal. The integrator therefore accumulates the difference between the input and quantizes the output signals from the DAC output which is in the feedback loop and makes the integrator output around zero. A zero integrator output implies that the difference between the input signal and the quantized output is zero [63].

The coefficients, a_1 and a_2, determine the signal and noise transfer function. Table 5.4 shows the specifications for the first order ADC. Based on the simulink simulation in MatLab, the coefficients are 0.5 and 1.

5.5.2 Design of Integrator

The integrator is the most important component in a ΣΔ modulator. As discussed earlier, oversampling converters typically use switched-capacitor circuits and therefore do not need sample-and-hold circuits. In many analog and

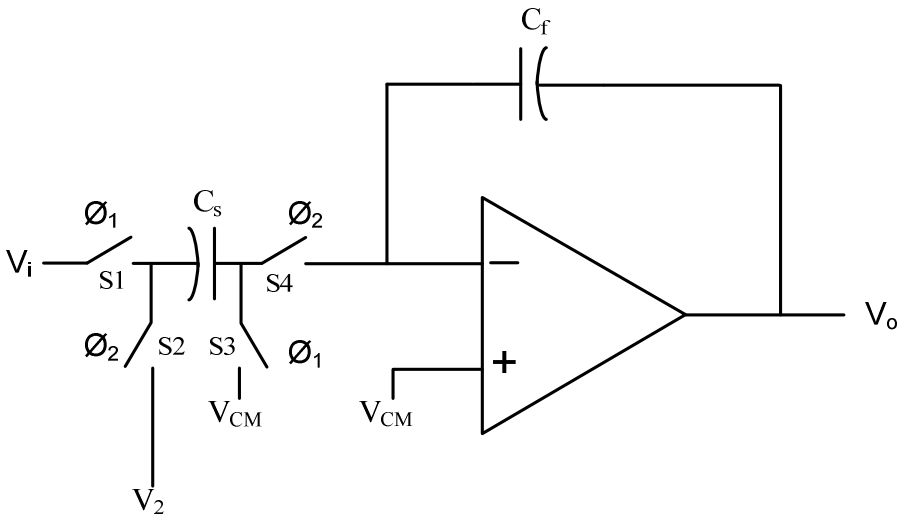


Figure 5.10 A noninverting integrator.

mixed-signal devices, SC circuits perform linear analog signal processing. They are used in various practical applications, such as data converters, analog filters, and sensor interfaces [64].

The basic building block of most SC circuits is the stray insensitive integrator as shown in Fig. 5.10 [34]. The SC integrator is single ended to explain the transfer function and time simply. It is the conventional non-inverting SC integrator which is used in our analog to digital converter architecture. The frequency response of the integrator is sensitive to the various parasitic capacitances presented on all the nodes in the circuit. However, there are some limitations on the operation of switches with low supply voltages. The low supply voltage may not allow enough overdrive to turn on the transistors used as switches even if complementary switches are used.

As seen from Fig. 5.10, the SC integrator consists of an OTA, a sampling capacitor C_S, an integrating capacitor C_f, and four MOS transistor switches. Fig.

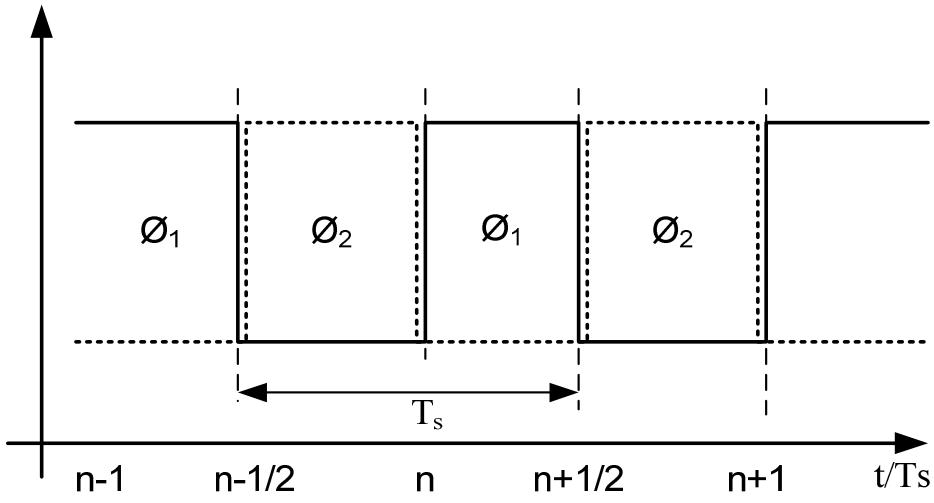


Figure 5.11 Timing diagram for the non-overlap signals.

5.11 shows the timing diagram of two non-overlapping clock signals, ϕ_1 and ϕ_2, which control the operation of the circuit. The common mode voltage V_{CM} is halfway between the mixed signal systems high reference voltage and low reference voltage. Hence the common mode voltage (V_{CM}) is 0.9 V. During the interval when the clock phase ϕ_1 is high, switches S1 and S3 operate and serve to charge the sampling capacitor, C_S to a voltage that is equal to the input voltage. Subsequently, clock signal ϕ_1 falls. Then clock signal ϕ_2 rises, switches S2 and S4 to turn on and the sampling capacitor, C_S is connected between the inverting OTA input, which is sometimes called the summing node, and ground. If the op-amp is ideal, the resulting change in the summing-node voltage causes the op-amp output to change so that the summing-node voltage is driven back to ground. After the transient has gone to completion, the voltage across C_S is driven to zero.

To find the relationship between the input and output, a charge conservation analysis is used. After switch S1 opens, the charge on the plates of the capacitors connected to node top and the inverting op-amp input is conserved until switch S1 closes again. Now define two points [n] and [n+1/2] as the time indices at which ϕ_1 and ϕ_2 first fall as shown in Fig. 5.11. Point [n+1] is defined as the next time index at which ϕ_1 falls. The points [n] and [n+1] are separated by one clock period T. If the switches and the op-amp are ideal, the charge stored at time index [n] is given by[49]:

$$Q[n] = (0 - V_i[n])C_s + (0 - Vo[n])C_f \tag{5.12}$$

where V_2 represents the input voltage at the end of ϕ_1 and V_O represents the output voltage at the end of ϕ_2. Here, if the op-amp is ideal, the voltage V_i from the inverting op-amp input to ground is driven to zero by negative feedback during ϕ_2.

At the same conditions, the charge stored at time index [n+1/2] is given by the following equation:

$$Q[n+1/2] = (0 - V_o[n+1/2])C_f \tag{5.13}$$

For charge conversation, $Q[n+1/2] = Q[n]$. Also, the charge stored on C_f is constant during ϕ_1 under these conditions; therefore, $V_o[n+1] = V_o[n+1/2]$. Combining these equations gives (5.14).

$$V_o[n+1] = V_o[n] + \frac{C_s}{C_f}(V_i[n]) \tag{5.14}$$

Thus, one complete clock cycle results in a change in the integrator output voltage that is proportional to the value of the input voltage and to the capacitor ratio. The above equation is used to find the frequency response of the integrator by using the fact that the signal is delayed by a clock period T in the time domain. The equation in z-domain results in the equation below [32]:

$$V_0(z)(1-z^{-1}) = \frac{C_S}{C_I}(v_1(z)\cdot z^{-1} - v_2(z)\cdot z^{-1/2}) \tag{5.15}$$

The transfer function of the DAI with the output connected to the ϕ_1 switches is given by [32]:

$$V_0(z)(1-z^{-1}) = \frac{C_S}{C_I}\frac{(v_i(z)\cdot z^{-1} - v_2(z)\cdot z^{-1/2}}{1-z^{-1}}) \tag{5.16}$$

Note that if v_2 (z) =V_{CM}, this equation can be written as [32]:

$$V_0(z) = \frac{C_S}{C_I}\frac{z^{-1}}{1-z^{-1}}v_1(z) \tag{5.17}$$

The (5.17) is used for the integrator in the design of modulator. The values of capacitances are shown in the Fig. 5.10, i.e. C_S = 12.5 pF and C_I = 25 pF so that the gain of the integrator is 0.5. Here the gain is kept less than 1 to make the first order modulator loop stable and also to avoid the integrator from saturating. The capacitance ratio is important than the individual values of the capacitors. Even

smaller capacitances can be used, but to avoid charge leakage problem, they are taken high.

5.5.3 Design of Operational Transconductance Amplifier (OTA)

As mentioned above, the operational transconductance amplifier (OTA) is the important element of most analog systems, particularly in switched capacitor techniques, and the performance of many circuit is influenced by the OTA performance [60], [68]. The OTA has sufficiently high voltage gain so that when the negative feedback is applied, the closed-loop transfer function can be made independent of the gain of the OTA. This principle is employed in many useful analog circuits and systems. The primary requirement of an amplifier is to have an open loop gain that is sufficiently large to implement the negative feedback concept. One of the popular methodologies is a folded cascade OTA.

If the OTA is intended to drive a small purely capacitive load, which is the case in many switched capacitor or data conversion applications, the output buffer is not used. On the other hand, if the op-amp is to drive a resistive load or a large capacitive load, the output buffer is used. Design of OTA consists of determining the specifications, selecting device sizes and biasing conditions, compensating the op-amp for stability, simulating and characterizing the OTA loop gain, creating common-mode range (CMR) on the input, in addition to determining the common-mode rejection ratio (CMRR), the power supply rejection ratio (PSRR), the output voltage range and the power dissipation.

The amplifier used in this system is a fully-differential cascode amplifier which can be seen in Fig. 5.12. The folded cascode amplifier topology is used because it achieves the highest gain with a single stage and load capacitor compensation. The area of the input transistors can be reduced because their flicker noise contribution will be reduced by the chopper technique. This OTA with chopping switches will be discussing later. The principal factors that effected the amplifier type selection were [12], [60]:

- Input Dynamic Range: The inputs to the amplifier may range between microvolts to 1 mV. Therefore, a gain somewhere in the range of 500 to1000 was required.
- Noise: Although our chopper implementation helped with the flicker noise, it offered no reduction in thermal noise. We needed to have a reasonably small amount of noise compared to the signal measured.
- Area: The area available is fairly small in a cultured tissue and cell recording environment. Although multiplexing the input signals does reduce the area, it may still not be enough for recording via massive arrays.

The cascode amplifier is the best choice for the following reasons:

- It provides a large gain in a single stage.
- Area is reduced because there is no need for a second stage.
- It is more stable because of self-compensation or load capacitor compensation.

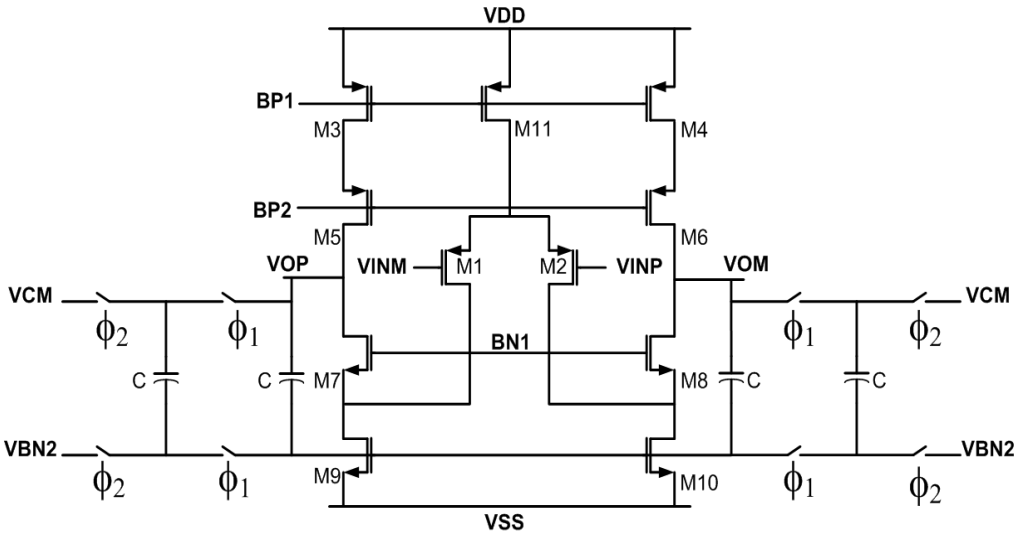


Figure 5.12 The fully differential transcendence amplifier (OTA) with SC CMFB and no chopper stabilization technique.

The cascode amplifier has an important drawback which is that the dynamic range of the output is somewhat limited due to the stacking of the transistors. As shown in Fig. 5.12, this amplifier exhibits a gain of 62 dB with a 3.2 MHz gain bandwidth. This configuration results in more than 80 dB CMRR.

5.5.4 Ota with Chopper Stabilized Switches

As discussed in previous section, the dominant noise source of the 1st ΣΔADC is DC offset and *1/f* noise in operational transconductance amplifier. To reduce the offset and noise of the OTA, a chopper stabilization technique is applied to the amplifier then called a chopper stabilized amplifier. The chopper stabilized amplifier is shown in Fig. 5.13. The first chopper in a PMOS differential pair converters a significant signal at low frequency to high frequency. The second chopper again transposes the signal at low impedance nodes and

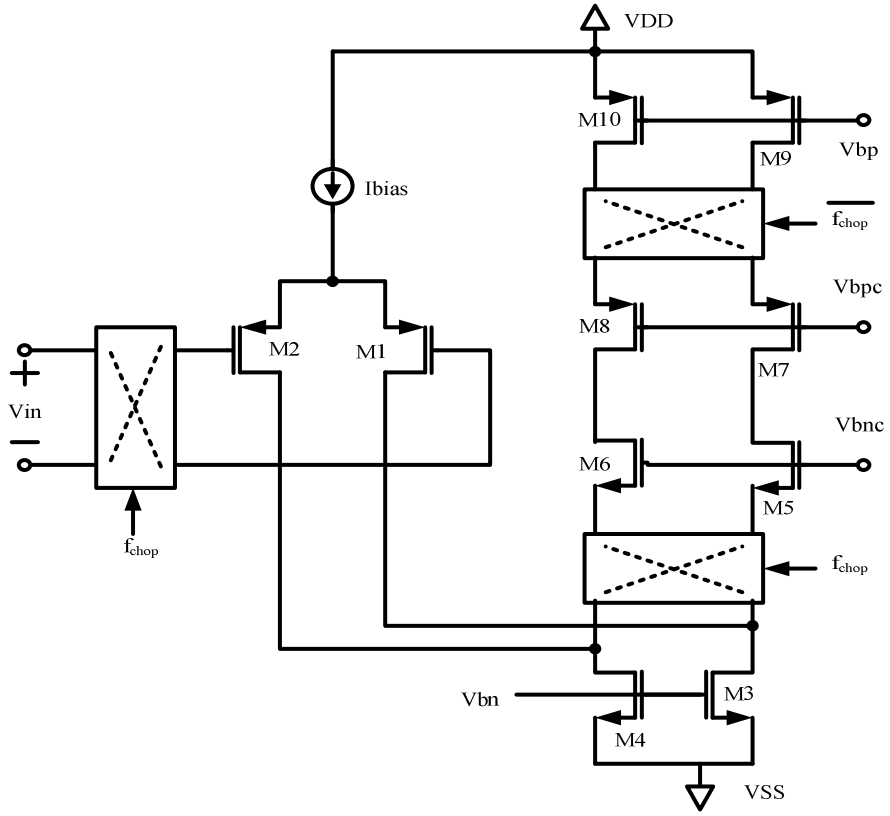


Figure 5.13 Chopper Stabilized Amplifier.

demodulates back the signal canceling out the offset of the bottom transistors. The offset and noise from the current sources will be canceled out by the third chopper which dynamically matches the two transistors on top. There are no consequences to the signal due to the third chopper.

The benefit of chopping at low impedance nodes comes from the large bandwidth of the basic amplifier. Therefore, we can chop at much higher frequencies where the only limitation is the charge injection residual offset and the slewing behavior of the input stage. In addition, the cascoded transistors provide low-pass filtering for the high frequency spectral contributions that are generated from chopping clock.

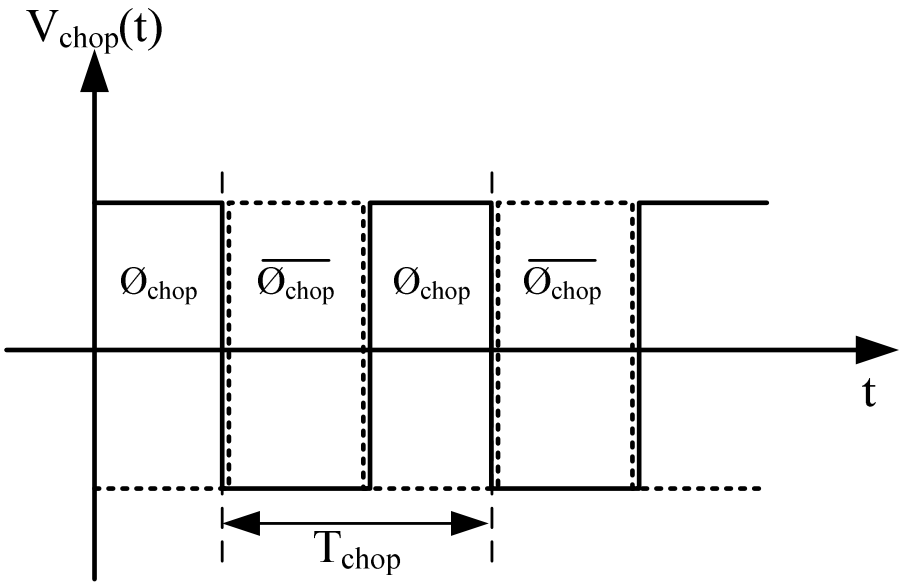
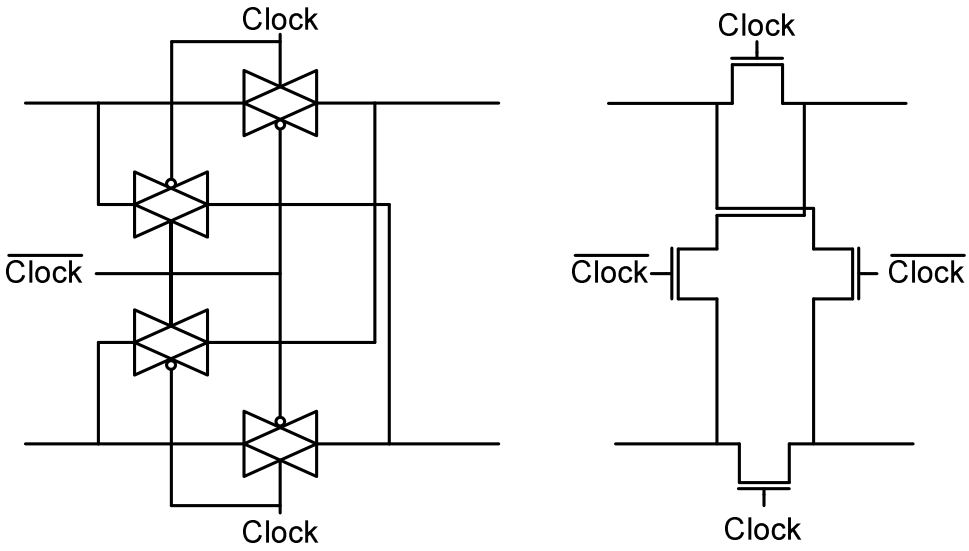


Figure 5.14 Nonoverlap chopping signal.

5.5.5 Chopper Modulator and Demodulator

The purpose of the modulator is to multiply the input with the waveform seen in Fig. 5.14. The variables ϕ_{chop} and $\overline{\phi_{chop}}$ are non-overlapped signals. The simplest way to do this is using the circuitry is shown in Fig. 5.15 [21]. Depending on input signal level, the type of chopper switch is different. The low-to-high input swing needs the switch in Fig. 5.15(a) while low input or high input only needs the switch in Fig. 5.15(b). The modulator inverts the signal when CLOCK is low and does not invert the signal when CLOCK is high. The demodulator is identical. However, the modulator and demodulator can be independently controlled which makes it possible to adjust for phase delay problems [62].



(a) (b)

Figure 5.15 Chopper modulator and demodulator.

Fig. 5.16 illustrates the circuit diagram. The input chopper Ms1, Ms2, Ms3 and Ms4 transposes the differential input signal applied to the terminals Vin+ and Vin- to the alternate output nodes. The second chopper Ms5, Ms6, Ms7 and Ms8 demodulates the signal and modulates *1/f* noise and offset at odd harmonics. The cascoded mirror M5, M6, M7 and M8 performs the required broadband differential to single ended conversion at the output. The need for large bandwidths implies small transistor lengths for M11 and M12 and therefore, also implies extra offset and 1/f noise. For this reason a third chopper is being introduced in the signal path Ms9, Ms10, Ms11 and Ms12. The unswitched cascode transistors provide further improvement in switching noise and residual offset by low-pass filtering some of the noise components generated from chopping and keeping low-voltage swings at their sources.

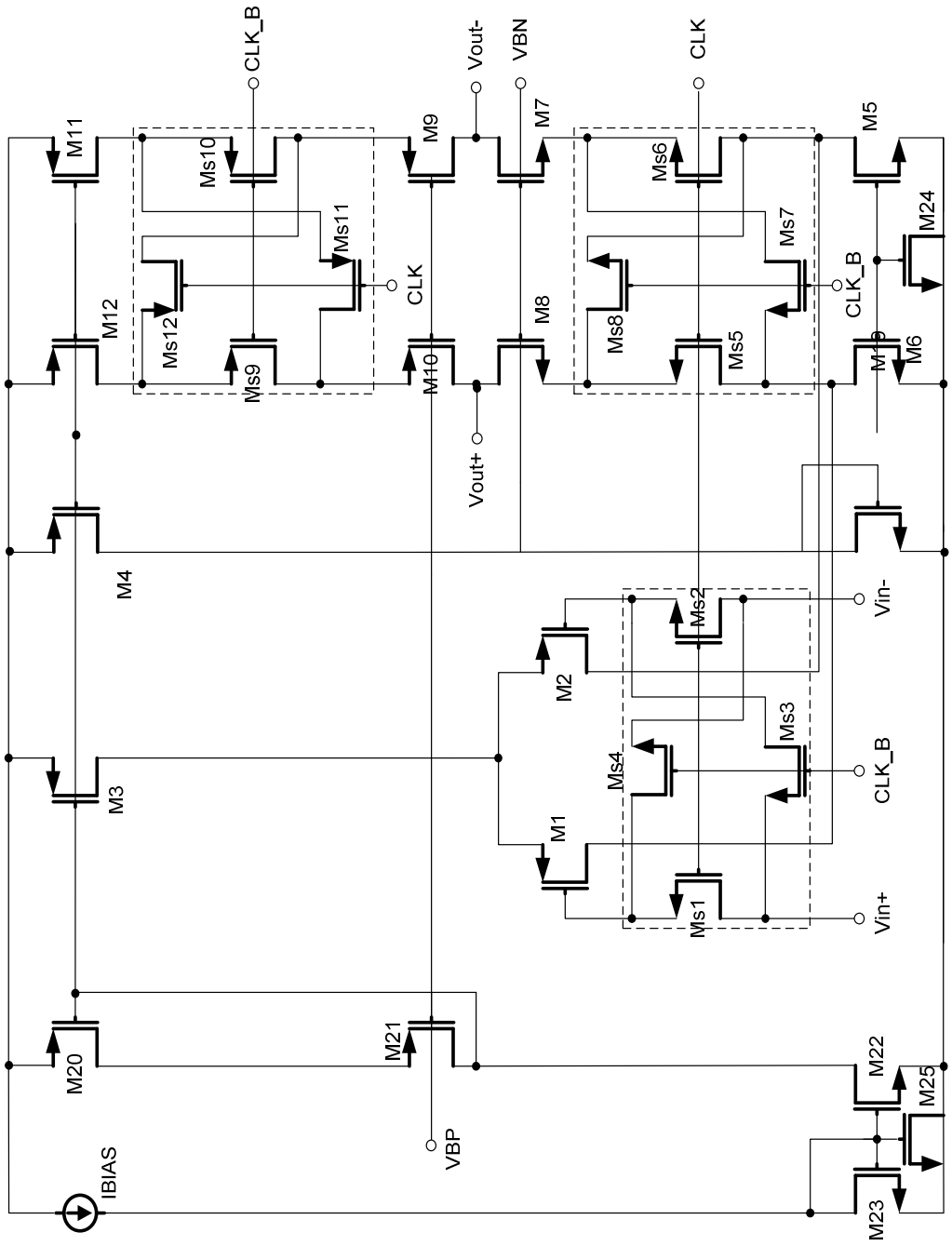


Figure 5.16 Schematic for Chopper Stabilized Amplifier.

Another source of concern in mixed-level applications is the substrate bounce coming from the digital circuitry. Modern processes have a low ohmic substrate that generate noise in the digital circuits affects and pollutes the substrate of analog circuit In CMOS technology for mixed level signal processing, the substrate bounce can reach 300mV in amplitude with spectral contributions in the gigahertz range further reducing the voltage swing [43]. In order to minimize substrate interferences, only PMOS transistors and NMOS switches with small dimensions are being used in the signal path [44]. The oxide capacitance of M25 decouples the BIAS line to ground. Substrate interferences present in the sources of cascoded transistors M7 and M8 will also be present at their gates such that gate source voltages of the same transistors can be considered constant for HF substrate noise [43]. For the same reason, the current sources M5 and M6 have their gates decoupled to ground via a large capacitance in M24.

As seen in Fig. 5.16, without chopper (Ms1~Ms12), this amplifier is nothing but a folded cascoded amplifier. A folded cascoded amplifier has the following open loop response by

$$A_v(s) = \frac{g_{m1} R_{out}}{(1 + s / p1)} \tag{5.18}$$

where R_{out} is the output impedance at V_{out} and p_1 is a pole of the system, which can be represented in the following equations,

$$R_{out} = g_{m5} r_{o5} r_{o7} \| g_{m11} r_{o11} r_{o9} \tag{5.19}$$

$$p_1 = \frac{1}{C_L R_{out}} \tag{5.20}$$

As seen in (5.20), a folded cascoded amplifier has a single pole (p_1) and C_L is presented for load capacitance. Therefore, gain bandwidth product is depicted as follows:

$$GBW = \frac{g_{m1}}{C_L} \tag{5.21}$$

From (5.21), the unity gain frequency is dependent on the load capacitor (C_L) and transconductance (g_{m1}) of the input device of the amplifier. Fig. 5.17 shows the simulated open loop AC response of the proposed OTA for 25 pF load conditions.

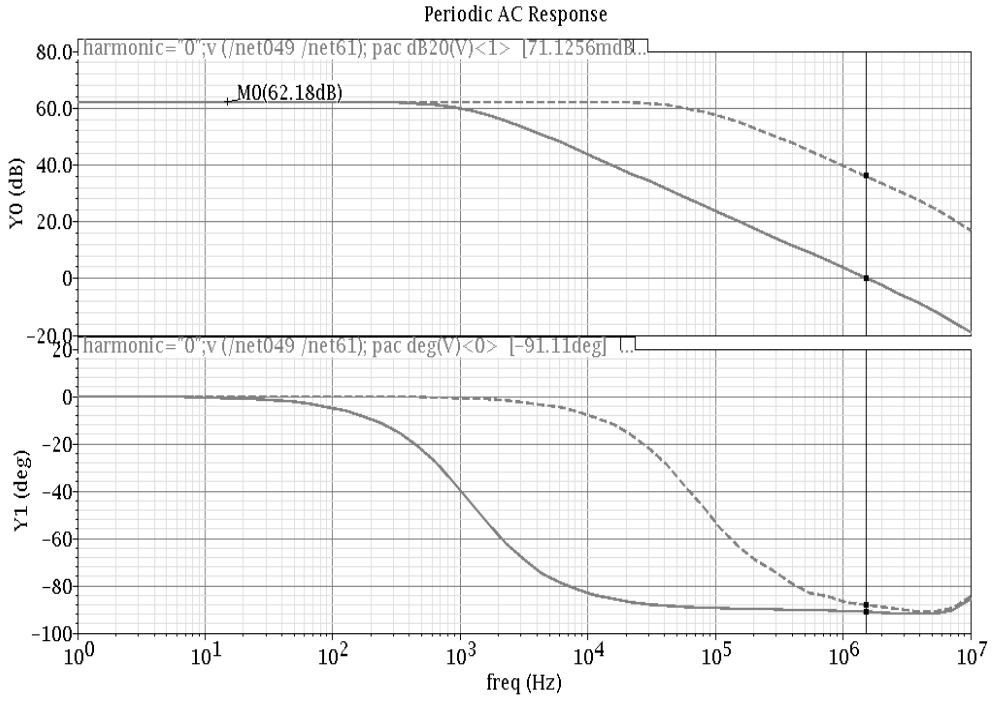


Figure 5.17 AC response of Chopper Amplifier with load (solid line) and no load (dash line).

From the simulation results, phase margin (PM) achieves 89.1 degrees at no load and full load conditions respectively.

5.5.6 Amplifier Common Mode Feedback

Although the magnitude and percent mismatch of parasitic capacitance has a considerable effect on the performance of the modulator, a ten percent difference should not cause the modulator to saturate. It was determined that the saturation in the initial design was due to the amplifier's common-mode feedback (CMFB). The CMFB produced a large common mode output ripple. The ripple is considered to be the output swing of the integrator when no input signal or parasitic mismatch is present. Together a parasitic mismatch error term and a large CM output ripple can easily saturate the modulator even for a small input parasitic mismatch. The CMFB produced a large ripple because of the following four reasons. First, the switches found in the CMFB SC circuit were too large,

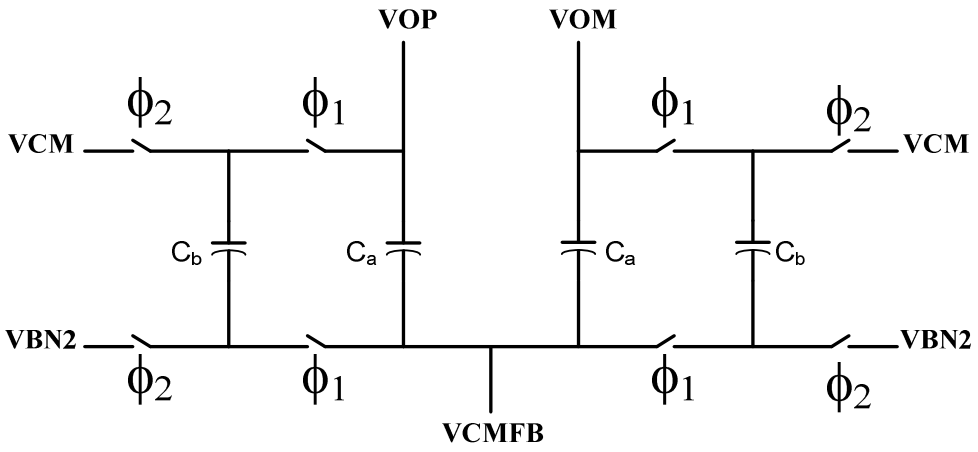


Figure 5.18 Switched capacitor common mode feedback circuit.

creating charge injection problems on the output voltage. Second, the averaging capacitors as C_a as presented in Fig. 5.18 in the SC CMFB circuit were too small allowing the output to leak. Third, the averaging and biasing capacitors, C_s, have a ratio of one half which aggressively pulls on the output. Last, the CMFB would update in phases when the output is not valid.

The averaging capacitors of the CMFB were increased in order to reduce the leakage at the output. With larger averaging capacitors, the ratio between the averaging and biasing capacitors has been reduced from one to one-tenth. This will lower the effect of the biasing capacitor on the output. The clocking of the CMFB has been changed to adjust the output common-mode while the output is valid.

5.5.7 Amplifier Bandwidth Challenges

The required unity gain bandwidth is derived from (5.22) resulting in (5.23). Solving τ, the settling time constant and the feedback factor β of the amplifier from (5.25) are used to determine ω_{bw}.

$$\tau = \frac{1}{\beta \varpi_{bw}} \tag{5.22}$$

$$\varpi_{bw} = \frac{1}{\beta \tau} \tag{5.23}$$

(5.23) is re-arranged in (5.24) to solve for τ. The variable T_s represents the time period available for the voltage to settle. This period is the clock period of

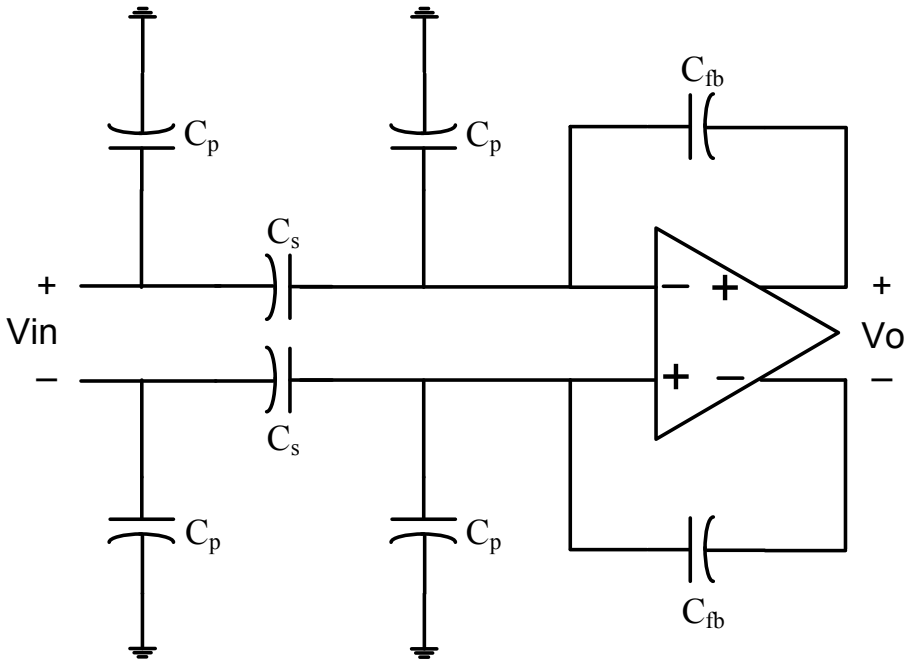


Figure 5.19 Integrator schematic showing the sampling, feedback and parasitic capacitor.

the switch capacitor sampling clock F_s. As shown in Fig. 5.19, feedback factor, β, is derivative from input and integration capacitor ratio.

$$\beta = \frac{C_{fb1}}{C_{fb1} + C_s + C_p} \tag{5.24}$$

There are four phase in each integration cycle of the integrator. During each phase the node voltages must settle within the determined error voltage of the desired value. With a sampling clock frequency of 262.144 kHz, the corresponding τ is equal to 238 ns.

$$Ts = \tau \ln(error) \tag{5.25}$$

$$\tau = \frac{-T_s}{\ln(error)} = 238ns \tag{5.26}$$

In order to determine the feedback factor, the capacitive network of the integrator is analyzed in Fig. 5.19. The sense capacitor C_s is the sensor and sampling capacitor of the interface integrator. The sum of the interconnect capacitances associated with this two-chip implementation is C_p. The integrating feedback capacitor is C_{fb}. From the integrator output back to the amplifier input is a capacitive divider representing the closed loop feedback factor of the amplifier as expressed in (5.26). Thus, β is 0.663.

The following two equations assume a parasitic capacitance C_p of 200 fF. The other capacitances C_{fb} and C_s are 25 pF and 12.5 pF respectively.

$$fugbw = \frac{1}{2\pi\tau\beta} = \frac{1}{2\pi \cdot 238 \times 10^{-9} \cdot 0.663} = 1.1MHz \tag{5.27}$$

The required amplifier bandwidths are extremely fast and difficult to meet with the *UMC 0.18 μm* processes. The feedback factor β is extremely small in this application. From (5.27) above, the large interconnect parasitic capacitances may affect frequency response. There are two negative effects on the amplifier requirements due to small feedback factor. The unity gain frequency bandwidth has been almost identified as shown in Fig. 5.20. The second is the closed loop gain of the amplifier is greatly reduced in Fig. 5.21. A reduction in loop gain has a detrimental effect of the amplifier's distortion and noise in the integrator. The amplifier's closed loop gain is shown depending on feedback factor in Fig. 5.22.

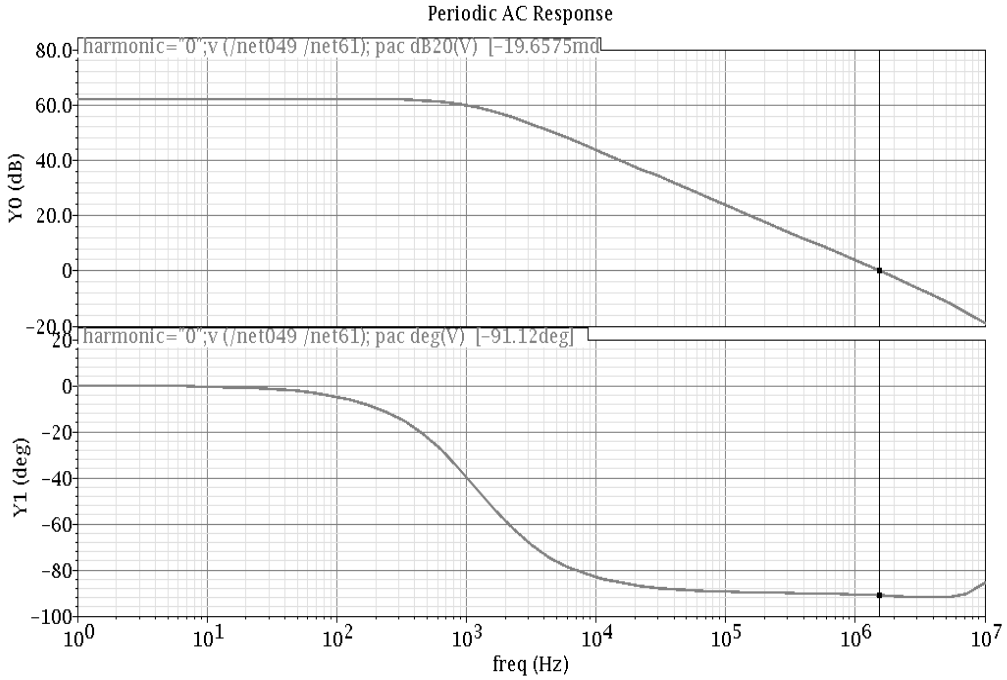


Figure 5.20 Open loop frequency response for the OTA.

From the open loop frequency response we can see that the DC gain is 63.2 dB and the unity gain bandwidth is 1.89 MHz with 89.1 phase margin. When determining the stability of a system, the closed loop which includes the feedback factor should be analyzed. Since the feedback factor is small, the closed loop frequency response is stable. This means that the 3 dB bandwidth is increased with feedback factor. Thus, the closed loop gain response is the open loop gain response multiplied by β. Since β is small, the open loop gain is shifted down lowering the gain and bandwidth but increasing the phase margin. This effect can be seen in Fig. 5.22 showing the closed loop response.

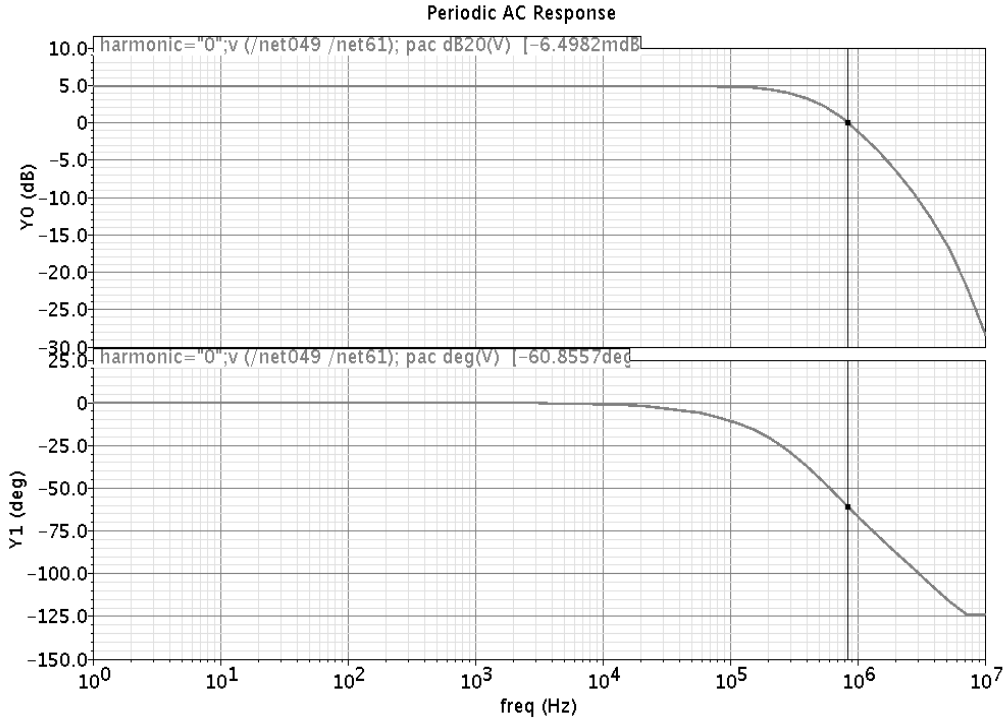


Figure 5.21 Closed loop frequency response for the interface amplifier.

5.5.8 Quantizer

The comparator is widely used in the process of converting analog signal to digital signals. In an analog-to-digital conversion process, it is necessary to first sample the input. Once, this sampled signal is applied to a combination of comparators to determine the digital equivalent of the analog signal. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. In its simplest form, the comparator can be considered as a 1-bit analog-to-digital converter. Hence, in the first order sigma delta modulator, the comparator (i.e. 1-bit analog-to-digital converter) acts as the quantizer.

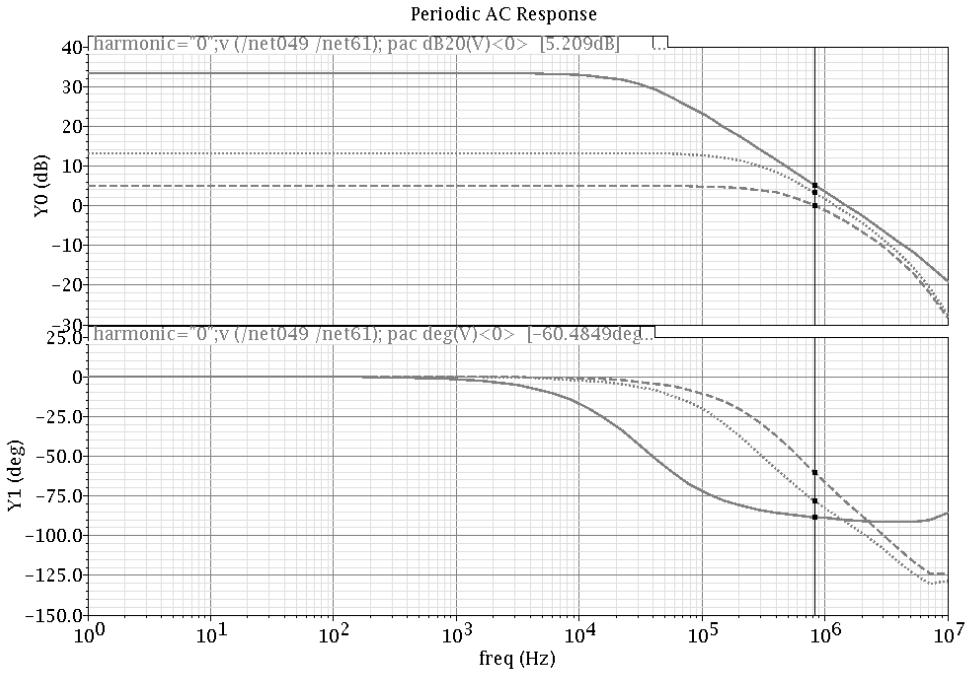


Figure 5.22 Closed loop frequency and open loop gain.

The quantizer inputs come from the differential outputs of SC integrator in ΣΔ modulator. The differential outputs of the integrator are compared resulting in digital output bit stream that modulates. The gain of a 1-bit quantizer is linear and self-adjusting within the loop of ADC. This is an advantage of 1-bit, two-level ADC’s. In multi-level quantizer case, the gain must be determined according to system stability requirements and implemented with adequate linearity.

To combine the sample-and-hold function and the comparator function and also to match speeds, a latched comparator is the best choice. Comparators are circuits which change the output state depending on the difference of the two input signals. A clocked comparator is used here to synchronize its operation with the other circuits in the ADC as they are run by high speed clocks. The schematic of the latched comparator is shown in Fig. 5.23 above.

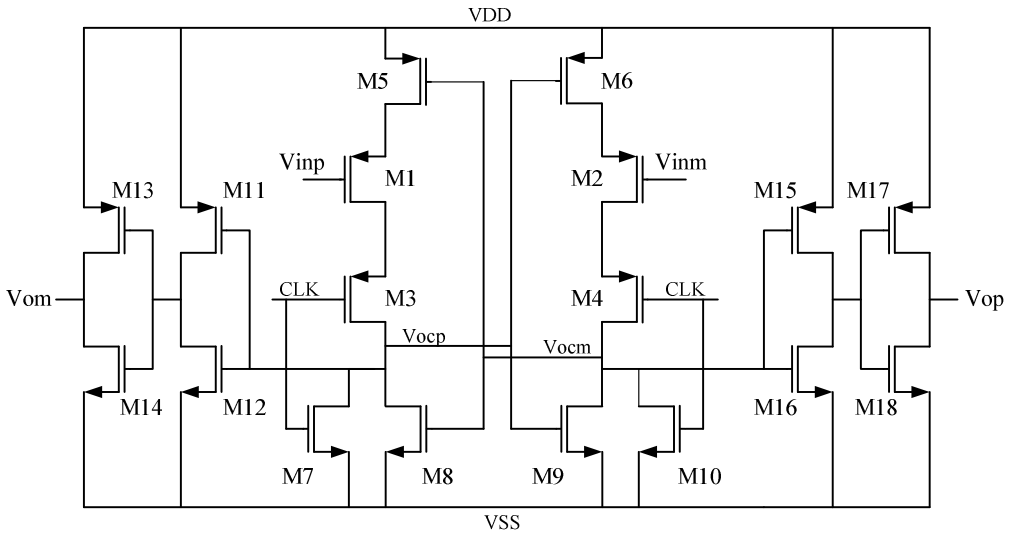
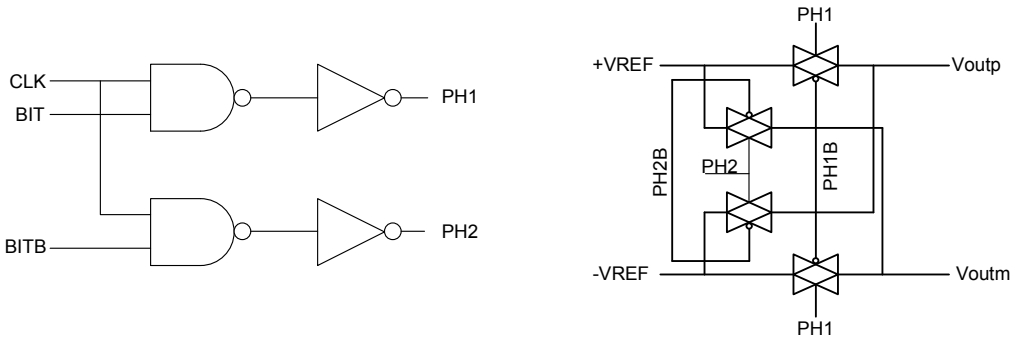


Figure 5.23 Comparator schematic implementing the single-bit quantizer.

As shown in Fig. 5.23, M1 and M2 are the input transistors which are connected to a feedback network formed by M5 and M6. M3 and M4 are control transistors. M8 and M9 form another feedback network for M7 and M10 which are pre-charge transistors used for refreshing the internal nodes when not in operation in order to reduce hysteresis. M11 to M18 form two inverters for each side which act as buffers to isolate the latch from the output load and to amplify the comparator output. During the pre-charge phase, i.e. when CLK goes high, transistors M3 and M4 are cut off and the comparator does not respond to any input signal. The voltages V_{ocp} and V_{ocm} will be pulled to the negative rail, V_{SS}, and the output of the inverters will be pulled to ground. During the comparison phase, i.e. when CLK goes low, both the voltages V_{ocp} and V_{ocm} drive V_{op} and V_{om} to opposite rails depending on the value of V_{inp} and $V_{inm.}$

In other words, a comparison, V_{inp} and V_{inm} are charged to the integrator output voltage. The CLK signal is high and creates a current path from V_{DD} to V_{SS} thereby grounding outputs, V_{op} and V_{om}, and resetting the comparator. When grounding the outputs of the comparator, a constant current consumption is present. When making a comparison, V_{inp} and V_{inm} are valid integrator outputs. The comparator reset signal CLK is released allowing the cross-coupled, positive feedback to drive V_{op} and V_{om} to opposite rails depending on the value of V_{inp} and V_{inm} from OTA output. If V_{inp} is greater than V_{inm}, V_{op} is pulled to V_{DD} and V_{om} is pulled down low.

In designing the W/L ratios of the transistors for the comparator, considerations have to be made for high speed operation. The delay of the whole comparator determines the fastest operation frequency of the comparator. For high-speed operations, the size of transistors M3 and M4 may be large enough so that their resistance values are minimal, but small enough to reduce the capacitance in order to have minimal comparator delay. The sizes of transistors M1 and M2 may be large enough to ensure quick response to the input signal, but small enough for minimal gate capacitances for high speed operation. The sizes of transistors M5, M6, M8 and M9 can be small enough for high speed operation, but large enough for quick regenerative action. In the inverter transistors pairs case, they are large enough for driving the output load to reduce the inverter delay, but small enough for minimal gate-capacitances to reduce the comparator delay.



(a) (b)

Figure 5.24 1 bit DAC with gate logic.

5.5.9 1 bit Digital-to-Analog Converter (DAC)

The comparator designed as shown in Fig. 5.23 will give an output of 1-bit digital input (BIT and BITB in Fig.5.24) to the DAC. The DAC converts the 1-bit digital signal to an analog signal and then feeds back to the switched capacitor integrator as shown in the block diagram of first order modulator of Fig. 5.9. Fig. 5.24 shows the transistor level schematic of 1-bit DAC. As seen the name 1-bit, the corresponding analog output will only have two levels is similar to the digital output. The 1-bit digital-to-analog converter (DAC) has two reference voltages as shown in Fig. 5.24: a positive reference voltage of $+V_{REF}$, and a negative reference voltage of $-V_{REF}$ between V_{DD} rail to V_{SS} rail.

The corresponding voltages of $+V_{REF}$ and $-V_{REF}$ are 1.5V and 0.3V in single supply voltage respectively. In case when the digital input is high, the DAC output will be the positive reference voltage, $+V_{REF}$. Otherwise, DAC output is $-V_{REF}$, respectively.

The quantizer used in this design is of 1-bit resolution hence the feedback DAC is also 1-bit in resolution. The 1-bit DAC can be implemented using a simple wire connected with the reference voltages. The advantage of a 1-bit DAC is that it is inherently linear. This linearity results in the output of the DAC being only two values ($+V_{REF}$ and $-V_{REF}$); therefore, no calibration or trimming is required.

5.5.10 Dither

It is well known that first order modulators produce tones. Dither is used to reduce the amount of idle tones [70]. There are two concerns when using dither. Dither must have a white noise type spectrum and must not saturate the quantizer. Dither is added prior to the quantizer. Therefore, the dither noise can be noise

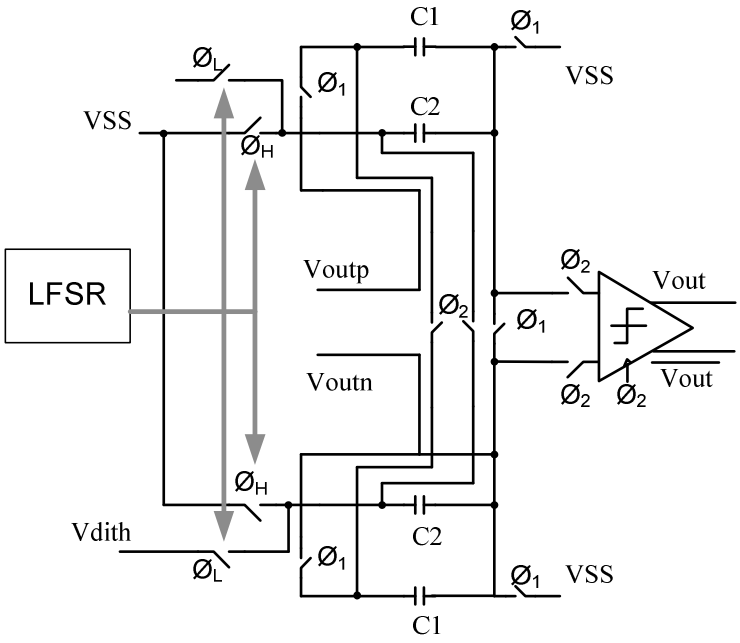


Figure 5.25 Implemented SC Dither Structure.

shaped along with the quantization noise [7]. Injecting dither into the integrator output is done with the structure shown in Fig. 5.25 [4]. One important point to make about this structure is the division of the difference between VINTP or VINTM and signal ground by two due to charge sharing when C1 and C2 are equal. However, the gain of the single bit quantizer will adjust as needed for the required loop gain. The disadvantage is the reduction in the differential integrator output voltage to be quantized. Switch control signals ϕ_L and ϕ_H are driven from a pseudo random number generator (RNG) with a linear feedback shift register as shown in Fig. 5.26. This pseudo RNG is used with the dithering controller to produce a white-noise property.

An on-chip Dither system can reduce test board area and complexity. The dither circuit on the AFE chip needs two phases in order to perform the dithering in Fig. 5.26. The single-bit, pseudo-random number generator was implemented using a Linear Feedback Shift Register (LFSR). The generated pattern will repeat every predetermined number of clock cycles according to the number of flip flops,

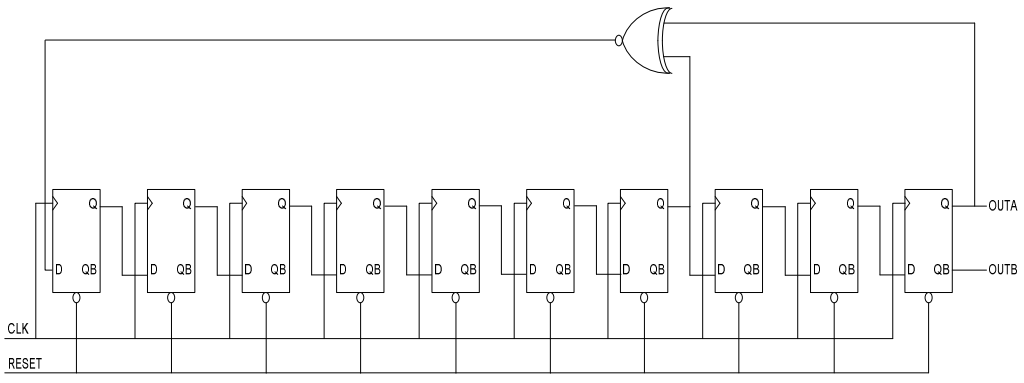


Figure 5.26 Single-bit pseudo RNG used for dither.

m, in the architecture [70]. This is known as the period of the generator. Equation (5.28) relates the number of D-flip flops in the RNG to its period

$$period = 2^m - 1 \tag{5.28}$$

where *m* is the number of D-flip flops (DFF). To produce the write noise by using them, 10 DFF are used. From this implementation, the switching pattern may repeat every 1023 cycles. In this project, a 262.1443 kHz master clock corresponds to a 65.536 kHz of RNG if there are four phases or master clock cycles per integration cycle. The RNG period is 1023 cycles multiplied by the

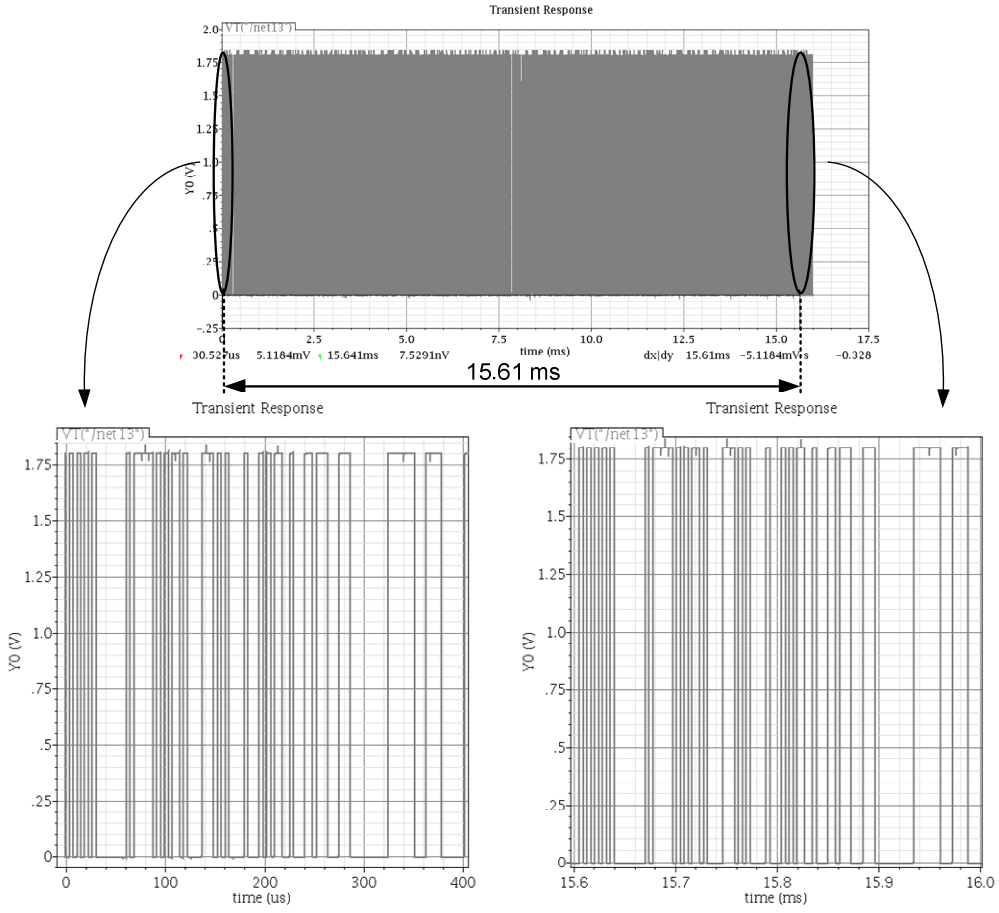


Figure 5.27 Implemented Dither simulation results.

period of one integration cycle, 15.26 μs. The total period a 15.61 ms period and corresponding frequency is 64.1 Hz. Fig. 5.27 shows the repetition signal every 15.61ms. The frequency 64.1 Hz is seen in the spectrum of the system when the dither is activated. The signal power depends on the dither voltage applied. Therefore, to avoid SNDR degradation, this frequency should not fall in the signal band of interest. For this implementation, the gas sensor signal band is DC to 32Hz. The simulation result shows that the signal from the random number generator repeats every 1023 cycles is provided in Fig. 5.27.

5.5.11 On-Chip Clock Generator

The clock generator for producing non-overlapping clock signals can be realized with a simple circuit constructed of logic gates. Such a circuit is shown in

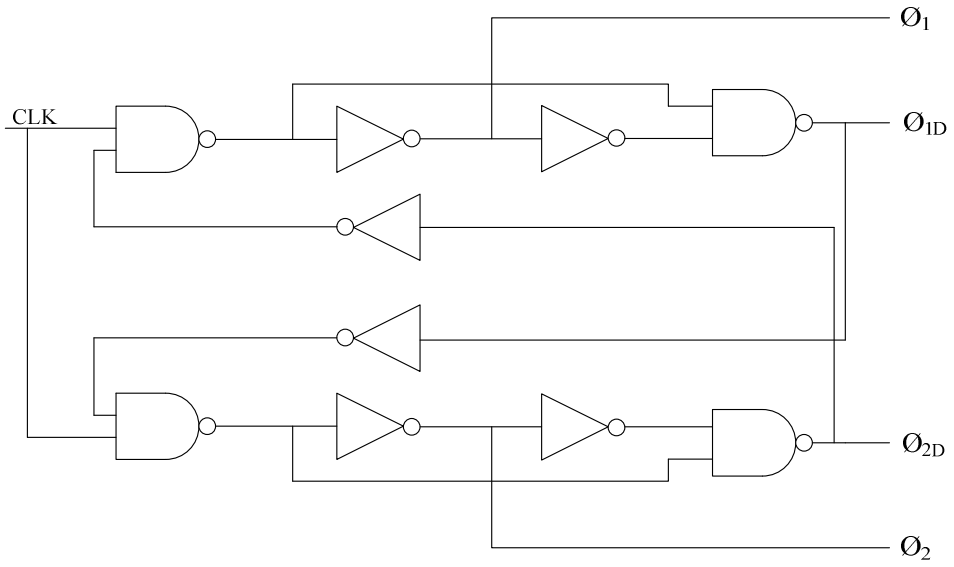


Figure 5.28 Non overlapping clock phase generator

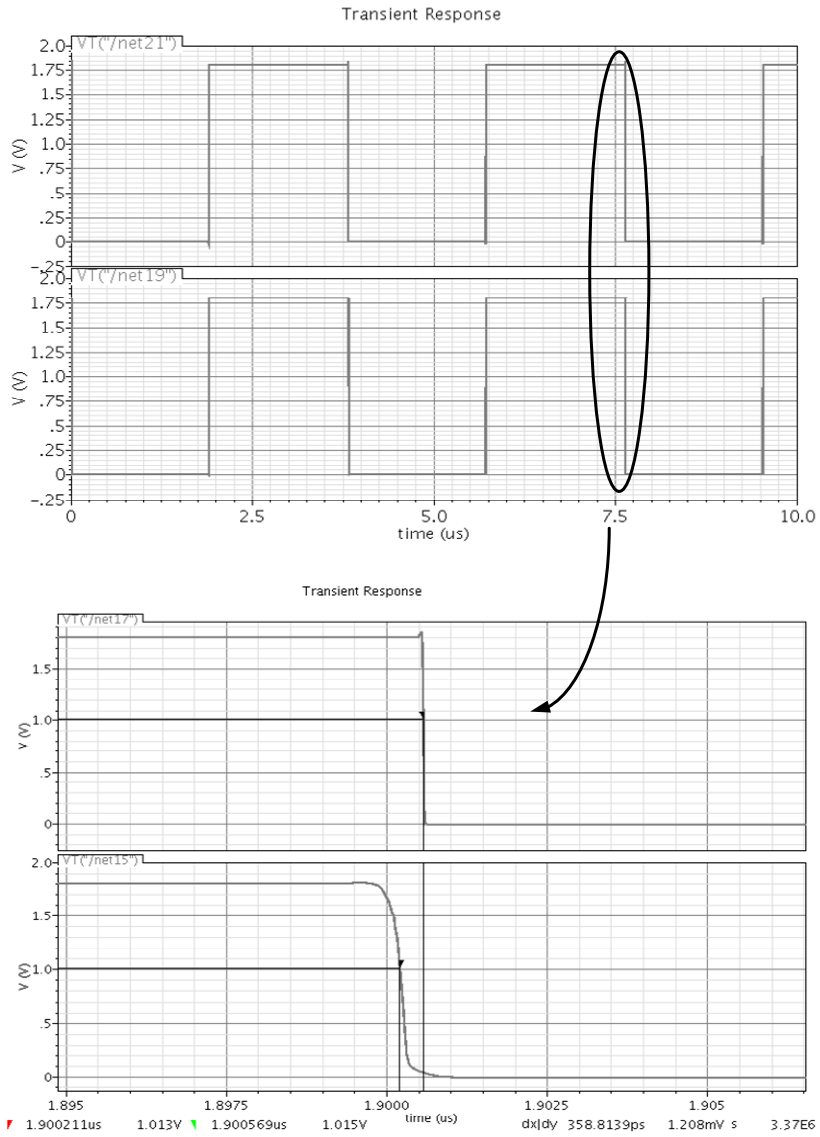


Figure 5.29 Output signal of non-overlap clock generator.

Fig. 5.28 [29], [31]. It consists of four NAND gates and six inverters. Complementary signals for the TG switches can be generated adding inverters subsequently. Further delayed clock can be produced by connecting six inverters again to one of the output clocks to produce its delayed clock. Thus,

complementary phase signals are taken one inverter after each phase and no compensation delay gate is needed to equalize the delay from the inverter. The expected timing diagram of clocks ϕ_1 and ϕ_{1D} (ϕ_1 delayed), ϕ_2 and ϕ_{2D} is shown in Fig. 5.29.

The main advantage of this circuit is its simplicity. At least a part of the buffering of output signals can be included in the delay elements, making the circuit quite robust. On the other hand, the non-overlap time often becomes larger than necessary because of the buffering included and the margin added to accommodate the process and temperature variations. The resulting speed penalty is emphasized in high clock rate circuits. Furthermore, the duty cycle of the generated clock signals is inherited from the input clock, requiring it to be close to 50%.

CHAPTER 6

EXPERIMENT RESULTS

The CMOS interface chip has been designed and fabricated in a 0.18 μm CMOS process. Fig. 6.1 shows a micrograph of the single-chip sensor system. The chip core area is 2.65x0.95 mm^2. The chip consumes 23.4 mW at a supply voltage of 1.8V for 16 sensor channels. The designed analog front end (AFE) has been packaged using a Quad Flat Package (QFP) 120-pin package type. In this chapter, the AFE chip measurement results will be presented.

The specific printed circuit board (PCB) in necessary for testing circuit designs especially for a low-power, high-resolution ΣΔ ADC which demands a low-noise environment. The layout of the PCB designed for the AFE test is shown in Fig. 6.2 and the 3D view for PCB is shown in Fig. 6.3. Two different settings are provided on the PCB.

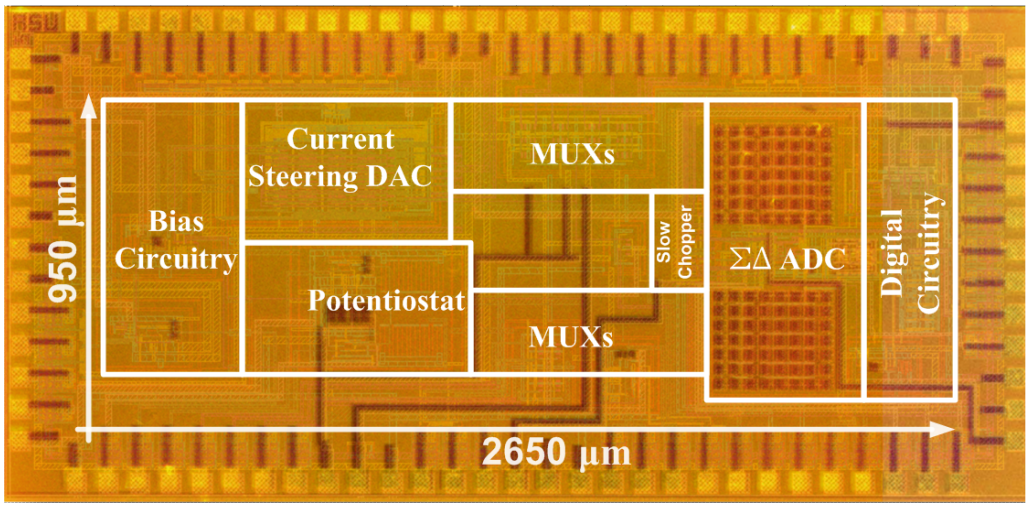


Figure 6.1 Micrograph of the analog front end IC for gas sensor system.

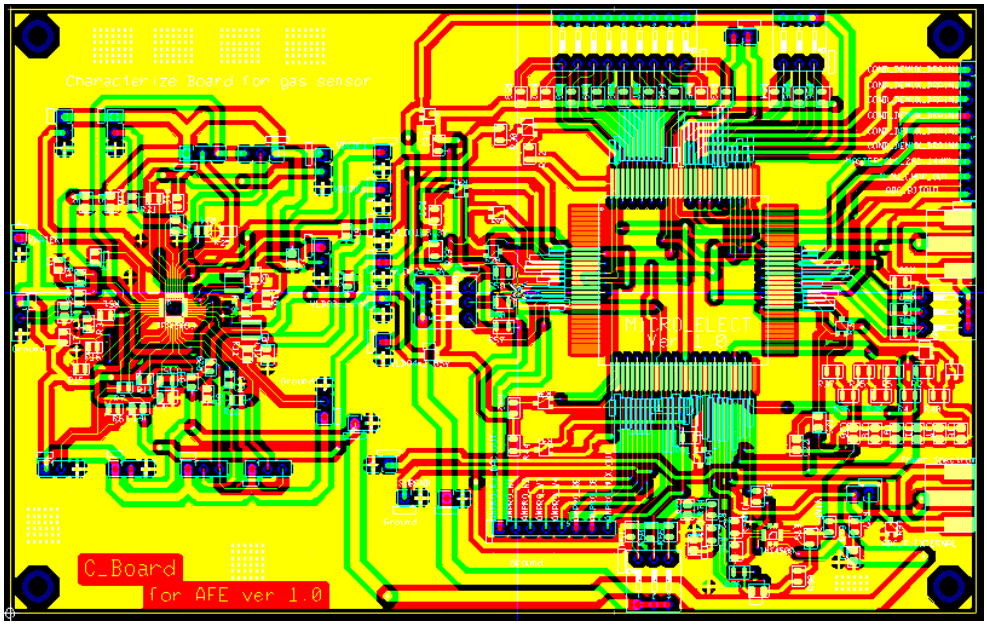


Figure 6.2 The PCB layout

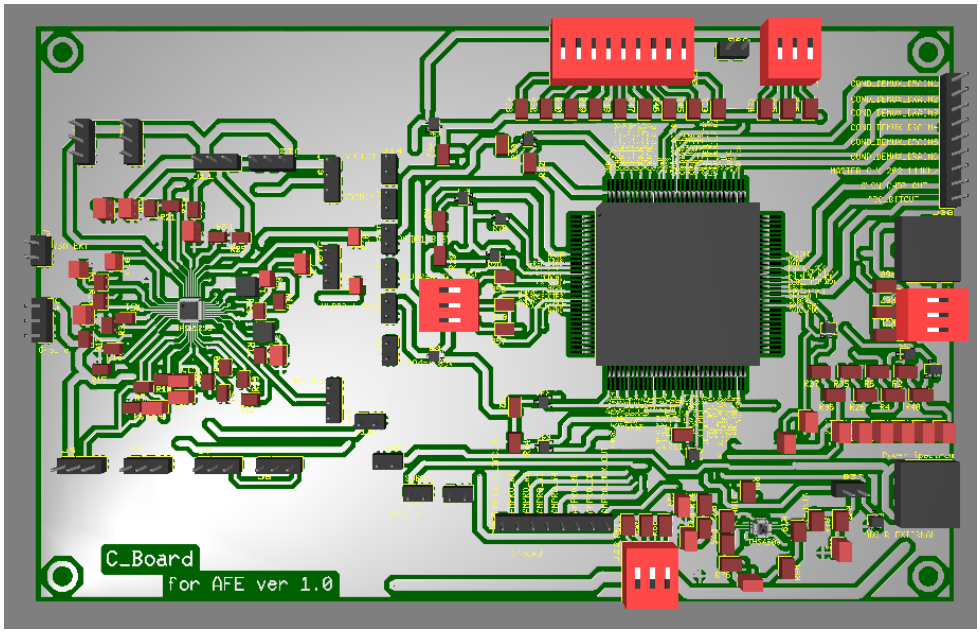


Figure 6.3 The PCB 3D view

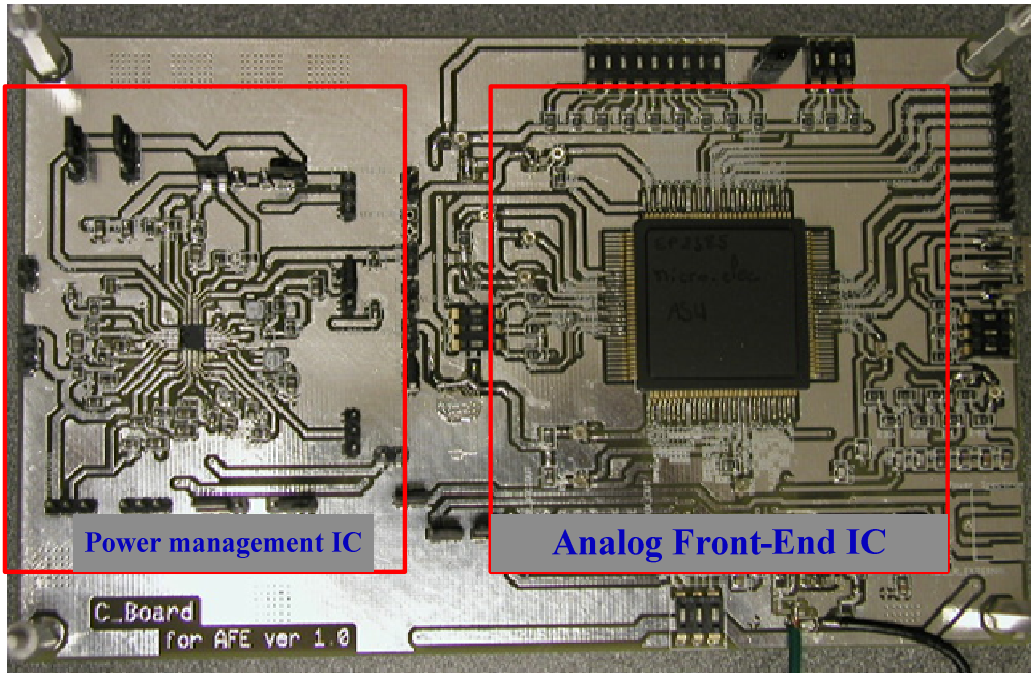


Figure 6.4 Photograph of the PCB for Testing AFE IC

The left side of the test board in Fig. 6.4 is a power management chip for mobile based module platform. The right side is the AFE IC in Fig. 6.4 shows a photograph of the PCB assembling discrete components.

Fig 6.5 shows the actual test setup for the testing of the AFE IC. The test setup was assembled from generic test-discrete components which resulted in a less than optimal configuration for testing the AFE IC. Noise in the test setup was a constant issue when taking measurements. There were two main components of noise in the system. The first component was noise picked up from the environment by the long wire or cable. The second component of noise was dominant and resulted from signals going through several cables and several connectors. Parasitic capacitors and inductors caused an excessive amount of

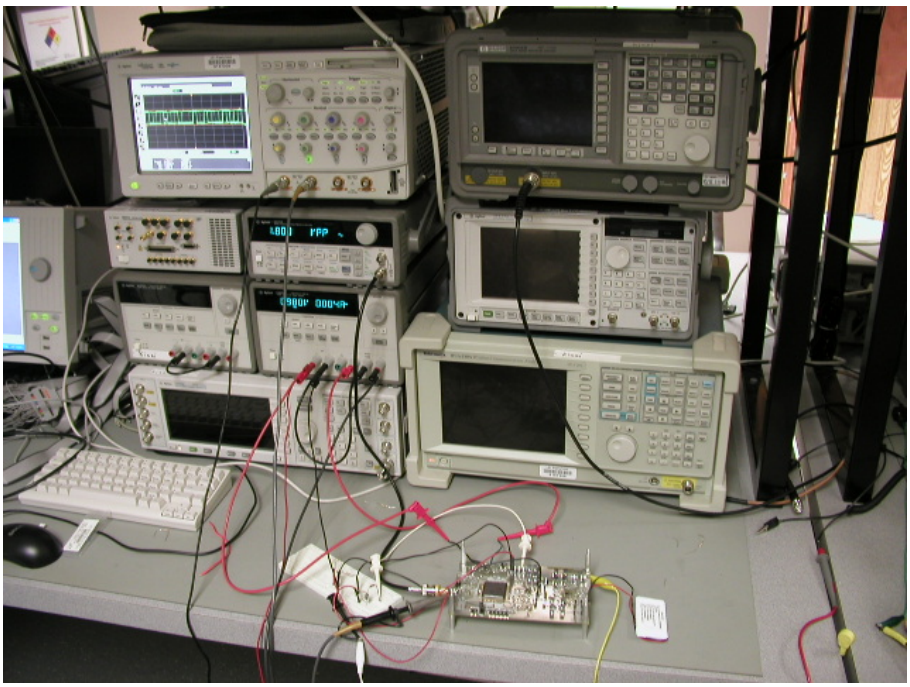


Fig. 6.5 AFE Test setup

ringing in the digital signal. Analog and digital sections used a common ground plane. The ground plane was implemented in double layers in PCB and connected to global ground in testing equipment. The ground viases were placed directly under the chip, making these visas a low resistance area, and ensuring that the analog and digital signals are referred to a common potential. The top was used mainly for analog signal traces. The second layer was a common ground plane. The top layer was broken into separate an analog power supply (AVDD) and a digital power supply (DVDD). All voltage references were generated using a Texas Instruments multi-regulator TPS65054. This includes all voltage supplies like AVDD, DVDD, VREF, VCOMMON, AVSS and DVSS. The output voltage from the power management IC can be adjusted by selecting the resistor ratio.

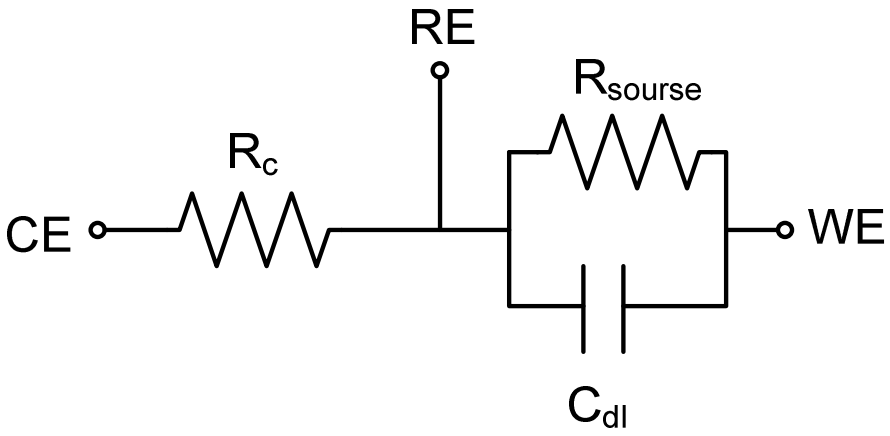


Figure 6.6 Equivalent circuit model for an amperometric sensor as R_c = 100 Ω, R_{source} = 10MΩ, 3.3MΩ and 1MΩ, C_{dl} = 10 μF.

6.1 Potentiostat Measurement

To test the potentiostat performance during the DC step operation, a fixed-value discrete test resistor was biased by the electrode potential drive block to create a current source. This current is presented as a faradic current source and this current was measured by the current readout interface to measure the potentiostat function. The test resistor was placed between the WE and RE/CE nodes in shown Fig. 6.6, and the small value resistor was placed between RE and CE in an electrolyte solution (*Note:* a possible option is to short the CE and RE electrode). Based on sensor analysis with a fitting sensor characteristic line, the control portion of the potentiostat was characterized by loading the circuit with a resistor (R_c = 100 Ω) between RE and CE and by placing a resistor (R_{source} = 10 MΩ) between RE and WE. Also, the stability tests of the potentiostat utilized an additional capacitor (Cdl = 10 μF) in parallel with the R_{source}. Fig. 6.7

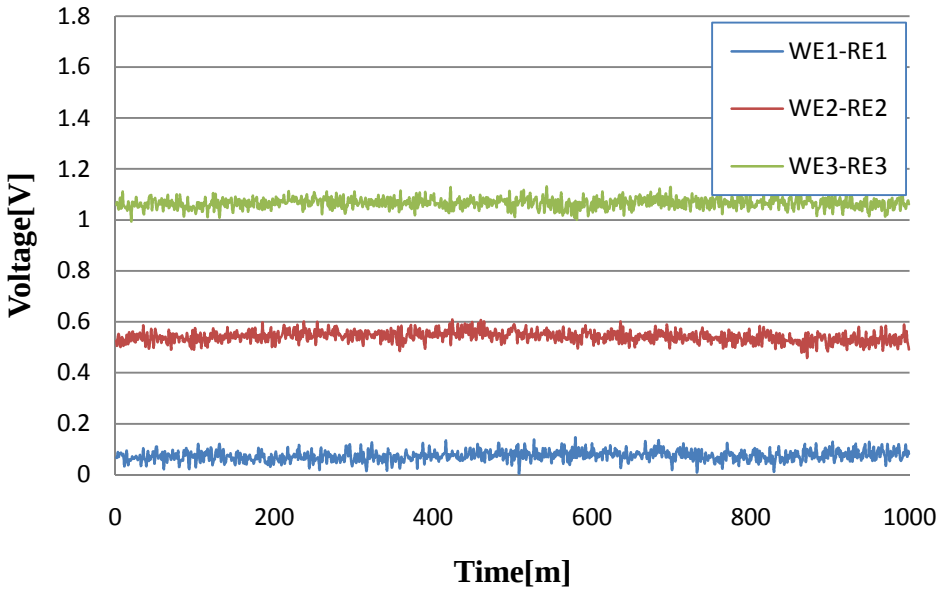


Figure 6.7 Measurement potentiostat functionality

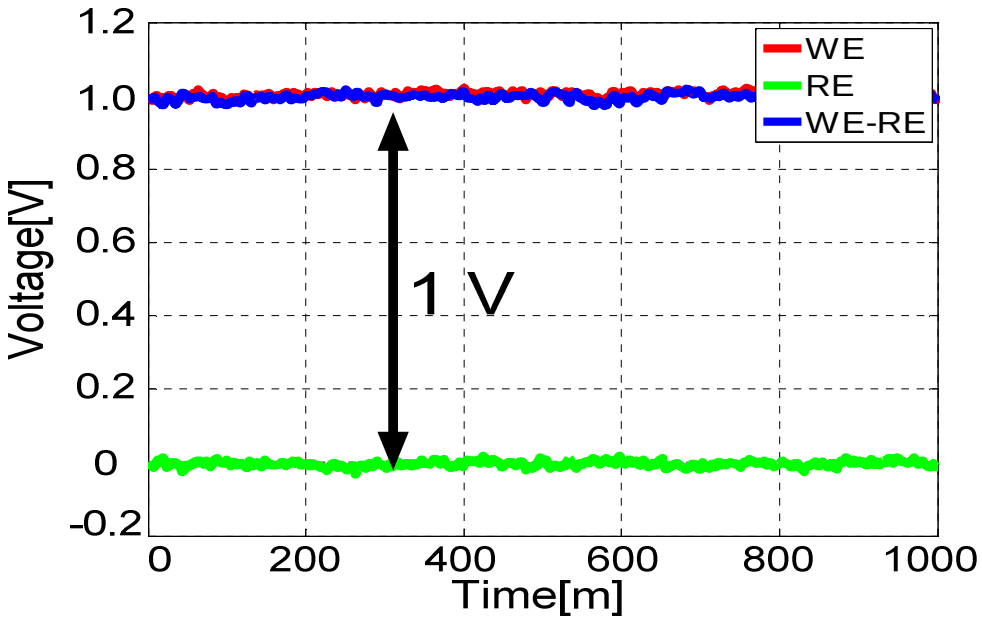


Figure 6.8 Results of the potentiostat

shows that the integrated potentiostat enforces a controlled constant potential between RE and WE to produce the desired perturbation for measuring and presenting current versus time. As shown in Fig. 6.7, the potentiostat can work as cyclic voltammetry because of keeping different voltage levels. Fig. 6.8 shows a typical constant voltage for amperometric sensor arrays to activate chemical reaction. The plot of the transfer function is close to unity as shown figure 6.8. In other words, V_{WE}-V_{RE} is properly transferred to the electrochemical sensor with on-chip electronics.

6.2 3 BIT RESISTOR STRING DAC MEASUREMENT

In this section, the 3-bit resistor string DAC measurement result is presented. Measuring 225mV of DC stimulus voltage with high accuracy is not easy because the voltage measurement fluctuates with amplitude larger than the

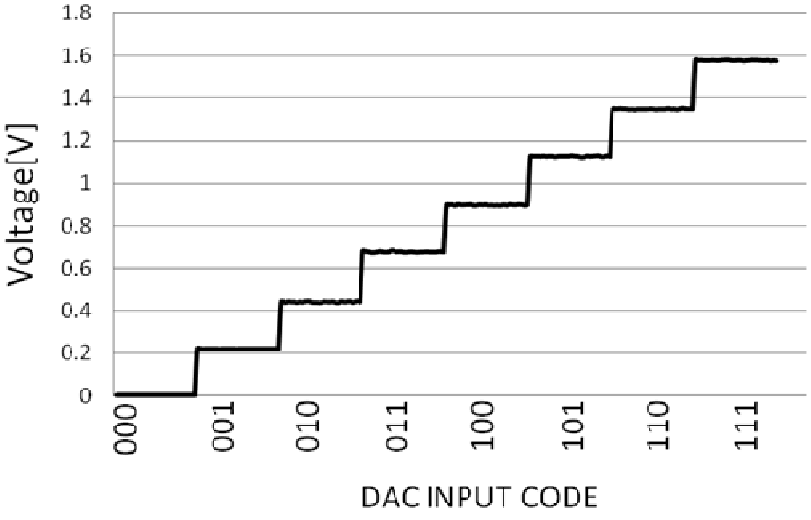


Figure 6.9 result of 3 bit resistor string DAC

desired accuracy due to the noise in the voltmeter. Therefore, the voltage value was integrated for at least 10 minutes and was divided by the length of the integration time. This method is a kind of moving averaging technique. Effectively, an average voltage from the DAC is calculated. A result of the 3-bit resistor string DAC is shown in Fig. 6.9. As shown in Fig 6.9, the 3-bit resistor string DAC is inherently monotonic. For this DAC, a reference voltage (VREF) is connected to one of the power management IC outputs with a buffer stage. The maximum DNL of the DAC is +0.026LSB/-0.013LSB while the maximum INL of the DAC is +0.005LSB/-0.028LSB. Fig. 6.10 shows the INL and DNL characteristic for the digital input code range. Because the DNL is kept below +/-0.5LSB, this DAC concludes that there are no missing codes.

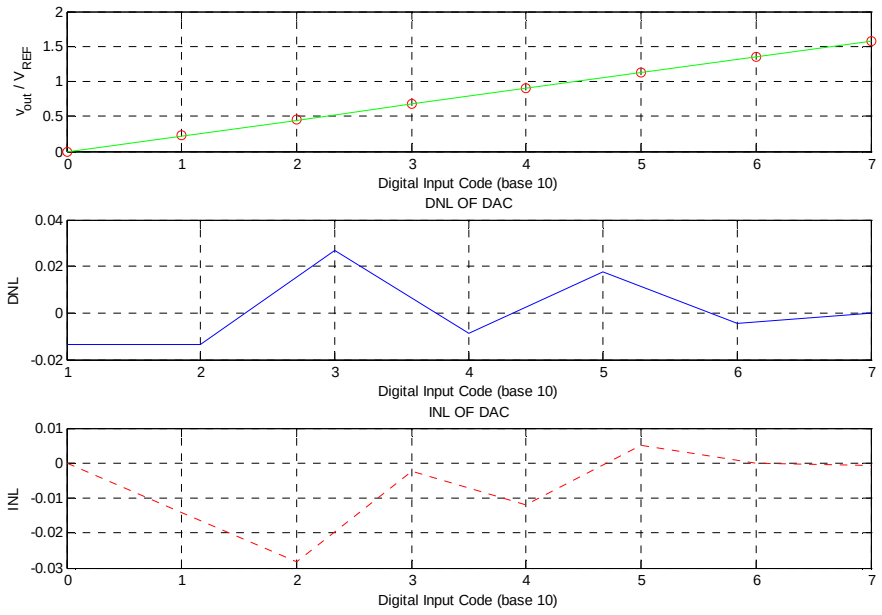


Figure 6.10 Measured DNL and INL of the 3-bit resistor string DAC

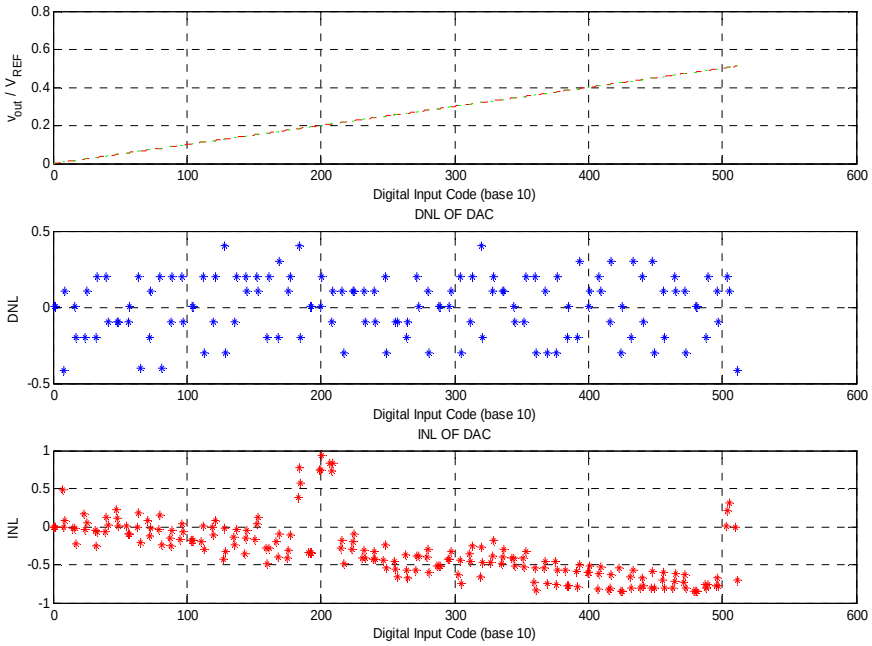


Figure 6.11 Measured DNL and INL of the 9 bit current string DAC

6.3 9-BIT CURRENT STEERING DAC MEASUREMENT

In this section, the measurement results of the 9-bit current steering DAC are discussed. First of all, to measure the current source, an ammeter is used with cables. Due to this set up, measuring 100 nA (1LSB) of current with high accuracy is not an easy task because the current measurement fluctuates with amplitude larger than the desired accuracy. Thus, to measure the current accurately, the current was integrated over time like the voltage measurement in the resistor string DAC, and then was averaged by the length of the integration time. The GPIB was connected to the NI data acquisition card (NI USB 6229). The LabView program controlled and received the current values in a function of time. Fig. 6.11 shows the current measurement result of the current steering DAC.

As can be seen from Fig. 6.11, the measured current follows the power of 2 at digital input code. To reduce the error rate, digital calibration is needed. The error can be up to 8% without calibration while the error can be down 2% below after calibration. The 1% physical reference resistors are used to do calibration in the DAC current source even though accuracy of reference resistors can become a possible error source. To check whether the accuracy limitation of the proposed calibration is mainly due to the reference resistors, other chips were tested. Based on the calibration, the DAC bias was kept the same as the previous chip to see the effect of chip-to-chip process variation. The maximum DNL of the DAC is +0. 0.402LSB/-0.420LSB while the maximum INL of the DAC is + 0.940LSB/-0.850LSB as shown in Fig. 6.9 In fact, the DNL is kept below +/-0.5LSB; thus, the 9-bit current steering DAC concluded that there are no missing codes.

6.4 ADC MEASUREMENT

The basic setup for the experimental testing is shown in Fig. 6.1. On the test circuit board the single-ended signal is converted to differential signal using LT1994 (LinearTech). The single-to-differential amplifier IC was built in PCB. The common-mode voltage of the test signal going into the ADC is set through 50 matching resistors connected to a voltage reference on the PCB. This common-mode voltage can be adjusted using a variable resistor but is nominally at half the supply or 0.9V. This voltage is bypassed to the board ground with a 10 μF capacitor. A 50% duty-cycle clock is generated by the Agilent 33120A function generator and Maxim DS1099 series. Both the ADC prototype and the 16802A

logic analyzer use this clock. The logic analyzer stores all the digital output codes including the slow chopper signal in an uncorrected format. The data is then down-loaded to a computer which provides the input of the digital decimation and low pass filters in MatLab. The correction can be implemented on-chip but die area and substrate noise would affect the AFE performances.

The linearity and noise performance of the converter can be characterized by a signal-to-noise-plus-distortion (SNDR) measurement. The SNDR is defined as the ratio of signal power to all other noise and harmonic power in the digital output stream. This characteristic determines the smallest signal that can be detected in the presence of noise and the largest signal that does not overload the converter. The dynamic linearity of the ADC was measured by analyzing a Fast-

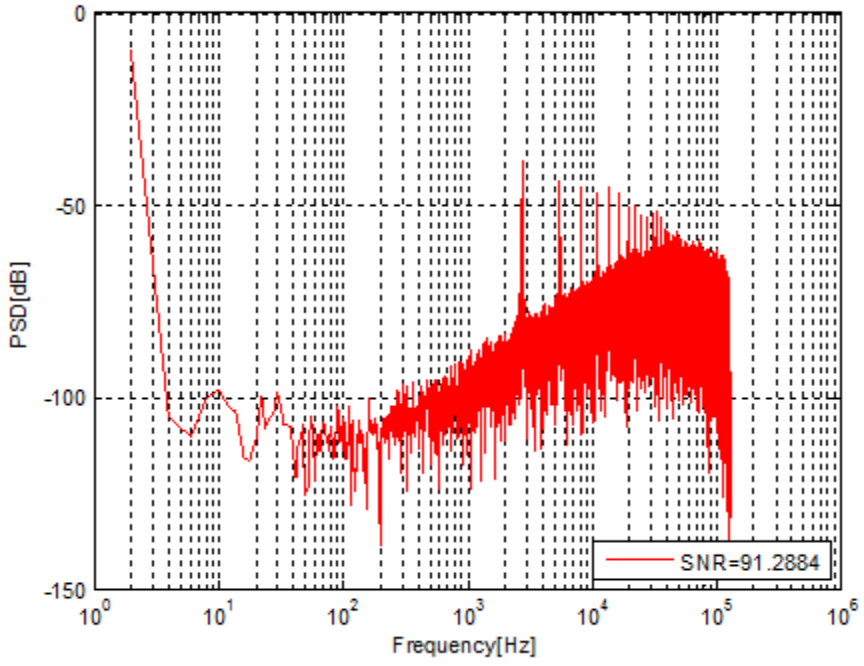


Figure 6.12 PSD of 1st order ΣΔ ADC without the slow chopper

Fourier-Transform (FFT) of the output codes for the single input tone using a Hanning window in MatLab. The peak SNR for a 1Hz DC input with 32Hz bandwidth was measured at 91.2 dB with a clock frequency of 262.144 kHz in Fig. 6.12.

The modulator was characterized by configuring the AFE to record the modulator single- bit stream output. Fig. 6.13 plots SNR and SNDR versus input voltage with dB scale referring to 1.2Vpp. The dynamic range is around 91dB. The results of this measurement imply that physical separation of analog and digital circuits, dedicated analog supply pins, and judicious deployment of analog substrate contacts provide adequate protection for analog circuits. The input signal amplitude was set to 1.2V of full scale and the modulator operating

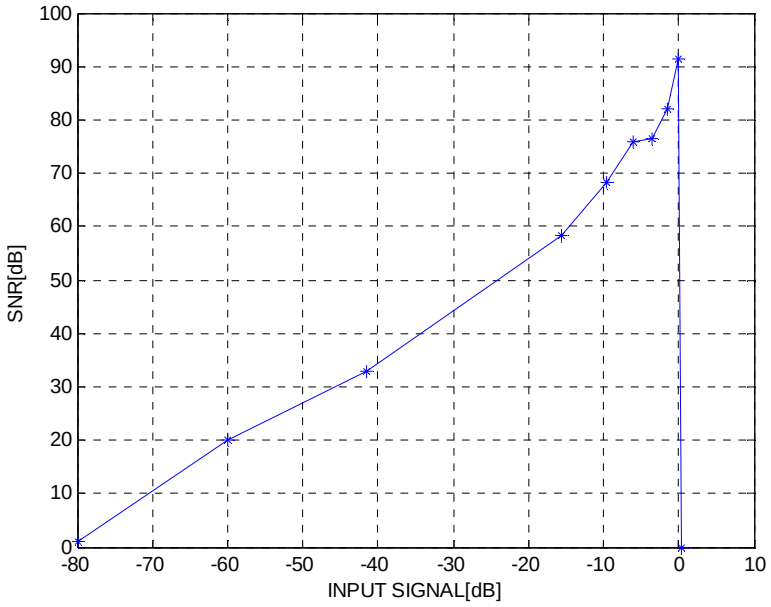


Figure 6.13 SNR vs. Input Signal Level

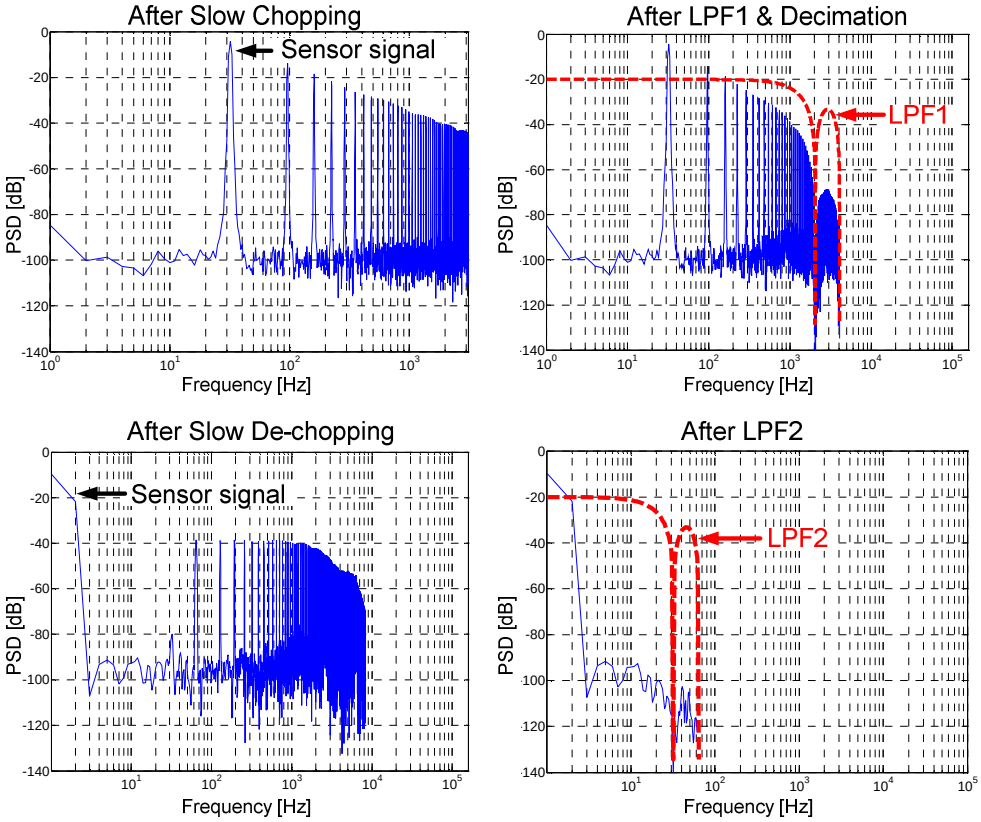


Figure 6.14 Measured PSD of the nested chopped ΣΔ ADC at each critical point.

frequency was 262.144 kHz, which gives a conversion rate of 32 Hz at an oversampling rate of 4096.

Fig. 6.14 shows the 65536-point FFT plot of the ADC output read. The measured resolution can be limited by the performance of the external signal generator when the ADC is tested. As seen in Fig. 6.14, the nested chopper ΣΔ ADC pushes offset and 1/f noise to high chopper frequency. In Fig. 6.15, the DC offset reduction due to nested chopping is shown. With slow chopping enabled, almost 500 μV offset is suppressed at DC.

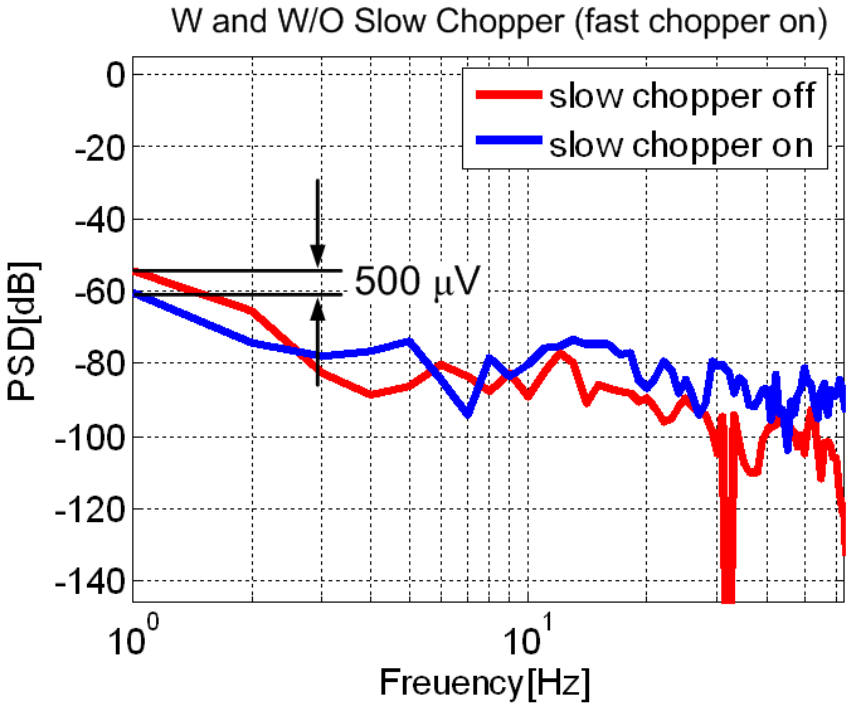


Figure 6.15 Offset reduction with slow chopper vs. no chopping

Table 6.1 and 6.2 show the specification of the two types of sensors and the main circuit specification using a single poly, 6-level metal 0.18-μm CMOS process. The differential amplifier for the ADC has a 68.2 dB DC gain and the class AB amplifier for resistor string DAC has 86 dB DC gain. The total power consumption is expected to be around 23.4 mW for 16 sensors. The chip core area is 2.65x0.95 mm^2. The AFE IC achieves is 91 dB SNR.

Table 6.1 Measured results of AFE and Electrical performance summary

Analog Front End IC	
Technology	0.18 μm CMOS, 1 poly 6 metal layers
Die size	2.65mm x 0.95 mm
Power consumption	23.4 mW (1.8V supply)
Resistor string DAC	DNL (+ 0.026/-0.012 LSB)/ INL(+0.005/-0.028 LSB), power(402.7 μW with class AB amp)
Current steering DAC	DNL (+ 0.402/-0.42 LSB)/ INL(+0.941/-0.808 LSB), power(93.6 μW)
Slow chopping freq/ Fast chopping freq.	32 Hz/131.072 kHz
System Input Referred Offset	500 μV
System Dynamic range	91 dB
Chemical Measurement Sensitivity	< 5 ppm
Amperometric Readout Range	10 nA-100 μA
Amperometric Readout Accuracy	< 0.05%
Conductometric Readout Range	10 kΩ-10MΩ
Conductometric Readout Accuracy	< 0.05%

Table 6.2 Sensor specification

Sensor Array	
Array size	2 cm x 2 cm for conductomeric sensor 10 cm x 10 cm for amperometric sensor
Number of channel	16 channels (Conductometric sensor: 8, Amperometric sensor : 8)
Electrode spec	Cr/Au (20/180 nm) on SiO2/Si substrates for conductometric sensor, thick carbon film with 1.25 Ag/AgCl for amperometric sensor

6.5 MINIATURE PLATFORM MODULE

The badge-style sensor platform module is shown in Fig. 6.16. The 4 layer PCB containing two multi-sensor chips has been assembled into a handheld application specific sensor system which additionally includes a microcontroller board (signal processing unit), a power management board with li-ion battery and a miniaturized gas-flow system developed by the University of San Diego and River side. The platform size is 65mm x 65mm x 23mm, (width, length and height). Fig. 6.16 shows a photograph and a schematic of the module platform. The module has a real conductometric sensor chip and an amperometric sensor chip on the top layer. To test circuit performance more during faradaic current change depending on gas concentration, a discrete test variable resistance was biased by the electrode potential drive block to create a current source. This

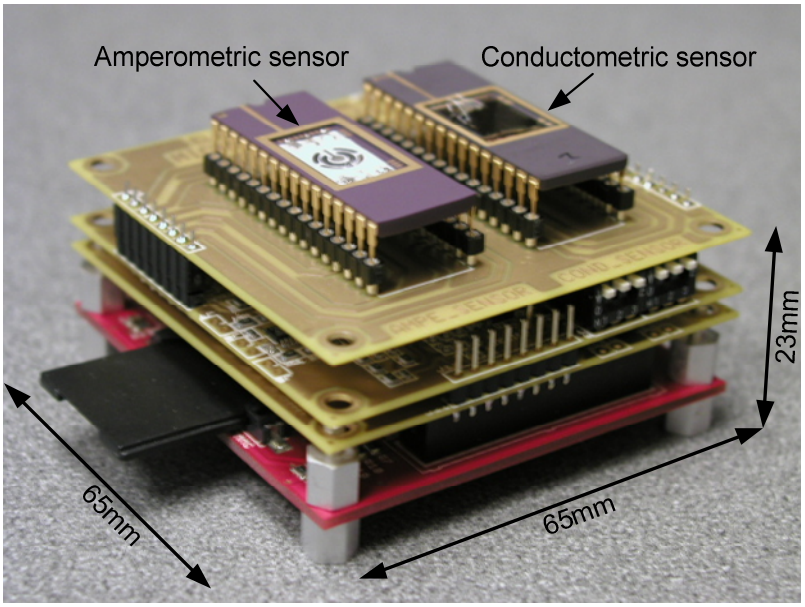


Figure 6.16 CMOS platform for gas sensors.

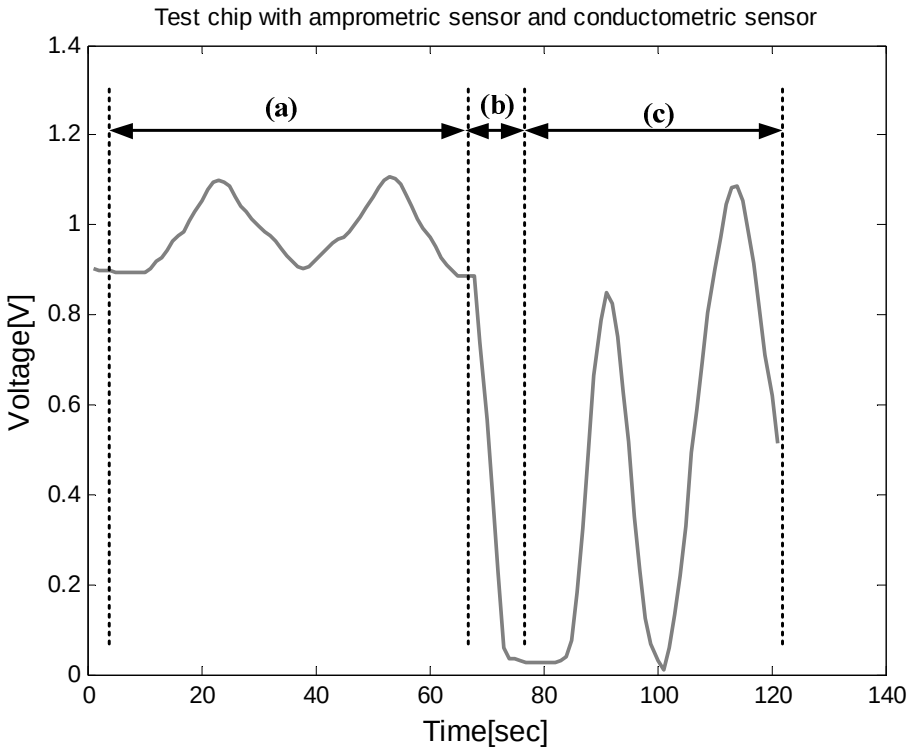


Figure 6.17 Result of testing platform (a) transient response for amperometric mode (b) interval change mode (c) transient response for conductometric mode

current was measured by an on-chip current readout block to record the potentiostat transfer function. The variable resistor was placed between the WE and RE nodes as R_{source} in Fig. 6.6. Also, the change in the conductometric sensor was tested as a variable resistance. Based on this setup, the AFE IC was tested. The change of the resistance and current convert input signal in the low-power tiny micro controller. In fact, the signals coming from the multi sensor chips are processed and evaluated by the MSP430 microprocessor (Texas Instruments). The sensor data are stored in tiny flash memory. To readout sensor data in tiny flash memory, WinHex program was used. After reading them, the data are transmitted

to a personal computer for post-signal processing. To do post-signal processing, MatLab was used to implement the decimation filter and the low-pass filter. Fig. 6.17 shows the results from the sensor platform module. In Fig. 6. 17, region (a) is presents the amperometric sensor output. As seen in (a), the graph shows that only oxidation happened over common mode voltage. When a change mode switch turned on, the common mode region went to a voltage which results in a chemical reaction with a conductometric sensor. Region (c) shows the conductometric sensor output. When the resistance of the conductometric sensor was changed, the output voltage of the sensor was changed.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

A 0.18-μm CMOS electrochemical analog front-end (AFE) circuit designed for a 16 channel air quality monitoring system is presented in this thesis. The AFE circuit for diesel and gasoline sensors can replace currently-used, expensive instruments that measure electrochemical reaction results. The circuitry consists of an integrated CMOS potentiostat, a low-noise current-to-voltage converter, a low noise instrumentation amplifier, a current steering DACs and a first-order nested ΣΔ ADC for the conductometric and amperometric sensor arrays. This thesis presents the first demonstration of bringing together conductometric sensor and amperometric sensor and CMOS technology.

To adaptively control the DAC current, the DAC control can be elaborated, which is not suitable for low-power applications. This thesis proposed a segmented 9-bit DAC scheme. The DAC can provide binary multiples of LSB current source. In addition, the DAC current should be maximized while meeting the DAC headroom constraint. This scheme considerably decreased the complexity of the DAC control.

In bio-chemical sensor applications, large spreads of base resistance in conductometric sensors and large spreads of current in amperometric sensors pose the greatest challenge to the gas detection system. Thus, several innovations have been made to design a stable AFE system, and the proposed techniques were verified with a prototype CMOS interface chip. Several contributions and possible improvements are delineated below. The architecture is also sampling-rate

scalable; by duty-cycling the system, a linear power scaling is achieved. To reduce residual offsets at low frequency noise that come from clock feed through mismatches and integrator mismatches, the nested chopper technique is implemented. A full signal chain is simulated with actual electrochemical reactions data from the amperometric and conductometric sensors. This chip implements a 16-bit ΣΔ ADC to measure the voltage that is generated by the 9-bit current steering DAC and sensors as well as the voltage generated by 3-bit resistor string DAC and potentiostat. The proposed design is fabricated and tested for the physical conductometric and amperometric sensors to detect diesel and gasoline exhaust.

The main contribution of this thesis is the design of low-noise, low-DC offset and energy-efficient CMOS interface circuitry for gas sensor arrays. Although most chemical sensor measurements are likely to be in a very low frequency or DC domain, there are several challenges associated with a single-chip based sensor readout system. To determine the effective dynamic range required in the base resistance change, the smallest resistance change that needs to be resolved in conductometric sensor has to be determined. Furthermore, amperometric sensor arrays suffer from the op-amp offsets and the 1/f noise in a standard CMOS potentiostat. To resolve this problem, larger devices and PMOS input pairs are used to design the system. Because of these problems, it is difficult to achieve small area, low power consumption and low noise in an analog front-end IC. To reduce die area and power dissipation in this system, a shared and reusable high resolution sigma delta ADC, a predetermined current steering DAC,

and an integrated potentiostat are used. To get more detection sensitivity, the sigma delta ADC in discrete domain was designed for a very wide dynamic range and high accuracy when power consumption is spent more. Thus, this system attempts to trade-off power consumption and resolution to increase the detection range for hazardous chemical gases. More and more, CMOS switched capacitor design can suffer from the DC offset and 1/f noise of the op-amp and especially residue offset from both chopper switches and CMOS switches; as such, the nested chopper technique is applied to the ADC because sensor signals are at very low frequencies.

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