Self Resonant Third Harmonic Mixer For 60 GHz Transmitter

by

Todd Jeffrey Martino

A Thesis Presented in Partial Fulfillment
of the Requirements for the Degree
Master of Science

Approved November 2010 by the
Graduate Supervisory Committee:

Sayfe Kiaei, Chair
Bertan Bakkaloglu
James Aberle

ARIZONA STATE UNIVERSITY

December 2010

ABSTRACT

Ongoing research into wireless transceivers in the 60 GHz band is required to address the demand for high data rate communications systems at a frequency where signal propagation is challenging even over short ranges. This thesis proposes a mixer architecture in Complementary Metal Oxide Semiconductor (CMOS) technology that uses a voltage controlled oscillator (VCO) operating at a fractional multiple of the desired output signal. The proposed topology is different from conventional subharmonic mixing in that the oscillator phase generation circuitry usually required for such a circuit is unnecessary.

Analysis and simulations are performed on the proposed mixer circuit in an IBM 90 nm RF process on a 1.2 V supply. A typical RF transmitter system is considered in determining the block requirements needed for the mixer to meet the IEEE 802.11ad 60 GHz Draft Physical Layer Specification. The proposed circuit has a conversion loss of 21 dB at 60 GHz with a 5 dBm LO power at 20 GHz. Input-referred third-order intercept point (IIP3) is 2.93 dBm. The gain and linearity of the proposed mixer are sufficient for Orthogonal Frequency Division Multiplexing (OFDM) modulation at 60 GHz with a transmitted data rate of over 4 Gbps.

ACKNOWLEDGMENTS

I offer my sincere thanks to my research advisor, Professor Sayfe Kiaei, for his guidance on this project. His perspective and his outlook on this work have been as encouraging as they have been instructive.

My project benefited greatly from endless technical discussions with Dr. Tino Copani. His research acumen and intuitive understanding of RF circuits proved invaluable in focusing this work, and for that I am very grateful.

My thanks also go to Professor Bertan Bakkaloglu and Professor James Aberle for serving on my committee and providing excellent instruction and advice in and out of various classrooms.

Finally, I would like to acknowledge my mother for her undying support and her unwavering confidence in my pursuits.

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CHAPTER 1

Introduction

Recent openings of unlicensed 57-64 GHz spectrum worldwide have spurred widespread research in millimeter wave systems and circuits. The approximately 7 GHz now available around 60 GHz in many countries worldwide promises ample bandwidth for short range, high throughput applications such as uncompressed high definition video.

The use of highly efficient modulation schemes such as Orthogonal Frequency Division Multiplexing (OFDM) requires that every block in the transmit chain maintain a high degree of linearity. Such modulation schemes are essential to provide the raw data throughput required for operation in this band.

This thesis will focus on frequency and system implementation issues for a third harmonic self resonant upconversion mixer at a radio frequency (RF) of 60 GHz. The ability of this circuit to mitigate challenges in voltage controlled oscillator (VCO) design in the mm-wave realm is described. This circuit is presented in the context of a transmitter suitable for operation under the IEEE 802.11ad draft physical layer specification. This document, which remains a work in progress, describes a standard for 1-7 Gbps wireless communications over a 10 meter range. It maintains backwards compatibility with older 802.11 standards (i.e., WiFi) and is expected to interoperate with

those networks at 2.4 and 5.2 GHz [1].

Scope

Mixer design for 60 GHz presents significant challenges. Active mixers with high conversion gain are desirable to maximize transmitted power in light of high path loss, but are power hungry. High data rate transmission often calls for complex modulation schemes, such as orthogonal frequency division multiplexing (OFDM), that place tighter constraints on transmitter error vector magnitude (EVM).

In order to satisfy these requirements, certain design requirements must be considered. First, the need for low transmit EVM imply that linearity and spectral purity are to be considered. Next, the mixer must have the highest possible conversion gain to make up for adverse channel conditions. These factors must be balanced against the need for a low power budget.

Thesis Contents

This thesis presents the design of a third harmonic active mixer in a 90 nm RF CMOS process. First the transmit specification is examined and used to develop circuit requirements. Next, the proposed third-harmonic mixer is presented and analyzed. Finally, simulation results are presented to validate circuit performance.

CHAPTER 2

Design Specification

Transmit Requirements

At present the 60 GHz design arena is a patchwork of different competing draft standards. The proposed mixer is designed using the guidelines contained in the IEEE 802.11ad draft physical layer specification. This standard supports 60 GHz transmission over a minimum of 10 meters by using beam forming methods combined with OFDM, single carrier (SC), or low-power SC.

The transmitter should have the characteristics given in Table I and adhere to the system mask shown in Fig. 1.

TABLE I
Transmitter PHY Specification for IEEE 802.11ad Draft [1]

Frequency range	56-66 GHz
Number of channels	4
Channel bandwidth	2.16 GHz
Minimum transmit range	10 m
Max EIRP	40 dBm average/43 dBm peak

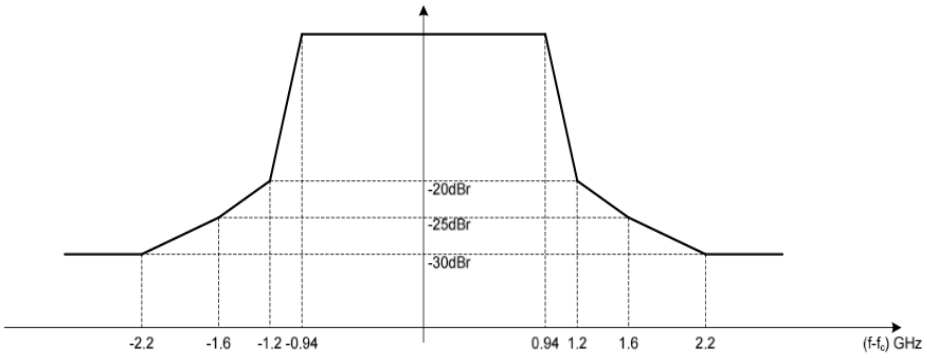

Fig. 1. Transmit mask for 802.11ad draft specification.

At present the 802.11ad draft specifies few requirements for overall transmitter linearity. At time of writing, the most crucial of these are the transmit EVM requirements for each corresponding modulation coding scheme (MCS), which are reprinted in Table II.

Table II
MCS, EVM and Data Rates in IEEE Specification [1]

MCS Index	**Modulation**	**EVM Value [dB]**	**Data Rate [Mbps]**
13	SQPSK	-7	693.00
14	SQPSK	-9	866.25
15	QPSK	-10	1386.00
16	QPSK	-11	1732.50
17	QPSK	-13	2079.00
18	16-QAM	-15	2772.00
19	16-QAM	-17	3465.00
20	16-QAM	-19	4158.00
21	16-QAM	-20	4504.50
22	64-QAM	-24	5197.50
23	64-QAM	-24	6237.00
24	64-QAM	-25	6756.75

Mixer Design Requirements

In order to assess the mixer circuit's requirements, simulations were performed in Agilent Advanced Design System (ADS) to assure that EVM and transmitted spectrum requirements were met. The test bench uses WLAN signal generators to replicate the various modulation schemes, including OFDM, used in the 802.11ad specification. Based on whether specification requirements are met, the target specification for the mixer can be revised and necessary phase array accuracy can be determined.

The signal chain under test includes an IF amplifier to model additional required gain and mixer nonlinearity, an ideal upconversion mixer, as required for the simulation setup, and a power amplifier (PA) based on a design reported by Voinigescu, et al. [2] The PA model has a gain of 5 dB at 61 GHz, an output 1 dB compression point of 6.4 dBm, and a saturated output power of 9.3 dBm. Note that the IF amplifier is only used to simulate both mixer behavior and additional signal preamplification. The preamplifier gain is assumed to be 9 dB, a value that is both achievable and enables the circuit to be made highly linear; thus only the nonlinearity of the mixer and the PA are considered.

Given that 60 GHz designs in CMOS are notorious for poor conversion gain, the design of the mixer circuit is instead focused on low power consumption and simplicity of the overall system. Having

determined the characteristics of the other blocks in the signal chain, the test bench is simulated with estimated values for the mixer. The estimated mixer parameters assume a conversion gain of -20 dB, an IIP3 of 1 dBm and input-referred 1 dB compression point (IP1dB) of -9.6 dBm. The results for transmit EVM appear in Fig. 2.

Index	EVM	RMS
30	11.12633577	-19.07295676
31	11.11795607	-19.07950092
32	11.13392756	-19.06703218
33	11.14067771	-19.06176779
34	11.16023927	-19.04652989
35	11.16350693	-19.04398707
36	11.17281919	-19.03674459
37	11.18671928	-19.02594520
38	11.18903902	-19.02414423
39	11.19025084	-19.02320356
40	11.17987748	-19.03125912
41	11.16437047	-19.04331521
42	11.17256709	-19.03694058
43	11.16216420	-19.04503187
44	11.16862155	-19.04000850
45	11.15263609	-19.05244937

Fig. 2. EVM results from ADS simulation.

The transmitted spectrum and mask requirement are shown in Fig. 3.

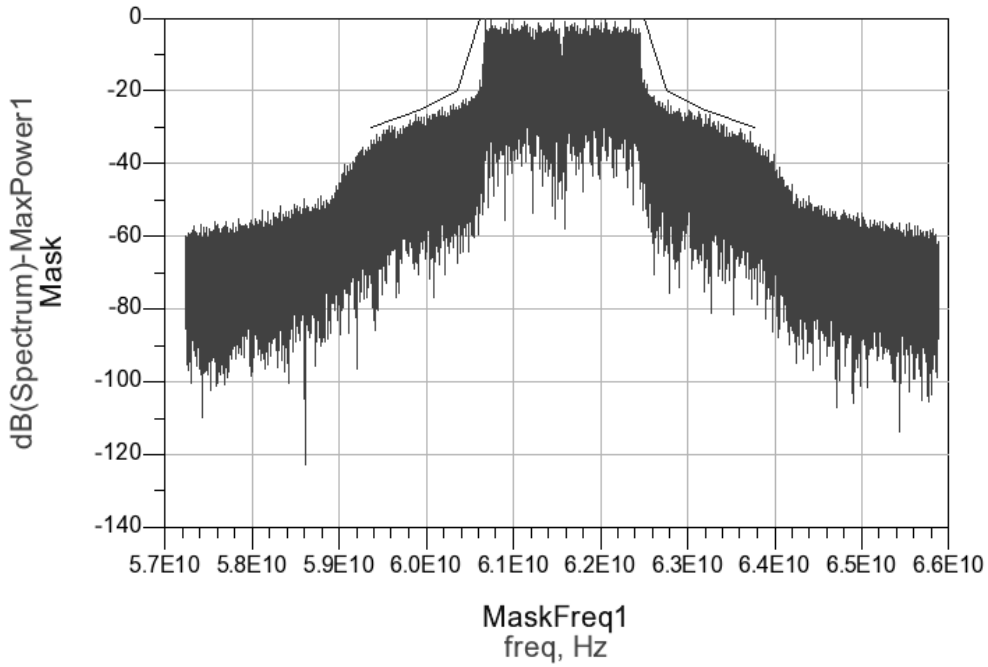

Fig. 3. Transmitted spectrum and mask from simulation.

The proposed system is designed to use OFDM according to these specifications. The transmitter path can support 16-QAM modulation and specified data rates up to 4200 Mbps.

CHAPTER 3

Subharmonic Mixing

For 60 GHz operation, a conventional mixer would require an LO signal of nearly the same frequency to perform the necessary frequency conversion. This requirement would exacerbate problems such as DC offset and poor isolation. Further, VCO design for this frequency is complicated because of the challenges in designing a circuit with low phase noise and low power consumption. Use of a lower LO frequency is preferred to relax these design constraints.

Description

Subharmonic mixing is a mixing process in which the desired output frequency is produced from the input frequency and a multiple of the LO frequency. In an upconversion scenario the output frequency can be described as

$$f_{RF} = | f_{IF} \pm n f_{LO} |, \quad (1)$$

where f_{RF} is the RF frequency, f_{IF} is the IF frequency, n the desired LO harmonic and f_{LO} the LO frequency. A choice of n=3 in an SHM design would, for example, enable the use of an LO frequency one-third of that required using a fundamental mixer.

SHMs are generally implemented by switching the input signal with multiple phases of a LO signal, as shown in Fig. 4.

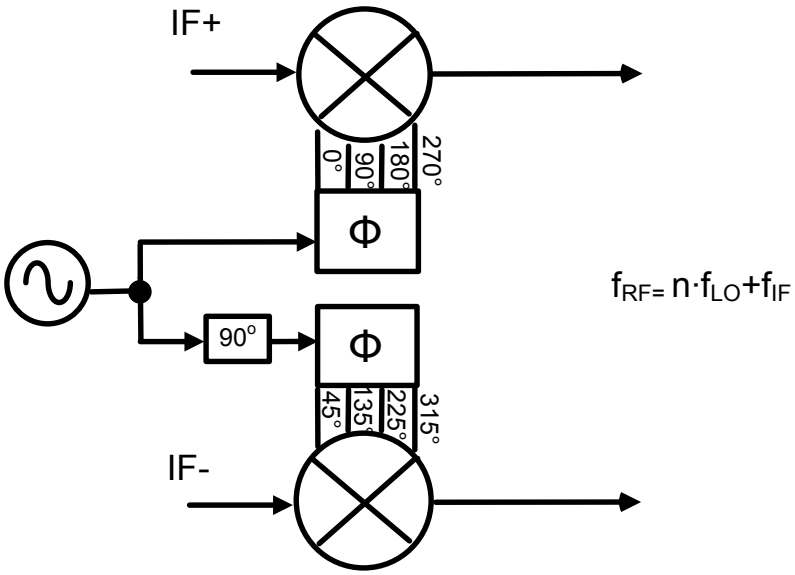

Fig. 4. Typical SHM approach.

A large number of SHMs are implemented by modifying Gilbert cell mixers by adding extra switching transistors in parallel with the normal switching quad. One of many approaches to doing so is shown in Fig. 5, a fourth-harmonic mixer.

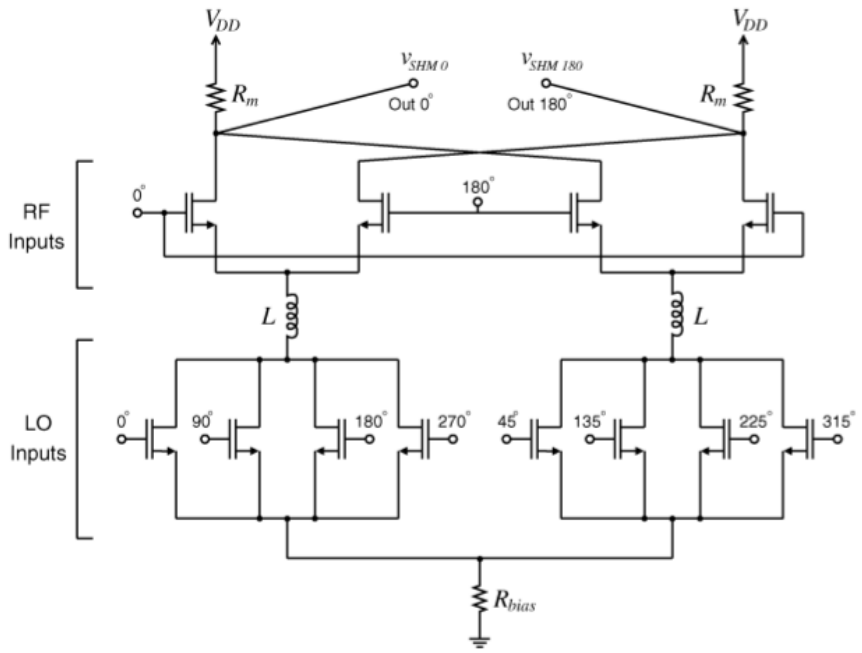

Fig. 5. Fourth-harmonic SHM.

Assuming that each transistor shuts off completely for $V_{gate} < V_{threshold}$ (i.e. ignoring subthreshold operation), the input signal will be switched at a frequency of $4*f_{LO}$ by either of the bottom sets of transistors. An overlay of the four LO signals is shown in Fig. 6.

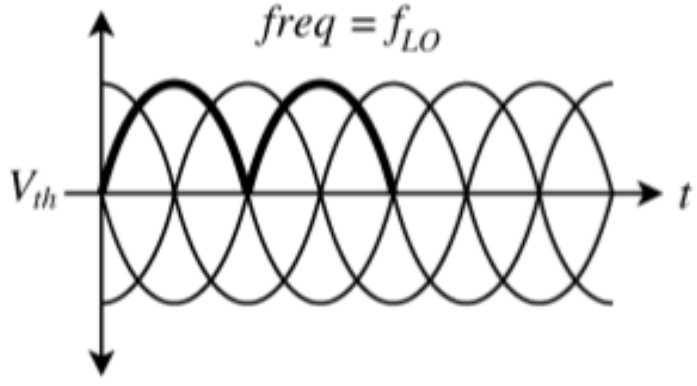

Fig. 6. Four-phase LO switching signals.

The result of this multiphase LO switching is a current mode signal through the switching circuitry that oscillates at the desired harmonic of the LO frequency, as shown in Fig. 7.

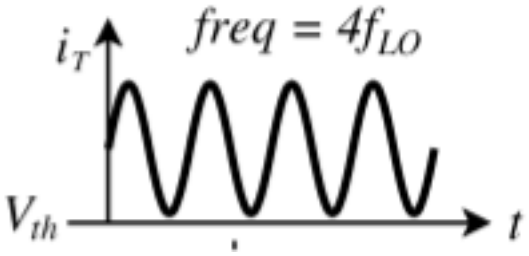

Fig. 7. Tail current due to added phases of LO switching.

By switching the signal current with this higher frequency signal, the input can be up or downconverted to the desired frequency without the use of a fundamental frequency LO.

Previous Subharmonic Mixers

In order to illustrate relevant design tradeoffs, in this section previous mixers above 20 GHz are considered. Larson and Kodkani presented a 24 GHz passive SHM in 0.13 μm CMOS designed to use a 12 GHz LO in downconversion to zero- or low-IF [3]. Fig. 8 shows the circuit, which cascades two stages of active device switching with no gain from the mixer itself. It is able to achieve a conversion gain of 3.2 dB with a DSB noise figure of 10 dB.

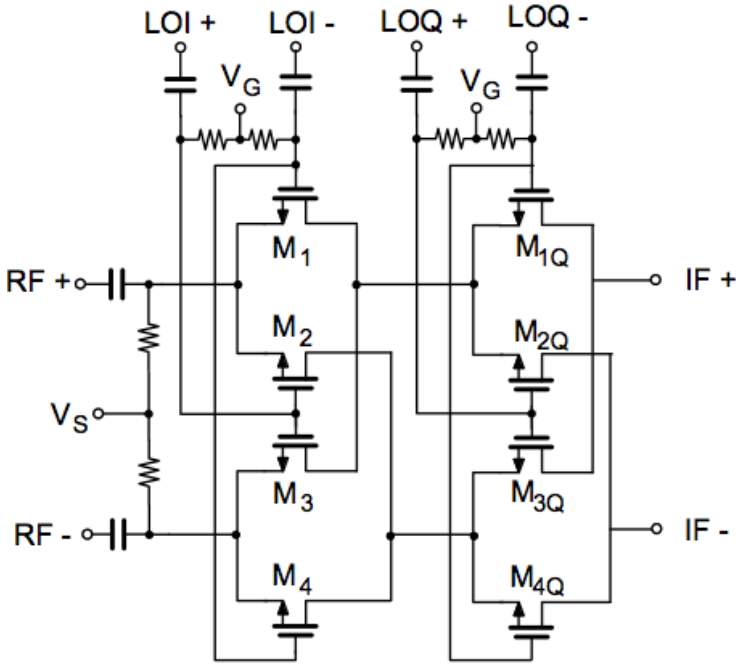

Fig. 8. 24 GHz passive SHM.

This circuit illustrates the design effort involved in achieving reasonable conversion gain from a high frequency mixer. Although the circuit is a passive mixer, it is implemented with active devices and is surrounded by active circuits: a preamplifier, active IF buffer and active LO single ended to differential conversion with active LO buffers. The system draws about 30 mW, excluding the 12 GHz LO.

Wang, et al. proposed a wideband SHM, illustrated in Fig. 9, based on a Gilbert cell and operating at up to 100 GHz in 90 nm CMOS [4]. Similar to the previous design, this circuit uses a four phase LO at one half the desired RF frequency. LO phase generation is handled by a 90° broadside coupler and two Marchand transformers used as baluns.

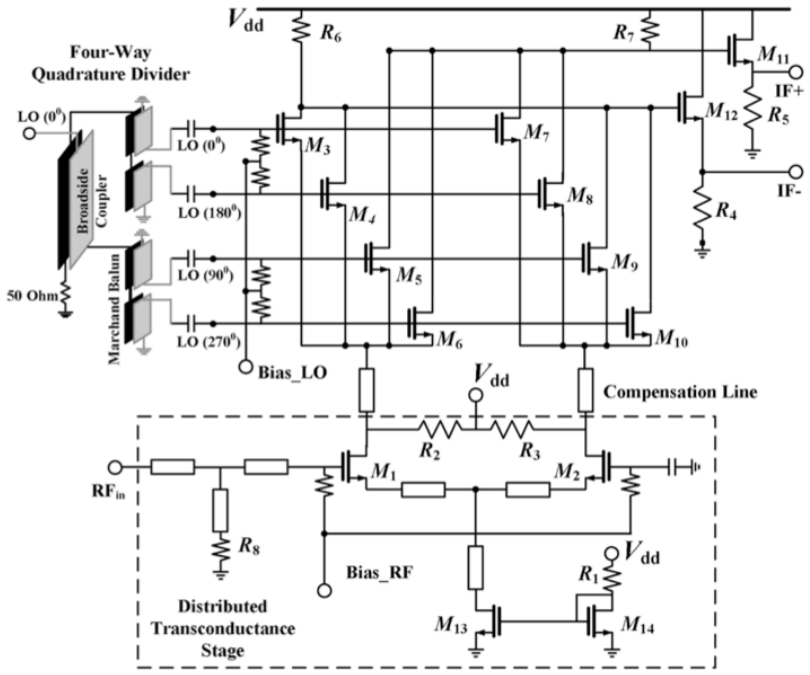

Fig. 9. 30-100 GHz wideband SHM.

This mixer achieves remarkable gain flatness over a 70 GHz bandwidth with -1.5 ± 1.5 dB reported throughout this range. Advantages of using this topology include the (relatively) high conversion gain at these frequencies and good isolation between RF, IF and LO ports. Here the power cost is more substantial, however, with the reported DC power consumption of 58 mW for the mixer circuit.

Finally, Yan, et al. demonstrated a 21 GHz frequency tripler using subharmonic mixing and a quadrature LO as shown in Fig. 10 [5]. This circuit is an example of a low power solution in 0.18 μm CMOS. The design works by feeding quadrature LO signals into two transistor pairs. The bottom pair produces a double frequency

component at the (coupled) source of the top differential pair, which performs the conversion to the output frequency.

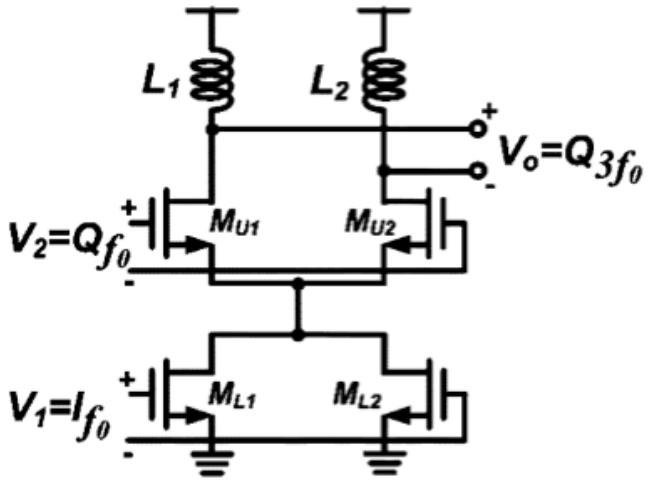

Fig. 10. 21 GHz frequency tripler using SHM techniques.

The simplicity and low power budget of this design make it an attractive choice for high frequency mobile use. Provided that the I/Q signals are generated precisely, the circuit achieved a conversion gain of around -5.7 dB at the output frequency. This performance is in the ballpark for many mm-wave mixers, but at relatively low power consumption. A potential concern about this topology is its ability to reject undesired harmonics. Since the circuit is fully differential, second-order harmonics are not a major problem, but unwanted odd-order harmonics may be. The authors address this problem effectively with output bandpass filters and report measured phase noise of below 130 dBc/Hz at 1 MHz offset from 21 GHz. However, the cost of this filtering is measured in silicon, and the die area of roughly 1 mm^2 is triple that of designs that do not use this filtering.

CHAPTER 4

Proposed Mixer Circuit

Block Level Description

The proposed self resonant mixer can best be understood by treating it as two successive fundamental mixer stages. The first of these stages is shown in Fig. 11. In this illustration the input stage of the proposed mixer circuit is modeled as a differential pair with a tail AC current source, whose generation is discussed shortly, and some load.

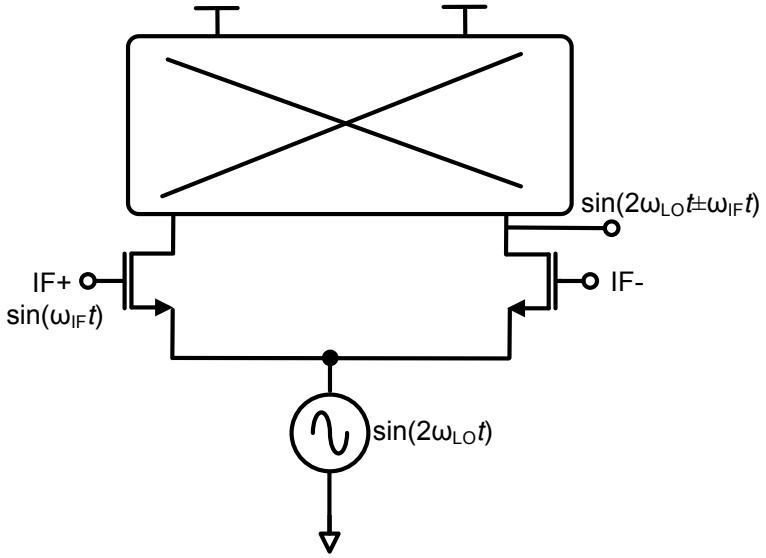

Fig. 11. Input stage of proposed mixer.

Either half of this circuit can be regarded as a single-balanced mixer, with the current source taken as the signal input and the gate signal as the switching input. Given input signals of the form

$$i_s = A\sin\left(2\omega_{LO}t\right) \tag{2}$$

and

$$v_g = \sin\left(\omega_{IF} t\right), \tag{3}$$

the signal at the drain node will have the form

$$i_d = \sin\left(2\omega_{LO} t \pm \omega_{IF} t\right). \tag{4}$$

The IF signal and upconverted spectra are illustrated in Fig. 12.

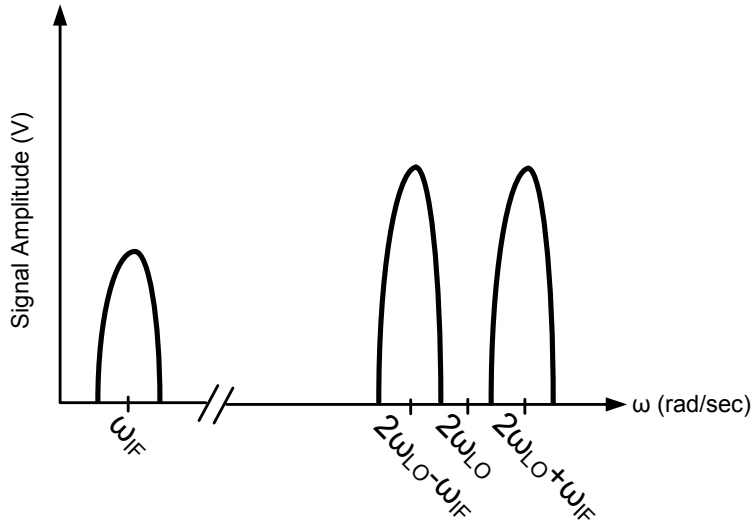

Fig. 12. IF and upconverted signal spectra.

The second mixing stage is illustrated in Fig. 13. Here the switching input is the LO signal applied to the switching quad. The signal input is the current signal generated in the previous mixing stage at frequency $2\omega_{LO} \pm \omega_{IF}$ and defined in (4).

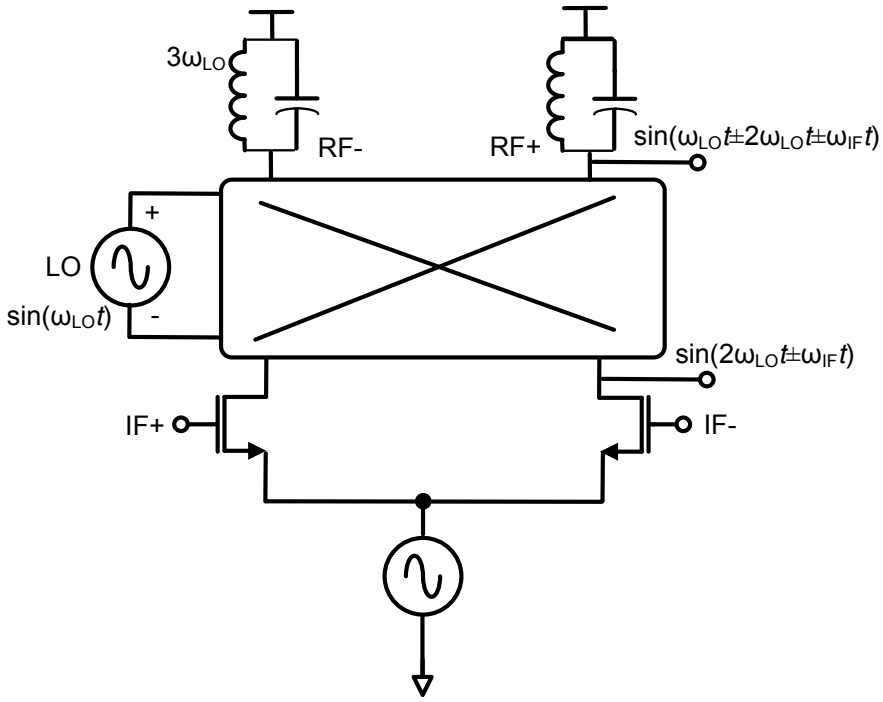

Fig. 13. Upconversion to RF with LO signal.

When multiplied with the LO signal, which has the form

$$v_{LO} = \sin\left(\omega_{LO} t\right), \tag{5}$$

the output signal

$$v_{RF} = \sin\left(\omega_{LO} t \pm 2\omega_{LO} t \pm \omega_{IF} t\right) \tag{6}$$

is produced. The output spectrum of this stage is shown in Fig. 14.

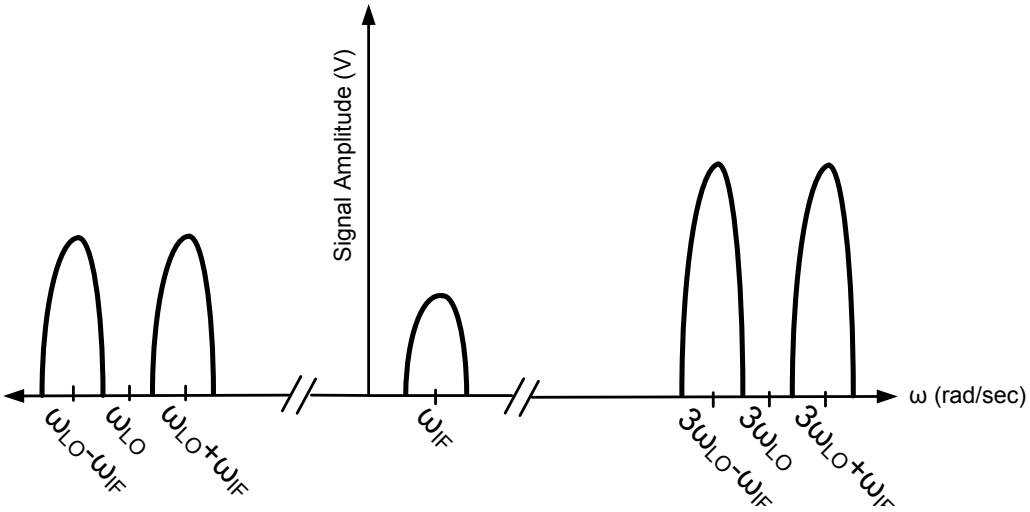

Fig. 14. Output spectra of RF mixing operation.

Note that there are four output frequency components; the desired signal is centered around frequency $3\omega_{LO}$. The LC circuit at the output node is tuned to this frequency in order to enhance the response.

The preceding analysis of self resonant mixing assumes an AC source at frequency $2\omega_{LO}$ is connected at the sources of the input stage. The simplified circuit diagram of the proposed mixer, shown in Fig. 15, illustrates how this signal component is generated.

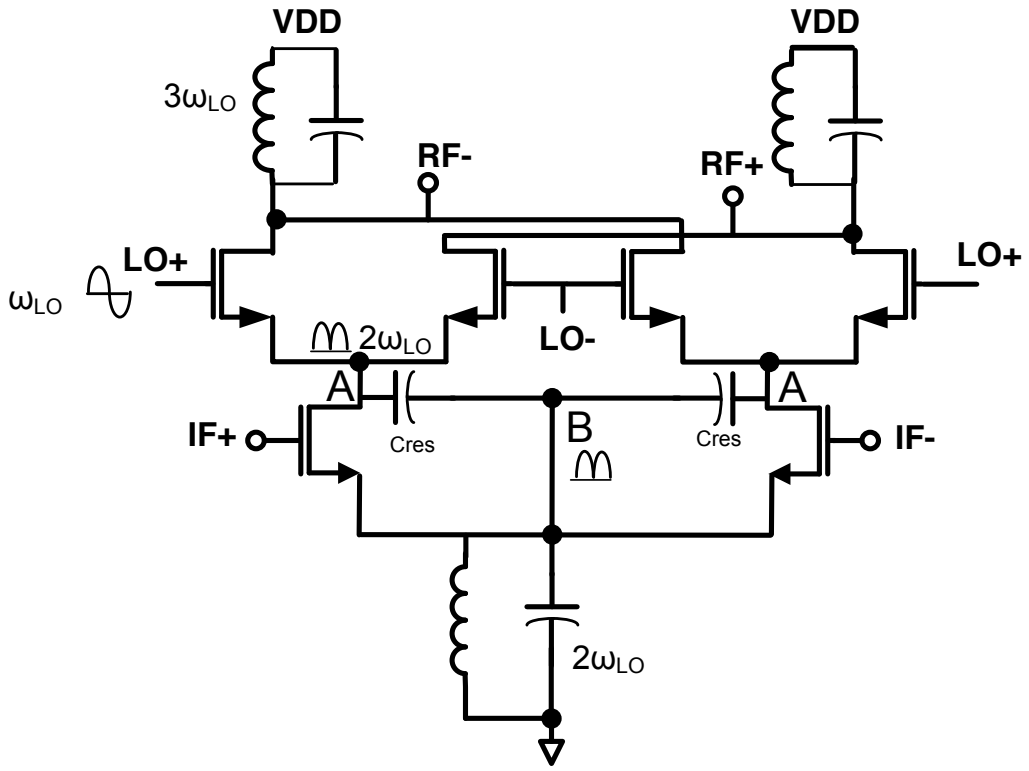

Fig. 15. Proposed mixer circuit and 2*LO generation.

Consider the voltage at node A assuming a sinusoidal LO input and neglecting subthreshold current in the MOSFETs. As one transistor of the switching pair turns on, the voltage at A is pulled up (towards the voltage at the RF node). As the input of this transistor drops below the threshold voltage, the opposite transistor turns on with a similar pull-up effect. The effect of this operation is a voltage signal at node A that peaks at a frequency of $2\omega_{LO}$. This signal is fed to the resonant node, B, via capacitors C_{res}. Because the signal is common mode it is reinforced by both halves of the circuit (the $2\omega_{LO}\pm\omega_{IF}$ components, however, are differential and cancel at node B). Connected to node B is a resonant tank tuned to provide maximum impedance at $2\omega_{LO}$. This

topology enables the resonant node to act like an AC source at the desired frequency.

In summary, the self resonance property enables the proposed mixer to perform subharmonic mixing by essentially providing a second fundamental mixing stage within the same circuit.

Circuit Analysis

In order to arrive at reasonable device and component sizes, the initial design for the mixer resembled the process for a Gilbert cell. However, design simulations were performed on the modified topology including load LC tanks and resonant network with a 20 GHz LO. For all transistors in the design a gate length of 180 nm was used. Although the IBM process used has a minimum feature size of 100 nm, using that size resulted in high λ values that caused poor large signal performance.

The overdrive voltage of the input transistors was determined using the relation

$$V_{OV} = \frac{A_{IIP3}}{\sqrt{32/3}} \approx 70\ mV\ . \qquad (7)$$

Here $A_{IIP3} \cong 224$ mV, which corresponds to a P_{IIP3} of 0 dBm for a 50 Ω input impedance. For a threshold voltage of 0.5 V plus some headroom for the resonant devices connected to the input transistors' sources, a bias voltage of 590 mV was chosen.

Using this V_{OV}, the optimum input stage width for maximum power gain was determined from simulations to be approximately 112 μm. These choices resulted in an input stage g_m of around 37 mS.

Next the switching quad transistors were biased at 850 mV to allow a large signal swing of around 350 mV or 4 dBm for a 50 Ω input impedance. The load to achieve the desired gain was calculated as $A_v=(2/\pi)g_mR_L$ = 135 Ω. Additionally, LC circuits are connected to the load for resonance at the output frequency of 60 GHz. The sizing of these components is L_{top}=70 pH, C_{top}=80 fF. Next the stability and linearity of this topology are considered. The passive devices in the resonant tank, L_{res} and C_{res}, are chosen to achieve 40 GHz resonance and sized as L_{res}=300 pH and C_{res} = 50 fF. The feedback capacitance C_{block} is simulated to determine its effect on gain and based on simulations, C_{block} = 1 pF is chosen.

The required source degeneration is determined by sweeping output power as a function of input power for different L_s values. Although the degeneration inductor affects both gain and linearity, in this design it was found to have a far heavier impact on circuit gain. Simulations performed on R_s revealed similar effects. After S-parameter simulations confirmed that the circuit was stable, L_s = 1 nH and R_s = 1 Ω were chosen to minimize the reduction of gain caused by degeneration.

Following these design steps periodic steady state and periodic

AC simulations were performed to determine the correct LO value for the circuit and to get an idea of the functionality of the circuit. Sweeping the LO power versus the voltage gain and various device sizes revealed that circuit gain continued to increase until around 24 dBm. Since such a high LO power is generally impractical, transistor sizes were adjusted to move the majority of the gain increase down to around 5 dBm. Even with these adjustments, the circuit gain continued to increase for higher LO power, but at a more gradual rate. Final device and component sizes appear in Table III. Note that all transistor lengths are 180 nm.

Table III
Mixer Device and Component Sizes

Device	**Parameter**	**Value**
Input transistors	W	120 μm
Switching transistors	W	20 μm
Degeneration resistance	R	1 Ω
Degeneration inductance	L	1 nH
40 GHz resonance inductor	L	300 pH
40 GHz feedback capacitor	C	50 fF
Resonant feedback capacitors	C	400 fF
60 GHz output inductor	L	80 pH
60 GHz output capacitor	C	80 fF
Load impedance (single-ended)	R	80 Ω
Input impedance (single-ended)	R	250 Ω (at 1 GHz)

Simulation Results

DC operating point information for the mixer circuit appears in Table IV.

Table IV
Mixer DC Operating Conditions

Device	Parameter	Value
Input transistors	Vbias	560 mV
	Vds	209 mV
	Vgs	553 mV
	Vt	479 mV
	Cgs	118 fF
	Cgd	30 fF
	gm	26.6 mS
Switching transistors	Vbias	850 mV
	Vds	796 mV
	Vgs	634 mV
	Vt	482 mV
	Cgs	21 fF
	Cgd	3 fF
	gm	8.7 mS
Branch current	Id	2.285 mA
Supply voltage	Vdd	1.2 V

Fig. 16 depicts the input stage linearity, determined by sweeping S11 over a range of IF power for different Ls values. Overall the linearity and gain are better for smaller inductances and so Ls = 1 nH is ultimately chosen. Fig. 17 shows the same simulation run for various Rs values; a similar effect on gain degradation was found, although overall linearity is not impacted much. Fig. 18 and Fig. 19 demonstrate stability simulations determined by S-parameter simulation as a function of IF frequency for varying Ls and Rs, respectively. Note that the stability is not affected much by changing these parameters.

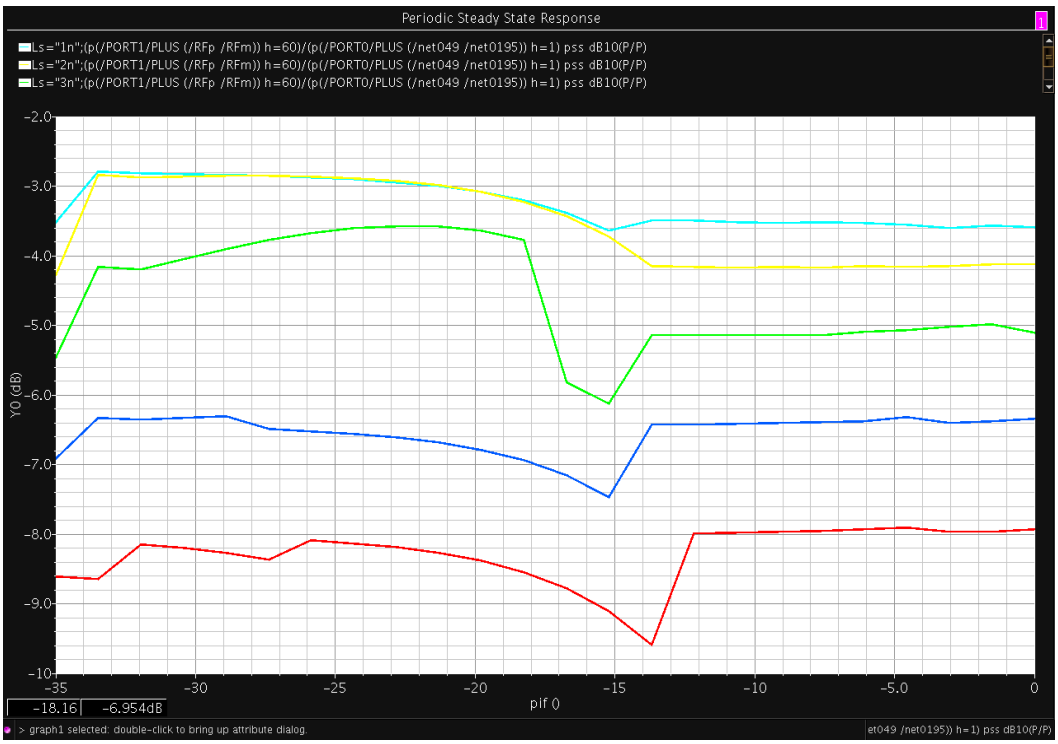

Fig. 16. Input stage linearity versus IF power for varying Ls.

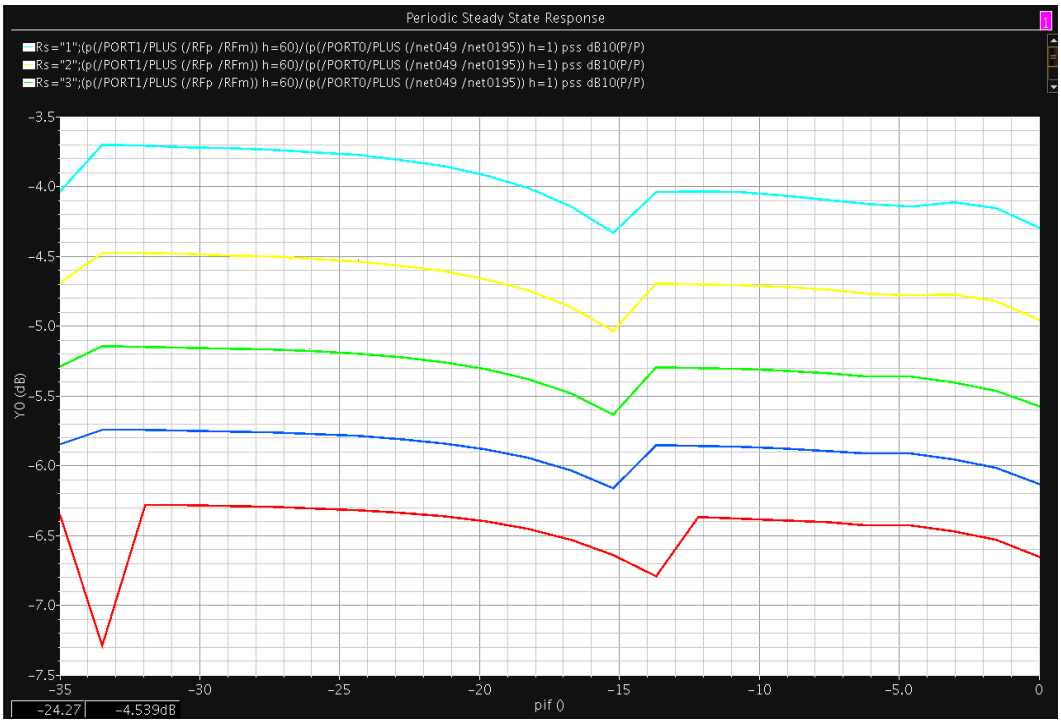

Fig. 17. Input stage linearity versus IF power for varying Rs.

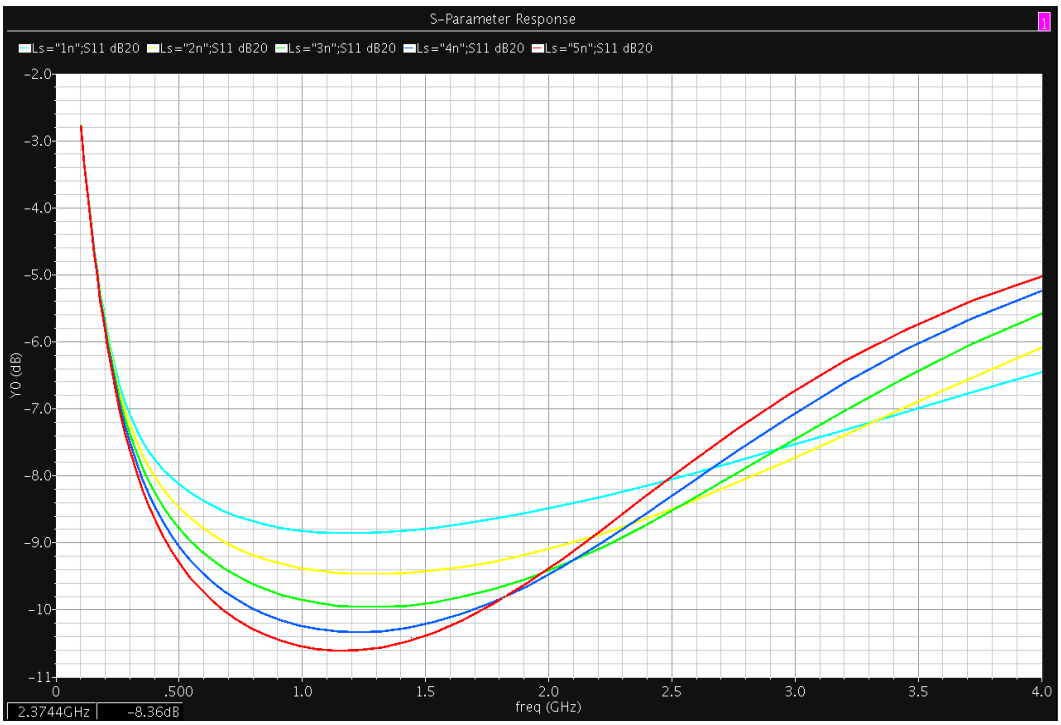

Fig. 18. Input stage S11 versus IF frequency for varying Ls.

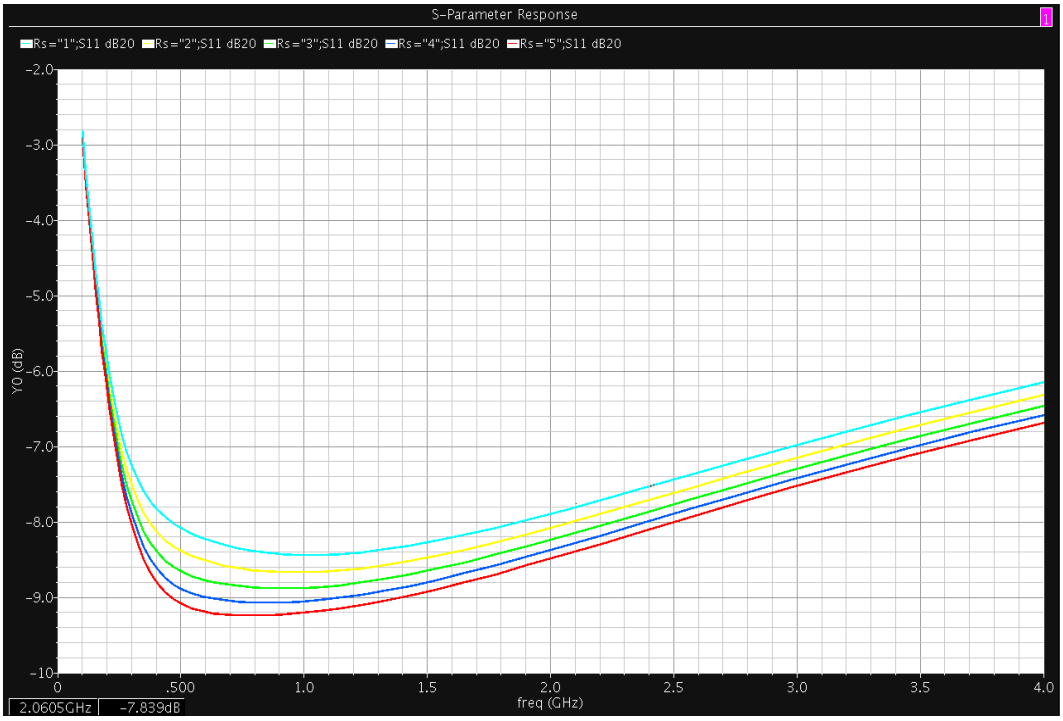

Fig. 19. Input stage S11 versus IF frequency for varying Rs.

Fig. 20 shows simulation results from iterating the input and load transistor sizes for optimal gain at lower LO power. The best compromise sizing was able to realize most of the gain benefit at 5 dBm LO power. Further width reductions in the input stage transistor were undesirable because they increased the input impedance by several hundred Ohms in simulations.

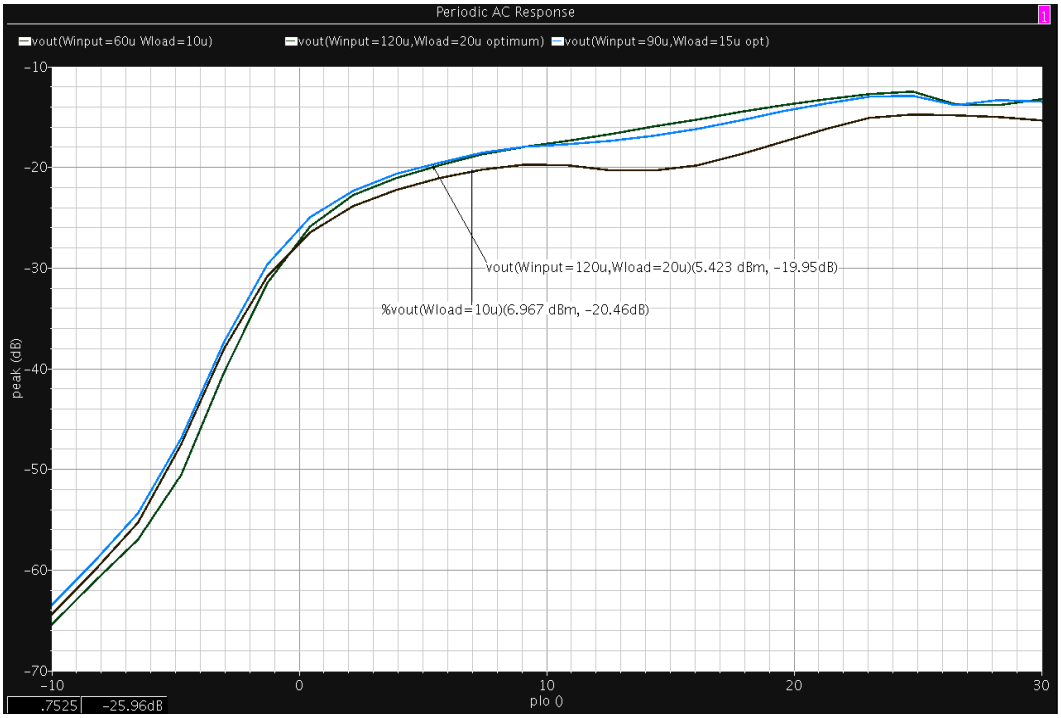

Fig. 20. Input stage gain versus IF frequency for varying Ls.

Fig. 21 demonstrates RF conversion gain as a function of output frequency. Here gain flatness suffers from a narrowband match at the output. Fig. 22 demonstrates S11 and S22 versus IF frequency.

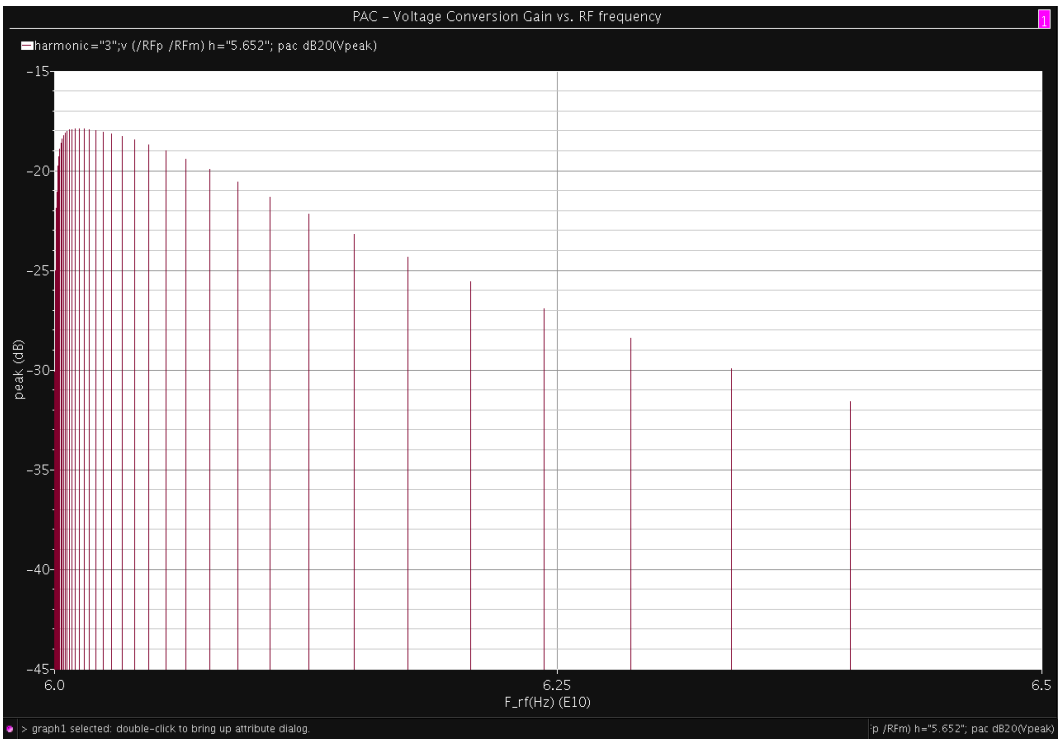

Fig. 21. Voltage conversion gain versus RF frequency.

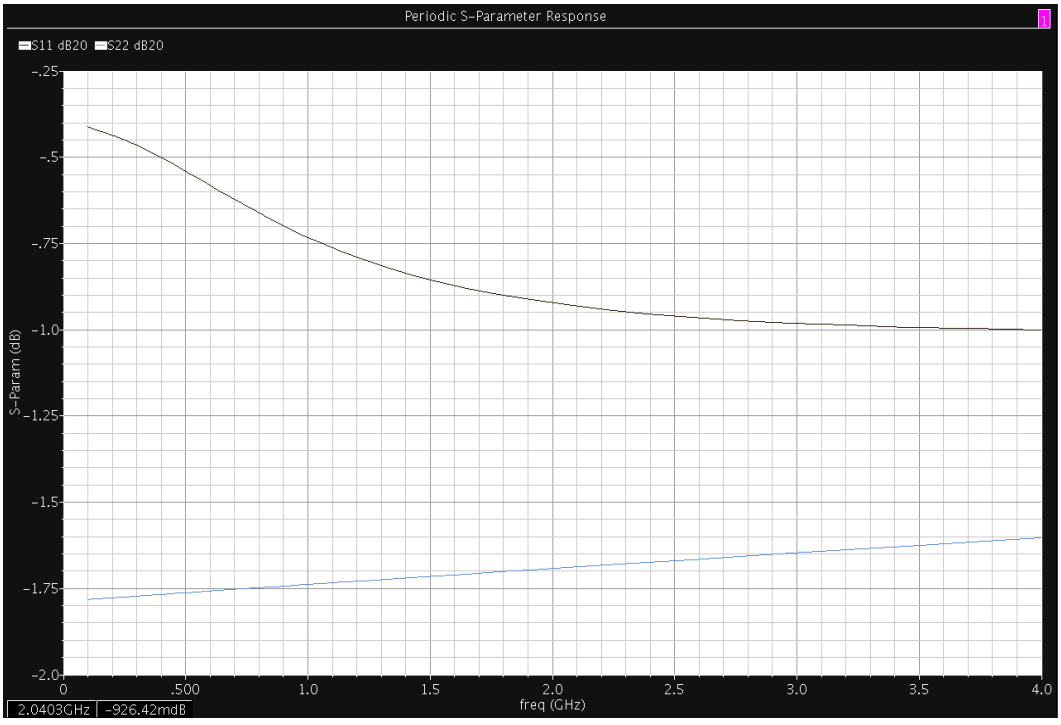

Fig. 22. S11 and S22 versus IF frequency.

Fig. 23 demonstrates the output power gain versus IF power. Good linearity is achieved up to about -6 dBm. This result is shown more explicitly in the IP1dB simulation of Fig. 24. Finally, mixer IIP3 is shown in Fig. 25.

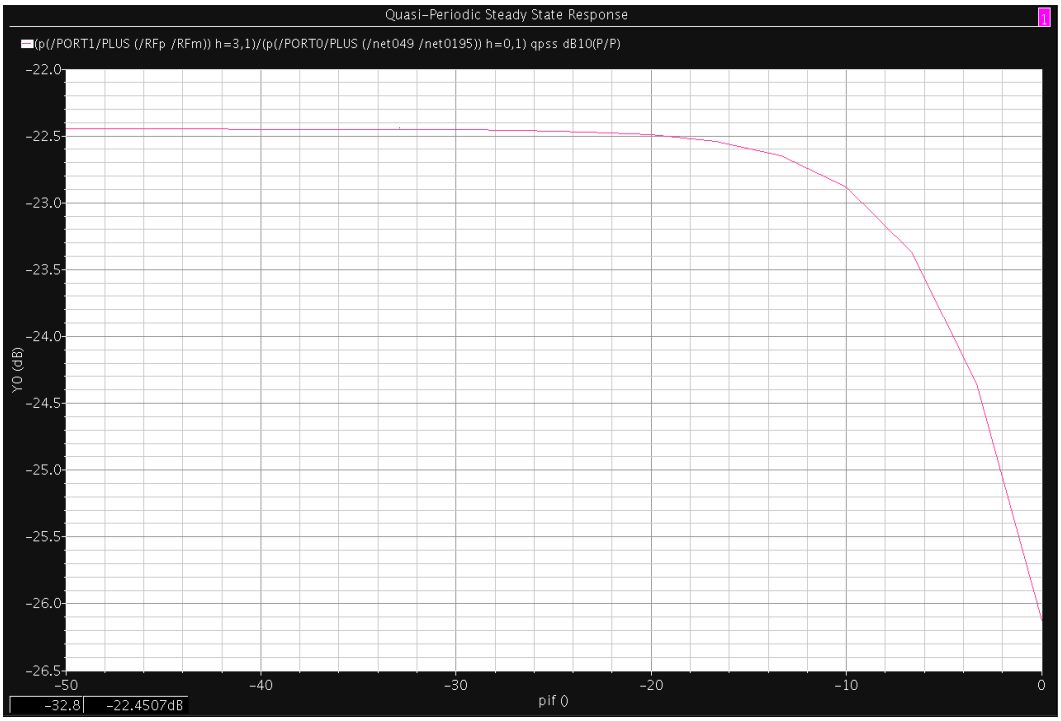

Fig. 23. Output power gain versus IF power.

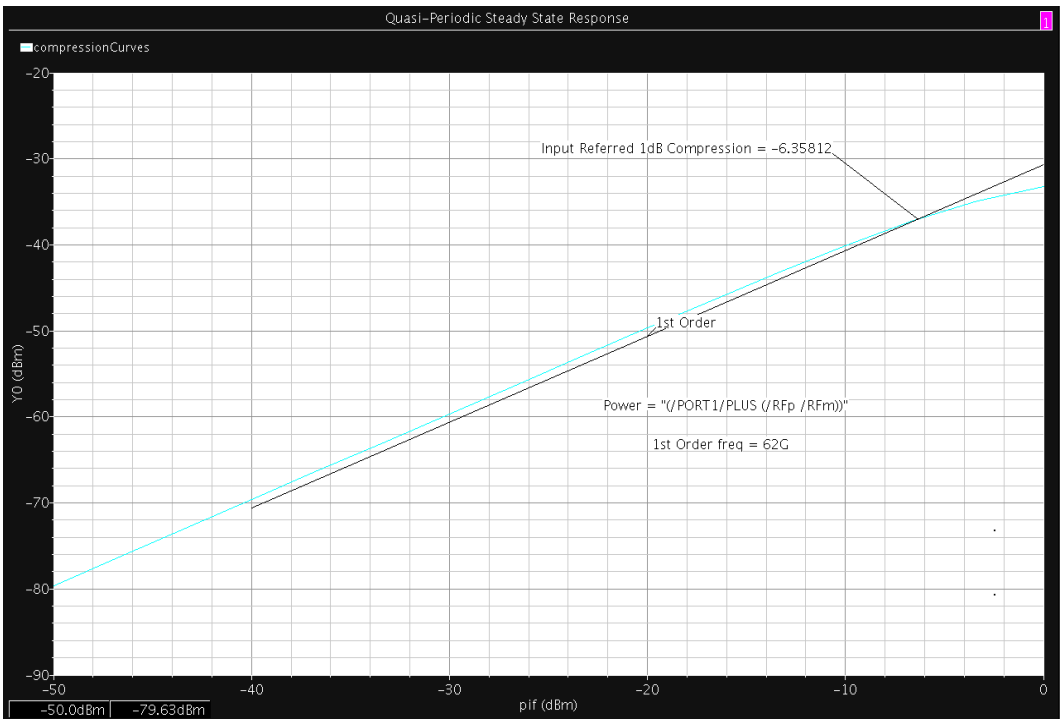

Fig. 24. Input 1-dB compression point.

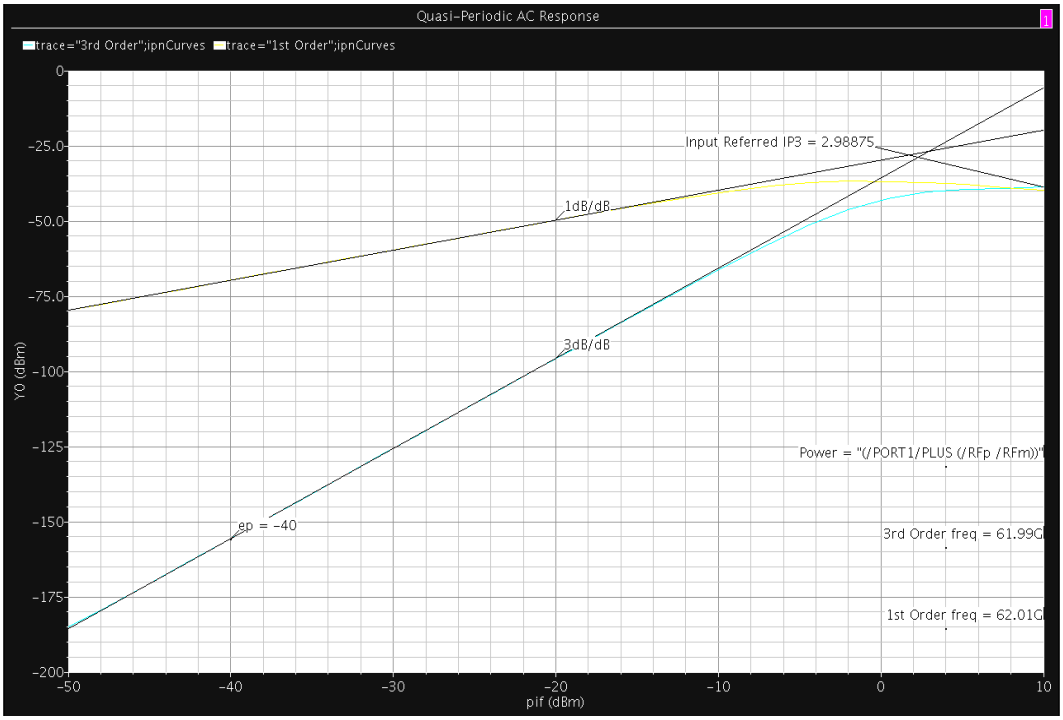

Fig. 25. Input referred third-order intercept point.

Table V summarizes the simulated performance of the self resonant third harmonic mixer.

Table V
Mixer Performance Summary

Parameter	**Value**
LO power	5 dBm
Conv. gain at 5 dBm LO	-18.5 dB
IP1dB	-6.3 dBm
IIP3	2.93 dBm
DC power	9.6 mW

CHAPTER 5

Discussion and Conclusion

In this work, a third harmonic mixer which mitigates the need for a 60 GHz VCO has been presented in 90 nm CMOS with 1.2 V supply. The mixer circuit is based on a Gilbert cell and is developed for upconversion to 60 GHz in accordance with the IEEE 802.11ad Physical Layer draft specification.

In the second chapter, this work discusses the linearity and EVM requirements for 60 GHz transmission using the IEEE 802.11ad draft specification as its target. Agilent ADS is used to generate a signal chain test bench which models the gain and linearity of other system blocks. Accordingly, device performance in the context of this overall system is used to determine the gain and linearity requirements of the mixer circuit and to arrive at minimum specifications for design. Estimating performance of the signal chain from the literature it is determined that, for a mixer conversion loss of 20 dB, IIP3 of 1 dBm and IP1dB of -9.6 dBm, data throughput above 4 Gbps is achievable.

The third chapter of this thesis presents an analysis of subharmonic mixing. It is noted that the plurality of subharmonic mixer designs are implemented with multiple LO phases to increase the magnitude of the desired $n*f_{LO}$ switching component.

This approach, while certainly effective, suffers from several drawbacks. These drawbacks relate primarily to the generation of

additional LO phases. One technique is to apply a differential LO signal to a set of passive phase shifters. This technique generally does not increase the power budget, but can suffer from mismatch in the shifter components leading to phase imbalance. In addition, the chip area requirements increase with the need for additional passive components. Active shifters can also be used. In this case the chip area requirements need not increase substantially. However, active devices will increase the dc power budget of the circuit, especially in the case of active shifters that are variations on single stage amplifier topologies. Active shifters, like their passive counterparts, will be subject to phase errors as well.

In chapter four a mixer circuit that uses a subharmonic LO without the phase generation and shifting requirements is described. This circuit, based on a Gilbert cell topology, is designed to perform upconversion from an IF of 1 GHz to RF of 60 GHz using a 20 GHz differential LO. It does so by essentially performing two stages of mixing. The first of these mixes IF with the 2*LO (40 GHz) signal at the resonant node, producing a frequency of $2f_{LO} \pm f_{IF}$ at the drain nodes of the IF input transistors. The second stage consists of this signal switched with the 20 GHz LO to produce four output frequency components, one of which is the desired 60 GHz signal.

The proposed mixer circuit has a conversion loss of 21 dB for 5 dBm LO power. This result is on the low end of a typical value for

conversion gain of a passive mixer. A typical 60 GHz transmit scenario would require additional gain blocks, which have been modeled in Chapter 2. In the context of the original simulation, the gain is 1 dB lower and the linearity is somewhat better; the output linearity is correspondingly better than the original projection. Linear circuit operation is the single greatest criterion for the OFDM modulation required for the higher throughput schemes in the IEEE standard. The -23.5 dB RMS constellation error is suitable for 4.5 Gbps transmission using QAM-16 modulation. This throughput is four times of the approximately 1 Gbps necessary for uncompressed HD video transmission. However, it should be noted that further data rate increases could be supported as well. Achieving an extra 1-2 dB of EVM reduction would enable the use of QAM-64 modulation and support data rates of up to 7 Gbps.

Frequency mixing and VCO generation are essential components of an RF transceiver system. This thesis proposes a new topology for subharmonic mixing that uses a feedback resonance node to perform upconversion in two stages. Such an approach can alleviate many of the design complications that are typically pushed onto the VCO implementation.

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