Phase Noise Reduction Using Active Biasing

by

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ABSTRACT

An investigation of phase noise in amplifier and voltage-controller oscillator (VCO) circuits was conducted to show that active direct-current (DC) bias techniques exhibit lower phase noise performance than traditional resistive DC bias techniques. Low-frequency high-gain amplifiers like those found in audio applications exhibit much better 1/f phase noise performance and can be used to bias amplifier or VCO circuits that work at much higher frequencies to reduce the phase modulation caused by higher frequency devices. An improvement in single-side-band (SSB) phase noise of 15 dB at offset frequencies less than 50 KHz was simulated and measured. Residual phase noise of an actively biased amplifier also exhibited significant noise improvements when compared to an equivalent resistive biased amplifier.

ACKNOWLEDGMENTS

I would like to thank my beautiful wife, Kaylee, for all of the support that she gave me throughout this effort. I also would like to thank Dr. James Aberle for his guidance and inspiration to pursue this degree. I am also grateful for Sergio Cardona of Raytheon Company for providing encouragement and research funding. I want to acknowledge that the idea of active biasing to reduce phase noise is a furtherance of the work performed by Roger Clark of Raytheon Company.

TABLE OF CONTENTS

Page

LIST OF TABLES

LIST OF FIGURES

Chapter 1

Introduction

Low phase noise is an important measure of signal purity and is a key specification in areas such as communications and radar. Communication systems that exhibit better phase noise performance typically have better bit-error rates while radar systems that exhibit better phase noise performance typically have better resolution. The most basic component in all electronic systems is the transistor because it is the fundamental building block for modern integrated circuits and analog devices. Transistors are also a common source of noise in electronic systems. One of the common noise sources in transistors is flicker noise. Sources of flicker noise are often attributed to lattice imperfections, wafer cutting and polishing scratches, impurities added in the manufacturing process, or generation and recombination noise in a transistor due to base current variation. Other contributing sources of noise include thermal noise, which is a function of temperature, bandwidth, and noise resistance as well as shot noise which is a function of the DC bias current [1].

The dominating contributor of phase noise in most systems is the local oscillator. A local oscillator may be as simple as a crystal oscillator or more complex with a phase-locked-loop (PLL) that controls a VCO. Common VCO topologies involve a radio-frequency (RF) transistor as the heart of the design. Reducing the transistor noise effects in the design of a VCO is a much studied and desired improvement to the overall system phase noise. The traditional approach

to lowering phase noise involves increasing the Q factor of the resonator, using capacitors to decouple power supply noise, and selecting lower noise transistors [2]. Some new approaches to lower phase noise include maximizing the amplitude of the tank voltage, optimizing the collector current waveform, and minimizing the loading of the VCO [3]. The design effort presented here will focus on reducing the effects of transistor flicker noise by using a technique known as active biasing. As a path to study improving phase noise of VCO circuits, an amplifier is first investigated in order to reduce transistor related noise effects.

Chapter 2

Types of Noise

Residual Phase Noise

Residual phase noise is often referred to as the open loop phase noise. This type of phase noise measurement differs from closed loop phase noise measurements in oscillators due to the lack of a carrier. Residual phase noise measurements are performed on devices such as amplifiers, frequency dividers, frequency multipliers, and mixers. Residual phase noise is a result of the purity of a signal after being applied to a device under test (DUT). In silicon devices such as transistors, the up-converted base-band flicker noise, or 1/f noise, is the leading cause of residual phase noise [4].

Single-Sideband (SSB) Phase Noise

The single-sideband phase-noise power-to-carrier ratio, or commonly referred to as the single-sideband (SSB) phase-noise, is a measurement of the ratio between the SSB power and the signal power over a 1 Hertz (Hz) bandwidth as shown in equation one.

$$L(\Delta f) = \frac{P_{SSB}}{P_S} \qquad (1)$$

Where $L(\Delta f)$ is the SSB phase noise, P_{SSB} is the SSB power, P_S is the signal power at the center frequency of the carrier, and Δf is the frequency offset from the carrier at which the sideband power is observed. Phase noise is related to frequency deviations since the instantaneous frequency equation contains a relationship with the change in phase in time as described by equation two [4].

$$f(t) = f_0 + \frac{d\phi(t)}{dt}\frac{1}{2\pi} \qquad (2)$$

The variable f_0 is the center frequency and $\frac{d\phi(t)}{dt}$ is the random phase fluctuation. Equation two shows that a random phase fluctuation will cause a random frequency fluctuation. The importance of this relationship explains why phase noise measurements are the key method of describing signal purity in oscillator design. Leeson's Equation for describing SSB phase noise describes the major contributors of transistor-based oscillator designs [5] and has been further clarified to be shown as in equation three [2].

$$L(\Delta f) = 10\log\{\frac{2FkT}{P_S}[1 + (\frac{f_0}{2Q\Delta f})^2](1 + \frac{\Delta f_{1/3}}{|\Delta f|})\} \qquad (3)$$

F is the noise figure of the active device, k is Boltzmann's constant, T is the temperature, Q is the loaded quality factor of the resonator, and $\Delta f_{1/3}$ is the flicker noise corner frequency offset. Equation three allows a simple calculation of device parameters to get an estimate of the expected SSB phase noise if a certain transistor was used in an oscillator design. Many other parameters should be looked at to do a proper oscillator design, but equation three allows an initial check to see if the device in question has the potential to give adequate results.

Chapter 3

Amplifier

In order to explore residual phase noise, two amplifiers were designed using bipolar-junction transistor (BJT) common-emitter (CE) topologies that were either resistive biased or active biased. The goal of the amplifier was not to be state of the art in terms of gain, noise figure, linearity, or isolation, but to design an unconditionally stable, general purpose amplifier that could be explored to see the effects of biasing on residual phase noise.

Design Parameters

Typical design parameters for RF amplifiers include frequency, bandwidth, noise figure, gain, and return loss. Other parameters include linearity, power consumption, and compression point. Table 1 shows the main parameters and design goals that were investigated in the design of the BJT CE amplifier.

Table 1: Amplifier Design Goals

Design Goals	
Center Frequency	5500 MHz
Bandwidth	3000 MHz
Noise Figure	< 3 dB
Return Loss	< -10 dB
Gain	> 5 dB
Stability (μ and μ')	> 1

The main concept of the design was focused on stability at the sacrifice of gain and noise figure. One way to ensure unconditional stability of an amplifier is to have the stability criterion μ or μ' be greater than one [6]. This implies that for

all frequencies the value of μ or μ' has to be greater than one. However, at higher frequencies the value of μ often drops below one, but the amplifier can still be considered unconditionally stable as long as the magnitude of the gain |S21| and |S12| are less than one. If the gain is less than one, then the conditions of oscillation cannot exist. One method to improve the stability is to resistively load the input or output of the amplifier. If the input is resistively loaded then the noise figure will degrade. If the output is resistively loaded, then the gain will be reduced. The output was loaded down with very small resistance values such that adequate gain could be realized that would enable the experiment to be performed.

With a stable amplifier design, two different DC bias techniques were investigated to see if there were any improvements or degradations to residual phase noise performance. Even though different bias techniques were being compared, all DC parameters of the amplifying transistor were the same in order to have a fair comparison. Common DC parameters means that the collector current, the base current, and the base voltage are identical for both the resistive and active biased amplifiers. Flicker noise is most commonly attributed to device impurities, but recent studies have shown that there is a non-linear relation of the DC bias on the 1/f corner frequency [7]. Low-frequency high-gain transistors like those found in audio applications exhibit much better 1/f phase noise performance and can be used to bias transistors or amplifiers that work at much higher frequencies to reduce the phase modulation caused by the higher frequency

devices. Essentially, a high gain device is placed in the loop of the DC bias circuit of a RF device. The flicker noise generated by the RF device is then compared against the noise of the DC bias circuit and the result is an overall system phase noise improvement [8].

When selecting a RF transistor to be used in the amplifier it was also desirable to use the same transistor in the oscillator design. The BFP640 from Infineon was selected because it exhibits high gain and low noise performance. The BFP640 is made in Silicon Germanium (SiGe) technology and has a typical transition frequency (f_T) of 40 GHz. This device is commonly used in dielectric resonator oscillators (DRO) utilized in direct broadcast satellite low noise blocks (LNB) [9] as well as in low noise amplifiers for global positioning devices [10]. The next device to select was the PNP transistor used in the active bias circuit. The BF723 from NXP Semiconductors was chosen because it exhibited a low transition frequency of 60 MHz with a reasonably high DC current gain of 50. Low transition frequency and high current gain are important parameters for this device in order to minimize the higher frequency effects added to the circuit and to suppress the up-converted baseband flicker noise.

Simulation

The modeling and simulation of the amplifier were performed in the Advancing the Wireless Revolution (AWR) Design Environment (DE). AWR Corporation offered an extended demonstration license to be able to support this effort. This license included all of the features that come with the standard

purchased version. Both the BFP640 and the BF723 included non-linear models provided by the manufacturer. Table 2 shows the transistor parameters used in the Gummel-Poon model for the BFP640. Figure 1 shows the package parasitic characteristics of the BFP640 used in the simulation. Table 3 shows the transistor parameters of the Gummel-Poon model for the BF723 PNP transistor. The Gummel-Poon model is commonly used because it includes the DC current effects on the current gain of the device that other models such as the Ebers-Moll model do not include [11].

Table 2: Gummel-Poon Model of BFP640 [12]

Transistor Chip Data:

IS =	0.22	fA	BF =	450	-	NF =	1.025	-
VAF =	1000	V	IKF =	0.15	A	ISE =	21	fA
NE =	2	-	BR =	55	-	NR =	1	-
VAR =	2	V	IKR =	3.8	mA	ISC =	400	fA
NC =	1.8	-	RB =	3.129	Ω	IRB =	1.522	mA
RBM =	2.707	Ω	RE =	0.6	-	RC =	3.061	Ω
CJE =	227.6	fF	VJE =	0.8	V	MJE =	0.3	-
TF =	1.8	ps	XTF =	10	-	VTF =	1.5	V
ITF =	0.4	A	PTF =	0	deg	CJC =	67.43	fF
VJC =	0.6	V	MJC =	0.5	-	XCJC =	1	-
TR =	0.2	ns	CJS =	93.4	fF	VJS =	0.6	V
MJS =	0.27	-	XTB =	-1.42	-	EG =	1.078	eV
XTI =	3	-	FC =	0.8		TNOM	298	K
AF =	2	-	KF =	7.291E-11				
TITF1	-0.0065	-	TITF2	1.0E-5				

All parameters are ready to use, no scalling is necessary.

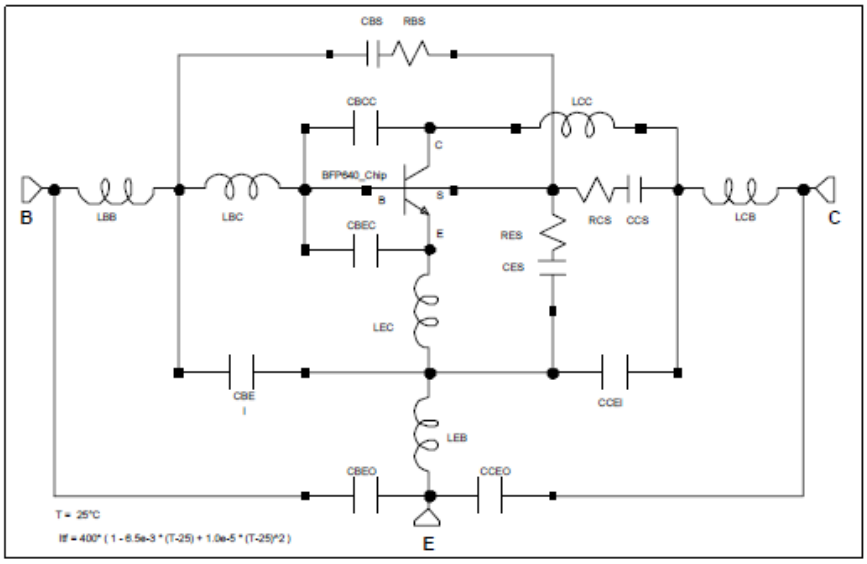

Figure 1: Package Parasitic Characteristics of BFP640

Table 3: Gummel-Poon Model of BF723 [13]

IS	5.35e-13	mA				0	0	Saturation current
IBE		mA				0	0	Reverse BE saturation current
IBC		mA				0	0	Reverse BC saturation current
BF	140					0	0	Fwd current gain
NF	0.873					0	0	Fwd ideality factor
VAF	149	V				0	0	Fwd Early voltage
IKF	24.1	mA				0	0	Fwd current knee
ISE	9.81e-14	mA				0	0	BE leakage current param
NE	1.03					0	0	BE leakage ideality factor
BR	0.01					0	0	Rev current gain
NR	0.984					0	0	Rev ideality factor
VAR	91.8	V				0	0	Rev Early voltage
IKR	1000	mA				0	0	Rev current knee
ISC	1e-10	mA				0	0	BC leakage current param
NC	2					0	0	BC leakage ideality factor
RB	19.9	Ohm				0	0	Base resistance
IRB	11	mA				0	0	Current where RB falls halfway to min
RBM	0.0241	Ohm				0	0	Minimum high-current base resistance
RE	0.0185	Ohm				0	0	Emitter resistance
RC	2.22	Ohm				0	0	Collector resistance
CJE	42	pF				0	0	CJ0 for BE junction
VJE	0.3	V				0	0	BE built-in potential
MJE	0.413					0	0	BE grading coefficient
TF	1.11	ns				0	0	Fwd transit time
XTF	576					0	0	Coef for bias dependence of TF
VTF	999000	V				0	0	Voltage for VBC dependence of TF
ITF	3000	mA				0	0	High-current parameter for TF
PTF	0					0	0	Excess phase param; must be degrees
CJC	16.5	pF				0	0	CJ0 for BC junction
VJC	0.3	V				0	0	BC built-in potential
MJC	0.7					0	0	BC grading coefficient
XCJC	1					0	0	Fraction of CBC to internal node
TR	0	ns				0	0	Rev transit time
CJS	0	pF				0	0	CJ0 for substrate capacitance
VJS	0.75	V				0	0	Built-in potential for substrate cap
MJS	0.33					0	0	Substrate cap grading coeff
XTB	0					0	0	Temperature scaling term for beta
EG	1.11					0	0	Energy gap at T=TNOM
XTI	3					0	0	Temperature scaling term
KF	0					0	0	Flicker noise coefficient
AF	1					0	0	Flicker noise exponent
FFE	1					0	0	Flicker noise frequency exponent
FC	0.5					0	0	Coefficient for forwar[Parameter descriptio
NKF	0.5					0	0	Exponent for high-current Beta roll-off
TNOM	27	DegC				-273.15	-273.15	Nominal temperature (parameter extractior
TEMP	27	DegC				-273.15	-273.15	Simulation temperature

The next step of the design was to select a DC operating point for the RF transistor. The goal was to select an operating point that would give sufficient output power, have relatively low noise, and operate in the class A region. Figure 2 shows the simulation test bench of how the BFP640 was evaluated. Figure 3 shows the collector-emitter voltage versus the collector current (IV curve) of the

device. The DC bias point was selected to be 3 V at 30 mA to achieve the desired goals.

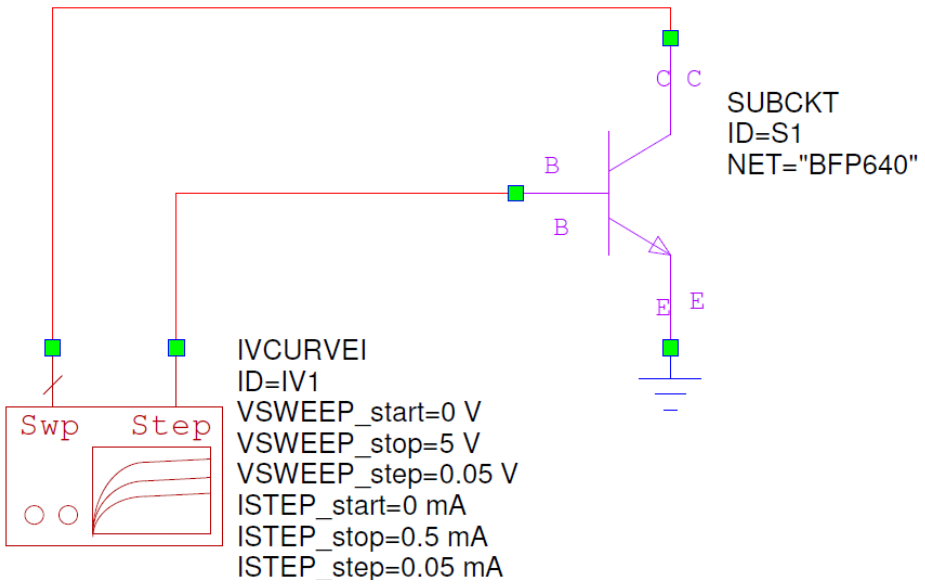

Figure 2: Simulation Test Bench of BPF640 IV Curve

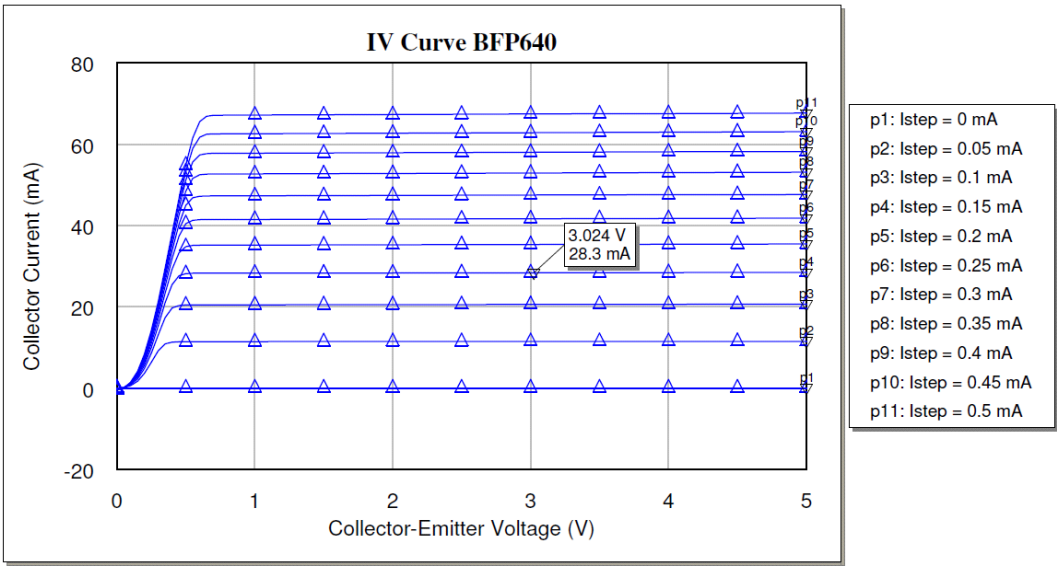

Figure 3: IV Curve of BFP640

The resistive biased circuit was designed first to the design goals shown in Table 1 previously. The active biased circuit was then designed by taking the resistive biased circuit and adding the PNP transistor to bias the base of the RF transistor. All input and output matching networks remained the same. The schematic for the resistive biased circuit is shown in Figure 4 while the schematic for the active biased circuit is shown in Figure 5.

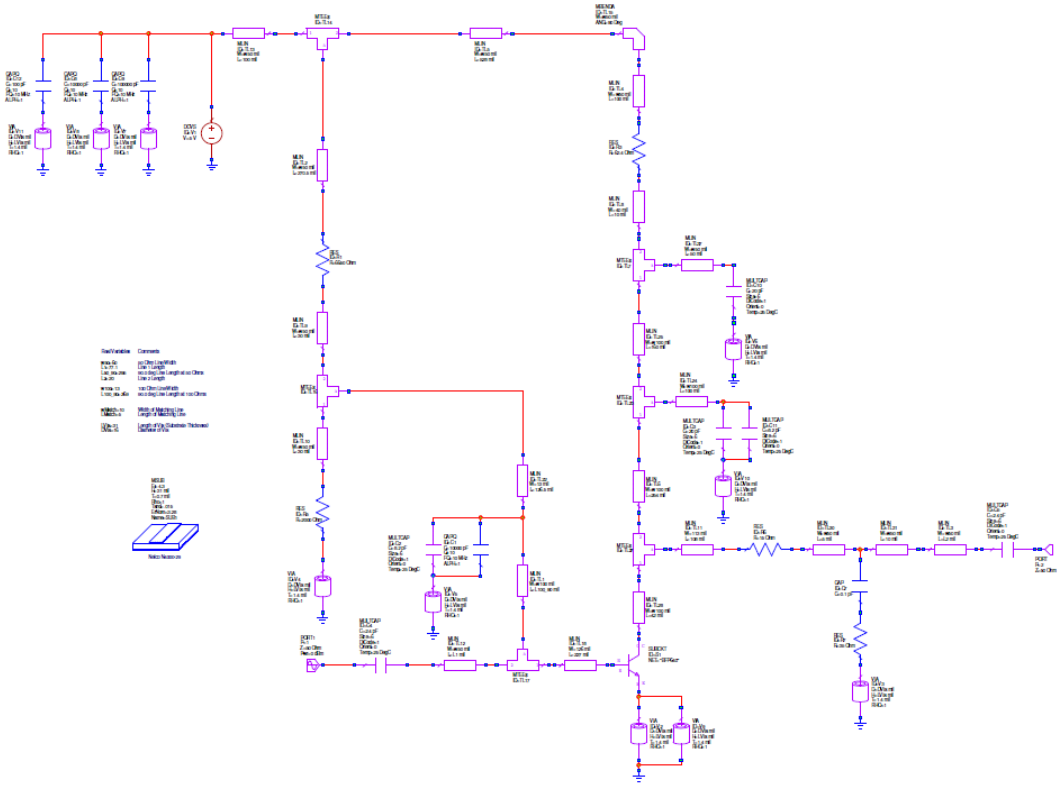

Figure 4: Schematic of Resistive Biased Amplifier

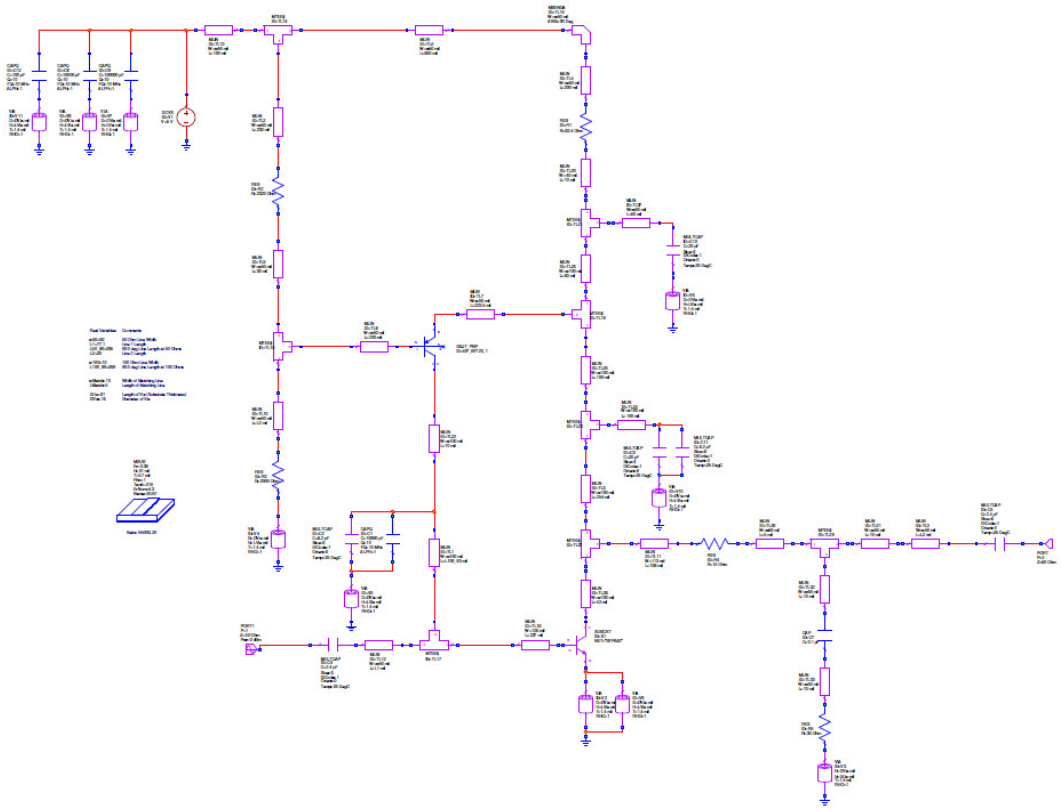

Figure 5: Schematic of Active Biased Amplifier

The stability coefficients were plotted along with the gain to ensure that the amplifiers are unconditionally stable as shown in Figures 6 and 7 for the resistive and active biased circuits respectively. The stability coefficient μ refers to the input, while the stability coefficient μ' refers to the output. Either μ or μ' can determine whether or not an amplifier is unconditionally stable. Unconditional stability is achieved according to the simulation because μ is greater than 1 for all frequencies where |S21| is positive.

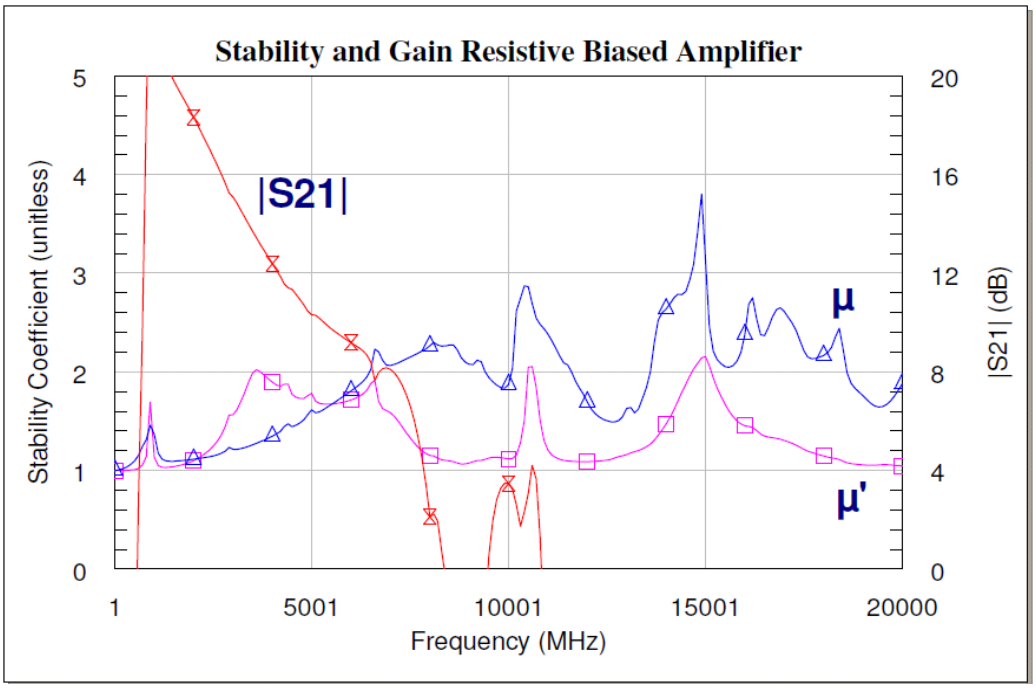

Figure 6: Stability of Resistive Biased Amplifier

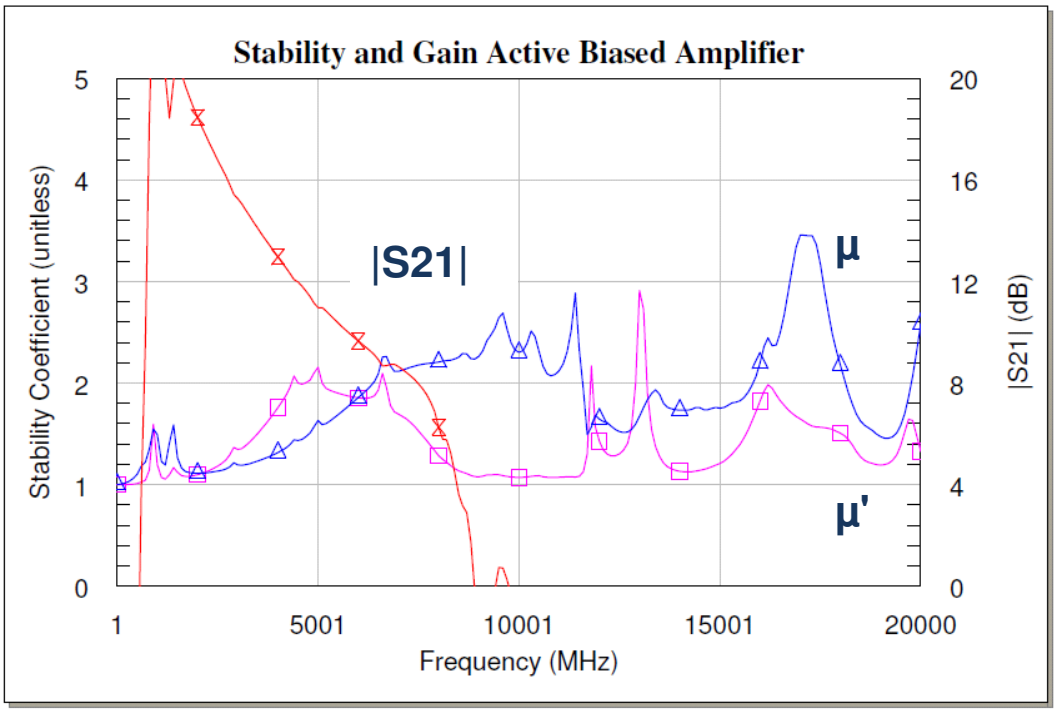

Figure 7: Stability of Active Biased Amplifier

A closer look at the gain over the frequency of interest for each circuit is shown in Figures 8 and 9 while the return loss is shown in Figures 10 and 11.

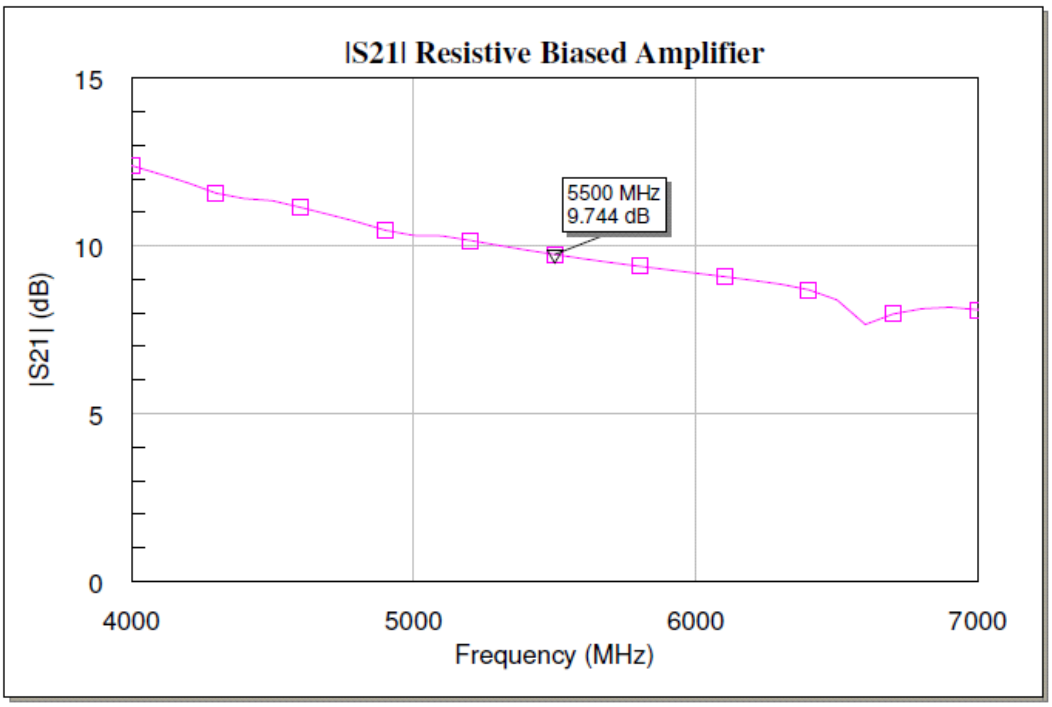

Figure 8: Gain of Resistive Biased Amplifier

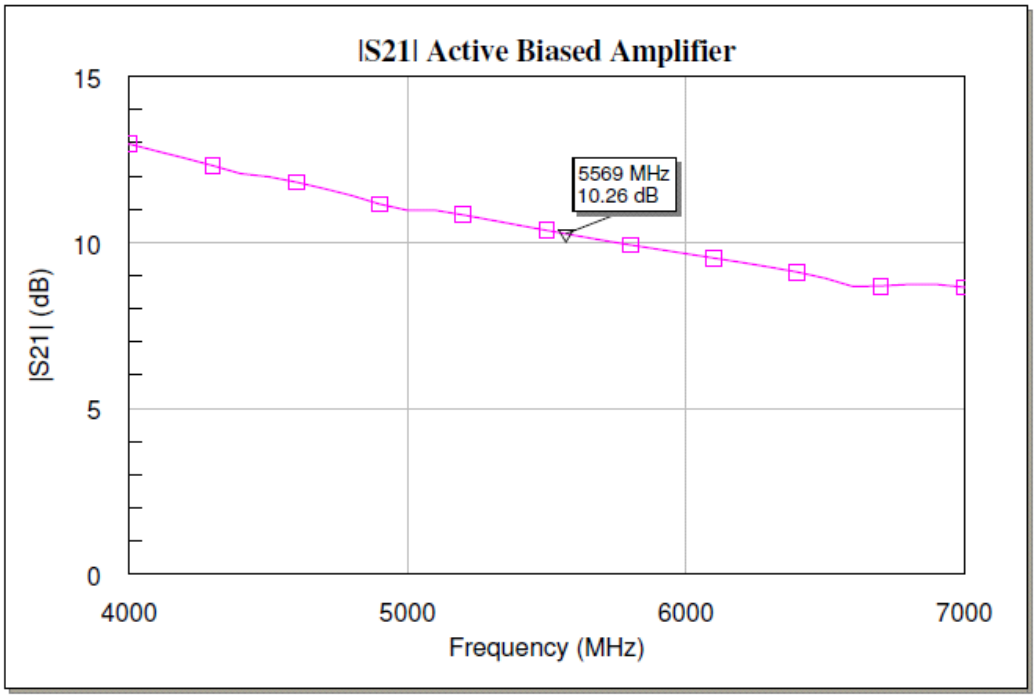

Figure 9: Gain of Active Biased Amplifier

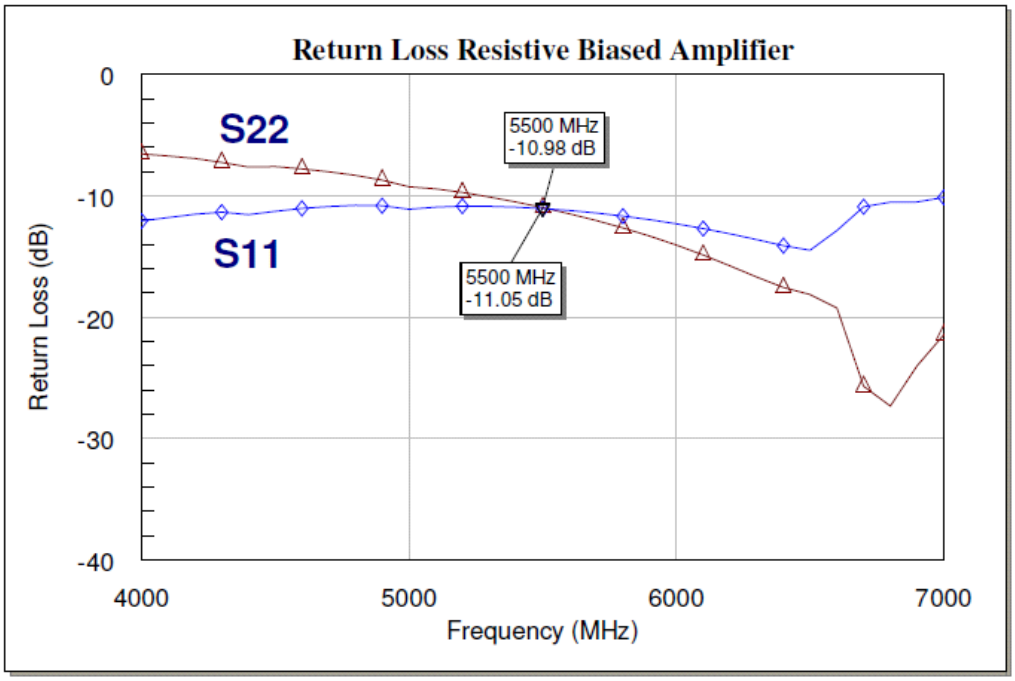

Figure 10: Return Loss of Resistive Biased Amplifier

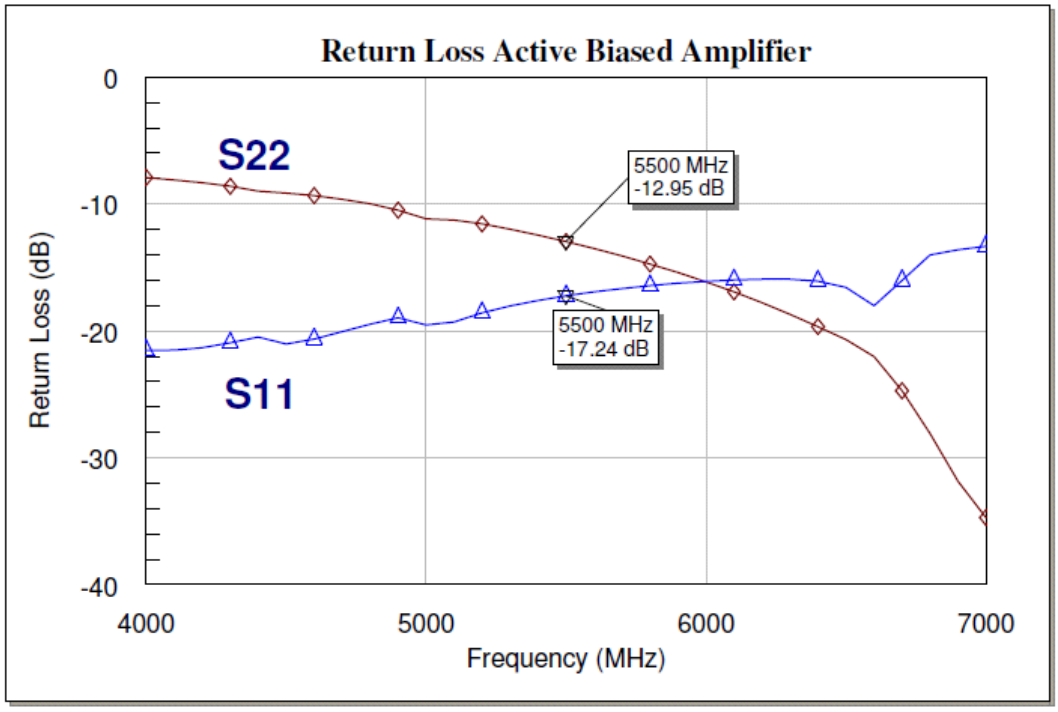

Figure 11: Return Loss of Active Biased Amplifier

Simulation of the linear noise voltage is a good first pass approach to see if there will be an improvement in the residual phase noise. The linear noise voltage for both the active and resistive circuits is shown in Figure 12. As can be seen, the results of the linear noise voltage simulation strongly suggest that an improvement in the residual phase noise performance will be obtained.

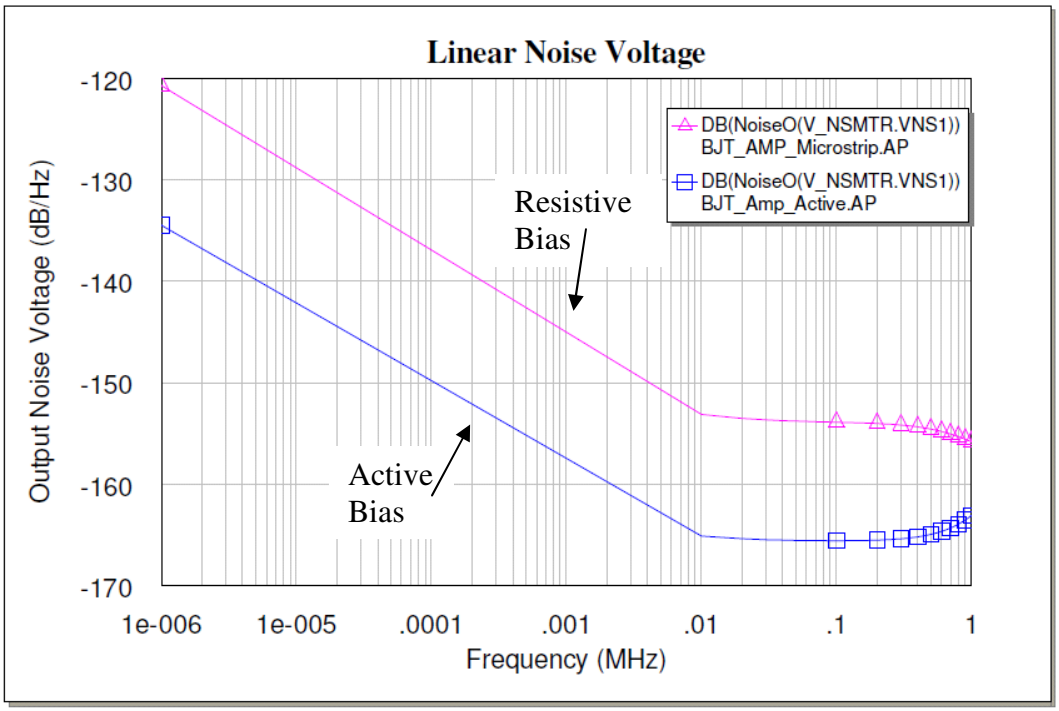

Figure 12: Linear Noise Voltage

The simulations showed that both amplifiers were stable and that the design goals were met. At this point, a physical layout was performed.

Design Layout

The physical layout was designed in AutoCAD and then the Gerber files were generated in Altium Designer Winter 09 edition. Figure 13 shows the layout of the resistive biased amplifier. Figure 14 shows the layout of the active biased amplifier. The input and output matching circuits are the same for both of these designs with the only difference being bias circuitry. The circuit card was built out of Nelco N4000-29 FR4 material with a substrate thickness of 31 mils. The copper thickness is one-ounce copper with Electroless Nickel Immersion Gold

(ENIG) plating. Prototron Circuits in Tucson, AZ fabricated the circuit card and the assembly was done at the Raytheon plant site in Tucson. The bill of materials (BOM) for the resistive and active biased amplifiers is shown in Table 4 and Table 5 respectively.

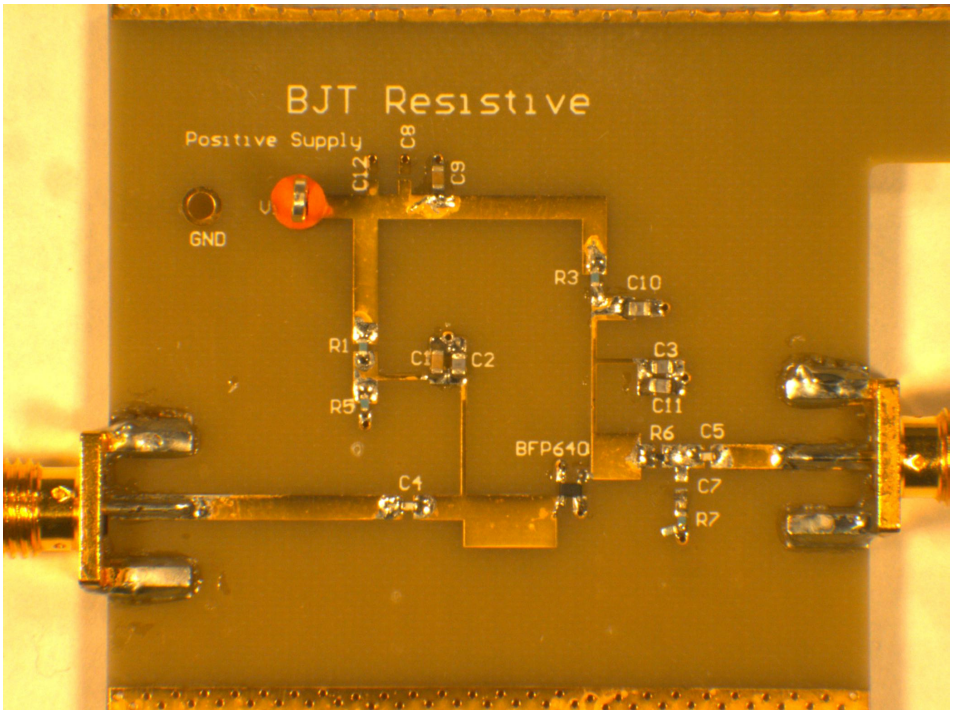

Figure 13: Resistive Biased Amplifier

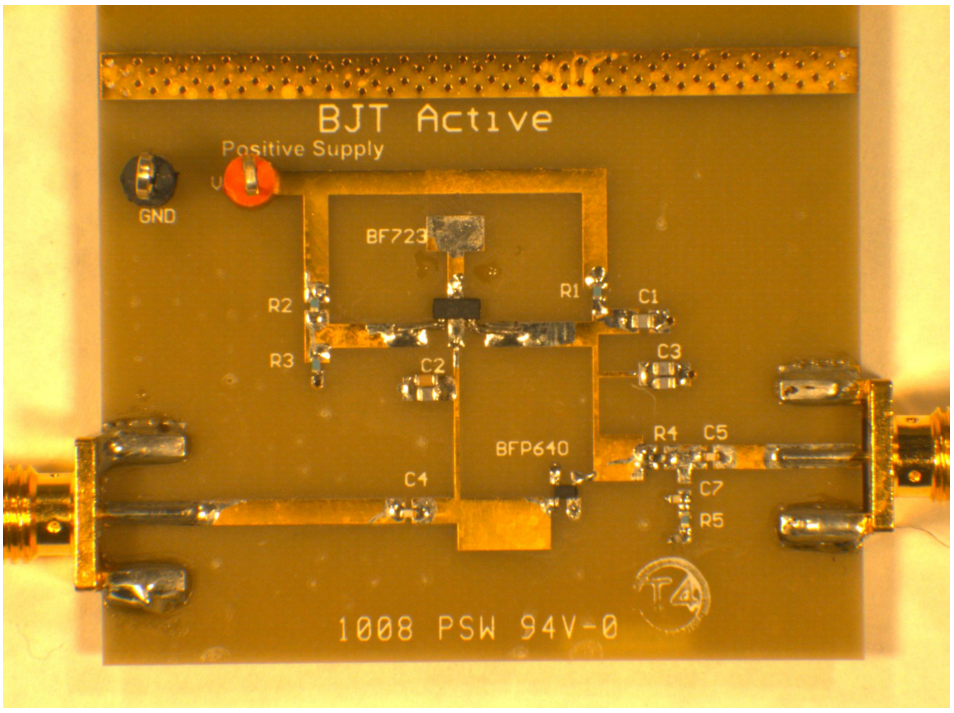

Figure 14: Active Biased Amplifier

Table 4: Bill of Materials for Resistive Biased Amplifier

Reference Designator	Comment	Part Number	Manufacturer
R1	6.65K Ohm Resistor	RK73H1ETTP6651F	KOA
R5	2K Ohm Resistor	RK73H1ETTP2001F	KOA
R6	15 Ohm Resistor	RK73H1ETTP15R0F	KOA
C1, C9	0.01 µF Capacitor	500R14W103KV4T	Johanson
C2, C11	10 pF Capacitor	C04UL100JC-6SN-X0B	Dielectric Laboratories
C4, C5	2.4 pF Capacitor	C04UL2R4C-6SN-X0B	Dielectric Laboratories
C7	0.2 pF Capacitor	C04UL0R2C-6SN-X0B	Dielectric Laboratories
C3, C10	22 pF Capacitor	C06F220J-9ZN-X1B	Dielectric Laboratories
R3	63.4 Ohm Resistor	RK73H1ETTP63R4F	KOA
R7	34.8 Ohm Resistor	RK73H1ETTP34R8F	KOA
S1	RF SiGe NPN Transistor	BFP640	Infineon

Table 5: Bill of Materials for Active Biased Amplifier

Reference Designator	Comment	Part Number	Manufacturer
R2	2.32K Ohm Resistor	RK73H1ETTP2321F	KOA
R3	2K Ohm Resistor	RK73H1ETTP2001F	KOA
R4	15 Ohm Resistor	RK73H1ETTP15R0F	KOA
C1	0.01 µF Capacitor	500R14W103KV4T	Johanson
C2, C11	10 pF Capacitor	C04UL100JC-6SN-X0B	Dielectric Laboratories
C4, C5	2.4 pF Capacitor	C04UL2R4C-6SN-X0B	Dielectric Laboratories
C7	0.2 pF Capacitor	C04UL0R2C-6SN-X0B	Dielectric Laboratories
C3, C10	22 pF Capacitor	C06F220J-9ZN-X1B	Dielectric Laboratories
R1	63.4 Ohm Resistor	RK73H1ETTP63R4F	KOA
R5	34.8 Ohm Resistor	RK73H1ETTP34R8F	KOA
S1	RF SiGe NPN Transistor	BFP640	Infineon
GP_BF723_1	PNP Transistor	BF723	NXP

Test Setups

Two main tests were performed in order to validate the design and to look for residual phase noise reduction. The first test was done on a network analyzer in order to measure the s-parameters. The s-parameter data shows the return loss, gain, and bandwidth of the amplifiers across a given frequency range. The test setup is shown in Figure 15. The second test was done using a residual phase noise test station designed by Aeroflex. The test setup is shown in Figure 16. A picture of the Aeroflex test setup is shown in Figure 17. For a more detailed explanation of how to setup the Aeroflex phase noise test station, please refer to Appendix A.

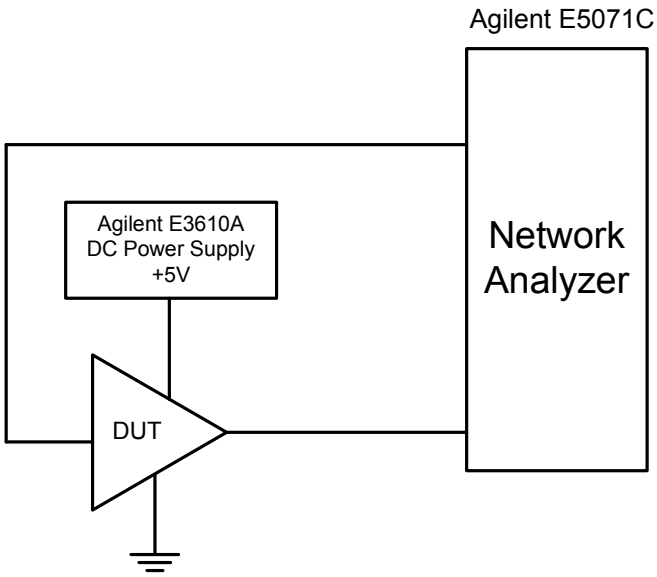

Figure 15: S-Parameter Test Setup

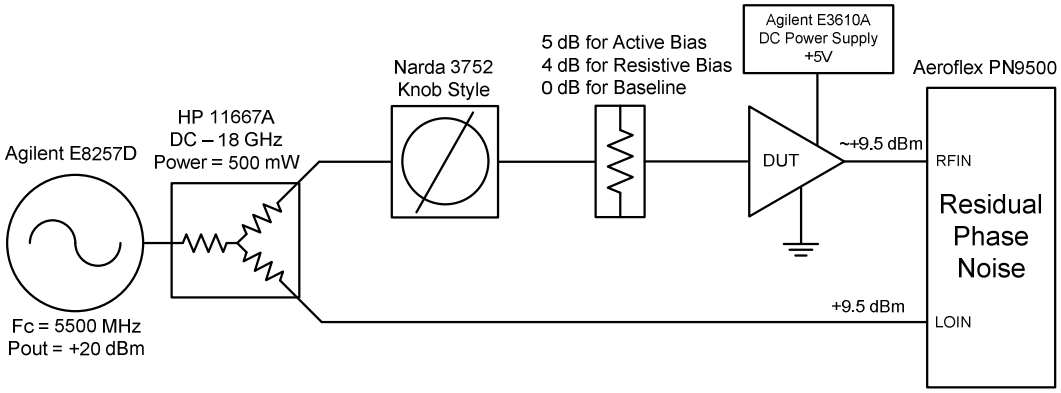

Figure 16: Residual Phase Noise Test Setup

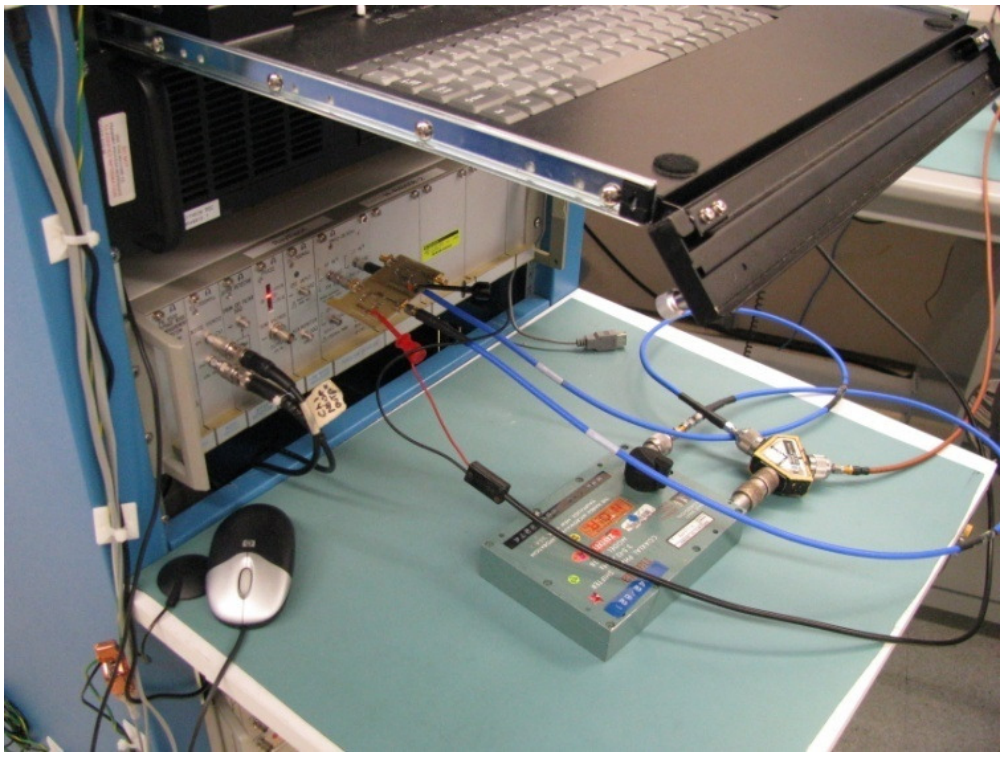

Figure 17: Picture of Residual Phase Noise Test Setup

Test Results

The s-parameter data for the resistive biased amplifier is shown in Figure 18 while the s-parameter data for the active biased amplifier is shown in Figure 19. For both amplifiers, the data follows the same trends as the simulation predicted. The overall gain was lower than predicted by 5 dB which was partially expected due to real parts, inaccuracies in the models, circuit card etching tolerances, and connectors being introduced that were not accounted for in the simulation. Even with the reduction in gain, there was enough gain out of the circuit to obtain valid phase noise measurements. As stated previously, the goal of the amplifiers was not to make a high gain device, but to make one that was stable and so no further effort was taken to try to increase the gain.

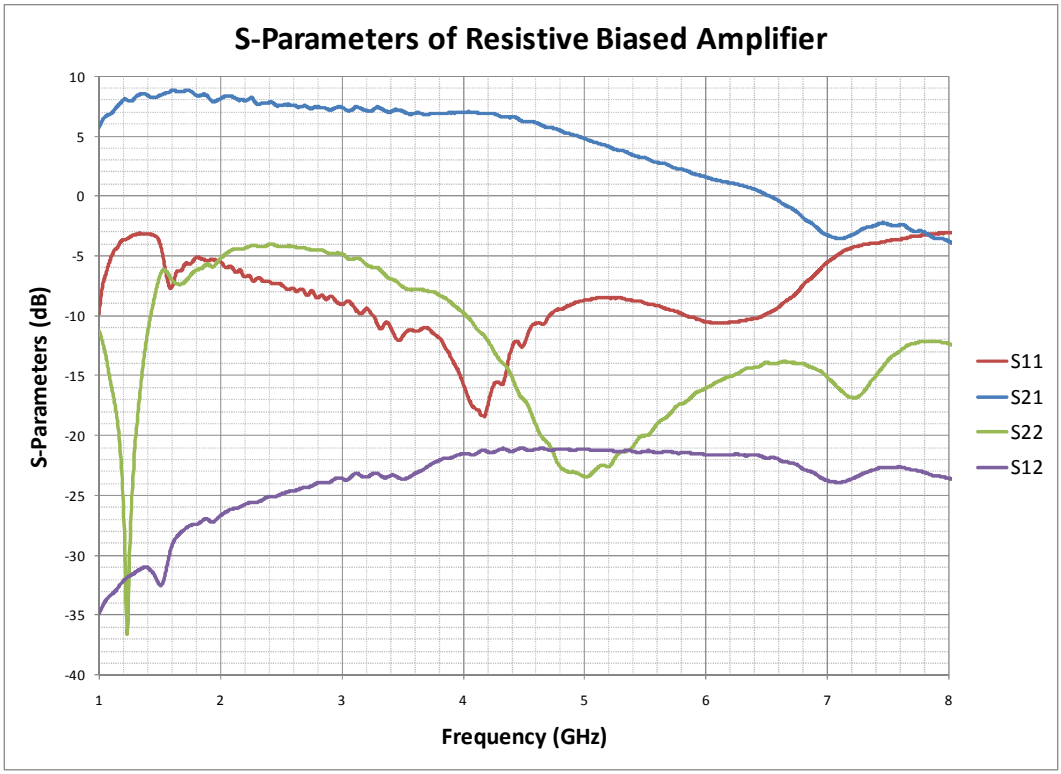

Figure 18: S-Parameter Data for Resistive Biased Amplifier

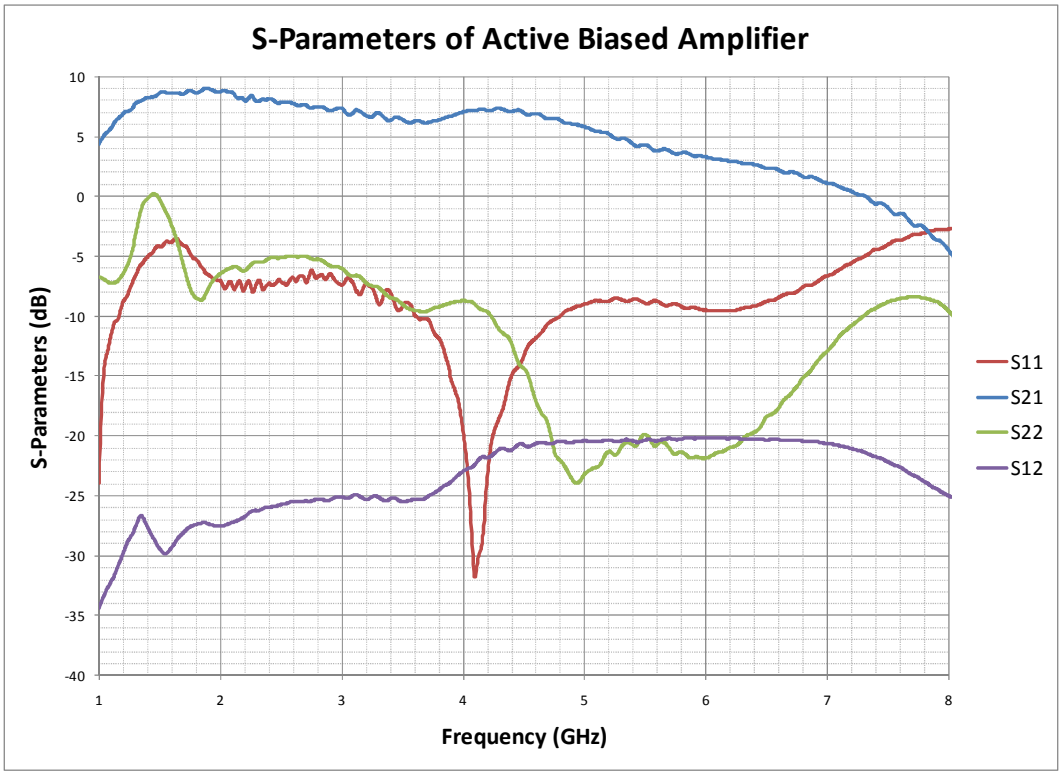

Figure 19: S-Parameter Data for Active Biased Amplifier

The testing of residual phase noise was done by comparing the system noise floor with that of the system with the resistive or active biased amplifiers included. The reason that the testing was done in this manner was to make sure that the results of the device under test were not buried in the system performance. The test results are shown in Figure 20. Both the active and resistive biased amplifiers add degradation in the overall residual phase noise when compared to the test station baseline measurement which shows that the test station has a low enough noise floor to properly characterize the amplifiers. The residual phase noise of the active biased amplifier showed about 15 dB improvement, when compared to the resistive biased amplifier at 100 Hz and 1 KHz offset frequencies as well as improved phase noise at higher offset

frequencies. The high improvement in close-in phase noise verified that active biasing can lower the flicker noise degradation that is characteristic of silicon type devices.

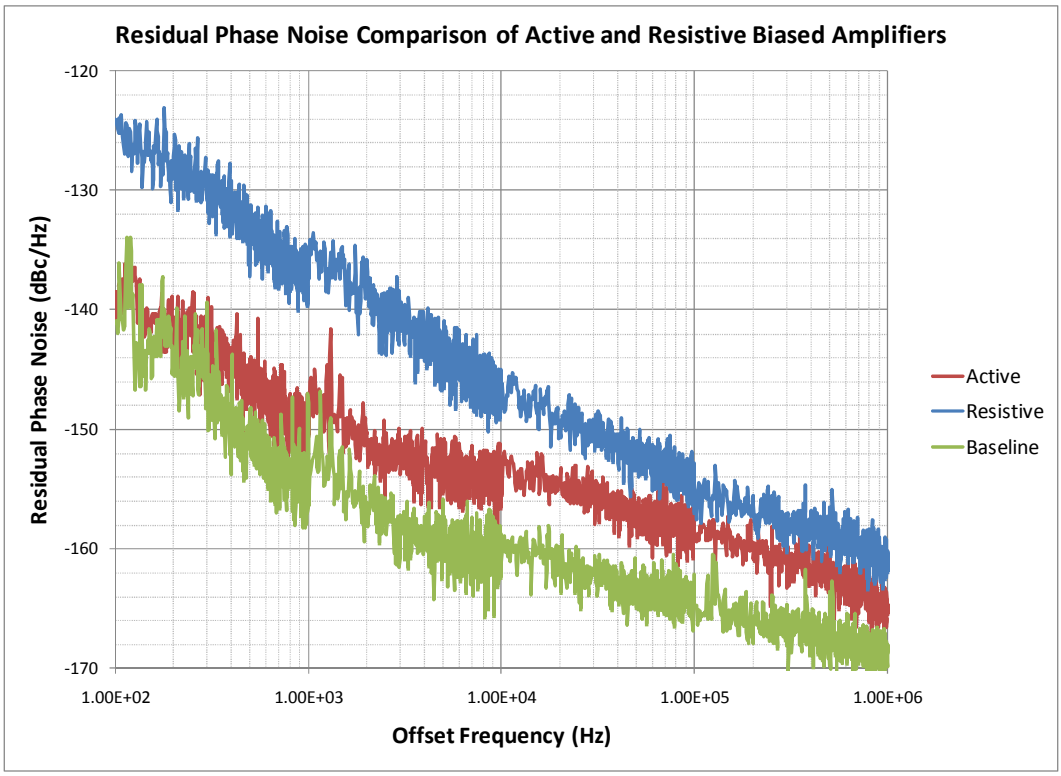

Figure 20: Residual Phase Noise Test Results

Chapter 4

Voltage Controlled Oscillator

Designing the amplifier in the previous section was done in order to gain confidence in the simulator and to prove that active biasing had the potential to reduce phase noise in voltage controlled oscillators. The next section will discuss the implementation of active biasing into a BJT negative-resistance based VCO.

Design Parameters

Typical design parameters for VCO circuits include, but are not limited to frequency range, tuning voltage, phase noise, output power, and power consumption. Table 6 shows the main parameters and design goals that were investigated in the design of the BJT negative-resistance VCO. The frequency tuning range was desired to be between 4000 MHz and 7000 MHz. In order to obtain this amount of bandwidth, a tradeoff between tuning range and phase noise would be required. This tradeoff is due to the quality factor (Q) of the varactor diode. Tuning range was sacrificed in order to keep the phase noise low. The design goal for center frequency was arbitrarily chosen to be 5500 MHz with 10% bandwidth but any center frequency between 4000 MHz and 7000 MHz is sufficient for this study.

Table 6: Design Goals of VCO

Design Goals	
Center Frequency	5500 MHz
Frequency Tuning Range	10%
Phase Noise @ 100 KHz	< -110 dBc/Hz
Tuning Voltage	1 - 12 V
Output Power	> 10 dBm
Power Consumption	< 200 mW

Many topologies are commonly used in designing microwave VCO circuits including negative-resistance, Hartley, Pierce, Clapp, Colpitts, tuned-input / tuned-output, and other differential versions of those previously mentioned [4]. The negative resistance topology was chosen for this design because of how well it is understood by designers and the minimal need for passive elements in the high-Q resonating structure. By minimizing the amount of passive elements in the resonating structure, the limitation of tolerance and availability of component values was eliminated.

A varactor diode was used as the voltage dependent reactive element. Varactor diodes are characterized by the fluctuation in capacitance to tuning voltage. The greater the change in capacitance value, the lower the Q of the device resulting in lower VCO phase noise. However, with lower Q, a greater tuning range can be achieved. This concept is shown in equation four [4].

$$Q_U = \frac{1}{\omega C_T R_s} \qquad (4)$$

Q_U is the unloaded-Q, ω is the radian frequency, C_T is the total capacitance of the varactor diode, and R_s represents the series loss of the diode. Since SSB phase noise is being investigated, a higher Q varactor diode was selected at the expense of tuning range. The varactor diode selected was manufactured by M-Pulse Microwave as a commercial-off-the-shelf (COTS) item. An abrupt diode with part number MP6304 was selected due to the availability of the part as well as the high unloaded-Q of 5000 and the convenient surface mount package.

One approach to designing voltage controlled oscillators is to imagine the VCO as an unstable amplifier that meets oscillation start-up conditions. A method to make the amplifier potentially unstable is to have the stability criterion μ or μ' be less than one for all frequencies that are desired and greater than one for all other frequencies. One way to meet the start-up conditions is to satisfy the criteria shown in equations five and six when the assumption is made that μ or μ' is less than one in these regions [14].

$$\mathrm{Re}(Z_{IN}) < -150\Omega \qquad (5)$$

$$\mathrm{Im}(Zin) \approx 0 \quad \text{with the slope} < 0 \qquad (6)$$

The traditional way of determining stable oscillating conditions is known as the Nyquist Stability Test. This test involves plotting the transfer function against frequency in the complex plane and then looking at the number of right-half plane poles. Although this method is conventional and well understood, it does not make for a great design parameter. On the other hand, equations five and six can be plugged into an optimizer to come up with a solution very quickly.

As previously discussed in the amplifier design section, active biasing of the DC input has the potential to lower the flicker noise contribution to the overall phase noise. This was demonstrated in the residual phase noise improvement when compared against the resistive biased counterpart. This same biasing technique was investigated in the VCO design to see if improvements could also be made. Intuitively speaking, the VCO should benefit the same way that the amplifier did from active biasing since the VCO is basically an unstable amplifier.

SSB phase noise will be investigated by performing measurements of the current VCO design since an oscillator internally generates a signal without an input signal. For this reason, residual phase noise measurements are not used to characterize VCO circuits. SSB phase noise is often used as a key parameter of oscillators because it quantifies the fidelity or purity of the tone or signal at some frequency. SSB phase noise is a measure of how well this goal is being met.

The same SiGe BJT device that was used in the amplifier section will again be used in the design of the VCO. As with the amplifier, a low transition frequency high gain device was used in the active bias circuit. The amount of parts that meet this specification is very large due to the fact that audio transistors have been around for decades. Out of convenience, the ZTX705 PNP Darlington transistor was selected due to the availability of a library part and good simulation results.

Simulation

AWR software was again used to model and simulate the VCO design. The same non-linear model was used for the SiGe BPF640 transistor. The non-linear model for the PNP audio amplifier is shown in Table 7.

Table 7: Adapted Spice Model of ZTX705 [13]

GBJT_PNP	2	1	4	0	ID="Q1"	IS=3.35584e-014	BF=85	VAF=212
	NF=1.002	IKF=0.817	ISE=3.6e-013	NE=4.1	BR=24			
	VAR=6	NR=0.999	IKR=0.114	ISC=1.406e-013	NC=1.13			
	RB=1.1	RE=0.4	RC=0.0339	CJE=1e-010	CJC=3.7e-011			
	VJC=1.045	MJC=0.595	IRB=1e+015	MJE=0.33	MJS=0.33			
	VJE=0.75	VJS=0.75	VTF=0					
GBJT_PNP	4	1	3	0	ID="Q2"	AREA=4	IS=3.35584e-014	BF=85
	VAF=212	NF=1.002	IKF=0.817	ISE=3.6e-013	NE=4.1			
	BR=24	VAR=6	NR=0.999	IKR=0.114	ISC=1.406e-013			
	NC=1.13	RB=1.1	RE=0.4	RC=0.0339	CJE=1e-010	CJC=3.7e-011		
	VJC=1.045	MJC=0.595	IRB=1e+015	MJE=0.33	MJS=0.33			
	VJE=0.75	VJS=0.75	VTF=0					

The DC bias point used in the amplifier design was again used for the VCO design because it is good for relatively low noise and high output power. The DC collector-to-emitter voltage used was 3 V with a collector current of 30 mA. According to equation three, noise figure and output power are contributors to the overall phase noise and are greatly affected by the DC bias conditions. The higher the output power and the lower the noise figure, the better the overall performance should be. Also, high output power is desirable so that additional amplifiers may be eliminated at the next level of assembly.

The next step in the simulation was to apply the negative-resistance architecture to a common-emitter BJT topology. This topology involves placing the resonating element on the base of the BJT, the collector matched to the output, and the emitter connected to ground. The DC bias voltage was then introduced into the design. A method used to decouple the power supply from the RF

performance is done by placing capacitors at a phase angle of 90 degrees on a high impedance line. This technique of using 90 degree lines decouples the effects of the power supply because at that point, the capacitors look like an alternating current (AC) open. The VCO stability was greatly influenced by the transmission line connected to ground that was placed on the emitter pin of the BJT. The use of a transmission line made the VCO unstable from 4 - 7 GHz and unconditionally stable elsewhere. The stability parameters for the resistive and active biased VCO circuits are shown in Figure 21 and Figure 22 respectively.

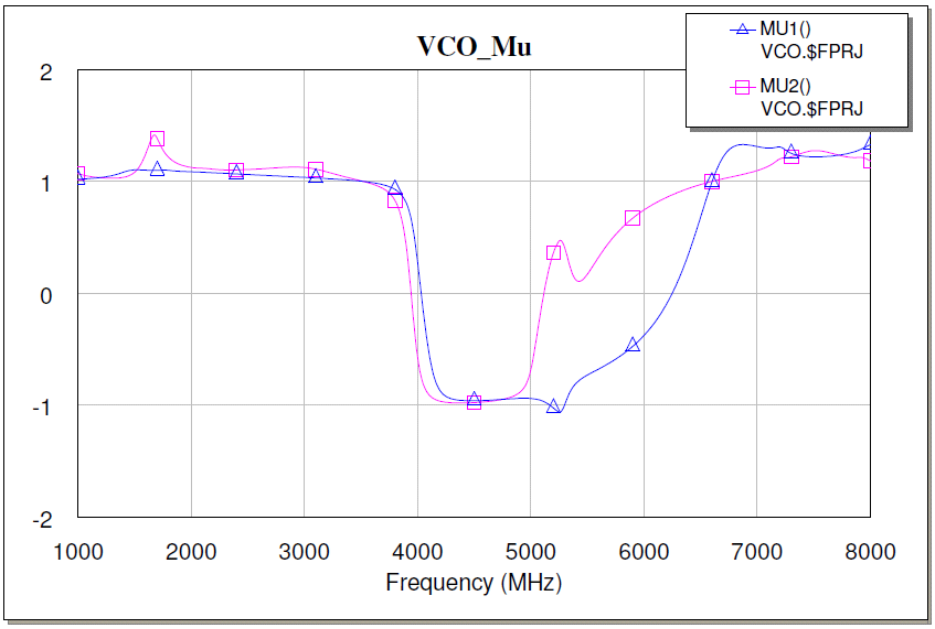

Figure 21: Stability Parameter of Resistive Biased VCO

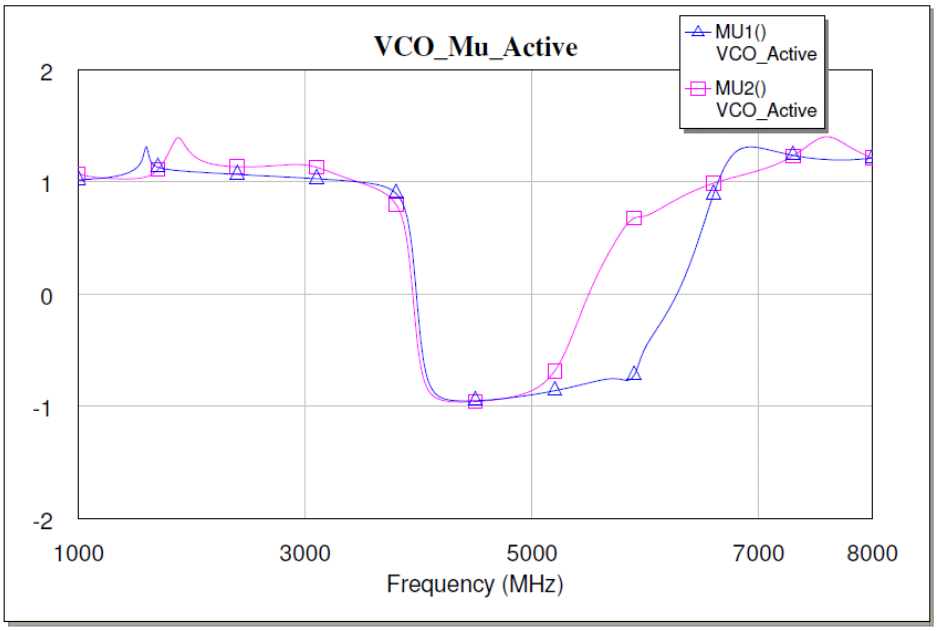

Figure 22: Stability Parameter of Active Biased VCO

When μ is > 1 the circuit is unconditionally stable and when μ is < 1 the circuit is potentially unstable. If the circuit is unstable then there is potential for oscillation, if the right start-up conditions present themselves. As stated in equations five and six previously, oscillations will occur when the real part of the input impedance is less than 150 Ohms and the imaginary part of the input impedance has a negative slope and is crossing zero. To get these conditions, the matching elements at the collector pin as well as the transmission line going to the varactor diode on the base pin were given to the optimizer tool as points of tuning. Within a minute of the optimizer running, the desired values were found. The input impedance for these values is shown in Figure 23. The input impedance is referenced to looking into the base of the BJT. The frequency that the start-up conditions achieved could be varied by changing the capacitance value of the

varactor diode to simulate an applied tune voltage. The schematic diagrams for the resistive and active biased VCO circuits are shown in Figures 24 and 25 respectively.

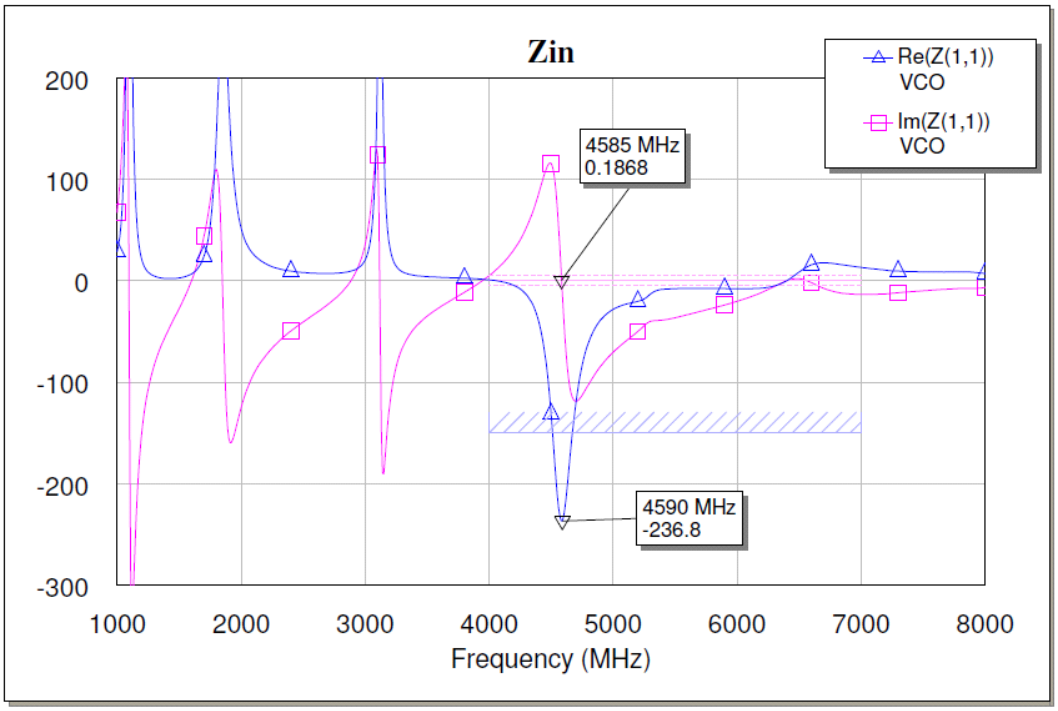

Figure 23: Input Impedance of the VCO

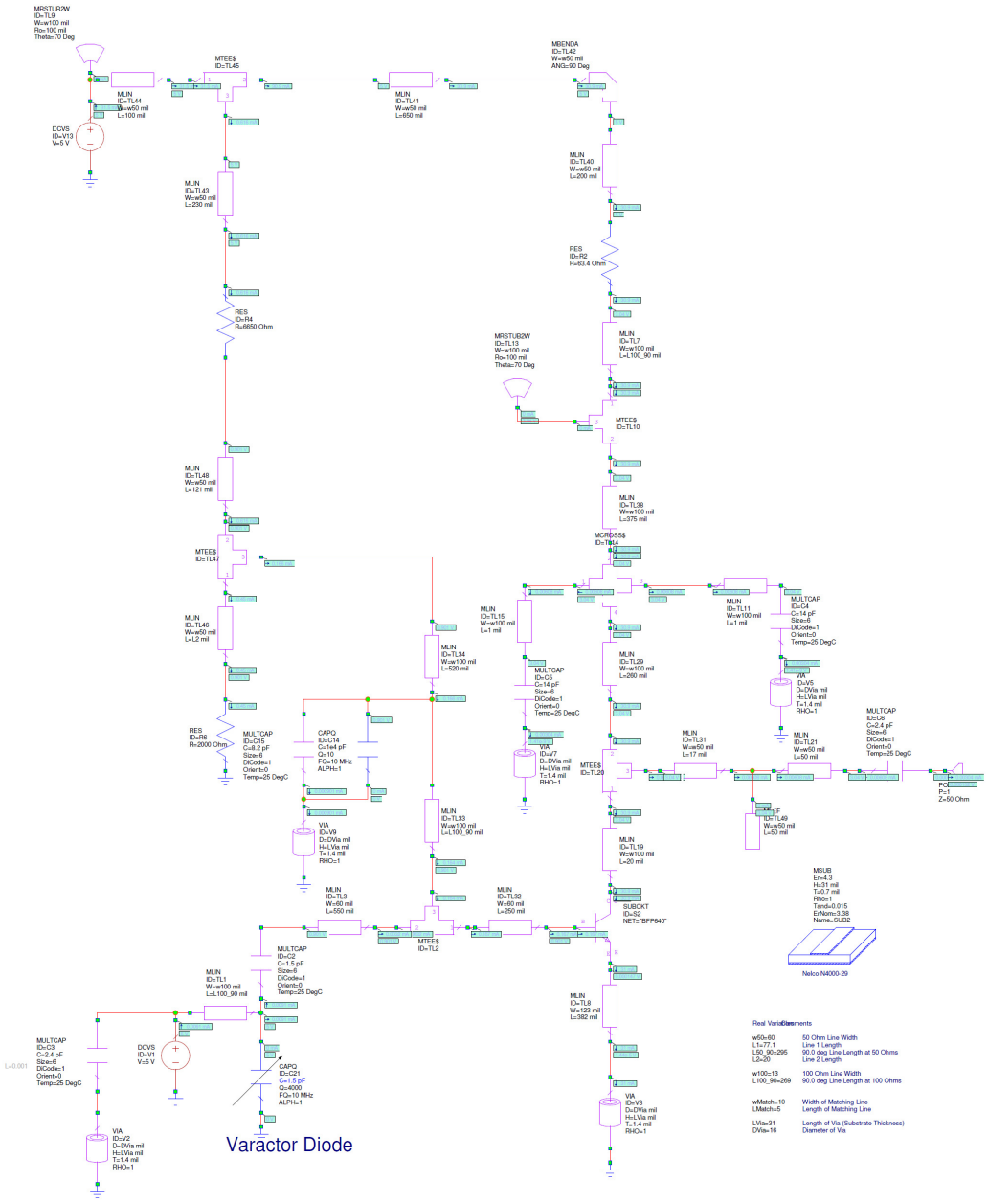

Figure 24: Schematic of Resistive Biased VCO

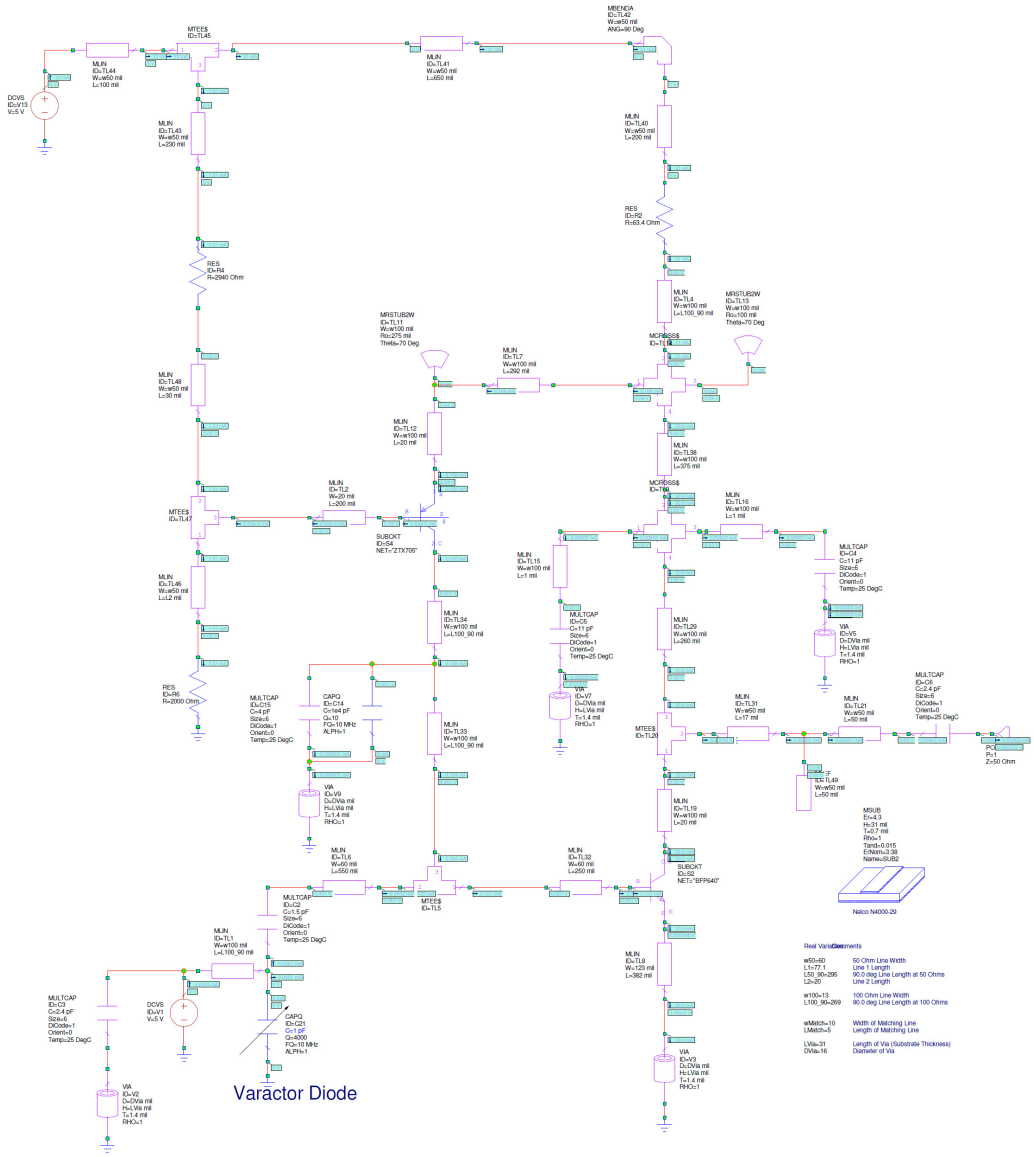

Figure 25: Schematic of Active Biased VCO

In order to find out the frequency of oscillation and the output power, a harmonic balance simulation was performed. In AWR the harmonic balance can be simulated using the Aplac-HB simulator. An Oscaprobe token was placed in the resonating structure near the base pin in order for the simulator to look at the oscillating conditions. The simulation setup is shown in Figure 26. After placing

the Oscaprobe token and setting up the measurement, a simulation was executed. The results of the active and resistive biased VCO harmonic balance simulations are shown in Figure 27.

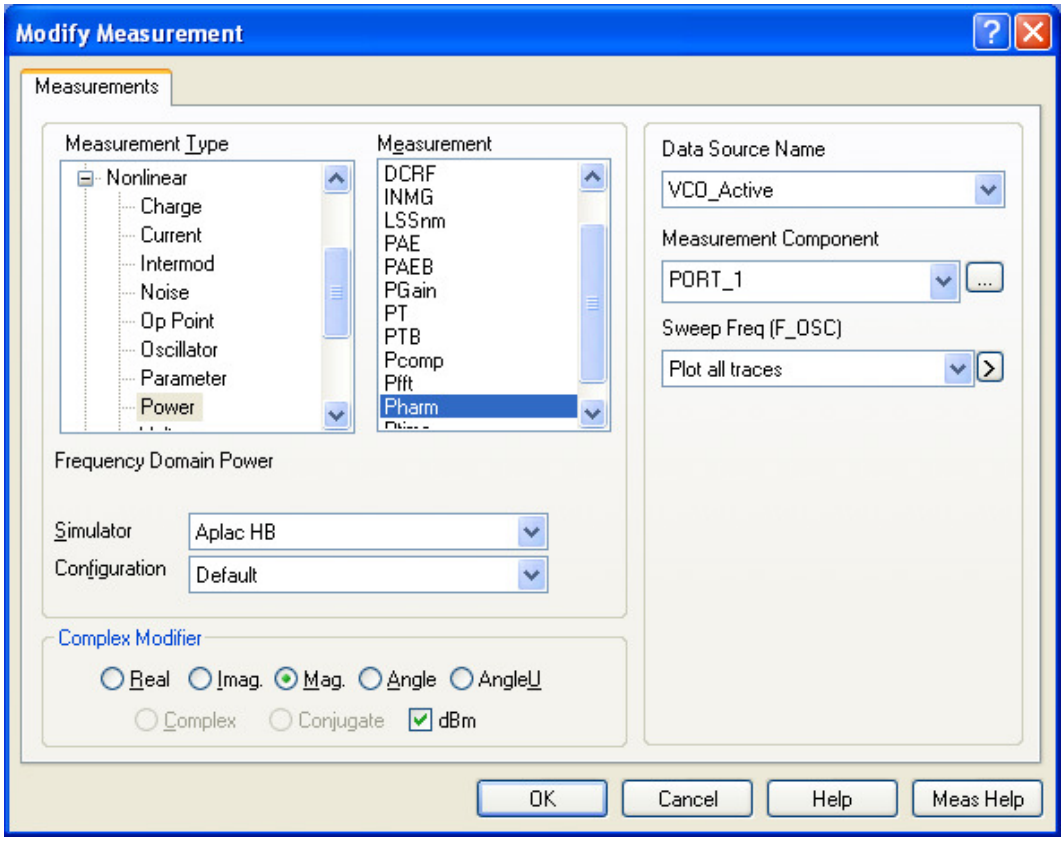

Figure 26: Harmonic Balance Measurement Setup

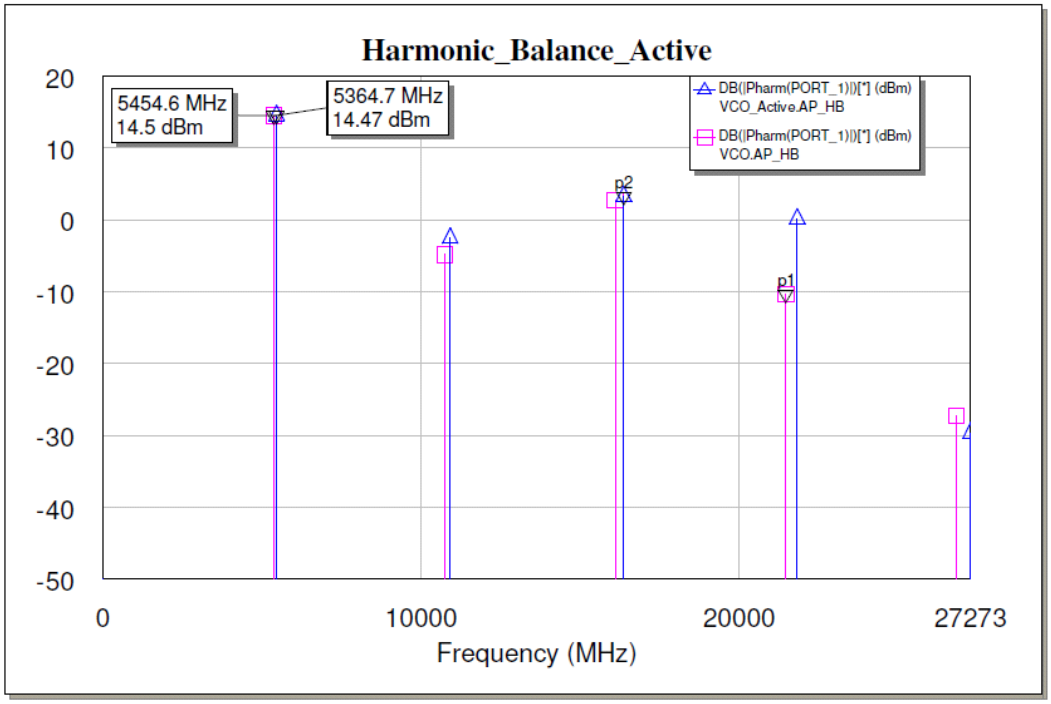

Figure 27: Harmonic Balance of Active and Resistive Biased VCO

The final parameter that was simulated was the SSB phase noise. Again, the Aplac-HB simulator in AWR was used for this measurement. This measurement setup is shown in Figure 28. The results of the active and resistive biased VCO phase noise simulations are shown in Figure 29. As anticipated, a lower phase noise was shown at the smaller offset frequencies for the active biased VCO when compared to the resistive biased design.

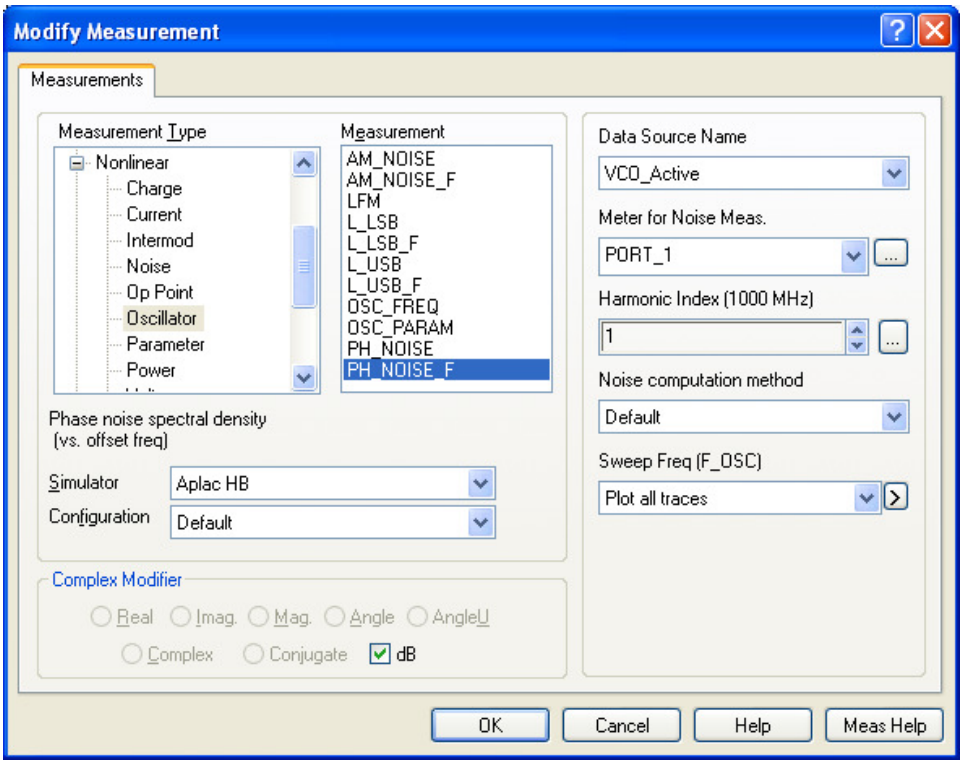

Figure 28: Phase Noise Measurement Setup

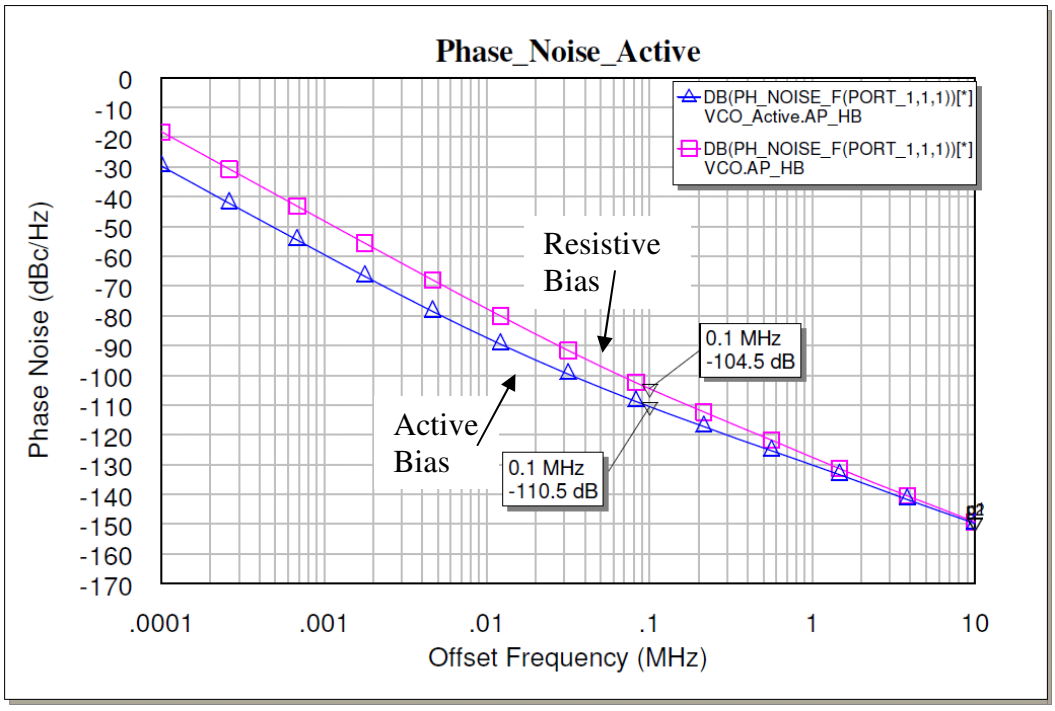

Figure 29: Phase Noise Simulation for the Active and Resistive Biased VCO

Design Layout

As before, the physical layout was designed in AutoCAD and then the Gerber files were generated in Altium Designer Winter 09 edition. Figure 30 shows the layout of the resistive biased VCO while Figure 31 shows the layout of the active biased VCO. The resonating structure and output matching circuits are the same for both of these designs with the only difference being bias circuitry. The circuit card was built out of Nelco N4000-29 FR4 material with a substrate thickness of 31 mils which was the same as the two amplifiers previously built. The copper thickness is half-ounce copper with hot-air-solder-leveling (HASL) plating. Prototron Circuits fabricated the circuit card and the assembly was done at the Raytheon plant site in Tucson. The bill of materials for the resistive and active biased VCO circuits is shown in Table 8 and Table 9 respectively.

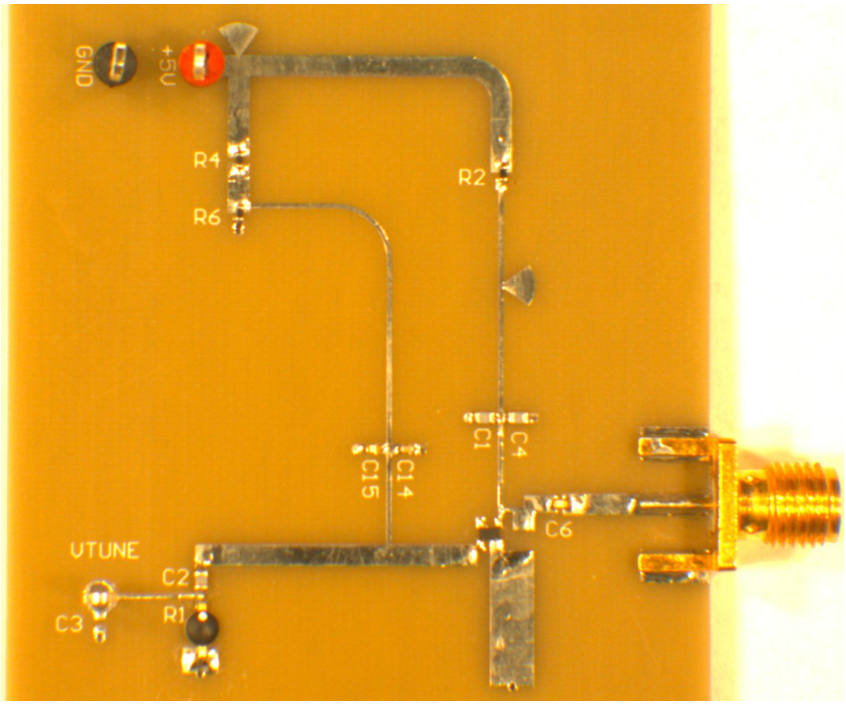

Figure 30: Resistive Biased VCO

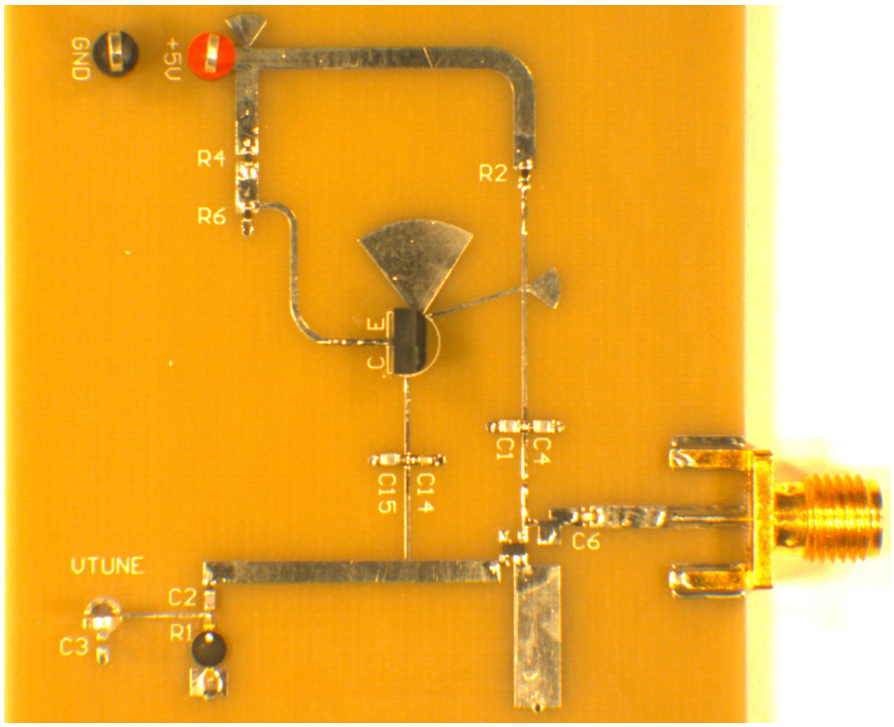

Figure 31: Active Biased VCO

Table 8: Bill of Materials of Resistive Biased VCO

Reference Designator	Comment	Part Number	Manufacturer
R4	6.65K Ohm Resistor	RK73H1ETTP6651F	KOA
R6	2K Ohm Resistor	RK73H1ETTP2001F	KOA
C2	1.5pF	C06CF1R5B-9ZN-X1B	Dielectric Laboratories
C14	0.01 µF Capacitor	500R14W103KV4T	Johanson
R2	63.4 Ohm Resistor	RK73H1ETTP63R4F	KOA
C4, C5	15 pF Capacitor	C06CF150J-9ZN-X1B	Dielectric Laboratories
C15	8.2 pF Capacitor	C04UL8R2C-6SN-X0B	Dielectric Laboratories
C6	2.4 pF Capacitor	C04UL2R4C-6SN-X0B	Dielectric Laboratories
C21	Varactor Diode	MP6304	M-Pulse Microwave
S2	RF SiGe NPN Transistor	BFP640	Infineon
	SMA Connector	142-0701-881	Emerson
	100 uF Capacitor	TAJD107K016R	AVX

Table 9: Bill of Materials of Active Biased VCO

Reference Designator	Comment	Part Number	Manufacturer
R4	2.94K Resistor	RK73H1ETTP2941F	KOA
R6	2K Ohm Resistor	RK73H1ETTP2001F	KOA
C15	3.9 pF Capacitor	C06CF3R9B-9ZN-X1B	Dielectric Laboratories
C2	1.5pF	C06CF1R5B-9ZN-X1B	Dielectric Laboratories
C14	0.01 µF Capacitor	500R14W103KV4T	Johanson
R1	63.4 Ohm Resistor	RK73H1ETTP63R4F	KOA
C4, C5	10 pF Capacitor	C04UL100JC-6SN-X0B	Dielectric Laboratories
C6	2.4 pF Capacitor	C04UL2R4C-6SN-X0B	Dielectric Laboratories
C21	Varactor Diode	MP6304	M-Pulse Microwave
S2	RF SiGe NPN Transistor	BFP640	Infineon
S4	PNP Transistor	ZTX705	Diodes Inc.
	SMA Connector	142-0701-881	Emerson
	100 uF Capacitor	TAJD107K016R	AVX

Test Setups

When the VCO was initially tested, a modification needed to be made in order to maintain a constant frequency. The tune input is extremely sensitive to variation and has high impedance which allows noise to influence the performance. In order to mitigate this issue, a shunt 100 µF capacitor with a series 100 KΩ resistor was added to the tune input. By adding a series resistor and a shunt capacitor, a low pass filter was designed that exhibited a time constant of ten seconds. This allowed the frequency to stay much more stable so that measurements could be taken.

In order to evaluate the phase noise performance of the VCO circuits, the Agilent E5052B phase noise meter with the Agilent E5053A down-converter were utilized. This test equipment has been used to measure devices that have SSB phase noise of -130 dBc/Hz at 10 KHz offset at 5 GHz center frequency which is much lower than the expected performance of the two VCO circuits that

were tested [15]. The test setup used for measuring the active and resistive biased VCO circuits is shown in Figure 32. A 15 dB attenuator was used to avoid saturating the test equipment.

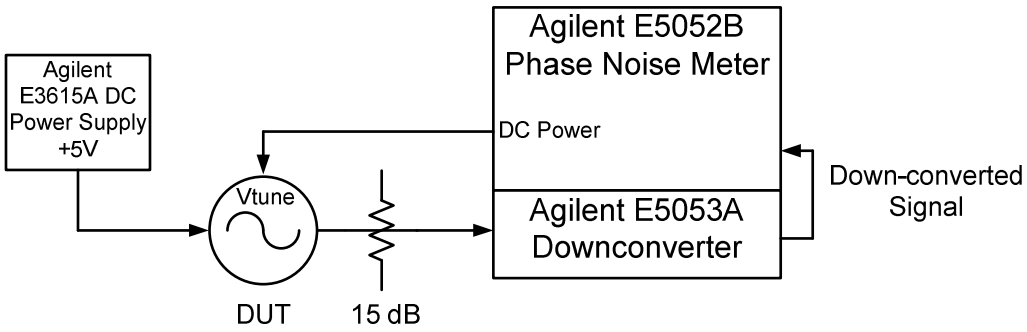

Figure 32: SSB Phase Noise Test Setup

In order to test the tuning range of each VCO, the Agilent E4407B spectrum analyzer was used. The spectrum analyzer display was set to max hold while the tuning voltage was swept from 1 V to 15 V. The test setup for this measurement is shown in Figure 33.

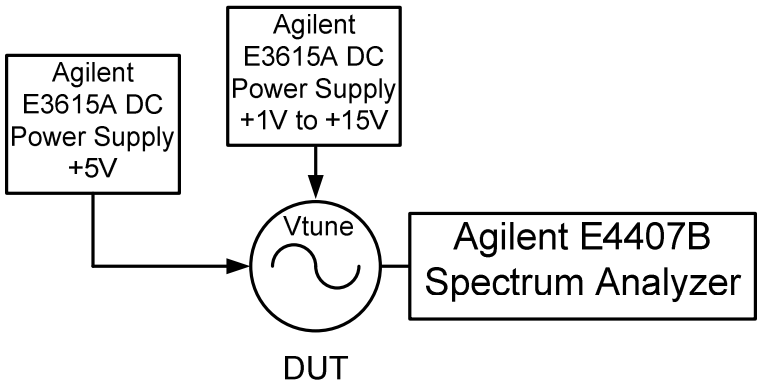

Figure 33: Tuning Range Test Setup

Test Results

Using the test setup shown in Figure 32 to measure SSB phase noise, a few measurements were taken at various tune voltages to see how the performance changed over frequency. Figures 34, 35, and 36 show the SSB phase noise results with 1 V, 3 V, and 5V input tuning voltages. The measured phase noise is very closely related to the phase noise predicted in simulation. There is a 5 dB difference in the simulation value which is most likely due to the fact that a model for the varactor diode was not available. In the simulation, a resistor was used to model the quality factor of the device and was arbitrarily selected. The phase noise improvement shown in the test data is at offset frequencies less than 50 KHz. A 15 dB SSB phase noise improvement was measured at those offset frequencies. Spurious signals appear on the active biased VCO at close-in offset fequencies caused by the power supply. These spurious signals are not seen on the resistive biased VCO because the overall phase noise is above the spurious levels. For this reason, the integrated noise of the active bias VCO is lower than the resistive biased VCO and represents an overall system improvement.

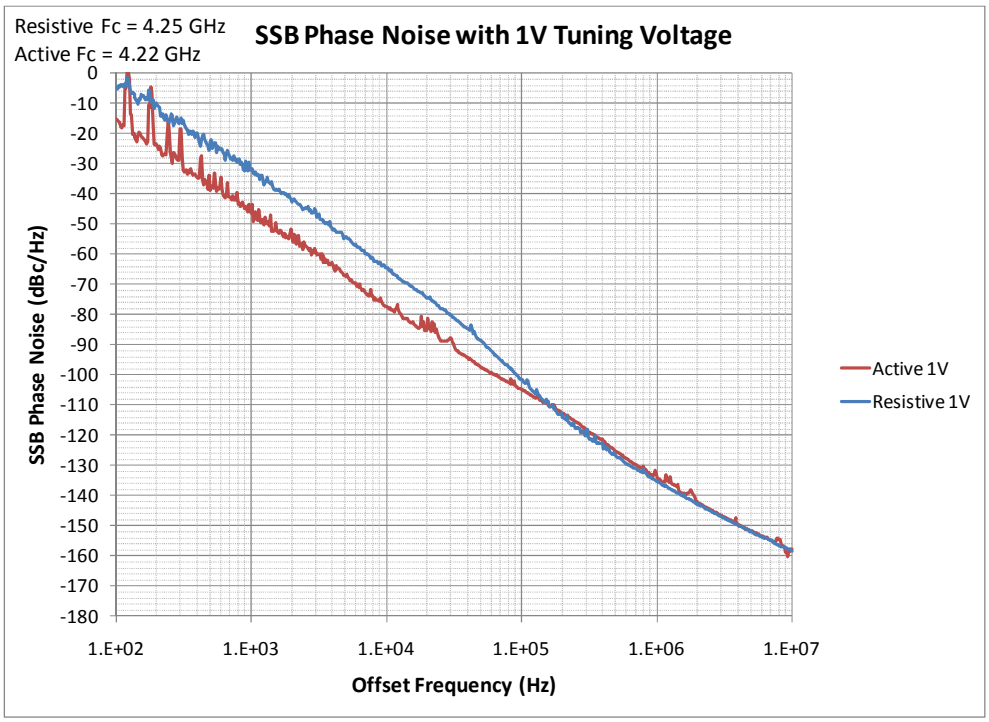

Figure 34: SSB Phase Noise with 1 V Tuning Voltage

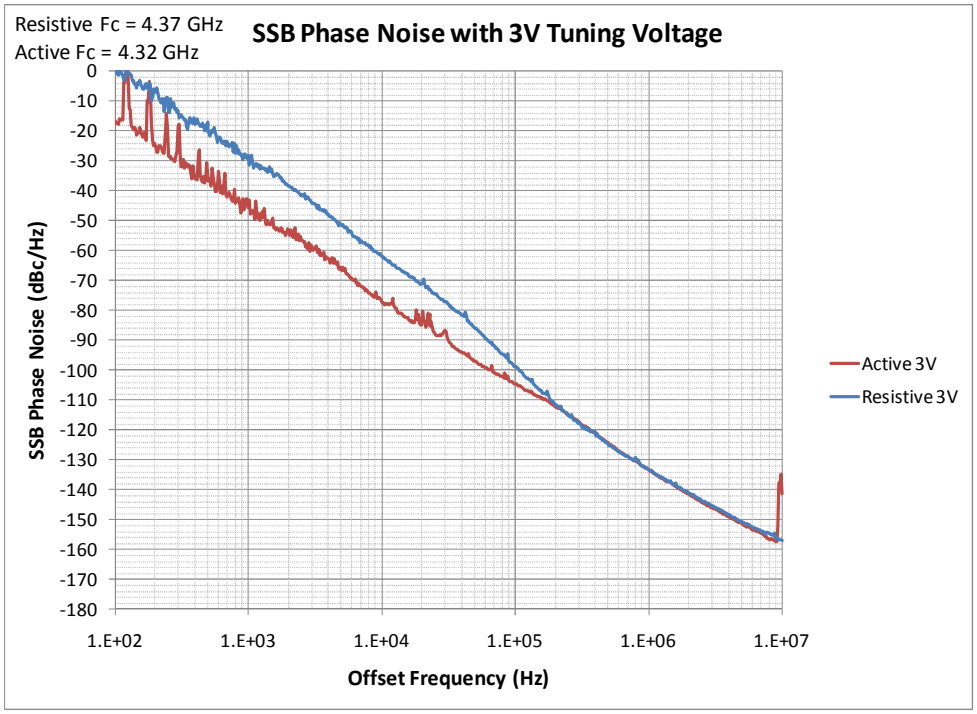

Figure 35: SSB Phase Noise with 3 V Tuning Voltage

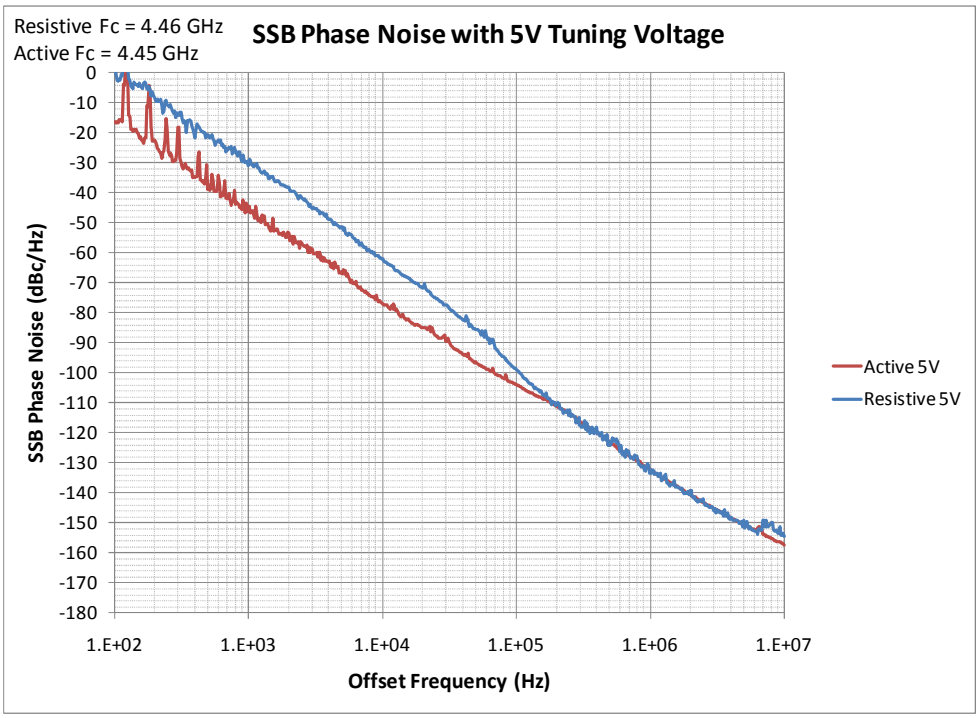

Figure 36: SSB Phase Noise with 5 V Tuning Voltage

The next test was done using the test setup previously shown in Figure 33 to measure the tuning range. Figures 37 and 38 show the tuning range as well as the amount of amplitude variation over that entire frequency range of the resistive and active biased VCO circuits. A tuning range of 4.27 GHz to 4.73 GHz was achieved with a 2 dB variation in output power over this band. That tuning range computes to 10.2% which was the design goal for these circuits. The actual frequency that was achieved was lower than the desired 5.5 GHz center frequency but it was still in the 4 - 7 GHz desired range. This difference is most likely due to variation in dielectric constant, thickness of the dielectric material, and additional line lengths in the resonator due to variants such as surface mount pads for the transistors and alignment of transmission lines in the actual layout. Regardless of

these differences, the overall goal was met in terms of tuning range, output power, and phase noise reduction at close-in offset frequencies.

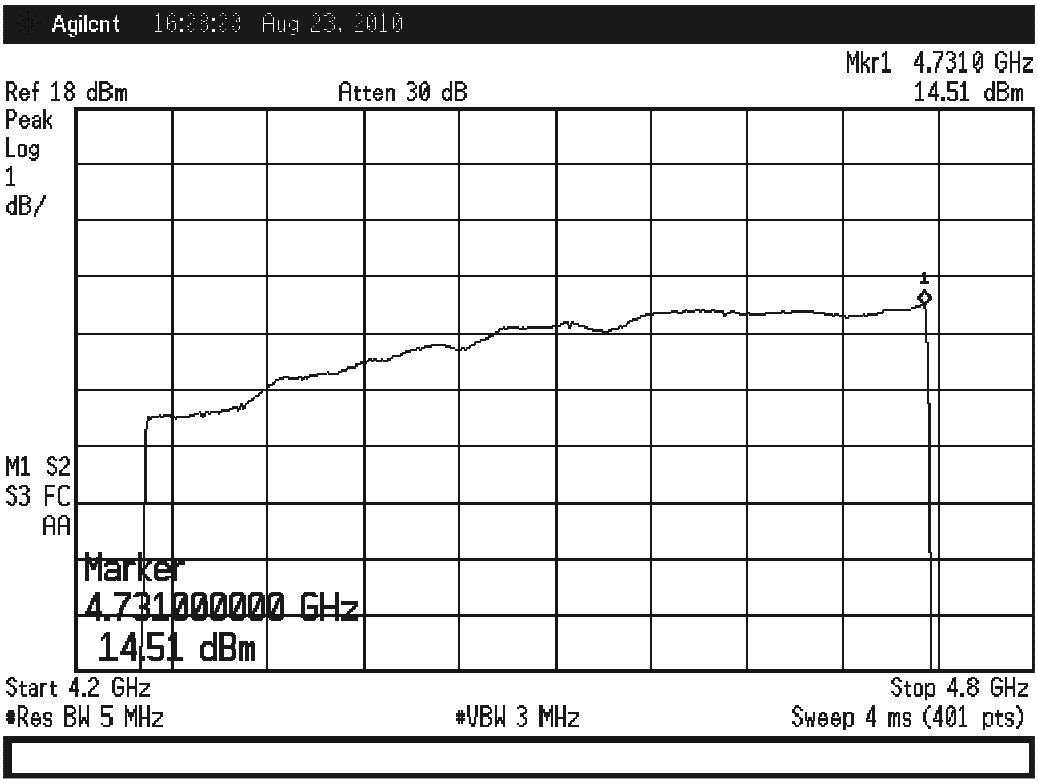

Figure 37: Tuning Range of Resistive Biased VCO

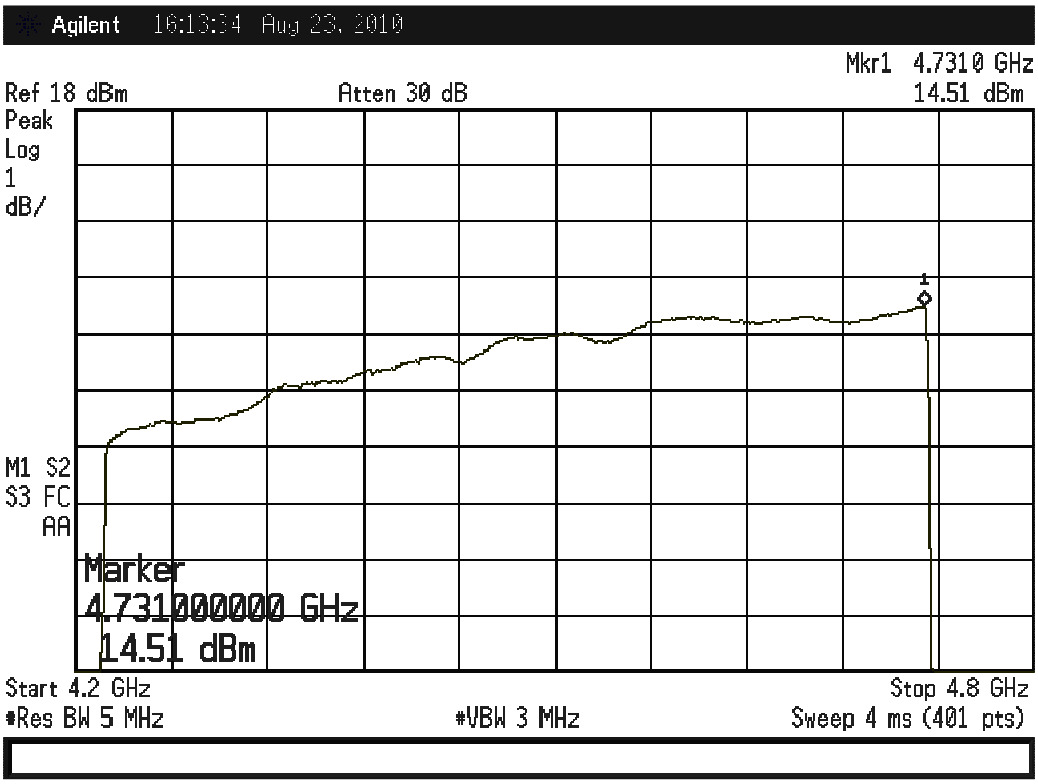

Figure 38: Tuning Range of Active Biased VCO

Chapter 5

Conclusion

Active biasing was proven to improve close-in phase noise performance in transistor based amplifier and VCO circuits. The VCO SSB phase noise demonstrated an improvement of 15 dB at offset frequencies less than 50 KHz. Residual phase noise of an actively biased amplifier also exhibited significant noise improvements when compared to an equivalent resistive biased amplifier. Future research could include applying active biasing to various RF integrated-circuits such as phase detectors, modulators, and phase shifters. Research could also focus on higher frequency amplifier and VCO circuits as well as high speed analog and digital logic circuits. While the research performed in this effort focused on silicon devices, future research could also focus on other technologies such as gallium arsenide (GaAs) and indium phosphide (InP)

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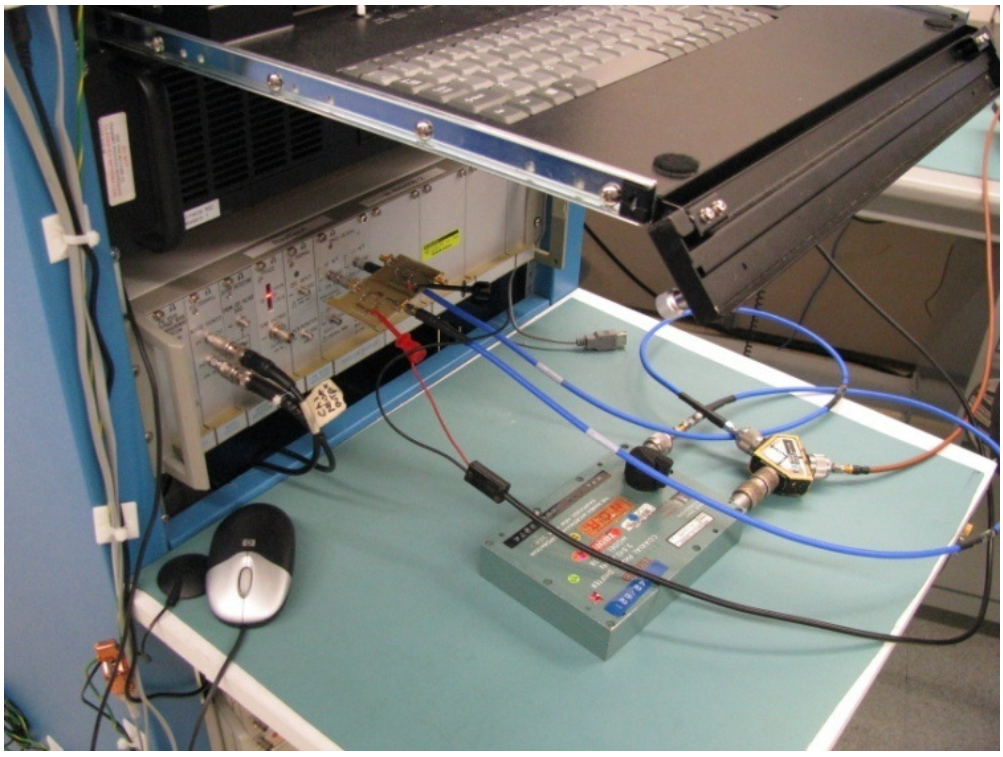
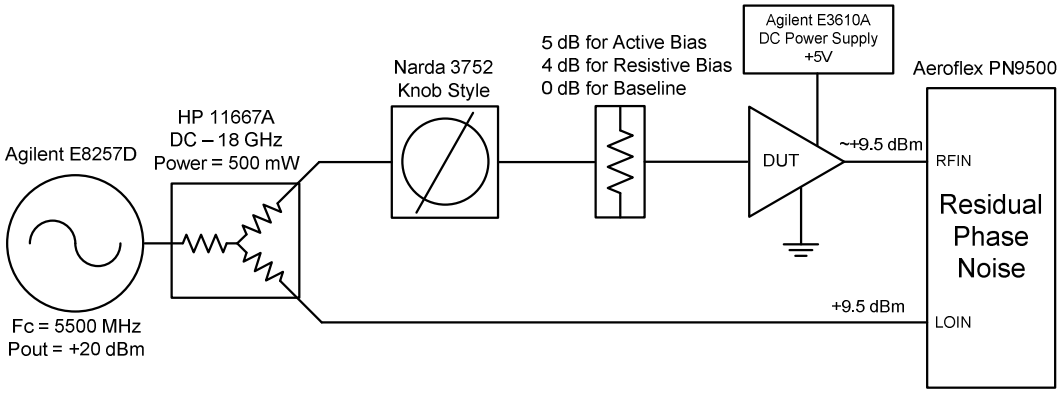
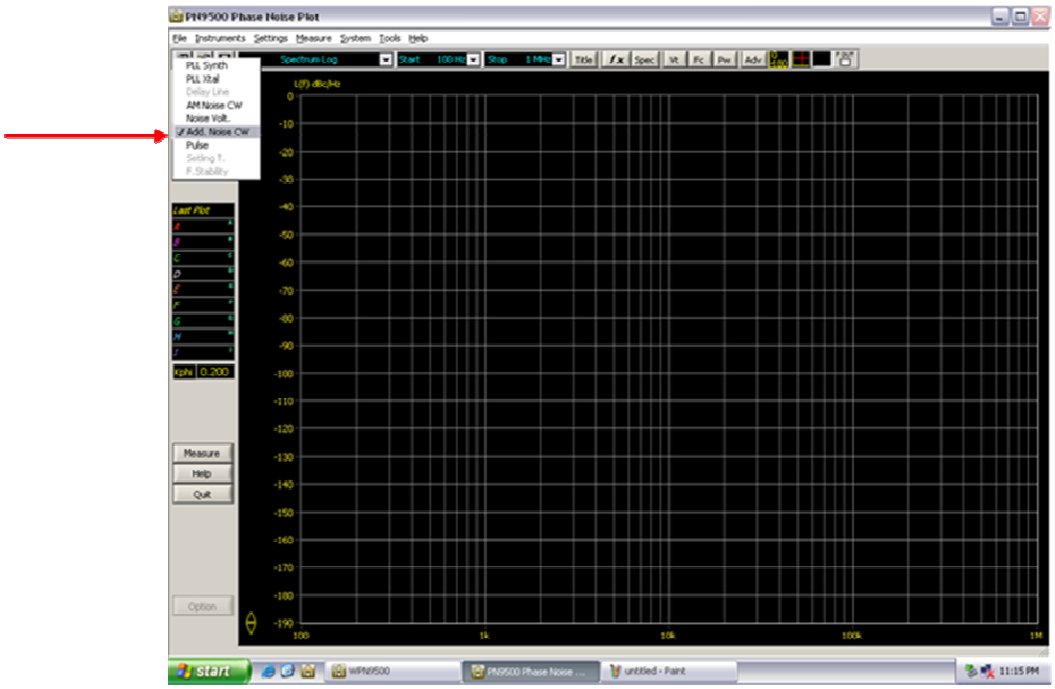
APPENDIX A

AEROFLEX PN9500 TEST STATION

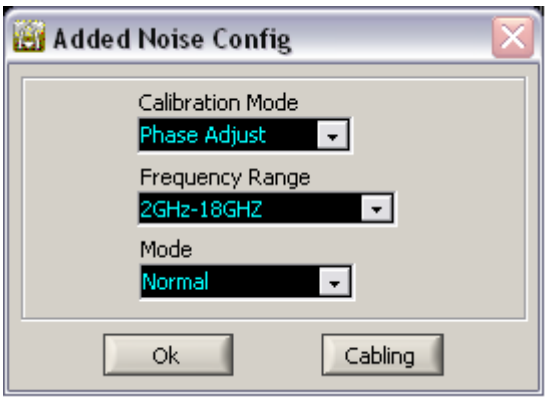




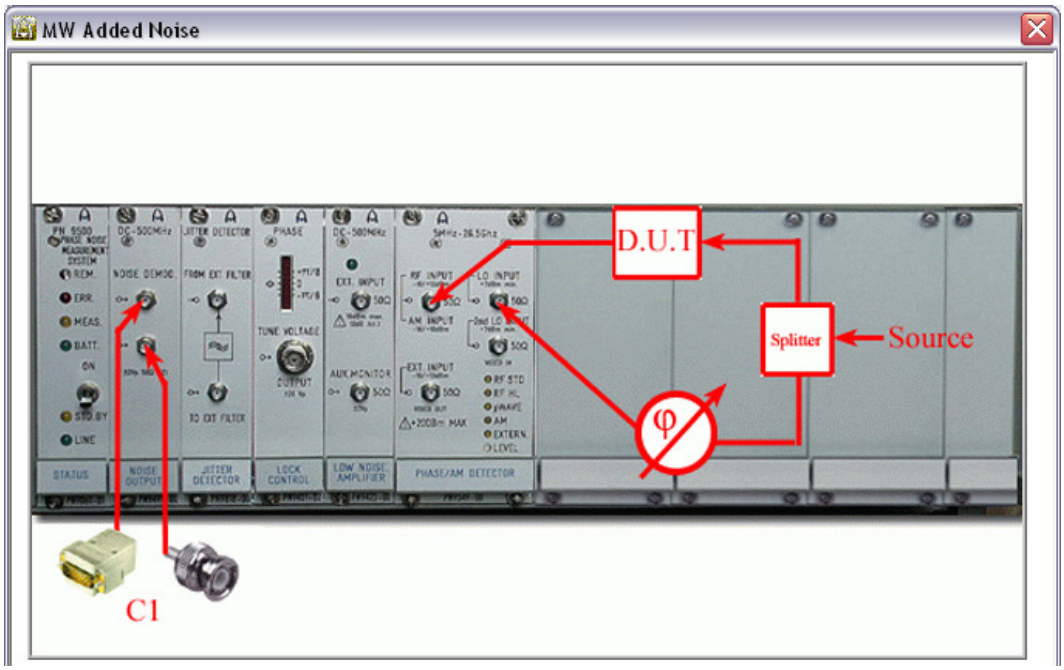
Step 1: Select Add. Noise CW.



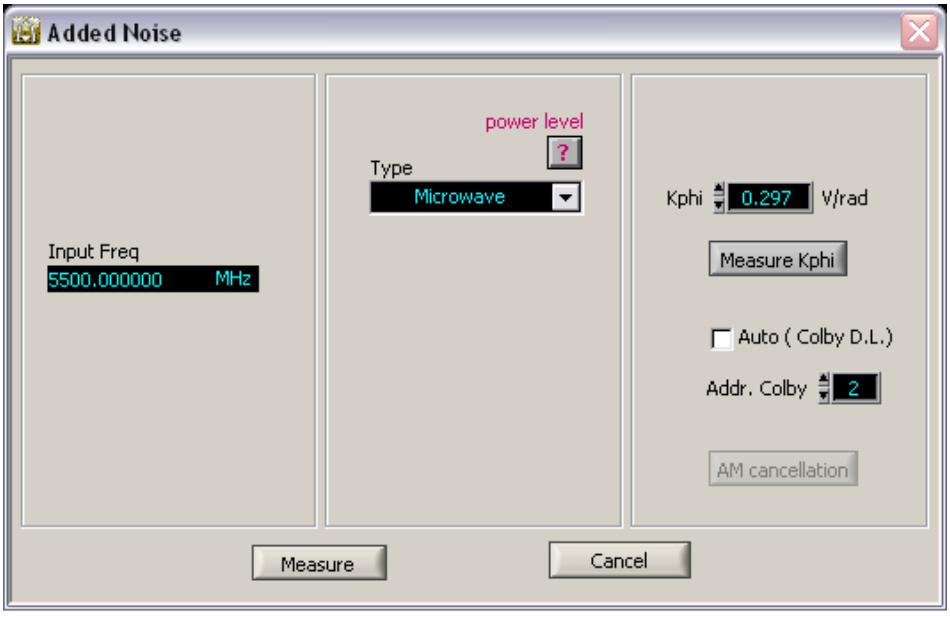
Step 2: Click config and set the parameters.



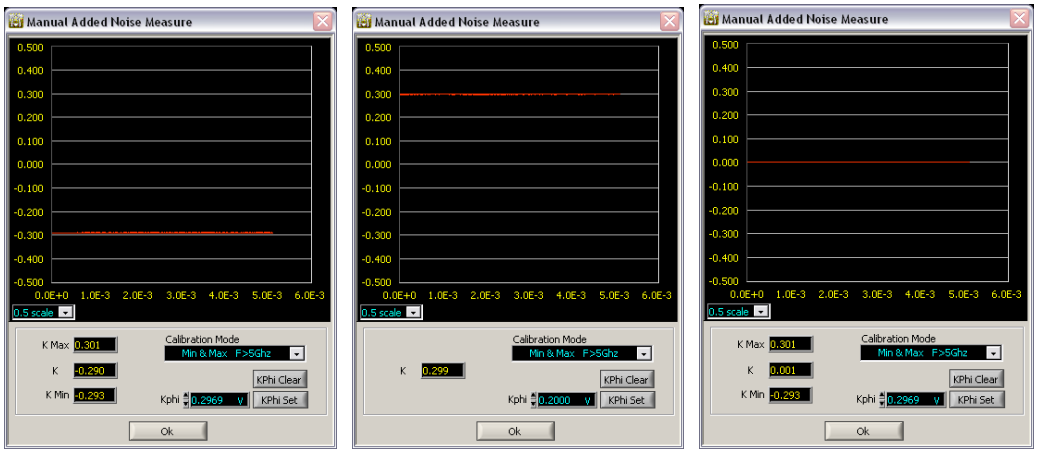
If cabling is clicked, the following screen will appear:



Step 3: Click measure and set the operating frequency and type then click measure Kphi (deselect Auto first).

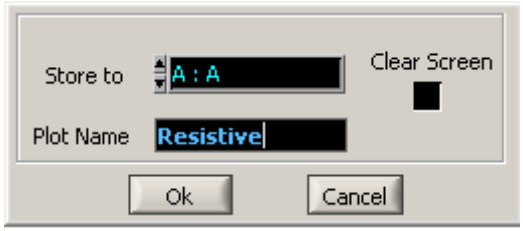


Step 4: Measure Kphi by finding the max, min, and zero points by changing the phase with the phase shifter.



Min Max Zero

Step 5: Select the channel to store the data and give it a name. The measurement will then begin.



BIOGRAPHICAL SKETCH

Jeremy Baldwin was born in 1982 in Chandler, Arizona. He received his Bachelors of Science in Engineering, Electrical Engineering degree from Arizona State University in 2006. He received his Masters of Science, Electrical Engineering degree from Arizona State University in 2010. Professionally, Jeremy worked for Orbital Sciences in 2004 and performed design and analysis of avionics control hardware. In 2006, Jeremy joined Raytheon Missile Systems and presently works in the RF electronics department. His most recent work has included design, modeling, and testing of radar and wireless communication hardware. He is listed as co-inventor for a patent entitled, "Resonator Ground Structures for Planar and Folded Distributed Electromagnetic Wave Filters." He currently resides in Sahuarita, AZ. 56