NVM Challenges in Medical Devices

by

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ABSTRACT

Electronic devices are gaining an increasing market share in the medical field. Medical devices are becoming more sophisticated, and encompassing more applications. Unlike consumer electronics, medical devices have far more limitations when it comes to area, power and most importantly reliability. The medical devices industry has recently seen the advantages of using Flash memory instead of Read Only Memory (ROM) for firmware storage, and in some cases to replace Electrically Programmable Read Only Memories (EEPROMs) in medical devices for frequent data storage. There are direct advantages to using Flash memory instead of Read Only Memory, most importantly the fact that firmware can be rewritten along the development cycle and in the field. However, Flash technology requires high voltage circuitry that makes it harder to integrate into low power devices. There have been a lot of advances in Non-Volatile Memory (NVM) technologies, and many Flash rivals are starting to gain attention. The purpose of this thesis is to evaluate these new technologies against Flash to determine the feasibility as well as the advantages of each technology. The focus is on embedded memory in a medical device micro-controller and application specific integrated circuits (ASIC). A behavioral model of a Programmable Metallization Cell (PMC) was used to simulate the behavior and determine the advantages of using PMC technology versus flash. When compared to flash test data, PMC based

embedded memory showed a reduction in power consumption by many orders of magnitude. Analysis showed that an approximated 20% device longevity increase can be achieved by using embedded PMC technology.

DEDICATION

“To my mother Madiha and father Ezzat who taught me everything I know, and who taught me that everything is achievable through dedication and hard work. To my grand mother Fathya who raised me with my parents. To my beautiful wife Maie who put up with me working more than full time while working on my Master’s, whose support was my main enabler through my course work. To my two beautiful children Yaseen and Malak who are my main motivation to succeed in life. To my brother Ahmed and my in-laws Mohamed and Malak, who supported me in many ways.”

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I am also indebted to my manager Carlos Acosta who was very understanding and supportive of me combining work and school. And to all my colleagues at Medtronic® Inc. who mentored me during my tenure in the company,

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Chapter 1

1 Introduction

The need for high density, low power and low cost memory has been growing at an incredible rate in the last three decades. In fact, it is the need for smaller, lower power memory that has been one the main drivers of pushing manufacturers to further reduce lithography and meet Moore's law when many believed it has reached its physical limitations. When Flash memory was invented in the 1980's**,** it was seen as a huge advance in NVM technology that would enable the area reduction of the memory cell to that of a single transistor. Flash has then quickly become the most volume produced memory today with vast investments in its production and a forecasted revenue of $55.2 billion in 2013 [19].

While Flash technology offers a good area advantage, especially when considering new advances in Flash technology such as multi-bit cell Flash, Flash memory is proving to be somewhat incompatible for use in ultra low power applications. The charge trapping mechanism (the core foundation of the flash memory technology) requires excessive voltage and current through each cell. A high end Flash cell in 65nm technology requires more than 6V and 100uA for program and erase operations [7]. Given the fact that a CMOS transistor in the same technology requires less than 1V, the operational voltage level and integration disadvantages are obvious. This is even more of a concern in ultra low power systems

that operate in the sub-threshold area such as in case of most medical devices.

Added to the power disadvantage of using Flash memory, such a high voltage is generated using high power circuitry such as charge pumps. These circuits require relatively large silicon areas and capacitances and have both area and reliability concerns. Moreover, the high current drained by a Flash mass erase and program operations lie among the most power consuming events in a medical device system and therefore additional battery monitoring and filter circuitries may be required. Moreover, while the Flash read operation is relatively fast 10-100 ns, Flash write access time is between 1 to 10 us. For very power conscious systems such as those of medical devices, the high voltage circuitry is allowed to ramp up just before the program operation which in turn adds to the Flash write and erase times [7].

Like many other ultra low power systems, the medical device industry has been struggling to customize Flash technology to meet its power specifications. Added to the complexity of that task is the fact that most of the medical devices operate in the sub-threshold domain which means that a dedicated high voltage circuitry is required for flash. While Flash technology has successfully invaded the medical devices arena and became the embedded memory of choice for firmware code storage and low frequency diagnostic data storage, as well as in some cases replacing

conventional high area EEPROM technologies, it is obvious that as the feature set of medical devices expands, as well as the growing need for faster and smaller devices with ultra low power consumption to accommodate a smaller battery without sacrificing longevity, a new type of NVM technology is inevitably needed. While many promising NVM technologies are being developed, among the most promising technologies is the PMC or CBRAM technology. PMC seems to be very fit for use in medical devices that operate in the sub-threshold arena. Added to the advantages of using PMC is the fact that requires a much simpler process that is very compatible with the logic process and requires only two additional steps. On the other hand, it is much more complicated to embed Flash memory in a logic process.

This document starts by stating the low power memory challenges faced by the medical device industry and other low power device makers. This is followed by a top level overview of the most popular new NVM technologies in chapter 2 with a brief description of their respective theory of operation, applications, as well as the advantages and disadvantages of each technology. Chapter 3 covers an in depth analysis of programmable metallization cell (PMC) also know as conductive bridge random access memory (CBRAM) technology and its modeling in both SPICE and CAD tools for evaluation purposes.

Chapter 4 provides a brief introduction to pacemakers and their function and applications. This is followed by an analysis of the PMC array model in chapter 5 developed using the PMC cell model in chapter 3.

Chapter 6 includes a summary of the results from the analysis the important characteristics of the PMC against Flash using the Verilog-A model described in chapter 3 and the conclusion

1.1 Definitions, Acronyms, and Abbreviations:

ROM	-Read only Memory
RAM	-Random Access Memory
SRAM	-Static Random Access Memory
DRAM	-Dynamic Random Access Memory
FeRAM	-Ferromagnetic Random Access Memory
MRAM	-Magneto-resistive Random Access Memory
PMC	-Programmable Metallization Cells also known as CBRAM
CBRAM	-Conductive Bridge Random Access Memory
PRAM	-Phase Change Random Access Memory
MLC	-Multi Level Cell
SLC	-Single Level Cell
PRAM	-Phase Change Random Access Memory
CAD	- Computer Aided Design

EEPROM -Electrically Erasable Programmable Random Access Memory

Chapter 2

2 Memory Overview

The main objective of this study is to explore new memory technologies and how they may or may not be a practical choice for use in medical devices. The review of literature for the most popular new NVM technology was conducted to pick to most appropriate technology to model and simulate. The following is a detailed description for each new technology highlighting the most important parameters like power consumption, speed, reliability and scalability. At the end of each section a brief evaluation is conducted to assess the NVM technology for use in medical devices.

2.1 FLASH

Flash memory is a type of EEPROM, since the floating gate and NAND flash invented by Toshiba in 1980 it has quickly become the most volume produced type of memory today. NAND flash compact architecture made it very suitable for portable date storage. It has quickly become the first choice for application requiring significant data storage. Intel® followed Toshiba® by inventing the NOR flash architecture which allowed random access allowing NOR flash to become a potential replacement of DRAM and SRAM for data and application execution. Even though flash has many draw backs, like high voltage circuitry for programming and

erasing as well as write and read access times, its durability, scalability and size made it a very popular choice for application like external as well as internal data storage. Since Flash is non-volatile, erasable, and does not require volume manufacturing, it can be used to replace ROM for firmware storage in devices. Even though flash is not as fast as SRAM and DRAM, it can be used in parallel with a smaller size cache memory to execute code in very high speed applications.

Structure and theory of Operation:

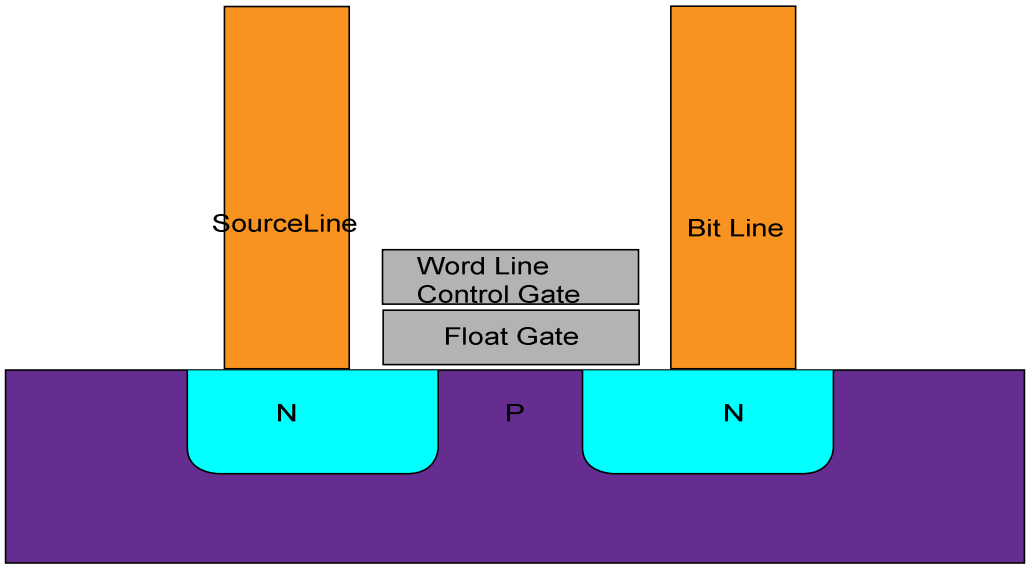


Figure 1. Flash cell structure showing a single transistor structure. This figure shows the CMOS transistor with a floating gate flash cell structure [16]

The NOR flash gate is analogous to a standard MOSFET Cell with an added gate between the gate poly and the substrate. The added gate

(floating gate) is surrounded by dielectric to isolate it from both the gate poly and the substrate. The structure of the flash cell makes it very scalable. This is especially true in case of NAND Flash architecture were interconnects are reduced to a minimum. It also makes the flash process very compatible with logic processes. The floating gate is capable of trapping charge inside permanently unless externally drained which gives the flash its non-volatile property. Depending on whether the floating gate holds a charge or not, a logic 0 or 1 can be read. If the FG contains a charge, the threshold of the MOSFET is increased (the charged FG forms an opposing electric field) and the gate voltage needed to form a conductive channel is higher than that of a cell with uncharged FG. When applying a small enough voltage on the gate a channel is formed only if the FG does not hold charge. If the FG contains trapped electrons, the path between the source and the drain remains resistive. To read the flash cell, a current is passed between the source and the drain and then sensed to determine whether the S-D path is resistive or conductive. In general, if the FG does not hold a charge the S-D path is conductive and a current is sensed, this generally represents logic 1. If the gate contains a charge, no channel is formed, and hence no current is sensed representing a logic 0.

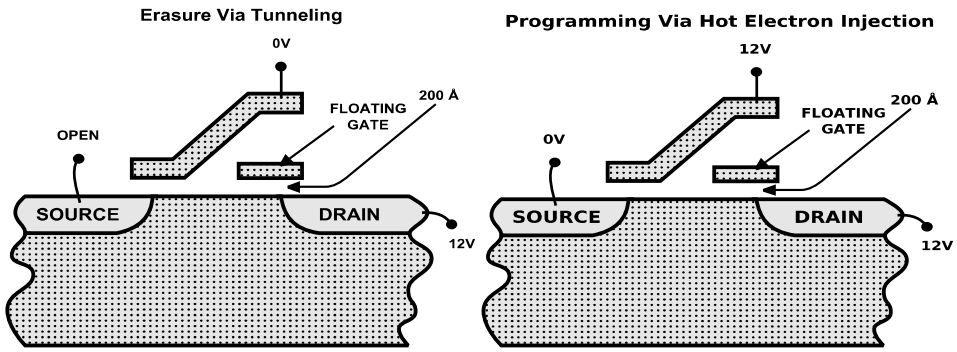
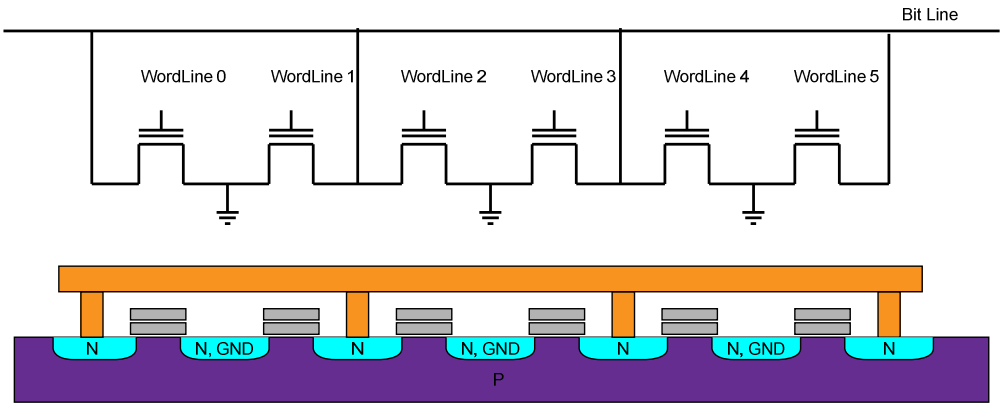


Figure 2. NOR Flash erase and program. Left diagram shows the erase process through tunneling. Right diagram shows voltages on drain and gate to trap charge via Hot Electron Injection [16]

NOR flash is erased (reset to logic 1) by applying a relatively high voltage of opposite polarity between the gate and the drain as shown in Figure 2. This forces the electrons in the floating gate to drain through tunneling. NOR flash can be reprogrammed using the hot electron phenomena by applying a high voltage on both the gate and drain. NAND flash is erased by tunnel release and is programmed through tunnel injection.



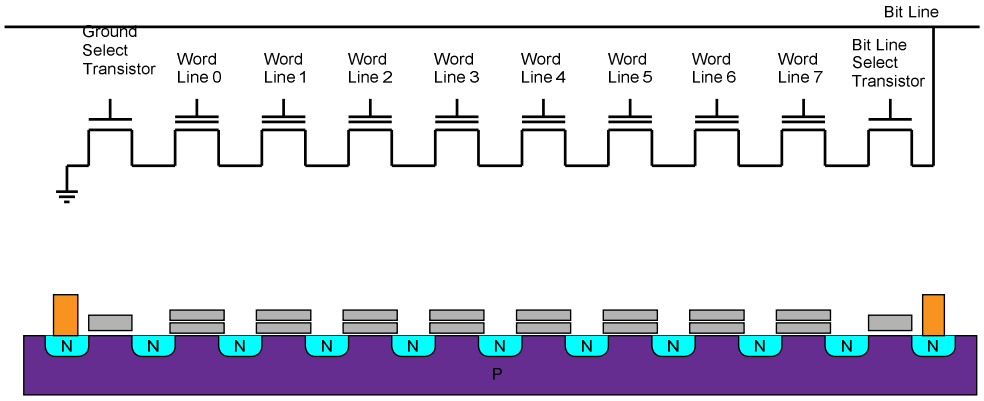


Figure 3. Flash architecture. Layout For an 8-bit NOR flash (TOP), layout For an 8-bit NAND flash (bottom) [16]

Flash technology has been configured in many different ways, the most famous architectures are the NAND and NOR flash. NOR flash cells are connected in parallel to the bit line allowing cells to be read and programmed separately. This architecture resembles the connections of a transistors in a CMOS NOR gate and hence their name. When NOR flash was initially introduced by Intel®, it was intended to compete with ROM thus was configured to allow random access write and read to individual cells. The major drawbacks of this architecture were related to both area and speed. Individual write access to flash cells require relatively complex decode circuitry as well as much more interconnections between cells. NOR flash architecture is very fit to replace ROM where not many writes occur.

NAND flash architecture was introduced to reduce area by getting rid of much of the interconnections between flash cells. In NAND flash, cells are connected in series preventing them from being read and programmed individually. Instead, cells have to be read and programmed in series. Write circuitry is a lot faster and simpler than that of a NOR flash. Reduced density also results in higher capacity and hence lower cost. Because of the series connection and removal of word line contacts, NAND flash memory is ideal for use in removable memory. NAND flash is used for data storage as a replacement to hard desk as well as external memory and memory cards. A major draw back to NAND flash is the weakness of its read signal, this result in a more complex sensing circuitry and read accuracy concerns. NAND flash is usually accompanied by an Error Correction Circuitry (ECC) to improve accuracy.

Advantages:

Flash technology enjoys huge wide spread, it is by far the most heavily produced memory today. Flash is easily scalable as its structure is in essence that of a single transistor. Flash memory is also very durable, which gives it an advantage in mobile memory applications. Not only is Flash one of the densest memories (only considering the array and not the control circuitry), several advancements in the FLASH technology have showed a lot of success. A good example of the advances in flash is the

2-bit and 3-bit per cell storage flash essentially doubling or tripling the flash capacity by having multiple floating gates instead of 1.

Disadvantages:

The main disadvantage of Flash memory is the fact that high voltage in needed to force charge in and out of the floating gate. In order to achieve this high voltage power hungry charge pumps are designed in the chip to create high enough voltage. Charge pumps need time to charge and hence write access times for the flash are in terms of milliseconds. This is orders of magnitude slower than other memories like DRAM (Dynamic Random Access Memory), FeRAM (Ferromagnetic Random Access Memory), MRAM (Magneto-resistive Random Access Memory) or PMC (Programmable Metallization Cells also known as CBRAM). Also since flash requires high voltage circuitry the area cost of the first bit makes it very impractical for use as a small memory.

Medical Devices Considerations:

NAND flash is currently being used in medical devices replacing ROM. It is used to store firmware code as well as record diagnostic data collected by the device. Its high density and robust performance made it a good fit for use in medical devices. The main advantage of flash is during product development where firmware can be updated to add feature or eliminate

bugs without the need for a new fracture like in the case of ROM. However, embedding flash in a logic chip is an expensive process. Moreover, flash has a very high first bit power cost. Since the memory used in medical devices is usually small (approx. 256Kbyte) using flash result in more power consumption than ROM.

2.2 ROM

Mask ROM is one of the oldest types of memory still used today. Mask ROM is fabricated with the desired data permanently stored on it. Combinational logic is used for address selection. Each address contains predefined data that will appear on the output bus when that address is selected. ROM is nonvolatile, however, it is also non reprogrammable. This makes it unusable for applications that require rewriting data such as data collection and hard drives. ROM is used today primarily to store boot up code and in some cases to store firmware code that is unlikely to change.

Advantages:

Since ROM is one time programmable, it does not require any programming circuitry. Programming circuits are normally power consuming, this makes ROM more power efficient than many types of memory like flash. Another advantage of ROM is that it is almost directly scalable to any technology. It mainly consists of combinational logic that

point to hard coded data. ROM also consumes less area than single bit FLASH since it does not require any high voltage analog circuitry.

Disadvantages:

ROM reads are generally slow. In a personal computer, SRAM is often used as an intermediate storage (Cache) to fetch code currently in use by the Central Processing Unit (CPU). ROM data is fabricated in silicon; it requires special radicals that will be used to hardcode the data. This makes ROM very specific to a certain application. ROM is only cost efficient when used in large scale manufacturing. Depending on the number of chips being fabricated, ROM can be the cheapest alternative.

Medical Devices Considerations:

ROM is generally used to store Firmware in a final product after R&D is completed. ROM can be much cost efficient if sufficient volume is produced. However, the fact that ROM is not programmable makes it a very expensive choice for use in research and development where firmware code needs much iteration to finalize. It also makes ROM not suitable to use to store diagnostic needed and hence another form of memory (EEPROM or Flash) is still needed alongside ROM.

2.3 FERAM

Ferroelectric random access memory is one of the emerging non volatile memories that compete with flash and other NVMs. The FeRAM structure is resembles that of a DRAM 1T1C structure (as shown in figure

4) but instead of storing charge in a capacitor, FeRAM stores data in a ferroelectric layer. Data stored in the ferroelectric layer is permanent and is not erased when power is off.

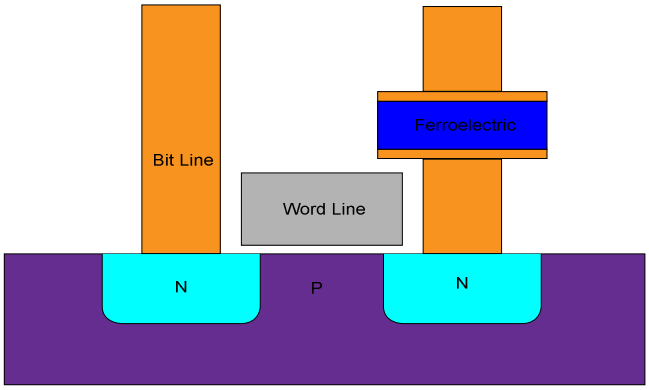


Figure 4: FERAM cell structure: the FeRAM cell structure resembles that of a 1T1C DRAM with a ferroelectric layer instead of a capacitor [16]

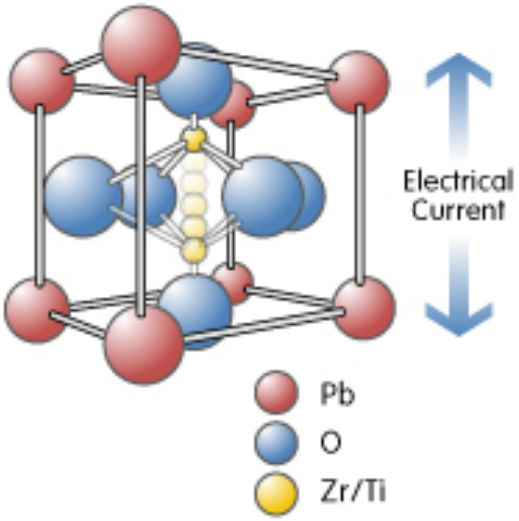


Figure 5. PZT crystal structure showing the Ferroelectric layer atom movements changing its resistance [12]

Theory of Operation:

The operation of the FeRAM is very similar to that of the DRAM. In a DRAM**,** cell writing is performed by either draining the dielectric of any charge (normally that means a logic “0”) or charging the capacitor temporarily (normally a logic “1”). The main advantage is that, unlike the capacitor that only holds the charge temporarily, the ferroelectric layer does not require constant refresh writes.

In a FeRAM cell, the dielectric is replaced by a thin ferroelectric film of lead zirconate titanate [$Pb(Zr,Ti)O_3$], commonly referred to as PZT shown in Figure 5. The Zr/Ti atoms in the PZT change polarity in an electric field to one of two possible polarities depending on the direction of the electric field. By charging the plates, the dipoles tent to align themselves with the field direction, and become permanently polarized. As shown in figure 4. Polarization is accomplished due to small shifts in the atom position within the crystal structure towards the electric field and hence redistributing the electric charge in the crystal. Once the ferroelectric layer is polarized it retains its state unless an electric field is applied. The ferroelectric have two possible polarization state “-Pr” and “+Pr”. To program the FeRAM cell, the plates are charged to produce an

electric in the two possible directions causing a ferroelectric layer to be polarized in the +Pr or –Pr direction.

The FeRAM memory technology relies on a characteristic of the ferromagnetic layer. When the Ferroelectric layer changes polarity, a brief pulse is created on the output as a result of the reorientation of atoms that attract the electrons towards the metal. This characteristic is utilized to read the memory cell. In reading the FeRAM cell, the cell is programmed to a specific polarization (say +Pr), if no pulse is sensed, then the cell held a previous polarization of (+Pr) and this is interpreted into a 1 or 0. If a pulse is sensed, then the cell held the opposite polarization (-Pr) and data is interpreted accordingly. One obvious disadvantage of the FeRAM is that this reading technique erases the previous content of the cell (destructive read) and hence the cell will need to be reprogrammed after each read operation.

Density:

There are two limitations that prevent FeRAM from becoming fully scalable. The first is the fact that a minimum amount of charge needs to be created during read in order to trigger the sense amplifier with reasonable accuracy. Another factor is that the ferroelectric material loses their ferromagnetic property when they become very small. Presently, FeRAM is manufactured down to 130nm.

Power Consumption:

FeRAM does not need any refresh writes since the ferroelectric material hold its polarization permanently. This gives the FeRAM an advantage over dielectric memories like DRAM. Even though significant charge is required to charge the plates and polarize the ferroelectric layer, unlike Flash memory, FeRAM does not require any high voltage circuitry. FeRAM consumes only 27μJ to write 4K bytes to an F-RAM [12]. Currently**,** FeRAM has matured to be in production for 512K X 16 and requires a voltage between 2.7V and 3.6V for program and erase operations.

Speed and Performance:

FeRAM operation is based on polarizing the ferroelectric material and displacing its atoms. This happens theoretically in the order of nanoseconds. In theory this operation is even faster than charging the capacitance in the DRAM to sufficient level to hold data. The fast access time makes FeRAM compete with the fastest memories available. Moreover, unlike the Flash, FeRAM does not require high voltage that is created through a charge pump that takes milliseconds to charge. A typical read or write access time is approximately 60ns [11].

Write Cycles:

Maximum write cycles for FeRAM exceed 10^{12} which is orders of magnitude faster than conventional Flash memories.

Medical Devices Considerations:

FeRAM is considered very suitable for use in medical devices for Flash memory replacement. As detailed in the leading sections it has both area, power and performance advantages over Flash memory. Unlike Flash, FeRAM does not require extremely high voltage (when compared to the logic process). However, the voltage required to program and erase FeRAM is still significantly higher that the logic operation voltage. Moreover, there has not been a lot of literature on how difficult it is to embed FeRAM in logic chips. Another consideration that further characterization is required to determine if FeRAM can change its state under high magnetic fields (MRI).

2.4 MRAM

Theory of Operation:

MRAM is unique in the fact that, unlike conventional memory where data is stored in the form of an electric charge or current flow, MRAM data is stored in magnetic storage elements. These elements consist of two ferromagnetic plates. Each plate is capable of holding a magnetic field. To store data, one of the plates is set to a particular polarity (acting as a permanent magnet); the other plate can be programmed with an external magnetic field to one of two possible polarities. To program the MRAM, the programmable plate field is set to a similar or opposite polarity as the permanent magnet. A thin insulating layer is placed between the two plates through which electron can tunnel through from on layer to the

other. This phenomenon is called the magnetic tunnel effect. If the magnetic fields on the two plates are parallel, electrons are more likely to tunnel through the barrier layer hence decreasing the cell resistance. If the magnetic fields on the two plates are opposite in polarity, electrons are less likely to tunnel through the barrier layer hence increasing the cell resistance. To read an MRAM cell, the electrical resistance is measured by passing a current from the cell to the ground. Generally, if the two plates have the same polarity, the resistance is lower and a logic “1” is read. If the polarities of the plates are opposite, the electrical resistance is higher and a logic “0” is read.

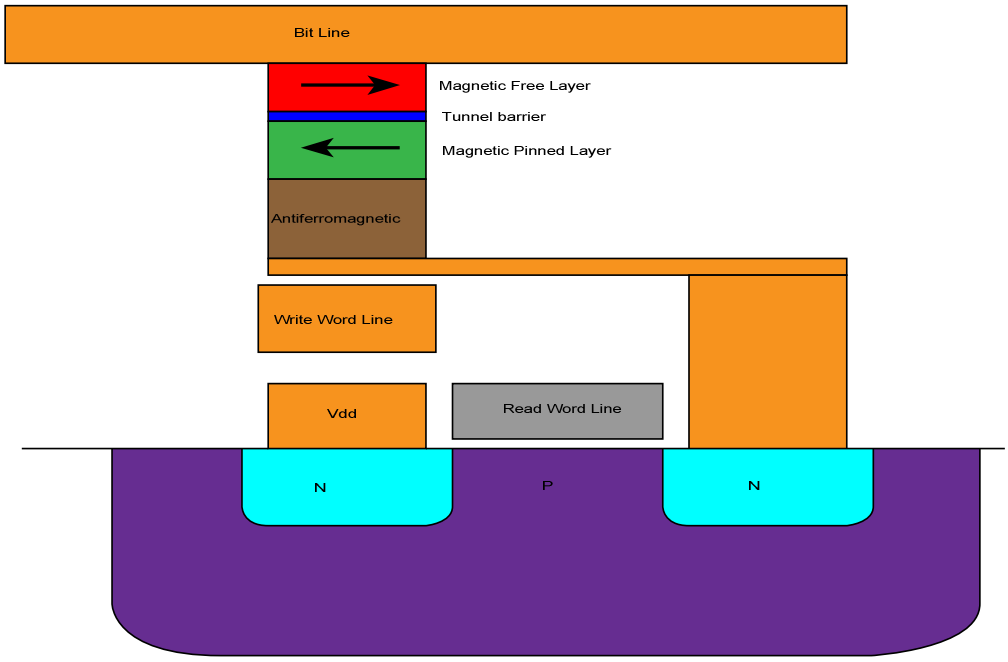


Figure 6: MRAM cell structure showing the programmable cell is placed between two write lines at right angles from each other. The anti-ferromagnet layer is used in “toggle mode” [16]

Several techniques to program the MRAM cell have been developed. Conventionally, the programmable cell is placed between two write lines at right angles from each other as shown in figure 6. When current is passed through the write lines a magnetic field is created. The programmable plate picks up that field and its polarity changes accordingly. Several disadvantages arise from using this technique, most importantly write integrity and power consumption. Significant current needs to be passed through the write lines to create a sufficient magnetic field. This makes the circuit relatively power hungry. Another disadvantage is that this technique limits the scalability and density of the MRAM cell. As technology shrinks and cells become close together (at about 180nm) it becomes more difficult to create a magnetic field that can target a specific cell without affecting neighboring cells. Cells close to the one being programmed can also be partially or fully programmed. This is called the half select phenomenon.

To overcome this problem, another approach has been developed to program the MRAM cell namely the “toggle mode”. The toggle mode uses a multi-step write with a modified multi-step cell. An artificial anti-ferromagnet is added to the cell whose magnetic orientation rotates back

and forth across the surface. This allows the programmable plate to have only two stable polarities. Write is performed by passing current to one plate and delaying the current on the other, therefore, rotating the field until the plate reaches the stable polarity. If the exact field intensity is not reached, the plate returns to its previous state and hence preventing the half select. A disadvantage to this approach is that it adds a lot of complexity to the cell as well as the control circuit. Also while the toggle method solves the half select issue, it does not address the large power consumption resulting from passing a significant amount of current for writes.

Among the most recent techniques still under refinement is the Spin Torque Transfer (STT). In this technique, spin aligned or polarized electrons are passed through the magnetic layer to directly torque the programmable ferromagnetic plates. When the polarized electrons pass through the un-programmed magnetic layer they change their spin. This re-polarization result in a continuous torque in the magnetic layer until it reverses its polarity. While this technique is very promising to solve the half select problem, it is only applicable to smaller technologies where lower current is needed for programming.

Density:

Even though MRAM has a very similar structure to that of one of the densest memories (the DRAM 1T1C structure), write integrity becomes an

issue at smaller technologies due to the half select problem when nearby cells get unintentionally partially programmed. Toggle mode writes provide some protection from the half select and allow MRAM to scale to smaller technologies (90 nm). As STT is refined scientists speculate that MRAM will be fully scalable.

Power Consumption:

While the MRAM cell requires relatively more current to write than other conventional memories like DRAM, it does retain data even when the power is off and hence does not require any refresh writes. It also does not require any high voltage circuitry for programming which gives it an advantage over FLASH that requires high voltage for high voltage writes. Even though conventional MRAM requires a lot more power for writes than reads, STT promises great power saving that will make the MRAM write power consumption close to the read power consumption.

Speed and Performance:

One of the main advantages of MRAM is that is surpasses pretty much all other memories except SRAM in write/erase time. MRAM operations are based on measuring voltages and not charges which result in less settling time. Researchers demonstrated access times as low as 1ns. When compared to flash, MRAM writes are hundreds if not

thousands of times faster that the flash programming time. Current sample chips offer a 35ns read/write time [13].

Even though SRAM has a slightly faster access time than SRAM is typically consists of a six transistor (6T) structure which makes it a much less dense and thus more expensive choice.

Medical Devices Considerations:

MRAM technology dependence on a magnetic field for program and erase operations makes it a poor choice for use in medical devices. In addition to the MRAM data integrity issues mentioned above, its sensitivity to intense magnetic fields makes raises concerns on medical device performance under an MRI. Also the high current use to generate the magnetic fields results in higher power consumption affecting device longevity.

2.5 PRAM

PRAM is one of several non-volatile memory technologies that have emerged as possible flash alternatives. Even though the technology has be around since the 60's, material quality and power consumption issues have just recently been improved enough to revive serious interest in this type of memory.

Theory of Operation:

PRAM makes use of the unique behavior of Chalcogenide glass which can be switched between two states (crystalline and amorphous) with the application of heat. The two states have very different electrical resistance. The amorphous state has a very high resistance and is conventionally used to represent a logic “0” while the crystalline state has a much lower resistance and is used to represent a logic “1”. The most popular chalcogenide used is an alloy of germanium, antimony and tellurium (GeSbTe). This alloy changes its state from a crystalline to amorphous state when high temperature is applied (> 600 C). To transition back to a crystalline state, the alloy is heated to above its crystallization point but bellow its melting point .Recently, literature has been published that proves that two other intermediate states between amorphous and crystalline can be detected. This allows double bit storage in a PRAM cell.

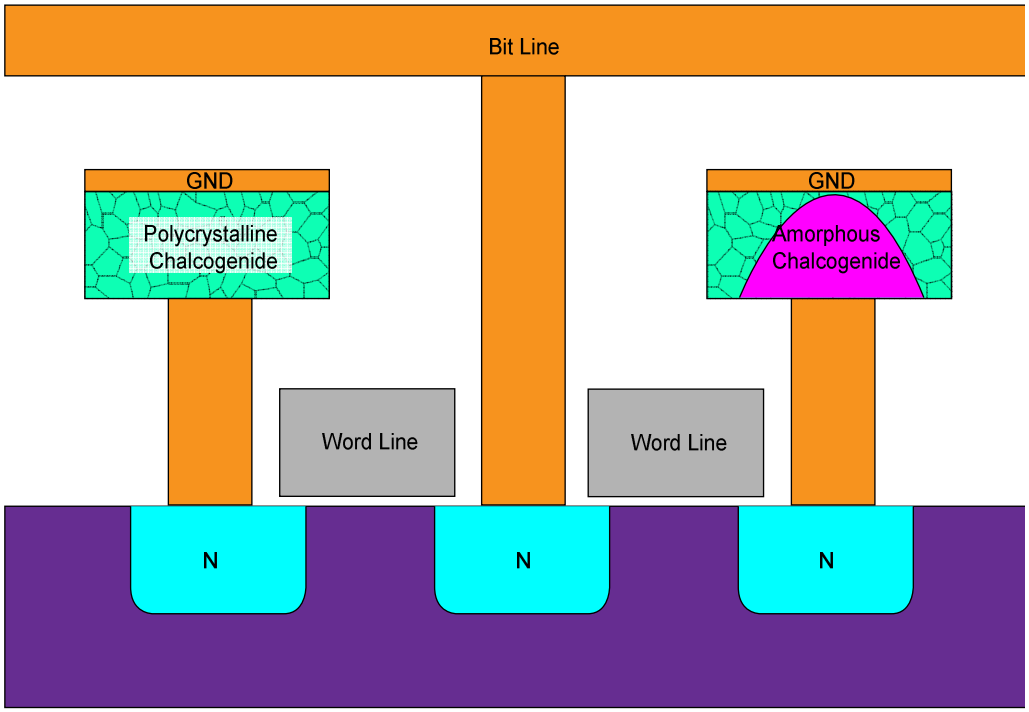


Figure 7: A cross section of two PRAM memory CELLS (One cell is in low resistance crystalline state, the other in high resistance amorphous state) [16]

Density:

The main concern in area arises from the fact that very high current ($>10^5$ A/cm^2) is needed to be passed through the active volume to change the chalcogenide phase. This requires a relatively large drive transistor that results in an area disadvantage. PRAM program and erase are destructive processes, i.e. they slowly degrade the PRAM cell. However, it has been shown that a PRAM cell can sustain 10^8 writes which is much more than FLASH. Moreover, current has to target each cell

independently, with the reduction in active area size cells tent to degrade faster.

Power Consumption:

PRAM cells require high voltage (> 12 V) to provide enough bias to drive sufficient current into the active area. This results in a power disadvantage. Also, as technology shrinks, this enormous current inevitably leaks into neighboring cells resulting in an increased power penalty. More importantly, since heat energy (through passing very high current in a small area) is used to program and erase PRAM cells very close attention is needed to ensure proper isolation of PRAM cells. The heat energy wasted in the process of program and erase is lost resulting in more electrical power consumed.

Speed and Performance:

While slower than DRAM, studies showed that PRAM can achieve switching times as low as 5ns. This is orders of magnitude faster than FLASH.

Disadvantages:

Power consumption is a concern with PRAM. Most emerging NVM technologies do not require any high voltage circuitry and use currents in the order of a few nano-Amps. Another major disadvantage of PRAM is its temperature dependence that requires significant changes to the

fabrication process. PRAM has to be programmed on board after solder as the high temperature solder process can change the PRAM cell phase.

Medical Devices Considerations:

The high voltage required to generate very high current density greatly increases PRAM power consumption. In addition, both reliability and temperature isolation concerns arise from the PRAM dependence on heat for program and erase functions. Like Flash, high voltage circuitry is needed to produce the high current intensity. High current operation means that it will be very difficult to embed PRAM into a digital chip.

2.6 PMC (CBRAM)

Recently with the great advances in the semiconductor industry and the continuing enhancement in processes that are capable of producing minimum dimensions in the sub 20nm range. It has become clear that memories that rely on charge storage (Flash, DRAM …etc) will have a hard time keeping up its data retention or state detection reliability with the continuously shrinking technologies. This is due to the fact the a minimum amount of charge need to be stored or trapped to result in a significant change in the cell resistance or threshold voltage to be reliably detected.

As recorded in the International Technology Roadmap for Semiconductors (ITRS) semiconductor memories that rely on charge storage may reach its scalability limits in the few years to come[10].

Among the most promising alternative NVM technologies is the CBRAM (conductive bridge memory) or PMC (Programmable Metallization cells). Like PRAM, PMC memory is a type of RRAM (Resistive Random Access memory) that rely on data storage via changing the resistance of a material rather than charge storage. PMC memory show the potential of overthrowing Flash and becoming tomorrow's ultimate memory. Studies on PMC show excellent scalability, speed, data retention, endurance, as well as power efficiency [3]. More importantly, it is very cost efficient as its fabrication requires few back end of Line (BEOL) flow steps which makes it compatible with most fabrication processes currently in place. The PMC technology utilizes the electrochemical formation and dissolution of conductive bridges or pathways made of highly conducive metals such as silver or copper through thin film solid electrolytes. These electrolytes have very high permeability to allow for high metal ion mobility through the electrolyte. They are typically chalcogenide (compounds containing element form the periodic column headed by oxygen with glass like properties). Conductive metal atoms such as silver or copper are then dissolved into the electrolyte. A thin film of the metal doped electrolyte is placed between an inert electrode and a silver or copper (depending on

the doping metal) to form the oxidizable electrode. Under normal conditions, the electrolyte exhibits a very high resistance due to the high resistivity of the electrolyte. By applying a bias voltage in the order of a few hundred mV ions form the metal electrode will be reduced at the inert cathode. Close by ions in the electrolyte will move to fill in for the reduced ion until eventually an ion moves from the metal anode into the electrolyte as shown in figure 8. Charge neutrality is maintained through the reduction of ions at the cathode and new ion moving into the electrolyte. The electro deposition process continues until a nano wire resulting form the accumulation of the conductive metal atoms on the cathode is formed between the electrode and the cathode. The formation of this conductive bridge results in the reduction of the device resistance by many orders of magnitude (approximately 100 kOhms) [1].

The resistance reduction is very considerable once the conductive bridge is formed, however, if the bias voltage needed to sustain the electro-deposition process is removed before then, the electro-deposit process ceases leaving the structure with a still high resistance. Once the conductive bridge is formed the current through the device surges to the current limit value set by the current limiter and the voltage across the device decreases to the threshold of the electro deposition causing the process to stop [1]. It is also worth mentioning that the threshold voltage

required to maintain the electro-deposition process is lower that the threshold voltage required to initiate the write process.

Resetting the device back to its high resistance state is done by reverse biasing the electrodes causing the electro deposition process to be reversed. In this process, the inert electrode along with the electrodeposited metal is made to be more positive than the oxidizable electrode. This will cause the deposited metal to dissolve in the electrolyte in the form of ions. The ions are the move to the low density atom area in the metal electrode where the ions were dissolved in the programming process. Once the conductive bridge is dissolved the process self terminates.

Theory of Operation:

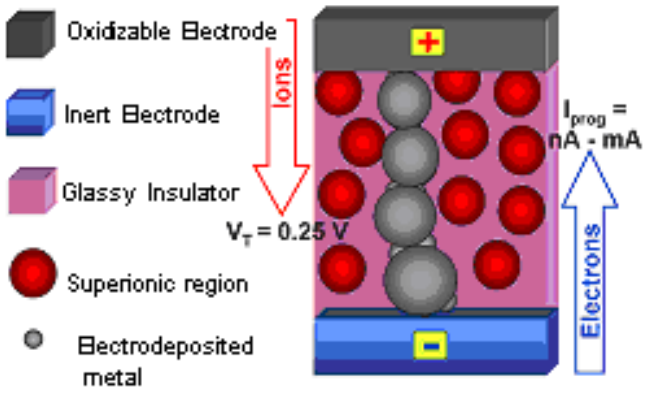


Figure 8. PMC program operation; Ion are reduced on the inert electrode forming a nano-wire (bridge) reducing the resistance of the PMC [17]

In essence , the PMC technology relies on the electrochemically changing the resistance of ion conducting material through the formation and dissolution of metallic pathways in the ion conducting material (e.g. Ge-Se electrolytes) sandwiched between an oxidizing electrode and inert electrode [6].

The programmable metallization cell is essentially an alloy of conductive metal atoms (e.g. Ag or Cu) dissolved in an ion conducting electrolyte placed between two electrodes. When a bias of a few mV is applied for a few nano-seconds [3] to the electrodes, a conductive pathway of metal is formed by oxidizing metal ions from the oxidizable electrode (e.g. Ag) that migrate through the electrolyte and are reduced on the inert electrode. This process continues until a nano-wire if formed between the two electrodes. This reduces the resistance between the electrodes by many orders of magnitude. The state of the PMC can be easily detected by simply sensing the resistance between the electrodes. No sophisticated sense circuitry is needed as the difference in resistance is lower by many orders of magnitude between the ON and OFF states.

Density:

Programmable Metallization Cells have a great advantage over other emerging memory technologies when it comes to area and scalability. Even though this memory technology is still in the characterization stage, robust functionality has been demonstrated for cell

with diameter of 20nm [14]. Theoretically feature size is projected to be shrinkable to 5-10 nm [10]. Literature showed that Vth and the ON resistance do not get vary much by reducing the cell size while the OFF resistance decreases as expected (figure 9). The difference between the ON and OFF resistance increases making the PMC allowing the PMC to be fully scalable.

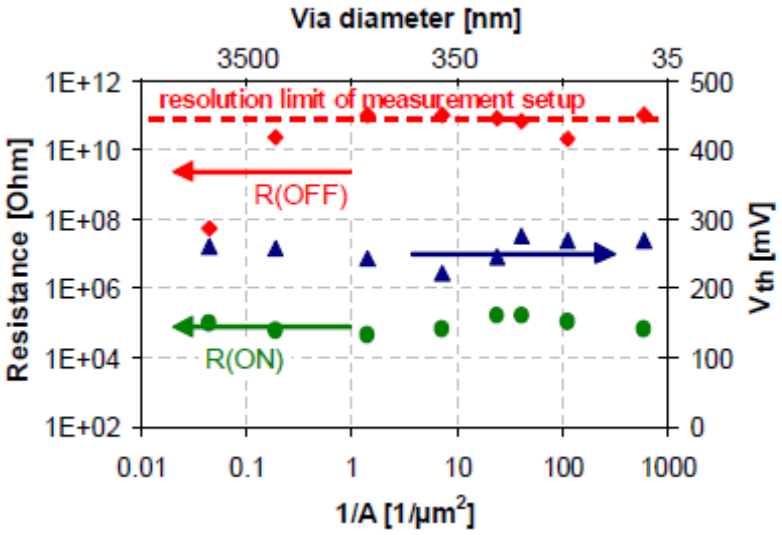


Figure 9. Scalability of CBRAM switching parameters from 5µm to 40nm at room temperature, with the contact area A of the tungsten plug [14]

Power Consumption:

PMC memory operation consumes ultra low power which makes it very suitable for use in medical devices. PMC memory write current are as low as 1nA (1nA -1 mA) [6]. A few hundred mV are applied for both program and erase for only a few tens of nano seconds (as low as 20ns) [10]. Moreover, simple sensing circuitry can be used to detect the state of

the PMC due to the great difference in resistance between the OFF and ON states.

Data Retention and Reliability:

Data storage through the displacement of ions in PMC has proven very reliable. PMC show great durability. Even after 10 years the difference between the ON and OFF states are still extremely wide (10^{-2}) [6], [9] and [14]. Figure 10 shows robust data retention for more that 10 years at 50 and 70 degree Celsius. Studies have shown that PMC technology operate at a wide temperature range. Figure 11 shows that the dependence of PMC critical parameter on temperature. The threshold voltages and ON resistance do not vary significantly by varying temperature. The OFF resistance slightly decreases with temperature but stays orders of magnitude large that the ON resistance.

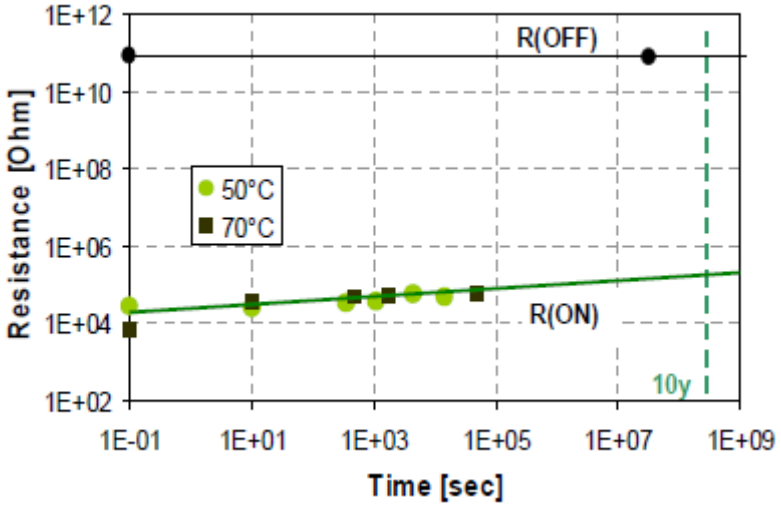


Figure 10. CBRAM data retention measured at elevated temperatures (via diameter 850nm) [14]

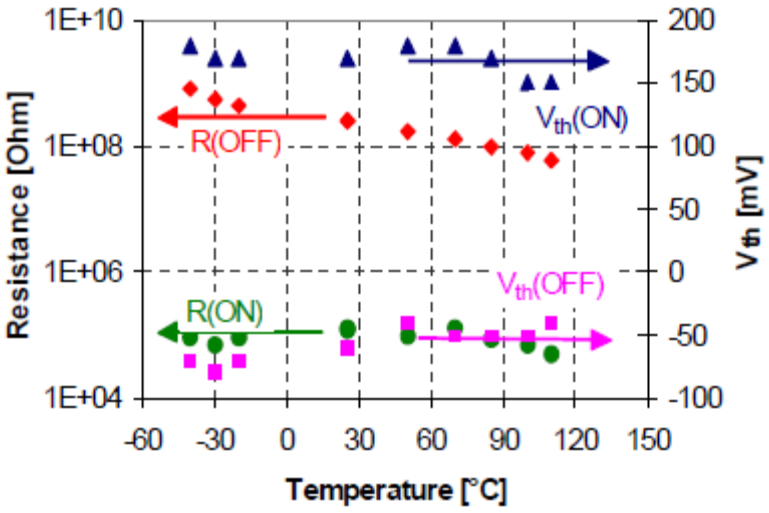


Figure 11. CBRAM switching parameter at different operating temperatures (viadiameter 380nm) [14]

Write Cycles:

It has been demonstrated that PMC withstand more that 10^{10} switching cycles which is orders of magnitude more than that FLASH maximum write cycles. It has been demonstrated that write currents as low as 1nA are sufficient to write PMC [6]. By carefully controlling the write current the prospect of multi bit storage by performing partial writes where the ions in the electrolyte are oxidized to form only a partial nano-wire. Discrete resistance states can be formed by varying the programming current which affects the shape of the nano-wire. 2^n states are required to store n bits. Literature shows PMC is capable of producing at least 4

discrete states by varying the programming current as shown in figure 12 and 13.

Speed and Performance:

Access time of less that 40ns have already been demonstrated [7]. This is many orders of magnitude lower than FLASH access times. ITRS projects PMC cycle times to be reduces to 20ns [ITRS 2009]. While this extremely fast speed in not an essential characteristic for memories used in medical devices, it is easy to see that great power consumption advantage this access time will produce and the impact on product longevity.

Future Enhancements:

PMCs show unique switching characteristics that could be used to expand the PMC to store multi bit data in a single cell. In PMC programming current (Iprog) passing through the device is a major factor in determining the shape of the nano-wire bridge formed and hence the final low resistance of the device. This process can be used to create multi-level capability (MLC). Figure 12 demonstrates the final ON resistance vs. the programming current. It is noted that even at the higher ON resistance (approximately 10^6 Ohms) is still at least an order of magnitude lower than the OFF resistance as shown in figure 13.

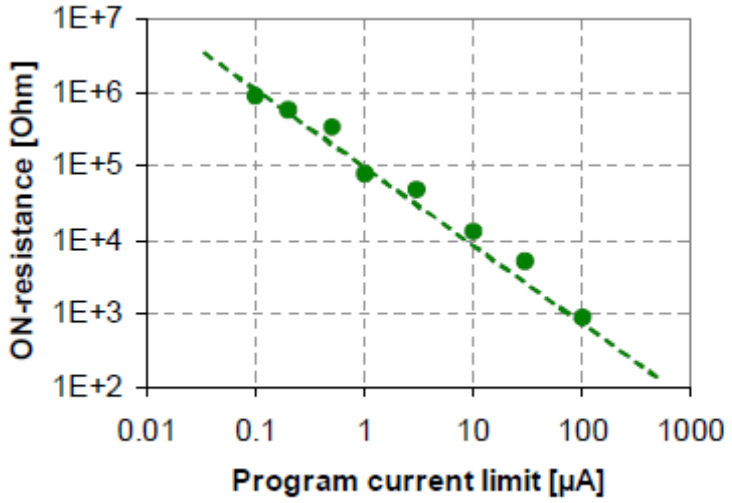


Figure 12. Dependence of the ON-state resistance on the programming current for cbram devices (via diameter 380nm) at room temperature [14]

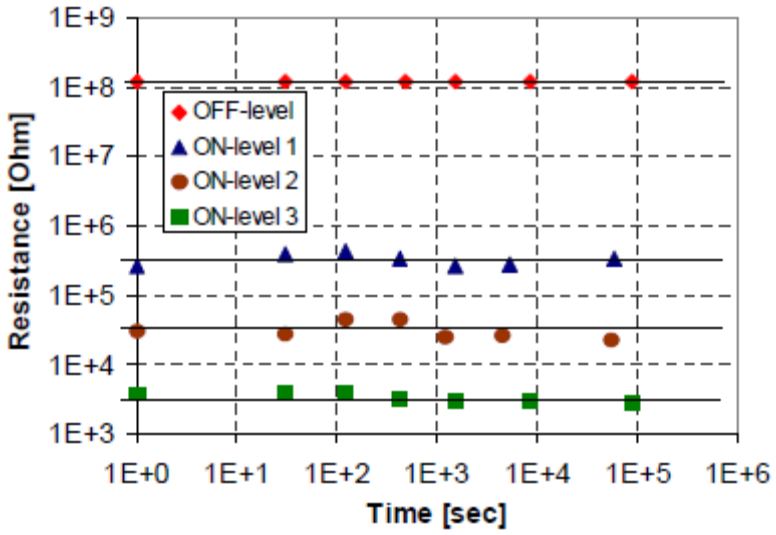


Figure 13. CBRAM multi-level capability, programming currents for ON-levels 1: 0.5µA, 2: 2µA, and 3: 20µA, respectively (via diameter 100nm) [14]

Disadvantages:

Since a PMC element needs only a few hundred mV to write and erase. Close attention need to be paid to the sensing voltage. The sensing voltage need to be closely controlled and significantly lower than the already low program and erase voltages. While this is beneficial for lower power consumption this type of memory requires a very controlled voltage source for reads [9].

Medical Devices Considerations:

Programmable metallization cells memory technology is ideal for use in medical devices. It requires very low voltage for program and erase operations resulting in power consumption that is orders of magnitude less that flash. It also does not require any high voltage circuitry resulting in a very low first bit cost. It is very easily integrated into the logic process with only two additional steps required to embed PMC in digital chips. It also showed very robust performance and can withstand many write and erase cycle and very long time periods. It also shows great potential for scalability and multi-bit storage which is something FeRAM does not offer.

2.7 NVM Critical Parameters Comparison:

Even though the CBRAM technology is in the early stages of development when compared to more mature new NVM technologies like FeRAM or MRAM, CBRAM is projected to have a superior overall performance when compared to other new memory technologies. The International Technology Roadmap for Semiconductors (ITRS), an independent research organization projects CBRAM to have superior feature size, overall are, data retention as well as write, erase and read time. The table below compares CBRAM side to side with other memories. The table demonstrates superior projected performance for CBRAM in each critical parameter. Date was obtained from the 2009 ITRS report.

		DRAM			Floating Gate (FLASH)					
		stand Alone	Embedded	SRAM	NOR	NAND	FeRAM	MRAM	PCM	CBRAM
Storage Mechanism		Charge on Capacitor		interlocked state of logic gates	Charge on Floating Gate		Remnant polarization a ferroelectric capacitor	Magnetization of Ferromagnetic layer	Reversibly changing amorphous and crystalline Phases	nano-bridge
Cell Elements		1T1C		6T	1T		1T1C	1(2)T1R	1T1R	1T1R/ 1D1R
Feature Size (nm)	currently demonstrated	50	65	65	90	90	180	130	65	180

	best projected	8	20	10	18	18	65	16	8	5-10
Cell Area	currently demonstrated	6F2	(12-30)F2	140 F2	10F2	5F2	22F2	45F2	16F2	
	best projected	4F2	(12-30)F3	141 F2	10F2	5F2	12F2	10F2	6F2	5F2
Read Time	currently demonstrated	<10ns	1ns	0.3ns	10ns	50 ns	45ns	20ns	60ns	3ns
	best projected	<10ns	0.2ns	70ps	1.5ns	8ns	<20ns	<0.5ns	<60ns	<3ns
Write/Erase Time	currently demonstrated	<10ns	0.5ns	0.3ns	1 us/ 10ms	1ms/ 0.1ms	10ns	20ns	50ns/ 120ns	3ns
	best projected	<10ns	0.15ns	70ps	2 us/ 10ms	1ms/ 0.1ms	1ns	<0.5ns	50ns	<1ns
Data Retention	currently demonstrated	64ms	64ms		>10y	>10y	>10y	>10y	>10y	>10y
	best projected	64ms	64ms		>10y	>10y	>10y	>10y	>10y	>10y
Maximum Write Cycles	currently demonstrated	>1E16	>1E16	>1E16	>1E5	>1E5	>1E14	>1E16	>1E9	>1E9
	best projected	>3E16	>3E16	>3E16	>1E5	>1E5	>1E16	>1E16	>1E15	>1E16
Write Operating Voltage (V)	currently domstrated	2.5	2.5	1	12	15	0.9 - 3.3	1.5	3	?
	best projected	1.5	1.5	0.7	12	15	0.7-1	<1.5	<3	?
Read Operating Voltage	currently demonstrated	1.8	1.8	1	2	2	0.9 - 3.3	1.5	3	1.5
	best projected	1.5	1.5	0.7	1	1	0.7-1	<1.8	<3	0.7

Write Energy (J/bit)	currently demonstrated	5.00E-15	5.00E-15	7.00E-16	>1E-14	>1E-14	3.00E-14	1.50E-10	6.00E-12	?
	best projected	2.00E-15	2.00E-15	2.00E-17	>1E-15	>1E-15	7.00E-15	1.50E-13	<2E-13	?

Chapter 3

3 Embedded PMC Modeling in Verilog A

In chapter 2 a thorough study on available non-volatile memory technologies suggested that PMC technology is the most suitable for use in medical devices as a potential replacement for Flash memory followed by FeRAM technology. Currently several medical devices used in study uses 256Kbyte of embedded flash memory along with a 16Kbyte SRAM chip. The goal is to simulate the power, area and reliability advantage of using PMC to replace embedded Flash memory. An easy , low cost to simulate the use of the PMC is to build a behavioral model that is then used to build a virtual PMC memory array that can be then simulated and compared against Flash. The model will be used to simulate the replacement of Flash with PMC in the microcontroller in the Medtronic Adams Pacemaker Family. The results from these simulations should provide an idea about the power saving when compare to the current embedded Flash memory. We shall use the electrical characteristics of Ag-Ge-Se PMC elements while choosing the right size driver transistor.

3.1 HDL Behavioral Modeling of Analog subsystems in Mixed signal chips:

Today's mixed signal IC's are becoming more complicated carry more features than ever before. While the digital portion of mixed signal system is adequately simulated and verified using HDLs, it is much more difficult and more time consuming to simulate analog blocks using simulation engines like SPICE or SPECTRE. While using these simulation engines is necessary to verify analog blocks, it has proven to be extremely inefficient to be used as the main instrument to verify analog digital interaction as well as other system level simulations. In a moderate size ASIC these each simulation may take days.

Conventionally, analog blocks were simulated in isolation of the rest of the system and then integrated into the system and the analog digital interface was sometimes verified visually. This method while might have been adequate for smaller system is very preliminary and normally rely on the designer's thoroughness. It also does not verify the active interface of timing. Moreover, with today's large systems, it can be impractical to use visual inspection.

With the rising cost of new technology mask costs and the increased complexity of mixed signal design , it has been evident that a new verification method is needed that can verify the block level integrations

and interface and also do that in a manner that does not impact the time to market of the IC.

Using analog block behavioral modeling HDL in verifying system level interactions has proven to be a practical way of verifying system and block level interactions without the time overhead of simulating the whole system in gate level. Behavioral modeling allow for a flexible level of extraction where the designer can define the behavior of an analog block at a top level or at a level very close to the actual circuit. Depending on the level of abstraction running mixed signal simulations using behavioral models is a lot faster that running the actual gate level simulation. Moreover, depending on how the system is portioned the designer has the flexibility of running actual analog blocks and behavioral models for others depending on his simulation targets. Most mixed signal simulations engine (like Cadence AMS simulator) and other allow the flexibility of running blocks in different languages at once (RTL, Verilog A/ AMS, Spectre, gate level etc.)

Another benefit it that behavioral modeling allows system designers to compare different system options in initial planning stages without having to go through the design cycle. Using general information about analog blocks, system engineers can construct a behavioral model for a specific block or IP and simulate their system with it to compare its performance. A clear example of this application is using behavioral

models for embedded memories. By knowing the most critical memory characteristics normally available in the public domain and without the need to develop the actual memory, one can the study the system behavioral when using different memory types and compare critical parameters such as speed and power consumptions.

This paper presents the use of a Verilog A behavioral model to mimic the behavior of PMC (CBRAM) and compare it to an existing system the uses EEPROM.

3.2 PMC Cell Physical Model:

The Verilog A model used to represent the PMC single bit cell was derived from the Spice model presented in [8]. The SPICE model used in this study was developed by Nad Gilbert and presented in [8]. The spice model in figure 14 representing the PMC single bit cell presented in [8] can be divided into four sections. Physical parasitic, threshold comparators, Write dynamics and Erase dynamics. The Verilog A model will ignore the physical parasitics except for the cathode and anode parasitic capacitors that are represented in the slew defined for the current to ramp up.

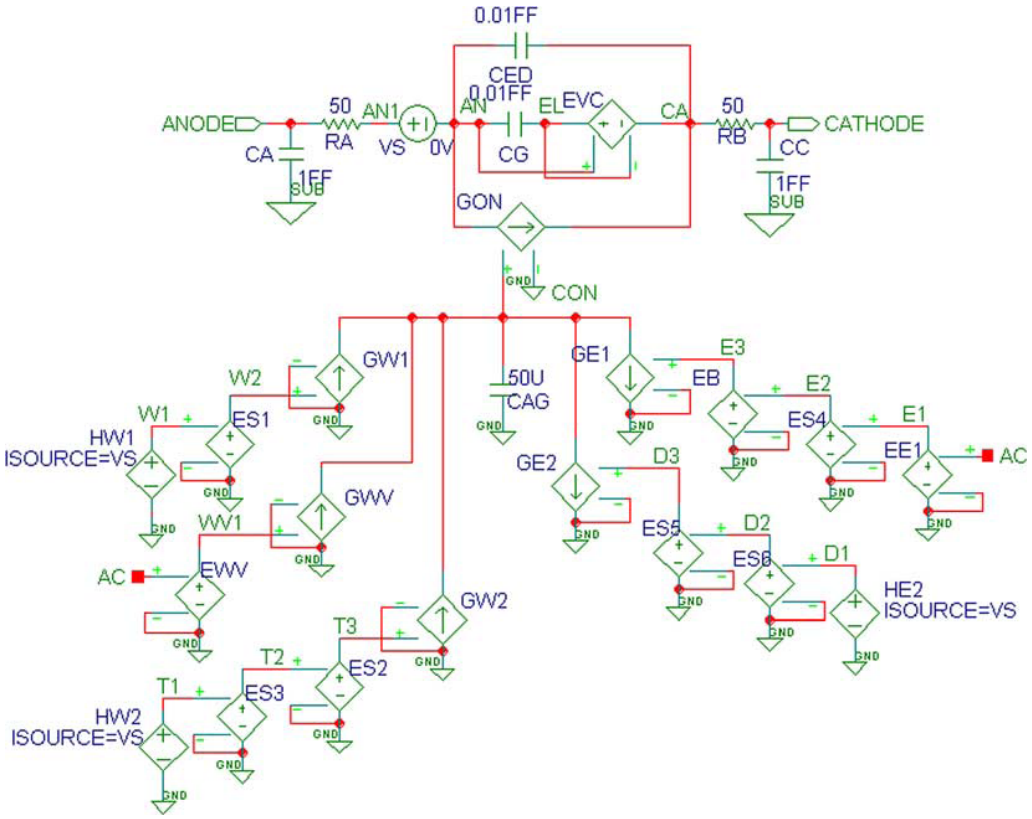


Figure 14. PMC SPICE MODEL representing the PMC single bit cell [8]

In both the Spice and Verilog A models the PMC write and erase dynamics are represented by the CAG and a voltage dependent current source acts as a voltage controlled resistance, these elements emulate the oxidation and reduction of Ag in the electrolyte hence representing the write and read process.

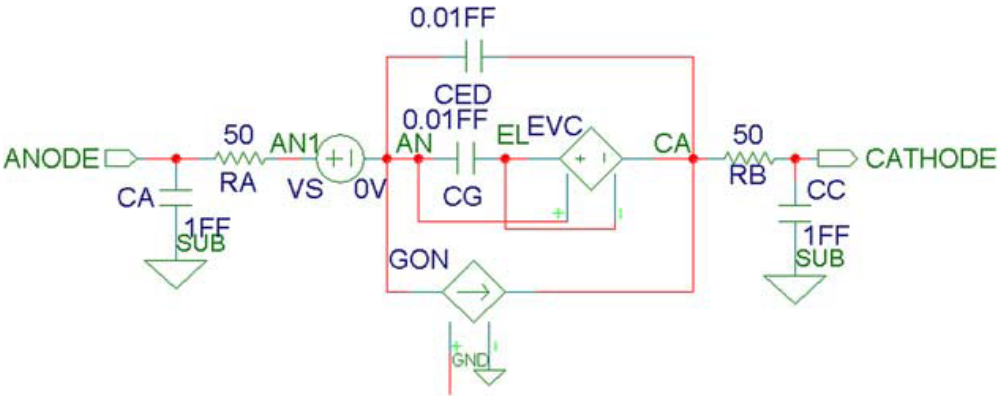


Figure 15. PMC parasitics equivalent circuit [8]

Figure 15 shows the equivalent circuitry of a PMC device. Capacitance CA represents the anode parasitic capacitance and CC represents the parasitic capacitances of the cathode to the substrate. RA and RC represent the electrodes contact resistances. Capacitance CED represents the capacitance of the dielectric around the electrolyte material. Capacitance CG in series with the voltage controlled voltage source model the variable capacitance of the PMC device. The capacitance CG decreases when the cell is written and increases when the cell is erased.

In the Spice model a write process is represented by increasing the charge stored in the capacitor CAG hence increasing the current GON effectively decreasing the resistance between the anode and the cathode. In the erase process electrons are pulled off the capacitors which decreases the reference voltage in the GON and its output current, hence

decreasing the over all resistance of between the anode and the cathode. The current output of GON is controlled by:

$I_{Gon} = V_{an;ac} \times Y_{con} + (V_{an;ca} / R_{off})$ eqn. 1 ref [8]

Or

$R_{on} = R_{off} / (R_{off} + Y_{con} + 1)$ eqn. 2 ref [8]

$-Y_{con}$ is numerically equivalent to node voltage CON which is designed to never go below 0V.

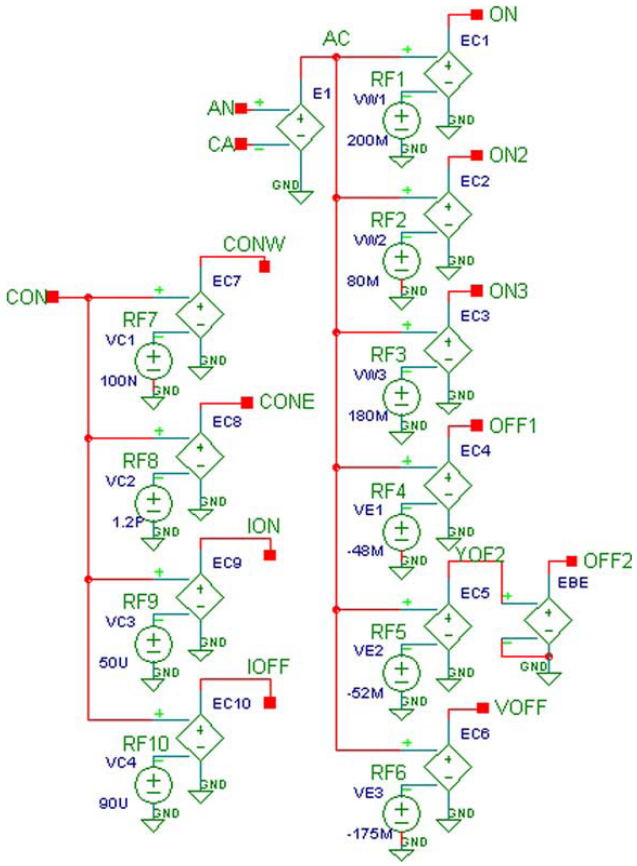


Figure 16. Comparators and thresholds for PMC switching dynamics [8]

In the spice model, voltage comparators (shown in Figure 16) are used to monitor the voltage across the electrolyte and trigger a write or an erase. The voltage difference between nodes AN and CA is measured by E1 and then compared to a number of references. SPICE E-Elements and reference voltages are used to initiate and stop write and erase processes in the spice model. E-Elements EC1, EC2, and EC3 and their corresponding reference voltages RF1, RF2 and RF3 are used to trigger the three write modes. E-elements EC4, EC5, EC6 and their corresponding reference voltages RF4, RF5, and RF6 are used to trigger the erase processes. EC7 and RF7 are used to trigger a write when the electro-deposition process on the cathode has already started also known as a “second write”. A second write requires less threshold voltage than when the oxidation-reduction process needs to be initiated. E-element EC8 and reference RF8 are used detect the device resistance and stop the erase cycle when the resistance of the device has returned to the off value. EC9 and EC10 along with references RF9 and RF10 are used to switch between erase voltage and current modes where current is needed to initiate the electro-deposition process by breaking the link and voltage completes the process.

The E-elements and their corresponding references initiate the write or erase processes. The variance in the cell resistance is achieve by

increasing and decreasing the current flow on COV and hence increasing or decreasing the current though the device and varying its resistance. It is important to note that the write mechanism is drive by both the current through the cell and the voltage across the anodes. The current is an important factor as is contributes to the amount of Ag atoms in the electrolyte forming the conductive bridge. Both current and voltage are used to determine the device resistance in the Spice model.

The three write mechanism are triggered by E-elements and modeled as voltage controlled current sources GW1, GWV, and GW2. The write is initiated when the voltage across the cell is large enough to initiate the electro-deposition process. This is determined by EC3 and RF3 in figure16. Once this write mechanism is triggered element EWV multiplies the voltage across the cell by a gain determined experimentally by curve fitting and converts it to current from GWV that is then integrated over time resulting in a voltage across CAG. As a result the voltage controlled voltage source CON creates current form across the device. After the electro-deposition process starts and current starts flowing across the device, the current contribution is modeled by GW1. The comparator EC1 and reference RF1 in figure 16 are used to determine that the voltage threshold have been developed across the device. The current flowing through the device is measured and converted to voltage by HW1 modeling the current contribution factor. The voltage across HW1 is then

converted to current by GW1. The current is integrated across CAG. After the electro-deposition process starts a lower voltage is required to keep it going that that to initiate it. Given that enough voltage is provided to keep the electro-deposition process going (determined by EC2 and RF2 in figure16), the current across the device is measured and converted to voltage by the current controlled voltage source HW2. The voltage controlled current source GW2 then converts this voltage back to current after multiplying it by a gain and integrates it over time across CAG. Depending on the voltage across the cell and whether or not the electro-deposition process has started, one or all three modes can take effect at the same time.

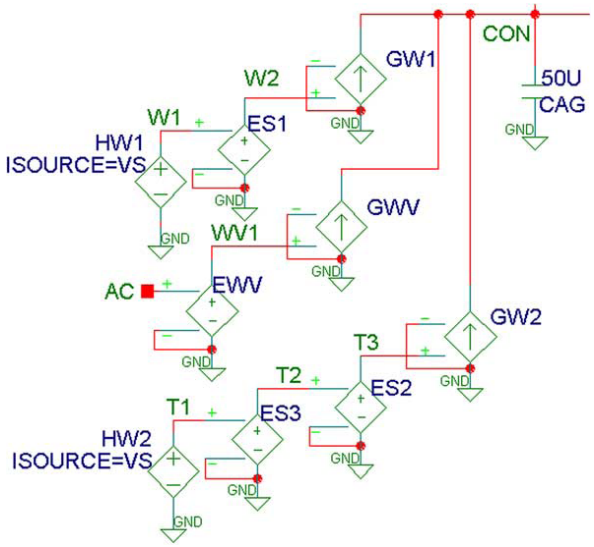


Figure 17. Dynamic write section of SMM for PMC. The sections include, FROM top to bottom, the first threshold current controlled, voltage controlled, and secondary threshold current controlled write operations [8].

The erase circuitry shown in figure18 also depends on both the current and the voltage across the device but in the reverse direction. Comparators EC9 and EC10 control the transition between voltage and current modes. The voltage controlled current sources E1, E2, and E3 convert the erase voltage across the device to current provided the minimum erase threshold voltage is available. The current is in the opposite direction compared to the write current controlled voltage sources. E-element EBE in Fig.10 and E3 in figure18 ensure the voltage at node CON does not go below zero. The fast erase is process is modeled by comparator EC6 in figure 16. When a large negative potential is provided across the device EC10 initiates the voltage mode. GE1 converts the voltage form E1, E2, and E3 to a current that pulls the charge off CAG reducing the voltage at CON and increasing the device resistance. HE2 converts the current across the device to voltage the then passes through ES6 that only allows positive voltage. Depending on the voltage on CON ES5 works as switch that turns on or off the voltage mode. The voltage is then finally turned to current by GE2. The created current pulls the charge off CAG further increasing the device resistance.

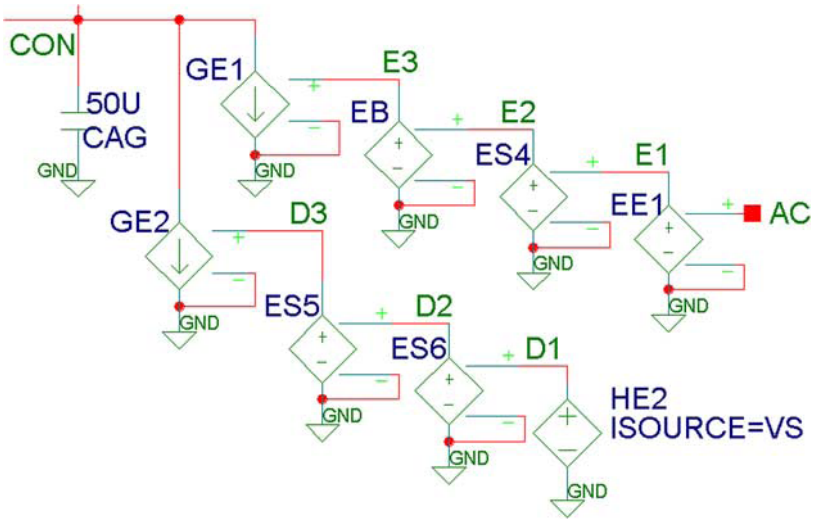


Figure 18. Dynamic erase section of SMM for PMC. The sections include thevoltage and current controlled erases froM top to bottom, ref [8].

PMC Physical Model simulation results ref [8]:

The SMM model discussed in section 6.1 simulated very closely to the lab results for a 0.5 µm diameter $Ag_{33}Ge_{20}Se_{47}$ PMC cell. Results in figures19 and 20 were obtained by applying a voltage sweep from -0.5 to 0.5 volts with the current being limited to 10 µA.

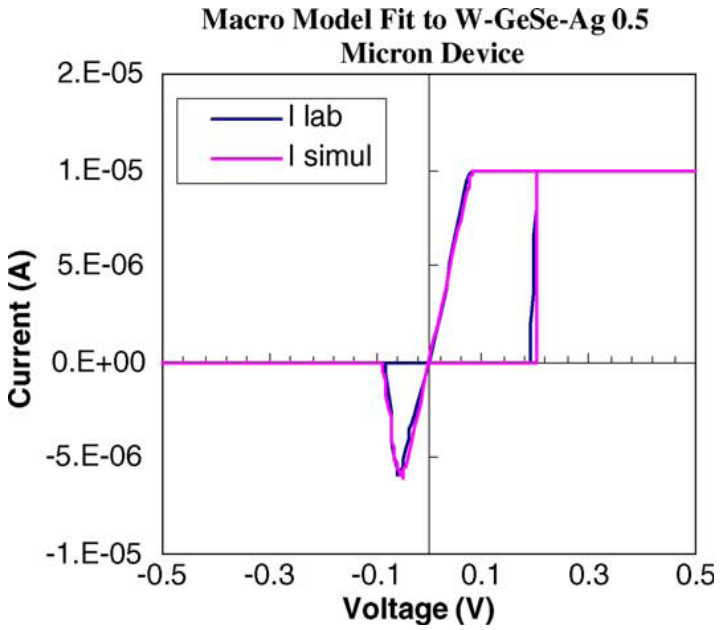


Figure 19. Results of curve fitting simulation data with experimental IV datafrom 4155. The device diameter was 0.5 µm. The current limit was 10 µA, ref [8].

Figure 19 shows that under forward bias the current remains very low the electrochemical deposition threshold of 200mV is reached , then the PMC device resistance is significantly lowered (as shown in figure20) and the current then ramps up until it reaches the voltage limit of 10µA. In a negative sweep on an ON PMC device shows the current remaining at the current limit of 10uA down to about 80mV since the PMC device has already been written before the device becomes ohmic. The constant current is achieved by lowering the voltage across the device. Once the erase threshold is reached at the resistance starts to increase and current is lowered by the erase mechanism describe earlier.

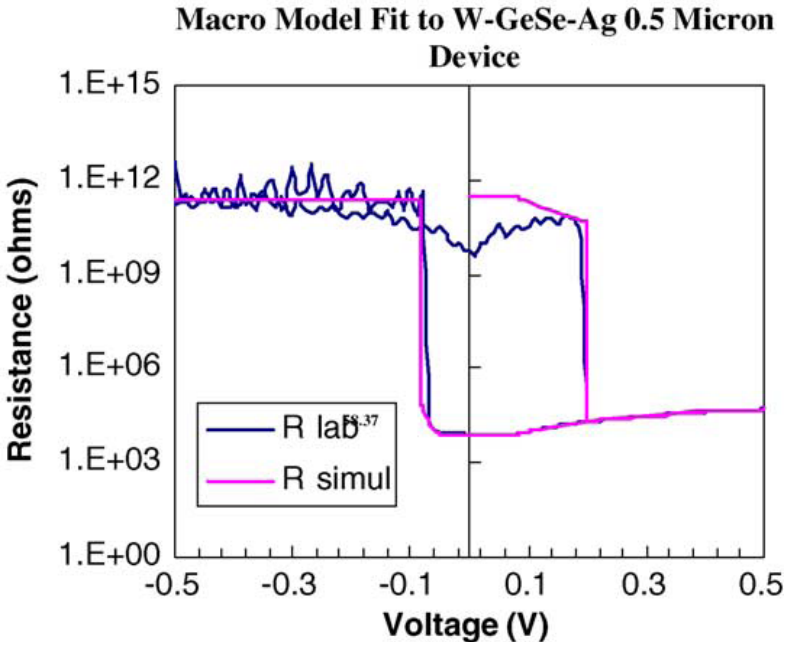


Figure 20. Results of curve fitting simulation data with experimental RV data. The device diameter was 0.5 µm. The current limit was 10 µA, ref [8].

3.3 PMC Cell Hardware Description Language (HDL) Model:

The PMC HDL model follows the same concept the SMM model employs. In fact, the HDL describes the same exact circuit. The main advantage of the HDL model is that is provides the designer with a very fast way to simulate large arrays of PMC memory in a reasonable time frame to acquire top level information regarding the feasibility and benefits of using this type memory in a system. The PMC model used in this study was developed by Nad Gilbert.

To represent the voltage component of the write process, the voltage across the intrinsic device is multiplied by a gain GWV. The defined gain was determined by curve fitting. This converts the voltage across the

device to a current, given by GWV. The current is integrated over time as a voltage on the large capacitor CAG.

VTH1 is the minimum voltage across the PMC device that can initiate the Ag reduction at the cathode and then its oxidation at the anode creating a conductive bridge. In the SMM as well the HDL model no charge is forced on CON until this threshold is reached. The amount of current pumped to CAG is controlled by integration gain value GIW1 that is obtained by experimental results. In the Verilog A model the gain is used to directly reduce the control voltage VCON and hence, resulting in the reduction in the overall resistance of the PMC element.

VTH2 is the minimum voltage across the PMC that will support continuing of the reduction/oxidation process that will lead to forming the conductive bridge. In the Spice model, the amount of current pumped to CAG is controlled by integration gain value GIW2. In the Verilog A model the gain is used to directly reduce the control voltage VCON.
If an excessive voltage of over 0.9 volts WVOV a high gain of GWOV is added to the above mentioned gains. The total of the integration of the above gains over the time that their respective threshold is met result in the amount of the charge stored in CAG in the Spice model.

The verilog A model directly represent CON as a voltage controlled resistance governed by.

```
RCON = (ROFF-RPMCS)/ (ROFF*RPMCS);
```

The voltage across RCON is modified by

```
  V (CON) = idt(V(VWRa,VERa)*1, RCON, RST);
```

Write Thresholds:

To represent the voltage component of the write process the voltage across the intrinsic device is multiplied by a gain GWV, which is determined by curve fitting, and then converts it into a current, given by GWV. The current is integrated over time as a voltage on the large capacitor CAG.

VTH1 is the minimum voltage across the PMC device that can initiate the Ag reduction at the cathode and then its oxidation at the anode creating a conductive bridge. In the Spice model no charge is forced on CON until this threshold is reached. The amount of current pumped to CAG is controlled by integration gain value GIW1 that is obtained by experimental results. In the Verilog A model the gain is used to directly reduce the control voltage VCON and hence, resulting in the reduction in the overall resistance of the PMC element.

VTH2 is the minimum voltage across the PMC that will support continuing of the reduction/oxidation process that will lead to forming the conductive bridge. In the Spice model, the amount of current pumped to CAG is

controlled by integration gain value GIW2. In the Verilog A model the gain is used to directly reduce the control voltage VCON.

If an excessive voltage of over 0.9 volts WVOV a high gain of GWOV is added to the above mentioned gains.

The total of the integration of the above gains over the time that their respective threshold is met result in the amount of the charge stored in CAG in the Spice model.In the verilog model the resulting current and voltage gains are used to vary the control voltage

```
VWR = WI1*GIW1*abs(IPMC) + WI2*GIW2*abs(IPMC) + WV*GWV*abs(VPMC)
+ WOV*GWOV*abs(VPMC);
VER = EI*GIE*abs(IPMC) + EV*GVE*abs(VPMC) + EOV*GEOV*abs(VPMC);
  //Control Voltage
  V(CON) <+ idt(V(VWRa,VERa)*1, RCON, RST);
```

Erase Thresholds:

A similar approach is used to represent the erase cycle with the resulting gain in current converted to voltage that will eventually reduce the control voltage VCON.

3.4 PMC cell level test bench:

After the Verilog-A model for the programmable metallization cell was completed and imported to the Cadence Spectre ® simulation tool. A symbol was created that encloses the Verilog-A model as shown in figure 21. A pulse voltage generator is uses to generate the program and erase pulses. Since the resistance of the PMC is decreased to a low resistance when programmed, a way to limit the current flowing through the device is needed to prevent very high current to flow when the device transitions between ON and OFF states. An easy way to create a current limiter was to construct another Verilog-A model for a current limiter.

3.4.1 Current limiter Verilog-A model:

A current limiter was added in series with the power source to limit the current flowing through the device during the transition between high and low resistance states. The model essentially represents a variable resistance that increases its resistance if the current limit is reached. To allow for maximum flexibility of the model and to study the effects of the limiting the current on the behavior of the PMC device, the maximum current limit it left to be programmable in the model.

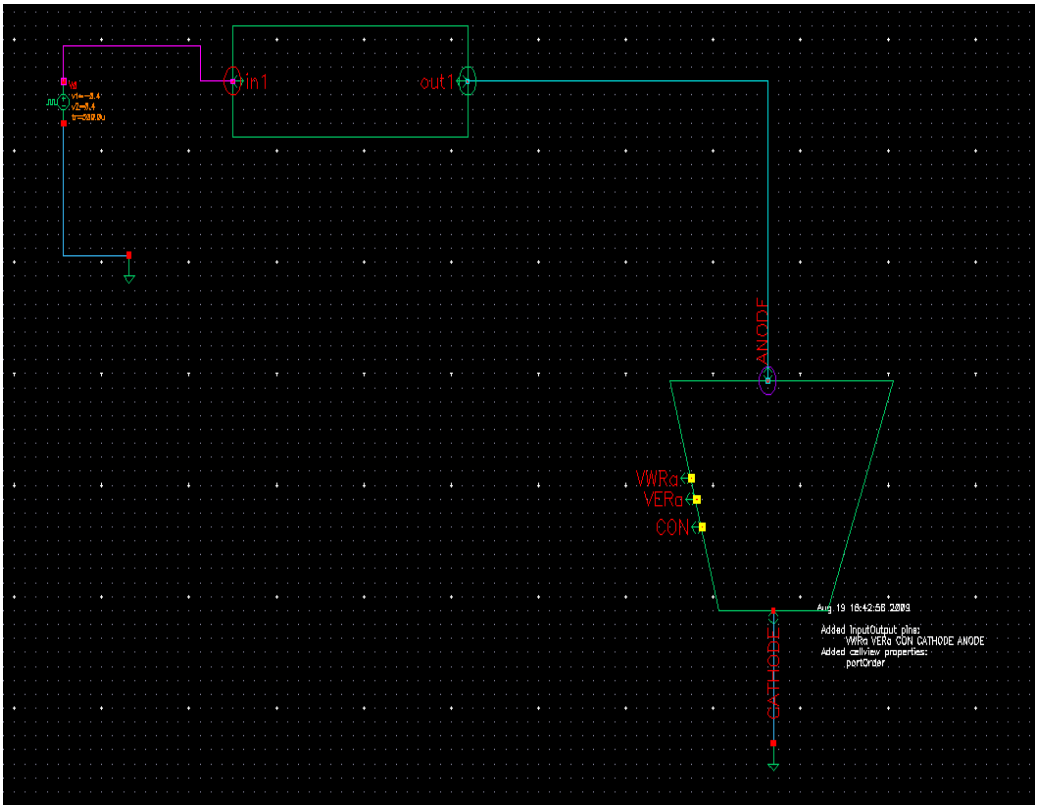


Figure 21. PMC test bench

3.5 PMC Test Bench Simulation results:

The main objective of this project is to prove the feasibility, reliability and the power advantage of using PMC memory technology to replace Flash in medical devices. To do so, a series of simulations were performed to prove the performance of the Verilog models and then to pick the best parameter that provide a reliable memory performance with the minimum power consumption. Moreover, the following simulation provides an insight on the effect of the critical parameter built into the PMC and current limiter model and their effects on the memory performance.

3.5.1 PMC and Current Limiter Basic Functional Simulation:

To prove the operation of the PMC and current limiter model a basic simulation was performed to generate program and erase pulses that are a lot higher than the program and erase threshold voltages. A stimulus square voltage pulse of +-400mv with rise and fall time of 0.3us and a 2us period was used to program and erase the PMC model as shown in figure 22.

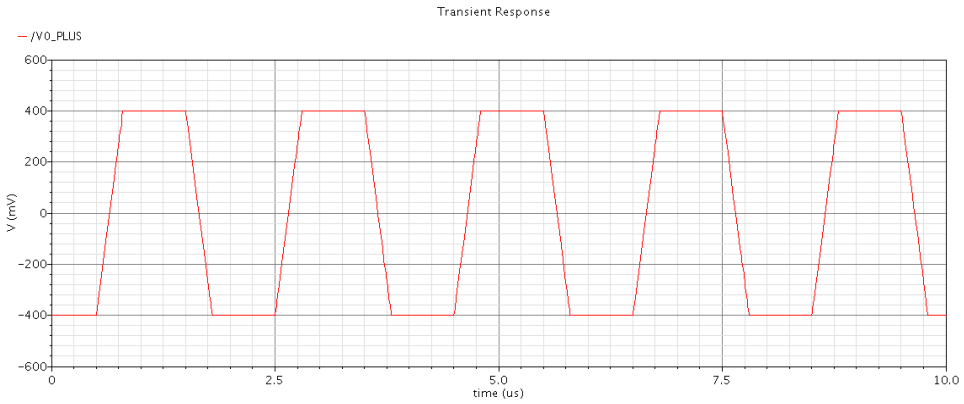


Figure 22. waveform showing input stimulus to the pmc cell

The stimulus voltage source is connected in series with a current limiter to limit the current flowing through the PMC element at low resistance. The current limiter is connected in series with the PMC anode as shown in figure 21. The current limit is programmable in the limiter Verilog-A model. In this case the current was limited to 40uA. This limit will ensure the PMC model is supplied with enough voltage to set is to a low resistance value. Figure 23 shows the output of the current limiter.

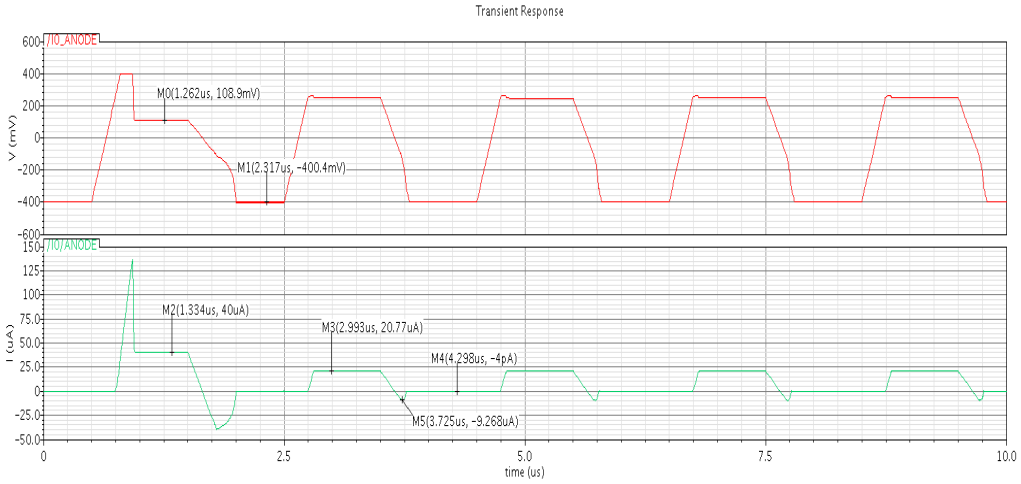


Figure 23. Waveform showing input voltage (top) and current (bottom) to the PMC cell

Figure 23 shows the input current to the PMC anode, the initial positive spike in current shown on the waveform is due to the simulation timing resolution in capturing the response of the current limiter voltage limit.

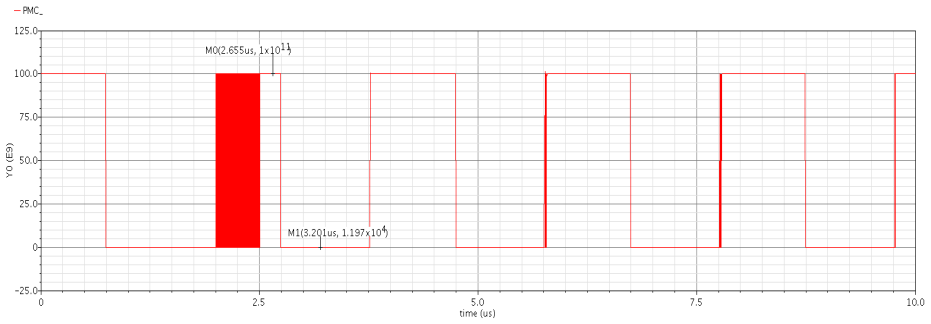


Figure 24. Waveform showing PMC cell resistance switching between OFF (high resistance state) and ON (low resistance state)

This initial simulation proves the basic erase and program operations of the PMC. It also shows that the current limiter successfully limits the current to the value programmed in the current limiter Verilog-A model.

3.5.2 Program Threshold (Vth ON) Simulation:

The programming threshold voltage (described as VTH1 in the PMC model Appendix A) is the minimum voltage needed to start the electro-deposition process and hence to build the conducting nano-wire through the high resistance electrolyte. For the model to behave accurately the PMC resistance in the OFF state should remain the same even when a programming pulse in generated if the voltage on the PMC anode is less than Vth ON. To minimize the programming power consumption the programming pulse voltage should be very close to (but more than) VTH1. This way, adequate switching in achieved with minimum voltage. Another factor affecting the programming pulse power is the duration or period of the pulse. The minimum duration needed to program the device is defined in the model as integration terms as shown in the appendix. Medical devices currently run the digital at relatively low speeds (less that 1MHz) hence a program pulse period of a 1us minimum is adequate for use in medical device. A simulation was performed to prove that the modeled PMC is only programmed when the voltage on the anode is greater than VTH1. When the program voltage pulse was set to 240 mV (less that the

threshold voltage of 250mV) the PMC resistance did not switch to the low resistance stage as shown in figure 26. When the programming voltage was ramped up to just above the threshold voltage 255mV the PMC resistance showed proper switching as shown in figure 26.This models that fact that a minimum voltage is required to initiate the electro-deposition process. It is worth mentioning that the model would allow the PMC programming voltage to be decrease below VTH1 (250mV) once the electro-deposition process starts (one the voltage on the PMC reaches VTH1 for a the minimum time unit) as long as the programming voltage does not fall below the minimum voltage required to sustain the oxidation-reduction process (VTH2 in the model. However, it is deemed impractical and more complicated to use a programming pulse that varies between VTH1 and VTH2 and hence programming pulses above VTH1 was only simulate.

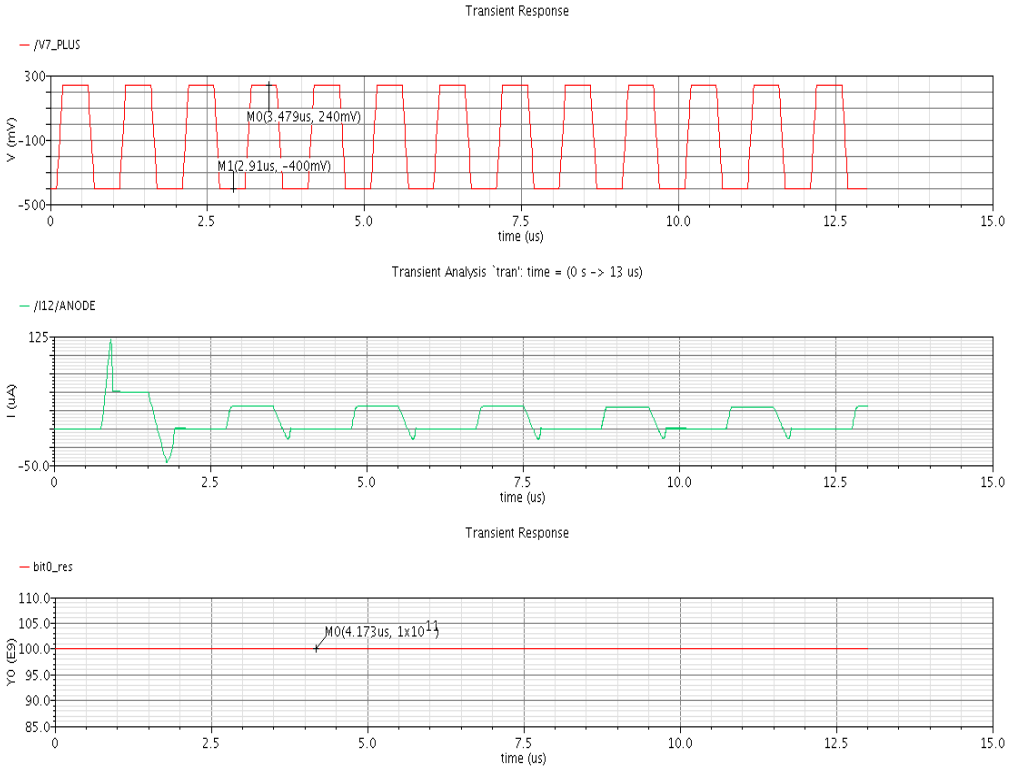


Figure 25. Waveform showing programming voltage (top) 240mV and the current through the PMC cell limited to 50uA (middle). The cell resistance (bottom) did not switch to the low resistance (ON) state as the minimum voltage of 250mV was not provided.

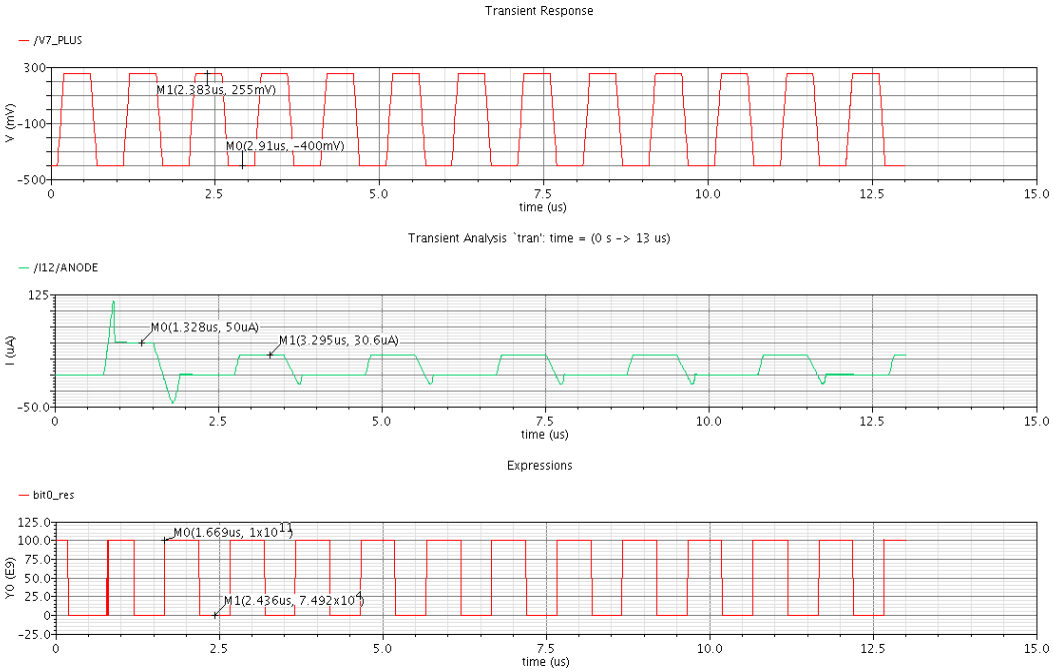


Figure 26. Waveform showing programming voltage (top) 255mV and the current through the PMC cell limited to 50uA (middle). The cell resistance (bottom) showed proper switching to the low resistance (ON) state as the programming voltage was above the minimum voltage required to initiate the electro-deposition process

Effect of modifying the Write threshold Voltage (VTH1):

The Verilog A model can be modified to simulate variability in the PMC important parameters and its dependence on factors like heat, PMC contact area, time, number of writes and programming currents. The model described in this paper allows for varying critical variables by simply changing their value in the model. This can be very useful when expanding the model to simulate second order effect or to fine

tune the model to match the behavior of PMC cells with different dimensions or under different conditions.

As shown in section 2.6 the write threshold voltage is independent of factors like contact area and number of cycle. However, write threshold voltage (VTH1) may vary significantly with factors like temperature. Figure 27 and 28 show the response of the model with VTH ON programmed to 250mV. Figure 29 show that the PMC can be programmed successfully using a programming voltage of 251mV slightly above the threshold voltage. Figure 30 shows that the PMC not being able to be programmed using a programming voltage of 240mV which is below the minimum voltage required to program the PMC.

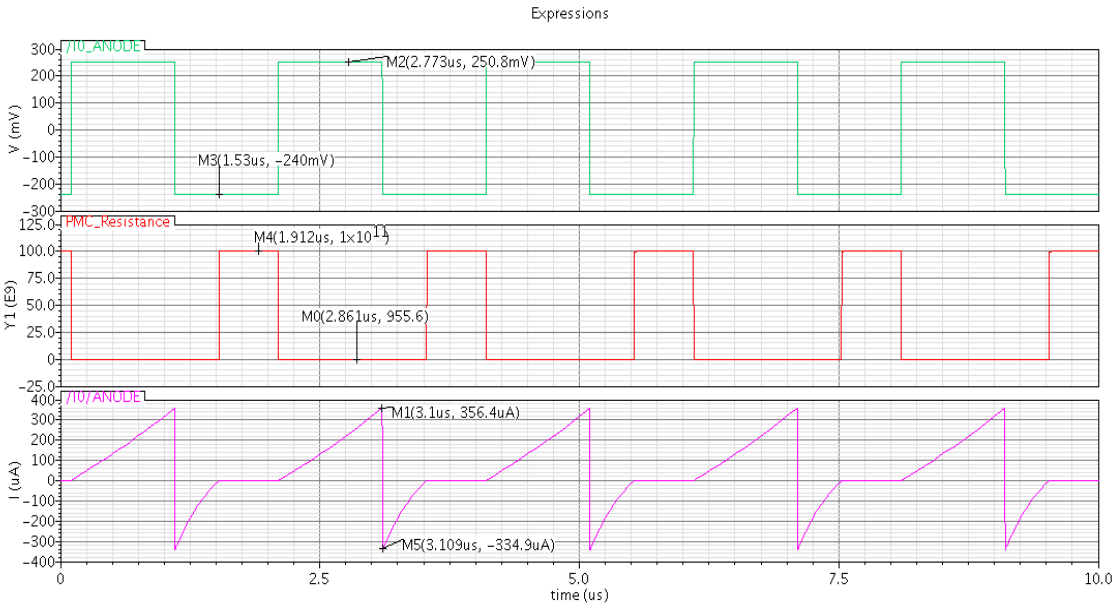


Figure 27. waveform showing waveform showing programming voltage (top) at 251mV and the current through the PMC cell limited to 400uA (middle). The cell resistance (bottom) showed proper switching to the Low

resistance (ON) state as the programming voltage is above the PMC model threshold of 250mV

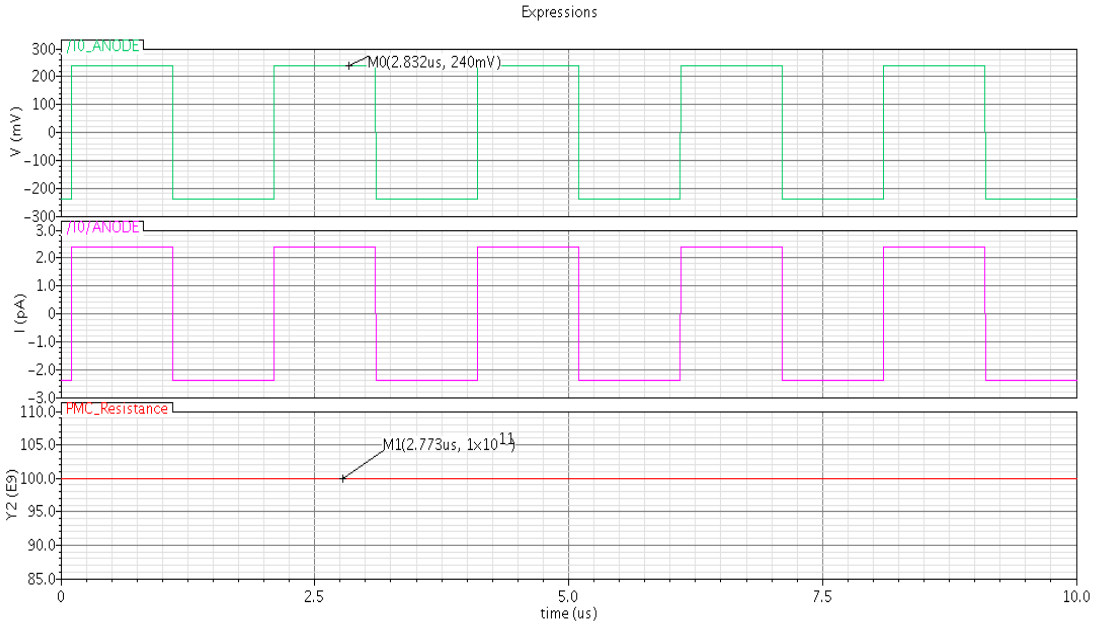


Figure 28. Waveform showing waveform showing programming voltage (top) at 240mV and the current through the PMC cell limited to 400uA (middle). The cell resistance (bottom) showed NO switching to the Low resistance (ON) state as the programming voltage is below the PMC model threshold of 250mV

The same simulation was repeated after modifying the model to reflect a 260mV required programming voltage. Figure 29 shows the PMC programmed successfully using a 261mV pulse while figure 30 shows that a programming pulse with amplitude 255mV was not sufficient to program the PMC.

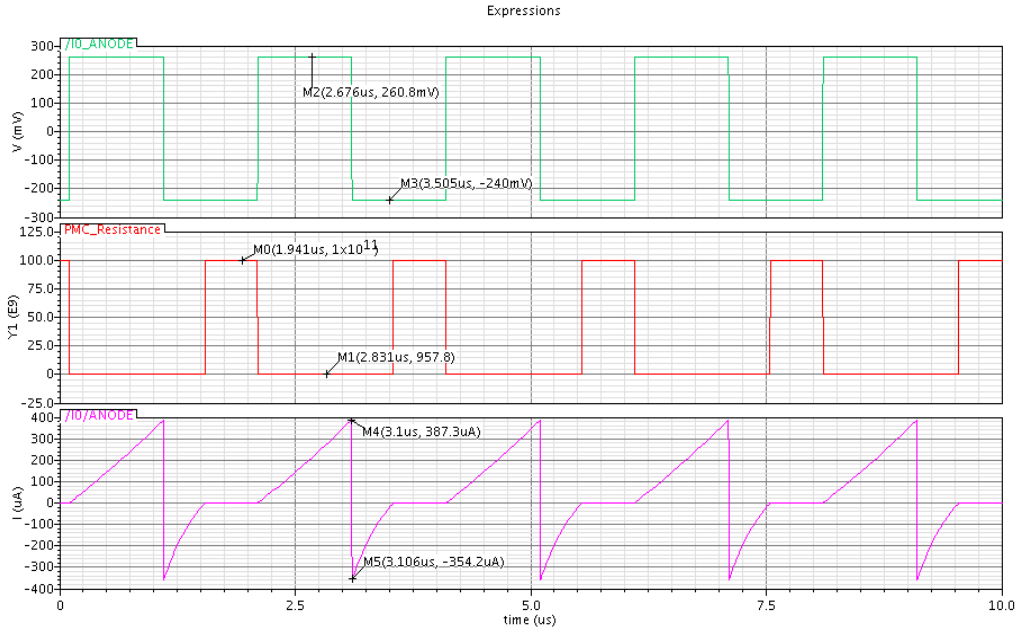


Figure 29. waveform showing waveform showing programming voltage (top) at 261mV and the current through the PMC cell limited to 400uA (middle). The cell resistance (bottom) showed proper switching to the Low resistance (ON) state as the programming voltage is above the PMC model threshold of 260mV

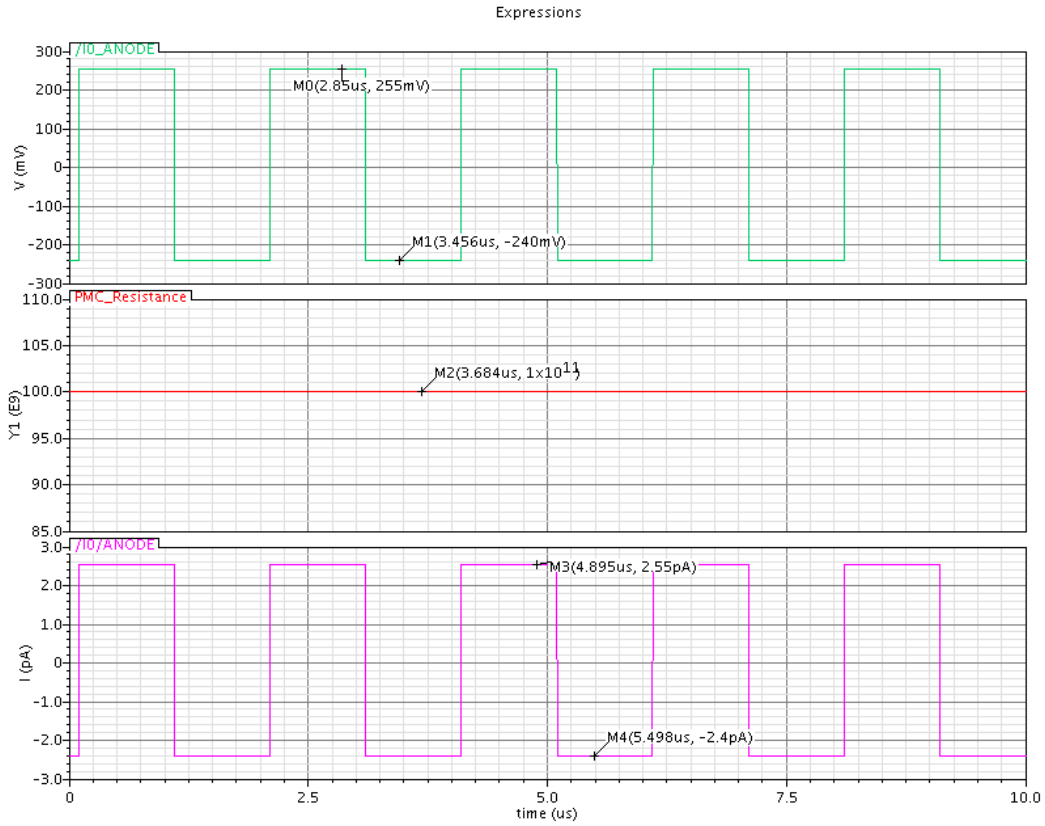


Figure 30. Waveform showing waveform showing programming voltage (top) at 255mV and the current through the PMC cell limited to 400uA (middle). The cell resistance (bottom) showed NO switching to the Low resistance (ON) state as the programming voltage is below the PMC model threshold of 260mV

3.5.3 Erase Threshold (Vth Erase) Simulation:

Much like in the case of programming voltage threshold, a minimum voltage is needed to start the electro-deposition process required to dissolve the conductive bridge and explained in section 2.6. To insure the models accuracy, the programmed PMC model resistance should not be increased (erase) if the erase voltage in less than the threshold defined in the model. With the erase voltage set to 90mV (below the 100mV required to start the erase process), the PMC resistance did not switch back to the high resistance stage as shown in figure 31

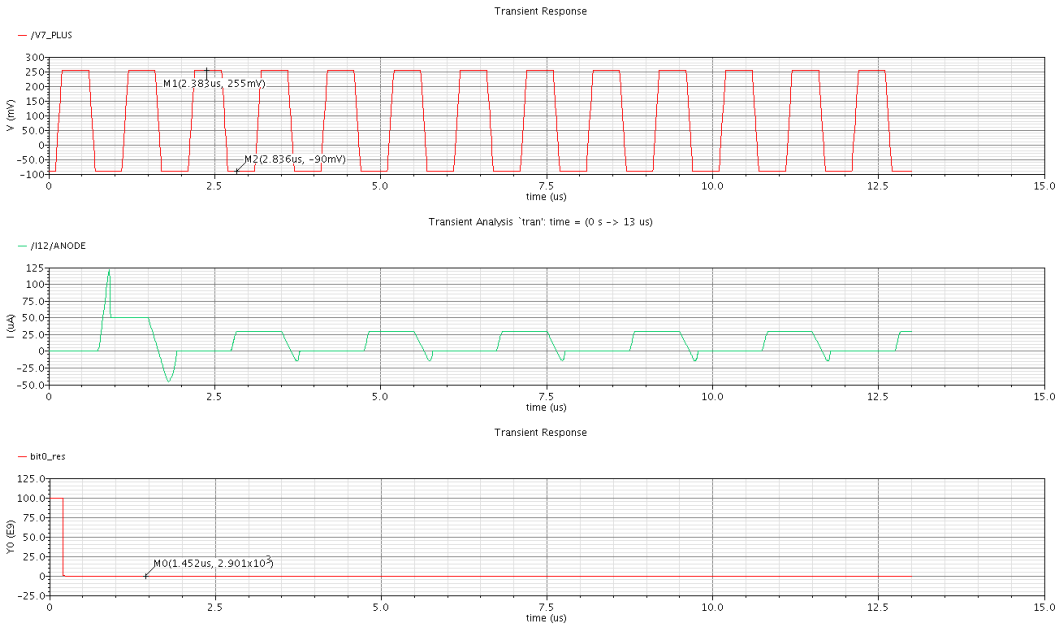


Figure 31. Waveform showing erase voltage (top) set to -90mV and the current through the PMC cell limited to 50uA (middle). The cell resistance (bottom) did not switch to the High resistance (OFF) state as the minimum voltage of -90mV was not provided.

When the erase voltage was increased to -150mV the PMC resistance switch to the high resistance state (OFF) state as shown in figure 32

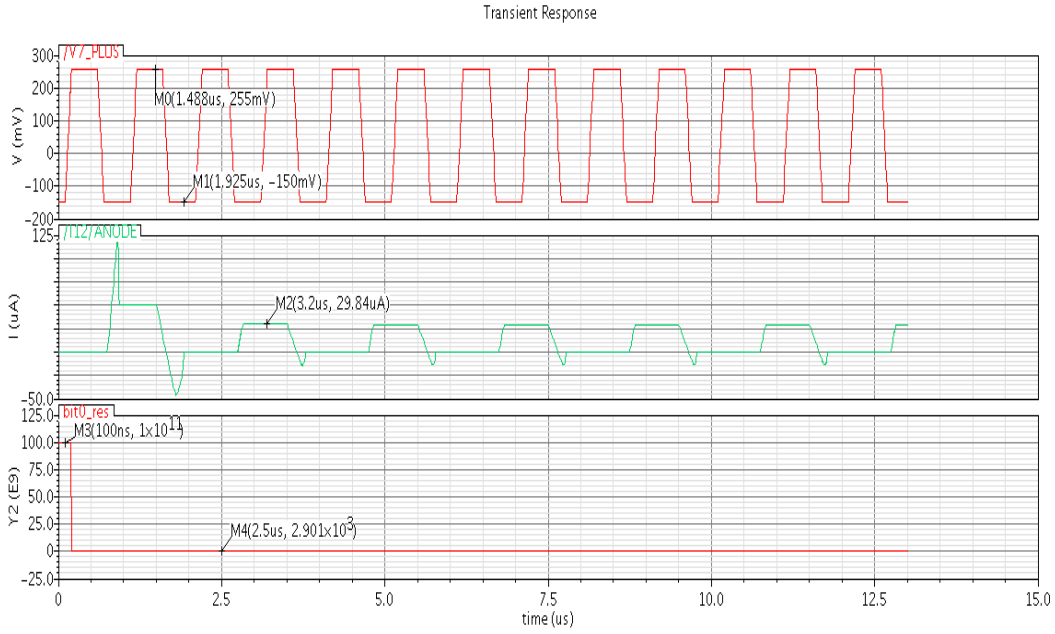


Figure 32. Waveform showing erase voltage (top) at -150mV and the current through the PMC cell limited to 50uA (middle). The cell resistance (bottom) showed proper switching to the High resistance (OFF) state as the erase voltage was set below the minimum voltage required to dissolve the conductive bridge

Effect of modifying the Erase threshold Voltage (VE):

Erase threshold voltage can also vary with temperature and hence the value for the VE parameter in the model can be modified to match the performance at a give temperature. Figure 33 and 34 show the results of a PMC model with the -150mV erase threshold. Figure 33 show successful

transition to the high resistance state with the erase voltage pulse at -151mV. Figure 34 shows no transition when the magnitude of the erase pulse was -140mV.

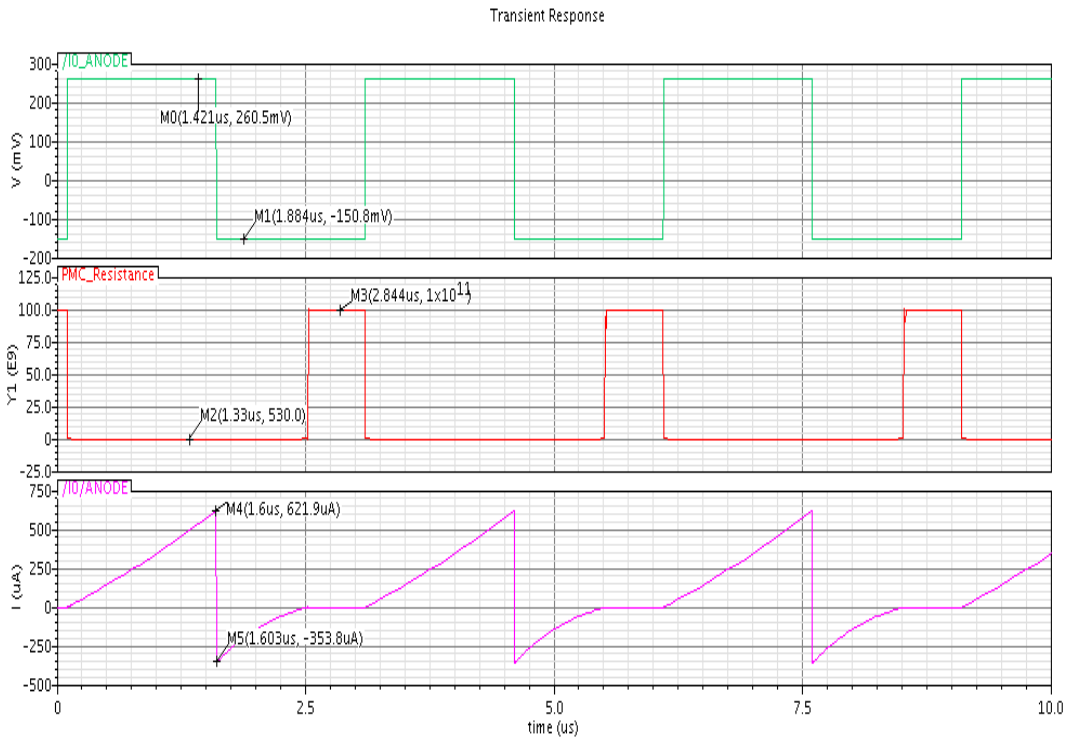


Figure 33. Waveform showing waveform showing erase voltage (top) at (-151mV) and the current through the PMC cell limited to 650uA (middle). The cell resistance (bottom) showed proper switching to the high resistance (OFF) state as the programming voltage is below the PMC model threshold of -150mV

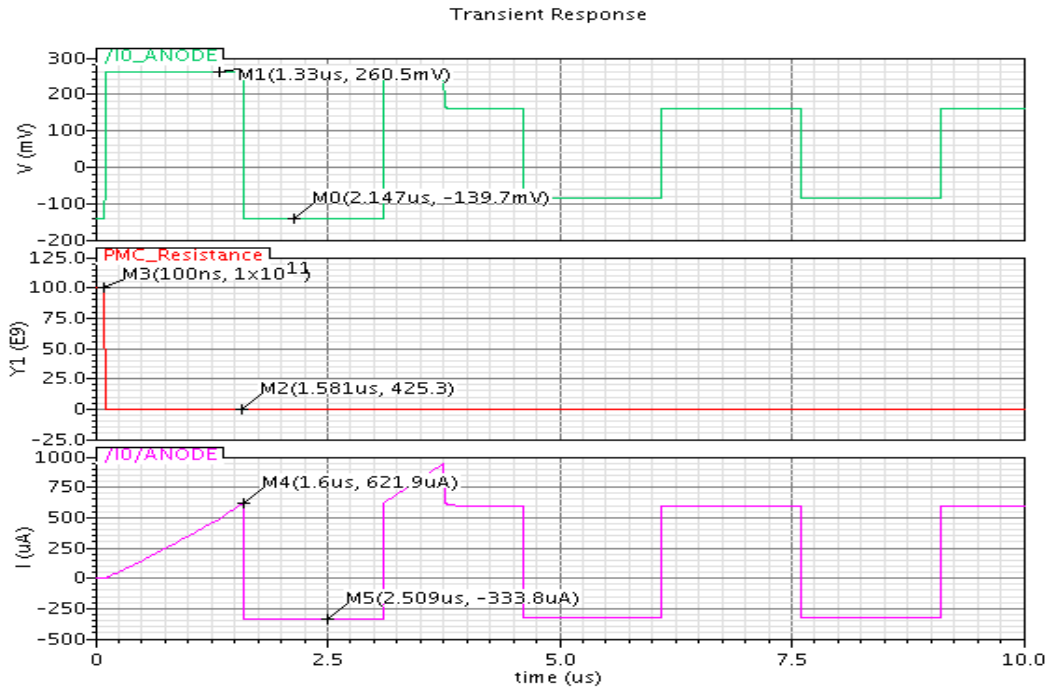


Figure 34. waveform showing waveform showing erase voltage (top) at (-140mV) and the current through the PMC cell limited to 650uA (middle).The cell resistance (bottom) showed NO switching to the high resistance (OFF) state as the erase voltage is above the PMC model threshold of -150mV

Figure 35 and 36 show the results of a PMC model with the -100mV erase threshold. Figure 33 show successful transition to the high resistance state with the erase voltage pulse at -101mV. Figure 34 shows no transition when the magnitude of the erase pulse was -99mV.

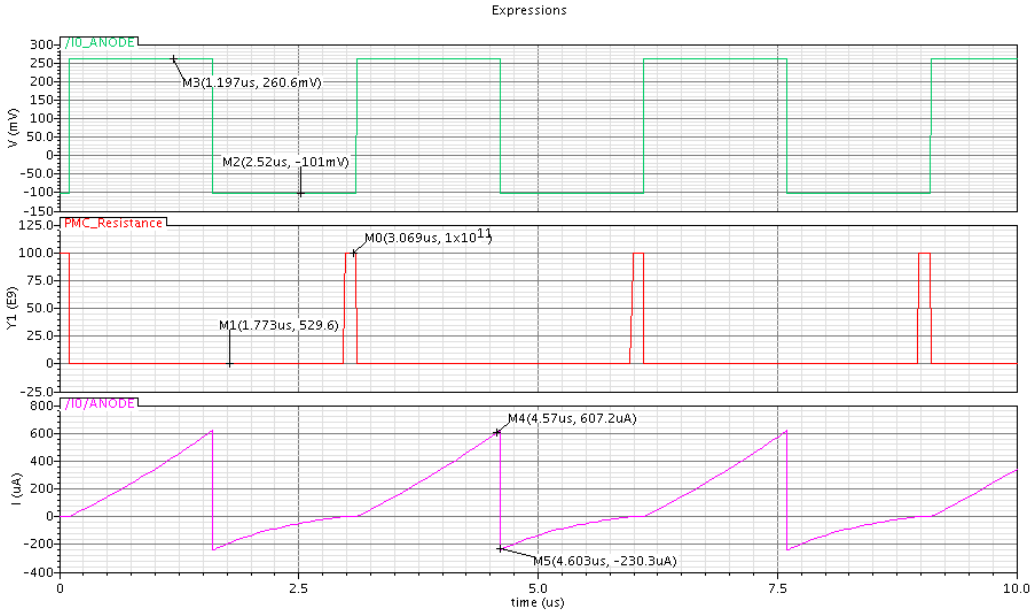


Figure 35. Waveform showing waveform showing erase voltage (top) at (-101mV) and the current through the PMC cell limited to 650uA (middle). The cell resistance (bottom) showed proper switching to the high resistance (OFF) state as the programming voltage is below the PMC model threshold of -100mV

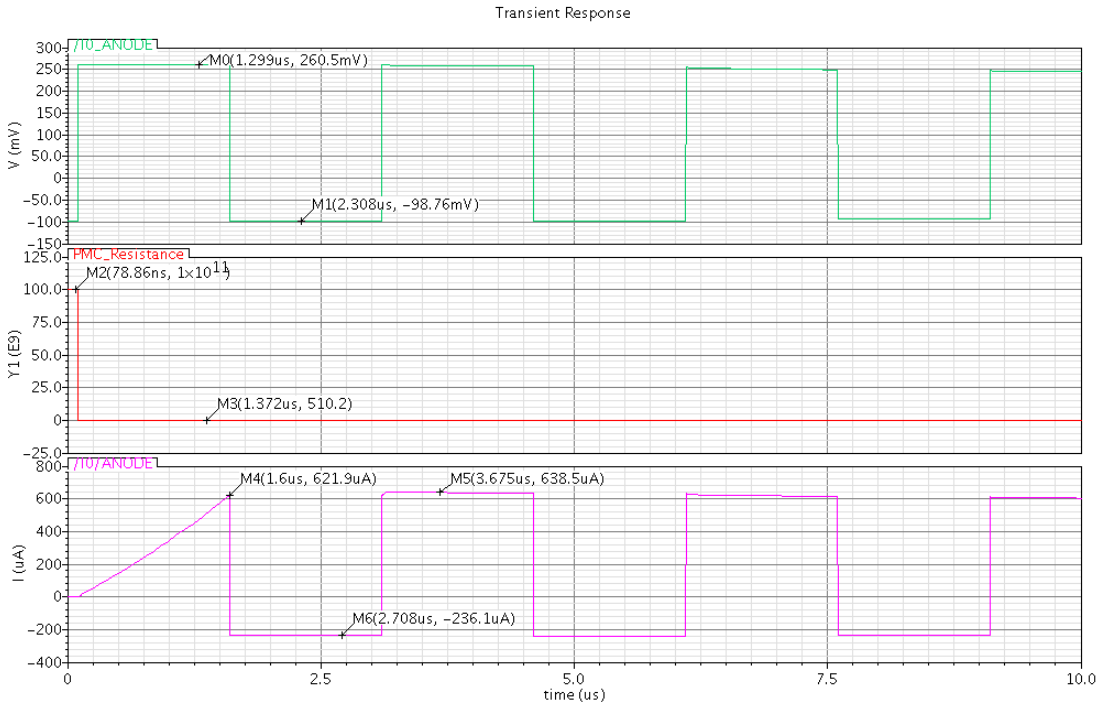


Figure 36. Waveform showing waveform showing erase voltage (top) at (-99mV) and the current through the PMC cell limited to 650uA (middle).The cell resistance (bottom) showed NO switching to the high resistance (OFF) state as the erase voltage is above the PMC model threshold of -100mV

3.5.4 OFF Resistance (ROFF) Simulation:

Another important parameter is the PMC OFF resistance. ROFF varies significantly with the change in temperature and the PMC via diameter. ROFF is reduced with the increase in temperature and the increase in via diameter [14]. To model the performance of PMC memory under different temperature conditions, the PMC model is required to allow for programming different value for the PMC maximum resistance or ROFF. It is also worth mentioning that a significant difference between ON and OFF resistance is needed for accurately detecting the PMC state without

the need for very sensitive current detection circuitry and hence very accurate modeling of ROFF is needed. Moreover, the total power consumption of the PMC memory array in dependent on the PMC resistance in both the OFF and ON states. To maximize the power benefit a very high OFF resistance in needed and hence going to a smaller diameter PMC cell benefits the total power consumption for the array. Several simulations were performed to prove that ROFF can be accurately represented in the Verilog-A model. Figure 38 show the results of a simulation of ROFF after it has been modified to 10E9 Ohm form 10E11 Ohm. The figure shows that the maximum resistance reached by the PMC is not 10E9. Figure37 shows the PMC resistance with ROFF remaining unchanged at 10E11.

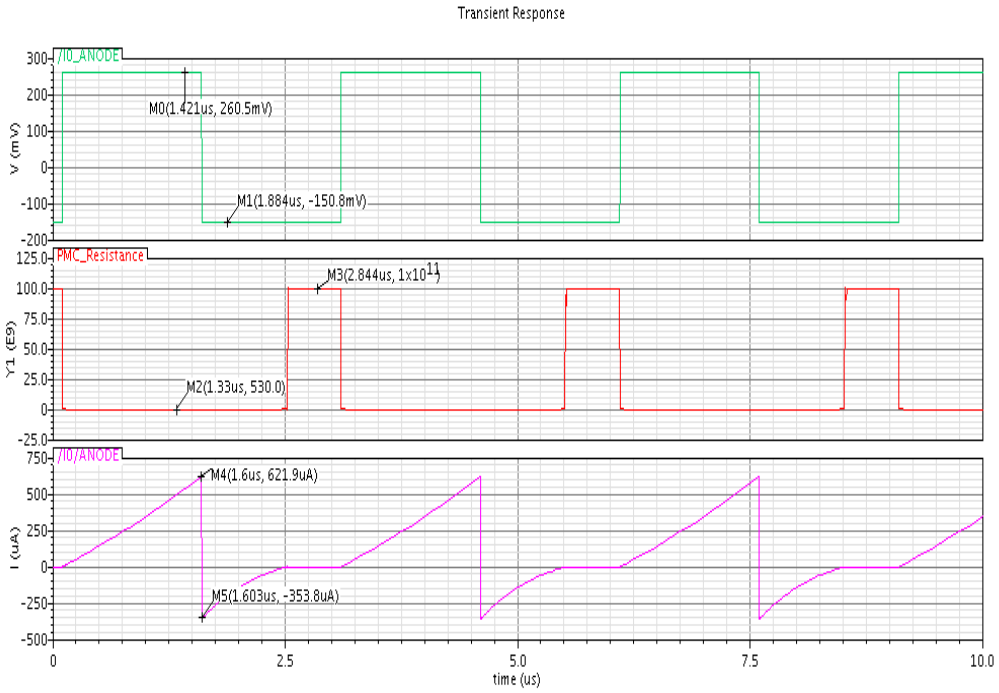


Figure 37. Waveform showing waveform showing the PMC off resistance with the model to reflecting a 10E11 OFF resistance

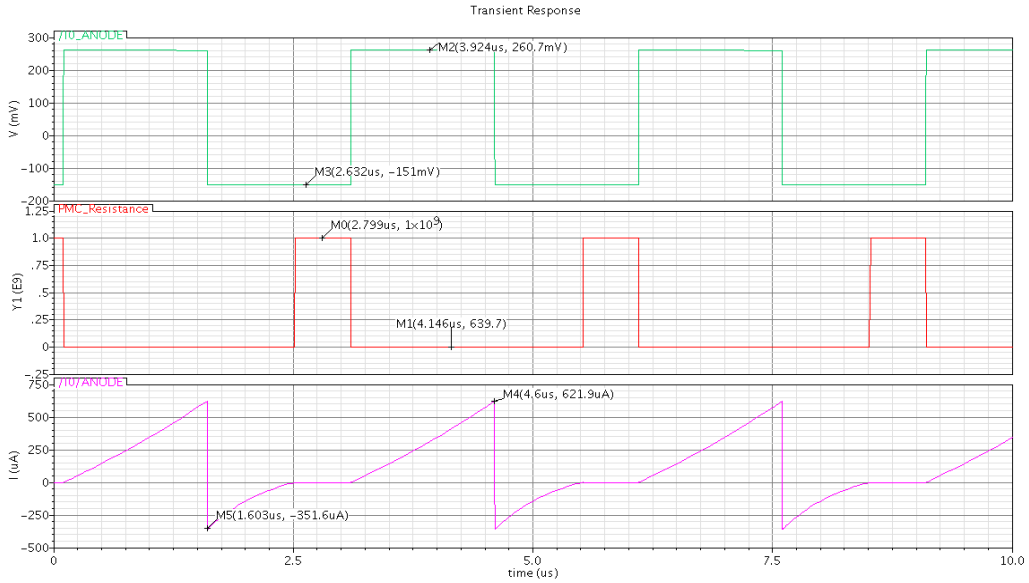


Figure 38: waveform showing waveform showing the PMC off resistance after modifying the model to reflect a 10E9 Ohm off resistance form a 10E11

Chapter 4

4 Pace Maker / Defibrillator SRAM Chip Use Model

Pacemakers are implantable medical devices that are prescribed for people whose hearts are beating too slowly or too fast or irregular. A pacemaker stimulates the heart muscle with precisely-timed discharges of electricity that cause the heart to beat in a manner quite similar to a naturally occurring heart rhythm. The pace maker consists of a pulse generator and with a battery that provides the timed electrical pulses and a pacing lead that is essentially an insolated wire carrying the electrical pulses to the heart. Newer pace makers also include monitoring circuitry

for vital biological functions such as pressure, temperature as well as position sensing using a 3D accelerometer. This information is stored in flash, EEPROM or SRAM and later communicated to a communication device that controls the programming and retrieving of data from the pacemaker referred to as the programmer. Much like a small computer, the programmer is used by the physician to externally adjust the pacemaker to meet the patient's needs; such a process is performed through telemetry using radio frequency waves.

Implanting the pacemaker requires two steps, initially the leads are inserted into the heat via guiding them through a main vein, and then the pacemaker is connected and placed under the skin in the upper chest area near the collar bone. Since inserting the device requires a surgery, pacemakers are designed to last 6-10 years without replacement depending on the stimulus pulse characteristics and the amount and data the device is set to collect and broadcast. Device longevity is an extremely important factor for a medical device, hence, a lot of time is spent in trying to design the most power efficient circuitry for a given function. However, approximately 20% of the device power is used up in memory reads and writes. Another very important factor is the size of the device. Medical pace makers can be bulky and if they are not thin enough a bump in the chest where the device is implanted can appear from the

outside. Newer pacemakers have up to 6 EEPROM chips in the system consuming a big percentage of the device area.

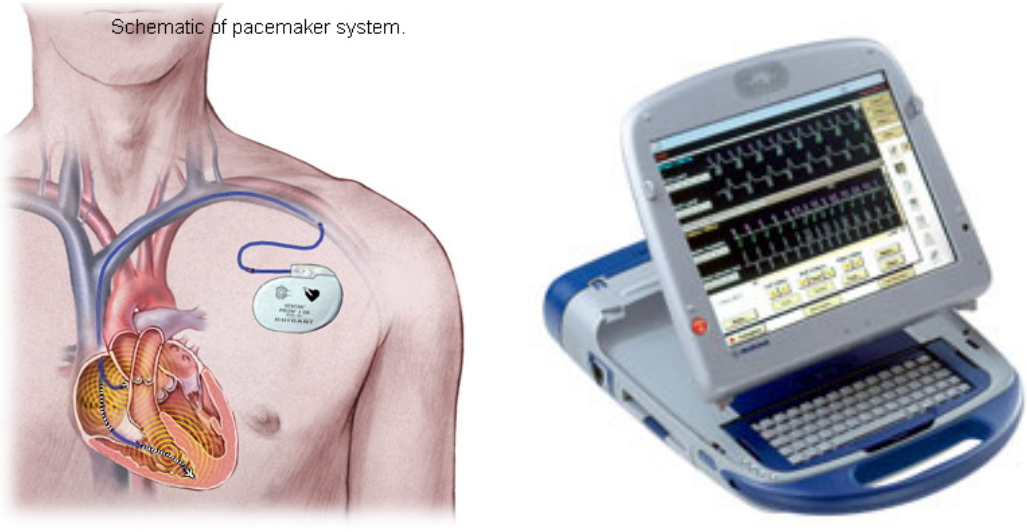


Figure 39: Showing a typical implanted pace maker (right) and a Medtronic® programmer (left) [17]

Flash was introduced recently to medical devices that conventionally used ROM as their main form of memory for Firmware and diagnostic data was typically stored in SRAM. The main drive of using flash was a twofold. First and more important, as the medical devices became more complicated, the firmware required to control them also became more complicated resulting in more risk in firmware errors. Prior to flash, an error in firmware always meant an ex-plant and implanting of new device with new ROM. This is drastic event for the patient and an extremely expensive process. Using flash or other NVM technologies would allow for

programming in field for firmware updates. The second main drive for NVM was the size factor. As more and more diagnostics were performed by the pacemaker and more data becoming required to store, area extensive SRAM chips became less appealing.

It is reasonable to assume 500,000 8bit memory accesses per day for a pacemaker running diagnostics. Although this number may vary greatly depending on the pacemaker setting it is reasonable average to go by. For these conditions a pacemaker using a 0.13um TSMC 32Mbit SRAM will consume approximately 800 nA of total current drain. For a FLASH with TSMC 0.25 um process chip with a 32Mbit word and 512 byte sector size the 500,000 access will equate to 125,000 write and 975 erase cycle reflecting a daily current drain average of 3uA from a 3.2V battery which equates to **9.6 micro-watts of power consumption.**

Chapter 5

5 PMC Memory Array Model

To simulate the behavior and power consumption of a PMC memory array, an 8bitx1 array was constructed. The PMC model described in chapter 3 was connected into array architecture.

5.1 PMC Array Model Design:

In this architecture each PMC is connected to a bit line through an ideal switch. A Verilog-A model of an ideal switch was used in the array model. When a defined voltage is reached (e.g. 1.4 V) the switch will have a zero resistance. When voltage on the switch is less that the defined voltage, the switch will have infinite resistance. The ideal switch is controlled by a word line allowing current trough the current limiter model to the PMC when its corresponding word is being accessed. Each word line is selected by raising the word line voltage to the ideal switch voltage (in this case 1.4V). Figure 40 shows the 8x1bit array. A one byte implementation is an adequate demonstration for this implementation for simulation purposes. However, a larger memory array is constructed by adding word lines, switches, and PMCs in the same construct.

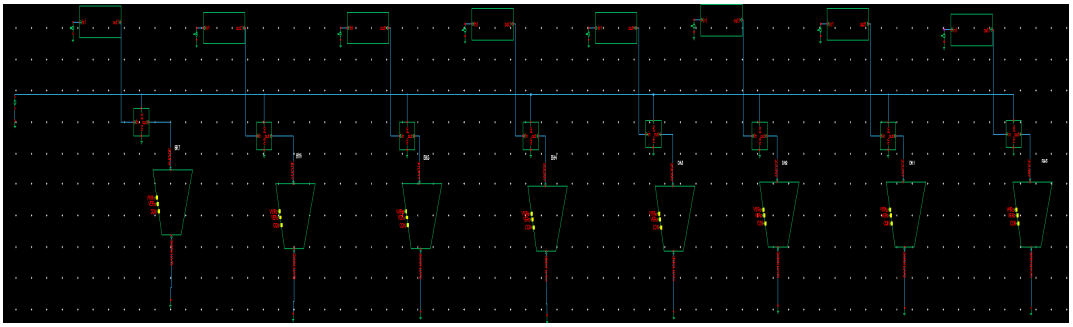


Figure 40. Showing an 8bit x1 PMC memory array

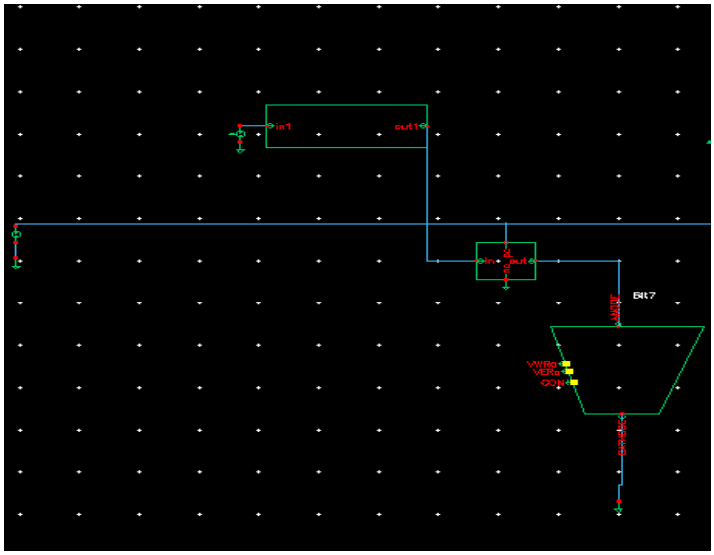


Figure 41. Showing a single PMC cell in the array connected to voltage source through a current limiter and an ideal switch model

Other than the selection switches and word lines, the read and write operation is identical to that described in chapter 3 where a voltage source is used to provide the program/erase pulse is connected in series with a current limiter to limit the current. The current limiter described in Appendix B is a variable resistance that increases in resistance when the current exceed the programmable limit in the model resulting in

attenuating the current to the maximum current (IMAX) parameter in the current limiter model. When the current is less that IMAX the current limiter will have a low resistance of 1Ohm. This configuration assumes that no additional bits are required for error correction code (ECC). If additional ECC bits are needed the model can easily be modified by appending each row of bits with the ECC bits each connected to a bit line and supply. This PMC architecture provides a simple, yet efficient way to connect programmable metallization cells using a minimum number of current limiters and with minimized connections.

5.2 PMC Array Model Simulation Results:

A critical parameter in the array performance is the word selection mechanism. In the array model, each byte is selected using a word line that is connected to a voltage source through a switch model. Once the voltage exceeds a predetermined voltage that is plugged in the switch model, the switch resistance decreases to zero allowing the program and erase of PMC cells through the bit lines that is connected in series to a current limiter and the pulse generator. To insure proper word selection the simulation was performed to demonstrate the word selection operation. The switch model was programmed to open when the voltage across the switch (the word line voltage) exceeds 1V. This assumes that the word line will be supplied from the digital regulated voltage of 1.4V. A

guard band of 400mV was added to allow the switch to operate with battery at end of life or when noises exist on the word line.

The word line voltage range was assumed to be 1.05V to 1.4V. Both maximum and minimum voltage was simulated by setting the word line voltage source to 1.05V and 1.4V respectively then applying a program and erase pulses on bit lines while measuring the change in the PMC cell resistance on each bit line. The PMC resistance was named BIT0 – BIT7 resistance depending on which bit line it is connected to. Figure 42 and 43 show the PMC cell resistance for all bits when the word line is set to 1.4V and 1.05V respectively. The word line voltage was plotted on the top section. The program and erase voltage which is identical for all 8 bit lines was printed on the middle plot section while the PMC resistance for all 8 bits in the last section. All 8 bits showed identical performance and adequate program and erase. To ensure the robustness of the bit selection mechanism a simulation was generated with the word line voltage below the 1V minimum, namely 990mV while applying the same program and erase stimulus on bit lines. With the word line voltage below the 1V limit, the PMC resistance for all 8 bits remained unchanged as shown in figure 44.

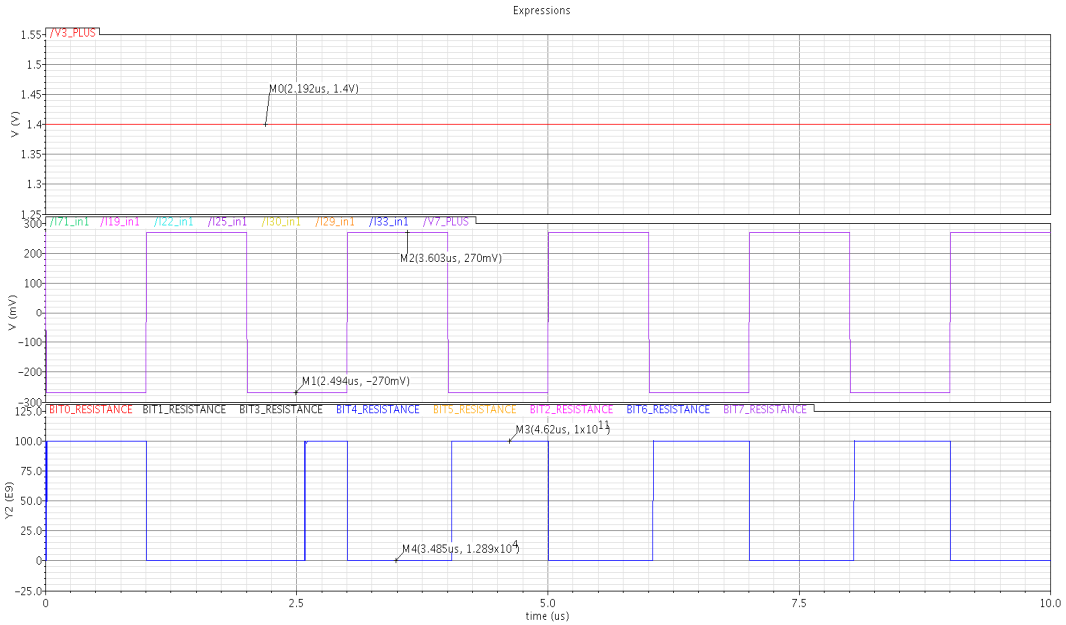


Figure 42. Showing word line voltage (top) set to 1.4v, program/erase pulse for all 8 bit lines combined (middle), and the PMC change in PMC resistance for all 8 bits (bottom) bit line resistances can be programmed when word line resistance is above the 1v threshold for the switches.

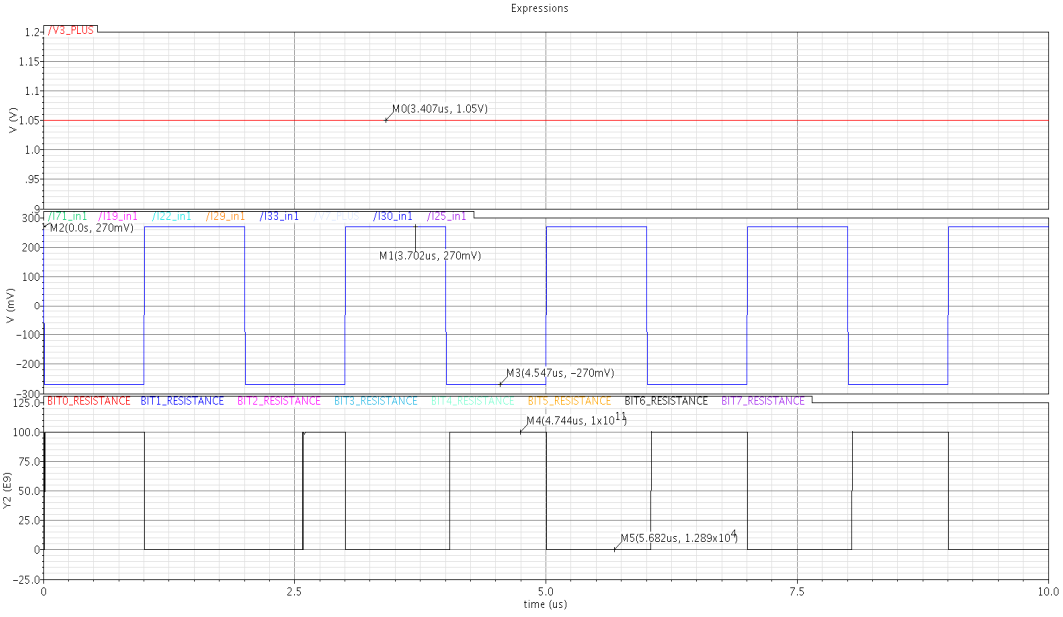


Figure 43. Showing word line voltage (top) set to 1.4v, program/erase pulse for all 8 bit lines combined (middle), and the PMC change in PMC

resistance for all 8 bits (bottom). Bit line resistances can be programmed when word line resistance is above the 1v threshold for the switches.

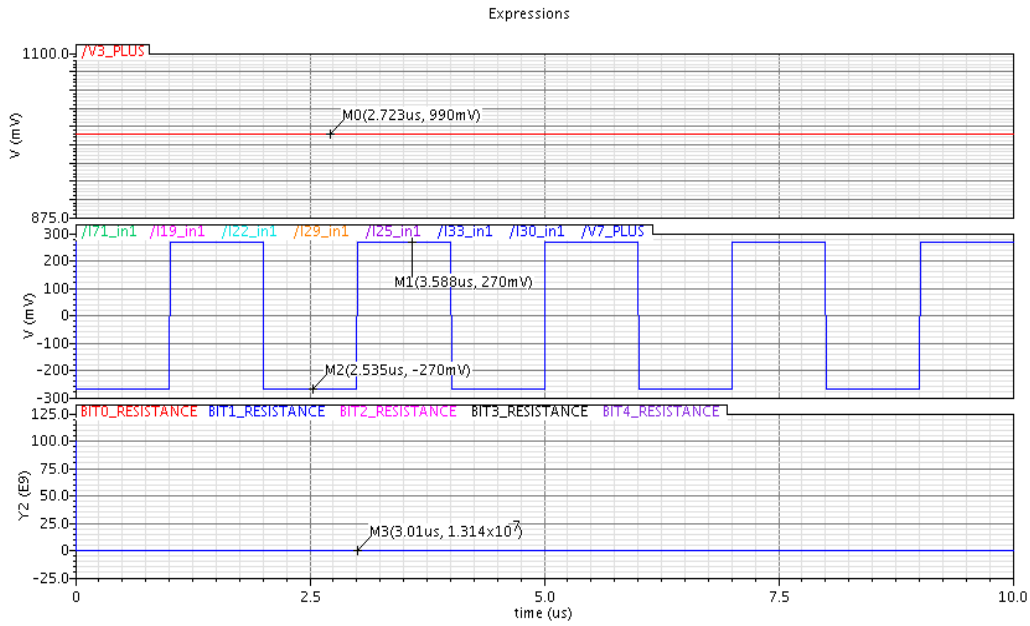


Figure 44. Showing word line voltage (top) set to 1.4v, program/erase pulse for all 8 bit lines combined (middle), and the PMC change in PMC resistance for all 8 bits (bottom). Bit line resistance remains unchanged when word line resistance is below the 1v threshold for the switches

5.3 Program/Erase Voltage and current limit Selection:

Write and erase threshold voltages, ON and OFF resistances as well as gain terms are all intrinsic characteristic of the device. Actual data from literature were used to optimize these parameters for a PMC of certain via diameter under nominal conditions. It has already been demonstrated that the model can be modified or fine tuned if the PMC physical area or operating conditions change or to embed a guard band for the PMC performance.

The main objective of this project is to minimize the power consumed by the NVM memory in a medical device and hence careful analysis was performed to choose the best setting for the current limit as well as the program and erase pulse duration and magnitude.

It makes practical sense to fix the pulse duration for both program and erase to the minimum clock cycle of the device. Since medical devices do not operate their digital at a much slower speed when compared to other industries such as cell phones of personal computers, a 1MHz clock is good estimate of the maximum operation speed for medical devices. Given that current devices operate at 100 KHz, this estimate factors in advances in algorithms for the next decade. With that in mind a program and erase cycle was set to 2 us.

After determining the pulse duration, the model can be used to determine the minimum current limit at which the PMC is programmed and erased successfully. This will he define the minimum current consumed by each cell. From the model, a minimum voltage of 0.25V is required to start the program operation while a -100mV is needed to initiate the erase process. Given the minimum voltages a 0.26V was selected as a starting point for the program pulse while -110mV was chosen for the erase pulse to be the starting point of the supply setting. Even though the supply can provide theses pulses for the program and erase, the current limiter defines the actual voltage on the PMC anode. As a starting point the

current limiter was set to 150uA and the output was logged in figure 45. The figure shows the word line selection voltage at 1.4V to allow the program and erase of the PMC. The second graph shows the program and erase pulse with 260mV program voltage and 110mV erase voltage. The PMC current input is shown on the third plot which is also the current limiter output. The plot shows the current limiter limiting the input current to the PMC to 50uA. With the current limit changed to 100uA the same behavior was observed as shown in figure 46. Since the current limiter is basically a variable resistance that changes resistance to attenuate the current when is exceeds the current limit, it reduces the actual resistance on the PMC anode by (current limiter resistance X current through current limiter). Figure 45 shows that the resulting voltage on the PMC anode is not enough to cause it to switch resistance from high to low and hence stronger erase voltage is needed. The erase voltage was increase to -260mV to match the program voltage. Even though a lower setting would have been sufficient, making the program and erase pulses the same magnitude but opposite in bias direction simplifies the program and erase circuitry. Figure 47 shows the word line select bit at 1.4V in the first plot as well as the modified program and erase in the second plot. The third plot shows the PMC current showing the first erase and program cycle successfully executed with the current limited to100uA. The fourth plot show sufficient voltage is exerted on the PMC anode for program and

erase. The last plot shows the change in PMC resistance, notice that due to the current limit, weak programming is noticed in subsequent with the ON resistance being approximately 40KOhm. The program and erase parameters of 260mV and -260mV respectively with a current limit of 100uA was chosen as an adequate setting to model the power consumed by the PMC device.

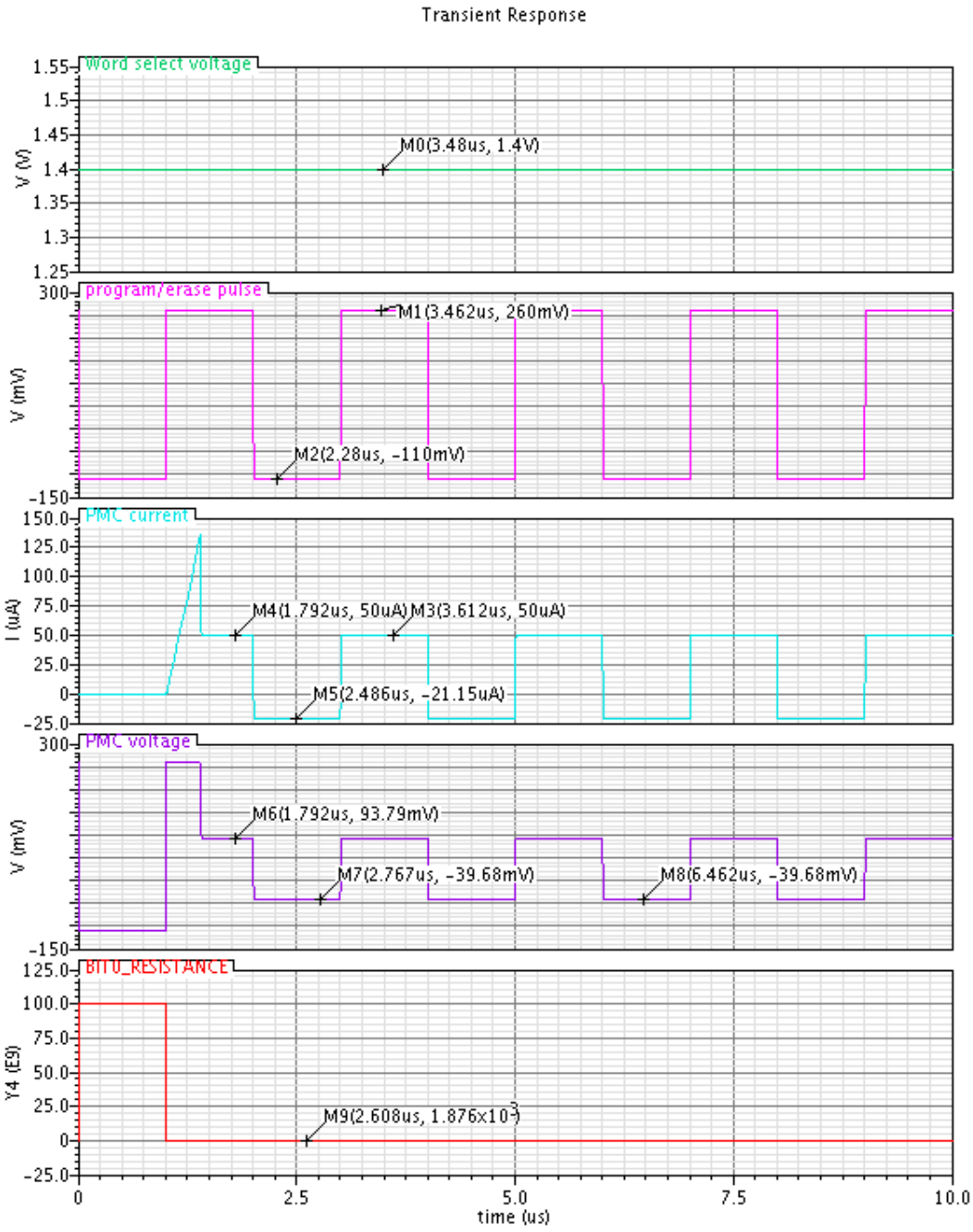


Figure 45. Showing word line voltage (top) set to 1.4v, program/erase pulse for bit0 (middle), and the PMC change in PMC resistance for bit0 (bottom). PMC input current limited to 50ua.Current limit setting resulting in insufficient voltage on the PMC anode

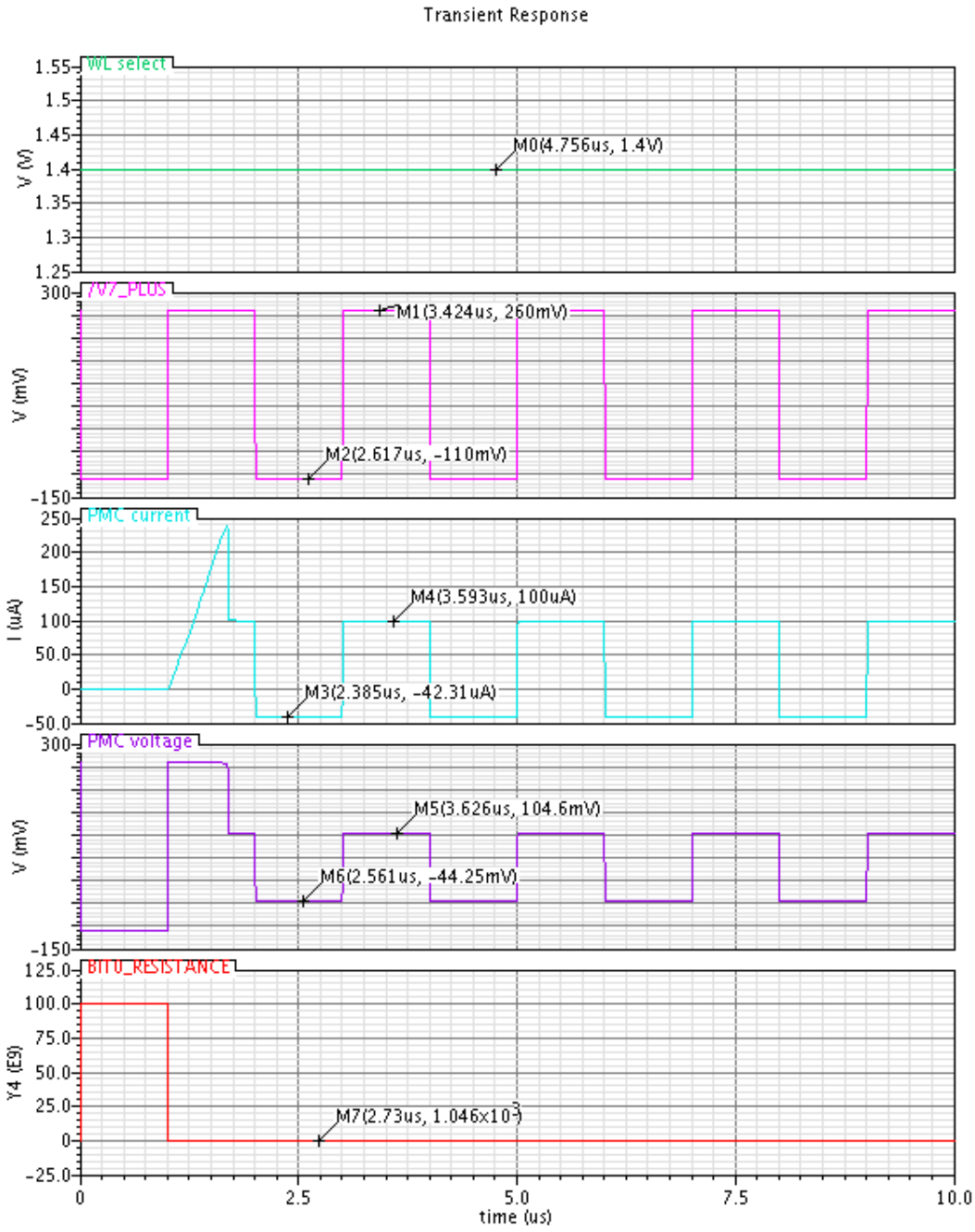


Figure 46. Showing word line voltage (top) set to 1.4v, program/erase pulse for bit0 (middle), and the PMC change in PMC resistance for bit0 (bottom). PMC input current limited to 100ua.current limit setting resulting in insufficient voltage on the PMC anode

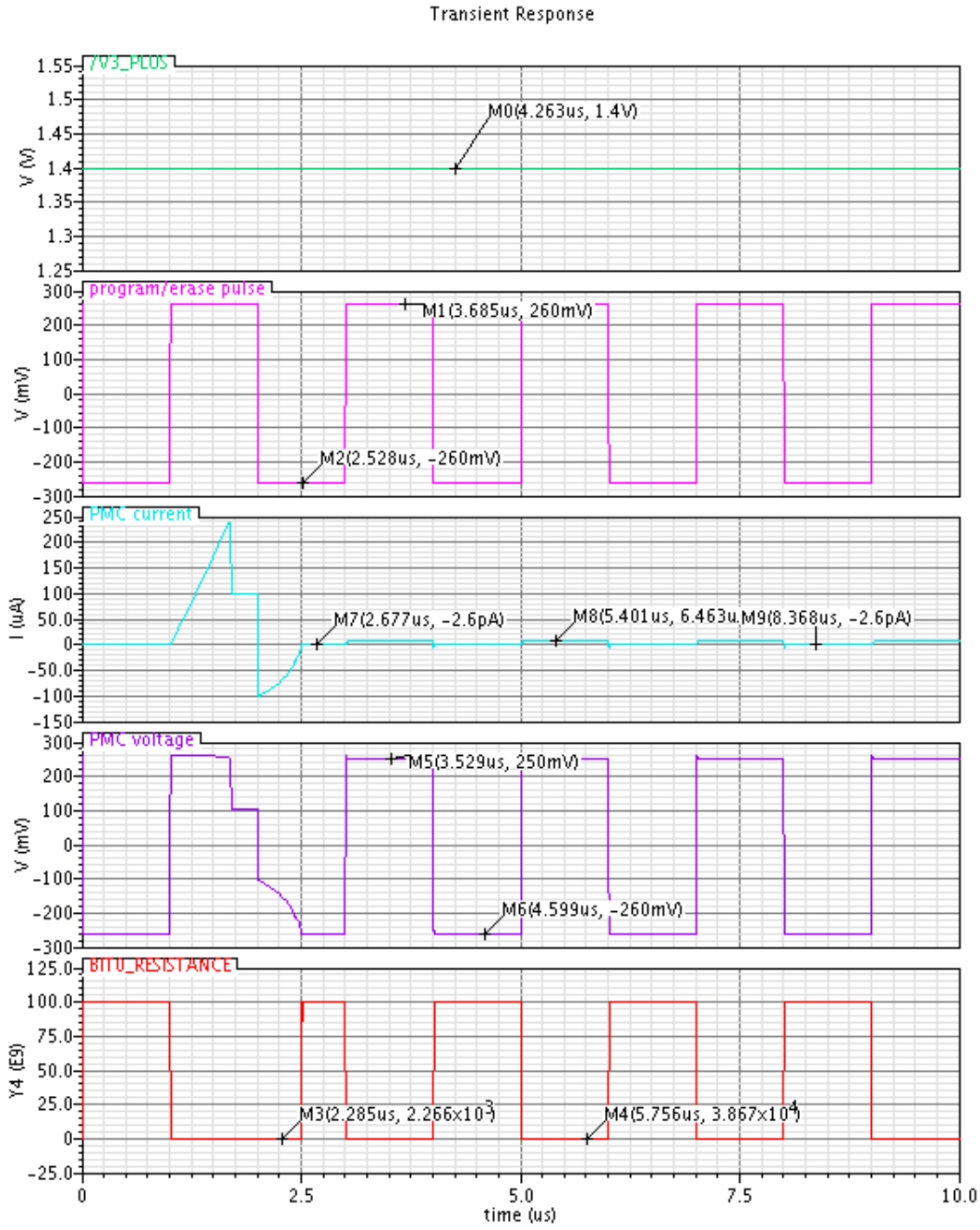


Figure 47. Showing word line voltage (top) set to 1.4v, program/erase pulse for bit0 (middle), and the PMC change in PMC resistance for bit0

(bottom). PMC input current limited to 100ua. Stronger erase resulted in adequate switching

5.4 Current limit effect on ON resistance:

The next simulation was designed to study the effect of limiting the current on the PMC ON resistance. Studying the effect of current limiting on the switching resistance is needed to determine the sensing circuitry needed to detect the state of the PMC as it is a function of the difference between the ON and OFF resistances. Simulating the effect of current limiting can also be used to study the feasibility of multi-bit storage as explained in detail in section 2.6.

Holding the WL voltage at 1.4V to allow the program and erase pulse to the PMC and maintaining the program and erase pulses at 260mV and -260mV respectively as shown in the second plot of figure 48 and 49. For the first simulation the current limit was set to 100uA as shown in figure 48. The resulting ON resistance was measured to be 2.3Kohm for the fist program and approximately 38KOhm for subsequent program cycles as shown in figure 48 in the last plot. When the current limit was increased to 400uA as shown in figure 49 the resulting ON resistance was close to 700 Ohms much lower than that in the first simulation.

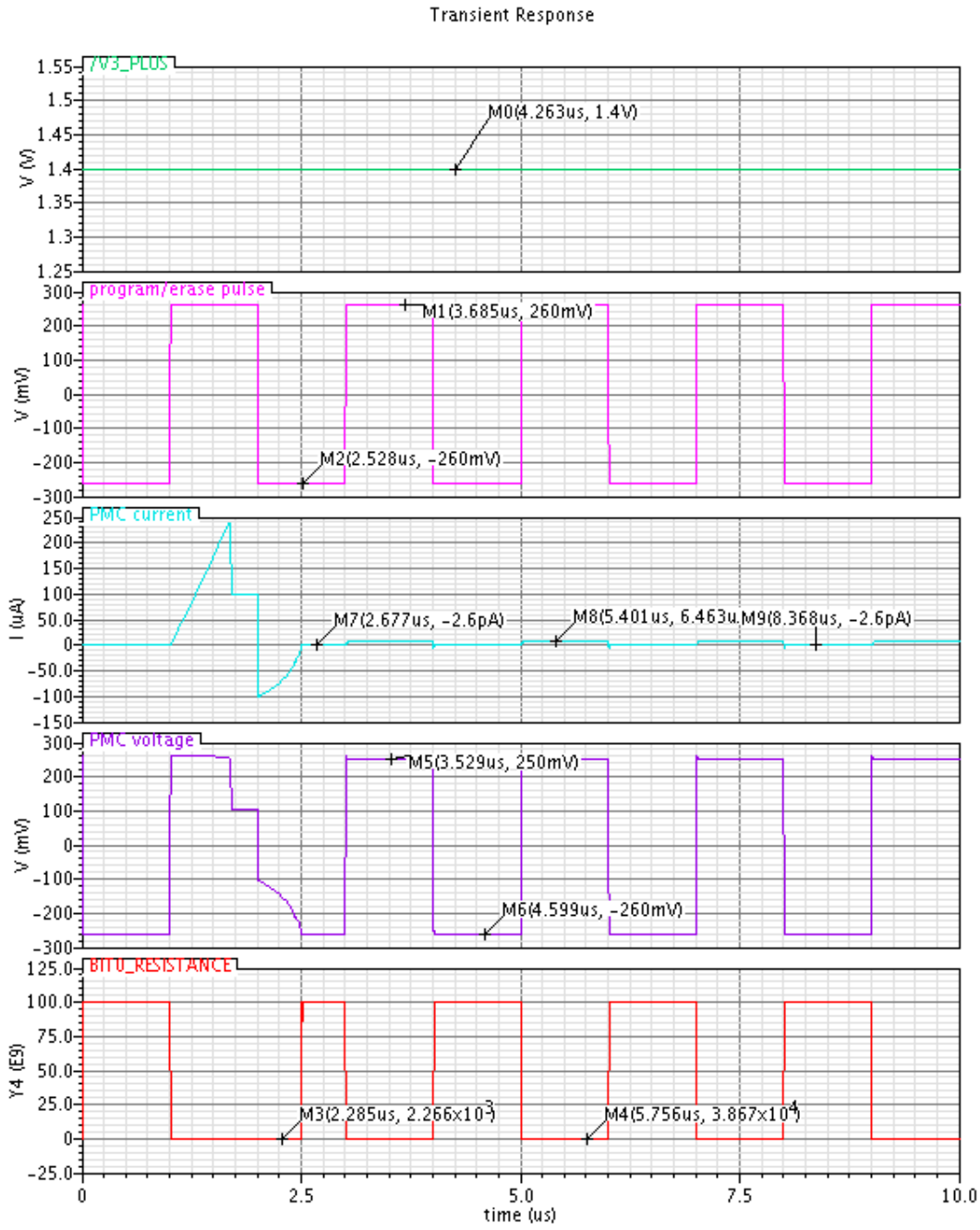


Figure 48. Showing word line voltage (top) set to 1.4v, program/erase pulse for bit0 (middle), and the PMC change in PMC resistance for bit0 (bottom). PMC input current limited to 100ua. Resulting RON is in the 38kohm range

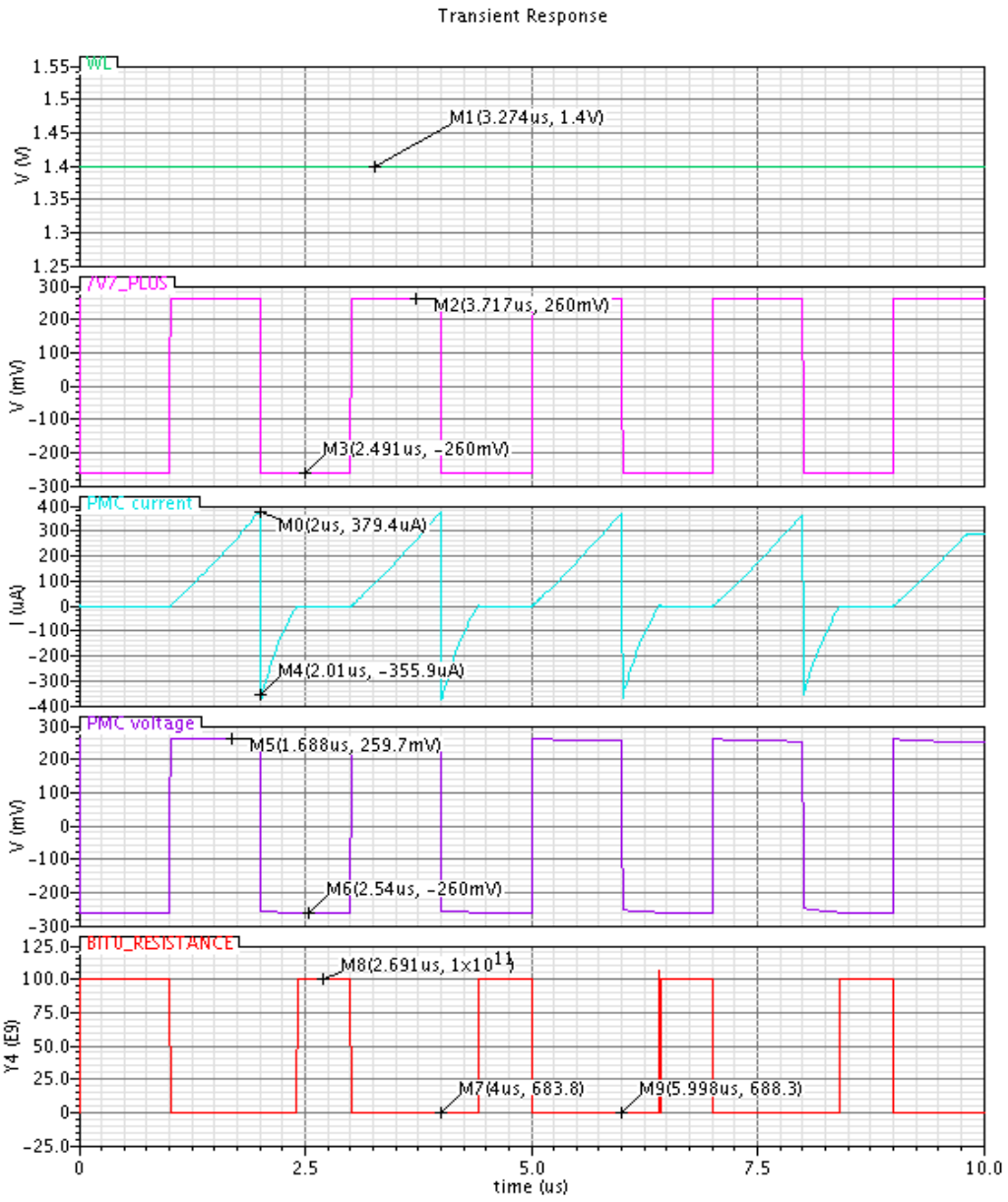


Figure 49. Showing word line voltage (top) set to 1.4v, program/erase pulse for bit0 (middle), and the PMC change in PMC resistance for bit0 (bottom). PMC input current limited to 400ua. Resulting RON is approximately 700 ohms

5.5 PMC Array Model Data Analysis:

The above described model was used to simulate average power consumption for write and erase. The program and erase parameters of 260mV and -260mV respectively with a current limit of 100uA was chosen as an adequate setting to model the power consumed by the PMC device. Simulations showed an average power consumption of 4.16 uWatts in back to back write and erase cycles. Using the usage assumption in chapter 5 of 500,000 accesses which in case of PMC memory can equate to 250,000 writes and 250,000 erases for a small array memory, and using the modeled erase and write cycle duration of 1 ns for write and 1ns for erase, a simple calculation shows the active daily use of the PMC array to be 5.7×10^{-6} %. This corresponds to an average daily power consumption of 4.16 uWatts X 5.7×10^{-6} which equates to 2.4×10^{-11} Watts. When compared to flash, the PMC array consumes $(2.4 \times 10^{-11}) / (9.6 \times 10^{-6})$ or 0.00025 %.

Chapter 6

6 Conclusion

The medical devices industry have expanded greatly in the past decade to address many diseases that were hard to control using conventional therapies especially in the fields of neurological, diabetes, pain management and heart rhythm diseases. Electronic devices have proven very effective in modulating and correcting neurological function to address electro-physiological disorders. A major concern on the use of medical devices is the limited longevity of the device due to battery lifetime. Since medical devices require a surgery to be implanted, a lot of resources and investments are focused in ways to increase battery longevity. One way to achieve this goal is minimize the power consumption of electronic circuits, in specific memory circuit.

Medical devices are now equipped with diagnostic sensors that can record parameters such as pressure, temperature, heart rate, posture etc. and store in electronic memory to detect disorder symptoms and alter its therapy accordingly or store the data for the physicians to review. This activity results in about 15% of the total power consumed by the device. The large percentage of power consumption and the major advance in memory technologies made looking for a new non-volatile memory an obvious way to increase device longevity. Given

the current lifetime of a medical device of little less than 8 years, reducing the 15% memory power consumption to a minimum saves the patient from the need to replace the medical device for another year of more.

This goal of this study was find an alternative technology to replace the current single bit Flash technology NVM in medical devices that can reduce help reduce the device power consumption and size while maintaining the same reliability measures as Flash. The research provided a thorough summary of all new non-volatile memory technologies that were deemed as possible candidates for use in a medical device. After careful review of the literature on each technology, the conductive bridge memory technology (CBRAM/PMC) has proven to be among the leading and most reliable memory technologies that are suitable for use in medical devices followed closely by FeRAM. PMC has an advantage over flash and other charge storage memory technologies as they are very compatible with sub-threshold operating devices. Moreover, PMC technology surpasses flash in, area, read/write access time, date retention and power. Medical devices operate in a narrow temperature range which mitigates any concerns about PMC operation at high temperatures.

After selecting the memory technology a Verilog-A behavioral model was used to simulate the memory operation and to construct a

design for the memory array to prove the feasibility of use in a medical device and to demonstrate the technology performance.

Simulation data showed PMC memory power consumption that is orders of magnitude lower that power numbers obtained by testing existing chips with embedded Flash. Data obtained from the memory array simulations showed that using PMC memory technology would reduce the 15% total device power used by flash memory to less that 1% resulting in an increase of more than a year in medical device longevity. A review on literature on PMC technology and Flash memory showed an area advantage of using PMC memory due to its high scalability and the elimination of high voltage circuitry. It also showed that PMC memory exceed or match all reliability, data-retention, temperature requirement for use in medical devices.

REFERENCES

[1] M.N. Kozicki, C. Gopalan, M. Balakrishnan, M. Park, and M. Mitkova, “Non-volatile memory based on solid electrolytes,” Proceedings of the 2004 Non-Volatile Memory Technology Symposium, 10-17, Orlando, Florida, November, 2004.

[2] M.N. Kozicki, M. Park, and M. Mitkova, “Nanoscale memory elements based on solid state electrolytes,” IEEE Trans. Nanotechnology, vol. 4, no. 3, 331-338 (2005).

[3] Kozicki, M.N.; Balakrishnan, M.; Gopalan, C.; Ratnakumar, C.; Mitkova, M., "Programmable metallization cell memory based on Ag-Ge-S and Cu-Ge-S solid electrolytes," Non-Volatile Memory Technology Symposium, 2005 , vol., no., pp. 7 pp.-, 7-10 Nov. 2005.

[4] M.N. Kozicki, M. Balakrishnan, C. Thermadam, M. Mitkova, “A low power non-volatile switching element based on copper in Deposited Silicom Oxide.

[5] M.N. Kozicki, M. Park, M. Mitkova, “A low power non-volatile switching element based on copper-tungsten oxide solid electrolyte,” IEEE Transactions on Nanotechnology 4, 331-338 (2005).

[6] C. Schindler, M. N. Kozicki, “Resistive Switching in Ag-Ge-Se with extremely Low Write Current .”

[7] N. E. Gilbert, M. N. Kozicki, “An Embeddable Multilevel-Cell Solid Electrolyte Memory Array.” IEEE Journal of solid state circuits. VOL. .42, No.6, June 2007.

[8] N. E. Gilbert, C. Goplan, M. N. Kozicki, “A macro model of programmable metallization cell devices.”

[9] D. kamalanathan, S. Baliga , S. C. Thermadam, M. N. Kozicki, “ON state stability of PMC.”

[10] http://www.itrs.net/Links/2007ITRS/2007_Chapters/2007_ERD.pdf

[11] G. Müller, T. Happ, M. Kund, G.Y. Lee, N. Nagel, and R. Sezi. “Status and outlook of emerging nonvolatile memory technologies,” IEDM Technical Digest, 567-570, (2004).

[12] http://www.ramtron.com/files/tech_papers/Ferro_Tech_Brief.pdf

[13]http://everspin.com/documents.php?pn=MR4A08BCMA35&hjk=8&a1f3=16Mb&a=No

[14] M. Kund, G. Beitel, C. Pinnow, T. Rohr, J. Schumann, R. Symanczyk, K. Ufert, G. Muller “Conductive bridging RAM (CBRAM): an emerging memory technology scallable to sub 20nm.”

[15] R. Symanczyk, R. Bruchhaus. R. Dittrich, M. Kund “Investigation of the Reliability Behavior of Conductive-Bridging Memory Cells.”

[16]Non-volatile memory (2010).Retrieved March 2010, from http://en.wikipedia.org/wiki/Non-volatile_memory

[17] http://www.heise.de/bilder/97895/0/0

[18] www.washingtonhra.com/21.html

[19] http://www.web-feetresearch.com/Latest%20Research%20%20TOCs/TOC%20-%20SDS450EFD-28%20-%20Embedded%20Flash%20Drives_2008-2012.pdf

APPENDIX A

PMC VERILOG A MODEL

Disclaimer: the following Code for the PMC Verilog-A model was programmed by Nad Gilbert.

Verilog A model:

```
// VerilogA for latest_pmc_8_2009, PMC_MEMORY_CELL, veriloga

`include "constants.vams"
`include "disciplines.vams"


module PMC_MEMORY_CELL (ANODE, CATHODE, CON, VWRa, VERa);
  inout ANODE, CATHODE, CON, VWRa, VERa;

  electrical ANODE, CATHODE;

  electrical CON, VWRa, VERa;

//Write Threshold Parameters
  parameter real VTH1  = 0.25;   //
  parameter real RW1ON = 100k;   //
  parameter real VTH2  = 0.125;
  parameter real RW2ON = 1e6;
  parameter real WVOV  = 0.9;

//Erase Threshold Parameters
  parameter real VE    = -0.1;
  parameter real EVOV  = -0.6;
  parameter real REON  = 200k;

//Resistance IC and Final
  parameter real ROFF  = 1e11;  // resistance of the PMC memory
element in the off stage
  parameter real RPMCS = 1e11;  // resistance of the PMC memory
element in the off stage
  parameter real RMIN  = 100;

//Capacitance Values
  parameter real CED   = 1e-15;
  parameter real CPMCS = 1e-14;

//Integration gain values
  parameter real GIW1  = 1e6;
  parameter real GIW2  = 1;
  parameter real GWV   = 5e3;
  parameter real GWOV  = 1e6;
  parameter real GIE   = 1e7;
  parameter real GVE   = 8e3;
  parameter real GEOV  = 3e4;

//Output Slew Limiting Essentially the AN and CA Capacitance
  parameter real SLP   = 1e9;
  parameter real SLN   = -1e9;

  real RPMC, CPMC, VPMC, IPMC, VWR, VER, RCON;
  integer WI1, WI2, WV, WOV, EI, EV, EOV, RST;
```

```
  analog
  begin
  @(initial_step)
   begin
     CPMC = CPMCS;
     RCON = (ROFF-RPMCS)/(ROFF*RPMCS);
     WI1 = 0;
     WI2 = 0;
     WV  = 0;
     WOV = 0;
     EI  = 0;
     EV  = 0;
     EOV = 0;
     RST = 0;
   end

  RCON = (ROFF-RPMCS)/(ROFF*RPMCS);

  VPMC = V(ANODE, CATHODE);
  IPMC = I(ANODE, CATHODE);
//Programming Conditions
    if ((VPMC > VTH2) && (RPMC > RMIN) && (RPMC < RW2ON)) WI2 =
1;
    else WI2 = 0;
    if ((VPMC > VTH1) && (RPMC > RMIN) && (RPMC < RW1ON)) WI1 =
1;
    else WI1 = 0;
    if ((VPMC > VTH1) && (RPMC > RMIN)) WV = 1;
    else WV = 0;
    if ((VPMC > WVOV) && (RPMC > RMIN)) WOV = 1;
    else WOV = 0;
    if ((VPMC < VE) && (RPMC < ROFF)) EV = 1;
    else EV = 0;
    if ((VPMC < VE) && (RPMC < REON) ) EI = 1;
    else EI = 0;
    if ((VPMC < EVOV) && (RPMC < ROFF)) EOV = 1;
    else EOV = 0;
//Force Control Voltage to zero volts in erase conditions
    if ((V(CON) < 0) && (VPMC < VE)) begin
    RST = 1;
    RCON = 0;
    end
    else RST = 0;

  //Set integration values for Control Voltage
  VWR = WI1*GIW1*abs(IPMC) + WI2*GIW2*abs(IPMC) +
WV*GWV*abs(VPMC) + WOV*GWOV*abs(VPMC);
  VER = EI*GIE*abs(IPMC) + EV*GVE*abs(VPMC) + EOV*GEOV*abs(VPMC);
   // VWR = WI1*GIW1 + WI2*GIW2 + WV*GWV + WOV*GWOV;
   // VER = EI*GIE + EV*GVE + EOV*GEOV;
  V(VWRa) <+ slew(VWR,1e12,1e12);
  V(VERa) <+ slew(VER,1e12,1e12);
```

```
  //Control Voltage
  V(CON) <+ idt(V(VWRa,VERa)*1, RCON, RST);
  RPMC = ROFF/(ROFF*V(CON)+1);
  I(ANODE, CATHODE) <+ slew(V(ANODE, CATHODE)/RPMC,SLP,SLN);

  end

endmodule
```

APPENDIX B

CURRENT LIMITER AND SWITCH VERILOG A MODELS

Current Limiter Model:

```
// VerilogA for latest_pmc_8_2009, currentlim, veriloga

`include "constants.vams"
`include "disciplines.vams"

module currentlim (in1 , out1 );

 inout in1 , out1 ;
 electrical in1 , out1 ;


//maximum current parameter
parameter real IMAX = 50u ;

 // parameter real Rlim = 1 ;


real VLIM , ILIM , RLIM ;
 analog
   begin

@(initial_step )
RLIM =  1 ;

 I(in1, out1 ) <+ V(in1, out1 )/RLIM   ;

  if ( I(in1, out1 ) > IMAX )

     begin
     RLIM = V(in1, out1 )/ IMAX  ;
     end


  else if (I(in1, out1) < -IMAX)
   begin
      RLIM = V(in1, out1)/IMAX ;
      end

  else

   begin

    RLIM = 1;
    I(in1,out1) <+ V(in1, out1) ;
  end



 end

endmodule
```

Ideal Switch Verilog A model:

```
// VerilogA for latest_pmc_8_2009, switch, veriloga

`include "constants.vams"
`include "disciplines.vams"

module switch (in, out , pc, nc ) ;
 inout in , out ;
 input pc , nc ;
 electrical in , out ;
 electrical pc , nc ;
 parameter real control_Vth = 1 ;


 analog begin
 if ( V(pc,nc) >= control_Vth )

  V (in, out ) <+ 0 ;

  else

  I(in , out) <+ 1E-8  ;
  end

endmodul
```