A Low Cost, High Dynamic Range, Versatile Digital Readout Integrated Circuit Unit Cell Prototype for Infrared Imaging Applications

by

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ABSTRACT

Readout Integrated Circuits(ROICs) are important components of infrared(IR) imaging systems. Performance of ROICs affect the quality of images obtained from IR imaging systems. Contemporary infrared imaging applications demand ROICs that can support large dynamic range, high frame rate, high output data rate, at low cost, size and power. Some of these applications are military surveillance, remote sensing in space and earth science missions and medical diagnosis. This work focuses on developing a ROIC unit cell prototype for National Aeronautics and Space Administration(NASA), Jet Propulsion Laboratory's(JPL's) space applications. These space applications also demand high sensitivity, longer integration times(large well capacity), wide operating temperature range, wide input current range and immunity to radiation events such as Single Event Latchup(SEL).

This work proposes a digital ROIC(DROIC) unit cell prototype of 30ux30u size, to be used mainly with NASA JPL's High Operating Temperature Barrier Infrared Detectors(HOT BIRDs). Current state of the art DROICs achieve a dynamic range of 16 bits using advanced 65-90nm CMOS processes which adds a lot of cost overhead. The DROIC pixel proposed in this work uses a low cost 180nm CMOS process and supports a dynamic range of 20 bits operating at a low frame rate of 100 frames per second(fps), and a dynamic range of 12 bits operating at a high frame rate of 5kfps. The total electron well capacity of this DROIC pixel is 1.27 billion electrons, enabling integration times as long as 10ms, to achieve better dynamic range. The DROIC unit cell uses an in-pixel 12-bit coarse ADC and an external 8-bit DAC based fine ADC. The proposed DROIC uses layout techniques that make it immune to radiation up to 300krad(Si) of total ionizing dose(TID) and single event latch-up(SEL). It also has a wide input current range from 10pA to 1uA and supports detectors operating from Short-wave infrared (SWIR) to longwave infrared (LWIR) regions.

DEDICATION

To my parents, Mahalakshmi S K and Late Krishna Prasad Chilukuri, for their support and encouragement throughout my life.

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Chapter 1

INTRODUCTION

1.1. Background

According to Planck's law of black body radiation, all matter above absolute zero temperature(0 K) spontaneously and continuously emits electromagnetic radiation, and the intensity of emitted radiation at any wavelength increases with the temperature of the matter[28], as illustrated in Figure 1.1.

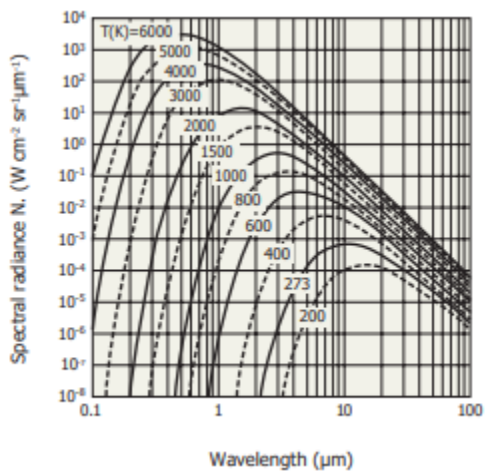

Figure 1.1: Family of Black Body Spectral Radiance(Intensity) Curves vs. Wavelength for Different Temperatures[13]

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It can be noticed from the above illustration that the wavelength of the emitted radiation at peak intensity reduces with temperature. Objects at room temperature to a few hundred centigrade emit electromagnetic radiation with peak intensity in the Infrared(IR) region. Objects hotter than 500 degree centigrade emit radiation with peak intensities shifting towards visible, ultra-violet, x-ray and gamma ray regions with increasing temperature.

1.1.1. Infrared(IR) Radiation

IR radiation covers wavelength ranging from 700nm to 1mm in the electromagnetic spectrum, which translates to frequency ranges from 430THz down to 300GHz[15]. Figure 1.2 illustrates the Electromagnetic spectrum.

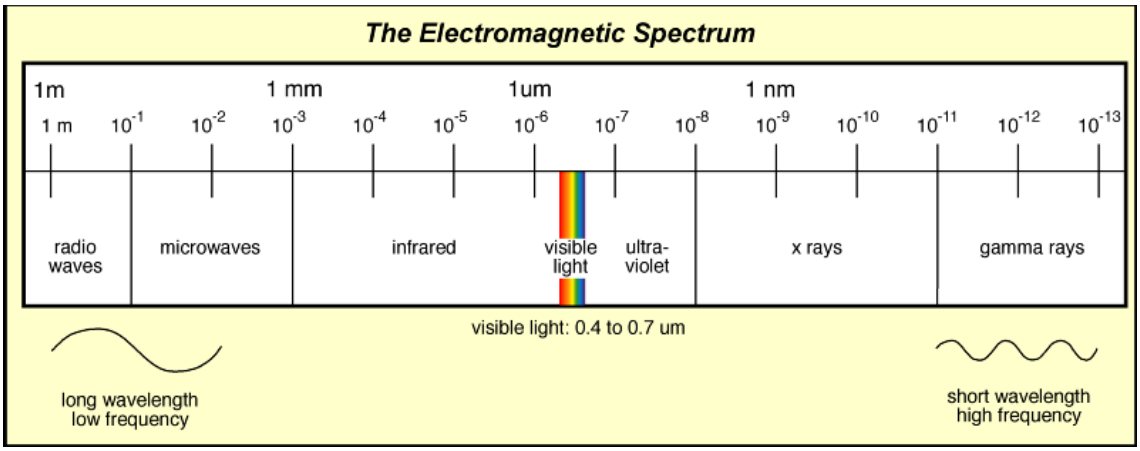

Figure 1.2: Electromagnetic Spectrum Showing IR Radiation Covering Wavelength 700nm to 1mm[4]

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IR radiation is subdivided into smaller regions called Near-Infrared(NIR), Short-wave Infrared(SWIR), Mid-wave Infrared(MWIR), Long-wave Infrared(LWIR) and Very-long wave infrared(VLWIR) based on their response to various IR detectors[17]. Table 1.1 illustrates this division.

Division Name	**Abbreviation**	**Wavelength(μm)**	**Responds to sensors**
Near-Infrared	NIR	0.7 - 1.0	Silicon
Short-wave Infrared	SWIR	1 - 3	InGaAs, PbS, PbSe
Mid-wave Infrared	MWIR	3 - 5	InSb, HgCdTe, PbSe
Long-wave Infrared	LWIR	7 - 14	HgCdTe, microbolometers
Very-long wave Infrared	VLWIR	12 - 30	Doped Silicon

Table 1.1: Division of IR Region into Sub-sections Based on Their Response to Various Sensors

1.1.2. IR Imaging Applications

At present, thermal infrared(IR) imaging systems are gaining popularity because of their applications in wide areas including military surveillance[18], space and atmospheric sciences[18], medical diagnosis[8], firefighting and IR spectroscopy. Figure 1.3 illustrates an application of IR imaging using Near-Infrared(NIR) radiation to detect stenosis(blockages/narrowing) of blood vessels in the heart of mammals.

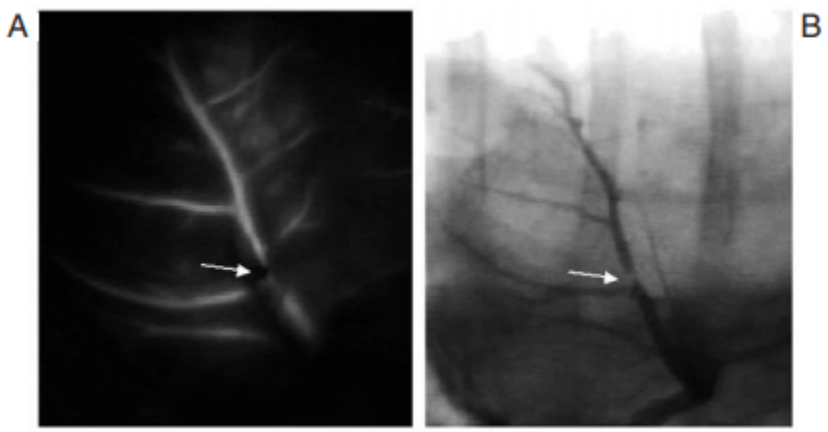

Figure 1.3: Significant Stenosis of the Proximal Part of the Left Anterior Descending Coronary Artery Depicted by Near-infrared Fluorescence Coronary Angiography (A) and Coronary Angiography (B). Image Taken From [8]

Hyperspectral IR imaging systems produce images that cover a wide portion of the IR spectrum. These systems operate in the LWIR or MWIR regions of the infrared radiation and are used in the military area to help detect and identify chemical gases present in the atmosphere to protect nations from chemical attacks [18]. They also have the ability to remotely sense IR signatures of ground or airborne targets in battlefields. Figure 1.4 illustrates an application that detects chemical gases in the atmosphere by sensing infrared radiation from the atmosphere, then classifying regions to a particular chemical species based on intrinsic infrared signatures of chemicals[18] and displaying them in a color-coded format.

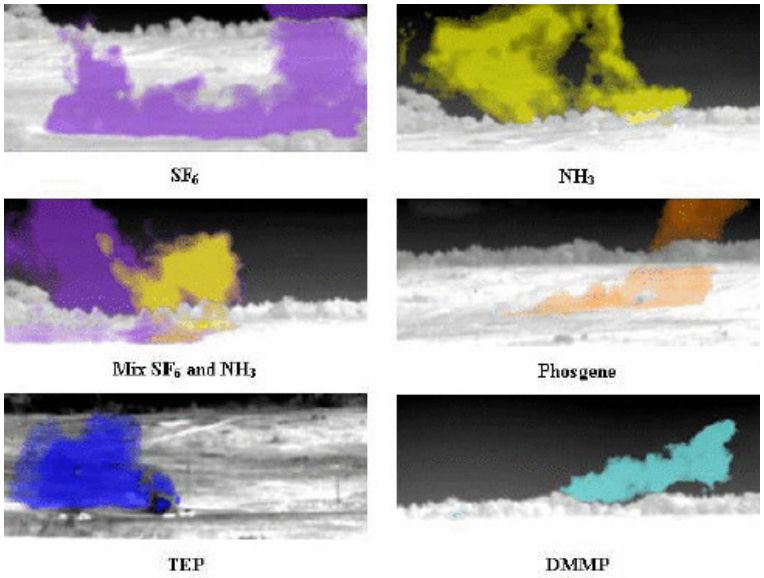

Figure 1.4: Chemical Gas Releases. Image Taken From[18]

Thermal imaging camera(TIC) renders heat picked up from the environment in focus as visible light by first converting them to electricity through use of IR detectors. These cameras are also used by firefighters as they allow them to see through smoke, detect where flames are concentrated and rescue victims invisible to the naked eye due to smoke by detecting their heat signatures. An example is shown in Figure 1.5.

Figure 1.5: A Drone Equipped with Thermal Imaging Reveals Where Flames Are Concentrated Inside of a Burning House, During a Training Exercise. (Roswell Flight Test Crew) Image Taken From [14]

1.1.3. IR Imaging Systems

Thermal(IR) imaging systems allow us to see temperature differences of various objects by making use of the fact that intensity of infrared radiation emitted increases with the temperature of the body as illustrated in Figure 1.1. These systems convert the intensity and thus temperature information of the environment in focus into a visible representation even if the environment is lacking visible light, by making use of detectors that convert the incident IR radiation into some form of electricity. The resulting visible contrast representation is termed Thermogram. There are two types of IR imaging camera systems: cooled and uncooled.

Cooled thermal imaging cameras have image sensors that are integrated with cryocoolers[28]. Cryocoolers are devices used to bring down the temperature of the sensors to as low as 73K. This is done to bring down the thermal noise of the sensors to a level below the signal that is intended to be measured. These types of cameras have very high sensitivity due to reduced thermal noise and they can be made to image in the MWIR and LWIR regions of IR radiation where thermal contrast is naturally high as described by the law of black body radiation. These cameras however have shorter service lives compared to uncooled cameras, because they are equipped with moving parts to perform the necessary cooling. These cameras have high imaging speeds and are capable of supporting microseconds of exposure times and also have greater magnification capabilities.

Uncooled cameras do not need cooling, they are instead equipped with detectors based on microbolometers. Microbolometers are thermal detectors made out of materials with high temperature co-efficient of resistance(TCR). They measure the intensity of incident IR radiation through change in their electrical resistance. Amorphous silicon and Vanadium oxide are some types of materials that can be used to

make microbolometers as they have high TCR and can be easily integrated with modern CMOS processes[9]. These type of cameras are mostly used to image IR radiation in the LWIR region. These cameras are less expensive as they do not require cooled packaging and they also have longer service lives compared to cooled cameras as they don't use any mechanical moving parts for cooling. One disadvantage of uncooled cameras as opposed to cooled cameras is that they use a rolling shutter(read out pixel data line by line), thus making it difficult to capture moving objects without blurring. Cooled cameras however use global shutter(read out pixel data all at once), thus they have faster response time.

Cooled cameras are best suited for applications that require high sensitivity, large contrast ratios and for those that have moving objects. They are also best suited for applications that require visualizing small targets or specific parts of the IR spectrum. This work focuses on readout integrated circuit(ROIC) unit cell design for NASA JPL's HOT-BIRD detector, which can operate with high quantum efficiencies even at a temperature of 150K. This only requires passive cooling and thus reduces cooling cost. However, the proposed ROIC can operate adequately enough at room temperature for testing purposes. Figure 1.6 illustrates a simple IR imaging system.

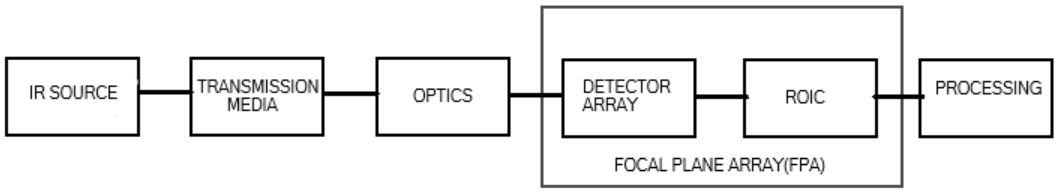

Figure 1.6: Simplified IR Imaging System

IR radiation from a source travels through a transmission medium and is focused onto the detector array through optics. The detector array comprises of individual detector unit cells that convert intensity information of the incident IR radiation to electrical charge, voltage or resistance and the ROIC unit cells accumulates and stores

the converted electrical information and transports it to processing circuits. The focal plane array(FPA) is the heart of any IR imaging system, the quality of the detector and ROIC used in them decides the quality of the imaging system.

1.1.4. Focal Plane Array(FPA)

Conventional charge-coupled device(CCD) and CMOS image sensors for visible light imaging are fabricated from silicon using mature processes. IR sensors, specially the ones used in high sensitivity applications, need to be fabricated with more exotic narrow bandgap materials[7], such as Mercury Cadmium Tellurite(MCT), Indium Antimonide(InSb), and less-well developed processes[12], as silicon is sensitive only to visible and NIR spectra. These narrow bandgap materials cannot be grown into crystals anywhere near the size of modern silicon crystals nor can they be used to construct electronics required to multiplex the resulting electrical charge, voltage or resistance. These functions of storing and transporting electrical charge, voltage or resistance is performed by an on-chip ROIC, that is fabricated in silicon using standard CMOS processes. The detector array made of narrow bandgap materials and ROIC are then hybridized into a structure called focal plane array(FPA), typically using indium bump-bonding, as in Figure 1.7.

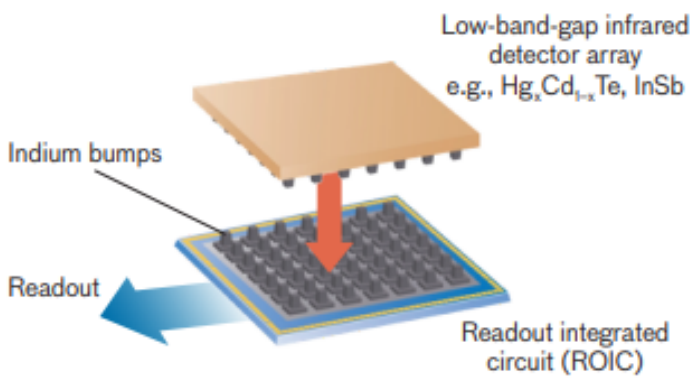

Figure 1.7: Components of a Typical IR FPA. Image Taken From [12]

These IR FPAs, compared to conventional discrete designs, have advantages of high packaging density, low cost, reduced signal leads through dewars, high feasibility, high flexibility for system integration and on-chip processing capabilities[7].

1.1.5. IR Detectors

IR detectors are devices used to convert incident IR radiation into electrical charge, voltage or resistance. There are two main types of IR detectors: photon detectors and thermal detectors[7].

Photon detectors convert the incident photons directly into free current carriers by exciting the electrons across the bandgap of semiconductor to the conduction band. This results in a change in detectors electrical property. These devices require cooling to keep the thermal noise minimal and the spectral response of these detectors depend on the bandgap of the semiconductor and wavelength of incident radiation[7].

In thermal detectors incident IR radiation is absorbed into the lattice of the detector and it changes the temperature of the detector, which further results in a change in its physical or electrical property. These detectors operate at room temperature and have wide spectral response, however they lack sensitivity and have slower response times compared to photon detectors[7]. Table 1.2 compares photon and thermal detectors.

Parameters	**Photon detectors**	**Thermal detectors**
Response time	Fast	Slow
Spectral responsivity	Narrow	Wide
Sensitivity	High	Low
Operating temperature	Below 200K	Room
Cost	Expensive	Economical

Table 1.2: General Properties of Photon and Thermal Detectors. Table Taken from[7]

NASA JPL's HOT-BIRD falls into the category of photon detectors. Some of the popular photon detector structures are Photovoltaic(PV), Photoconductive(PC), and Schottky Barrier detectors. The proposed ROIC unit cell is suitable to be used with all these types of detectors.

Photovoltaic(PV) detectors: These detectors are based on semiconductor P-N junction devices. When IR radiation is incident on these structures the inherent P-N junction barrier results in a photovoltaic (PV) effect. If IR radiation with energy greater than the bandgap of the P-N junction is incident on the structure it generates electron-hole pairs and results in photocurrent. The generated photocurrent increases with increasing intensity of incident radiation. These devices are nominally operated under zero bias to obtain higher output shunt resistance, which is important to obtain high sensitivity and good input injection[20]. The output shunt resistance of these detectors are expressed as R_oA, where R_o is the shunt resistance of the detector normalized to detector area A, under zero bias. They consume near zero power and their performance is limited by thermal and flicker noise.[7]

Photoconductive(PC) detectors: These detectors convert the incident IR radiation into electron current through change in conductivity of the detector. The detector conductivity increases with increasing intensity of incident IR radiation. These detectors operate at a fixed bias voltage, and thus give out photocurrent that increases with increasing intensity of incident photons[20]. They consume non-zero power and require heat dissipation mechanisms. In addition to thermal and flicker noise, these devices are also limited by recombination noise of charge carriers[7].

Schottky barrier detectors: They are based on metal-semiconductor schottky barriers and usually made of thin platinum-silicide(PtSi) using standard CMOS processes. Due to their low forward barrier photoexcited charge carriers can jump over the schottky barrier and accumulate in the silicide layer[7], which can then be trans-

ferred into ROIC. Thus their main mechanism of action is charge accumulation. The generated charge is proportional to incident photon flux. NASA JPL's HOT BIRD falls into this category.

NASA JPL's space-based and airborne remote sensing applications such as water vapor and green house gas measurement demand IR detectors capable of detecting wide spectral ranges. Using classical optical components such as prisms and filters to separate out different wavelengths of wide-band IR spectra, before they reach detectors that detect different subsections of wide-band IR spectra results in complicated and heavy systems[5]. A simple system will result in using a single optical system and seeking a detector that can respond separately to each wavelength subsection. At present detectors made of Mercury Cadmium Telluride(HgCdTe)(MCT), and Quantum Well Infrared Photodetectors(QWIPs) are sensitive to wide spectral ranges and have detection capability in MWIR-LWIR ranges.

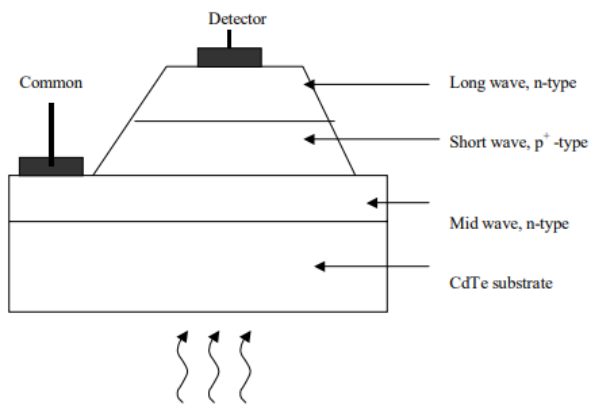

Figure 1.8: Schematic Cross Section of Triple Layer IR Detector in HgCdTe. Image Taken From[5]

Figure 1.8 illustrates an n-p-n three layer structure in HgCdTe which is epitaxially grown on CdTe substrates. The detector is illuminated from the backside through the substrate as CdTe has a bandgap much higher than wavelengths of interest. The wavelengths of interest can be selected by applying appropriate bias voltage at the

"Detector" contact. The "Common" contact is usually held at mid-supply and appropriate bias above or below mid-supply is applied at the "Detector" contact to select the wavelength subsection. However, these HgCdTe detectors are associated with expensive fabrication costs and they need to be operated at very cold temperatures. NASA JPL recently developed the HOT-BIRD detector capable of operating at 150K[1] and with lower fabrication costs compared to HgCdTe.

Another important property of these detectors that decides the performance of the overall IR imaging system is the quantum efficiency(QE), also termed as the Incident Photon to Converted Electron(IPCE) ratio[24]. It is defined as the number of signal charge carriers(electrons/holes) created per incident photon. Since the energy of a photon is inversely proportional to its wavelength, QE has an inherent wavelength dependence. A plot of QE vs wavelength is termed spectral response of the detector. Figure 1.9 shows the spectral response of MWIR InAs/InAsSb HOT-BIRD detector.

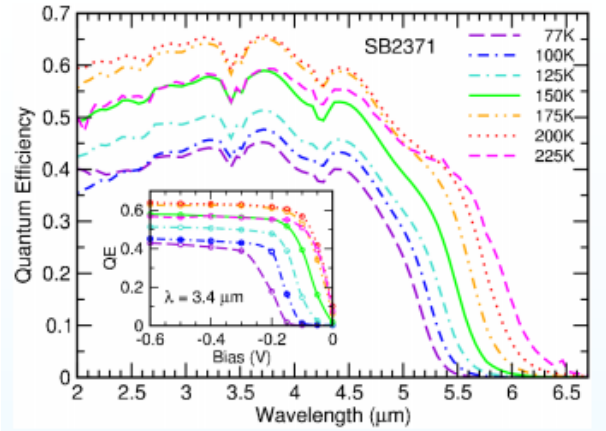

Figure 1.9: Spectral Response of the MWIR InAs/InAsSb HOT-BIRD Detector. Image Taken From[1]

As seen in the above figure the quantum efficiency increases with increasing temperature and with increasing reverse bias. This is due to reduction of the bandgap energy of the detector. Dynamic range of FPA cameras at a given wavelength depends on QE and ratio of strongest to weakest IR radiation in the imaging environment.

1.1.6. Readout Integrated Circuit(ROIC)

Readout integrated circuits(ROICs) form an interface between the IR detectors and other processing circuitry. They are responsible for maintaining detector bias voltages, controlling frame rates and integration times, integrating/accumulating weak detector signals over time to improve signal to noise ratio(SNR), holding measured signal in analog or digital form and multiplexing held data to processing circuits on demand. As such the performance of ROIC impacts the performance of the entire IR imaging system. Thus ROIC performance in terms of detector bias control, input current range, frame rate, injection efficiency, size and pitch, power, cost, charge storage(well) capacity, noise, output data rate and operating temperature should be considered in its design[7]. ROICs can be broadly classified into two main types based on whether individual unit cells hold an analog or digital equivalent of the signal measured: Conventional analog ROIC and Digital ROIC(DROIC)[12]. Conventional analog ROICs hold an analog voltage or charge equivalent of incident IR radiation in individual pixel unit cells and an analog to digital converter(ADC) outside the pixel array digitizes the analog voltage or charge before multiplexing it to digital processing systems. DROICs on the other hand perform in-pixel digitization of electrical voltage or charge equivalent to incident IR radiation. DROICs are the focus of this work. Chapter 2 discusses ROICs, their types and architectures in more detail.

1.2. Motivation

Emerging advanced IR imaging applications for industrial research and development, space and airborne remote-sensing as well as NASA JPL's current IR imaging requirements with the HOT-BIRD detector, demand ROICs with well capacities greater than a billion electrons (to support longer integration times),

dynamic range greater than 16-bits, high sensitivity or low noise and strong detector bias control all at the same time with low cost, size and power[1]. Many existing conventional analog ROICs in the market and literature, do not meet the above-mentioned requirements due to limitations of ADCs that are needed to perform the readout[12]. Even high performance DROIC based imaging systems in market, such as the ones from FLIR Systems[2], have a well capacity of only about 18 million electrons and dynamic range of the order of 14-16 bits. State of the art DROICs in the literature, such as the ones from MIT's Lincoln Laboratory, fabricated in advanced 65-90nm processes also has well capacity of only 230 million electrons when operated at high sensitivities[12], which translates to a dynamic range of 16 bits with a conversion gain(electrons per digital count) of 3500. Thus, there is a need for DROICs that meet the above-mentioned requirements, and this thesis focuses on designing such a DROIC unit cell in a low cost 180nm process.

1.3. Prior Work

Many industries and people in academia are working towards developing state of the art DROICs and IR detectors for advanced IR imaging systems. In [12], MIT's Lincoln laboratory, developed a DROIC unit cell that uses a digital counter to count the number of incident photo-electrons on the pixel. In [2], FLIR Systems describes its ISC0903, a 30μm pitch ROIC suitable for industrial thermal cameras. [7] describes several common DROIC unit cell architectures and compares their performances and trade-offs. [20] describes the physics behind the operation of various IR detectors. Table 1.3 below compares the performance of ROICs described in [12], [2] and this work.

Parameter	MIT DROIC	FLIR ISC0903	This work
Process	90nm	NA	**180nm**
Pixel pitch	30μm	30μm	30μm
Bits	16	14	**20**
Digital count(LSB electrons)	3000-6000	800	**1218**
Well capacity(electrons)	$\sim$ 200 to 400 million	18 million	**1.27 billion**
Integration capacitance	1-2.5fF	NA	50fF
Operating temperature	68-85K	65-300K	150-300K
Input current range	NA	20pA-10nA	**10pA-1uA**
Detector resistance(Rd)	150MΩ	NA	350MΩ
R_oA (Ωcm^2)	NA	10^3	NA

Table 1.3: Comparison of Performances of MIT's Lincoln laboratory DROIC, FLIR ISC0903 ROIC and DROIC Presented in This Work

1.4. Proposed Solution

The work presented in this thesis builds on the DROIC unit cell proposed in [12] and provides a new way to achieve high well capacities and high sensitivities at the same time, by using a 12-bit digital counter based coarse ADC within the unit cell combined with a global 8-bit DAC based fine ADC. This provides an effective way to increase the overall dynamic range to 20 bits, achieve high sensitivities to detect as low as 1218 electrons and simultaneously increase well capacity to 1.27 billion electrons. The proposed DROIC unit cell is designed on a low cost 180nm on-semiconductor process. The proposed DROIC makes use of a simple single ended amplifier to obtain tighter control on the detector bias voltage and effectively increases the tolerable input current range of the DROIC. The proposed DROIC is specifically designed for NASA JPL'S HOT BIRD detector which can be either p-on-n type or n-on-p type, where the detector either sources or sinks current respectively. The proposed DROIC unit cell is expected to work in radiation

environments of upto 300krad(Si) of total ionizing dose(TID) and is also immune to radiation induced single event latchup(SEL). The proposed DROIC can operate across temperatures ranging from 150K to 300K.

1.5. Thesis Organization

This thesis is organized into 5 chapters. Chapter 1 provided some background on FPAs, ROICs and discussed about previously developed ROICs and how they compare with ROIC unit cell proposed in this thesis. Chapter 2 provides insight on detector circuit modeling for simulation, ROIC types, proposed ROIC architecture, specifications and compares their advantages and design trade-offs. Chapter 3 provides circuit details and analysis of the proposed DROIC unit cell. Chapter 4 discusses results from simulating the proposed DROIC. Chapter 5 concludes and provides information on future improvements.

Chapter 2

DETECTOR MODELING & ROIC ARCHITECTURES

2.1. Detector Circuit Model

As explained in section 1.1.6, ROICs are an interface between the detector array and processing circuits. Detector arrays for IR FPAs are 2-dimensional(2D) arrays of photodetectors made of bandgap engineered materials sensitive to IR spectra. An equivalent circuit model and cross-section of a HgCdTe(MCT) photodiode is illustrated in Figure 2.1.

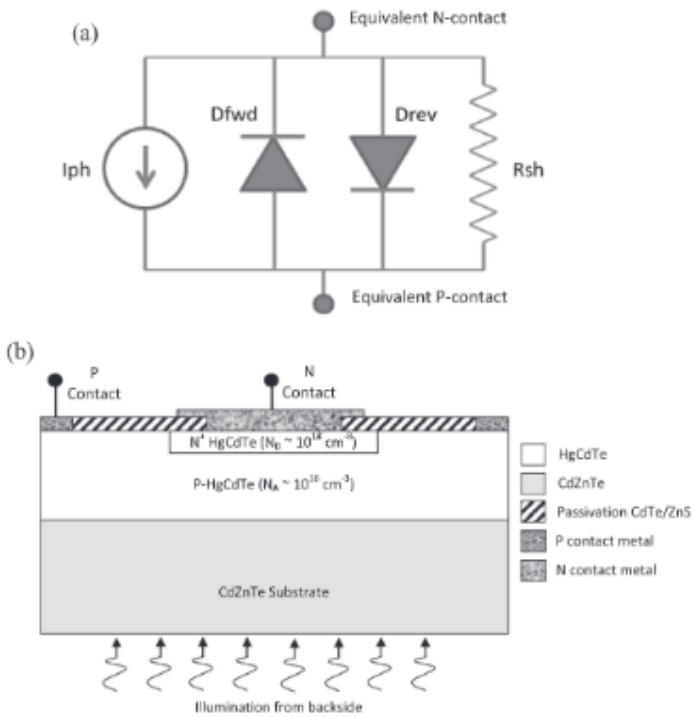

Figure 2.1: (A) Circuit Model for HgCdTe Photodiode and (B) Schematic Cross-section of HgCdTe Photodiode. Image Taken From [22]

Photon detectors conduct two types of current: dark current and illumination current. The leakage current that flows through the photodiode in the absence of photo-

excitation, under application of a bias voltage is termed dark current. Photo current that is a result of photo-excitation is termed illumination current. Diodes Dfwd, Drev combined with shunt resistance (Rsh) in Figure 2.1 (a), form the dark current model of the MCT photodiode. Dfwd and Drev are standard PSPICE diode models. The forward dark electrical characteristics of MCT photodiode can be matched by adjusting the PSPICE model parameters of the Dfwd diode[22]. These MCT photodiodes are mainly used in reverse bias mode, as the widths of the depletion region of these devices are larger in reverse bias mode, which reduces the junciton capacitance of the photodiode and increases absorptivity of photo-excited charge carriers into the ROIC. Reverse current conduction of these MCT photodiodes is accounted by the diode Drev, with modified PSPICE model parameters, in opposite direction, such that forward conduction of Drev represent reverse conduction of the MCT photodiode[22]. Shunt resistance(Rsh) models the zero-bias dark current. It is important that the input resistance of the ROIC unit cell is much lesser than the detector shunt resistance(Rsh) to achieve maximum injection efficiency. Illumination current is modelled by a constant current source in parallel to the dark current model[22]. Simplified models that are only a representative of the photodiode don't include the Dfwd diode as they are main used only in reverse bias, and they omit the obvious shunt resistance but explicitly show the junction capacitance as shown in Figure 2.2. Appendix A.1 includes implemented verilogA code to model the photodetector.

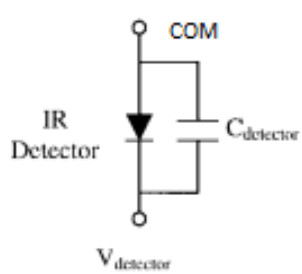

Figure 2.2: Simplified IR Detector Model. Image Taken From[7]

2.2. Prior ROIC Architectures

ROICs are a 2D array of ROIC unit cells or pixels. Each unit cell in the ROIC array maintains the bias of the photodetector to which it is hybridized in the detector array, and integrates charge or photocurrent on a capacitor in the unit cell and holds the integrated signal value either in digital or analog form. Some general specifications of the ROIC unit cell are discussed below[7, 2] in section 2.2.1. Different ROIC types conventional analog and digital are discussed in section 2.2.2.

2.2.1. ROIC Specifications

Different IR imaging applications demand different requirements from the ROIC unit cell. Below discussed parameters are common to most of the commercial and academic ROICs.

1) *Detector bias range, resolution and control*: The detector bias range is the range of voltages within the supply headroom that the ROIC can bias the detector at. A larger bias range allows DROICs to be compatible with a variety of detector arrays. Detector bias resolution specifies the accuracy to which the detector bias voltage can be set. Detector bias control refers to the stability of the detector bias across the range of detector currents. High bias resolution and stable bias control are necessary to achieve low dark current, high injection efficiency, low flicker noise and high linearity.

2) *Injection efficiency and bandwidth*: The ratio of current entering the ROIC unit cell and total detector current is termed injection efficiency. High injection efficiency helps obtain high dynamic range at high frame rates. High bandwidth helps achieve faster response times. The input resistance of the ROIC unit cell must be lesser than the detector shunt resistance to obtain high injection efficiency and bandwidth.

3) *Well capacity*: The maximum amount of charge a ROIC unit cell can store is termed well capacity. Large well capacities are desired to achieve large integration times and high dynamic range. The well capacity of a conventional analog ROIC depends on the background or dark current of the photo-detector and the value of the integration capacitor. Higher well capacities can be achieved by limiting dark current values and using large integration capacitors. However pixel or unit cell area limitations impose restrictions on possible capacitor values.

4) *Noise*: There are 3 main sources of noise in IR imaging systems: Background radiation noise or photon noise, detector noise and readout circuit noise. Detectors and readout circuits are prone to random, time-invariant noise due to inherent non-uniformities in the fabrication process. This noise is termed Fixed Pattern Noise(FPN)[7]. Processing circuits and software apply certain algorithms to eliminate FPN. Other sources of noise in the readout circuit include white(thermal) noise, flicker noise and reset noise from clocking digital circuits. Combined noise of the detector and readout circuit show be below the levels of photon noise to achieve Background Limited Infrared Photodetection(BLIP)[20]. BLIP is achieved when the IR imaging system's noise performance is limited by background photon noise and not by the IR imaging system itself.

5) *Dynamic Range*: The ratio of well capacity to the noise floor of IR FPAs is termed Dynamic range. Dynamic range requirement for IR FPAs depend on the application needs to distinguish between strongest and weakest IR signals. Dynamic range of ROIC is limited by integrating capacitor values and thus ROIC unit cell area, noise levels and linearity.

6) *Frame rate and integration time*: Frame rate is the rate at which the output image is updated. Higher frame rates are desired to image fast moving targets and rapidly changing systems. Circuit speed and leakage limitations decide the maximum

and minimum attainable frame rates. Integration time is the interval during which the ROIC unit cell accumulates detector current/charge onto the integration capacitor. The ROIC well capacity and sensitivity decide the allowable integration times.

7) *Readout rate*: It is the rate at which the ROIC can multiplex data to processing circuitry. It is usually limited by allowable power consumption and circuit speed. High frame rate or high resolution applications demand higher readout rates.

8) *Array size and Pitch*: Array size refers to the product of number of rows and columns of individual ROIC unit cells in the ROIC array and Pitch refers to the distance between consecutive pixels. High resolution applications demand large array size and small pitches. However, large pixel pitches are needed to achieve high dynamic range.

9) *Power dissipation*: It is the total power a ROIC consumes. This is a strict specification on IR imaging systems that use photon detectors than thermal detectors. In photon detector based systems the allowable power dissipation is decided by the maximum heat loading the cooling system can take, which ultimately decides the cost of the system.

10) *Operating temperature*: The operating temperature is decided by the type of the detector used and the region of wavelengths the detector is intended to detect. This can vary widely based on the application requirements.

2.2.2. ROIC Types

Depending on whether the ROIC unit cell stores the measured signal in analog or digital form, there are two types of ROIC unit cells: Conventional analog ROIC and Digital ROIC unit cells.

Conventional ROICs: In conventional analog ROICs, the unit cells accumulate and stores the incoming photo-current or charge on a capacitor, which acts like a

charge well as shown in Figure 2.3(b). The well capacity or maximum charge that can be stored during an integration is equal to the product of the capacitor value and maximum voltage allowed across the capacitor. The circuit contains an injection transistor M_i, which biases the detector at the desired operating point, collects photocurrent and delivers it to the integration capacitor, while simultaneously isolating the detector bias from the following circuitry: Integration capacitor (C_{int}), reset switch(M_{rst}) and pixel select switch(M_{sel}). The integrating capacitor voltage is proportional to the intensity of incident photoelectrons, and this voltage is connected to a multiplexer bus through switches and simple buffers, which can then be read out to output ports sequentially, through use of a row-column decoder(pixel select) circuit for further processing using Analog to Digital Converters(ADCs) as in Figure 2.3(a).

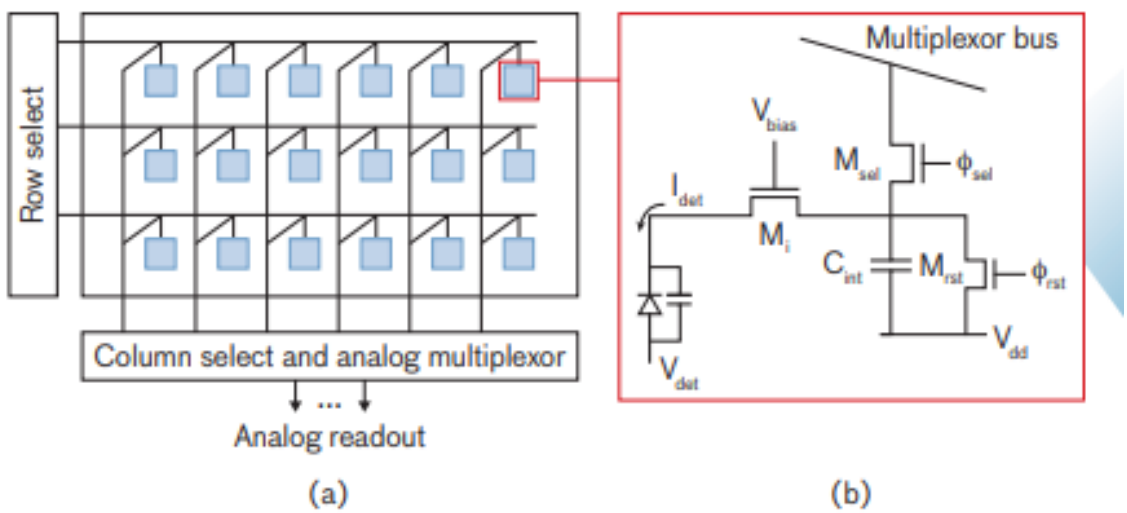

Figure 2.3: (A) Analog ROIC Architecture with (B) Simplified Unit-cell or Pixel Circuit Diagram [12]

Current technology limitations allow to achieve a well capacity of only <25 million photoelectrons in a 30μm pixel[12]. Assuming the ROIC is optimized for noise and

we achieve shot-noise limited detection(Poisson process limited statistical fluctuations associated with the detected photoelectrons), maximum dynamic range or SNR_{max} is achieved when

$$SNR_{max} = \frac{Signal_{max}}{Noise} = \frac{N_{well}}{\sqrt{N_{well}}} = \sqrt{N_{well}} \tag{2.1}$$

Where N_{well} is the well depth in terms of number of photoelectrons.

Thus with analog ROICs, a maximum well depth of 25 million photoelectrons results in an SNR_{max} of 5000 which corresponds to only 12.3 bits of dynamic range[12]. As explained earlier to obtain maximum sensitivity these IR FPA systems need cooling using dewars, and these dewars have limited output ports. It is a challenge to maintain the SNR(dynamic range) while keeping the number of output ports a minimum. Current ADCs can support 14 bit of dynamic range at a data rate of 20 Megapixels per second[12]. Thus to achieve higher output data rate, increasing the number of output ports may be necessary. The limitations on maximum well capacity and maximum data rate per output port make it difficult to scale this analog ROIC technology to current high sensitivity, high frame rate and high resolution applications.

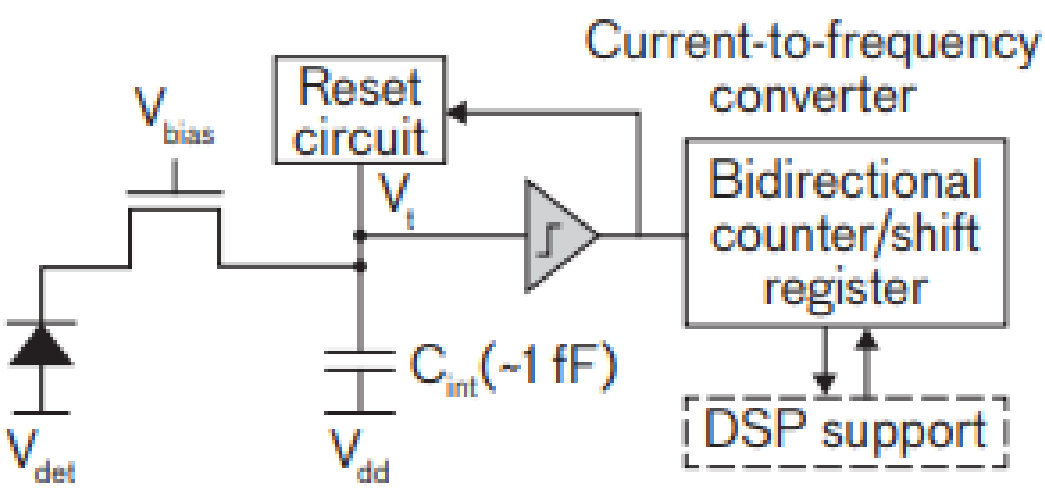

Figure 2.4: Digital ROIC Unit Cell Architecture. Image Taken From [12]

Digital ROICs(DROICs): MIT's Lincoln laboratory introduced the DROIC based FPAs that convert the read analog signal into digital within the pixel unit cell to overcome limitations of conventional analog ROICs[12]. Figure 2.4 shows the structure of the basic unit cell. The circuit consists of a direct injection transistor that also biases the photodetector and a current to frequency(I to F) converter based ADC. The I to F converter makes use of an integration capacitor to convert the photocurrent to a voltage, and this voltage is compared to a known reference voltage(V_t) using a comparator and a reset circuit resets the integration capacitor to supply(V_{dd}) once the threshold voltage is reached (capacitor well is full). This results in a voltage swing from V_{dd} to V_t on the integration capacitor and also results in a pulse train at the output of the comparator, the frequency of this pulse train is proportional to the photocurrent from the detector. The pulse train from the comparator drives a 16-bit counter, which counts the number of times the capacitor well is filled. At the end of integration cycle the counter value represents the number of capacitor well fills, thus the LSB of the digital count is a representation of the maximum charge on the integration capacitor, which is given by

$$Q_{max} = C_{int}(V_{dd} - V_t) \tag{2.2}$$

The same counter can be reconfigured to work as a shift register to readout the measured data at the end of the integration cycle. Furthermore these counter/shift registers of individual unit cells can be connected in a daisy chain fashion in the overall unit cell array to shift measured signal data from pixel to pixel and finally to a serializer which multiplexes measured signal data from various pixels onto output ports. This architecture allows to configure the conversion gain(number of photoelectrons required for filling the capacitor well once), which is equivalent to the LSB or Q_{max} of the ROIC, by having multiple integration capacitors in parallel and switch-

ing between one or a parallel combination of integration capacitors, or through use of pre-amplification. This allows the DROIC unit cell to be configured to either maximize the well depth(Large value of LSB, and high dynamic range), or maximize sensitivity(Smaller LSB value, and less quantization noise). The quantization noise associated in this conversion process is given by

$$Quantization\ noise = \frac{LSB}{\sqrt{12}} = \frac{Q_{max}}{\sqrt{12}} \tag{2.3}$$

With an integration capacitor of 1fF and maximum voltage swing of 1V, the LSB of the digital count is approximately 6200 electrons and the resulting quantization noise is only 1790 electrons. Also, even with a low conversion gain(LSB) of 3500 for high sensitivity imaging, the 16-bit digital well corresponds to an overall well capacity of $2^{16} * 3500 =$ approximately 230 million photoelectrons. This is almost 10 times the well capacity achievable in conventional analog ROICs. Overall the DROIC based FPA technology allows to achieve high-sensitivity, high dynamic range, low power and high speed data readout. Table 2.1 illustrates the advantages of DROIC over conventional analog ROICs.

Analog ROIC	**Digital ROIC**
Digitization is performed by ADCs outside pixel	In-pixel digitization (for DSP support, and fewer dewar penetrations)
Dynamic range limited by that of ADCs	High dynamic range through use of digital counters
Data rate limited by ADC sample rate	High data rate using digital readout circuitry
Scaling results in large expensive systems	Easy scaling to meet emerging demands
Higher power consumption	Digital circuits operate with less power
Analog ROICs are less compact	DROICs use smaller transistors

Table 2.1: Advantages of Digital ROIC over Analog ROIC

2.3. Proposed DROIC Architecture

MIT's DROIC unit cell architecture in [12] allows to configure the conversion gain of the ROIC unit cell to achieve either maximum dynamic range or minimum quantization noise. However certain applications, such as the earth science applications of NASA JPL, demand both high dynamic range and low quantization noise at the same time as described in section 1.1.2. The proposed DROIC unit cell architecture tries to achieve both at the same time, while also improving the detector bias control. Figure 2.5, shows a simplified schematic of the proposed DROIC unit cell.

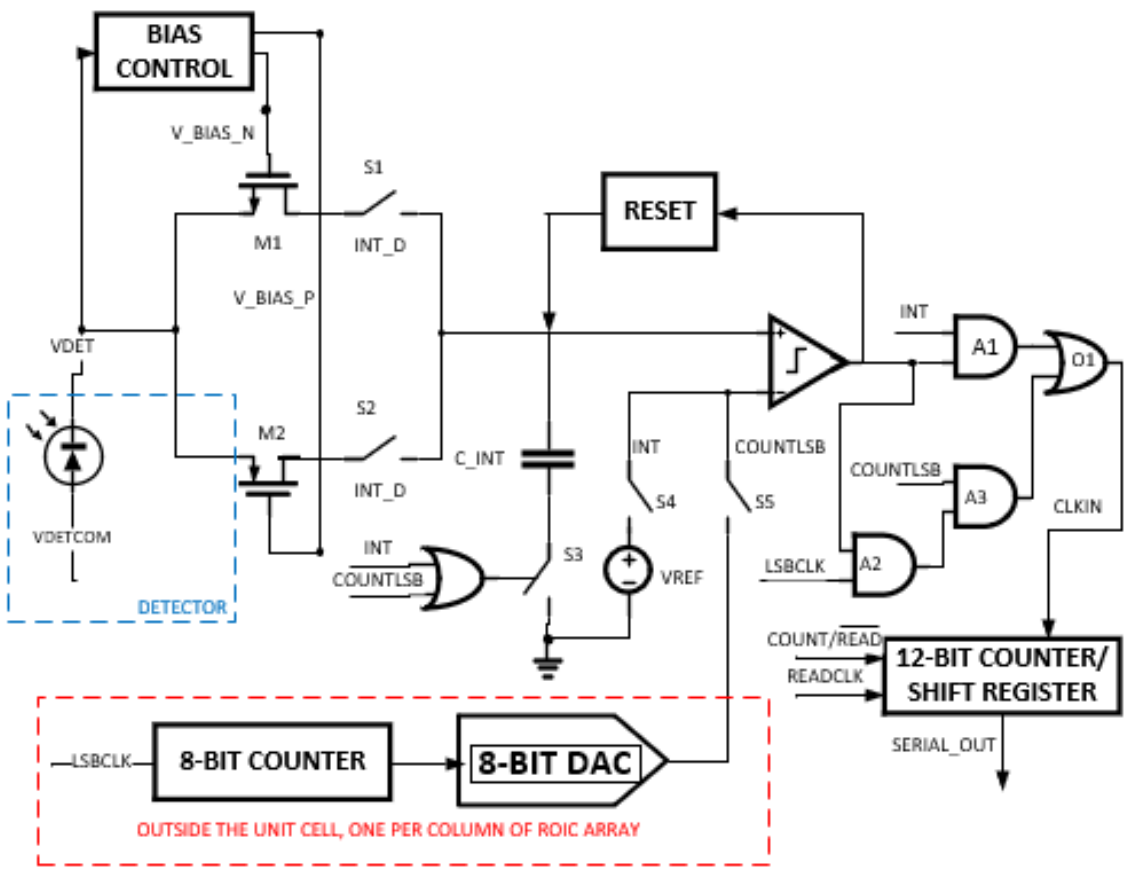

Figure 2.5: Proposed DROIC Unit Cell Architecture Simplified Schematic

The detector node VDETCOM is usually held at mid-supply and the DROIC unit cell is expected to bias the VDET node at appropriate voltages to tune the sensitivity of the detector to different subsections of the IR spectra. The ROIC sources or sinks current onto the integration capacitor depending on whether the detector is p-on-n type or n-on-p type respectively. The proposed cell makes use of two direction injection transistors M1(NMOS) and M2(PMOS) to sink or source the photocurrent onto the integration capacitor C_INT, and simultaenously bias the detector node VDET. An added bias control block will ensure the bias is accurate, stable and biases only one of the transistors M1 or M2 per frame, depending on whether the detector is sinking or sourcing current respectively and shuts down the other transistor. More details about the biasing circuit are covered in chapter 3. Switches S1, S2 and S3 are used to control the integration time through control signals INT and INT_D. INT_D is a delayed version of INT and the three switches together with the integration capacitor C_INT implement bottom plate sampling to eliminate the effects of charge injection[19]. The integration capacitor C_INT, comparator with VREF threshold, and RESET circuit implement a current to frequency converter similar to the one in [12]. Thus when the control signal INT is high, the pulse train output from the comparator whose frequency is proportional to input photocurrent feeds the 12-BIT counter/shift register and at the end of the integration cycle(when INT is pulled low), the 12-bit digital count in the counter is proportional to the input photocharge.

With a C_INT of 50fF and maximum voltage swing across the capacitor of 1V, the total number of electrons required to fill the capacitor well once(LSB) is approximately 312000 electrons. Thus the overall digital well capacity is $2^{12} * 312000 =\sim 1.27$ billion photoelectrons. While this has certainly improved well capacity compared to prior architectures, the sensitivity is still low as the LSB is 312000 electrons. For high sensitivity applications an LSB less than 3500 electrons is desired[12].

To improve sensitivity and dynamic range an 8-bit counter driving an 8-bit DAC outside the unit cell(one per column of the DROIC array) is added to act like a fine ADC to perform the LSB measurement. Figure 2.6 illustrates this operating procedure, while detector is sourcing current.

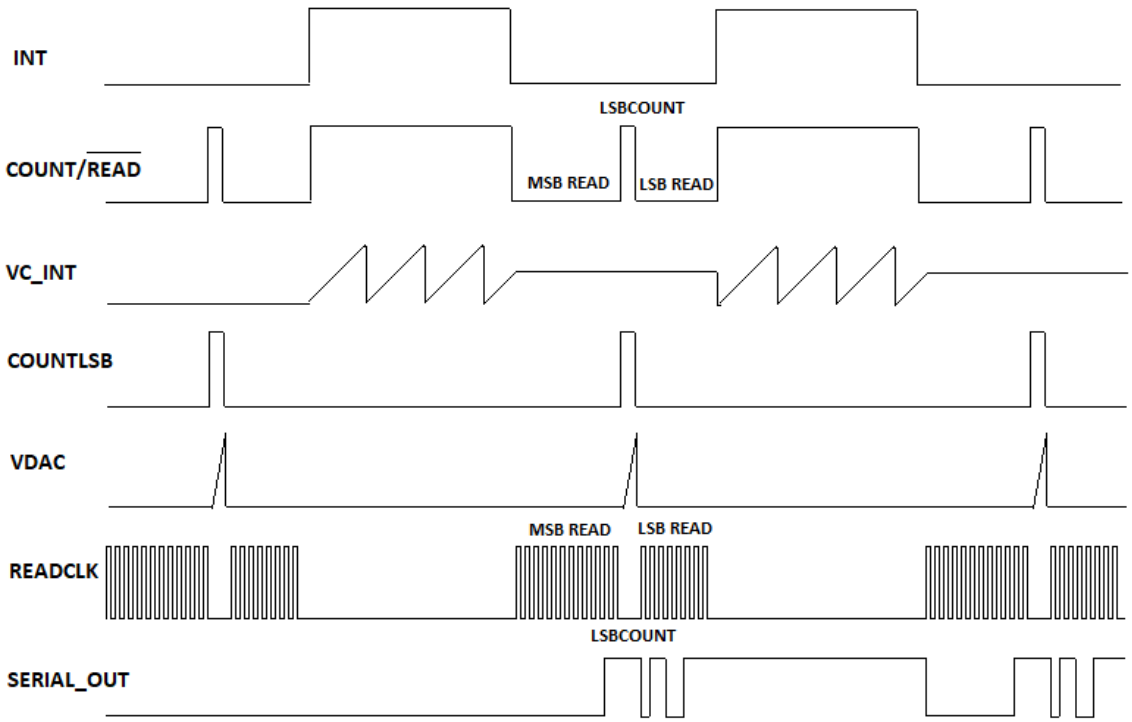

Figure 2.6: Waveforms Illustrating the Operation of the Proposed DROIC Unit Cell Architecture While the Detector Is Sourcing Current

At the end of integration cycle the 12-bit counter is first reconfigured as a shift register through use of COUNT signal and the number of times the integration capacitor fills, termed now on as MSB portion(12-bit), is readout through use of READCLK. The 12-bit counter/shift-register feeds in zeros to the counter while shifting the data out. After reading out this 12-bit MSB portion, the counter/shift-register is reconfigured to operate as a counter, the comparator threshold is switched from VREF to the output of 8-bit DAC, and the 8-bit counter is started to ramp up the DAC through use of LSBCLK clock signal. Added logic circuitry(AND gates A1,A2,A3

and OR gate O1) ensures, the 12-bit counter counts up the LSBCLK clock until the comparator trips. Thus at the end of the DAC linear ramp cycle(after 256 cycles of LSBCLK clock), the 12-bit counter holds an 8-bit representation of the LSB portion. This 8-bit LSB portion can be then readout through use of READCLK clock and configuring the counter/shift-register as a shift-register. This reduces the overall LSB of the unit cell to $\frac{312000}{256} =\sim 1218$ electrons.

Thus this architecture helps bring down the overall LSB(conversion gain) of the unit cell to 1218 electrons for use in high sensitivity applications. The maximum well capacity is 1.27 billion electrons, thus the dynamic range of this overall unit cell is $\frac{1.27\ billion}{1218} =$ 1.043 million, which corresponds to 20 bits. In other-words, the 12-bit MSB digital data combined with the 8-bit LSB digital data, increases the dynamic range of the overall pixel to 20 bits, while maintaining low LSB of 1218 electrons for high sensitivity applications. It is important to ensure the IR FPA's noise performance is limited by shot noise and quantization noise only, the DROIC circuit noise levels should be much lower than these to achieve 20-bit dynamic range.

There are two types of integrating modes in DROICs: Integrate-While-Read and Integrate-Then-Read. Integrate-While-Read mode enables to readout data while integrating incoming photocurrent at the same time. Integrate-Then-Read mode enables to readout data only after integration cycle has finished. The proposed architecture supports only Integrate-Then-Read mode as seen in Figure 2.6. However, the DROIC architecture can be used in applications that demand near continuous integration, because MSB readout, LSB measurement and LSB readout can all be performed within time intervals as short as 5us.

2.3.1. High Speed Readout Architecture

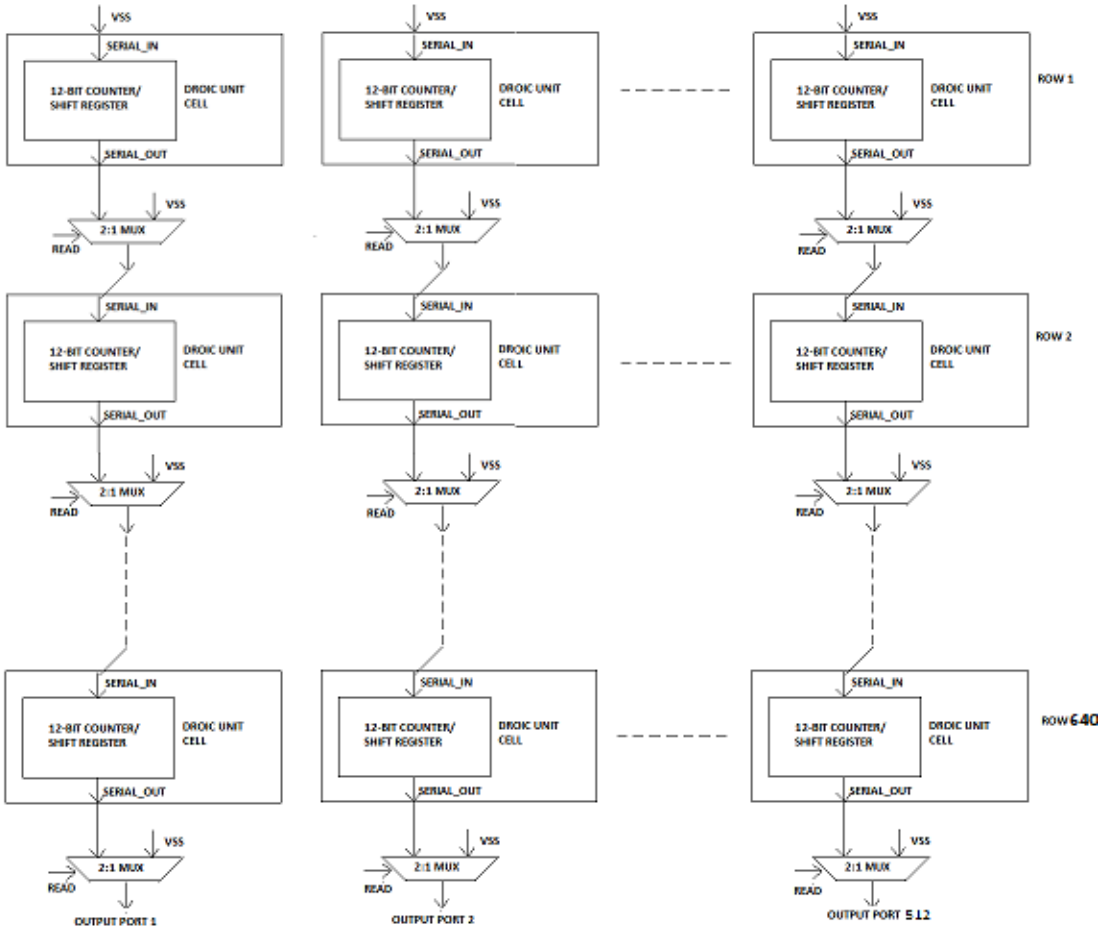

Figure 2.7: Simplified High Speed Readout Architecture

NASA JPL's IR imaging applications demand a resolution of at least 640x512. A DROIC array of 640x512 unit cells has 327680 unit cells and reading out the counter data in all these 327680 unit cells using conventional methods would require 327680 parallel metal output ports which is impractical. Furthermore, these metal output ports would be long, at least 320*30μm = 9.6mm, and add a lot of parasitic capacitance, thus limiting achievable readout rates. To overcome these limitations a daisy-chain readout configuration can be used as illustrated in Figure 2.7. In this

architecture serial data output from the shift register of individual unit cells is connected to serial data input of the shift registers in the unit cells just below them, through use of multiplexers when data is being read out. These connections can be made through lower level metals and the length can be shorter reducing the parasitic load capacitance, and now readout rates as high as 1GHz are easily achievable in this 180nm process and much higher readout rates would only be limited by the process's fT(unity current gain frequency). Also an output port per individual column as shown in Figure 2.7, overall 512 immediate ports would be sufficient to read out the data in all of 327680 pixels reducing the required number of ports by a factor of 640 compared to conventional routing methods. Further serializers can be used to reduce the total number of final output ports to as low as 1,2,4,8 or 16.

Chapter 3

CIRCUIT IMPLEMENTATION OF PROPOSED DROIC UNIT CELL

3.1. Overview

The proposed DROIC unit cell is implemented in ONC18 (on-semiconductor 180nm) process, using 1.8V devices. Prior DROICs discussed in section 2.2 are implemented in much advanced 65 or 90nm processes which add a lot of cost overhead. This 180nm process implementation reduces this cost overhead significantly. The basic building blocks of the unit cell as shown in Figure 2.5 of section 2.3 are: 1) DROIC front-end: This includes bias control circuitry, direct-injection transistors, integration capacitor and bottom-plate sampling switches 2) Comparator, reset circuit and bias buffer 3) 12-bit counter/shift-register and control circuitry 4) 8-bit counter and 8-bit DAC

There are several challenges in implementing these circuit blocks:

1) Pixel area is limited to 30x30μm, and all of the unit cell circuitry including the 12-bit counter which occupies a huge layout foot-print, has to fit within these dimensions.

2) Radiation hardening through addition of bulk contacts for every single transistor used in the unit cells to make it suitable for NASA JPL's IR imaging applications such as space and earth remote-sensing, adds to the layout area overhead.

3) The detector bias has to be stable across a wide range of input current (10pA-1uA).

4) Low noise of the DROIC unit cell on the integration capacitor to ensure high sensitivity

5) Lower power consumption to benefit from cost savings

3.2. DROIC Front-end

DROIC front-end circuitry is responsible for biasing the detector at the desired voltage, isolate the detector bias from following unit cell circuitry: integration capacitor combined with bottom plate sampling switches and reset switches, and integrate the incoming detector photocurrent on the integration capacitor. An important specification for these ROIC structures is *Injection efficiency*. It is defined as the ratio of the current entering the readout circuit to the total detector current. Several front-end ROIC structures have been developed for various applications. Of them Direct-Injection(DI), Buffered Direct-Injection(BDI) and Capacitive Transimpedance Amplifier(CTIA) structures are popularly used in commercial ROICs.

Direct Injection(DI) architecture:

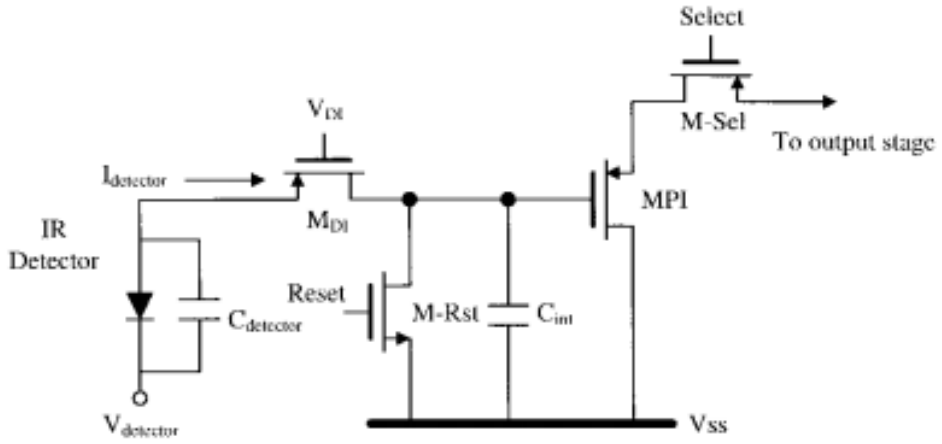

Figure 3.1: A Direct Injection(DI) Readout Circuit. Image Taken From [7]

Figure 3.1 illustrates the DI architecture. This architecture utilizes a common gate transistor M_{DI} to bias the IR detector through gate voltage V_{DI}, isolate it from the detector bias and sense the detector current $I_{detector}$ onto the integration capacitor

C_{int}. The integration capacitor voltage can be reset using the control signal *Reset*. The voltage on the integration capacitor is readout using a source follower transistor *MPI* and select switch *M-Sel* using the *Select* control signal. This simple architecture consumes little area and is appropriate for applications that demand high packaging density. Also the circuit consumes power only when integrating incoming charge from the photodetector, and thus has less power dissipation. The injection efficiency of this architecture as in [27] is given by

$$\eta = \frac{R_d g_m}{1 + R_d g_m} \tag{3.1}$$

Where R_d is the detector shunt resistance and g_m is the transconductance of the DI transistor M_{DI}.

Equation 3.1 shows that the injection efficiency of this architecutre is dependent on the *gm* of the transistor M_{DI}, which is directly dependent on the detector photo-current, which includes background current and dc dark current[27]. Thus this architecture is not suitable for applications that demand high sensitivity(low background current or dark current), which is the focus of this work. Also this architecture requires a stable and low-noise bias voltage V_{DI} for operation and the detector bias voltage has non-uniformities resulting from non-uniformities of the threshold voltage of the direct injection transistor M_{DI}[7].

Buffered Direct-Injection(BDI) architecture:

Figure 3.2 illustrates the BDI readout circuit architecture. The structure improvises the DI architecture by adding a negative gain stage $-A$ between the detector node and the gate of the direct injection transistor M_{BDI}, thereby reducing the input impedance of the DI architecture by a factor A. This helps achieve high injection efficiencies even at low background or dark

currents[7]. It also has strict control on the detector bias voltage due to the negative feedback. A larger gain provides higher control on the detector bias voltage. This architecture is immune to threshold voltage non-uniformities as negative feedback sets the detector bias voltage and also has better noise performance compared to DI architecture. However the added gain stage consumes active power and results in large area when implemented as a differential amplifier.

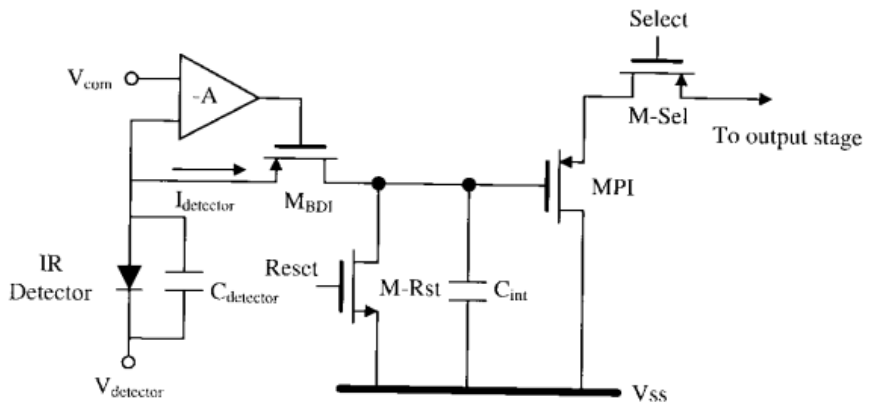

Figure 3.2: Buffered Direct-injection(BDI) Readout Circuit. Image Taken From [7]

Capacitive Transimpedance Amplifier(CTIA) architecture:

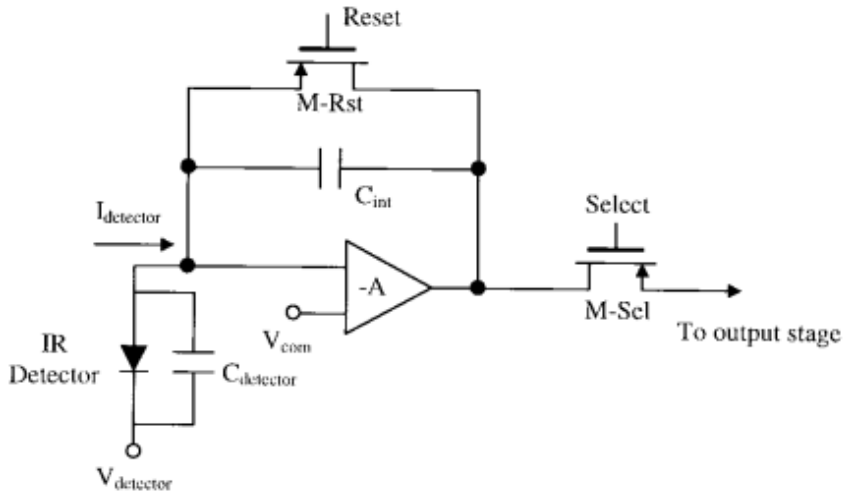

Figure 3.3: Capacitive Transimpedance Amplifier(CTIA) Readout Circuit Architecture. Image Taken From [7]

Figure 3.3 illustrates the CTIA architecture. This architecture places the integration capacitor in feedback of a negative gain stage $-A$ to obtain better bias stability similar to the BDI architecture. Due to the miller effect on the integration capacitor, small values of integration capacitor will yield high sensitivities by reducing the noise at the detector node. Further the input impedance of this architecture is independent of the detector current unlike DI and BDI. However, the *Reset* clock from the reset switch can couple to the detector node due to clock feedthrough and affect the stability of the detector and the amplifier[7]. Further the amplifier needs to have large gain to reduce the offset on the detector bias and this results in large area. The injection efficiency of this architecture as in [27] is given as

$$\eta \approx 1 - \frac{t}{Rd[(1+A)C_{int} + C_{detector}]} \tag{3.2}$$

Where, t is the integration time, R_d is the detector shunt resistance, A is the gain of the amplifier, C_{int} is the integration capacitance and $C_{detector}$ is the detector shunt capacitance. It is thus clear that the injection efficiency of this architecture drops with increasing integration time. To ensure the drop isn't significant, the architecture requires large amplifier gain which results in large area and large integration capacitance. The area and injection efficiency constraints limits the use of this architecture in this work.

Proposed DROIC front-end circuit architecture:

The architecture uses an improvised BDI scheme of integrating the current from the detector. The original BDI structure results in large area and power consumption in meeting the requirements of wide input current range in this work. Several other advanced schemes such as Source Follower Direct Injection(SFDI), Share-Buffered Direct Injection(SBDI), Switch Current Integration(SCI) are described in [16] and [7, 7] respectively.

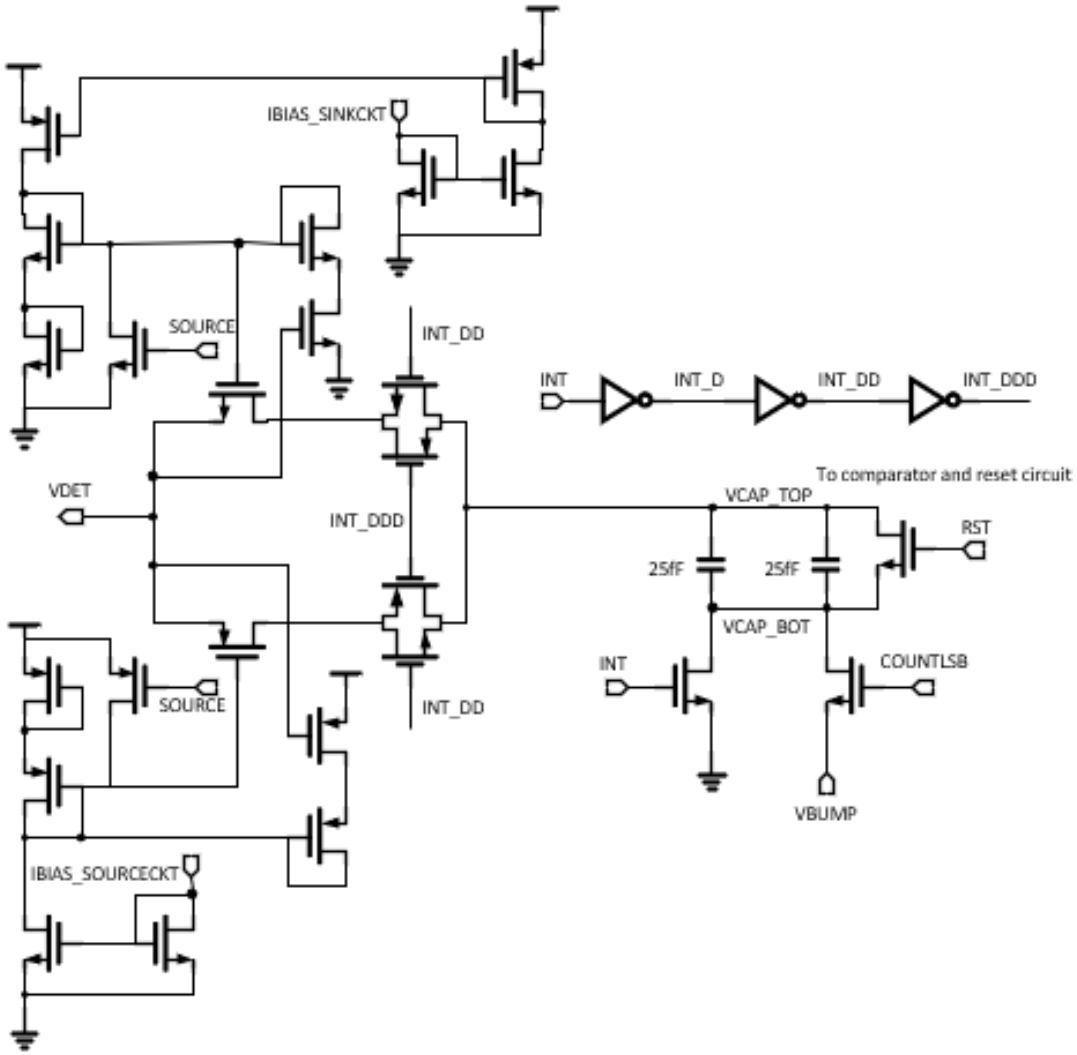

Figure 3.4: Schematic Implementation of the Proposed DROIC Front-end

However, the SFDI scheme described in [16] suffers from lack of isolation between the detector and integration capacitor combined with reset switch. The SBDI and SCI schemes also use a differential amplifier in their implementation, which adds to the area and power overhead. An improvised BDI scheme is used in this implementation to achieve better bias stability, low-noise, low area and control on input-resistance through use of a single transistor amplifier feedback as shown in Figure 3.4. Bias currents IBIAS_SINKCT and IBIAS_SOURCECKT can be used to tune the bias voltage

across corner variations. Further the implementation uses bottom plate sampling[19] to mitigate the effects of charge injection on the integration capacitor at the end of integration cycle. Due to area limitations the clocks required for bottom-plate sampling are generated using simple delaying inverters, instead of non-overlapping clock generators. Also this ROIC circuit can operate with detectors that are either p-on-n type or n-on-p type, that source or sink current respectively.

3.2.1. Pins & Functions

Table 3.1 describes the pin outs and their functions in the DROIC unit cell cicruitry.

Pin	Type	Direction	Function
VDET	Analog	I/O	Pin-out to bias the photo-detector node
INT	Digital	I	Control integration time
SOURCE	Digital	I	Control current sourcing/sinking
IBIAS_SOURCECKT	Analog	I	Bias the source circuit
IBIAS_SINKCKT	Analog	I	Bias the sink circuit
COUNTLSB	Digital	I	Control signal to start LSB counting
VBUMP	Analog	I	Bump the integration capacitor voltage
RST	Digital	I	Global capacitor voltage reset

Table 3.1: Table Illustrating the Pins and Their Functions of the DROIC-frontend Circuitry

3.2.2. Integration Capacitor

The value of the integration capacitor decides the well capacity and the reset noise left on the integration capacitor after resetting, due to thermal fluctuations, which is termed Johnson-Nyquist noise[21]. The total reset noise in terms of standard deviation of electrical charge is given as

$$Q_n = \sqrt{K_B T C} \tag{3.3}$$

Where:

$K_B = 1.38064852 * 10^{-23} m^2 kg s^{-2} K^{-1}$, is the boltzmann constant

T = Operating temperature in Kelvin

C = Value of the integration capacitor

A higher value of the integration capacitor helps achieve higher well capacity, however it increases the charge thermal noise on the capacitor. With an integration capacitor of 50fF, the total reset noise due to thermal fluctuations at room temperature of 300K, in terms of standard deviation of electrical charge is about 90 electrons, this is less than 10% of the desired LSB of the DROIC unit cell(1218 electrons), and is a good design value. With a maximum voltage swing of about 1V across the capacitor, the charge capacity of this integration capacitor is about 312000 electrons, combined with the 12-bit counter, the total well capacity is thus 1.278 billion electrons.

3.3. Comparator, Reset & Bias Buffer

A rail-to-rail input comparator is needed for the operation of fine ADC and to support detectors that source or sink current. Also the comparator is required to have low propagation delay to ensure the signal lost during every reset period of the integration capacitor is low. Three stage topology with a pre-amplifier, decision stage and buffer as in [6] offers low propagation delay and also has high sensitivity due to pre-amplifier gain, and helps to keep the offset and gain errors of the coarse ADC low. The reset circuit consists of simple PMOS and NMOS for sinking and sourcing operations respectively. While sinking the capacitor voltage is reset to supply and while sourcing the capacitor voltage is reset to ground. Figure 3.5 shows the implementation of the three stage comparator.

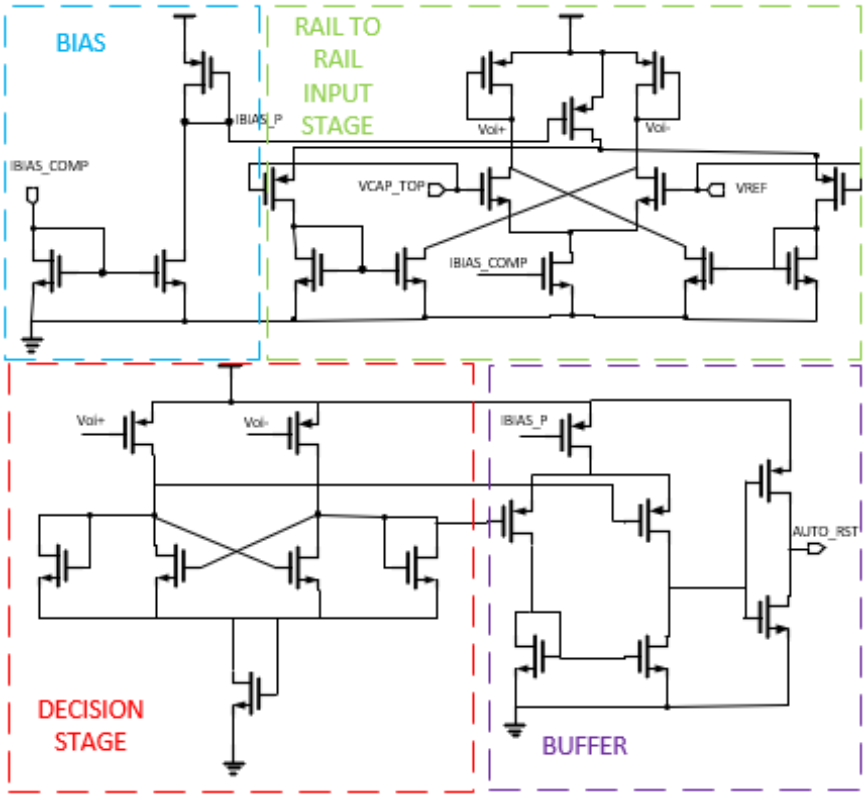

Figure 3.5: Rail-to-rail Input Comparator Implementation

3.3.1. Comparator Pins & Functions

Table 3.2 describes the pin outs and their functions in the comparator.

Pin	Type	Direction	Function
IBIAS_COMP	Analog	I	Pin-out to bias the comparator
VCAP_TOP	Analog	I	+ve input of comparator from integration cap
VREF	Analog	I	-ve input of comparator from reference
AUTO_RST	Digital	O	Digital output of comparator

Table 3.2: Table Illustrating the Pins and Their Functions of the Comparator

Figure 3.6 shows an area efficient multiplexer circuit used to switch the reference of the comparator voltage to 8-bit DAC reference voltage for LSB measurment.

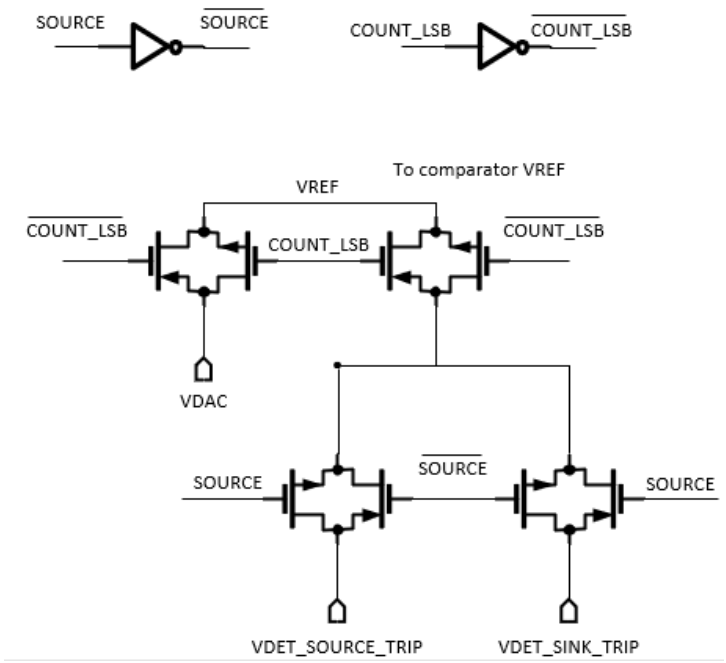

Figure 3.6: Circuit to Switch Reference Voltage of Comparator for LSB Measurement

Table 3.3 shows the pins and their functions exclusive to the VREF switching circuit.

Pin	Type	Direction	Function
VDAC	Analog	I	Input voltage from external 8-bit DAC ramp
VDET_SOURCE_TRIP	Analog	I	Threshold voltage of tripping in source mode
VDET_SINK_TRIP	Analog	I	Threshold voltage of tripping in sink mode

Table 3.3: Table Illustrating the Pins and Their Functions of the VREF Switching Circuit

Figure 3.7 shows the schematic implementation of reset circuit and bias buffer. The reset circuit is meant to auto reset the integration capacitor only during integration. During the LSB measurement phase the auto reset circuit has to be disconnected to leave the capacitor in tri-state. This is performed through a simple transmission gate that tri-states the reset control signal $AUTO\_RST\_OUT$ that goes into the reset circuit when LSB measurement phase is active and connects the comparator output

AUTO_RST to the reset circuit when integration phase is active. Further a bias buffer circuit is essential to maintain the detector bias at the required voltage while integration phase is not active, as the front end circuit is also inoperative. If this isn't done the photodiode bias will swing away from the desired point while not integrating and degrades the response time of the detector during integration. Simple NMOS and PMOS pass gates are implemented to pass on the desired bias voltage onto the detector node in the bias buffer as voltage VDET_SINK is close to ground and voltage VDET_SOURCE is close to supply for the NASA HOT BIRD detector. This effectively reduces the area of the circuit.

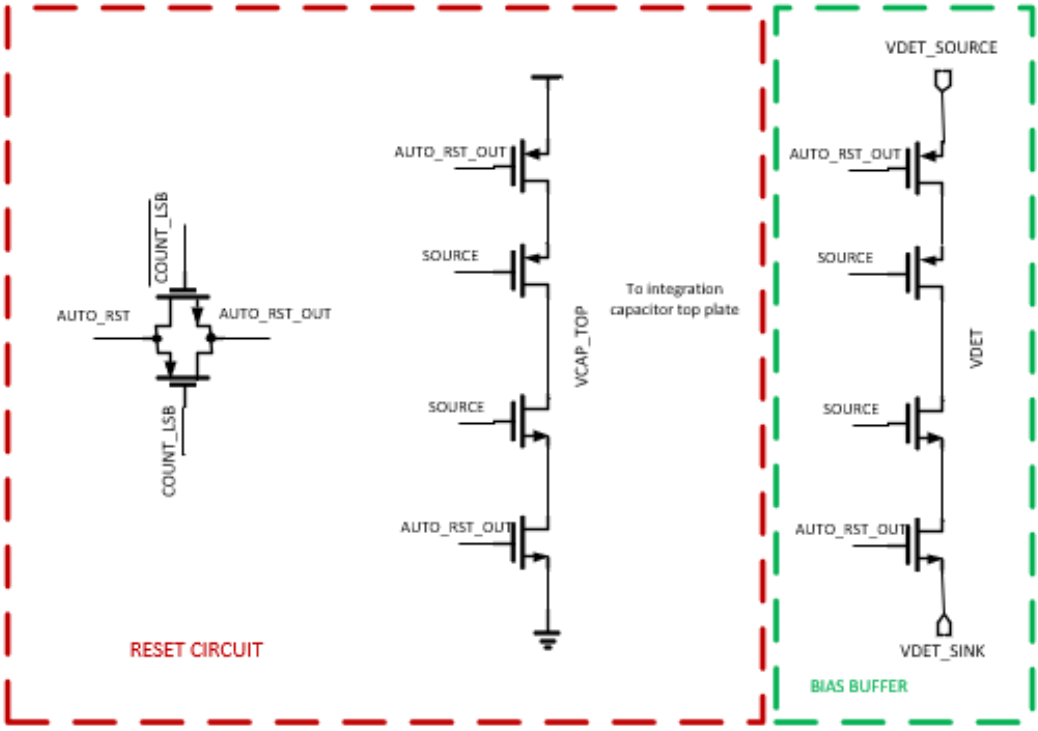

Figure 3.7: Schematic of Reset Circuit and Bias Buffer

3.4. D Flip Flops for Counters

Two important parameters of D-Flip Flops for this application is the transistor count and data holding method: static or dynamic. Since this work uses a low cost 180nm process and pixel pitch is limited to 30μm, the transistor count and the area of the D-Flip Flops used in the counters are required to be small. Several low transistor count D-Flip Flops such as True Single Phase Clock(TSPC) are proposed in [25]. However all these flip flops are of dynamic nature. To enable longer integration times the D-Flip Flops need to be static, that is they should have a positive feedback that holds the data for the required amount of time. Dynamic Flip Flops leak held data over time and are not suitable for this application, where it is desired to achieve integration times of the order of 10ms. Several area and power efficient Single Edge Triggered(SET) D-Flip Flops are proposed in [26]. All the D-Flip Flop circuits in [26] use a Master-Slave configuration and the proposed 12-transistor D-Flip Flop in [26] uses feedback for the slave D latch, but not for the master D latch. This architecture still results in irrecoverable leakage at longer integration times.

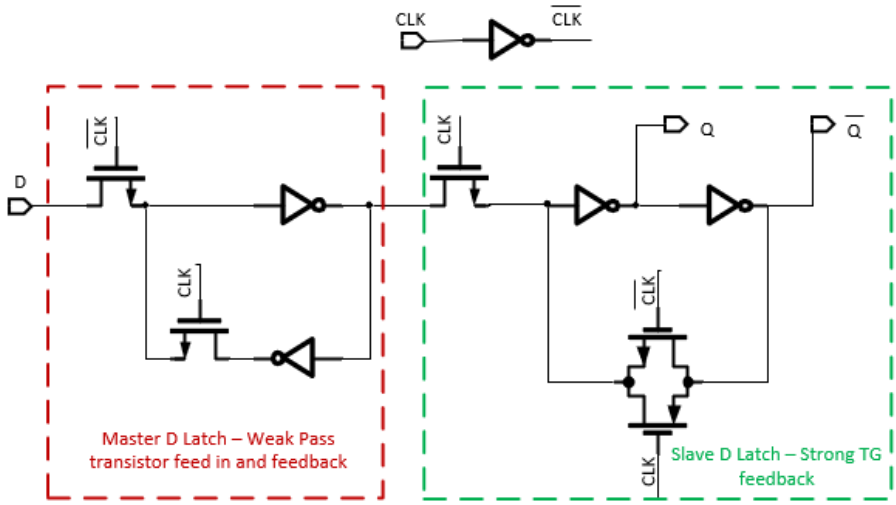

Figure 3.8: Schematic of DFF Implementation

An improved version of this SET D-Flip Flop, which is positive edge triggered, is shown in Figure 3.8, is implemented in this work, which uses a weak pass gate based feedback for the master D-latch and a strong transmission gate based feedback for the slave D-latch, which reduces the noise margin levels at the master D-latch, however it is restored at the slave D-latch. The advantage of this is the area savings that results in using multiples of these D-Flip Flops in the 12-bit counter for the DROIC.

Table 3.4 shows the pins and their functions of the D-Flip Flop circuit

Pin	**Type**	**Direction**	**Function**
D	Digital	I	Input data signal
CLK	Digital	I	Clock to trigger DFF to read and store data
Q	Digital	O	Output of the stored DFF data
$\overline{Q}$	Digital	O	Inverted output of stored DFF data

Table 3.4: Table Illustrating the Pins and Their Functions of the DFF

3.5. 12-bit Counter/Shift-register

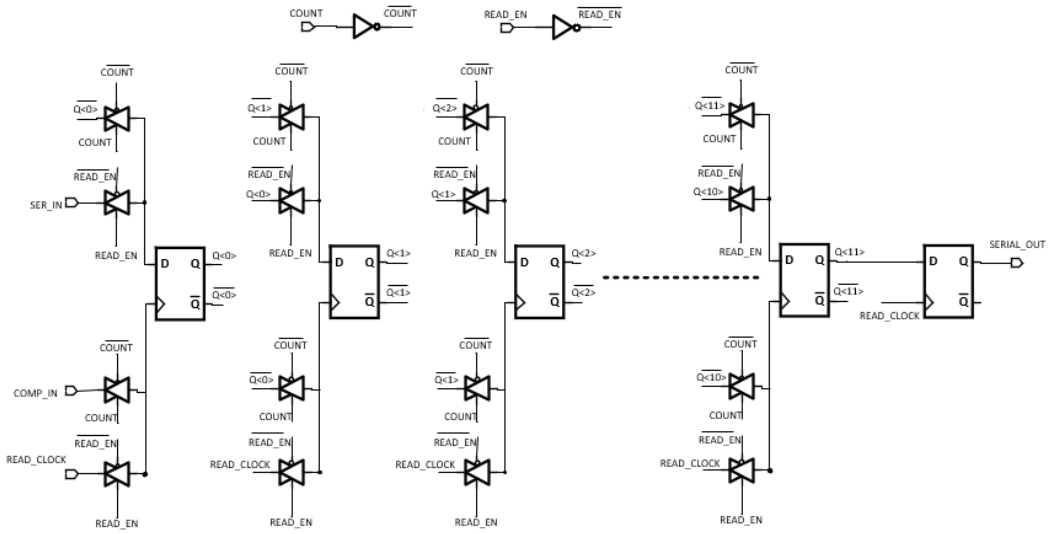

Figure 3.9: Schematic of 12-bit Counter Implementation

The 12-bit counter inside the pixel is meant to count the number of comparator output pulses which is equivalent to the incoming photodetector charge in MSB mode and is also reconfigurable as a right shift register. A synchronous counter architecture needs complex digital logic to count in a binary fashion[11] and adding shift functionality makes it more complex. This adds to the area overhead. An asynchronous/ripple counter can perform binary counting with simple digital logic. Figure 3.9 shows the implemented binary asynchronous counter/shift-register architecture. The complexity of digital circuit is reduced through use of simple 2:1 transmission gate based multiplexer, this reduces the overall area of the 12-bit counter/shift-register implementation. The D Flip Flops shown in the figure are implemented as explained in section 3.4. Table 3.5 shows the pins and their functions of the 12-bit counter/shift-register.

Pin	**Type**	**Direction**	**Function**
COUNT	Digital	I	Enable counting
READ_EN	Digital	I	Enable reading through right shifting
SER_IN	Digital	I	Serial data input in right shift mode
COMP_IN	Digital	I	Input clock pulse to count
READ_CLOCK	Digital	I	Clock input for right shift readout
SERIAL_OUT	Digital	O	Serial data output of counter

Table 3.5: Table Illustrating the Pins and Their Functions of the 12-bit Counter

There is a need for a control circuit to control whether the counter/shift-register is in count mode or right shift mode. Figure 3.10 shows the implementation of the control circuit. The circuit uses a digital clock signal input DAC_CLOCK, which is the same clock that drives the external 8-bit counter, which drives the 8-bit DAC.

The control logic also makes a decision as to whether the counter should count the comparator pulse output in integration mode or if it should count the DAC_CLOCK for the period of time the comparator output is high to measure the LSB.

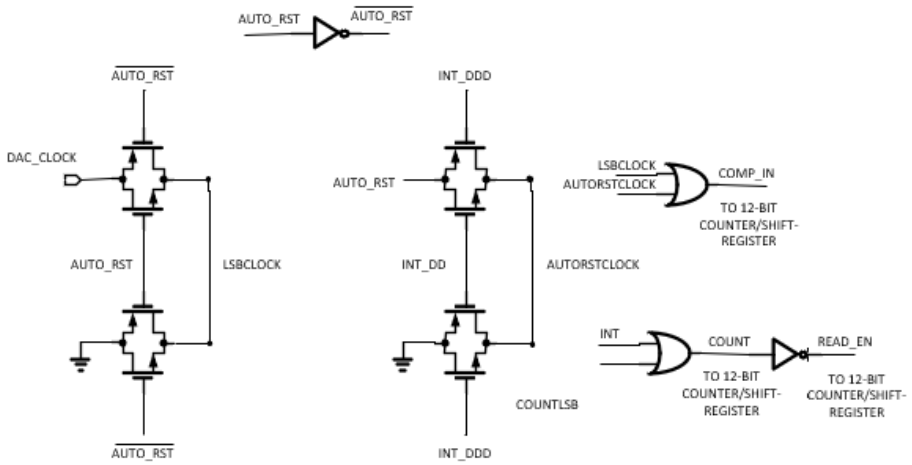

Figure 3.10: Schematic of Control Circuit for the Counter Shift-register

3.6. 8-bit Counter and 8-bit DAC

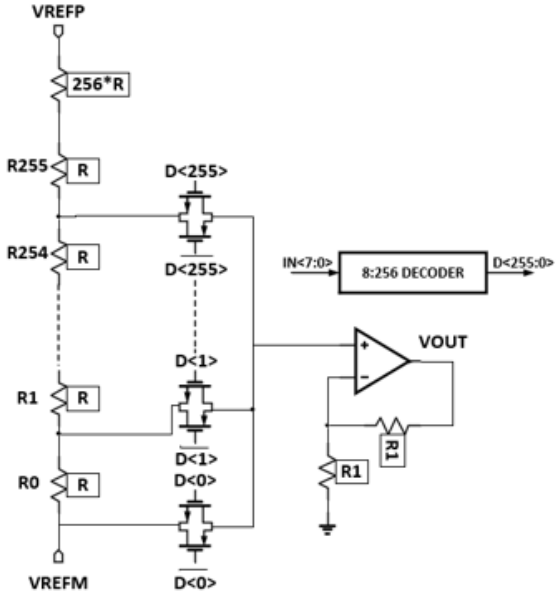

Figure 3.11: Schematic of 8-bit DAC Implementation

The 8-bit up counter uses the same architecture as the 12-bit counter/shift-register, but limited to just 8-bits. The 8-bit DAC is implemented as a resistive string DAC as shown in Figure 3.11. VREFP and VREFM are reference voltage inputs to the DAC. $IN < 7 : 0 >$ is the 8-bit counter data output that feeds the DAC. VOUT is the output voltage of the DAC. This topology is chosen for its simplicity of implementation and lower cost. Further the output of this DAC is guaranteed to be monotonic[3]. That is the output of this DAC always increases or remains constant and never decreases with increasing digital input code. Also for any input code transition only few switches move and thus the glitch energy this DAC consumes is low[3]. However there is a design trade-off to make in this implementation to optimize either noise or power. To ensure the Effective Number Of Bits (ENOB) of this DAC is close to 8 bits, the circuit noise at the output of the DAC should be less than the LSB of the DAC. The 8-bit DAC is allowed to swing 1V, thus its LSB is 3.906mV. The circuit noise at the output of the DAC has to be lesser than this LSB of 3.906mV. This requires small values of resistances in the string DAC to keep the thermal noise low. But smaller values of resistances increase the power consumption of the DAC. So to get the required noise performance this DAC burns significant power. As these DACs are not for every single pixel unit cell but only for every column in the pixel array, the overall power consumption of the entire ROIC cell can be kept low.

3.7. Layout Design

Two parameters need utmost attention in layout design: area and radiation hardening to prevent Single-Event Latchup(SEL). The overall DROIC unit cell area is dominated by the 12-bit counter. The D-Flip Flop used for the 12-bit counter is optimized in terms of transistor count to have only 15-transistors as shown in Figure 3.8. The layout of the D-Flip Flop is also optimized mainly for area.

Figure 3.12 shows implemented layout of the D-Flip Flop. Figure 3.13 shows layout of the 12-bit counter and Figure 3.14 shows the layout of overall unit cell.

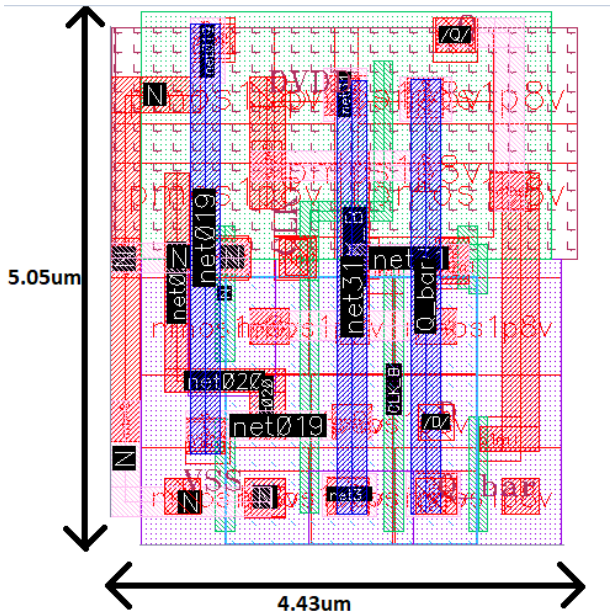

Figure 3.12: Layout of the D Flip Flop

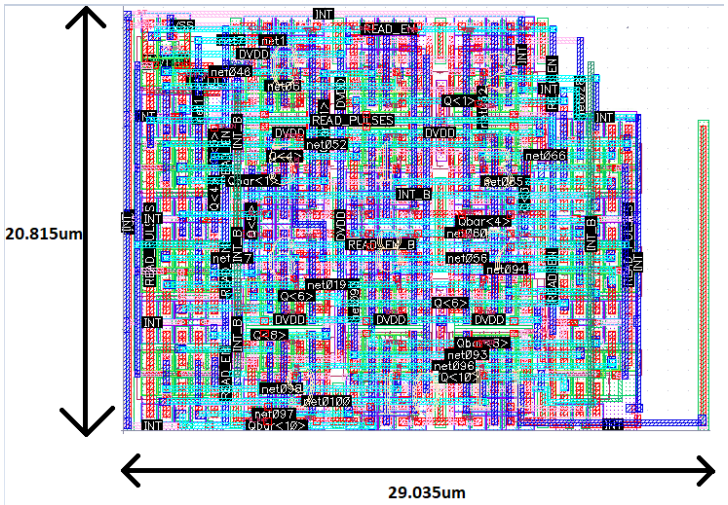

Figure 3.13: Layout of the 12-bit Counter

As seen in Figure 3.14, the 12-bit counter accounts for more than 70% of the DROIC unit cell area which is limited to 30umx30um, and it justifies the effort of

reducing the transistor count in the D Flip Flops used in them. The DROIC unit cell also has a 5umx5um pad to bond it with the detector array, as seen in Figure 3.14. The integration capacitor sits in the topmost metal layers and thus looks overlapping with the 12-bit counter area in the 2D representation of the layout.

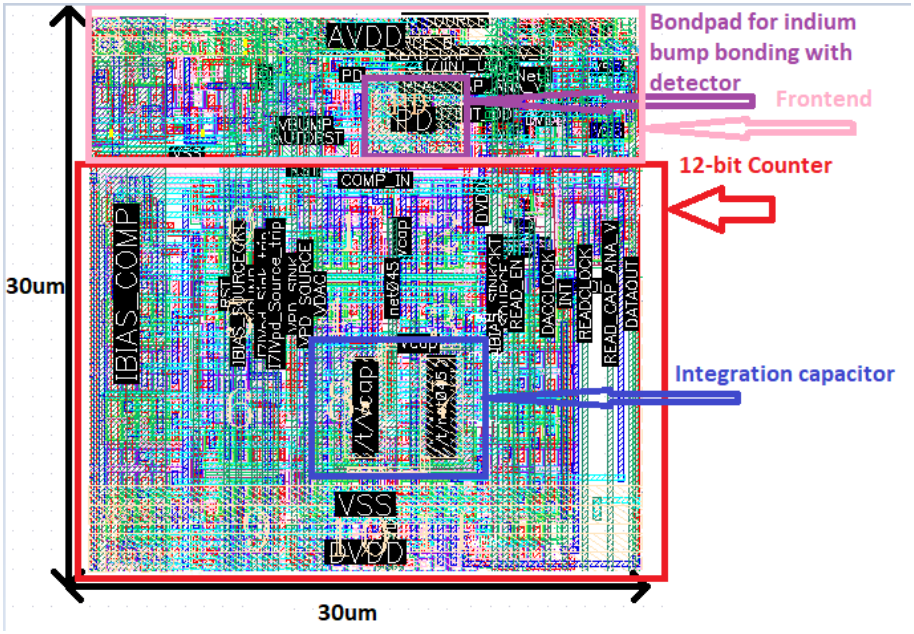

Figure 3.14: Layout of the Overall DROIC Unit Cell

3.7.1. Radiation Hardening

The DROIC unit cell is meant to withstand ionizing radiation in space applications of NASA JPL. Parasitic devices inherent in the CMOS topology may amplify the transient currents in analog and digital CMOS structures that result from incident ionizing radiation[10, 29]. Under certain conditions, the circuit may remain in a high current state after an ionizing particle passes through it, until the circuit is powered down, this is termed Single-Event Latch-up(SEL). SEL occurs when the product of the gains of the parasitic bipolar transistors formed by substrate, well and diffusion becomes greater than one[10].

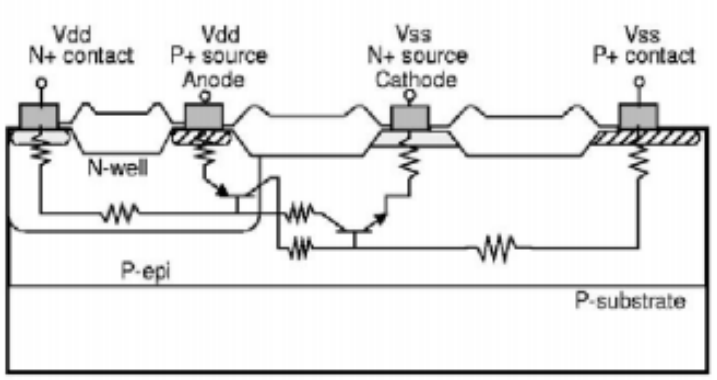

Figure 3.15: Typical CMOS Structure Showing Parasitic Components And Latch-up Path. Image Taken From [10]

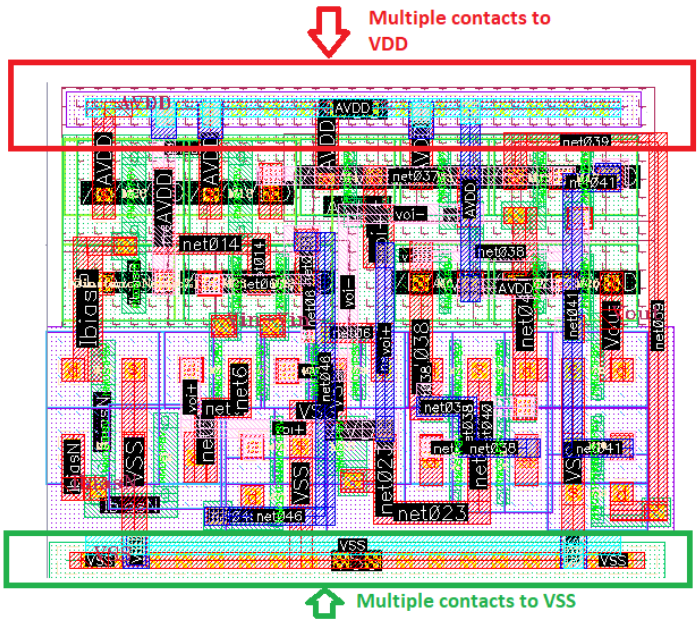

Figure 3.16: Layout of Comparator Illustrating Multiple Supply Contacts to Mitigate SEL

These parasitic bipolar transistors are off during normal operation, however they may be turned on by transient currents resulting from ionizing radiation. Figure 3.15 shows the parasitic bipolar transistors and their relation to CMOS structures. Majority carriers flow through wells, substrates and cause voltage drops that can turn on the parasitic bipolar transistors. Reducing the resistances along the ohmic paths shown in 3.15 will reduce the sensitivity of the structure to latch-up[29].

This is normally done through adding multiple contacts to supply(Vdd) and ground(Vss). Figure 3.16 illustrates the layout of the comparator used in the DROIC unit cell that implements multiple supply contacts to mitigate SEL. The number of contacts required depends on the expected amount of transient currents resulting from ionizing radiation.

Chapter 4

SIMULATION RESULTS

4.1. DROIC Front-end Performance

The NASA MWIR InAs/InAsSb HOT BIRD detector can operate at bias voltages from -1 to 1V, as shown in Figure 4.1.

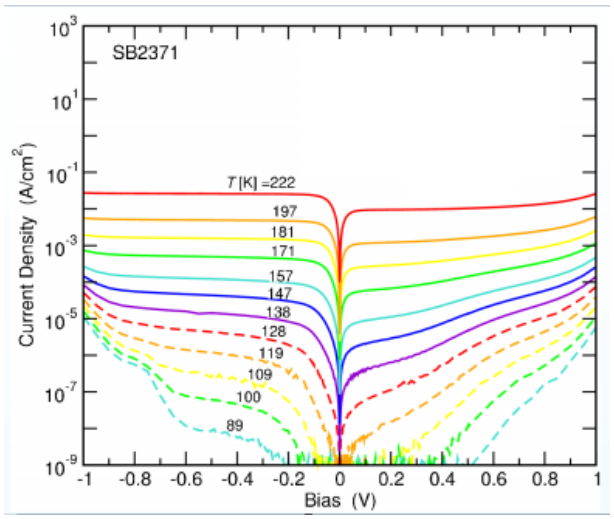

Figure 4.1: Current Density of the NASA HOT BIRD Detector vs. Bias Voltage[1]

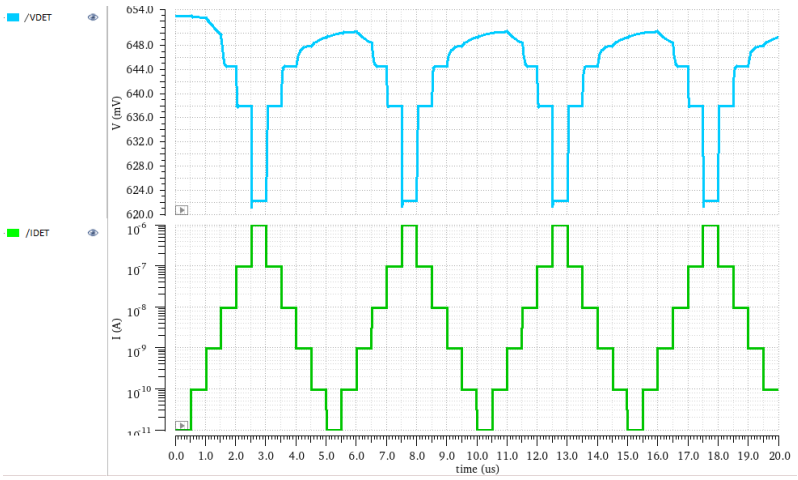

Figure 4.2: Transient Response VDET Vs IDET, While Sinking Current at 150k

HOT BIRD detector is mainly operated at 150K[1], and to obtain near maximum current density at that temperature a bias of 0.25V is sufficient as seen in Figure 4.1. The detector common node voltage is usually held at mid supply of 900mV, and when the detector node VDET is 0.25V below this voltage, that is at 650mV the detector sinks current and when it is 0.25V above, that is at 1.15V the detector sources current. Figure 4.2 shows the transient response of the detector bias voltage VDET, at steps of the detector current IDET, in the typical process corner, while sinking current at a bias of around 650mV and at a temperature of 150K. The overall bias variation seen is $\pm 15mV$ across the entire current range of 10pA to 1uA.

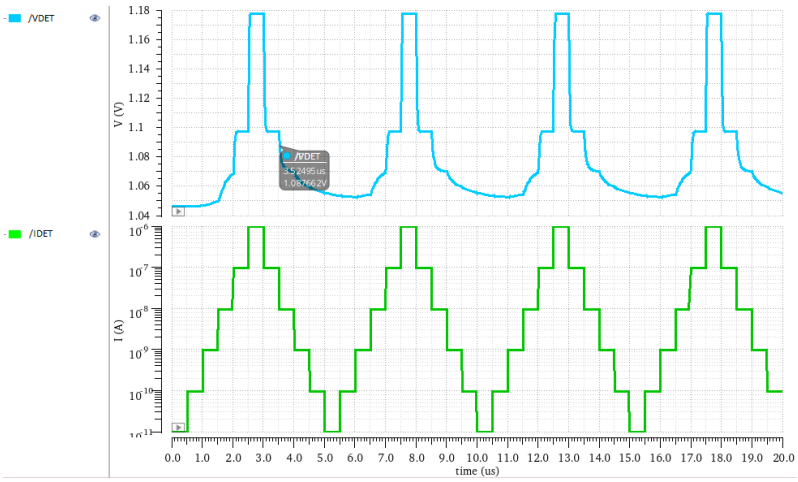

Figure 4.3: Transient Response VDET Vs IDET, While Sourcing Current at 150k

Figure 4.3 shows the transient response of the detector bias voltage VDET, at steps of the detector current IDET, in the typical process corner, while sourcing current at a bias of around 1.15V and at a temperature of 150K. The overall bias variation seen is $\pm 65mV$ across the entire current range of 10pA to 1uA. The sourcing circuit of the ROIC has less control on the bias compared to sinking circuit. This is due to lesser mobility and hence lesser gm of the PMOS transistors used in the sourcing circuits compared to the NMOS transistors used in the sinking circuits. Area limitations limit the achievable gm from the PMOS sourcing circuits.

Figure 4.4 shows a plot of the DROIC input resistance vs frequency across various detector currents from 10pA-1uA, at 150K while sinking current. Figure 4.5 shows a plot of injection efficiency vs detector current assuming a detector resistance of $350M\Omega$ for high sensitivity applications[12]. A drawback of the DI architecture is that its input resistance and thus injection efficiency is dependent on detector current at low background currents.

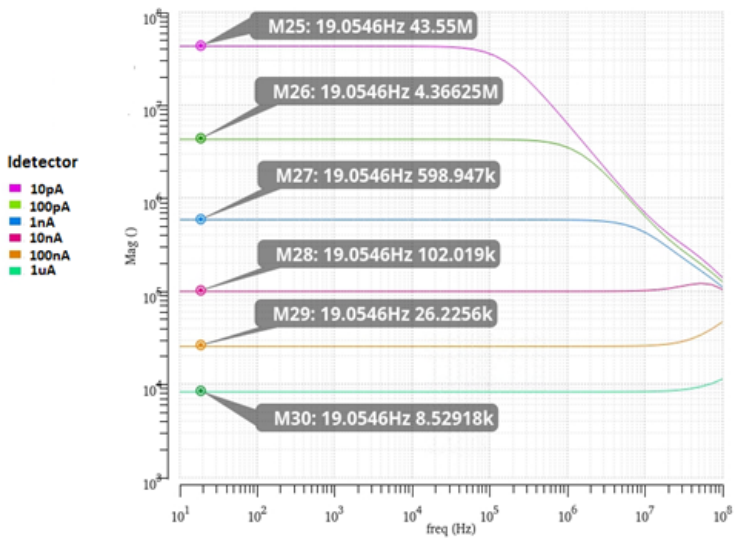

Figure 4.4: Input Resistance of the DROIC Unit Cell, While Sinking

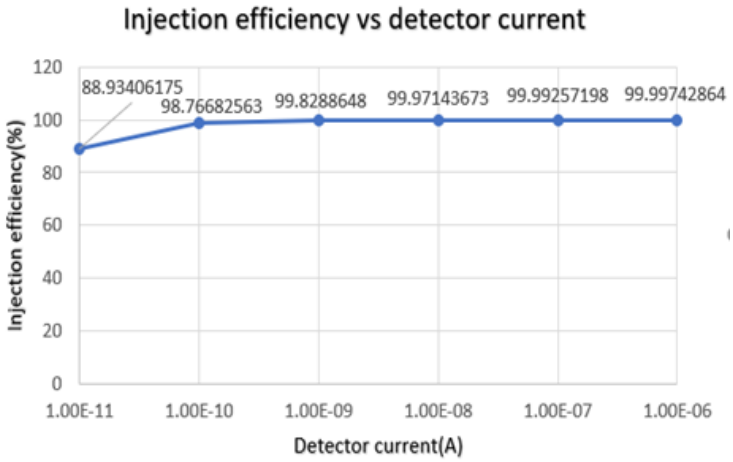

Figure 4.5: Injection Efficiency of DROIC Unit Cell, While Sinking

Figure 4.6 shows a plot of the DROIC input resistance vs frequency across various detector currents from 10pA-1uA, at 150K while sourcing current. Figure 4.7 shows a plot of injection efficiency vs detector current assuming a detector resistance of $350M\Omega$. Similar to bias performance, injection efficiency performance of the source circuit is degraded compared to the sink circuit due to low mobility and thus gm of PMOS devices, also limited by area constraints.

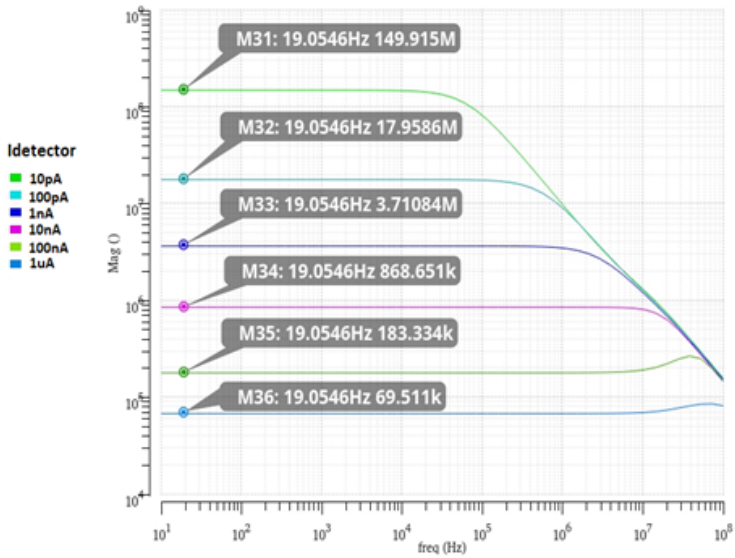

Figure 4.6: Input Resistance of the DROIC Unit Cell, While Sourcing

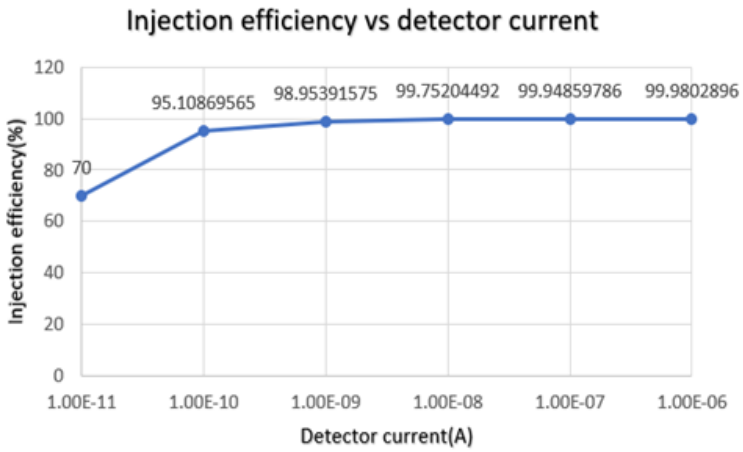

Figure 4.7: Injection Efficiency of DROIC Unit Cell, While Sourcing

Figure 4.8 shows the static noise performance of the DROIC front-end. This does not include any switching noise or reset thermal noise. The static noise is dominated by MOS flicker noise. The RMS integrated noise on the integration capacitor in 1MHz bandwidth is 475.6uV, which corresponds to $\sim 150e-$, this is about 15% of the LSB of 1218 electrons. This noise can be reduced by increasing the width of the transistors[23] used in the front-end circuit, however it results in an increased area.

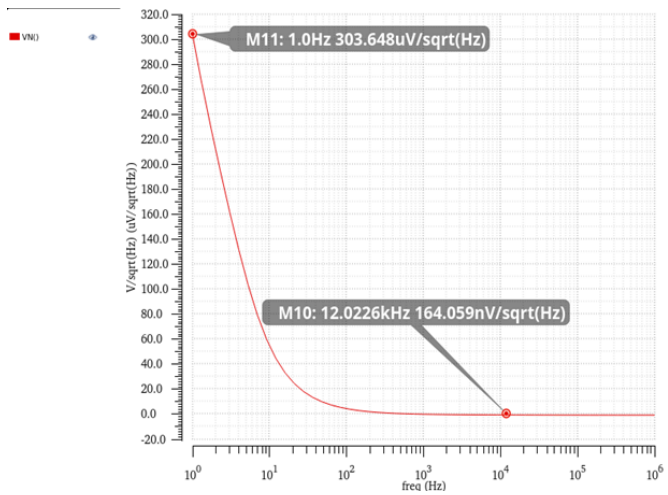

Figure 4.8: Static Noise of the DROIC Front-end

4.2. Comparator Performance

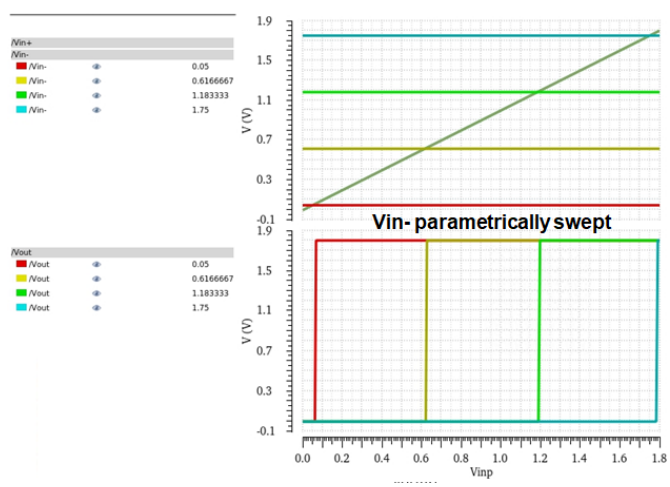

Figure 4.9: Rail-to-rail Comparator Common Mode

As discussed in section 3.3 the comparator should have a near Rail-to-Rail input common mode and low propogation delay. Figure 4.9 illustrates the common mode performance of the implemented comparator.

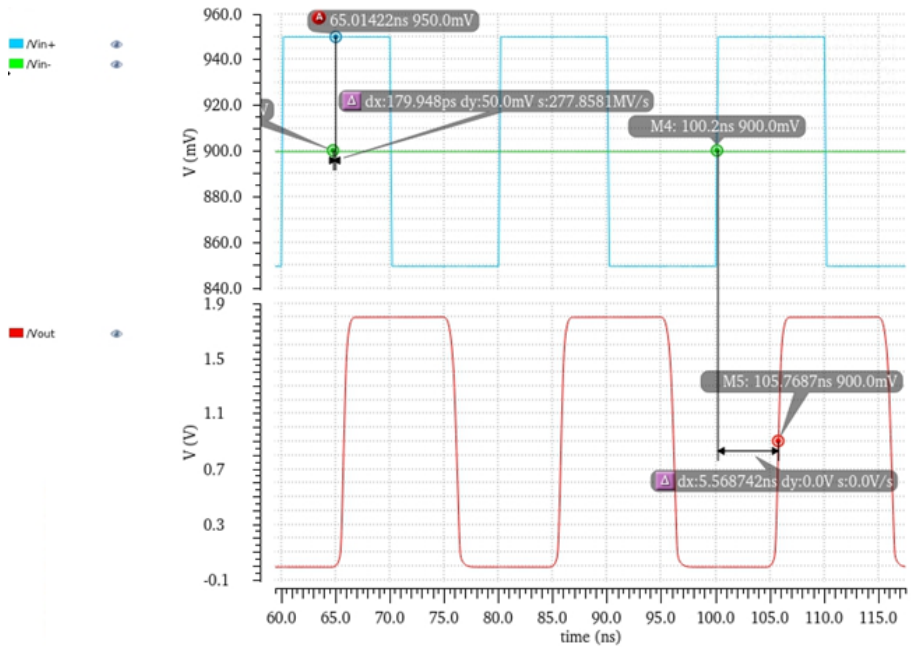

Figure 4.10: Simulation Illustrating the Propagation Delay of the Comparator

Figure 4.10 shows the propagation delay of the implemented comparator as 5.6ns with an overdrive of 50mV. This enables integration times to be as small as $2^{12} * 5.6ns \sim= 25us$, with 2us of buffer time for readout. Smaller propagation delays reduce the amount of signal lost during the auto reset period of the integration capacitor.

4.3. DAC Performance

Noise at the output of the 8-bit DAC affects the ENOB of the DAC. If the noise level is greater than the LSB of the DAC, the ENOB starts to reduce from the ideal 8-bits and this affects the dynamic range of the entire DROIC unit cell. RMS integrated output referred noise of the DAC is 382.7uV in a bandwidth of 1MHz, which is about 10% of the DAC LSB of 3.9mV.

DAC output noise is dominated by the thermal noise of the resistive string and flicker noise of the gain stage.

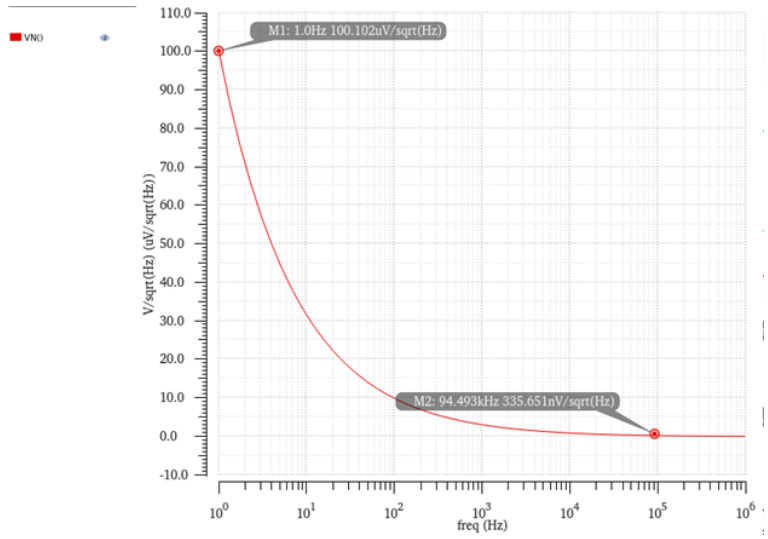

Figure 4.11: Simulation Illustrating the Noise at Output of DAC

4.3.1. DAC Linearity

Figure 4.12 shows the DNL and INL performance of the DAC. It has a DNL of ±0.1 LSB and an INL of 2.5 LSB. The effective number of bits obtained from the DAC is 7.98 bits at the schematic level.

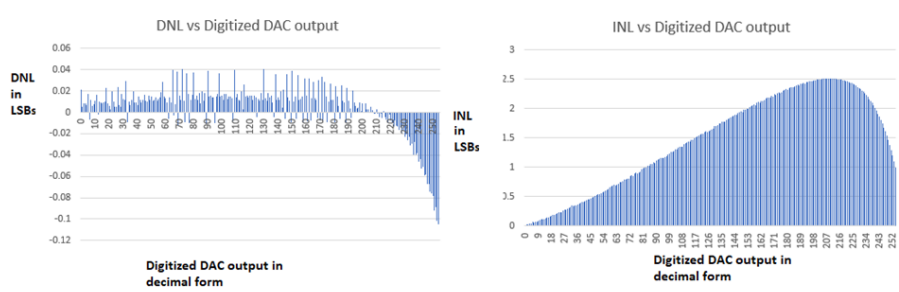

Figure 4.12: Simulation Illustrating the Linearity of DAC

4.4. D Flip Flop Operation

Figure 4.13 shows waveforms from simulating the implemented D flip flop.

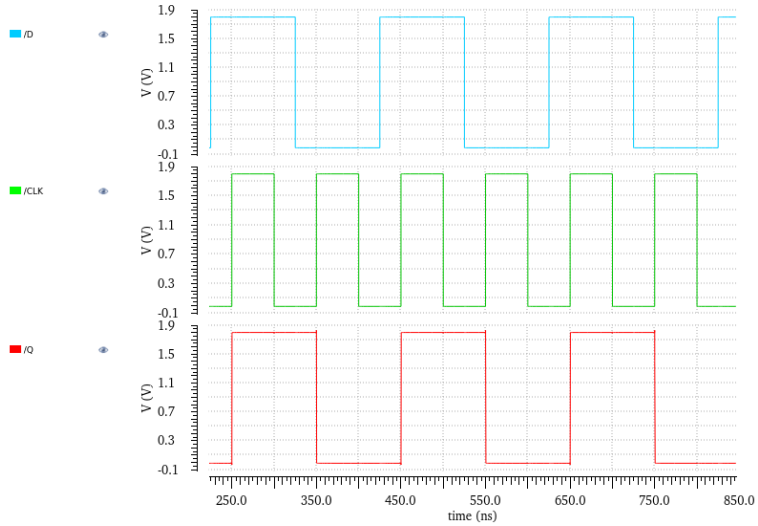

Figure 4.13: Simulation Illustrating the Operation of the D Flip Flop

4.5. 12-bit Counter Operation

Figure 4.14 shows the operation of the 12-bit counter.

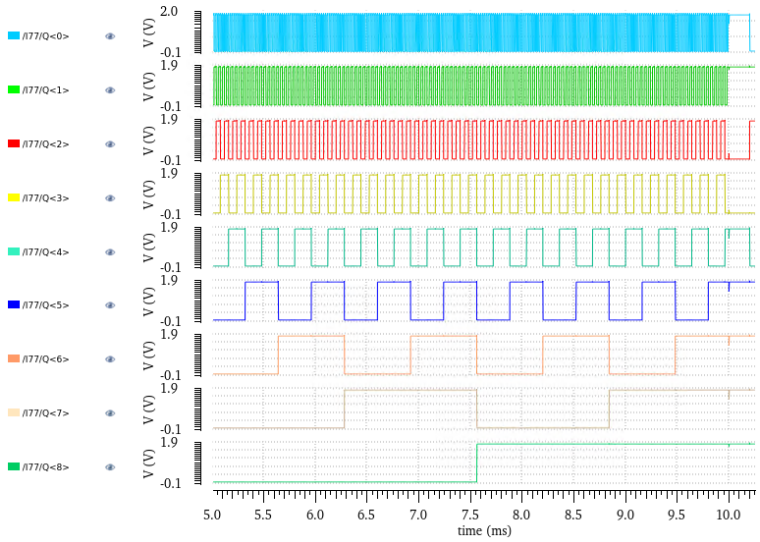

Figure 4.14: Simulation Illustrating the Operation of the Counter

4.6. Frontend Linearity

Figure 4.15 shows the DNL performance of the I to F converter. It has a DNL of $\pm 0.2LSB$.

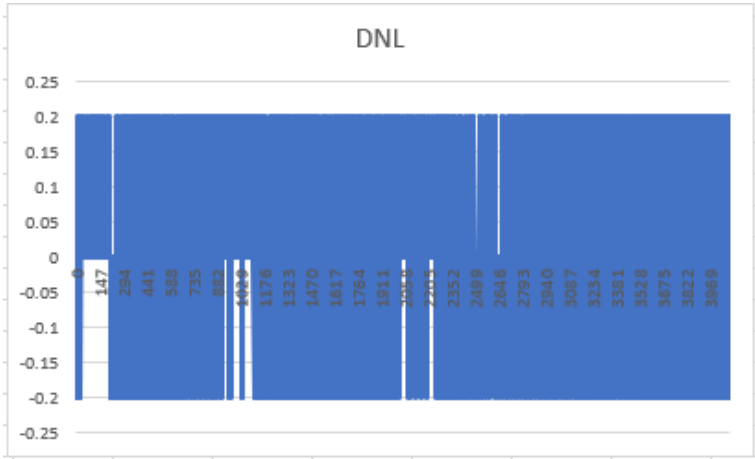

Figure 4.15: Simulation Illustrating the DNL of the Frontend

Figure 4.16 shows the INL performance of the I to F converter. It has a INL of 5.75LSB. The effective number of bits of the 12-bit I to F converter is 11.73 bits.

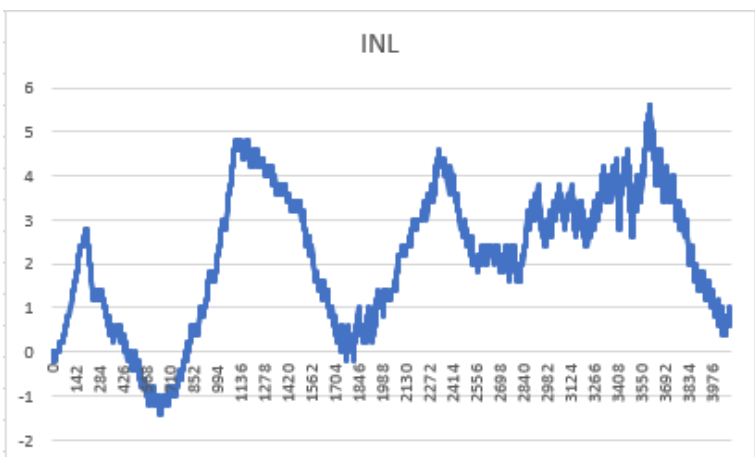

Figure 4.16: Simulation Illustrating the INL of the Frontend

4.7. Frontend Operation

Figure 4.17 shows the operation of the DROIC unit cell with an integration time of 200us, corresponding to a frame rate of 5KHz, which is the maximum frame rate of this DROIC. At this rate only the MSB mode is operating and LSB mode is switched off. Figure 4.18 shows the operation of the frontend circuit with an integration time as large as 5ms.

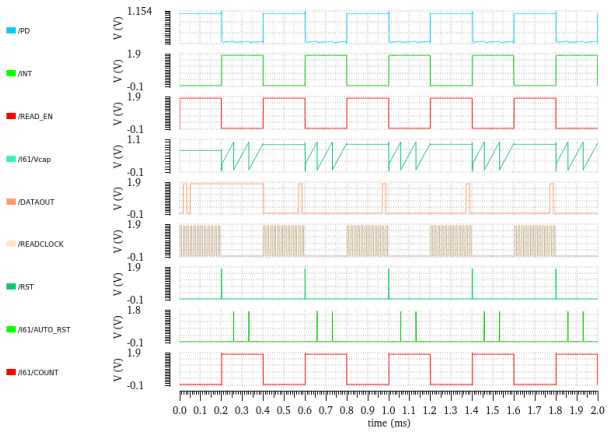

Figure 4.17: Simulation Illustrating the Operation of the Frontend with an Integration Time of 200us.

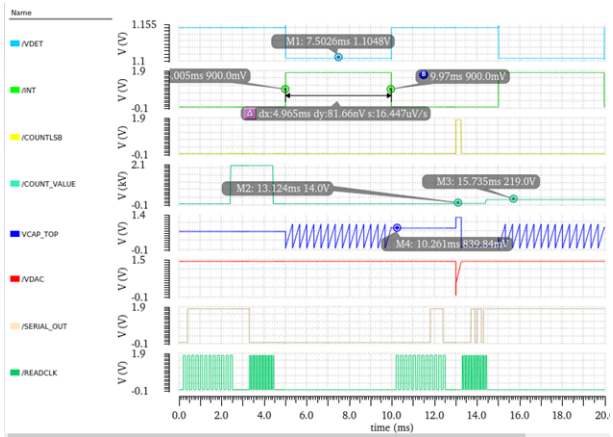

Figure 4.18: Simulation Illustrating the Operation of the Frontend with an Integration Time of 5ms.

4.8. Overall DROIC Performance

Table 4.1 shows the worst case achieved performance of the overall DROIC unit cell across corners at the schematic level.

Parameter	**Value**
Process	180nm
Pixel pitch	30μm
ENOB	19.7
Digital count(LSB electrons)	1285 electrons
Well capacity(electrons)	1.12 billion
Input current range	33pA-1.25uA
Detector resistance(Rd)	350MΩ
Bias variation	$\pm 74mV$
Integration time	200us-5ms
Injection efficiency	67% worst case at slow corner and 33pA IDET
Non-linearity	0.15% INL
Noise on integration capacitor	373e-
Power	7.2uW over 5ms of integration

Table 4.1: Overall DROIC Performance

Chapter 5

CONCLUSION

This thesis work gave a background on IR radiation, IR imaging systems, IR detectors, FPA and ROICs. Further following tasks were accomplished

1) A new coarse ADC + fine ADC based DROIC unit cell architecture to improve the dynamic range, well capacity and sensitivity was proposed.
2) Comparison of several DROIC front-end architectures such as DI, BDI and CTIA were done and a new DROIC front-end circuit was proposed to improve bias stability across a wide input current range.
3) Several common circuits such as D-Flip Flops, Counter/Shift-Registers, and DACs were implemented from scratch to be area efficient.

As a future extension of this research work a 640x512 DROIC unit cell array will be developed and fabricated by the team at Alphacore. This can be later hybridized with the NASA HOT-BIRD detector and its performance can be evaluated.

REFERENCES

[1] https://esto.nasa.gov/forum/estf2019/presentations/gunapala_s1p3_estf2019.pdf.

[2] https://flir.netx.net/file/asset/12702/original.

[3] https://training.ti.com/precision-dacs-string.

[4] http://www.columbia.edu/∼vjd1/electromag_spectrum.htm.

[5] M. Nurul Abedin, Ishwara B. Bhat, Sarath D. Gunapala, Sumith V. Bandara, Tamer F. Refaat, Stephen P. Sandford, and Upendra N. Singh. The future of single- to multi-band detector technologies: Review. 2006.

[6] R.J. Baker. *CMOS: Circuit Design, Layout, and Simulation*. IEEE Press Series on Microelectronic Systems. Wiley, 2019.

[7] Chih-Cheng Hsieh, Chung-Yu Wu, Far-Wen Jih, and Tai-Ping Sun. Focal-plane-arrays and cmos readout techniques of infrared imaging systems. *IEEE Transactions on Circuits and Systems for Video Technology*, 7(4):594–605, Aug 1997.

[8] Christian Detter, D Russ, A Iffland, S Wipper, MO Schurr, H Reichenspurner, G Buess, and B Reichart. Near-infrared fluorescence coronary angiography: a new noninvasive technology for intraoperative graft patency control. In *Heart Surgery Forum*, volume 5, pages 364–369. FORUM MULTIMEDIA PUBLISHING, 2002.

[9] Semiconductor Devices. http://www.scd.co.il/scd/templates/showpage.asp?dbid=1&lngid=1&tmid=84&fid=1319.

[10] J. M. Hutson, R. D. Schrimpf, and L. M. Massengill. The effects of scaling and well and substrate contact placement on single event latchup in bulk cmos technology. In *2005 8th European Conference on Radiation and Its Effects on Components and Systems*, pages PC24–1–PC24–5, Sep. 2005.

[11] R. Katreepalli and T. Haniotakis. Energy-efficient synchronous counter design with minimum hardware overhead. In *2017 International Conference on Communication and Signal Processing (ICCSP)*, pages 1423–1427, April 2017.

[12] Kenneth I. Schultz, Michael W. Kelly, Justin J. Baker, Megan H. Blackwell, Matthew G. Brown, Curtis B. Colonero, Christopher L. David, Brian M. Tyrrell, and James R. Wey. Digital-pixel focal plane array technology. *LINCOLN LABORATORY JOURNAL*, 20(2):36–51, 2014.

[13] Hamamatsu Photonics K.K. Infrared detectors, 2019. Cat. No. KIRD0001E13.

[14] KQED. https://www.kqed.org/science/1220591/heat-seeking-drones-could-reduce-fire-deaths.

[15] S. C. Liew. Electromagnetic waves, Retrieved 2006-10-27. Centre for Remote Imaging, Sensing and Processing.

[16] Henk Martijn, Urban Halldin, Per Helander, and Jan Y. Andersson. A 640 by 480 pixels readout circuit for ir imaging. *Analog Integrated Circuits and Signal Processing*, 22(1):71–79, Jan 2000.

[17] Miller and Friedman. Photonic rules of thumb, 2004.

[18] Y. Montembeault, P. Lagueux, V. Farley, A. Villemaire, and K. C. Gross. Hypercam: Hyperspectral ir imaging applications in defence innovative research. In *2010 2nd Workshop on Hyperspectral Image and Signal Processing: Evolution in Remote Sensing*, pages 1–4, June 2010.

[19] D. Osipov and S. Paul. Flying-capacitor bottom-plate sampling scheme for low-power high-resolution sar adcs. In *2018 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)*, pages 1–4, Oct 2018.

[20] R. L. Petritz. Fundamentals of infrared detectors. *Proceedings of the IRE*, 47(9):1458–1467, Sep. 1959.

[21] R. Sarpeshkar, T. Delbruck, and C. A. Mead. White noise in mos transistors and resistors. *IEEE Circuits and Devices Magazine*, 9(6):23–29, Nov 1993.

[22] Raghvendra Sahai Saxena, Navneet Kaur Saini, R.K. Bhan, and R.K. Sharma. A new circuit model of hgcdte photodiode for spice simulation of integrated irfpa. *Infrared Physics & Technology*, 67:58 – 62, 2014.

[23] Y. Seo, C. Woo, M. Lee, M. Kang, J. Jeon, and H. Shin. Improving bsim flicker noise model. In *2019 Electron Devices Technology and Manufacturing Conference (EDTM)*, pages 2421–2426, March 2019.

[24] Sean E. Shaheen, Christoph J. Brabec, N. Serdar Sariciftci, Franz Padinger, Thomas Fromherz, and Jan C. Hummelen. 2.5% efficient organic plastic solar cells. *Applied Physics Letters*, 78(6):841, Feb 2001.

[25] J. Shaikh and H. Rahaman. High speed and low power preset-able modified tspc d flip-flop design and performance comparison with tspc d flip-flop. In *2018 International Symposium on Devices, Circuits and Systems (ISDCS)*, pages 1–4, March 2018.

[26] M. Sharma, A. Noor, S. C. Tiwari, and K. Singh. An area and power efficient design of single edge triggered d-flip flop. In *2009 International Conference on Advances in Recent Technologies in Communication and Computing*, pages 478–481, Oct 2009.

[27] P. Song, Z. Ye, W. Hu, and X. Hu. Injection efficiency of di and ctia readout integrated circuit. In *2015 International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD)*, pages 81–82, Sep. 2015.

[28] FLIR Systems. Technical note: Cooled vs uncooled thermal imaging, 2015.

[29] R. R. Troutman. Latchup in cmos technologies. *IEEE Circuits and Devices Magazine*, 3(3):15–21, May 1987.

APPENDIX A

VERILOGA CODES

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A.1. Photodiode Model Code

```
`include "constants.vams"
`include "disciplines.vams"

nature Efield
units = "E";
access = E;
`ifdef EPHASE_ABSTOL
abstol = `EPHASE_ABSTOL;
`else
abstol = 1e-6;
`endif
endnature

discipline optical
potential Efield;
Enddiscipline

module Photodiodemodel(optgnd, vtop, vbot, inlig);
parameter real Rspvty = 1e-6;
parameter real Rdark = 350e6;
parameter real Wi = 700e-9;
parameter real len = 100e-6;
parameter real wid = 10e-6;
parameter real Is = 1e-14;
parameter real Rs = 1e3;
input [0:1] inlig;
inout optgnd, vtop, vbot;
electrical vtop, vbot;
optical [0:1] inlig, optgnd;
branch (vtop, vbot) res, cap, photo;
real Optmag, ehotbird, Cj;
integer direction = -1;
ehotbird = 16 *`P_EPS0;
Cj = ehotbird*len*wid/Wi;
I(cap) <+ ddt(Cj * V(cap));
I(res) <+ Is*(limexp(V(res)/($vt))-1);
Optmag = E(inlig[1], optgnd)*E(inlig[1], optgnd)+
    E(inlig[0], optgnd)*E(inlig[0], optgnd);
I(photo) <+ direction*Rspvty*Optmag+V(photo)/Rdark;
end
endmodule
```