Nickel Silicide Contact for Copper Plated Silicon Solar Cells

by

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ABSTRACT

Nickel-Copper metallization for silicon solar cells offers a cost effective alternative to traditional screen printed silver paste technology. The main objective of this work is to study the formation of nickel silicide contacts with and without native silicon dioxide SiO_2. The effect of native SiO_2 on the silicide formation has been studied using Raman spectroscopy, Rutherford backscattering spectrometry and sheet resistance measurements which shows that SiO_2 acts as a diffusion barrier for silicidation at low temperatures of 350°C. At 400°C the presence of SiO_2 results in the increased formation of nickel mono-silicide phase with reduced thickness when compared to samples without any native oxide. Pre and post-anneal measurements of Suns Voc, photoluminescence and Illuminated lock in thermography show effect of annealing on electrical characteristics of the device. The presence of native oxide is found to prevent degradation of the solar cells when compared to cells without any native oxide. A process flow for fabricating silicon solar cells using light induced plating of nickel and copper with and without native oxide (SiO_2) has been developed and cell results for devices fabricated on 156mm wafers have been discussed.

DEDICATION

To my Mother and
Father

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I would like to thank my adviser Dr. Stuart Bowden for giving me the opportunity to work at Solar Power Lab (SPL). With Dr. Bowden's guidance I have learnt a lot about solar cell characterization. I would like to thank William Dauksher who is our research lab manager and a process engineer. He has helped greatly in installing tools and making protocols to ensure smooth functioning of the lab. He has always been available to discuss new ideas & design of experiments.

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CHAPTER 1

INTRODUCTION

Motivation

In the last decade the cost to install solar panel has dropped by more than 70% which has opened up new markets for deployment of solar energy[1]. In the US it is predicted that by the year 2021 it will have 100GW of cumulative solar installed capacity[2]. It can be said that the cost of solar is going to be important factor involved in the future of the solar industry. One of the major components in solar cell manufacturing is the cost of silver paste metallization. For best practice wafer to cell cost is 0.20$/$W_p$ and typical solar paste cost is 0.09$/$W_p$ and typical consumption on 156mm wafer is 300mg of silver paste[3]. The rapidly reducing cost of various other components and processes over the years has made silver paste second most expensive material after the wafer cost in current technology of c-silicon solar cell. The silver paste price is controlled mainly by the prices of silver in the international market. Silver prices have been very volatile ranging from 500 to 1400US$/kg during the last 5 years[4]. According to ITRPV on average there is 120mg/cell of silver and the aim of the industry is to further reduce this value to 40mg/cell by 2025[5]. In 2011, the photovoltaic industry consumed 11% of the worlds silver production[4]. More recently in 2015 the demand for silver in PV increased by 23% from previous year[6]. The volatile nature of silver as commodity and its availability cause uncertainties in the pricing and cost evaluation of the technology. In the future if solar energy has to reach the terawatt scale the solar industry will use up a significant amount of the world silver supply at the current consumption rate. Thus for sustainable growth of solar energy in the future, it is necessary to explore

alternative metallization schemes which have similar performance, abundant and cheaper.

Nickel-Copper metallization by plating offers a method for obtaining high efficiency solar cells at a low cost. The price of Copper has been in the range of 3 to 10$/kg during the last decade which is more than 100x reduction as compared to silver price[7]. Fine linewidths <30μm can be achieved by using femto-second laser to pattern the dielectric for contact opening this results in lower optical shading losses[8]. Metallic copper having close to bulk conductivity can be deposited reducing the series resistance. The formation of good ohmic contact with Nickel can be achieved by annealing at low temperatures of 400°C further reducing resistive losses. All these factors contribute to improvement of the solar cell efficiency while at the same time reducing the cost of the raw material involved.

There are a few challenges associated with the Ni-Cu plating technique that have prevented its implementation in industry. Achieving good adhesion of copper contacts to silicon is challenging. Copper is a fast diffusion species in silicon and forms recombination centers[9]. A good ohmic contact is required at Ni-Si interface to reduce series resistance. The above challenges can be solved by forming a silicide layer at Ni-Si interface. During formation of NiSix may spike through the junction and cause shunts or increase metal induced recombination. This results in general deterioration of electrical properties of the cell. In this work the formation and characterization nickel silicide is studied and how to mitigate its effects on electrical properties.

Aim of Thesis

A new processing method is proposed and evaluated for the fabrication of Ni-Cu metallization for solar cells. The aim of this work is to study the contact formation of

nickel silicide and its effects on the electrical and mechanical properties of the solar cell device with and without a native oxide on the silicon surface. It is important to understand the formation of nickel silicide layer and its properties to develop a process for Ni-Cu plated front contacts. Conventionally for most plating processes some pretreatment is required to remove the native oxide formed to get a clean interface between metal and semiconductor. In this work the native oxide is intentionally left on the surface and its effects on the formation of contacts are studied using sheet resistance, Raman, Rutherford backscattering characterization & Suns Voc techniques. Finally, cell results fabricated using the native oxide and its effects on the process have been discussed.

Thesis Outline

The thesis is presented in 5 chapters. Chapter 2 covers an overview of silicon solar cell fundamentals, nickel copper metallization, simulation results and overview of light induced plating method. Chapter 3 covers experiments and results on nickel silicide characterization using sheet resistance, Raman spectroscopy and Rutherford backscattering. Chapter 4 focusses on the results obtained from Suns Voc, photoluminescence & Illuminated lock in thermography. Here the effects of native silicon dioxide on pFF of solar cell are discussed. Contact resistance adhesion and a summary of the results of solar cell devices fabricated are also presented. Finally, Chapter 5 covers the future works and conclusions.

CHAPTER 2

BACKGROUND LITERATURE

Solar Cell Fundamentals

A solar cell is a photovoltaic device that converts the sunlight into electricity. The incident light produces a current and also generates a potential, the electron hair pairs are then separated. The band gap of Si is 1.1eV and any photon that has energy ≥1.1eV can be absorbed and could result in the excitation of electrons from valence band to conduction band. This process results in the generation of electron hole pairs in the semiconductors. The separation of carriers is due to the presence of the p-n junction which causes the movement of electrons towards the n-type side and the holes to the p-type side. The charge is then collected by front and rear contacts which can be connected to an external load.

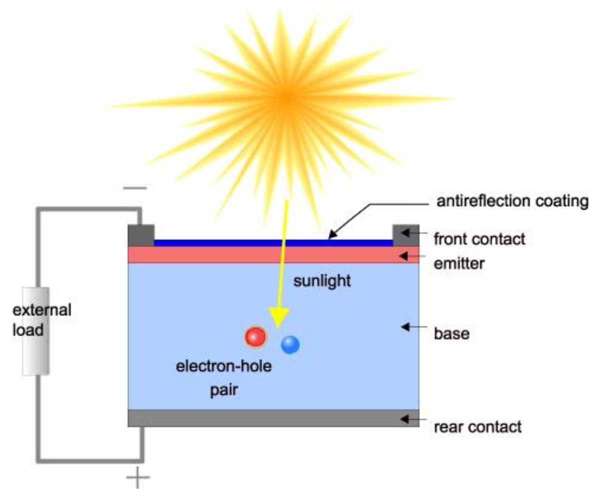


Figure 1 Cross-section of a Solar Cell [10].

Screen Printing

Metallization of solar cells enables the collection of light generated current. Silver paste metallization using screen printer has been used widely across the industry for the last few decades. It is easy to implement and is well understood by the industry.

Yet there are a few challenges associated with silver paste. The bulk conductivity of silver paste is 2-3 times when compared to pure silver[11][12]. It is very challenging to achieve low contact resistance with lightly doped silicon emitters. Finally, the linewidth achieved using the best screen printers is limited to 50µm. All these factors contribute to optical and resistive losses in the solar cell and limit the performance of the cell.

Ni-Cu plating

With Ni-Cu plated contacts it is possible to overcome the challenges associated with silver paste technology. The plated metal has the bulk conductivity of Copper making it 2x more conductive as compared to the silver paste[11]. The nickel seed layer is annealed to form a thin nickel silicide layer which has a low resistivity 10-20µΩ.cm[13]. This low resistivity helps in forming good ohmic contact with lightly doped silicon. Contact opening of less than 10µm can be achieved using femto-second laser ablation of dielectric[8]. Taking lateral overgrowth during the plating process into account feature sizes of 30µm are easily achievable. This reduces the shading losses associated on the front grid of the solar cell.

Ni-Cu plated contacts has some challenges associated with it. Copper is a fast diffusing species in silicon and form minority carrier recombination sites[9]. This can severely affect the electrical properties of the solar cell by increasing recombination. Adhesion of the copper metal on silicon is poor and requires a Nickel seed layer to promote adhesion. To overcome these challenges a thin nickel layer is plated before plating thick conductive layer of copper. Nickel is annealed to form NiSi which acts as an adhesion promoter and also serves as a diffusion barrier[14]. One of the main challenges associated is the Nickel silicide formation that results in spiking through the p-n junction[15][16]. This results in shunting of the solar cell and formation of

recombination centers which reduces the open circuit voltage and the fill factor of the solar cell.

There are a few reasons that make the formation of nickel silicide very desirable in the formation of Ni-Cu stack. Nickel mono-silicide formation after annealing is necessary to form a good ohmic contact between Ni and Si layers[17]. The low contact resistance is important in order to reduce the series resistance losses[18]. This is possible due to the 0.6eV[19] low barrier height for the NiSi phase. Nickel silicide formation consumes 1.83nm of Si per nm of Ni which is the least compared to Cobalt and Titanium silicide[20]. Nickel silicide formation is diffusion controlled compared to nucleation controlled growth with $CoSi_2$ & $TiSi_2$[20]. The annealing temperatures required to form the nickel silicide is in the range of 250-700°C[21]. The lower thermal budget required is important because these temperatures do not have any significant effect on the dopant profile of the solar cell. Also the maximum temperature allowable at this stage is limited by the Al-back surface field which is formed at peak temperatures of 800-950°C but starts flaking off at 600°C.

One of the purposes of the nickel silicide is to serve as an adhesion layer for the Ni-Cu stack. It has been reported that the adhesion of the plated contacts is dependent on the thickness of the nickel silicide layer[14]. Formation of deep and uniform layer of silicide results in better adhesion of Ni-Cu stack.

Copper is a fast diffusing species even at room temperatures. Nickel silicide formation can also be used as an effective barrier to prevent Copper from diffusing into the silicon substrate during processing and operating conditions[22].

On annealing results in the formation of low resistivity nickel silicide phase. There are 3 reported $NiSi_x$ stable phases and some of their properties are tabulated in Table 1.

	Ni_2Si	NiSi	$NiSi_2$
Temperature (°C)	250-400	350-700	800-900
Barrier Height(eV)	0.8-1	0.6	
Resistivity (μΩ-cm)	34-50	10.5-18	24-30
Raman peaks(cm^{-1})	100,140	190,216,362	224,283
Diffusion activation energy (eV)	1.3	1.5-1.6eV	

Table 1 Properties of the Different Phases of Nickel Silicide [19][20][23].

Simulation

In order to verify the performance potential of Ni-Cu plated cells a simulation is done and results are compared with silver paste cells. Here the assumption is that the problems associated with adhesion, Cu diffusion and nickel silicide shunting do not affect the cell performance. For comparison 2 cells are simulated using Griddler 2 solar cell simulation software[24]. Griddler 2 is finite element model simulator which analyses the solar cell by dividing the front and rear of the cell into meshes. Each mesh is further made up of nodes and triangular elements which individually analyzed. Griddler 2 uses the two diode model for calculating terminal voltage[25]. A large area solar cell is made at the Solar Power Lab at Arizona State University using double print silver paste technique. The double print results in higher aspect ratio fingers which requires sophisticated printers with alignment capabilities for reprinting. This is used to produce higher efficiency cells and can be considered as state of the art in the printing technology. Silver paste cell with known I-V properties is replicated to establish other recombination cell input parameters. These cell parameters are used for to simulate a Ni-Cu plated cell.

	Double Print Ag Paste	**Ni/Cu Laser ablated**
Emitter Sheet Resistance	60Ω/□	90Ω/□
No of fingers	72	100 (grid not optimized)
Finger width	60 µm	20 µm
Finger Height	15 µm	10 µm
Finger Contact resistance	2 mΩ-cm2 [1]	1 mΩ-cm2 [2]
Measured resistivity	$3.95*10^{-6}$ Ω-cm	$1.66*10^{-6}$ Ω-cm

Table 2 Cell Parameters Used for Simulation in Griddler 2.

Table 2 the cell parameters for both the simulated cells are shown. For the silver paste cell the grid has been optimized to minimize optical and resistive losses based on sheet resistance of the emitter. For Ni-Cu plated cell the grid has not been optimized since the process was still in development stage. From preliminary data a finger width of 20µm was obtained was obtained for plated cells. Finger sheet resistance are measured values. The actual and simulated results are tabulated below in Table 3. There is an increase in the short circuit density with the Ni-Cu plated cell. This is due to three reasons. Firstly, there is less optical shading loss because laser patterned fingers are much thinner compared to the screen printed silver paste. Secondly, the lower surface concentration results in more absorption of the shorter wavelengths in the base region of the semiconductor. This results in better blue response in the IQE. Lastly, the improvement in aspect ratio of the finger profile compared to the silver paste fingers. The improvement in open circuit voltage is due to the lower surface concentration of dopants at the surface. This results in a reduction of recombination centers in the emitter region. There is a small reduction in the front grid series resistance due to improved line resistance and contact resistance. The improvement of series resistance directly

correlates to the increase in fill factor for the Ni-Cu plated cells. The reduction in optical shading is mainly due to the ability to form lines that are 20μm wide. The efficiency of the simulated Ni-Cu plated cell is 18.7%. This is an absolute gain of 0.5% in efficiency over the double print silver paste technology.

	J_{sc} (mA/cm^2)	V_{oc} (mV)	Fill Factor %	Rs Ω-cm^2	Optical Shading %	Efficiency %
Measured Double Print Ag Paste DI0550-09	35.9	620	78.3	0.685	5.65	17.4
Simulated Double Print Ag Paste	36.61	623	79.93	0.395 (front grid)	5.65	18.23
Measured Ni/Cu Laser patterned DI0585-03	37.4	608	74.8	1.02	4.17	16.9
Simulated Ni/Cu Laser patterned	37.37	325	80.1	0.365 (front grid)	4.17	18.7

Table 3 Measured and Simulated Cell Results from Griddler 2.

The above simulated results show that there is significant gain in the short circuit density that can be gained due to the laser patterning process for Ni/Cu plating. This is confirmed by actual cell results that have high Jsc-37.37mA/cm2. For Voc of actual cell results with Ni/Cu laser is lower compared to simulated values. This is maybe to metal induced recombination which is discussed later. The series resistance of the cell

Light induced plating

Light induced plating has a similar concept to electroplating. Electroplating consist of the following parts. An anode which is the source of the metal that is to be deposited. A cathode or the workpiece which gets deposited with the metal ions and gets plated. A power supply to drive the process of plating. An electrolyte solution containing the metal ions that needs to be plated. In electroplating both the anode and the cathode are immersed in the electrolyte solution.

A direct current flows through the anode and oxidizes it resulting in the formation of metal cations which get dissolved in the electrolyte solution. These positively charged metal ions get attracted to the negatively charged cathode and accept the electrons and get deposited. This deposition process is known as reduction.

In LIP technique the anode is immersed in the electrolyte. The front of the solar cell is introduced into the electrolyte solution while keeping the rear side dry. The front side of the solar cell is illuminated by LED's submerged in the electrolyte. The rear side of the cell is contacted with brush wire and is connected to the power supply. The illumination of the solar cell forms a potential difference between the front and rear of the solar cell. The dielectric layer which has been locally patterned on the front surface by laser. This exposes the underlying n+ emitter which is the where the metal ions get reduced and deposition takes place. The deposition rate is governed by the illumination intensity and the bias applied through the rear contact.

CHAPTER 3

NICKEL SILICIDE CHARACTERIZATION

Sample Preparation

For this experiment 156mm p-type Czochralski Si (1 0 0) resistivity 2-5Ω-cm were used. The wafers are 170μm thick and are etched in 30% KOH and RCA cleaned. Before deposition of the nickel layer the native oxide is removed using a Buffered Oxide Etch (BOE 1:10) solution. MRC944 DC magnetron sputter tool is used to deposit 120nm of NiV (90%-Ni, 10%-V). For samples with an oxide layer the oxide etch step is replaced by the following step. A self-limiting wet oxide is grown using pure Nitric acid at 70°C for 10 minutes. This results in the formation of 2-3nm thick layer of SiO_2. The samples are annealed by Rapid Thermal Anneal (RTA) AST-280 furnace in nitrogen ambient. After annealing the unreacted nickel is selectively etched using $H_20:H_2SO_4:H_2O_2$ (4:2:1). To ensure complete removal of unreacted nickel an un-annealed sample is used as a control sample during the etching process. The wafers are rinsed and dried using spin rinse drying.

These samples are used for sheet resistance measurements, Raman spectroscopy and Rutherford backscattering spectrometry experiments in this work.

Sheet Resistance

The sheet resistance (ρ_s) of the silicide layer was measured using a four point probe. On each sample 5 measurements at different locations to monitor uniformity in annealing tool. The annealing temperature was varied from 325-900°C and the samples are annealed for 2 minutes. The sheet resistance of as-dep layer of Nickel was measured before annealing. The sheet resistance values are plotted using a box plot and shown in Figure 2. At low temperatures of 325°C the sheet resistance increase compared to as-dep film. This is due to formation Ni_2Si which is reported to be the

more resistive phase of silicide. Another reason for the high value of sheet resistance can be accounted to the thin layer of silicide formed due to small thermal budget. As the temperature is further increased to 400°C the thickness of the silicide increases & there is a sharp drop in the ρs reduces to below 5Ω/□. With increase in temperature to 500°C the sheet resistance is 1Ω/□ and this indicates the onset of NiSi formation. NiSi is reported to be the least resistive phase of the silicide[26]. The minima is reached at 600°C anneal indicating formation of pure NiSi phase. Even after increasing the temperature further to 700°C there is no change in the sheet resistance values. This may be due to the agglomeration of NiSi on the surface[27]. At higher temperature a second factor that contributes to the increase in sheet resistance is the nucleation of $NiSi_2$ phase. The silicon rich phase is known to nucleate in islands thus forming discontinuous films which drastically increases the sheet resistance[28]. This effect can be seen in the slight increase in sheet resistance at 900°C. Overall the temperature range can be broadly divided into three zones each with associated with the presence of a particular phase. The initial range of 300-500°C is the formation of Ni_2Si the metal rich phase. The second zone has the lowest sheet resistance ranging from 500-800°C. The last zone is the silicon rich phase NiSi2 which has the higher sheet resistance. It must be noted that there is no sharp boundary for these zones and it may vary by 50-100°C depending upon conditions in which the processing and measurements were done.

The sheet resistance measurements directly show temperature ranges from 500°C to 600°C might provide best sheet resistance at least thermal budget.

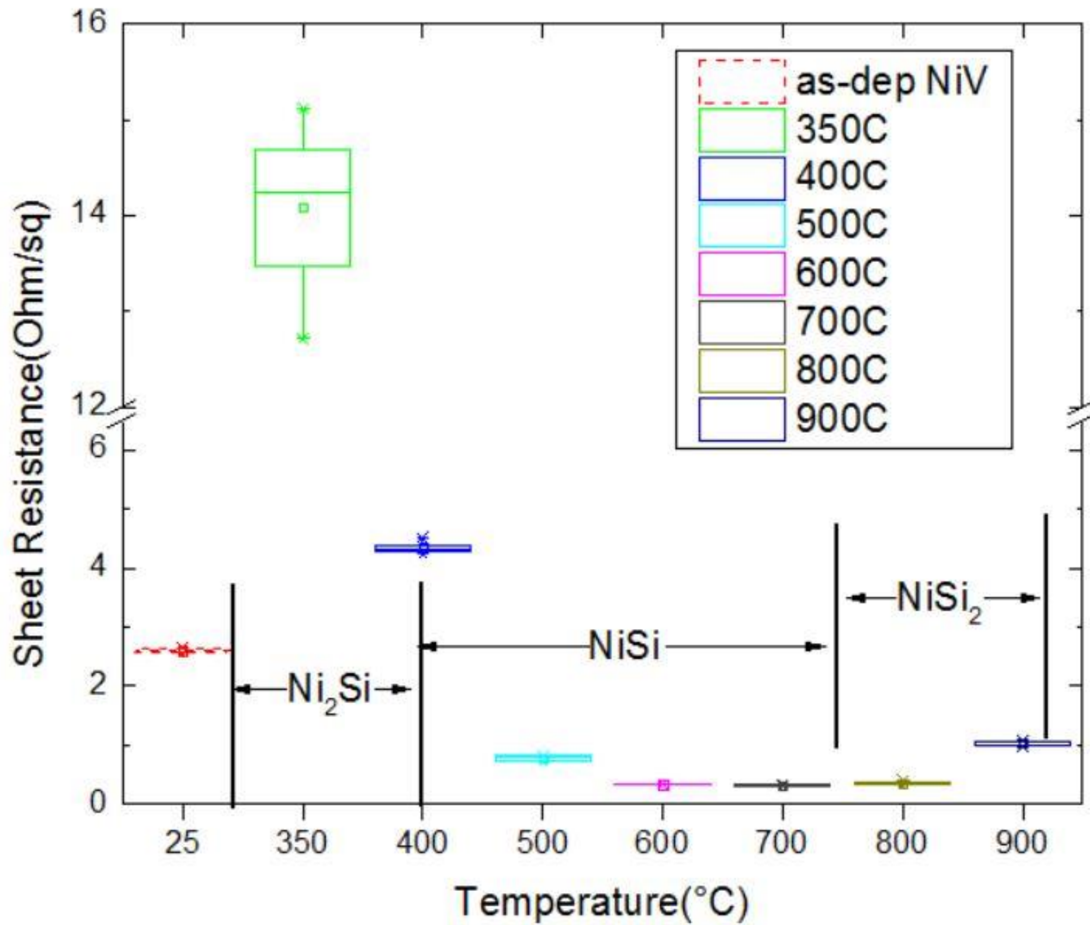


Figure 2 Sheet Resistance of $NiSi_x$ after Annealing.

Raman spectroscopy

Raman spectroscopy is spectroscopic technique based on inelastic scattering of monochromatic light. Inelastic scattering is due to the frequency of incident photons changing after interaction with the sample. Absorbed photons from the incident light source are emitted with either an up or down shift compared to the incident frequency. The shift provides information about vibrational rotational and other low frequency transitions[29].

For this study a Renishaw inVia Raman Microscope equipped with and excitation laser at 532nm is used. The samples were loaded onto the stage and the laser was focused using

50x magnification microscope as shown in Figure 3a. The laser power is set to 10%, this is done to reduce the local heating of sample during the acquisition of data. As silicide formation can take place at low temperatures 200-250°C it is important to avoid the local heating of the sample[30]. Each acquisition is for 5 seconds and 100 acquisitions are done.

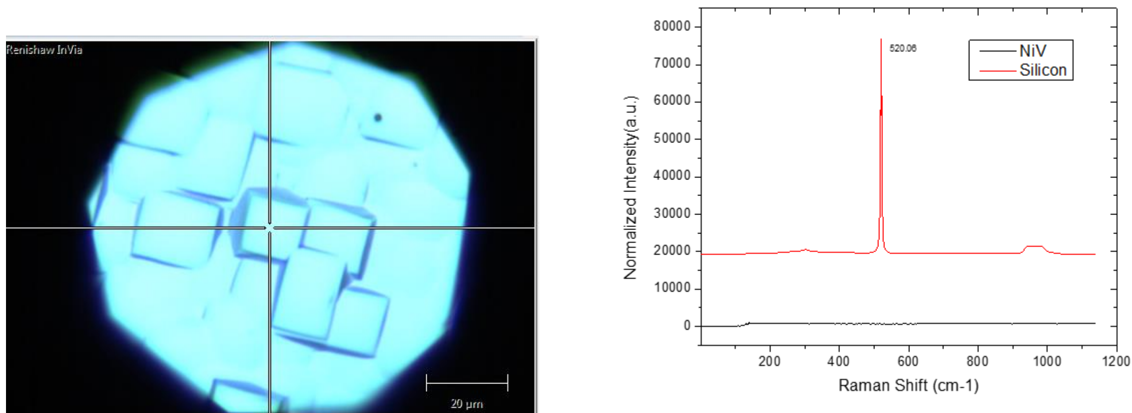


Figure 3 a) Sample View Through Optical Microscope at 50x Magnification B) Raman Spectrum of Niv and Phosphorus Doped Si.

A sample Raman spectrum for NiV and phosphorus doped Si is shown in Figure 3b. The NiV sample does not does not show any peaks indicating that it is Raman inactive compound. For Si the characteristic peak at 521cm^{-1} which are 3 degenerate optical phonons is observed at 520.06cm^{-1}[31][32]. The 2-phonon Si peak at 300cm^{-1} and the plateau at 950-100cm^{-1} are also observed[33]. The Si peak position can vary with stress caused due to thin films on the Si surface.

Raman spectroscopy is used to detect the formation of NiSix phases and its dependence on annealing time and temperature. The Figure 4 below shows the Raman spectra of silicide formation at different temperatures annealed for 2minutes. The metal rich phase

Ni_2Si has been reported to form at temperatures of 250-400°C[30]. This is the higher resistivity phase of the silicide as seen from sheet resistance data in previous section. The Ni_2Si phonon signals are reported to be at 100 and 140cm^{-1}[33]. In this study the 100cm-1 peak is not observed under any of the conditions. The peak at 140.97cm^{-1} that is the Ni_2Si peak which has been observed in this study. This peak intensity for Ni_2Si is very strong in the 325 -400°C samples. The peak at 521.33cm^{-1} is the silicon peak. The intensity of Si peak gradually decreases as the temperature increases. This is due to the increase in the thickness of the Ni_2Si layer being formed hence reducing the probing of underlying silicon lattice. As the temperature is further increased 500°C the peak at 140.97cm^{-1} broadens and the intensity is comparable to the noise. At 500°C the Si peak vanishes indicating the $NiSi_x$ layer is the only volume of sample that is being analyzed by the incident beam. The peak intensities for Ni_2Si and NiSi are significantly reduced compared to the background. At 600°C the peak shifts to 139.62cm^{-1} and the intensity reduces significantly compared to the background noise. The larger full width half maximum (FWHM) indicate a broadening of the Raman spectra are produced due to a decrease in phonon lifetimes, which is caused due to defects[32]. A lower value for FWHM would indicates a lower defect density in silicide and the presence of single phase silicide in the thin film. FWHM is plotted for each of the three silicide phases as a function of temperature in Figure 5, there is clearly an increase in the FWHM of Ni_2Si as the temperature increases indicating the formation of NiSi and reduction of Ni_2Si phase in the film.

Nickel mono-silicide (NiSi) has 12 active optical phonon signals[23] that have been predicted by group theory. Depending upon preparation methods and sensitivity of detector a maximum of 12 lines can be detected for NiSi. The lines reported for NiSi in

literature are 197, 217, 255, 267, 290, 314, 363cm^{-1}[23] and 197, 214, 255, 288, 314, 332, 360, 397cm^{-1}[33].

In Figure 6 four peaks are observed at 194.75, 214.81, 291.8, and 363.99cm^{-1} which are clearly associated with the formation of NiSi. The two peaks that strongly indicate the presence of NiSi are 194.75 & 214.81cm^{-1}. These peaks are found at subdued intensities at lower temperatures of 325°C indicating the formation of NiSi. The intensity of these peaks consistently increases and is maximum at 600°C. At 700°C the peaks start to broaden this might be due to agglomeration of NiSi and formation of smaller grains. Due to increase in grain boundaries and defects the lifetime of the phonon signal reduces and this causes the peaks to broaden[23].

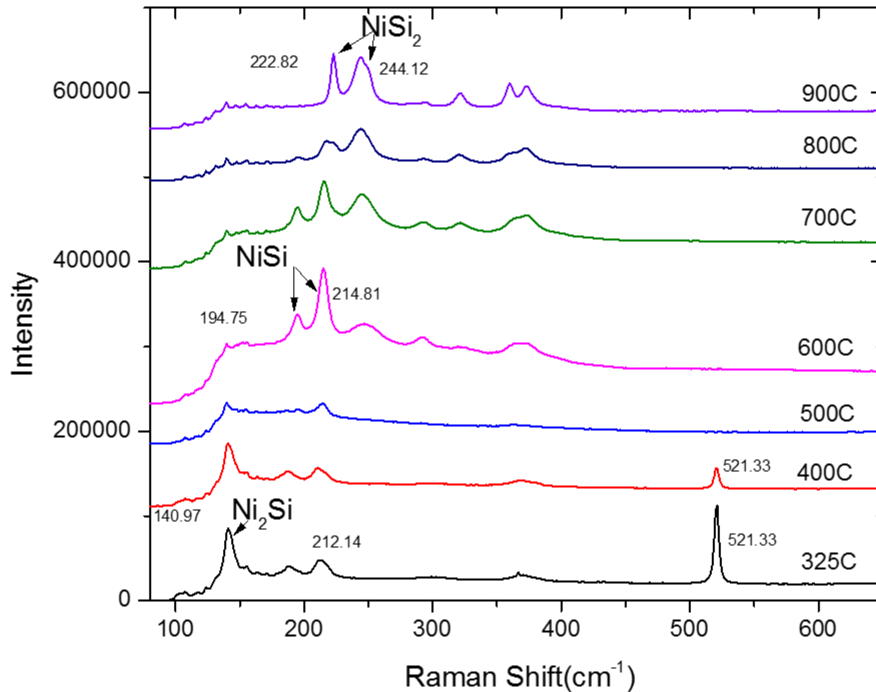


Figure 4 Raman spectrum of $NiSi_X$ from 300-900°C for 2 minutes.

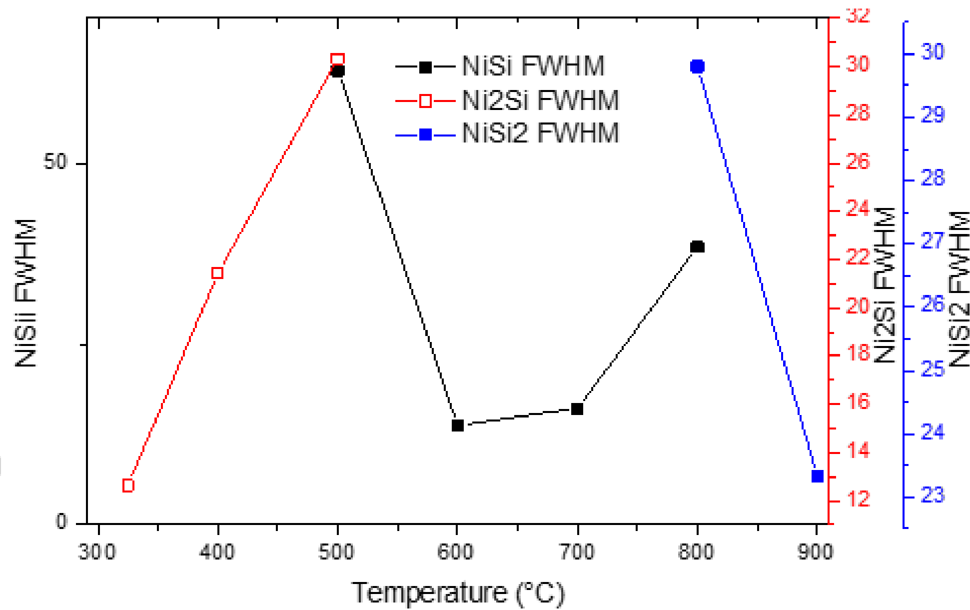


Figure 5 Full width at half maximum of a) NiSi peak at 216cm^{-1} b) Ni_2Si peak at 140.97cm^{-1} c) $NiSi_2$ peak at 222.82cm^{-1}

In Figure 7 the 216cm^{-1} peak position is plotted as a function of temperature. Since the only variable is the temperature the cause of the shift can be associated with stress or strain in the NiSi film during annealing[34][35]. At lower temperature the 216cm^{-1} peak is left shifted 210.8cm^{-1}. As the temperature is increased the peak position moves to the right and finally reach 216cm^{-1} which is reported in literature[23]. It has been reported that peak position depends upon the doping type of the silicon substrate and this can greatly affect the stress in these films[34]. The likely source of peak shifts is the biaxial strain in the silicide films[36].

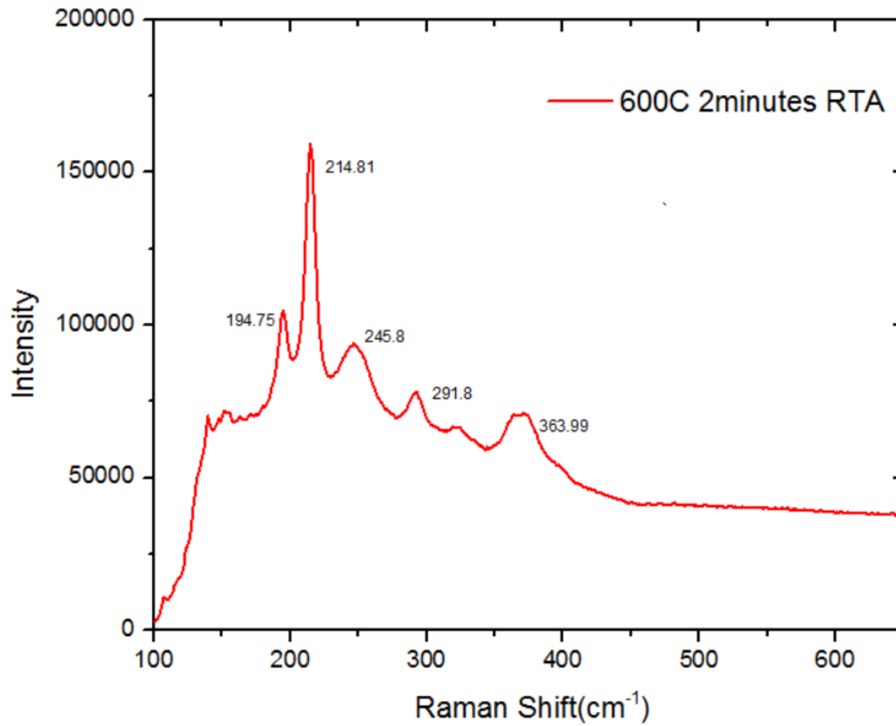


Figure 6 Raman spectrum of NiSi after 2 minutes RTA at 600°C.

In Figure 5 the FWHM of the 216cm^{-1} peak is plotted as a function of temperature. The FWHM is at minima at 600°C. At 600°C where the Ni_2Si peak has completely disappeared and only the NiSi peak is present the FWHM is minimum. At 700°C there is a slight increase in the FWHM this may be due to the agglomeration NiSi layer which has also can reduce phonon decay time thus due to grain boundaries formation[34].

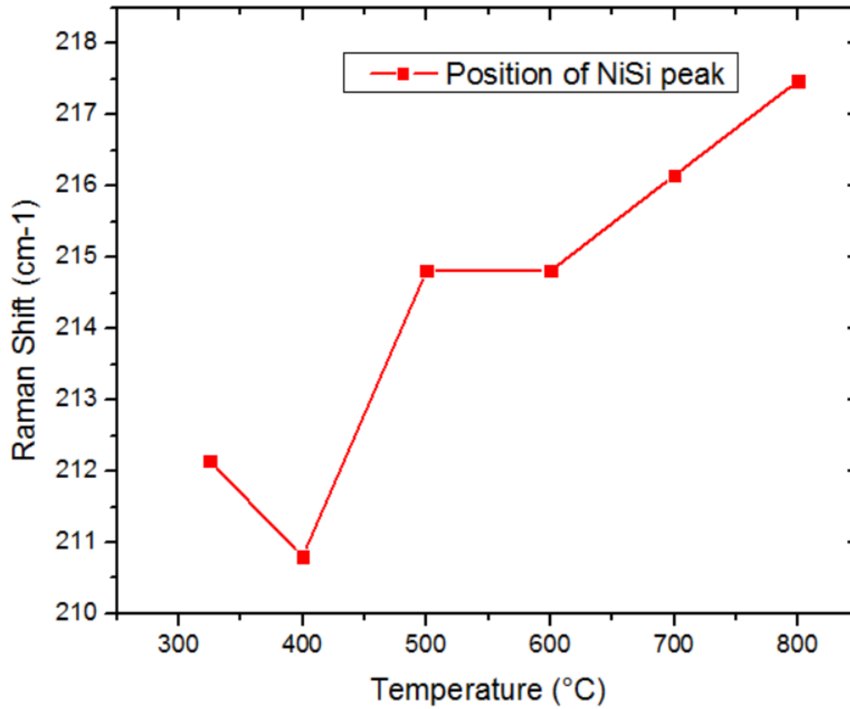


Figure 7 Raman shift of peak as a function of annealing temperature.

Further increase in temperature results in the nucleation of the silicon rich phase of NiSi2. This can be seen at 800C with formation peak at 245cm^{-1} and 244.12cm^{-1} at 900°C. The peak at 222.82cm^{-1} is also associated with formation of $NiSi_2$. It has been reported the formation of $NiSi_2$ phase is nucleation controlled and due to this it forms islands of silicide layers[28]. The formation of discontinuous silicide islands results in the formation of more resistive silicide layer.

In conclusion, results from the Raman spectroscopy data show that there is NiSi is formed at temperatures as low as 325°C along with Ni_2Si. A film with dominant single phase of NiSi is formed at 600°C. Further increase in temperatures can result in the formation agglomerated films at 700°C and the peaks begin to broaden. At 900°C silicon

rich $NiSi_2$ phase is formed and from sheet resistance data it can be confirmed that it is a higher resistance phase.

Time dependence of $NiSi_x$ formation

As seen in previous section within the temperature range of 325-500°C there are two phases of $NiSi_x$ that co-exist. The more desirable phase for solar cells is NiSi due to its lower resistance. To understand the formation of NiSi a time dependent study of annealing is discussed in this section.

In Figure 8 annealing is done for 2, 10 and 20 minutes and the Raman spectrum is plotted. For the 2 minute anneal both Ni_2Si and NiSi phases are observed along with the Si peak. At this stage some of the Nickel has reacted and formed Ni_2Si and NiSi while there is still some unreacted Nickel leftover. On further annealing the Ni_2Si peak becomes sharper and there is increase in intensity of the peak. There is a reduction in the silicon peak intensity and this is due to increase in total thickness if the silicide layer. For 20-minute sample there is significant change s in the peak. The Ni_2Si peak intensity is greatly reduced in comparison to the NiSi peak. The FWHM of NiSi peak is greatly reduced indicating a much sharper peak and presence of much purer phase of NiSi.

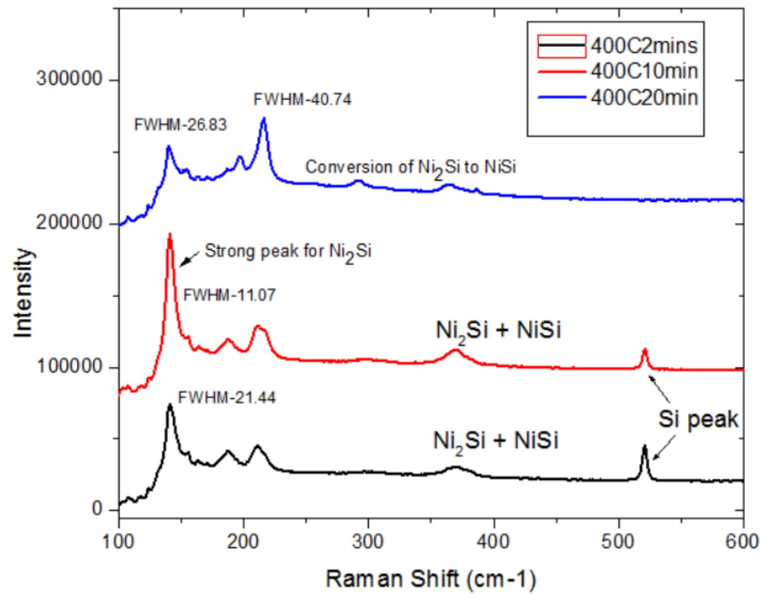


Figure 8 Comparison of Raman spectrum for various annealing time at 400°C.

The time series of anneals show the sequential formation of NiSi from Ni_2Si. The initial reaction takes place by solid state diffusion. Here the nickel atoms diffuse into the silicon lattice and result in the formation of Ni_2Si. After all the nickel has been consumed the Ni_2Si layer is converted to NiSi resulting in the lower sheet resistance. This can be seen by comparing the spectrum of 10 and 20 minute anneal spectrum. The Figure 9 explains the formation the phase formation of $NiSi_x$ with progressing time

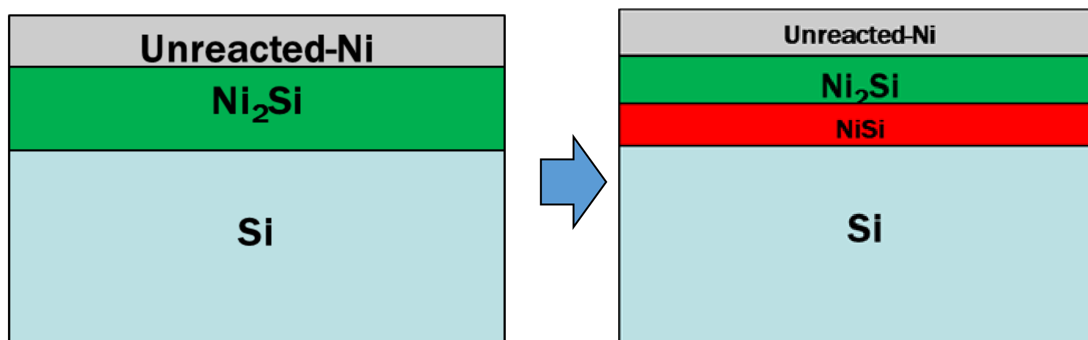


Figure 9 Schematic of NiSix phase formation with at 400°C a) 2 minute annealing b) 10 minute annealing.

Limiting the supply of Nickel

To further understand the formation of NiSix layer in the 350-600°C another set of samples is prepared using NiV layer of 30nm layer thickness. A thin layer of nickel will limit the formation of silicide formation because of reaction limited growth and not diffusion. The samples are annealed from 350-600°C for 2 minutes and the Raman analysis is shown below in Figure 10. At 350°C the Ni2Si peak is observed at 140.97cm^{-1} as seen earlier. For the 400°C anneal the Ni2Si peak intensity is increased and NiSi peak at 214.81cm^{-1} is also observed. As the temperature is increased further to 500°C only NiSi peaks are seen at 196.09 and 216.15cm^{-1}. The absence of Ni2Si peaks at 500°C shows that it has been consumed during the formation of NiSi. Further increase in temperature to 600°C there is no noticeable change the Raman signals.

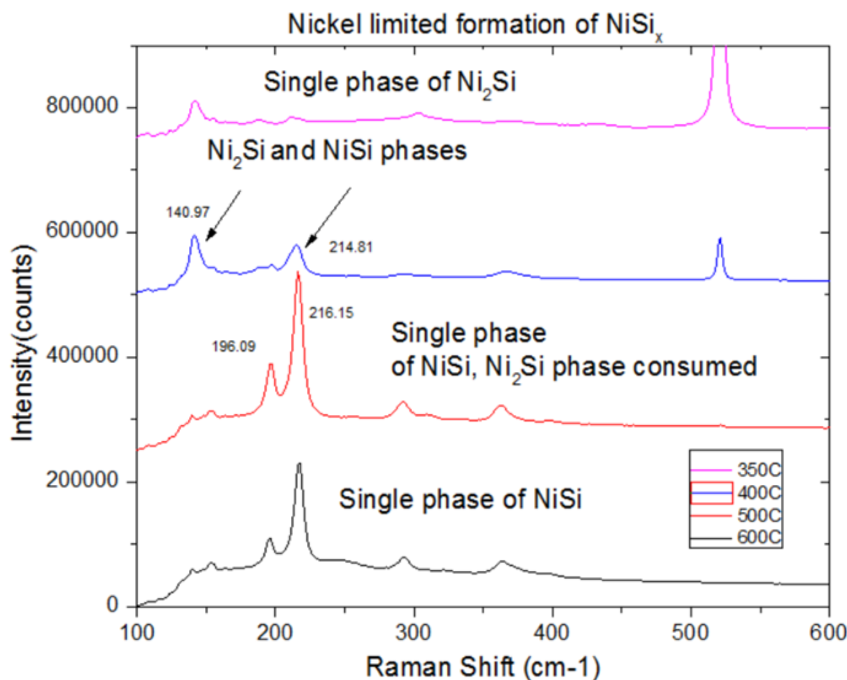


Figure 10 Limiting supply of Ni during the silicidation using 30nm NiV 2 minutes RTA.

The results from the time dependent study and limited supply of Nickel indicate that NiSi can be formed at low temperatures of 400-500°C. If the flux of Ni atoms is reduced at the Ni-Si interface it will promote the growth of NiSi at much lower thermal budget.

There are a few challenges associated with plating 30nm thin layer of Ni: 1) uniformity of the deposit metal layer throughout the device 2) process control of plating rates at such low in industrial tool is difficult 3) the formed silicide may not provide good adhesion and still might require deeper silicide.

In conclusion, the phase formation of nickel silicide depends on three factors 1) Annealing temperature 2) Annealing time & 3) Amount of Ni available for silicidation.

Effect of SiO_2 on the formation of NiSix

From previous section it can be seen that reducing the flux of Ni atoms at Ni-Si interface results in the formation of NiSi with lower thermal budget. Increasing the temperature and time for annealing will increase the depth of the silicide formed. This is not desirable as silicide that goes through the junction will shunt it creating a leakage path for current. A simple solution is to form a deep junction initially so that this can be avoided but this increase the thermal budget for diffusion of phosphorus and the cost for production.

It has been reported that even natively formed SiO_2 forms a diffusion barrier for silicidation reaction[37]. SiO_2 forms a strong barrier which hinders the kinetics of the silicidation reaction[37]. Hence, most studies on $NiSi_x$ have been done with a clean Ni-Si interface to achieve silicidation easily. This is usually achieved by pretreatment of the substrates before Ni deposition using Buffered Oxide Etch. Here the aim is to use the native oxide on the silicon surface as a diffusion barrier to retard the flux of Ni atoms for silicidation so before.

In the following experiment a 1-2nm thick SiO_2 layer is grown chemically using pure nitric acid at 70°C for 10mins on Si substrate. 120nm of NiV is deposited on the SiO_2/Si wafers, followed by annealing and etching of unreacted Nickel. The Raman spectra of the samples are then analyzed and plotted below in Figure 11.

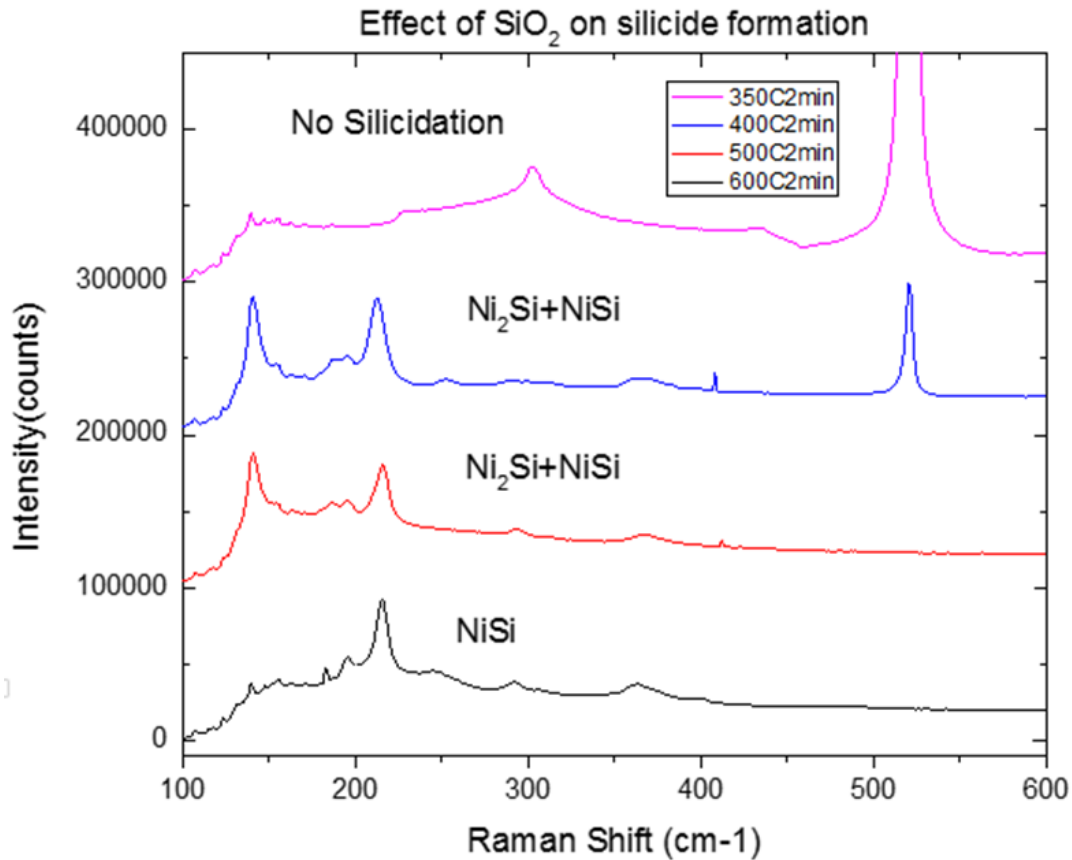


Figure 11 Effect of SiO2 on silicide formation with temperature for 2 minute RTA.

At 350°C annealing there is a small peak at 140.97cm^{-1}, the intensity of which is comparable to the background noise. This is much different from the 325°C peak in Figure 4 where this peak is very prominent. In fact, at 350°C the 2-phonon signal at 300cm^{-1} along with the optical phonon peak at 521cm^{-1} can be observed in the Raman spectra. This indicates that the silicidation reaction is being prevented by the SiO_2 layer. This is in line with results published in literature.

Although at higher temperatures of 400-500°C there is clearly formation of both Ni_2Si and NiSi phase. It is likely that at higher temperatures the diffusivity of Ni atoms is high enough to go through the oxide barrier layer. Since, SiO_2 is a porous dielectric layer it is possible that at 400°C the Ni atoms start diffusing through the voids in the SiO_2 film and the silicide reaction can take place at Ni-Si interface. This would explain the direct formation NiSi at lower temperatures. At 600°C the Ni_2Si peak intensity reduces sharply compared to lower temperatures and only NiSi single phase is detected.

In conclusion, SiO_2 acts as an effective diffusion barrier at 350°C. Although at higher temperatures of 400°C it can be seen that the silicide formation can progress even with the presence of SiO_2. The SiO_2 layer here is used to control the flux of Ni atoms at the Ni-Si interface and which directly affects phase formation of silicide.

Rutherford Backscattering

In previous section it has been shown that SiO_2 affects the kinetics of silicide formation. To further understand if the thickness and composition of the silicide formed Rutherford backscattering is used. For the above samples to evaluate the effect if SiO_2 on the formation of silicide a 2 MeV He^{2+} ion beam is used to irradiate the samples. For samples with lower thermal budget θ= 60° inclination to the sample is provided to probe more region of the film.

In Figure 12 & Figure 13 the RBS data and RUMP simulation for samples annealed at 400°C for 2 minutes with and without oxide are shown. The large peak at channel 270 is for nickel in the silicide. This peak is wider for the samples without oxide in both the samples. The tailing of the peak at lower channels is most likely due to the surface roughness. The counts for nickel is significantly higher in the case without oxide when compared to with the sample with native oxide under identical annealing conditions. The higher nickel counts indicate towards a silicide film that is metal rich compared to

the film formed with oxide. A step is observed at channel 200, this corresponds to the amount of silicon in the silicide layer. After that the counts rise steeply and plateau. The plateau channel 180 to 0 is when the ion beam is analyzing the silicon from the substrate.

Using RUMP[38] simulation software a RBS plot of a thin film can be simulated. The results of the RUMP thickness and atomic composition have been compiled in Table 4. The effect of the oxide on composition and thickness can be clearly seen at lower tempertures. The sample with oxide at 400°C has Ni:Si ratio of 1:1 indicating the formation of NiSi. While the film without any native oxide results in Ni:Si ratio of 2:1 indicating the presence of Ni_2Si. This effect can be clearly seen in the sample annealed at 360°C for 8 minutes. The error for this simulation is close to 1% for Ni and 2% for Si%.

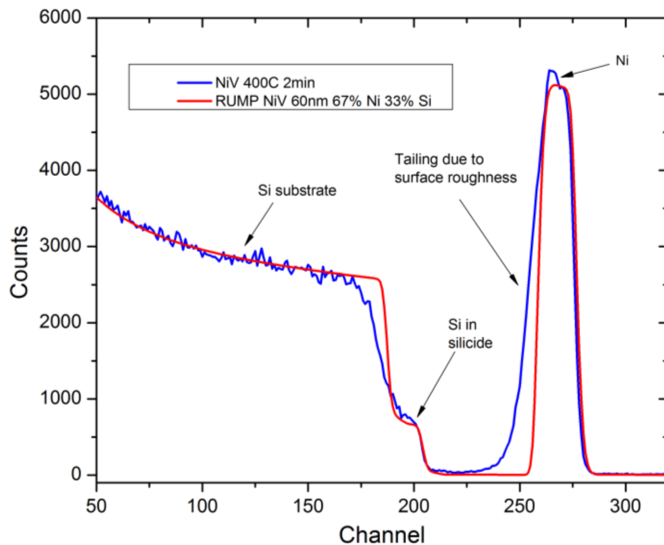


Figure 12 RBS experimental data & RUMP simulation for annealing at 400°C for 2 minutes.

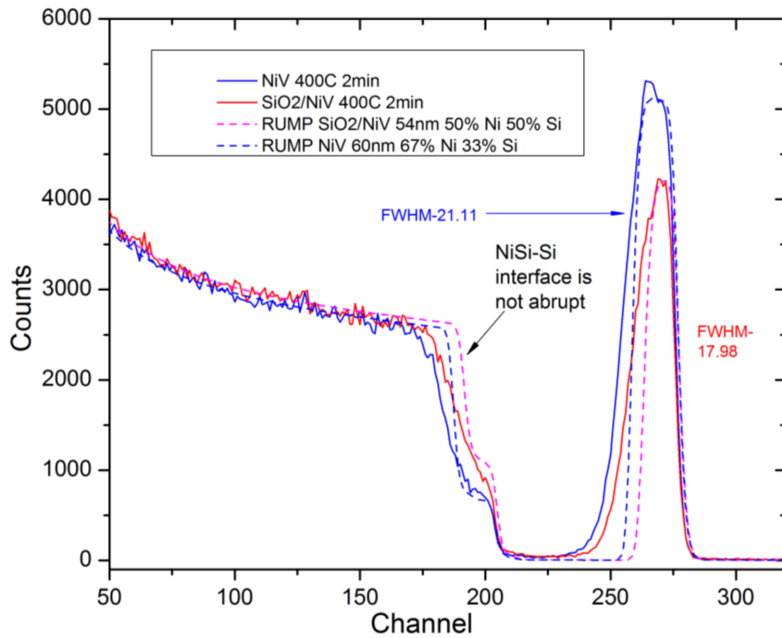


Figure 13 RBS experimental data and RUMP simulation for400°C for 2 minute annealing with and without oxide.

Sample	Temperature °C	Time (minutes)	RUMP Areal Density nm	RUMP Ni atomic %	RUMP Si atomic %
NiV	360	8	65	62%	38%
SiO2/NIV	360	8	51	55%	45%
NiV	400	2	60	63%	37%
SiO2/NiV	400	2	54	50%	50%
NiV	500	5	365	63%	37%
SiO2/NiV	500	5	340	50%	50%

Table 4 RUMP simulation for Nickel silicide films.

The simulated film thickness can be found from RUMP. Using the thickness data and sheet resistance the resistivity of the phase can be found. The equation for resistivity is$\rho_s = R_s * d_{Silicide}$. The literature values for NiSi range from 10.5-18 μΩ.cm and 24-30 μΩ.cm for Ni_2Si[39]. The measured values shown in Table 5 are in good accordance with the values in literature.

Sample id	Thickness nm	Sheet resistance	ρ (μΩ.cm)
SiO2/NiV 400°C	54.74	4.21	23.03
NiV 400°C	59.14	4.34	25.69

Table 5 Resistivity calculation for $NiSi_x$ after 400°C anneal for 2 minutes.

In conclusion, the native oxide has significant effect on the thickness and composition of nickel silicide films during annealing. With the help of sheet resistance, Raman and Rutherford backscattering data above it can be concluded that native oxide is acting as a barrier layer for diffusion of Ni atoms and can be used to form NiSi at lower temperatures.

CHAPTER 4

NICKEL COPPER PLATED SOLAR CELLS

Solar Cell Fabrication

For all the experiments carried out in this work 156mm p-type Czochralski-Si substrate (1 0 0). The resistivity of the wafers used is 2-5Ω-cm and thickness is 190μm. The wafers procured from vendors are first treated in 30% KOH solution for saw damage removal. Then the wafers are textured in 2% KOH at ~80°C for 25 minutes for texturing of the surface. Texturing exposes the (1 1 1) planes of the wafers resulting in an increase in the optical path length of through the wafer. This results in a reduction in reflectance from the surface of the wafer. The wafers are then cleaned using RCA-1 and RCA-2 clean to remove organic and ionic impurities from the surface. A thin layer of PECVD oxide is deposited onto the back side of the wafers. The next step is diffusion of phosphorus using diffusion furnace ~800°C which results in a surface concentration of $1E21/cm^3$ and a junction depth of 200-300nm. Phosphosilicate glass is removed using Buffered Oxide Etch (BOE 1:10). The sheet resistance of the n^+ layer is 60Ω/□. A 78nm thick layer of Silicon Nitride (SiNx) is deposited on the front surface using PECVD. This layer serves as Anti-reflection coating (ARC) and a surface passivation layer to reduce minority carrier recombination. The film deposited suing the PECVD reactor is not stoichiometric so it is usually written as SiN_x.

At this stage for silver paste metallization front side contact is made by screen printing silver paste. The back side contact is made using aluminum based paste which also forms the back surface field. The contacts are them fired using a belt furnace with peak temperatures at 850°C. This process flow mentioned above for Al-BSF solar cell makes it easy to manufacture at low cost.

For Ni-Cu plating the process can be divided into two part. The first part is patterning of the SiNx layer to expose underlying n+ layer of silicon. The second part is the actual plating process.

Laser Patterning of Dielectric

The patterning process flow is shown in Figure 14. After PECVD SiNx deposition a masking layer of a-Si is deposited using the same PECVD tool. The laser patterning is done using 800nm 140fs pulse laser. This results in the removal of the a-Si masking layer and exposes the underlying SiNx ARC. The wafers are then introduced in a BOE tank for controlled etching of SiNx layer. The etch time is optimized to ensure complete removal of SiNx and minimal undercutting. H_2 plasma etch is used to remove the remaining the a-Si. Now there is an 8-12µm opening in the SiNx layer. This is followed by screen printing of the Al-BSF and firing in a belt furnace. The firing step causes bowing of the wafer. If the laser patterning is done after the wafers are bowed it will cause non-uniformity because the laser will not be in focus at different locations.

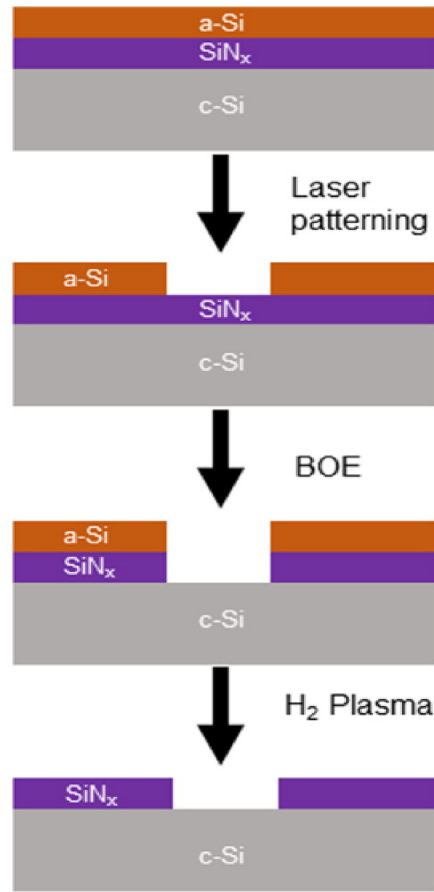


Figure 14 Indirect removal of SiN_x using a laser ablated a-Si etch mask and Buffered Oxide Etch[8].

Ni-Cu-Sn Plating

Once the dielectric SiNx ARC layer is patterned the wafers can now be plated with Ni-Cu-Sn stack. Nickel seed layer is plated first which on annealing forms a diffusion barriers, good ohmic contact and adhesion layer[40]. Copper is the conducting layer through which the photo-generated current is collected. Tin metal is plated which serves as a solder metal because of its low melting point of 230°C.

The process flow for plating is shown below in Figure 15. Nickel metal of thickness <500nm is plated onto the solar cell using light induced plating with a bias. An acid based electrolyte is used for the Ni plating electrolyte. Nickel anodes are submerged in the process tank where the electrolytes is circulated. The plating current density

during operation is 15 mA/cm². The front of the solar cell is submerged in the electrolyte and rear contact is made with wire brush to apply bias from power supply. After nickel plating the wafer can be annealed to form the nickel silicide layer or can be plated with copper. Rapid thermal annealing is done at 300-500°C for 2-10 minutes in nitrogen ambient for the formation of nickel silicide. The unreacted nickel is etched using a mixture of H_2So_4:H_2O_2:H_2O (4:2:1). Another layer of nickel is plated for to improve adhesion. For copper an acid based chemistry is operated at 30 mA/cm². The copper electrolyte also contains proprietary additives like brightener, stress reducer and carrier to improve the quality of the electro-deposited metal. It is also possible to anneal at the Ni-Cu stack and form the $NiSi_x$ layer. Finally a thin layer of tin is plated onto the Ni-Cu stack using LIP. The steps subsequent to this will have a limit on the temperature due to the low melting point of Tin.

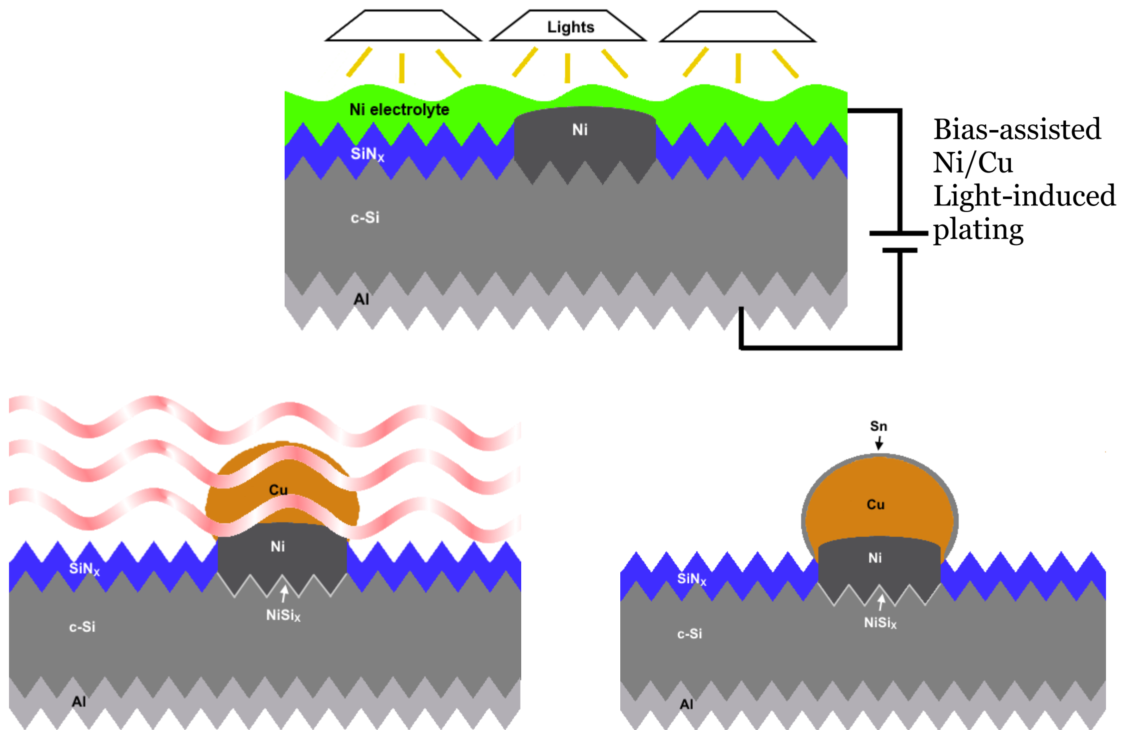


Figure 15 Ni-Cu-Sn plating process flow[41].

Suns Voc

The Suns V_{oc} method is developed by Sinton et al. is a fast and non-destructive electrical characterization technique[42]. This method recreates the series resistance free dark J-V curve which is a useful for characterization during cell processing. The recombination mechanism of the solar cell strongly affect the electrical properties of the device. Once the p-n junction is formed the solar cell can separate the carriers and generate a potential. The open circuit voltage is measured at various light intensities with a flash light decaying in less than 1 second as shown in Figure 16 a. The light intensity is monitored using a reference cell encased next to the sample stage. The series resistance of the cell has no effect on the measurement since no current is drawn from the sample cell. The voltage of the sample is measured and the reference cell calibration is used for generating corresponding current values as shown in below Figure 16b. The pseudo fill factor values obtained depend on the diode quality of the cell and is free from the effects of series resistance. The pFF value depends on recombination and shunting effects. Another advantage is that contact resistance does not significantly affect the Suns V_{oc} curve because there is no direct current measurement[42]. The measured Suns Voc and the double diode fit are plotted in Figure 16 c. This plot shows the measured Suns Voc at various light intensities. The shunt resistance is a fitted value usually calculated by measuring the slope of pseudo light I-V curve at 0.3V.

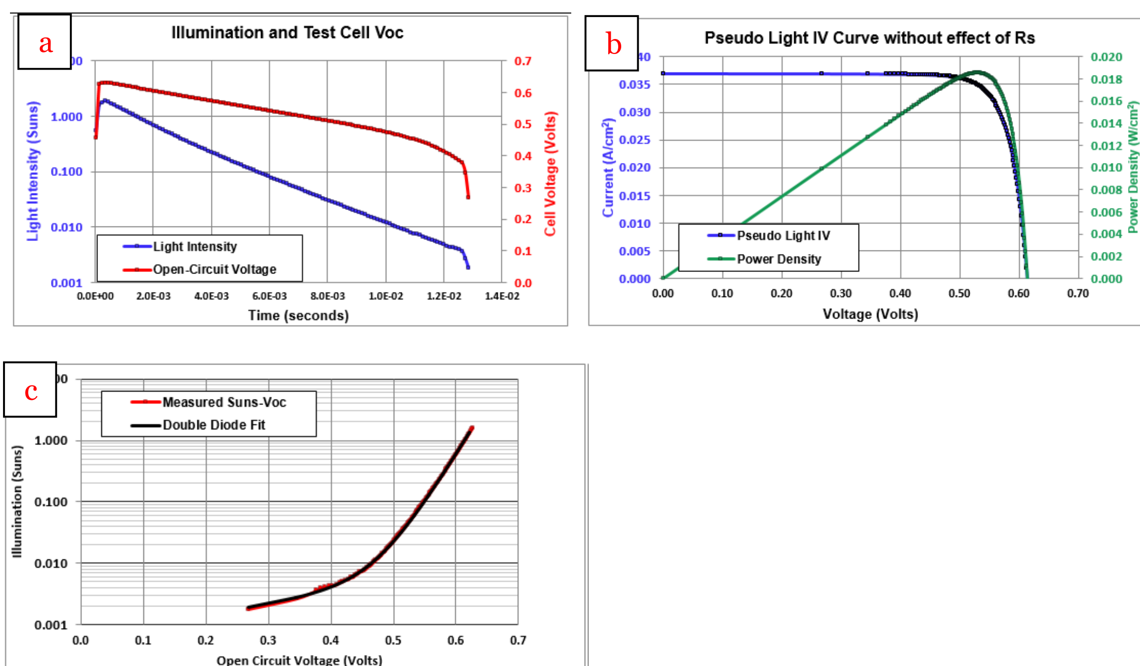


Figure 16 a) Plot of light intensity and cell voltage decay with time b) Pseudo J-V curve c) measured Suns Voc.

For diffused junction solar cell, the junction is formed after diffusion of phosphorus on p-type substrates. Next the Al- back surface field is printed and fired on the back side of the cell. It is now possible to measure the Suns V_{oc} of the device by using a sharp probe to puncture through ARC layer on the front of the cell.

In this experiment, the Suns V_{oc} measurement is done to study the effect of annealing temperature and time on the recombination of the cell. A thin layer of Ni is plated onto the front of laser ablated samples. The front contact is made on the bus-bar using sharp probes. The samples pFF is calculated using the Suns V_{oc} technique before and after annealing. The average pFF before annealing measured for a sample size >60 is 0.821. One sample has a pre-treatment step of 20 seconds BOE before plating to remove native

oxide while the other sample is plated with the native oxide. Each sample was annealed for 2 minutes from 360-600°C.

The Suns V_{oc} measurements are done after annealing the samples. The following metric of

$\text{pFF change} = \frac{\text{pFF after anneal}}{\text{pFF before anneal}}$ Is used to analyze the effect of annealing.

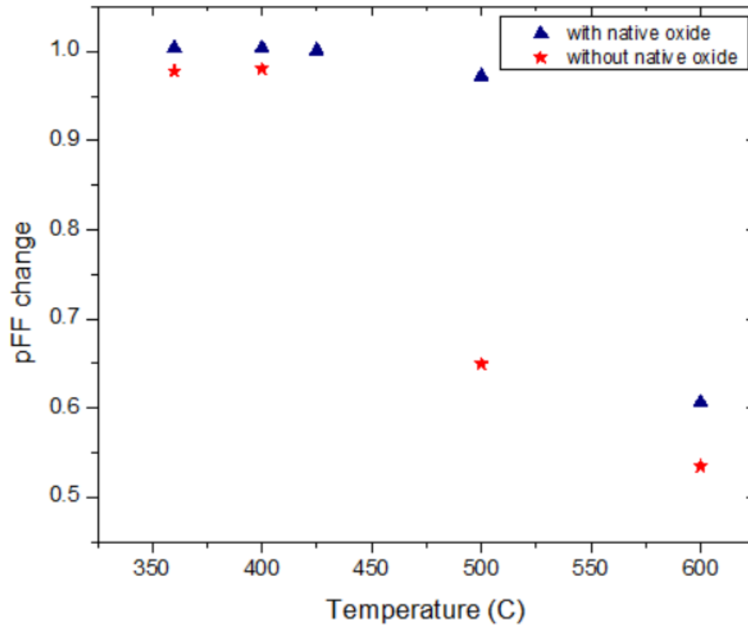


Figure 17 pFF change for samples with native oxide and without native oxide.

In Figure 17 it can be seen that the pFF change is very small at 360-400°C range. At higher temperature of 600°C there is considerable reduction in the pFF resulting in large pFF change. For samples annealed at 400°C the SunsVoc obtained was ~615mV which is in good agreement with pre-anneal values. For samples annealed at 600°C the SunsVoc reduced to below 100mV.

There is also a clear effect of BOE pretreatment before plating which can be seen in Figure 18, note the change in y-axis scale. At low temperatures of 360°C the sample

without oxide show a change of ~2% in pFF while the samples with native oxide show no change if pFF.

The above effects can be caused due to 1) shunting of the cell caused due to the $NiSi_x$ spiking through the junction 2) increased recombination sites due to the formation of metal silicide. The pFF reduction mechanism has been investigated in the following section using Photoluminescence and Illuminated lock in thermography.

In Figure 18 a plot shows pFF change in more detail. The samples without oxide undergo some deterioration due to annealing even at low temperatures. While samples with oxide have no effect at 400-425°C. This is an easy way to optimize the process space for annealing & plating parameters.

In Figure 19 the Suns Voc data for sample annealed at 400C for 2 minutes is shown. The pseudo Voc is 615mV and pFF is 81.5%. This is representative of the actual cell results and shows that the annealing process does not have any effect on the open circuit voltage of the cell. There is a good fit between the measured Suns V_{oc} curve and double diode model.

In Figure 20 the Suns Voc data for sample annealed at 600°C for 2 minutes without native oxide has been shown. The pseudo Voc is dropped to 84mV and the pFF is 37.5%. This drastic reduction in cell characteristics is due to metal induced recombination and shunting. The software is unable to fit measured Suns Voc curve to the double diode model.

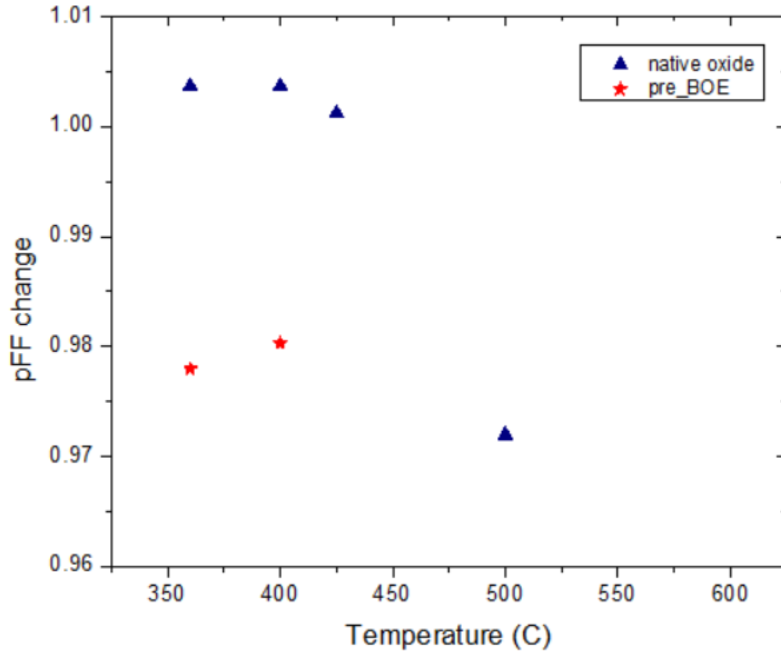
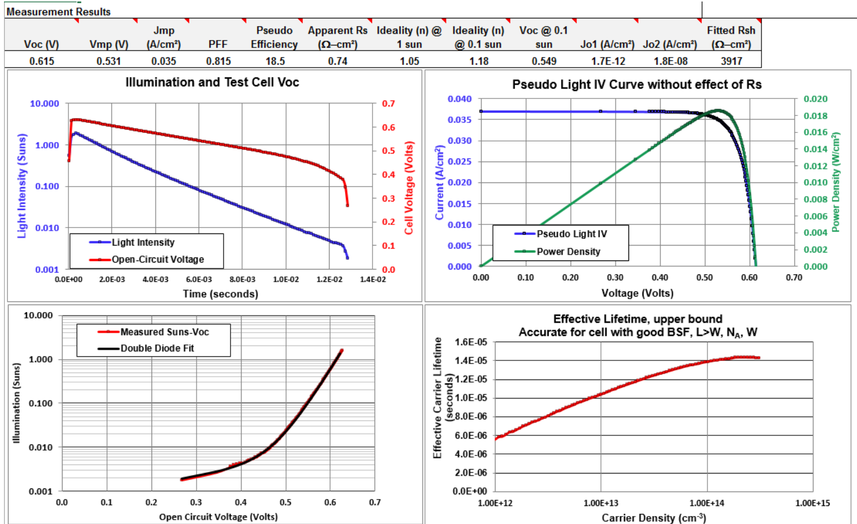


Figure 18 pFF change for 2 minute anneal from 350-500°C


Measurement Results

Voc (V)	Vmp (V)	Jmp (A/cm²)	PFF	Pseudo Efficiency	Apparent Rs (Ω–cm²)	Ideality (n) @ 1 sun	Ideality (n) @ 0.1 sun	Voc @ 0.1 sun	Jo1 (A/cm²)	Jo2 (A/cm²)	Fitted Rsh (Ω–cm²)
0.615	0.531	0.035	0.815	18.5	0.74	1.05	1.18	0.549	1.7E-12	1.8E-08	3917

Figure 19 SunsVoc data after annealing at 400°C for 2 minutes with native oxide.

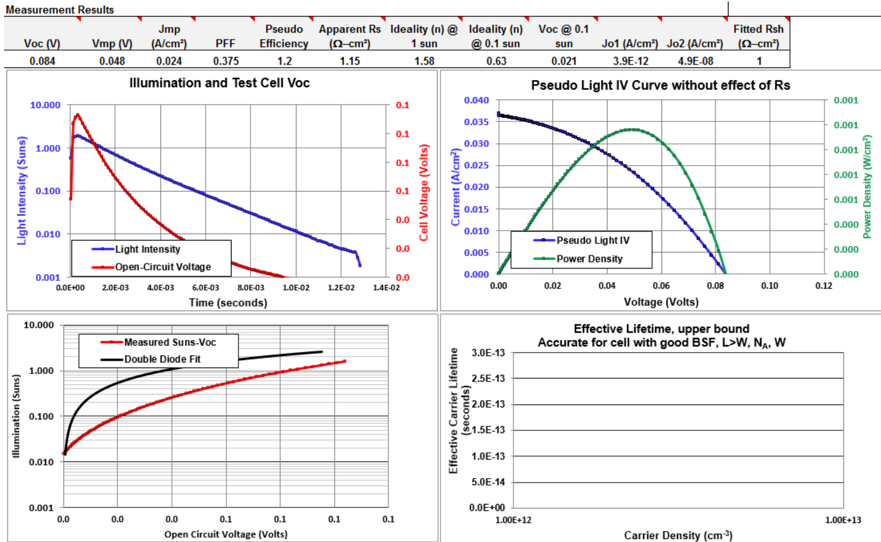


Figure 20 Suns Voc curve for cell without native oxide and annealed at 600°C for 2 minutes.

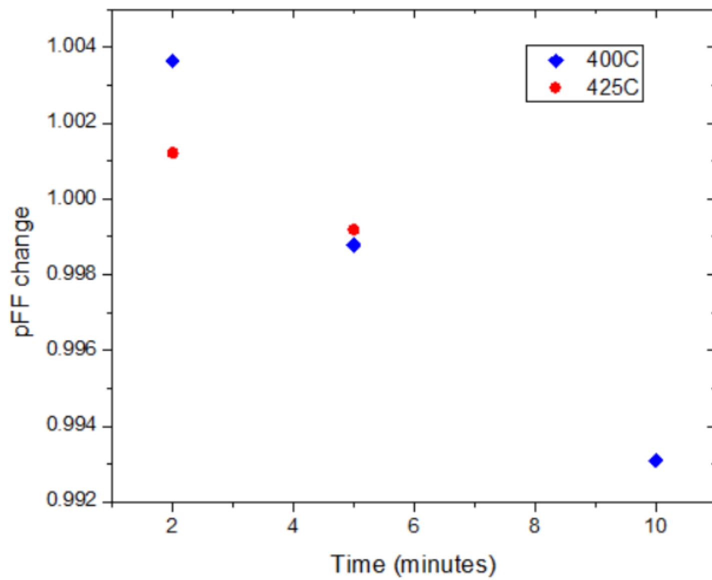


Figure 21 pFF change with different annealing time and temperature for samples with native oxide.

For further optimization of annealing time and temperature another set of experiments is carried out. In Figure 21 it can be seen that there is no pFF change 400°C 10 minutes

or 425°C 5 minutes and these are both equivalent. From Raman data in previous section it is known that if nickel atom are limited in supply annealing time can be increased at lower temperatures of 400°C. Since here the nickel supply is not limited the higher temperature of 425°C for 5 minutes is optimized annealing temperature.

Photoluminescence & Illuminated Lock in Thermography

Photoluminescence (PL) imaging is done by illuminating the solar cell by external light source resulting in photons from the band to band $e^{-}h^{+}$ pair recombination[43]. This techniques has been studied in detail for characterization of silicon solar cells[44].

A 40W, 808nm laser is used to spatially illuminate the wafer. A high resolution IR camera is used for detecting the PL signal. Intensity of the PL signal is directly proportional to the rate of radiative recombination.

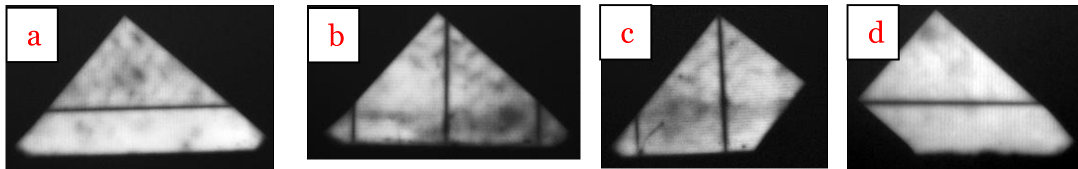


Figure 22 PL images after Ni plating

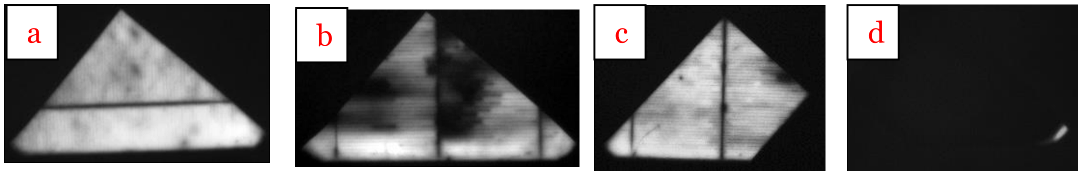


Figure 23 PL images after annealing for 2 minutes at a) 400°C b) 500°C c) 500°C d) 600°C

In Figure 22 the PL image after Ni plating is shown. In Figure 23 the PL image after annealing is shown. The 400°C 2 minute anneal in Figure 23a shows no change in PL intensity signal indicating that the annealing is causing no metal induced recombination at this stage. In Figure 23 b & c show the PL image after 500°C 2 minute annealing. There is significant reduction of PL intensity near the bus-bar in

both images. This reduction in intensity could be due to the Ni diffusion creating recombination center near the junction. Further increase in annealing temperature to 600°C results in no PL intensity. Only the pseudo corner of the wafer is visible in the image. This is due to the design of the plating holder which prevents plating of metal near the corners. Since, this region has significantly large region where there is no plating, metal induced recombination does not cause reduction in the PL intensity.
In Illuminated Lock in Thermography (ILIT) a pulsed illumination is used as an excitation source. The pulsed illumination allows for local heating and reduces the diffusion of heat to nearby regions. The solar cell can be illuminated under real operating conditions to evaluate spatial distribution of power loss and the various mechanisms of power loss. Wafers with p-n junctions without metallization can also be investigated using this techniques. For more details on this method refer[45], [46]. The setup has LED's on the stage and the wafer is p-n junction facing the LED. The camera vertically above the stage detects wavelengths in the 3-5µm range. In Figure 24 the ILIT images after Ni LIP have been shown. The bright spots on the corners and the edges are due to edge shunts due to processing and handling of the wafers. A bright spot on the bus-bar in Figure 24 b & c is due to repetitive laser ablation at the finger and bus-bar intersection. It is still not clear though why a particular spot on the bus-bar would be particularly affected by repetitive ablation. This may be due to the effect of random texturing at the particular location or a surge in laser power. After annealing images are shown in Figure *25*. There is no visible change in the 400°C anneal similar to the response in PL image. For the 500°C anneal in wafer b & c there is strong resemblance in the patterns observed in Figure 23 & Figure *25* b& c. Nickel silicide layer formed during annealing is forming deep spikes locally. These could be ohmic or non-ohmic shunts

which increase the dark current and reduce the voltage in that region leading to overall poor electrical characteristics.

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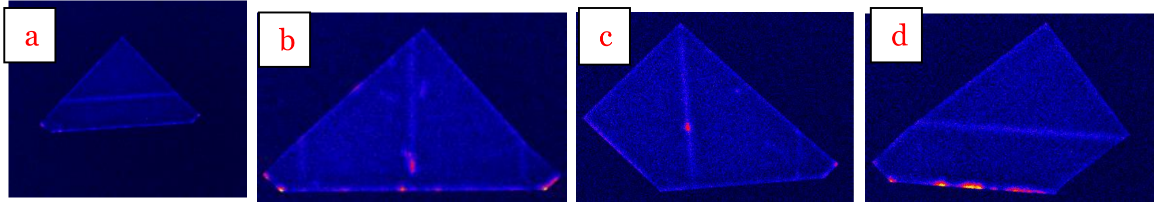

Figure 24 ILIT images after Ni plating.

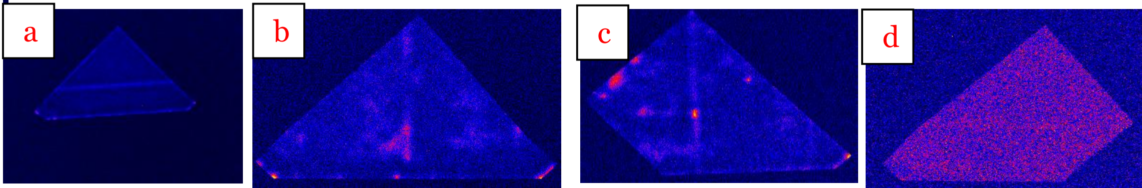

Figure 25 ILIT images after annealing for 2 minutes a) 400°C b) 500°C c) 500°C d) 600°C

Contact Resistivity

Contact resistance is an important measurement for metal-semiconductor contacts. A low resistance contact can result greatly improve the fill factor of the cell by reducing resistive losses at the contact. For the solar cell device photo-generated current enters from the n^+ emitter and flows vertically through the silicide to the Ni & Cu metal stack. To measure the contact resistivity of the sample two types of samples have been prepared. The first set of samples uses sputtered NiV (Ni-90%, V-10%). Before deposition SiO_2 was etched and sputtering was done on bare silicon.

Figure 26a shows the IV data for various pattern spacing. From the slope of the lines the resistance can be found. The resistance is then plotted against the spacing in Figure 26b. The calculations are done as shown in Table 6. Sheet resistance values obtained from the contact resistance measurement are compared with four point probe technique to gauge the accuracy of TLM pattern results.

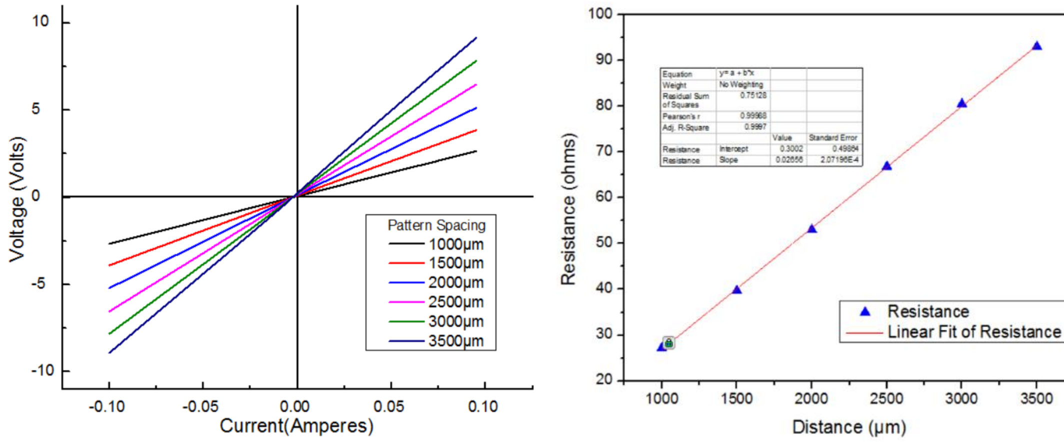

Figure 26 a) IV measurements for varying spacing b) Resistance v/s pattern spacing

In Figure 27 the contact resistivity before and after annealing for 2 minutes is plotted on semi-log scale. As the annealing temperature is increased the contact resistivity decreases as expected due to the formation of NiSi. The results clearly indicate the reduction in contact resistivity due to annealing and the importance of annealing at high temperatures.

Sample Id	DI0596-06	Equation
$R_{contact}$ (Ω)	0.15	y intercept/2
Transfer length (µm)	5.38	x intercept/-2
R_{sheet} (Ω/□)	79.69	Slope = R_{sheet}/width
ρcontact (mΩ-cm²)	0.02	R contact*transfer length*width
ρcontact (mΩ-cm²)	0.02	Transfer length = sqrt($\rho_{contact}$ /R_{sheet})

Table 6 Equations used for contact resistivity.

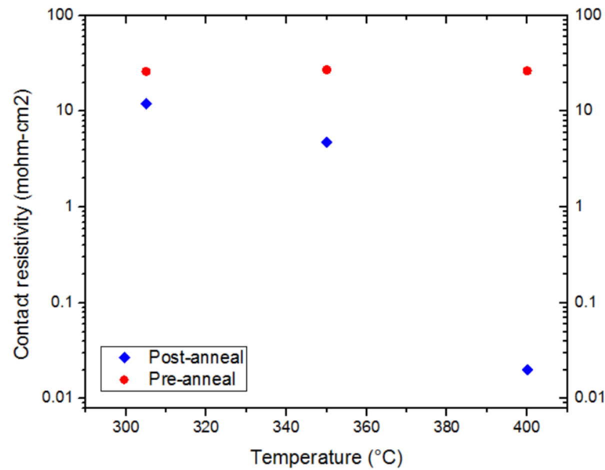

Figure 27 Contact resistivity of sputtered NiV before and after annealing.

For the second type of sample laser ablated samples metallized by LIP Ni and Cu are used as shown in Figure 28. TLM pattern is made to study the effects of native oxide and annealing conditions on the contact resistance. The measurements and calculations are done in the same way as shown above and the results are summarized in Table 7.

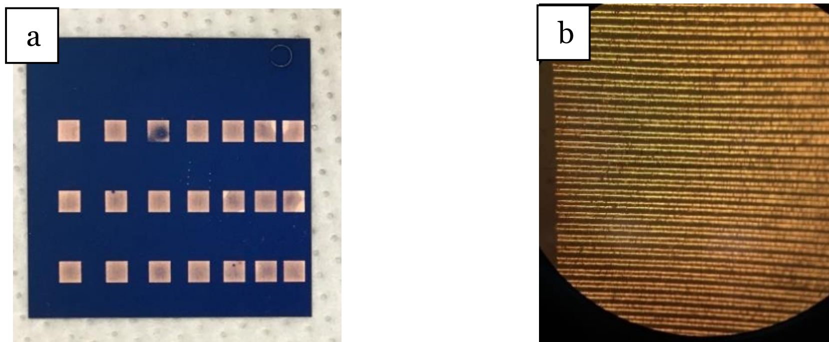

Figure 28 a) Image of contact TLM pattern b) optical microscope image of laser ablated pattern

The sample preparation for the TLM patterns is challenging and greatly affects the measurements. The laser scans can be made only in one direction to reduce damage to the underlying silicon. If vertical scan are also made then the local Voc drop is very high which inhibits the plating process which uses the photovoltaic property of the cell.

Conditions	Sample Id	Annealing temperature °C	Annealing time (minutes)	Contact resistivity mohm-cm^2
Without native oxide	DI0638-17-A	425	2	21.84
Without native oxide	DI0638-17-C	400	2	55.56
With native oxide	DI0638-14-A	425	2	64.39
With native oxide	DI0638-14-B	400	2	48.03

Table 7 Summary of measured contact resistivity values with and without native oxide.

Since the laser lines are not connected so the current would not flow through the metal. A silver based ink is tabbed onto the pattern after annealing and dried in muffle furnace. The probes are then contacted onto the silver pads to make measurements. The contact resistivity for samples with oxide is higher when compared to samples without native oxide. For samples without native oxide the resistivity decreases with increase in temperature but for samples with native oxide the opposite trend is observed. In general the contact resistivity for plated contacts has been high compared to that obtained from sputtered contacts. The sheet resistance of the semiconductor

obtained during the measurements was in-line with that measured using four point probe technique which shows that the measurements are correct.

Adhesion

Adhesion of coper directly to silicon is poor, so the use of nickel as an adhesion layer is important. Nickel on annealing forms a silicide which improves the adhesion of nickel copper stack. Forming a deep silicide is important for good adhesion but this can have negative impacts on the pFF as seen in the Suns V_{oc} study. Thus optimization of annealing conditions is very important to get good adhesion without affecting the electrical characteristics of the solar cell.

Plating time on the cells is controlled to form ~500nm of Ni and 8µm of Cu. For peel testing experiments a thin layer of Tin is also plated using LIP process. Then the bus-bars are soldered using lead solder coated 1.5mm wide ribbons along the length of the bus-bars.

The cells are using a 12mm Scotch 3M 401+ tape at 180° over fingers and bus-bars. The peel force measured is 0.30±0.08 N/mm with the tape width taken as a reference. The Ni-Cu plated cells passed tape test on the bus-bar while on the finger the results were not consistent throughout the wafer. Some fingers along the edges peeled off during tape test but the fingers in between bus-bars would adhere well. A 180° peel test is done at 200mm/min while the cell is held onto a vacuum chuck and the pull force is recorded in N/mm to take into account the width of the bus-bar. Three types of samples are used for this experiment. A silver paste printed cell, Ni-Cu plated cell with and without oxide annealed at 400°C for 5 minutes. The pull test data is plotted in Figure 29 for the 3 cells. The adhesion data from is varies greatly across the sample and thus can be difficult to state the actual peeling force between metal and silicon. Even though it is clear the Ag control samples have much greater

adhesion. It was also observed that during pull test of Ag control cells silicon started to peel off from the vacuum stage. This means that the adhesion between metal and silicon was not the point of failure. For sample with and without oxide the strength was consistently below 1N/mm and there was no difference between the two samples in case of adhesion.

It must also be noted that the bus-bar designed in the laser ablated cell is not a continuous metal strip but is made up of an array of fingers as shown in Figure 30. This reduces the effective area of metal in contact with silicon. A simple solution to this problem would be to increase the number of scans in the bus-bar region. This results in severe damage to the underlying crystalline silicon due to multiple overlapping scans of the laser patterning process. This process would also increase the time for pattering thus reducing throughput.

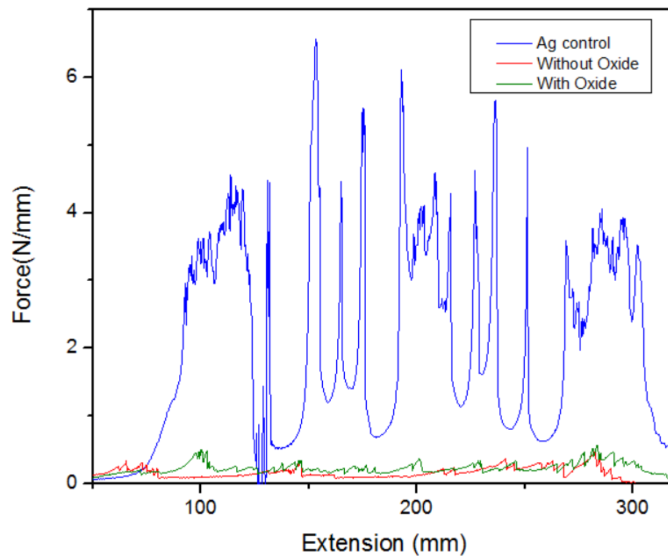

Figure 29 Peel test data for Ag control and Ni-Cu plated cell with and without oxide

Since, the adhesion of laser ablated cells has been significantly poor as compared to the Ag control cells other bus-bar less interconnect strategies need to be investigated. Another way to verify if adhesion can be improved is to anneal at high temperatures of

500°C for 10 minutes. This severe thermal budget will ensure a uniform and deep silicide layer formation but will cause severe deterioration of the photovoltaic properties of the cells. The LIP process uses the photovoltaic property of the cell so subsequent plating after severe annealing will be greatly affected due to low Voc along the grid pattern.

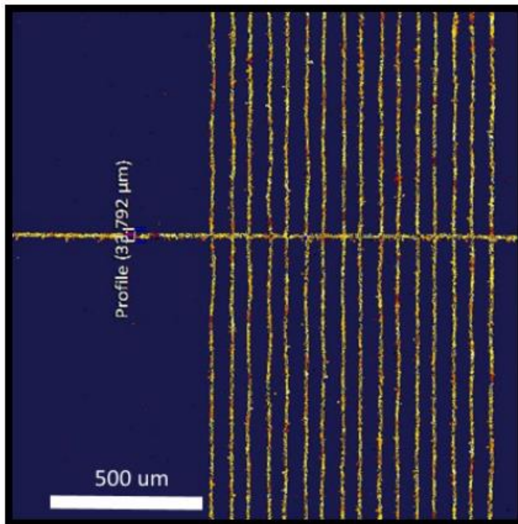

Figure 30 Optical microscope image of bus-bar and finger intersection[47].

Ghost Plating

Ghost plating is the unintentional plating of metal on the dielectric layer where the grid pattern has not been made. This can happen due to the presence of pin holes in the film where the n^+ emitter is exposed to the electrolyte, breakdown of dielectric and highly porous dielectric layer. The pinholes then become regions where metal ions from the electrolyte get reduced during the LIP process causing nucleation sites for metal deposition. The ghost plating depend mainly on the conditions at which the SiNx was deposited and the subsequent processing that it undergoes. Ghost plating is undesirable as it can have detrimental effects on the performance of the solar cell. Firstly, ghost plating reduces the optically active area and this reduces the photo-generated current.

Secondly, there is metal in direct contact with silicon which will increase surface recombination and reduce the voltage of the cell.

In Figure 31 below the solar cell is introduced in BOE for 20 seconds to remove native oxide just before the plating process. The optical microscope images show that there is ghost plating on the nitride layer where the laser patterning has not been done. To find the root cause of ghost plating another sample is made with identical processing but without any pre-treatment of 20 second BOE before plating. The images using the same 50x magnification are shown in Figure 32. There is little or no ghost plating. This implies that the BOE treatment before plating is opens pinholes in the SiNx layer.

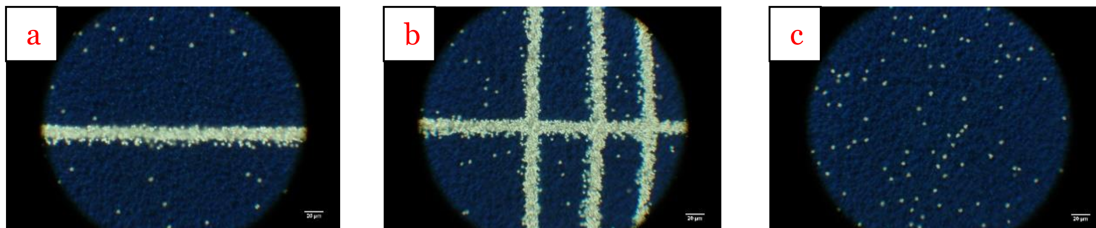

Figure 31 Optical microscope images of Ni plating with BOE a) Finger b) Bus-bar & c) between fingers.

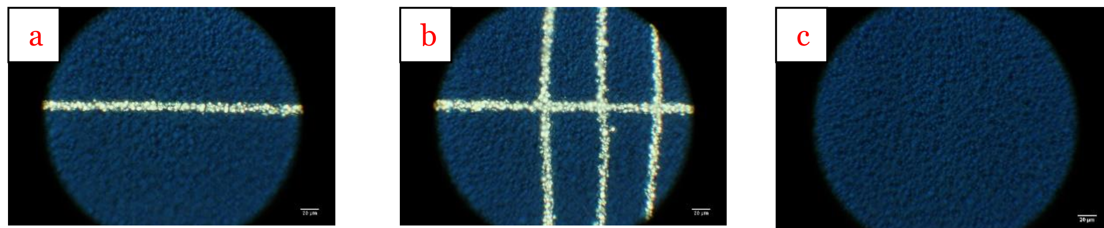

Figure 32 Optical microscope images of Ni plating without BOE a) Finger b) Bus-bar & c) between fingers.

In Figure 33 the reflectivity of the SiNx film is measured and plotted showing that there is a change reflectivity due to the BOE treatment. This change is mainly due to the reduction in thickness of the SiNx film because the BOE is etching a few nanometers of the film. There is a shift in the minima from 600nm to 550nm caused

due to the pre-treatment. This reduction in film thickness causes increases ghost plating on the cells.

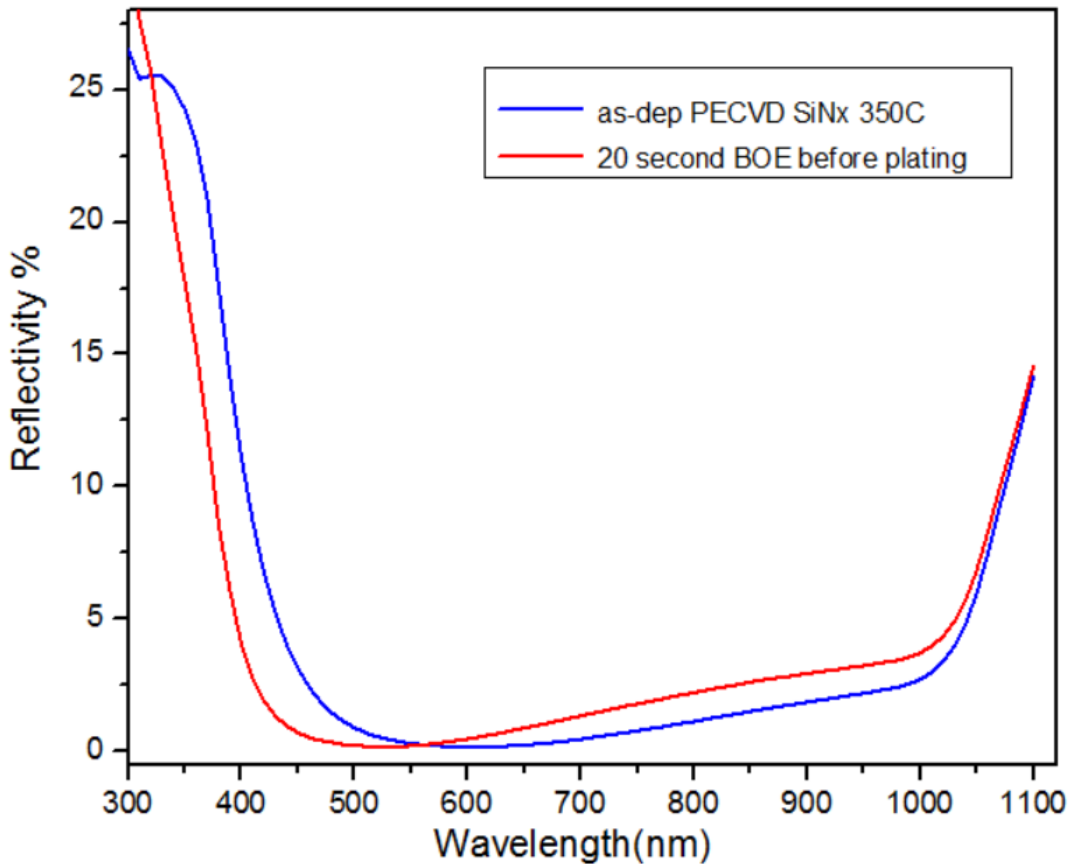

Figure 33 Reflectance of SiNx film before and after 20 second BOE treatment.

Cell results

IV curves are measured using flash tester by Sinton Instruments. The tester measures the short circuit density J_{sc}, open circuit voltage Voc, Fill Factor FF and maximum power point. The pseudo IV curve is also measured using the Suns Voc measurement. The series resistance is calculated by the difference between the pseudo IV curve and actual IV curve.

The cells evaluated here have been plated with Ni/annealed/re-plated with Ni/ Cu. In Figure 34 a box plot showing the pFF for cells made with and without native oxide is

plotted. The range for the pFF values for cells made without native oxide is very large compared to the cells made with the native oxide. Also the pFF values for cells without oxide is below 80% other than a few outliers indicating there is shunting & recombination happening due to the annealing. This is in-line with the Suns Voc measurements shown in the previous section. The pFF for cells with the native oxide is consistently above 80% indicating that the cells are not shunted during the annealing process.

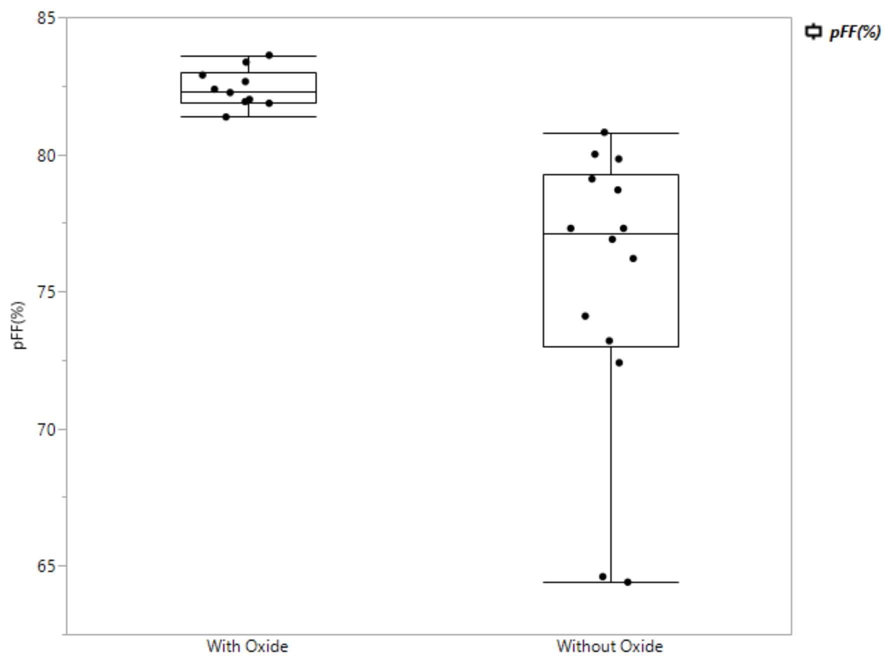

Figure 34 Comparison of pFF after with and without oxide after annealing.

Sample ID	Jsc mA/cm²	Voc mV	Eff %	Rseries Ω-cm²	Rshunt Ω-cm²	FF%	pFF %	pEff %
DI0657-12 400°C 5 min	36.6	633	13.34	4.143	9912	57.56	82.26	19.06
DI0638-02 425°C 5 min	36.6	608.2	16.51	1.225	4717	74.05	80.54	17.95

Table 8 IV results of large area plated cells with native oxide and annealed at 400°C for 5 minutes.

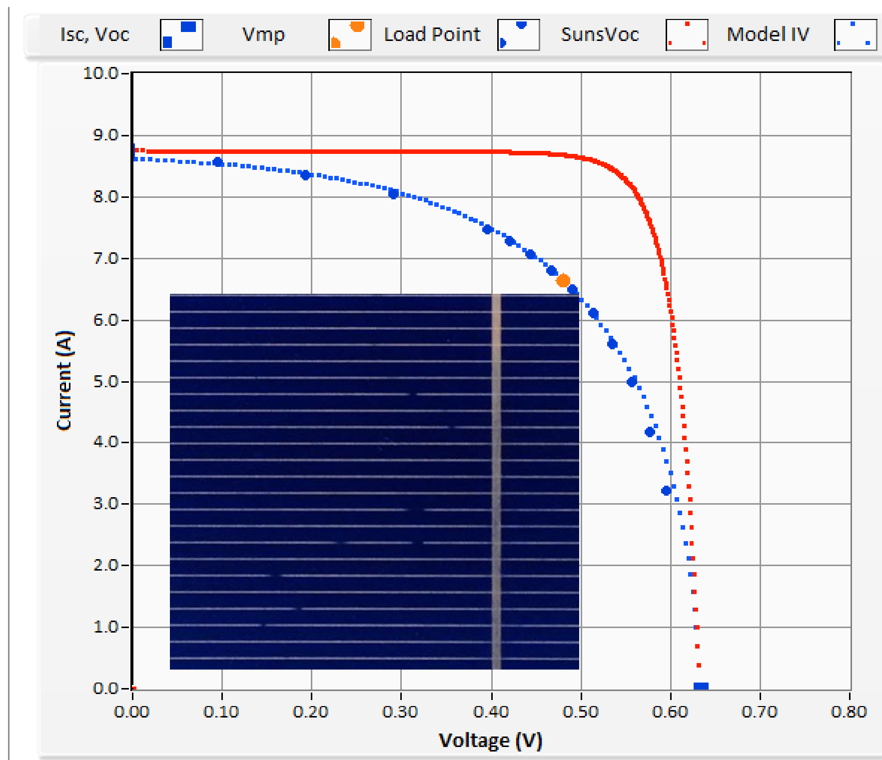

Figure 35 DI0657-12 measured IV and Suns V_{oc} curve with an inset image showing broken fingers.

In Table 8 and Figure 35 is the summary of the measured IV data of cell plated with native oxide and annealed at 400°C for 5 minutes. The V_{oc} and J_{sc} for the cells is equivalent to the cells with silver paste at Solar Power Labs, ASU. The series resistance of the cell is 4.143 Ω-cm^2 which is leading to reduced FF and efficiency. The inset in Figure 35 shows an image of the broken fingers on the front grid caused during the processing of wafers. The discontinuous finger and bus-bars can be seen more closely in Figure 36a. The discontinuity results in increased series resistance. In Figure 36 the electroluminescence of the cell is shown. During EL the solar cell is forward biased. In EL image the series resistance and the local recombination can cause change in the contrast. Acquiring images with cooled CCD camera by applying high current densities show the effect of series resistance. In Figure 36 the discontinuous bright lines between the bus-bars show are due to broken fingers.

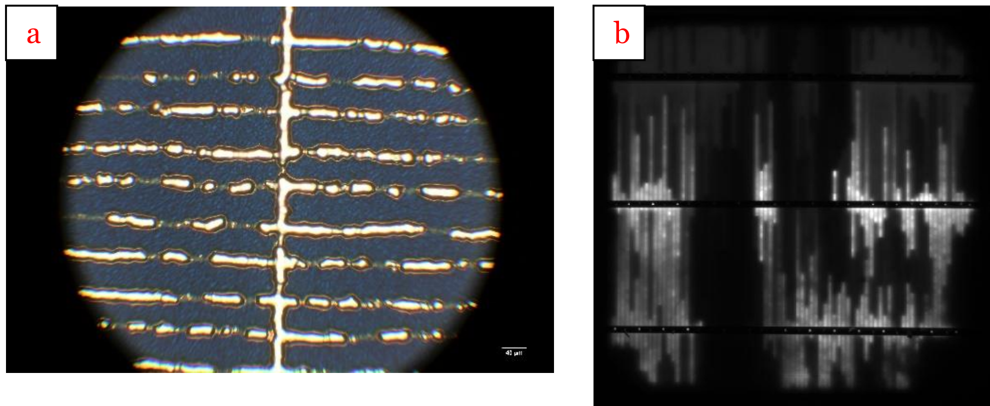

Figure 36 a) Optical microscope image of bus-bar b) Electroluminescence image of plated cell.

CHAPTER 5

DISCUSSION

Future Work

There are many aspects of Nickel-Copper plating that still need to be investigated for solar cells. Some of these are related to solar cell itself like the junction depth and surface concentration. Others are related to the patterning of the front grid and plating and annealing parameters to get better adhesion & IV properties.

1. Junction engineering is required to achieve good adhesion. The drive-in of the emitter will allow the use of higher thermal budget for silicide formation. The silicide layer thickness is an optimization between contact resistance and shunt resistance. Epitaxial grown wafers might be more suitable for plating since it is easy to control junction depth and surface concentration.
2. With the incorporation of lasers the feature size of $<10\mu m$ can be achieved. Moving to a no bus-bar design with multi-wire interconnects may result in improved performance and simpler process flow. Optimization of the front grid for minimal optical shading and resistive losses based on finger linewidths and contact resistance.
3. Selective emitter offers opportunities to further reduce the series resistance by having highly doped and deep regions of phosphorus on the surface. This can reduce contact resistance although it will add more processing steps which may or may not be economical.
4. Adhesion of metal to silicon and reliability testing of plated contacts as per industry standards is required. This will give insight if there is any power degradation during the lifecycle of the cell and its mechanism and failure points.

5. Demonstration of applying knowledge to other high efficiency cell architectures like PERC. The formation of nickel silicide layer should not vary drastically depending upon cell architecture. The metallization scheme described in this work should be applicable to other silicon solar cell architectures with Ni-Cu plated metallization.

Conclusion

The main goal of this work was to understand the formation of nickel silicide with and without native oxide to evaluate its effects on the electrical and mechanical properties of nickel-copper plated silicon solar cell. Using LIP technique it has been shown that it is feasible to deposit metal on SiO_2.

Copper metallization offers a cheap and sustainable alternative to silver paste metallization. Although the implementation of this technology in the industry has been hindered due to issues related performance, reliability & high volume manufacturing.

The main contributions of this work are:

1. Using Raman spectroscopy to identify key parameters that can be controlled during the processing steps to form desirable phase of Nickel mono-silicide.
2. The use of native oxide formed on the silicon surface acts as diffusion barrier at low temperature to Ni atoms and promotes formation of NiSi. This also resulted in formation of a thinner silicide layer being formed at the Ni-Si interface confirmed by Rutherford backscattering analysis.
3. Suns V_{oc} measurement is a fast and non-destructive technique that can be used to optimize the annealing parameters and monitor the process effects on the solar cell. In conjunction with Photoluminescence and Illuminated Lock in

thermography the mechanism related to the deterioration of the cell parameters can be monitored.

4. The avoidance of pre-treatment step of BOE eliminates ghost plating.
5. Large area devices on 156mm substrates were fabricated using the above process. Cell results of 16.5% are promising and further process development and optimization can significantly improve the cell performance.

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