Ion Transport in Surface Modified Cylindrical Silicon-on-Insulator Nanopore with Field Effect Modulation

by

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ABSTRACT

Solid-state nanopore research, used in the field of biomolecule detection and separation, has developed rapidly during the last decade. An electric field generated from the nanopore membrane to the aperture surface by a bias voltage can be used to electrostatically control the transport of charges. This results in ionic current rectification that can be used for applications such as biomolecule filtration and DNA sequencing.

In this doctoral research, a voltage bias was applied on the device silicon layer of Silicon-on-Insulator (SOI) cylindrical single nanopore to analyze how the perpendicular gate electrical field affected the ionic current through the pore. The nanopore was fabricated using electron beam lithography (EBL) and reactive ion etching (RIE) which are standard CMOS processes and can be integrated into any electronic circuit with massive production. The long cylindrical pore shape provides a larger surface area inside the aperture compared to other nanopores whose surface charge is of vital importance to ion transport.

Ionic transport through the nanopore was characterized by measuring the ionic conductance of the nanopore in aqueous hydrochloric acid and potassium chloride solutions under field effect modulation. The nanopores were separately coated with negatively charged thermal silicon oxide and positively charged aluminum oxide using Atomic Layer Deposition. Both layers worked as electrical insulation layers preventing leakage current once the substrate bias was applied. Different surface charges also provided different counterion-coion configurations. The transverse conductance of the nanopore at low electrolyte concentrations ($<10^{-4}$ M) changed with voltage bias when the Debye length was comparable to the dimensions of the nanopore.

Ionic transport through nanopores coated with polyelectrolyte (PE) brushes were also investigated in ionic solutions with various pH values using Electrochemical Impedance spectroscopy (EIS). The pH sensitive poly[2–(dimethylamino) ethyl methacrylate] (PDMAEMA) PE brushes were integrated on the inner walls as well as the surface of the thermal oxidized SOI cylindrical nanopore using surface-initiated atom transfer radical polymerization (SI-ATRP). An equivalent circuit model was developed to extract conductive and resistive values of the nanopore

in ionic solutions. The ionic conductance of PE coated nanopore was effectively rectified by varying the pH and gate bias.

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1. INTRODUCTION

Sequencing of DNA strands and rapid detection and separation of specific biomolecules like peptides, virions, proteins, enzymes and other biomolecular complexes through a nanopore are of vital importance to various biomedical applications and bioanalytical studies (Howorka, Siwy 2009). This field which pioneered with gramicidin peptide pores reconstituted in artificial lipid membranes drew exponentially increasing interests within the last decade after it has been maturely developed using α-hemolysin (αHL) pores (Bayley 2000, Hladky, Haydon 1970). These biological pores were functionalized with artificial binding sites and could therefore detect a broad range of analytes. However, they had inevasible shortcomings such as small pore size, thermal, chemical, and physical variation restrictions. These challenges prevented researchers from a thorough understanding and control of ionic and molecular transport and encouraged them to develop man-made devices. In the recent 10 years, researchers consecutively fabricated solid-state nanopores using silicon nitride (Fologea 2005, Ho, Qiao et al. 2005, Li, Stein et al. 2001, Stein, McMullan et al. 2004), glass capillaries (Zhang 2004), silicon or silicon-on-insulator (Chang, Iqbal et al. 2006, Storm, Chen et al. 2003, Petrossian, Wilk et al. 2007a, Petrossian, Wilk et al. 2007b), carbon nanotubes (Henriquez, Ito et al. 2004, Ito 2004), and graphene (Schneider 2010). Unlike the gramicidin peptide and αHL pores having fixed size, solid state nanopores can be fabricated with different sizes and shapes according to specific processing method. Also, these "abiotic" channels have an almost unlimited lifetime and are chemically, mechanically, electrically and thermally robust and stable. The ionic and biomolecular transport in the nano-channels can be studied under different parameters such as channel sidewall surface charges, transmembrane voltage, chip bias voltage, electrolyte solution pH, ionic strength and temperature in a wide range. Furthermore, the solid state materials enable the nanopore chip to be integrated with electronic circuits forming independent low-cost biosensor devices.

1.1 Review of Existing Solid-State Nanopores

The solid-state nanopore used for DNA molecule sensing was pioneered by Li et al using silicon nitride membrane by the ion sculpting technique (Li, Stein et al. 2001, Li, Gershow et al.

2003). The Si_3N_4 membrane was flat on one side and had a bowl shaped cavity on the other side. A feedback-controlled Focused Ion Beam (FIB) drilling system generated massive high energy argon (Ar) ion beams sputtering on the flat surface of the membrane to remove the materials from the surface, and then precisely stopped the erosion process as soon as breakthrough was achieved by counting the ions transmitted through the opening pore (Fig. 1.1 Left). Right after they got the open pore size which was much larger than that of the molecule, it was shrunk to molecular scale by exposing it to an ion beam at room temperature due to a lateral atomic flow of matter into the pore (Fig. 1.1Right a). The resulting nanopore then bridged two insulated reservoirs of KCl ionic solution for DNA molecule sensing (Fig. 1.1Right b). Current blockades appeared in the form of isolated transient reductions in current flow once the DNA passing through the pore (Fig. 1.1Right c) and the current magnitude was clearly quantized.

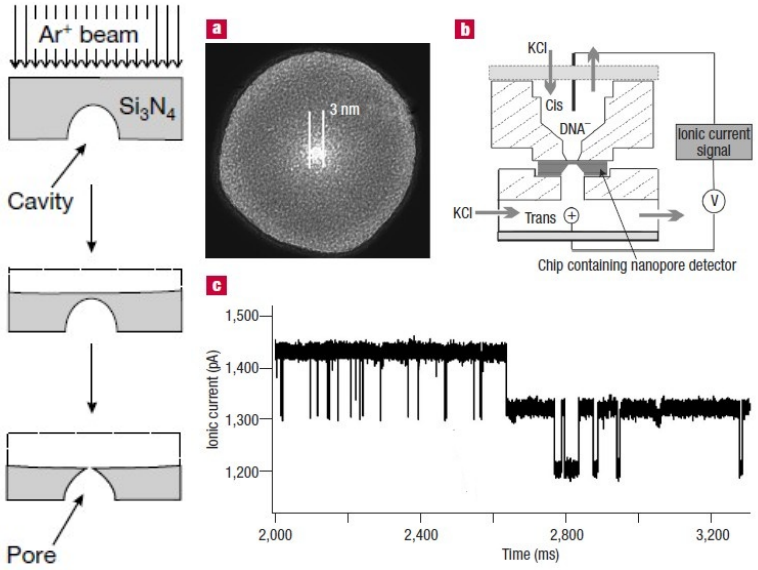


Figure 1. 1: Process flow and molecules sensing for the first solid-state pores. Left: Sputtering removes material from a free-standing Si_3N_4 membrane with a cavity. Right: (a).Transmission electron microscopy (TEM) image of a 3 nm silicon nitride nanopore. (b). Nanopore single DNA transport sensing experiment setup. (c). Current trace with introduction of 3-kilobase long (1 μm) double stranded DNA to the reservoir.

Storm et al. similarly used electron beams from TEM for shrinking the silicon dioxide pore, starting with a SOI wafer as shown in Figure 1.2 (Storm, Chen et al. 2003). A larger pore was formed at the silicon device layer and BOX layer interface after the silicon on both sides was anisotropically wet etched with KOH from square windows and the BOX layer in the windows was removed in buffered hydrogen fluoride. The pore was then thermal oxidized and left an opening of 20*20 nm^2. It was further shrunk to several nanometers by the electron beam which had the intensity around 10^5 to 10^7 Am^{-2} in a TEM with an accelerating voltage of 300 kV. The physics of the observed fine tuning of nanopores was determined to be driven by the surface tension of the viscous silicon oxide.

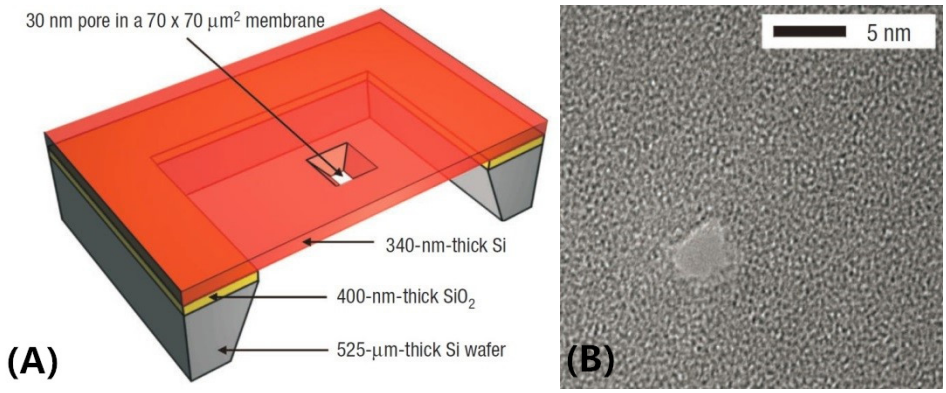


Figure 1. 2: SOI nanopore. (A) Illustration diagram of the nanopore device. (B) TEM imaging of silicon oxide nanopore after electron irradiation.(Storm, Chen et al. 2003)

Ion beam sculpting and electron beam tuning were the two most prevalent methods of fabricating silicon material nanopores. Besides that, carbon nanotube nanopores wwere prepared by microtoming a multi-wall carbon nanotube (MWNT) attaching on a TEM grid with epoxy (Ito 2004). It provided benefits of smooth sidewalls and identical size. A graphene nanopore was obtained by drilling a nanopore into the graphene monolayer which was attached on SiN support membrane with a 5 μm hole, using the highly focused electron beam of a TEM (Schneider 2010). The ultra-thin thickness of graphene nanopores had the potential to enhance the measurement resolution. The approach to generate glass nanopipettes with diameters of 40 nm used a

commercially laser-based pipette puller (Karhanek, Kemp et al. 2005). The pulled glass nanocapillary could be easily positioned at any point within a microfluidic channel. Researchers used diversified ways of fabricating nanopores with different materials, which opened up more fields of application for nanopores and initiated the rapidly development in the nanopore field.

1.2 Ionic Transport in Nanochannel with Field Effect Modulation

Unlike in macro-fludics, the surface charges play a very important role on the ionic transport through nanopores since the surface charges related Electrical Double Layer (EDL) has the comparable size and covers most or all the region of nanochannels. The surface charge profile can be changed by a DC voltage bias applied on the nanopore membrane which is completely covered and electrical isolated by an insulating surface (eg. silicon oxide). This configuration is analogous to a metal–oxide–semiconductor field-effect transistor (MOSFET) which consists of drain, source, gate terminal, gate dielectric and a thin conducting channel right below the gate dielectric (Fig. 1.3). In the SOI ionic field effect transistor, a gate voltage is applied on the silicon device layer, V_{DS} is applied in one side of the bath and ionic current I_{DS} is regulated by different V_G and V_{DS}. The influence of the nanopore channel walls surface charge on ionic flow by the gate bias has significant implications for rectification of ionic current (Siwy, Heins et al. 2004, Jiang, Stein 2011, Nam, Rooks et al. 2009, Karnik, Fan et al. 2005), biomolecules filtering (Nadtochiy, Melnikov et al. 2013) and potentially for slowing down DNA sequencing (Fologea, Uplinger et al. 2005).

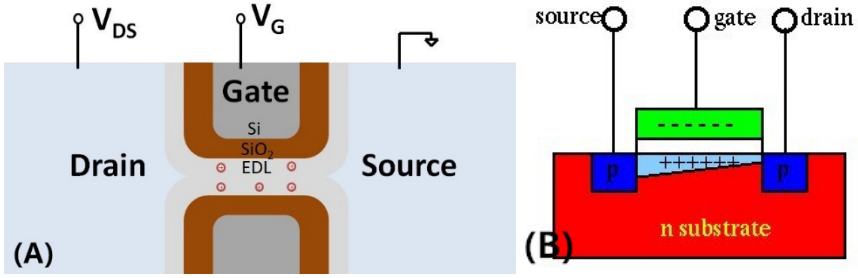


Figure 1. 3: The chip voltage biased nanopore is analogous to MOSFET device. (A) Cross section of a SOI nanopore in ionic solution. (B) Diagram of a PMOS transistor.

Several groups have studied on how the gate bias changed the ionic current flow through the nanochannel. Nam, Rooks et al fabricated 10 nm Si_3N_4/TiN/Si_3N_4 nanopore covered by ALD negatively charged TiO_2 gate dielectric using E-beam lithography and Reactive Ion Etching (RIE) (Nam, Rooks et al. 2009). They found the I_{DS} increased with negative V_G. However, they counted all the surface charges contributing to the ionic current and ignored the fact that some ions in the stern layer are immobilized. Jiang and Stein deposited Cr on Focused Ion Beam (FIB)-drilled Si_3N_4 pores. They shrank and isolated the pore using ALD aluminum oxide and found out that I_{DS} slightly increased with V_G. However, they mixed more than one cation and used cations with different mobilities, which complicated the ionic flow.

In our group, a 340 nm long cylindrical SOI nanopore was fabricated. The nanopore process flow was compatible with standard cleanroom facilities for a high throughput fabrication and it had the ability to be integrated into any electronic circuit constituting an advanced biosensor with the potential for large-scale production. The gate voltage was applied on the silicon membrane, which was completely covered with negatively charged thermal silicon oxide layer, positively charged ALD aluminum oxide layer and pH sensitive polyelectrolytes (PE) brushes respectively for comparison. The ionic current was investigated under different voltage bias in different aqueous solutions. The 360 nm longer cylindrical nanopore provided more surface area inside the channel compared to other pores. A more obvious impact of V_G on the I_{DS} was observed.

Chapter 2 presents in detail the microfabrication process flow of a cylindrical nanopore with silicon dioxide surface on silicon-on-insulator substrate and introduces the high aspect ratio aluminum oxide etching process.

Chapter 3 describes the nanofludics concept, the ionic current measurement setup, the experimental protocol and the results of ion transport experiments performed on SOI nanopores with field effect modulation.

Chapter 4 introduces Surface-Initiated Atom Transfer Radical Polymerization (SI-ATRP) of polyelectrolyte brushes on SOI nanopore and studies ionic transport in polyelectrolyte brush coated SOI nanopores with field effect modulation.

2. FABRICATION OF SILICON-ON-INSULATOR NANOPORES

2.1 Fabrication Process Flow of Silicon-On-Insulator (SOI) Nanopores

The SOI nanopore process flow was first designed, utilized and calibrated by Dr. Leo Petrossian in ASU Center for Solid State Electronics Research (CSSER) cleanroom facilities in 2007 as shown in Figure 2.1 (Petrossian, Wilk et al. 2007a, Petrossian, Wilk et al. 2007b). The 4-inch wafer was purchased with the silicon-on-insulator (SOI) structure which had a 340 nm top silicon layer, 450 μm thick p-type handle silicon wafer and a 1 μm buried oxide (BOX) layer (Fig. 2.1A). The fabrication started with patterning nanopores on the device (top) layer. Before the patterning, the wafer was put into a dry oxygen atmosphere furnace at 1000°C for 60 mins. A 60 nm layer of SiO_2 was thermally grown covering the whole wafer as a hard mask for etching the device layer. This oxidation consumed about 30 nm of the device layer, resulting in the top silicon thickness decreasing to 310 nm. The thickness of the each layer was measured by Woollam WVASE32 variable angle ellipsometer every time before and after each processing step. When the wafer was handled from the ellipsometry stage or from the other processing tools' wafer stage to the wafer holder, particles attachment on the wafer was avoided to the best effort by blowing with a nitrogen gun or other cleaning methods. Particles on the wafer would cause pinholes or defects during the deposition of the next layer, which might destroy the whole process. For example, the wafer might get punched through during a deep RIE processing at that pinhole's position. The device layer was then spin coated with 6% polymethyl methacrylate (PMMA) in methoxybenzene at 3000 rad/min for the electron beam lithography patterning. 15 minutes hard bake on hot plate at 170°C was applied and the film with a thickness of 230 nm was obtained (Fig. 2.1B). A larger thickness was chosen compared to Leo's process to achieve bigger etch resist processing margin of PMMA being left for the device layer etching. A PMMA layer with 230 nm thickness was able to provide a feature size resolution up to 30 nm.

The wafer was then exposed in the JEOL JBX-6000FS/E EBL system with an area dose of 800 $\mu C*cm^{-2}$ to pattern a 7*7 dies array. Each die had an either 100 nm or 150 nm diameter filled circle in the center and alignment markers at the edge. The wafer cassette had a slight mechanical flatness issue which had several microns height deviation from one side to the other

side. During the exposure, the 7*7 array was divided into subgroups of 2 dies or 4 dies for each group according to the focus variation. Every group was separately exposed and it was re-focused using electron beam burn test before the exposure. After long time exposure on the whole array, the wafer was developed in an ASU proprietary recipe solution which mixed eleven parts methyl isobutyl ketone: isopropanol 1:3 with ten parts 2-ethoxyethanol: methanol 3:7 with one part methyl ethyl ketone: ethanol 26.5: 73.5 for 20 seconds in room temperature, and then immersed in isopropanol for 25 seconds followed by the drying step using nitrogen gas. A one minute hard bake at 100°C on the hot plate was utilized right after the development to strengthen the PMMA etch resistance, straighten the resist sidewalls and sharpen the corners. Then the pattern depth was measured by Bruker Dektak XT stylus profilometer check whether it was exposed and developed properly. After the lithography, the pattern was transferred to the SiO_2 hard mask by an Oxford Instruments Plasmalab 80+ Reactive-ion Etching (RIE) tools using CHF_3:Ar 25 sccm: 25 sccm chemistry at 30 mTorr with 25 watts forward power for 20 mins (Fig. 2.1C). The etch rates were 6 nm/min for SiO_2 and 3 nm/min for PMMA at the plane surface so 100% over etch was used on the 100 nm feature size pattern. The nanopore pattern was then transferred to the silicon device layer by Inductively Coupled Plasma (ICP) RIE using a Surface Technology Systems Advanced General Etch (STS-AGE) tool. The silicon etch recipe, which was 10 sccm Cl_2 gas, 500 watts coil power, 50 watts platen power and 6 mTorr pressure, provided the etch rate of 200 to 250 nm/min on Si and 20 nm/min on SiO_2. 2 minutes and 20 seconds etch time was applied. Cl_2 plasma in the ICP-RIE provided a very good anisotropic etch and resulted in a vertical and smooth sidewalls (Fig. 2.1D). This was the crucial step to generate a straight long cylindrical nanopores profile for the whole processing. The remaining PMMA from last step was removed by Cl_2 plasma gas removed the PMMA very fast compared to the etch rate on Si.

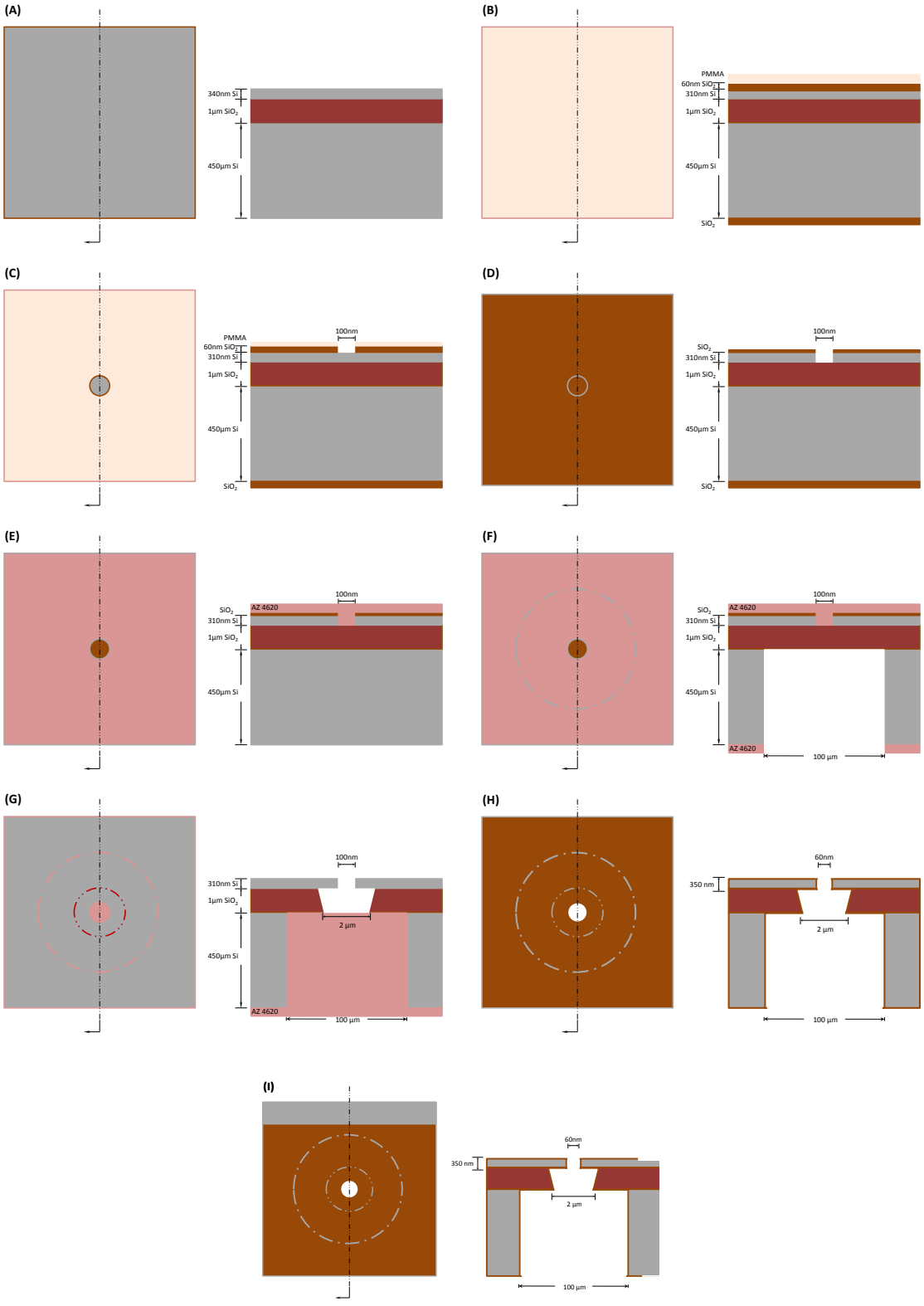

(A)
340nm Si
1µm SiO2
450µm Si
(B)
PMMA
60nm SiO2
310nm Si
1µm SiO2
450µm Si
SiO2
(C)
PMMA
60nm SiO2
310nm Si
100nm
1µm SiO2
450µm Si
SiO2
(D)
SiO2
310nm Si
100nm
1µm SiO2
450µm Si
SiO2
(E)
SiO2
310nm Si
AZ 4620
100nm
1µm SiO2
450µm Si
(F)
SiO2
310nm Si
AZ 4620
100nm
1µm SiO2
450µm Si
AZ 4620
100 µm
(G)
310nm Si
100nm
1µm SiO2
2 µm
450µm Si
AZ 4620
100 µm
(H)
350 nm
60nm
2 µm
100 µm
(I)
350 nm
60nm
2 µm
100 µm

Figure 2. 1: Complete process flow for the fabrication of a single cylindrical SOI nanopores. The left picture is the die top view from the device layer, and the right one is the cross section view from the center of the pore. (A) The SOI water from the factory. (B) Growth of a mask layer of 60 nm SiO_2 using thermal oxidization in dry atmosphere and spin coat a layer of 6% PMMA. (C) Opened a 100 nm diameter aperture using EBL and etched the SiO_2 using RIE with CHF_3: Ar gas. (D) Etching of the Si device layer in an ICP RIE with Cl_2 gas. (E) Protecting of the device layer using photoresist AZ4620 and removal of the bottom SiO_2 layer using BOE 20:1. (F) Opened a 100 μm diameter aperture using photolithography and etched the Si bulk to the BOX layer using Bosch process. (G) Protecting of the backside wafer and etching of BOX Layer from the device layer using BOE 20:1. (H) Thermal oxidation in dry atmosphere to provide electrical isolation. (I) Obtained an access to the device layer by BOE 20:1 dip from the edge of the die.(Petrossian, Wilk et al. 2007b, Petrossian, Wilk et al. 2007a)

The processing was flipped to the backside of the wafer after etching of the device layer. The 60 nm thermal SiO_2 layer on the backside was removed first. Before that, the device layer was protected by being spin coated with a layer of AZ 4620 positive photoresist at 2500 RPM, followed by 5 minutes oven bake at 120°C which resulted in an 8.5 μm resist protective layer. The device layer was then immersed in Buffered Oxide Etch (BOE) 20:1 for 5 minutes. The etch rate of BOE 20:1 on the thermal SiO_2 was about 27 nm/min so that 5 minutes gave sufficient over etch time to remove all the SiO_2 on the backside (Fig. 2.1E). The wafer was cleaned by being immersed in AZ 400T photoresist stripper at 110°C for 5 minutes followed by water rinse to remove the AZ 4620 resist at device layer. The device layer was then recoated a layer of AZ 4620 positive photoresist at 2500 RPM and oven baked at 120°C for 5 minutes to protect the surface during backside etch.

Hexamethyldisilazane (HMDS) was spin coated on the backside of the wafer at 2500 RPM to promote the adhesion of the photo resist which was spin coated at 2500 RPM next upon that. The wafer was then soft baked on a hot plate at 100°C for 5 minutes resulting in a film thickness of 8.5 μm. A cleanroom wiper was matted on the hot plate to prevent the resist on the

backside from sticking on the hot plate. The 100 μm circle opening on the backside was patterned by OAI Model 808 high-resolution mask aligner using an exposure time of 100 seconds with backside alignment technique. The wafer was then developed by AZ 300 MIF developer for 5 minutes followed by water rinse and followed with a post-development oven bake at 120 °C for 30 minutes. A Surface Technology Systems Advanced Silicon Etch (STS-ASE) tool implemented with Bosch process was used for the backside silicon bulk etching (Bosch 1996). Before the wafer was put into the chamber, a blue tape was attached on the device layer to reduce the helium cooling flow leakage from the bottom and further protect the surface as well during the etching. The JLEFAST recipe was applied. One cycle of the recipe included a etch phase which is 600 watts coil power, 12 watts platen power, 20 mTorr, 136 sccm of SF_6 for 14.8 seconds followed by a passivation phase of 600 watts coil power, 2 watts platen power, 14 mTorr and 90 sccm of C_4F_8 for 7.0 seconds. During the passivation phase, a PTFE layer was deposited on the exposed surfaces. When it turned into the etch step, the PTFE deposited on the bottom of the surface was removed instantly by the ion bombardment and the etch window was then etched one step down. The PTFE on the sidewalls was kept intact and protected the sidewalls from being expanded so that it generated good anisotropy deep silicon etching profile. The etch rate depended on the feature size and etch depth. It was about 1.1 μm/min on the 100 μm feature size and it slowed down as the etching proceeded since it became harder for the etchant species going into deep silicon hole. It also varied under different tool maintenance conditions and between different places on the wafer. The BOX layer worked as the etch stop layer and the deep silicon etch recipe provided a good etch selectivity of silicon to the BOX layer which was about 100 to 1. Short over-etching time had to be set because thinning down the BOX layer decreased the capacitor of the device which increased the electrical measurement noise. In addition, the BOX layer provided a mechanical support for the silicon nanopores membrane. On the other hand, all the silicon in the etch window was made sure to be removed for the through-via device. The strategy was an etch run with an underestimated etch time was first proceeded, followed by small increments with a etch depth measurement using the ZeGage™ optical profiler. Then a 380 cycles run was proceeded first, and 393 μm silicon was etched away which gave an etch rate of

1.034 μm/min. Second run was set at 57 cycles and the total etch depth reached 441 μm/min on both center and side of the wafer which gave an etch rate of 0.842 μm/min. 18 cycles was set for etching the last 9μm silicon and it found out the silicon was completely etched with a 5 minutes overetch time (Fig. 2.1F). Upon the completion of the backside etch, the wafer was immersed into acetone to remove the blue tape, followed by cleaned in heated AZ400T for 5 minutes at 120°C to remove the photoresist. The piranha solution, H_2SO_4 and H_2O_2 at 1:1 ratio was used to remove all the organic contamination including the PTFE layer deposited on the sidewalls of the backside pore. Once the nanopores membrane was formed, the wafer had to be handled with extra caution. No nitrogen gun blow could be used to dry the wafer since it would break the 1.5 μm thick and 100 μm wide silicon device + BOX membrane. All the drying process was done by IPA rinse followed by 80°C oven bake for 5 minutes afterwards.

The through-via window in the BOX layer was opened up by BOE 20:1 etch entering from the nanopores window at the device layer. Before that, the backside of the wafer was protected by spin coating a layer of AZ 4620 positive photoresist at 2500 RPM and oven baked at 120°C for 5 minutes. The wafer was then thrown into the BOE 20:1 solution. The isotropic etchant generated a hemispherical etching profile starting from the Si/SiO_2 interface and punched through the BOX layer after around 37 minutes with a etch rate of 27 nm/min. Since the backside pores were all filled with photoresist, the etchant started to laterally expand the BOX opening. Dr. Petrossian controlled the total etch time within 60 minutes and a 2μm diameter inverted trapezoidal cavity in the BOX layer was generated (Fig. 2.1G). Rest of the BOX layer still provided enough mechanical support to the silicon nanopores membrane. Upon completion of the etching, the wafer was thoroughly rinsed with DI water for 15 minutes to completely remove all the residual BOE in the cavity. The wafer was then cleaned in heated AZ400T for 5 minutes at 120°C, followed by the piranha solution, H_2SO_4 and H_2O_2 at 1:1 ratio. At last, a uniform 44 nm electrical isolation SiO_2 layer was thermal grown in dry atmosphere at 1000°C for 60 minutes and the nanopores size was shrunk to 60 nm from 100 nm and to 110 nm from 150 nm (Fig. 2.1H & Fig. 2.2).

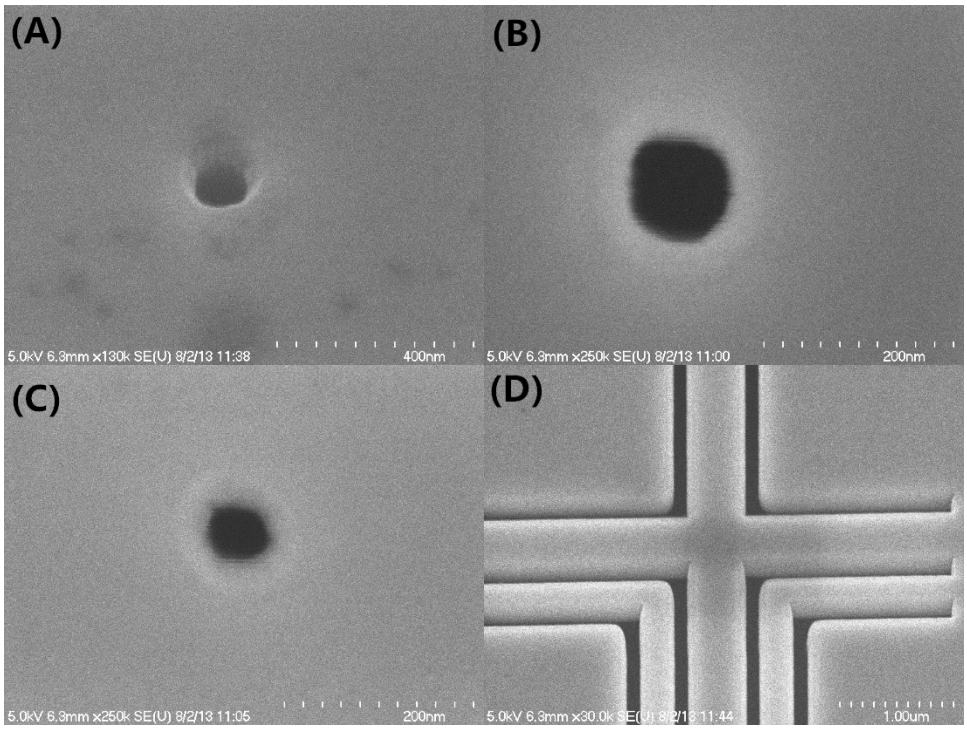


Figure 2. 2: SEM pictures of SOI cylindrical nanopore. (A) Top view of a diameter 110 nm nanopore with a tilted angle. (B) Top view of a 110 nm diameter nanopore. (C) Top view of a 60 nm diameter nanopore. (D) A picture of alignment marker showing the etch sidewalls profile of the silicon device layer.

Upon completion of the final thermal oxidation step, the wafer needed to be diced into pieces of single die. AZ 4620 photoresist was spin coated at 2500 RPM and oven baked at 120°C for 5 minutes on both front side and back side of the wafer consequently to protect the membrane from breaking and being contaminated. The wafer was manually scribed by using diamond pen and was also manually broken into dies. Each die was then cleaned in heated AZ400T for 5 minutes at 120°C, followed by the piranha solution, H_2SO_4 and H_2O_2 at 1:1 ratio. After the cleaning step, one edge of the die was immersed into BOE 20:1 for a length of 2 mm for 2.5 minutes to open a silicon layer window for the electrical contact (Fig. 2.1l). The die was rinsed in the DI water and stored in DI water and IPA at 1:1 ratio in a 50 ml Falcon Polypropylene conical tube.

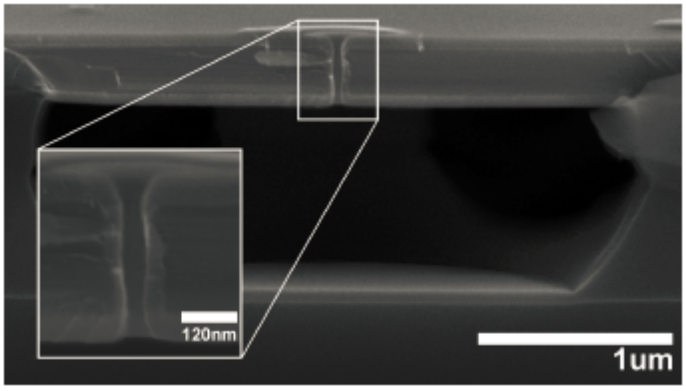


Figure 2. 3: A SEM picture of cross section of a 40 nm cylindrical nanopore with 2 μm diameter BOX layer cavity. Adapted from (Petrossian, Wilk et al. 2007a, Petrossian 2008)

Dr. Petrossian established and developed this standard cleanroom high throughput fabrication process for the nanopore which could be identical reproduced with high quality cylindrical nanopore profile every time. But this pore met an aqueous filling issue due to the special cylindrical geometry compared to other solid state pore even with hydrophilic SiO_2 surface. The problem was found out that air bubbles easily got trapped in the inverted trapezoidal cavity in the BOX layer and stuck hardly by the shorter base at SiO_2/Si bulk interface of the inverted trapezoid as shown in the Figure 2.3. An alternative way for the BOE layer etch was considered in order to avoid the inverted trapezoidal geometry. It came out that the BOX layer could be first dry etched from the device layer nanopore window all the way to the SiO_2/Si bulk interface before the BOE etch so that the BOE etch would only do a lateral expansion to get a rectangle cavity profile instead a trapezoidal one. But the original thermal SiO_2 hard mask could only withstand an etch of the first Si layer. A good hard mask with high selectivity to both Si and SiO_2 was needed for etching the device layer and BOX layer.

2.2 Nanopores Patterning Using Al_2O_3 Hard Masks on SOI Substrates

Aluminum oxide thin films, deposited using Atomic Layer Deposition (ALD), are a promising semiconductor dry etching hard mask layer that can be used when patterning high aspect ratio nanostructures.(Chekurov, Koskenvuori et al. 2007, Henry, Walavalker et al. 2009)

Al_2O_3 films provide exceptional selectivity over silicon (10000:1) and an extremely high aspect ratio in an etch profile using ICP-RIE.(Dekker, Kolari et al. 2006) Deposited using ALD ensures the layer to be dense and pin-hole free. The high density of aluminum oxide, however, comes at the cost of the layer being difficult to pattern initially. While some groups report success in patterning the aluminum oxide layer using lift-off techniques, a process involving dry etching of the hard mask layer would be preferable in terms of process reproducibility.(Henry, Walavalker et al. 2009)

In this section, the development of an Aluminum Oxide dry etch hard mask process to pattern nanopores in silicon-on-insulator substrates for nanofluidic applications was studied. Based on previous studies on the alumina etch conditions using both chlorine and fluorine related gases,(Il Kim 2010, Kang, Kim et al. 2008, Min, Kang et al. 2013, Xue-Yang, Kim et al. 2009, Yang, Woo et al. 2010) we investigated the etching properties of sub-100 nm patterns in alumina using electron-beam-sensitive polymethylmethacrylate (PMMA) resist, comparing different gas chemistries to achieve good selectivity of alumina over PMMA. Using an optimized patterning process, the alumina layer was used to transfer the initial pattern into the underlying silicon device and buried silicon dioxide layer. An anisotropic sidewalls profile of the buried silicon dioxide layer is preferred, since it prevents air bubble trapping in the nanofluidic device. While pattern transfer into the silicon device layer benefits from the excellent dry etching selectivity of the alumina layer, deep trench etching into the buried oxide using the alumina hard mask is still limited by the etch selectivity using an RIE process.

2.2.1 Process Flow of SOI Nanopores Fabrication Using Al_2O_3 Hard Mark

The fabrication of the cylindrical nanopore structure started with the deposition of an ALD Al_2O_3 hard mask layer upon the device layer of a double side polished SOI wafer with a 340 nm silicon device layer and 1 μm BOX layer using a Cambridge NanoTech Savannah ALD System. The deposition chamber was alternately filled using water vapor and Trimethylaluminum (TMA) gas precursor pulses (George 2010) and a uniform Al_2O_3 layer with the thickness of 53 nm was obtained at a stable rate of 0.8 Å/cycle at 180 °C chamber temperature. 6% PMMA in

methoxybenzene was then spin coated at 3000 r/min and followed by a 15 minute hard bake at 170°C to obtain a thickness of 250 nm for electron beam lithography (EBL) (Fig.2.4A).

Nanopores in the PMMA layer were patterned in a JEOL JBX-6000FS/E EBL system with an area dose of 800 $\mu C*cm^{-2}$. The patterns were developed in a mixture of 11 parts of 25% methyl isobutyl ketone(MIBK) in isopropanol, ten parts of 30% 2-ethoxyethanol (CS) in methanol and 1 part of 26.5% methyl ethyl ketone (MEK) diluted in ethanol for 20 seconds in the room temperature and rinsed in IPA and dried with nitrogen gas. A one minute hard bake at 100°C on a hot plate was utilized right after the development to enhance the PMMA etching resistance and straighten the developed nanopore sidewalls in the PMMA layer. The Al_2O_3 hard mask layer was etched using ICP-RIE at 300 W coil power and 30 W platen power using 20 sccm BCl_3 at 10 mTorr chamber pressure in an Advanced General Etch tool from Surface Technology Systems (Fig.2.4B). Etch rates of 5.6 nm/min on alumina and 23 nm/min on PMMA ensured that the alumina was anisotropically etched all the way to the Si device interface before the PMMA layer was totally removed. The remaining PMMA was cleaned in a 200W Oxygen plasma.

The patterns were then transferred to the 340 nm silicon device layer vertically using the ICP-RIE described previously at 500 W coil power, 50 W platen power, 6 mTorr chamber pressure using 10 sccm Cl_2 gas flow (Fig.2.4C). A 20:1 selectivity of silicon to alumina was achieved with etch rates of 11 nm/min on alumina and 220 nm/min on silicon. A slight over etching with a total etch time of 2 mins 20 secs was applied to drill the nanopore to the 1000 nm BOX layer. 25 nm of the alumina hard mask was consumed and a hard mask layer of 28 nm thickness was left for the 1000 nm BOX etching. The BOX layer etch was attempted using CHF_3: Ar 25 sccm: 25 sccm, 25 W forward power, 4 mTorr pressure in an Oxford Instruments Plasmalab 80+ RIE tool. A selectivity of 40:1 was observed with etch rates of 10 nm/min on the silicon dioxide and 0.25 nm/min on the alumina layer respectively (Fig.2.4D).

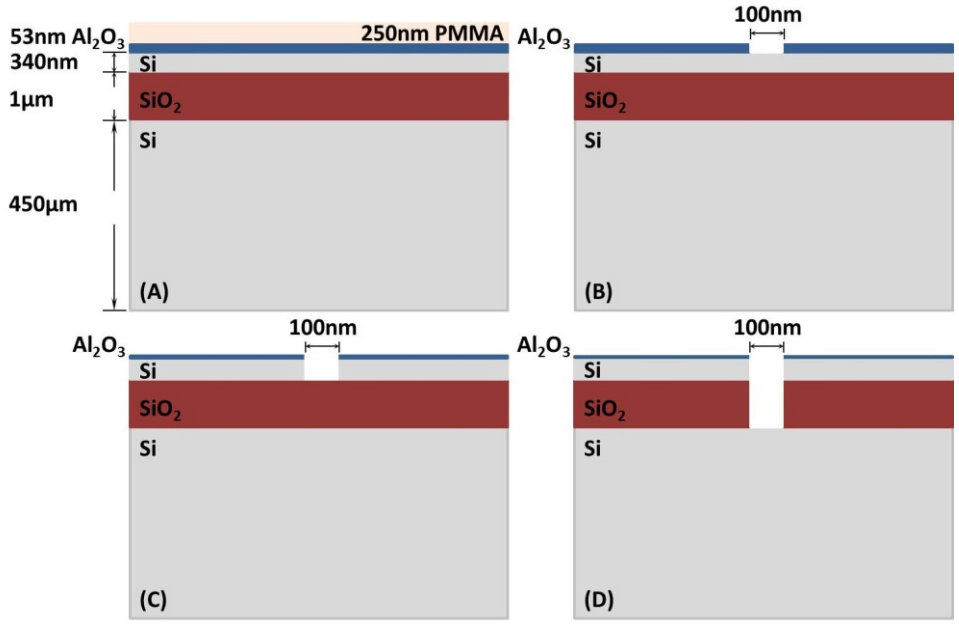


Figure 2. 4: Cross-sectional rendering of SOI nanopore etching using alumina hard mask. (A) The SOI wafer is covered with a 53 nm ALD alumina thin film on the front side, followed by spin-coating of 250 nm PMMA. (B) The PMMA is patterned using EBL to open 50, 100 & 150 nm diameter apertures and the patterns are transferred to the alumina hard mask using ICP-RIE with BCl_3 chemistry. (C) The silicon device layer is etched using Cl_2 gas in an ICP-RIE tool. (D) The BOX layer is etched using CHF_3: Ar gas mixture in a Plasmalab 80+ RIE tool.

During the process of the nanopore pattern being transferred into the alumina hard mask layer and nanopore etching in silicon and silicon dioxide layer, the etch selectivities of alumina over PMMA, silicon and silicon dioxide and the degree of anisotropy of each step are the key points of investigation. Different etch chemistries and etch conditions, such as tools, pressureand power were studied to achieve the desired nanopore profile.

2.2.2 Transfer of Nanopores Pattern into the ALD Al_2O_3 Layer

Figure 2.5 shows the etch rates of alumina and the selectivity to PMMA using Cl_2, Ar, Ar/BCl_3 mixtures and BCl_3 gas chemistries at 10 mTorr chamber pressure and 200 W forward power in an Oxford Instruments Plasmalab 80+ RIE tool. Total gas flow was controlled at 40

sccm for each run except for Cl_2 being set at 10 sccm due to chlorine gas pipeline limitation. Pure BCl_3 gas chemistry did yield the best selectivity over PMMA (0.19:1) and the highest etch rate of 2.9 nm/min on Al_2O_3, based on the following reaction,

$$Al_2O_3 + 3BCl_3 \rightarrow 2AlCl_3 + (BOCl)_3$$

The BCl_3 plasma reduced the oxide and formed a stable volatile compound tricholoro-boroxine $(BOCl)_3$ which provided a higher etch rate compared to a Cl_2 plasma.(Shamiryan, Baklanov et al. 2009) The PMMA resist also showed good resistance (15 nm/min) to the BCl_3 gas chemistry. The etch rate of Cl_2 plasma on an alumina film was slightly lower than that of BCl_3 plasma. However, it rapidly consumed the PMMA at a rate of 105 nm/min, resulting in a worse selectivity compared to that of the BCl_3 plasma etch. Pure Ar sputtering was found to sputter away the PMMA film at a rate of 50 nm/min without etching the alumina film (<0.1 nm/min). Ar-rich Ar / BCl_3 gas mixtures gave results similar to pure Ar sputtering. This shows that the alumina film is a dense and strong bonded film and that the Al-O bonds cannot be broken by pure ionic sputtering without providing enough chemical reactants.

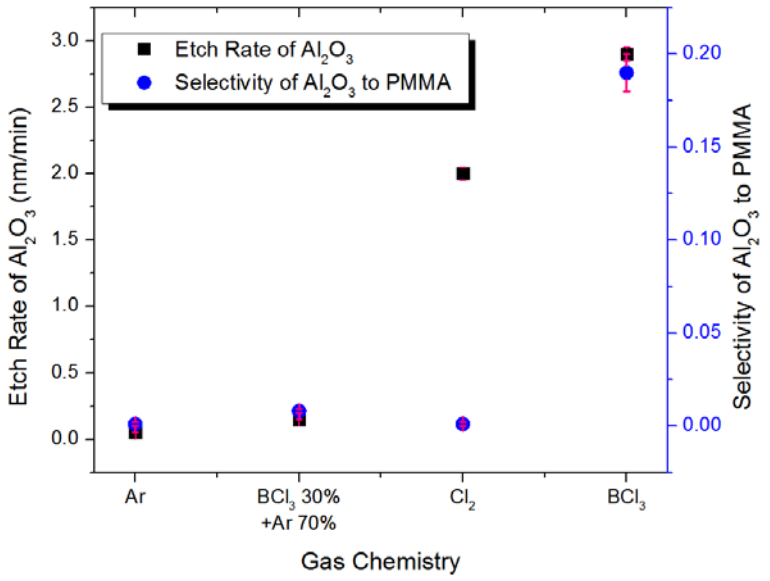


Figure 2. 5: Etch rates of alumina and selectivity of alumina to PMMA using Cl_2, Ar, Ar/BCl_3 mixtures and BCl_3 gas chemistries in an RIE tool using 200 W forward power.

A low pressure of 10 mTorr was set since the etch rate of alumina decreases sharply beyond 15 mTorr due to deposition of etch byproducts on the surface.(Yang, Woo et al. 2010) At a high process pressure when the mean free path is short, highly concentrated radicals of BCl_2^+ and BCl_3^+ make the non-directional chemical etching dominant and the etch byproducts are deposited on the surface, preventing the occurrence of ion milling. However, at extremely low process pressure (<5 mTorr) with a long mean free path, ion milling dominates the etching process so that selectivity over PMMA is lost. The chemical reaction with the support of BCl_2^+ and BCl_3^+ plasma ion sputtering on Al-O bonds and deposited Al-Cl and BCl-O compound byproducts at a proper etch pressure optimizes the etch rate, anisotropy and selectivity over the resist.

BCl_3 gas at a process pressure of 10 mTorr was found to provide the best conditions for the anisotropic alumina layer etching with an optimal selectivity over PMMA. However, after regular RIE etching, geared PMMA sidewalls appeared and the roughness of the pattern profile reached 1-2 μm (Fig. 2.6A). Resist burn and reflow occurred during etching which were caused by high temperature at the surface and bombardment with non-ionized radicals. Moving to an ICP-RIE system solved this problem. The Helium gas cooling on the wafer backside in the system prevented the resist burn by keeping the wafer at room temperature. The vertical and clean sidewalls of an etched alumina reference pattern obtained using the optimized etch conditions are shown in Figure 2.6B. The platen bias in the ICP tool brings more BCl_2^+ and BCl_3^+ ions vertically to the alumina surface, thereby enhancing anisotropy, etch rate and selectivity. The 150 nm and 100 nm nanopore patterns were transferred to the alumina hard mask layer (Fig. 2.6C) from an e-beam-exposed PMMA layer (Fig. 2.6D) without horizontal expansion. The patterns on the alumina hard mask appeared because of the deterioration of the PMMA resist at the end of the alumina etching step using BCl_3. This caused the alumina mask to be etched in certain areas, leading to what appears to be cracks. However, these features in the alumina layer are shallow enough so that they did not cause any pinhole to form. Thus, the subsequent Silicon and BOX layer etching was not affected. The results of sub-100 nm nanopore patterns in the 53 nm Al_2O_3

layer demonstrate the usefulness of an alumina hard mask in the fabrication of nano-MEMs devices.

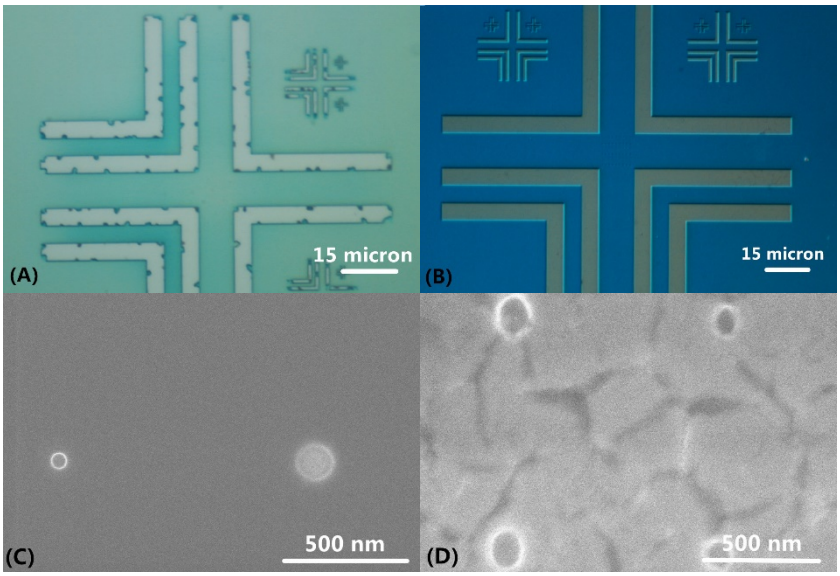


Figure 2. 6: (A) Optical microscopic image of PMMA resist burn after alumina etching using BCl_3 in an Oxford RIE system with 200 W forward power, 40 sccm BCl_3 and 10 mTorr chamber pressure. (B) Optical microscopic picture of alumina alignment pattern with remaining PMMA on the top showing straight alumina sidewalls after ICP-RIE using 300 W coil power and 30 W platen power with 20 sccm BCl_3 and 10 mTorr chamber pressure. (C) Scanning Electron Microscope (SEM) picture of 100 nm and 150 nm nanopores in the patterned PMMA layer on the SOI substrate before etching. (D) SEM picture of 100nm and 150nm nanopores transfered to the alumina layer using BCl_3 plasma in the ICP-RIE tool after remaining PMMA is washed away. The patterns on the alumina hard mask due to the deterioration of the PMMA resist at the end of etching step were shallow enough so that they did not affect the subsequent Silicon and BOX layer etching.

2.2.3 Etching of Si Nanopores Using an ALD Al_2O_3 Hard Mask

The high aspect ratio nanopore etching in the silicon device layer was initially tested using a Bosch process in the ICP-RIE tool as it provides good selectivity of alumina over silicon

(100000:1).(Dekker, Kolari et al. 2006) The recipe started with a 14.8 seconds etch cycle at 600 W coil power, 12 W platen power, 20 mTorr, 136 sccm of SF_6, followed by a passivation phase at 600 W coil power, 2 W platen power, 14 mTorr and 90 sccm of C_4F_8 for 7.0 seconds. However, the isotropic chemical reaction between SF_6 and Si enlarged the nanopore size from 150 nm to 500 nm before the first passivation cycle, forming a barrel-shaped aperture instead of a cylindrical one as shown in Figure 2.7A. The alumina hard mask was not enlarged during this etching step as expected. The requirement for preservation of the nanopore sidewall slope and initial patterning diameter prompted a switch to a chlorine gas recipe in ICP-RIE as described in the previous section. The chlorine etch resulted in straight side walls and a cylindrical nanopore profile in the silicon layer as shown in Figure 2.7B. An array of nanopores with diameters ranging from 50 nm to 190 nm and a size increment of 20 nm was etched anisotropically without any expansion at any size. The Chlorine gas etched away the alumina layer at a rate of 11 nm/min, since the Chlorine gas is one of the typical etchants for an alumina layer as reported previously. However, a 20:1 selectivity of silicon over alumina was observed, being more than twice the selectivity compared to the selectivity of silicon over a silicon dioxide mask.(Petrossian, Wilk et al. 2007b, Petrossian, Wilk et al. 2007a) In addition, the remaining 28 nm-thick alumina layer provides sufficient thickness for etching of the buried oxide as discussed in the following paragraph.

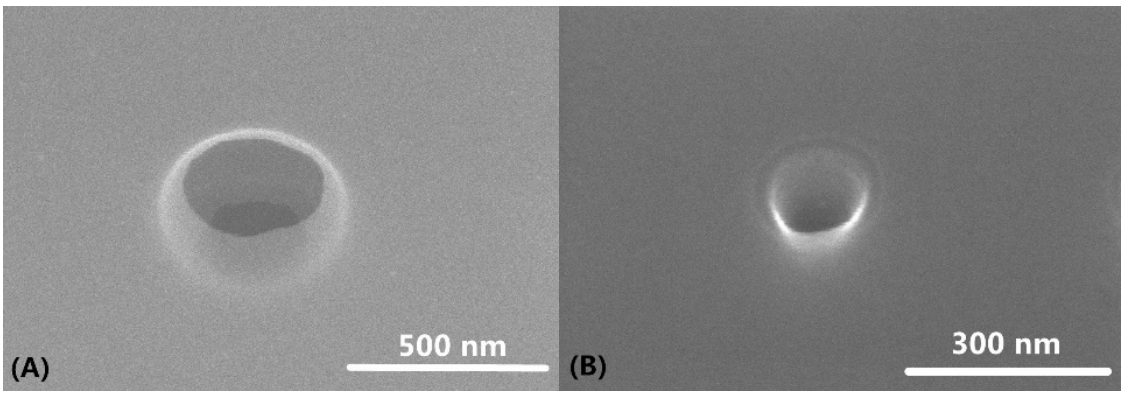


Figure 2. 7: SEM pictures of nanopores etched into the silicon device layer after the alumina mask layer has been removed (A) shows the enlargement of a nanopore to 500 nm diameter

(150 nm pattern diameter) when using the Bosch process which involves SF_6 as the etchant. (B) displays a nanopore that has been etched using 500 W coil power and 50 W platen power with 10 sccm Cl_2 at 6 mTorr chamber pressure in an ICP-RIE tool. The final nanopore geometry exhibits vertical sidewalls and no evidence of lateral enlargement at a pattern diameter of 150 nm.

2.2.4 Etching of Nanopores through the BOX Layer Using an ALD Al_2O_3 Hard Mask

In order to accomplish free fluid flow through the nanofluidic structure, the buried oxide layer below the silicon device layer has to be etched, preserving the nanopores diameter in the silicon device layer on the order of tens of nanometers. While the silicon nanopores membrane can be released using wet chemical etching of the buried oxide (BOX) layer from the top-side(Petrossian, Wilk et al. 2007a), the isotropic wet etching generates an inverted trapezoidal geometry cavity in the local vicinity of the silicon nanopores, which easily traps an air bubble during electrolyte filling. Being able to etch both the silicon device layer and the BOX layer with controlled anisotropy, using a single hard mask layer would significantly improve the fluidic properties of the final device. The aluminum oxide hard mask offers the selectivity over both silicon and silicon dioxide which regular silicon dioxide and silicon nitride hard masks cannot deliver.

Using a CHF_3 – based silicon dioxide etch recipe (50 W forward power, CHF_3: Ar 25 sccm: 25 sccm, 4 Pa pressure) in an Oxford Instruments Plasmalab 80+ RIE tool resulted in a selectivity of 40:1 of SiO_2 over alumina, which enables etching through the BOX layer using a 28nm thick alumina mask. However, undercuts occurred in the silicon device layer after 45mins of etching while the CHF_3: Ar plasma was able to etch the BOX layer anisotropically (Fig. 2.8). The silicon nanopores sandwiched between the alumina and BOX layer was not able to withstand the transverse ion collision, which caused the nanopores size to double and the profile to assume a champagne cup shape, as shown in Figure 2.8. A possible solution to prevent transverse ion collisions to damage the nanopores is to employ a passivation layer on the silicon nanopores sidewalls during etching of the BOX layer. A combination of Octofluorocyclobutane (C_4F_8) and H_2 gas has the potential to accomplish a high aspect ratio nanochannel etch in the BOX layer.(Fukasawa, Kubota et al. 1994) The platen bias in an ICP configuration would be able to

direct the etchant plasma to the bottom surface area to enhance the ratio of chemical reaction so that it causes less roughness on the nanopores sidewalls. Using a passivation mechanism, however, will affect the etch rate inside the nanochannels, which in turn might decrease the etch selectivity that can be accomplished.

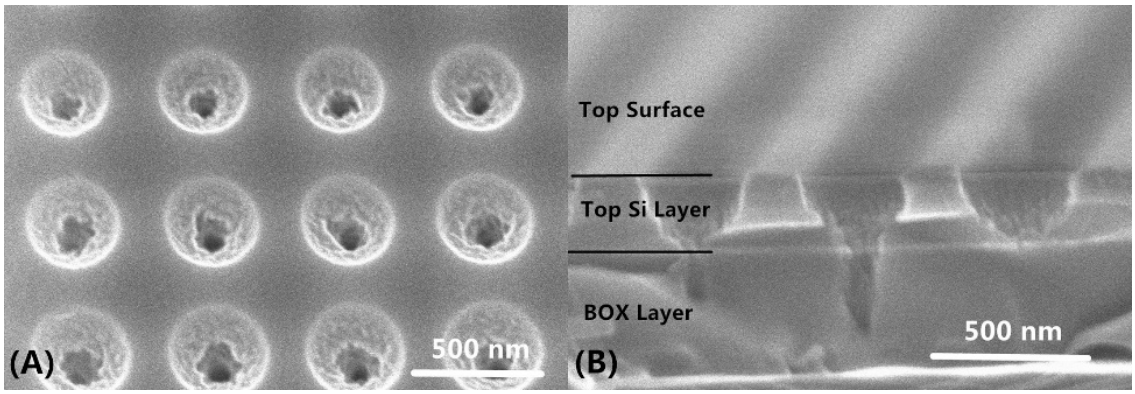


Figure 2. 8: SEM pictures of the SOI wafer after a BOX layer etch using 50W forward power, CHF_3: Ar 25 sccm: 25 sccm at 30 mTorr chamber pressure after the alumina layer has been removed. (A) Top view of nanopores array. (B) Cross sectional view of nanopores array showing the champagne cup shape of the nanopores in the silicon layer.

2.3 Process Adjustment and Surface Charge Modification Using ALD Al_2O_3 Deposition

Leo's nanopores processes were suffering from aqueous solution filling issue due to the air bubble trap in the 2 μm diameter inverted trapezoidal cavity in the BOX layer. The size of the cavity was controlled since the expansion of the area decreased the mechanical support for the upper 340 nm thick silicon suspended membrane which might be easily broken. In a new batch of nanopore fabrication, a 120 minutes BOE 20:1 etching time for the BOX was tried and the void diameter increased to 7.9 μm from 2 μm as shown in Figure 2.9. Surprisingly, the device membrane was still robust and it became much easier to be fill with aqueous solutions.

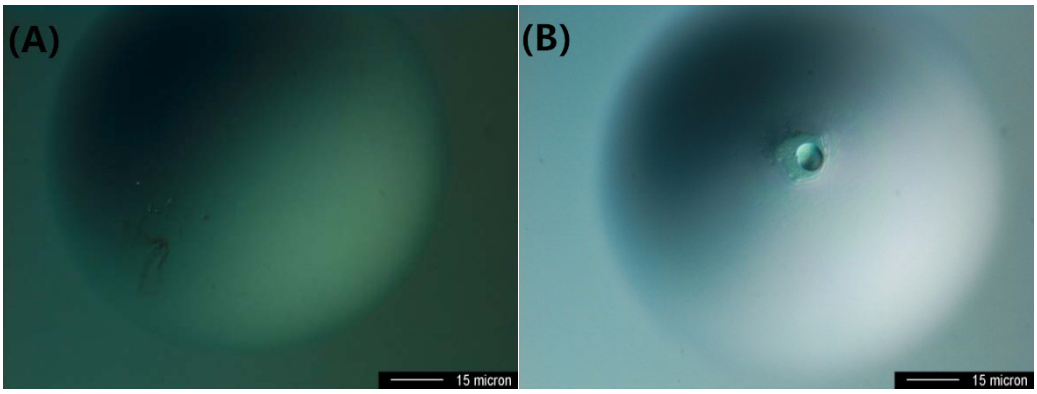


Figure 2. 9: Optical top view of the nanopore device membrane. (A) Before BOE. (B) After BOE.

The nanopores device was also deposited with a uniform 10 nm ALD alumina layer using Cambridge NanoTech Savannah ALD System and the pore was shrunk to 40 nm from 60 nm (Fig 2.10). The silicon contact area was avoided to be deposited by covered with Kapton tape during the deposition. The positively surface charged alumina nanopores provides another choice for the ionic current measurement using gate bias modulation in comparison to the negatively charged SiO_2 surface which will be introduced in next Chapter.

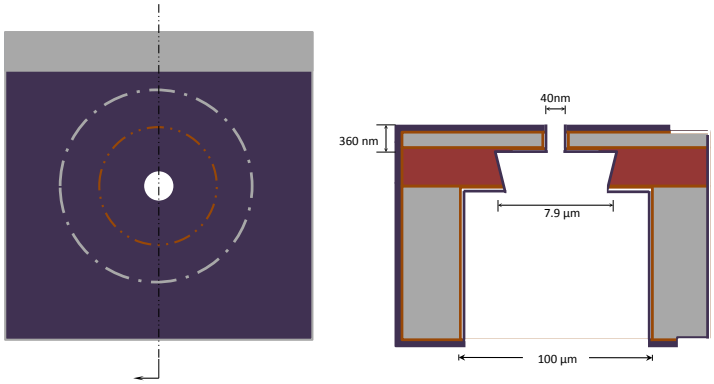


Figure 2. 10: Illustration of nanopore with depositing a 10 nm ALD alumina layer.

2.4 Summary

The SOI nanopores process flow is compatible with standard cleanroom facilities for a high throughput fabrication. The buried oxide layer provides a robust etch stop for the nanopore membrane and the sub-100 nm aperture size is precisely controlled by electron beam lithography and thermal oxidation. The surrounding thermal SiO_2 coating not only works as a good electrical insulation layer, but also provides native negative surface charges. As a comparison for ionic transport experiments, the device was deposited with an ALD Al_2O_3 layer whose surface is positively charged in neutral and acid solutions.

To avoid trapping air bubble in the cavity in the local vicinity of the silicon nanopores during electrolyte filling, nanopores patterning using Al_2O_3 hard mask is studied. The excellent selectivity of Al_2O_3 over both Si and SiO_2 in both RIE and ICP RIE processes enabled fabrication of vertical nanofluidic channels through both the Si device and buried oxide (BOX) layer. BCl_3 plasma has proven to be the optimal gas chemistry for patterning sub-100 nm nanopores in the hard mask layer, since it showed the highest etch rate on Al_2O_3, the highest selectivity of Al_2O_3 over PMMA compared to Cl_2, Ar, Ar/BCl_3 mixtures and anisotropic pattern transfer. The capability of using plasma etching to transfer nano-structures in PMMA directly into the Al_2O_3 hard mask enabled compatibility with existing mask designs, avoiding the need for image reversal compared to a lift-off process for patterning the hard mask layer. Using the Al_2O_3 hard mask, nanopores exhibiting smooth vertical sidewalls were etched in the silicon device layer using a Cl_2 plasma in an ICP-RIE tool. While this plasma chemistry resulted in a reduced selectivity over SF_6-based plasma, the resulting sidewall profile showed excellent anisotropy. Alternatively, the hard mask can be used with an SF_6-O_2 mixture to accomplish a vertical sidewall profile in silicon. In addition, the Al_2O_3 hard mask process with its excellent selectivity enables other plasma etch chemistries for silicon and silicon oxide to be studied for nano-MEMS processing, some of which were previously precluded due to fast deterioration of a hard mask like SiO_2. In particular, it enables silicon dioxide etching using H_2 + Fluorine-based plasma chemistry, which will be pursued as a next step. However, care has to be taken to maintain the anisotropic sidewall profile of the silicon layer, which is easily etched due to sputtering effects.

3. IONIC TRANSPORT IN SOI SINGLE NANOPORE WITH FIELD EFFECT MODULATION

3.1 Introduction to Electrical Double Layer

The electrical double layer (EDL) is a charge screening phenomenon at the solid-liquid interface which exists very commonly in our daily life. When it comes to nanofludics, it draws more interests from researches due to the high surface-to-volume ratio and comparable size to the dimension of the nanofludics. It is caused by the existing of surface charges at the solid surface due to the dissociation of the surface groups and the adsorption of ions in the electrolyte to the surface (PERRAM, HUNTER et al. 1973). Once the solid surface is immersed in the electrolyte, a group of ions, we call counter-ions, which have the opposite charges to the solid surface, are attracted to the solid surface to neutralize the charges and form an electrostatic shielding layer in the liquid right next to the solid/electrolyte interface. It is first realized by Hermann von Helmholtz. The literally 'double layer' represents the layer of charged solid surface and the counter-ions layer in the ionic solution and they form a simple parallel plate molecular capacitor.

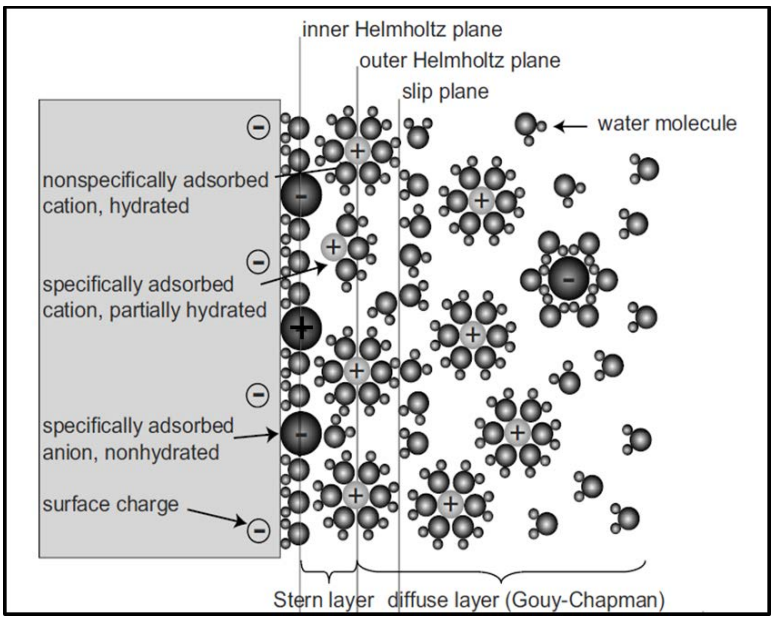


Figure 3. 1: Gouy-Chapman-Stern model of the electric double layer. Adapted from (Schoch, van Lintel et al. 2005).

The model of the EDL is now commonly described as the three layers model which was suggested by Otto Stern and later further developed by David Grahame as shown in Figure 3.1 (Schoch, van Lintel et al. 2005). The original capacitor Helmholtz layer splits into Inner Helmholtz Layer (IHL) and Outer Helmholtz Layer (OHL). The inner Helmholtz Layer consists of a group of water molecules and non-hydrated co-ions and counter-ions adsorbed and immobilized on the solid surface due to a specific chemical adsorption potential. This potential is related to the geometrical restrictions of ions, water molecules size and the short range interactions between ions, the surface walls and the water molecules. The center of non-hydrated plane is Inner Helmholtz Plane (IHP) The next layer, Outer Helmholtz Layer, contains a layer of bound, hydrated, and partially hydrated counter-ions by the coulomb force and they are centered at Outer Helmholtz Layer (OHL). The spatial region which combines both IHL and OHL is also called Stern layer. However, the solid surface charge has not been totally screened by the counter-ions in both Helmholtz plane. A diffuse layer which consists of mostly mobile counter-ions and a little bit co-ions situates next to the stern layer to comprehensive neutralize the surface charge. The balance between attractive electrostatic force from the surface charges and the random thermal motion upon the ions makes most of the counter-ions move within this layer. The layer starts from slip plane, or shear plane, which is an imaginary plane distinguishes the immobilized ions adsorbed on the solid surface from the mobile counter-ions and it is regarded as an extension or junction layer between Helmholtz plane and bulk electrolyte(Hunter 1981).

3.2 Introduction to Zeta Potential, Debye Length and Nanopores Conductance Plateau

3.2.1 Zeta Potential and Debye Length

Due to the accumulation of counter-ions at the solid-liquid interface, the potential at the interface departs from the bulk behavior which is shown in Figure 3.2. The surface is assumed as negatively charged oxide surface, and anions and cations in the electrolyte are considered as co-ions and counter-ions, respectively. In the inner region, where is from the surface to the Shear plane, the potential shows a linear relationship with the normal distance to the plane since the charges adsorbed to the surface are spatially fixed. The net negatively charged non-hydrated

ions in the Inner Helmholtz Layer increases the potential from ϕ_s at surface to ϕ_i at IHP, and then, the potential linearly decreases across the hydrated counter-ions layer in the Outer Helmholtz Layer. In most of the case, the two potentials are considered as the same since the difference is not caused by the electrostatic force form the surface charges. The value of the surface potential measured at this shear plane is called the zeta potential ζ. Beyond the shear plane, the distribution enters a diffusion decay region which follows the Poisson-Boltzmann equation. In other words, the zeta potential ζ is the potential the closest region to the solid surface where the motion of ions is still hydrodynamic (Hunter 1981).

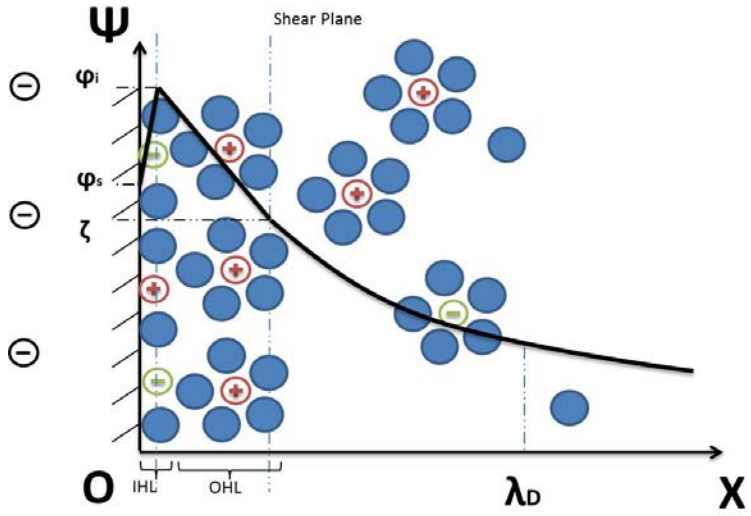


Figure 3. 2: Schematic representation of a possible potential distribution at a negatively charged oxide surface with normal distance to the surface.

In the diffusion region, the potential follows the fundamental Poisson-Boltzmann equation:

$$\nabla^2\Psi = \frac{d^2\Psi}{dx^2} = -\frac{e}{\varepsilon_0\epsilon_r}\sum_i n_i^0 z_i \exp[-z_i e\Psi(x)/k_B T] \quad (3.1)$$

where Ψ is the electric potential due to the surface charge, $\nabla^2\Psi$=div(gradΨ), x is the normal distance to the surface, e is the elementary charge, ε_0 is the Vacuum permittivity, ϵ_r is the relative

permittivity of the electrolyte, n_i^0 is the i ion concentration at Ψ=0, z_i is the valency of ion i, k_B is the Boltzmann constant and T is the temperature.

Debye-Hückel approximation assumes the surface potential is small everywhere in the EDL which gives ($e^{-y} = 1 - y \; for \; small \; y$) (Hunter 1981, Schoch, Han et al. 2008)

And then

$$\nabla^2\Psi = \frac{d^2\Psi}{dx^2} = -\frac{e}{\varepsilon_0\epsilon_r}[\sum_i n_i^0 z_i - \sum_i n_i^0 z_i^2 e\Psi(x)/k_B T] \tag{3.2}$$

The first term in the square bracket must be zero to keep the electro-neutrality in the bulk electrolyte

$$\nabla^2\Psi = \frac{d^2\Psi}{dx^2} = \kappa^2\Psi \tag{3.3}$$

where

$$\kappa = (\frac{e^2\sum_i n_i^0 z_i^2}{\varepsilon_0\epsilon_r k_B T})^{1/2} \tag{3.4}$$

κ is called the Debye-Hückel parameter.

The potential decays exponentially in this diffusion region with the characteristic length Debye length

$$\lambda_D = \kappa^{-1} = (\frac{\varepsilon_0\epsilon_r k_B T}{e^2\sum_i n_i^0 z_i^2})^{1/2} \tag{3.5}$$

which denotes the position of the 1/e decay of the zeta potential and it decays to about 2% of the shear plane value with a length of 3 λ_D to the surface.

The Debye-Hückel works only in the lower surface potentials. The Gouy-Chapman model numerically solves the Poission-Boltzmann equation for unsymmetrical electrolytes and high surface potentials which results in more accumulation of counter-ions and the reduction of co-ions at near surface region.

The Debye length is an important characteristic length which stands for size of area where counter-ions accumulates, and it is only related to the electrolyte type, electrolyte concentration and temperature. The lower the concentration, the longer the Debye length. For instance, the Debye length increase from 0.306 nm for 1 M KCl to 96.717 nm for 10 μM KCl and 305.845 nm for 1 μM KCl at 25℃ by the calculation of (Petrossian 2007). Therefore, when it

comes to the nanopores, the ion distribution within the nanopore can be figured out according to the Debye length under different molarities of the electrolyte. Figure 3.3 gives an example of ion distribution surrounding the silicon oxide nanopore under 10 mM and 10μM KCl, respectively. Silicon dioxide is negatively charged so that the K^+ ions are the counter-ions which accumulate at the surface (Behrens, Grier 2001). Under high molarity electrolyte, the Debye length is quite short compared to the aperture size the counter-ions and co-ions are still evenly distributed within the aperture expect for a layer of counter-ions adsorbed on the surface which is much less than the number of ions in the bulk solution inside the pore. However, in the low molarity KCl case, a larger area of the K^+ ions needed to be accumulated to provide the same amount of counter-ions to neutralize the fixed surface charges and causes a much longer Debye length. Within this area, most of the Cl^- ions are depleted and K^+ ions become the majority ion in the nanopore which contributes to the pore conductance if the pore size is comparable to the Debye length.

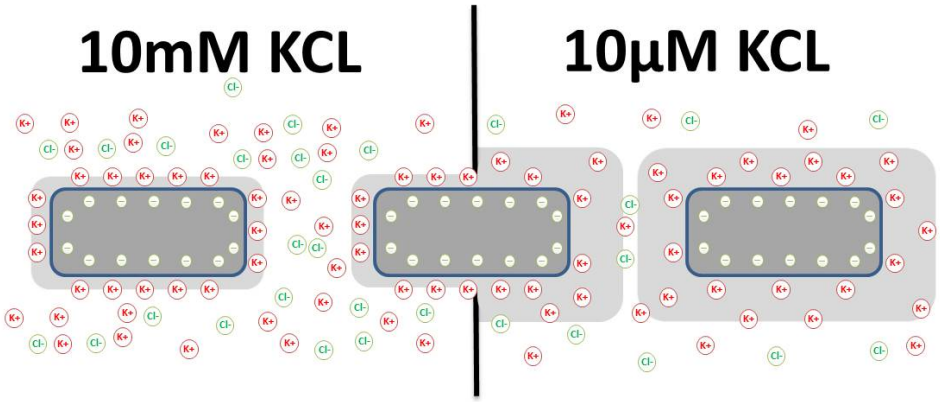


Figure 3. 3: Ion distribution surrounding negatively charged silicon dioxide nanopores in different molarity KCl ionic solution. Left: 10 mM KCl. Right: 10 μM KCl. The gray area shows the Debye length.

3.2.2 Nanopore Conductance Plateau

In the low molarity electrolyte, when the nanopore reaches sub-100 nm size, the double layers from each side of the aperture walls overlap inside the nanopore and generate a counter-

ion enriched ion distribution profile in the aperture. This profile changes the regular rule of ion conduction of the aperture which is called conductance plateau of nanopores (Pu, Yun et al. 2004).

For a regular cylindrical ion channel, the ionic current has the expression, (Zhang, Hassanali et al. 2011)

$$I_{cond} = (KA + K^{\sigma}p)E. \quad (3.6)$$

where E is the tangential electric field parallel to the channel walls, K is the bulk conductivity, K^{σ} is the surface conductivity, A is the round pore channel cross sectional area and p is the cross sectional perimeter. The ionic current has a bulk convective component which is proportional to which is proportional to the ion mobility μ and electrolyte concentration n. The first component is dominant in large pore and high concentration electrolyte. For the sub-100 nm pores with low concentration electrolyte solutions, an excess of counter-ions go inside the pore to neutralize the surface charge and contribute to the total ionic current (Schoch, Renaud 2005). The second term dominates under this condition and the ionic current does not change with the concentration of the solutions. It is most related to the counter-ions mobility and surface charge densities which varies from pH of the solution, temperature, the composition and concentration of the electrolyte solution and the nature of the surface material (Kirby, Hasselbrink 2004, de Lint, Benes et al. 2003). And it shows a current plateau on the plot of ionic current with the electrolyte solution concentration (Stein, Kruithof et al. 2004, Schoch, van Lintel et al. 2005, Joshi 2011).

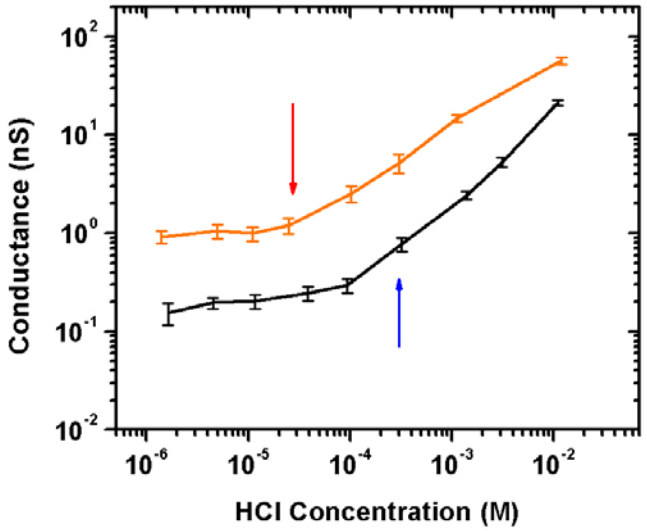


Figure 3. 4: Silicon dioxide nanopores array conductance as a function of HCl concentration ranging from 3 μM to 100 mM for 34 nm pore diameter array (black) and 95nm pore diameter array (orange). The nanopores length is 340 nm. Figures were adapted from (Joshi 2011).

Figure 3.4 gives an example of the conductance log-log plot with the function of HCl concentration of two sizes of silicon dioxide nanopore array measured by Dr. Punarvasu Joshi. It shows the linear drop at high molarity concentration and starts to deviate from the bulk conductivity when the Debye layers overlap in the nanochannel which is $8*10^{-4}$ M for the 34 nm pore and 10^{-4} M for the 95 nm pore. H^{+} ions are the counter-ions in this case and contribute most of the ionic current by accumulating near in the stern layer and diffusion layer. The current plateau shows that a constant number of H^{+} ions are kept in the nanochannel under low concentration electrolyte.

Not all the hydrogen ions inside the nano-aperture can contribute to the ionic current since most of the ions are in the stern layer and they are immobile as introduced in the previous section. However, the question whether the ions in the stern layer, no matter hydrated or non-hydrated, can provide any current is still under debate (Lyklema, Minor 1998, Zhang, Hassanali et al. 2011, Netz 2003, Lyklema 2014). Dr. Zhang used the continuum hydrodynamics and molecular dynamics simulation and showed that the ions are not mobile at where water is

stagnant, which means they are not dynamic at all in the Stern layer. On the other side, Dr. Lyklema and some other researchers (Lyklema, Minor 1998, Dukhin 1996) insisted that some of the ions move in the stern layer which caused a dynamic stern layer. How they moved and how many ions moved still need to be solved. They may move inside the layer, or they may hop to the diffuse layer and then return. What we know for sure is that most of the ions are stagnant to the surface due to the chemical potential, electrostatic force, viscosity near the walls and surface roughness. However, the stern layer accumulates up to 85% of the counter-ions. Only a few of them moves in this layer would cause a significant influence in the surface conductance.

3.3 Electrical Characterization Setups

This section briefly describes the procedure of the single nanopore conductance measurement with field effect modulation, including nanopore device mounting, ionic solution preparation, amplifier setup and leakage current subtraction. The same setup was written in Dr. Joshi's thesis in detail (Joshi 2011). This section will not totally repeat Dr. Joshi's steps but adds additional steps based on author's experiments and some considerations of leakage current issue with the voltage bias.

3.3.1 Nanopore Chip Mounting

The nanopore chip was vertically sandwiched between two custom made Teflon chambers filled with electrolyte solution using threaded metal rods with screws. The pore got the access to the chamber through the 1.5 mm diameter drilled hole on the holder and was sealed by the Silicone O-rings on each side of the chip. Figure 3.5A shows the O-ring glued on holder by water resistant silicone adhesive and the inset picture is the side view. The top right picture compares two O-rings with different sizes, the small thick red silicone O-ring (4.2 mm outside diameter, 2.2 mm inside diameter and 1.5 mm thick) and the large thin black Viton O-rings (7 mm outside diameter, 5.5mm inside diameter and 1 mm thick). They both provide a leak proof seal and have different benefits and drawbacks.

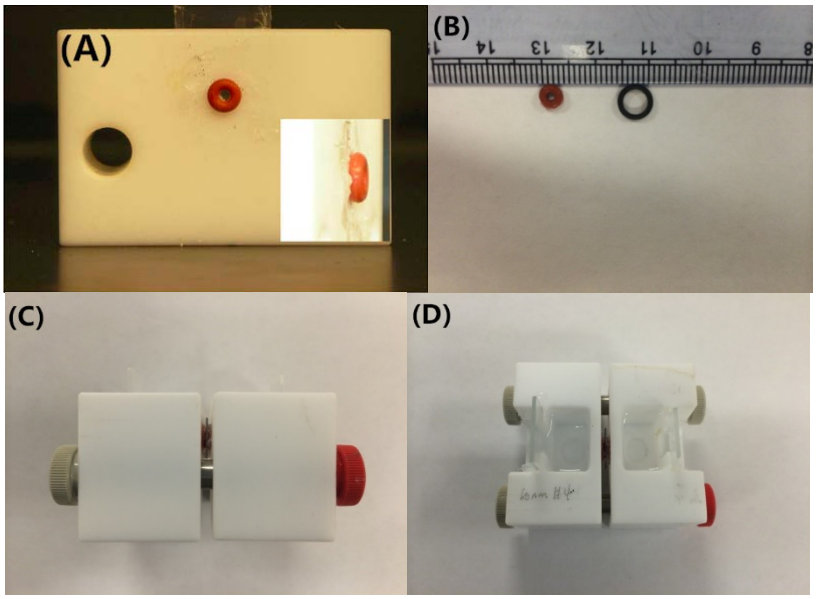


Figure 3. 5: Telfon holder for mounting the nanopore device. (A) Teflon holder with small silicone O-ring. (B) The size comparison between two O-rings. (C) Side view of the mounted nanopore chip. (D) Top view of the mounted nanopore chip.

The drilled holes on each side of the chamber, the center of the O-rings and the nano-aperture in the chip needed to be perfectly aligned to obtain the aqueous access. The red O-ring was soft and it easily got elastic deformed when sealing the chip and chamber. It was also quite small so that any small misalignment between two O-rings caused further position shift and tilted the chip when they were getting squeezed. So the red O-ring had to be well immobilized and aligned on the holder by the glue first. The elastic deformation shrank the inside diameter and gave a very small access from the chamber to the nanochannel which brought the air bubble stuck inside the O-ring. A longer de-bubble time was taken in the desiccator, sometimes it took two days. However, the small contact area of ionic solution on the chip was beneficial since it decreased the whole system capacitance which was proportional to the measurement noise and had less chance to get leakage current during the chip bias step because of the smaller area which brought less defects on the chip surface. The Figure 3.5 C&D show the mounted nanopore device with good alignment using the red O-ring. On the other hand, the larger black O-ring used

the harder Viton. No glue was needed and it made the mounting and de-bubble process much easier. But it brought extra noise and more leakage current because of large contact area.

During the mounting, the chip was very gently handled and delivered using soft tweezers. Any small collision with the chip might break the nanopore membrane. The pore also was kept as wet as possible. Once it got dry, it took larger effort to refill the solution into the channel.

3.3.2 Electrolyte Solutions Preparation

Aqueous HCl, KCl and KOH solutions were used to measure ion transport through the single nanochannel. A broad range of molarities of the solutions were prepared for each type. The 100 mM HCl was first made by diluting the 36.5 % assay hydrochloric acid stock solutions. 4.15 ml stock solution was poured into a VWR media polycarbonate graduated bottle which already filled with 495.85 ml nanopure water from a Cascada Bio water purification system (Pall Corporation, Ann Arbor, MI) to get a 500ml bottle of 100 mM HCl. The 100 mM KCl salt solution was prepared by dissolving of 0.05 M EM Science PX1405-1 KCl powder into 500 ml nanopure water. The next concentration, 10 mM, was made by ten times diluting the 100 mM solution with nanopore water and stored in a 50 ml Falcon Polypropylene conical tube. Similarly, the 1 mM, 100 µM, 10 µM, 1 µM molarity of both HCl and KCl solutions were made by diluting the solution of previous concentration level. The 100 mM KOH solution was prepared by dissolving Potassium Hydroxide solid (85%, EMD) and then it was diluted to get lower molarities as well. The conductivity and pH values were measured and recorded after preparing all solutions as shown in Table 3.1. The salt KCl solutions pH values were at around 5 because the nanopure water is a little bit acidic.

Solution	Conductivity (mS/cm)	PH Value
100mM HCl	26.4	1.36
10mM HCl	2.89	2.16
1mM HCl	0.315	3.20
100μM HCl	0.045	3.94
10μM HCl	0.00277	3.98
1μM HCl	0.00187	4.02
100mM KCl	12	4.34
10mM KCl	1.3	4.67
1mM KCl	0.12	4.86
100μM KCl	0.014	4.99
10μM KCl	0.002	5.30
1μM KCl	0.00186	5.42
100mM KOH	15.3	12.98
10mM KOH	2.03	12.06
1mM KOH	0.16	10.88
100μM KOH	0.011	9.57
10μM KOH	0.003	7.30
Nanopure water	0.00102	5.52

Table 3.1: The pH and conductivity values for different molarities of Hydrochloric Acid (HCl), Potassium Chloride (KCl), Potassium Hydroxide (KOH) solutions and nanopure water. The solution conductivity and pH value were measured by the Accumet XL50 multiparameter meter.

0.1% Triton X-100 (Sigma Aldrich Chemical) was last added to the freshly prepared ionic solution. The non-ionic surfactant helped filling the nanopore with liquid much easier. Although, the non-ionic surfactant residues might adhere on the nanopore surface, partially block the

nanopore and decrease the nanochannel conductance after the pore was immersed in the Triton X-100 added solution for a while, the detergent could not be avoided since it was hard to fill the solution in a 340 nm long 40 nm wide nanochannel without the detergent (Bratov, Abramova et al. 2013).

During preparation of the solution, any type of contamination had to be minimized. All the glassware had to be cleaned in 1:1 solution of sulfuric acid and hydrogen peroxide for 5 minutes and rinsed with deionized water. After drying, they were stored in new airtight plastic bags. 100 mM HCl, 100 mM KCl, 100 mM KOH solutions and nanopure water were filtered one more time using the disposable syringe and 0.1 μm PALL Acrodisc Syringe Filter for diluting to the next concentration. After preparation, all the solution were stored in 5°C refrigerator and the tube lips were tightly closed.

3.3.3 Measurement Tool Setups

The ionic current through the nanopore was measured by the Axopatch 200B (Molecular Devices, Sunnyvale, CA) low noise transimpedence amplifier using Ag/AgCl electrodes (Alfa Aesar, Ward Hill, MA) in the voltage clamp mode (Sherman-Gold 1993). The voltage bias was added on the Silicon surface of the chip using Keithley 236 source measure unit using Wilco aluminum wire and the leakage current going to the silicon was measured simultaneously. Figure 3.6 shows the illustration diagram of electrical setups. The ionic current through a single nanopore under low concentration electrolyte solutions is in the range of picoamperes. The Axopatch 200B is a common low noise amplifier used in electrophysiology for measuring ion transport through lipid bilayers and membrane ion channel. In the voltage clamp mode, it applies a DC voltage to one side of the solution and receives a small current signal through the other one of the Ag/AgCl electrodes. The current signal is then converted to a voltage output via a large feedback resistor which is output to Digidata 1322A data acquisition system.

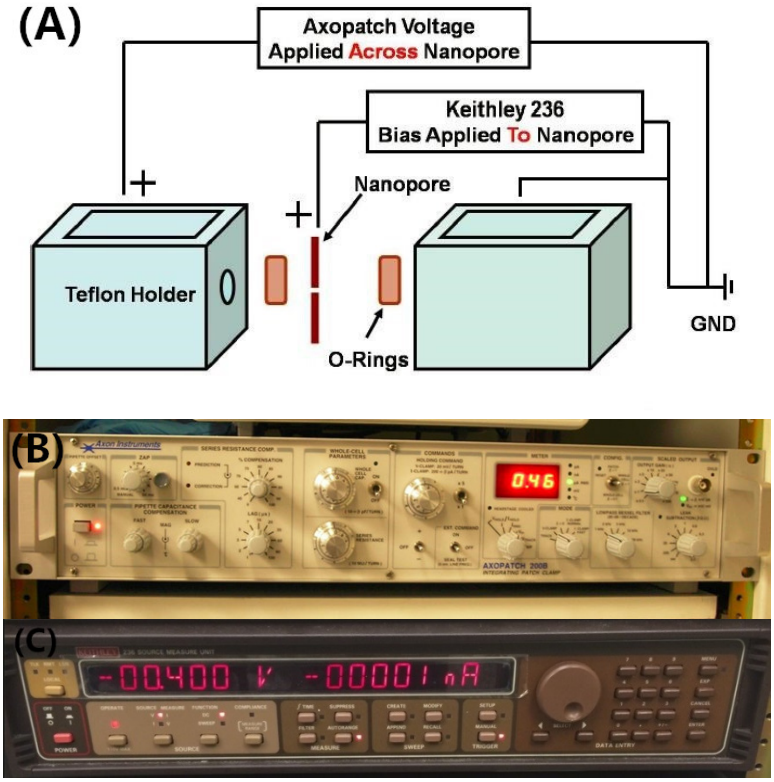


Figure 3. 6: Electrical setups. (A) Electrical set up illustration for the nanopore aqueous ionic current measurement with chip bias modulation. (B) Picture of Axopatch 200B Low Noise Current Amplifier. The red number shows the noise level. (C) Picture of Keithley 236 source measure unit. The left number shows the DC Voltage applied and the right current number shows the current received from the wire.

The aluminum Wilco wire was hooked up the chip surface by being soldered on a PCB board clamp pin as shown in Figure 3.7. The pin was clamped on the chip and was mechanical stabilized by the epoxy glue on the back side of the chip. On the front side, silver paste was painted between the pin and the silicon surface to generate electrical contact. Sometimes, the large surface contact area of silver paste brought extra noise to the measurement. Then, the aluminum Wilco wire was manually positioned to directly contact the silicon surface. The Axopatch 200B electrodes and Keithley 236 wire shared the same ground to ensure the bias leakage current kept in the same loop.

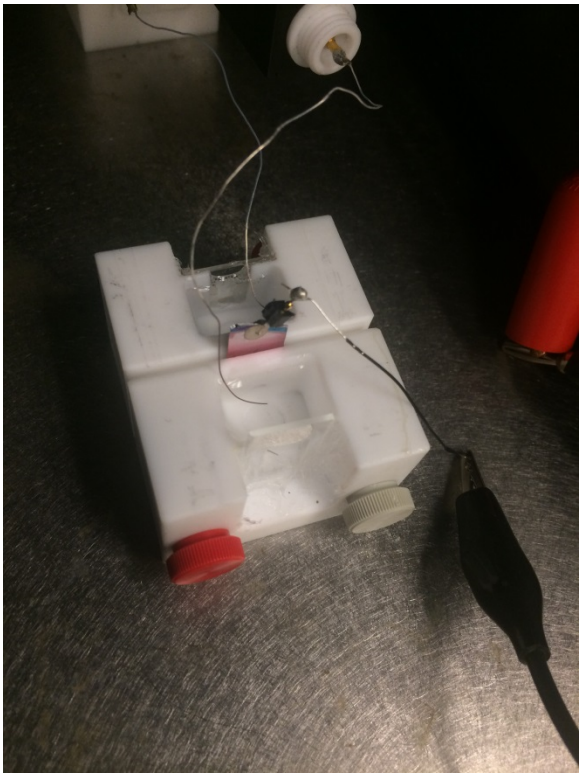


Figure 3. 7: The picture of electrical setups with voltage bias. The nanopore chip was picked from side of the wafer and it had an extra edge area which is easier for biasing. Two Ag/AgCl electrodes from the amplifier headstage were immersed in the bath of each side of the nanopore chip. The aluminum Wilco wire was soldered on the PCB board pin which had the electrical contact with the top silicon surface of the nanopore chip.

3.3.4 Leakage Current Subtraction

As mentioned above, leakage current was generated going to the top silicon layer of the SOI device when the DC voltage bias was applied on that layer. It leaked to the electrolyte solution through the pinholes or grain boundary in the silicon dioxide and through local dielectric breakdown due to the roughness of the surface. No matter what kind of leakage mechanism it is, it has to be subtracted before getting the real ionic current though the nanochannel.

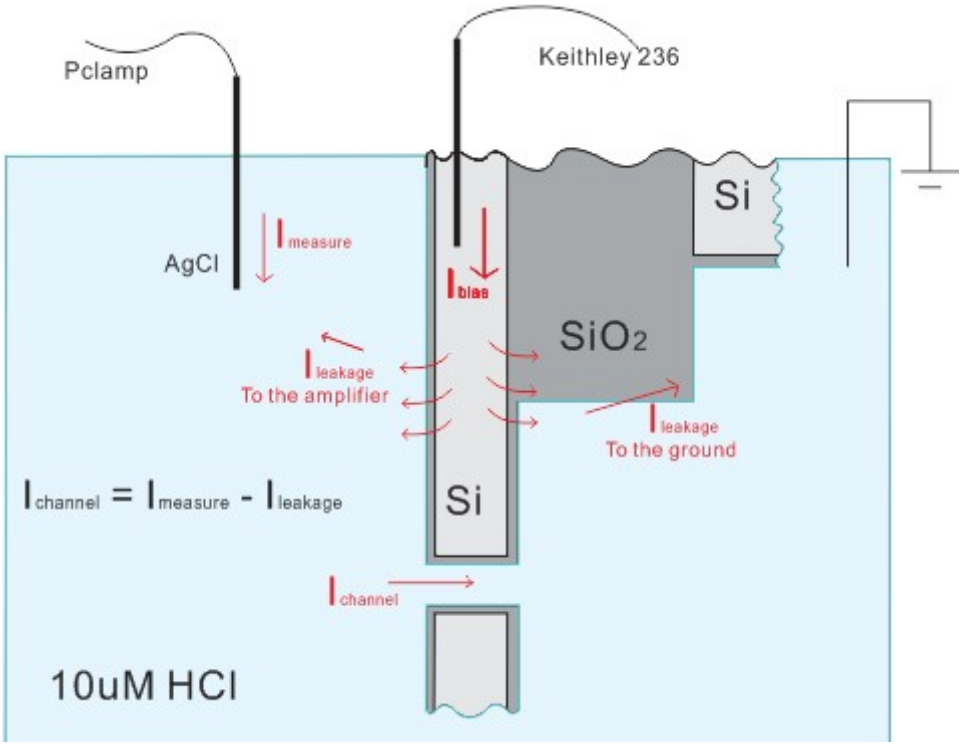


Figure 3. 8: Leakage current diagram.

Figure 3.8 illustrates the leakage current flow from the top silicon layer to the solution bath. One part goes through the front side of the device to the Axopatch amplifier. Another part goes to the ground from the back side of the device. For the nanopore ionic conductance measurement under the substrate bias modulation, the bias voltage was applied before a transmembrane voltage applied (V_{pclamp} = 0V), and a total leakage current number (I_{bias1}) was shown on the Keithley 236. At this time current offset ($I_{pclamp1}$) could be read from the amplifier (Pclamp software) was generated and it was equal to the leakage current through the front side of the device ($I_{pclamp1} = I_{leakage1}$). The other part ($I_{bias1} - I_{leakage1}$) went to the ground. Then a V_{pclamp} was applied, both current in the Pclamp and Keithley turned into another value ($I_{pclamp2}$ & I_{bias2}). The leakage current from the front side ($I_{leakage2}$) now proportionally increased to $I_{leakage1} * \frac{Ibias2}{Ibias1}$. The real ionic current going through the nanopore was derived by being subtracted by $I_{pclamp2}$.

$$I_{channel} = (I_{pclamp2} - I_{leakage1} * \frac{Ibias2}{Ibias1}) \quad (3.7)$$

3.3.5 Measurement Procedure and Tips

The whole measurement was placed in a Faraday cage as shown in Figure 3.9. It filtered out most of the mechanical vibrations and electrical noise such as the 60 Hz building power noise injecting in the current trace. It created a mechanical stable and electrical noise isolated environment which was also the prerequisite for the nanopore ionic transport experiments.

Figure 3. 9: Faraday cage for electric noise and mechanical vibration isolation.

Before the measurement, the continuity test on the pore was first run using high molarity solution such as 100 mM HCl to see whether the pore was filled with aqueous solution properly. Two Ag/AgCl wires which were prepared by soaking Silver wires in 5% sodium hypochlorite (NaOCl, Bleach) solution for 20 minutes were inserted to the holder trans and cis baths respectively from the headstage. A baseline current was recorded using Clampex software by applying a constant DC voltage. The conductance level could tell whether the pore was completely filled by roughly comparing the theoretical bulk conductance equation

$$G = \sigma * A/L \tag{3.8}$$

where σ is the solution conductivity, L is the length of the nanoaperture and the A is the cross section area. Once the single nanopore was properly filled with solution, the measured value was

very close to the theoretical value and the surface conductance only played a very small role under high concentration solution. When the measured value apparently differed from the theoretical value, it showed that an air bubble was still stuck inside the pore, and the chamber bath was changed back to nanopure water and vacuum pumped for several hours in the desiccator until continuity could be measured.

During the exchange of the bath, pipet tips were kept very clean after first use and no crossover using different concentration of the solution was allowed. Any particle or dirt would cause blocking the pore in this series of measurements. After the continuity test was done, the nanopore was rinsed by nanopure water at least 3 times before changed to lower molarity solution.

The bias electrode electrical contact was checked before the measurement. A good contact showed leakage current injection on the current trace when negative bias was applied with zero transmembrane voltage. During the measurement, Keithley 236 was set back to 0 V for a while before the bias voltage was changed to another value to get accurate charge accumulation amount on each bias voltage level.

After the measurement, 3 times rinse with nanopure water was used again. The holder with the chip was stored in the desiccator under the vacuum to avoid contamination and liquid evaporation. Dr. Punarvasu Joshi used to seal the water inside the holder using Parafilm. But the tight wrap with Parafilm sometimes caused the leakage of the holder from the glue between the acrylic glass window and the holder. Once it happened, the chip had to be remounted, refilled. However, the silicon dioxide or ALD alumina layer would be peeled off at where it contacted the O-ring causing the loss of electrical isolation. Therefore, one single nanopore chip cannot be remounted multiple times unless it was recoated with the dielectric layer which, however, would shrink the diameter of the nanopore.

3.4 Nano-channel Conductance Measurement Results with Gate Voltage Modulation

3.4.1 Ionic Current through SiO_2 Gate Dielectric Nanopores

The SiO_2 gate dielectric 60 nm single nanopore ionic current was first measured using low molarity 10 μM HCl ionic solution with the gate bias modulation. Figure 3.10A shows the current transient trace with both -8 V gate bias (black) and 0 V gate bias (red) under a 0 V to 1 V transmembrane voltage step. The black trace shows a much larger current step which is corresponding to a larger ion channel conductance under negative gate bias. To be quantified how much it gets enhanced, the leakage current injected from electrolyte to the silicon substrate was excluded according to the steps in section 3.3.4.

In the black trace, the 350 pA upshift at the region of V_{trans} = 0 V corresponds to the leakage current through the front side of the device,

$I_{pclamp1} = I_{leakage1}$ = 350 pA

The total bias leakage current read from Keithley 236 is I_{bias1} = -560 pA when V_{trans} = 0 V and I_{bias2} = -600 pA when V_{trans} = 1 V. Negative sign shows the current flows from the dielectric layer to the gate electrode since a negative bias is applied. Then the injected current through the front side of the device to the amplifier at V_{trans} = 1 V is

$I_{leakage1} * \frac{Ibias2}{Ibias1} = 350 * \frac{600}{560}$ = 375 pA

I_{plamp2} is at 500 pA which is shown in the trace, then the actual ionic current through the nano channel after subtracting the leakage current is

$I_{channel} = (I_{pclamp2} - I_{leakage1} * \frac{Ibias2}{Ibias1}) = 500 – 375 = 125$ pA

The original current step in the red trace is 25 pA. The -8V gate bias shows a 4 times enhancement in channel conductance.

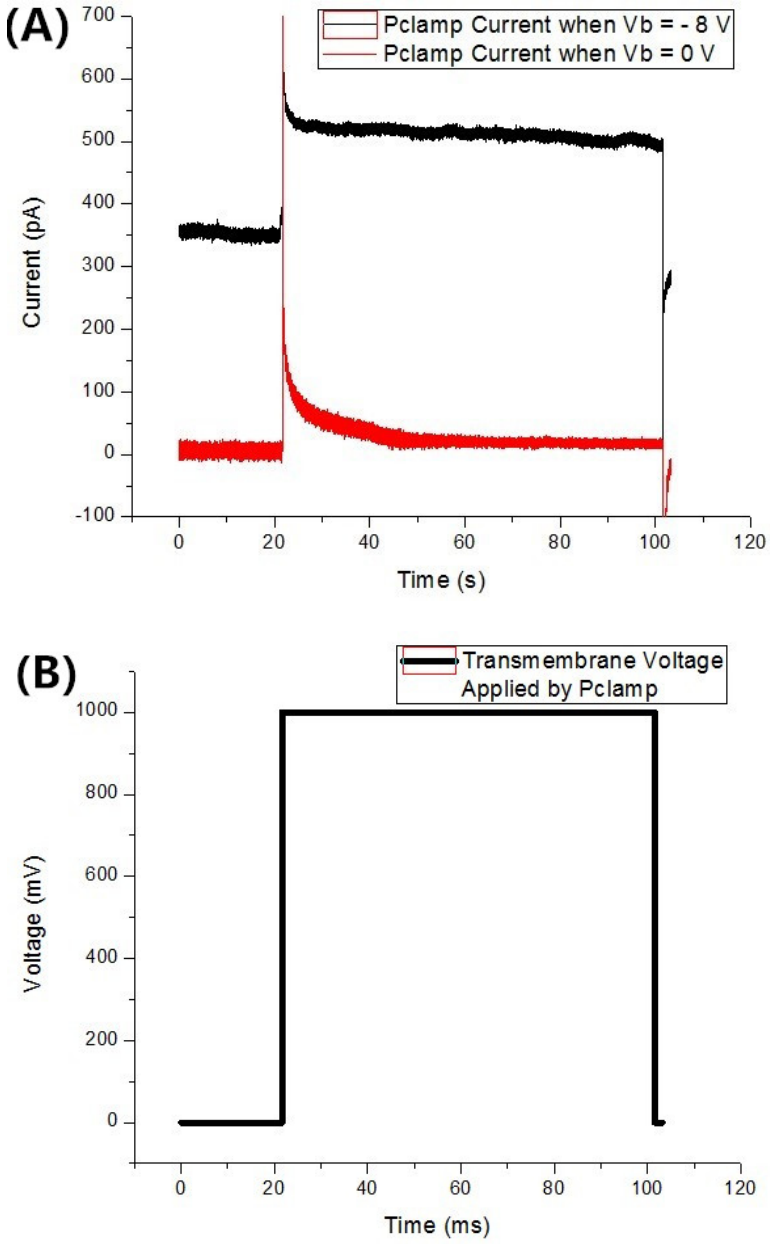
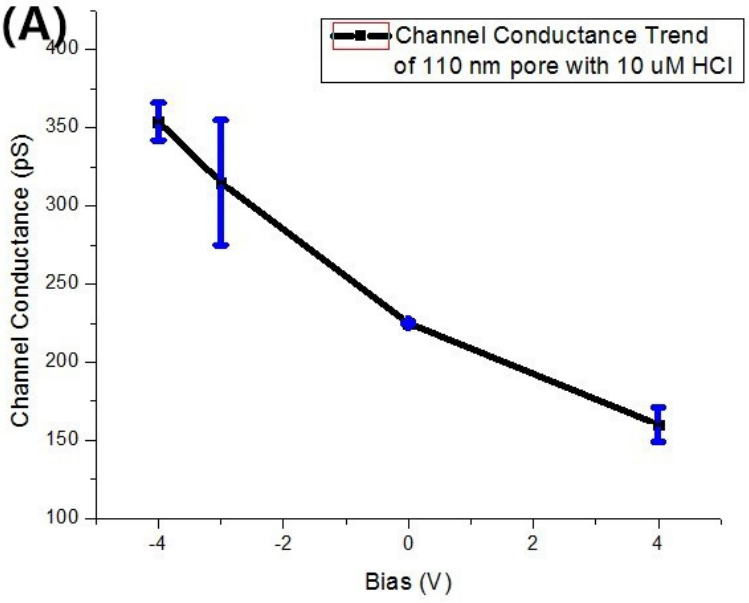


Figure 3. 10: (A) Current trace of 60nm wide SiO_2 gate dielectric pore with 10 μM HCl ionic solution under 0V bias (red) and -8V bias (black). (B) Transmembrane voltage applied from the amplifier.

The isoelectric point of silicon dioxide surface is at pH value of 2 where the surface carries no net electrical charge. The low molarity HCl ionic solution shows a pH of 4 to 5 so that the silicon dioxide surface is negatively charged and the surface charge density is at around -5 to

-15 mC/m^2 (Kosmulski 2001, Dove, Craven 2005). In the SiO_2 naopore, hydrogen ions are counter-ions and chloride ions work as co-ions. Once the negative bias was added on the gate, it attracted the more hydrogen ions into the pore and depletes co-ions (Joshi, Smolyanitsky et al. 2010, Smolyanitsky, Saraniti 2009). Since Cl^- ions' mobility is only about 25% of the H^+ ions' mobility in water (Lide 2008), these high mobility extra hydrogen ions resulted in a high ionic current in the nanopore channel.

A set of conductance data was plotted as the change of gate bias V_g using 10 μM HCl ionic solution on both 110 nm and 60 nm pore. All the values corresponded to the actual ionic current which was subtracted by the leakage current. At the negative bias side, the channel conductance prominently increased with negative bias absolute value due to the attraction of hydrogen ions in the ion channel by the bias. On the other hand, when a positive gate bias was applied, Cl^+ ions started to be attracted into the pore and H^+ ions got depleted. The 110 nm pore and 60nm pores' curves show the same conductance trend because the Debye layer overlapped in both pore in such a low molarity electrolyte solution.



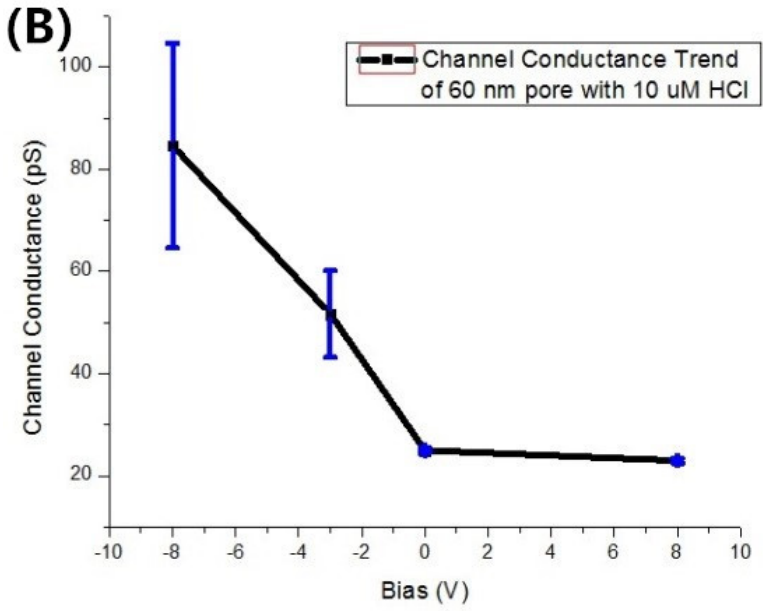


Figure 3. 11: Single nanopore conductance in 10 μM HCl under gate bias modulation (A) Nanochannel conductance of 110 nm diameter pore. (B) Nanochannel conductance of 60 nm diameter pore. Transmembrane voltage is 1 V. Error bar is noted in blue

3.4.2 Ionic Current through Al_2O_3 Gate Dielectric Nanopores

The isoelectric point of ALD surface is at pH value of around 8.5. It shows a positive surface charge density at 40 to 60 mC/m^2 in the low molarity HCl ionic solution which has a pH value between 4 to 5(Dove, Craven 2005, Kosmulski 2001). This provides a good comparison with negatively charged SiO_2 surface for us to better understand how ions move corresponding to different surface charges. On the other hand, KCl cannot be used in SiO_2 pore since the Potassium ion has high mobility in the amorphous SiO_2 and it penetrates SiO_2 fast and brings noise in the measurement (Sze 2002). However, Potassium is an essential mineral macronutrient and is the main intracellular ion for all types of cells. It is very common to be used as biological solutions in all kinds of biosensors. It is necessary to understand how Potassium ions move in the nanopore and contribute to ionic current under field effect modulation. Alumina coated surface provides this platform perfectly solved the incompatibility issue of potassium ions to the nanopore surface. Not like the H^+ ions having a much higher mobility than the Cl^- ion, the K^+ ion has very

similar mass and mobility as the Cl^- ion's ($7.6*10^{-8}$ $m^2V^{-1}S^{-1}$ for K^+ and $7.9*10^{-8}$ $m^2V^{-1}S^{-1}$ for Cl^-) (Lide 2008). The symmetric, monovalent KCl salt ionic solution can help explain how ions move under different bias voltages.

The experiments started with the ionic current measurement with 100 mM HCl and 100 mM KCl electrolyte solutions as shown in Figure 3.12. The nanopore chip was coated with a homogeneous 10 nm ALD alumina layer which shrank the nano-aperture size to 40 nm from 60 nm. The applied transmembrane voltage V_{DS} was changed to 0.4V since large voltage brought random spike noise to the current signal. The measured conductance values were close to the theoretical bulk resistance equation. Higher conductance of HCl ionic solution was due to the higher mobility of hydrogen ions. Both traces did not change with the gate voltage. The Debye length was quite thin under these two molarities so that any ions distribution change in the diffusion layer due to the bias did not affect the bulk conductance.

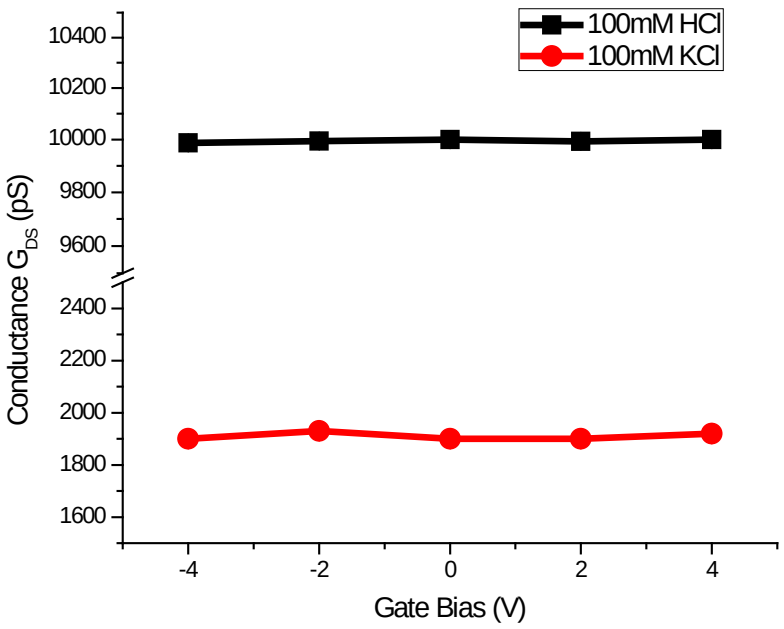


Figure 3. 12: The 40nm Alumina pore conductance in 100mM HCl (Black) and 100mM KCl (Red) ionic solution with the change of gate bias. Transmembrane voltage is 0.4 V.

The low molarity 10 μM HCl and 10 μM KCl electrolyte solutions were tested on the 40nm Alumina pore. The positive surface charge made the nanopore as a chloride ion dominant channel. For the 10 μM HCl trace, the increasing ionic current at the negative bias side showed the negative gate bias was still attracting H^+ ions to the stern and diffusion layer bias irrespective of the surface charge type. On the positive bias side, it further depleted H^+ ions and caused the slightly ionic current drop although some chloride ions got attracted inside channel. The interesting result was got on the 10 μM KCl ionic solution measurement. It showed flat on the negative side and slight decrease on the positive and same results were reproduced on another two 40 nm pores with multiple measurements.

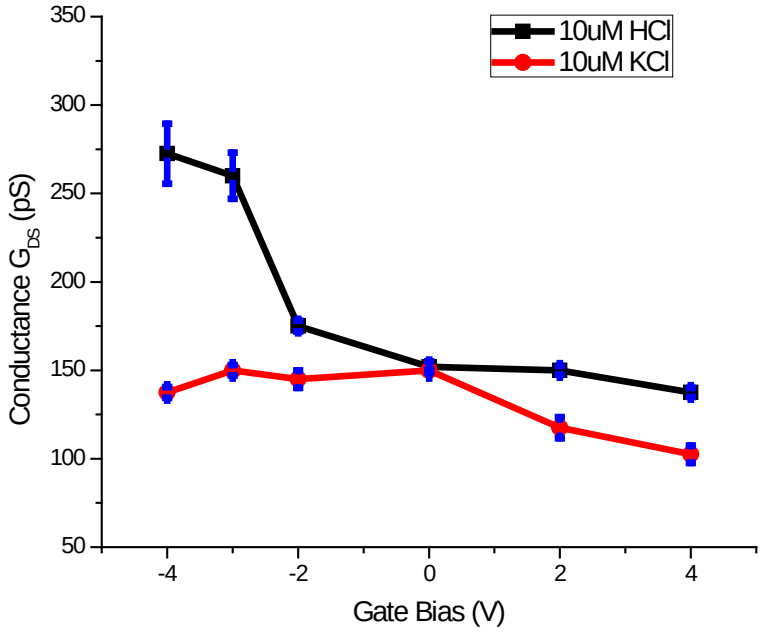


Figure 3. 13: The 40nm Alumina pore conductance in 10 μM HCl (Black) and 10 μM KCl (Red) with the change of gate bias. Transmembrane voltage V_{DS} is 0.4 V.

Let's start with counting the number of ions in side and surrounding the nanopore.

For 10 μM KCl ionic solution, the density of ions is

ρ = Molarity * N_A = $10*10^{-6} * 6.023*10^{23} = 6.023 * 10^{18}$ Cl^- ions/L = $6.023 * 10^{21}$ Cl^- ions/m^3

The volume of the 40nm diameter 360nm long cylindrical nanopore is

$V = \pi r^2 * L = 4.5*10^{-22}\ m^3$

If the pore is zero surface charges, the number of total molecules is

$\rho * V = 2.7$ molecules

which means there are only about 3 K^+ and 3 Cl^- ions floating in the pore.

However, for the alumina surface which has a surface charge of σ=40 mC/m^2 and total inside surface area of $A_S = \pi*d*L = 4.5 * 10^{-14}\ m^2$, the total number of monovalent ions to compensate the surface charge is

$N = A_S*\sigma/q = 11250$ ions

It is impossible for the Cl^- ions in such a low concentration of KCl ionic solution to compensate all the charges on such a large surface. Then the inside surface of pore tries adsorbing as many Cl^- ions as it can, but it still shows a positively charged ion channel and most of the Cl^- ions are adsorbed in the stern layer. The liquid in the stern layer is completely immobilized, more and more evidences show counter-ions are partially mobile in this region. (Bonthuis, Netz 2012, Lyklema 2014, Lyklema, Minor 1998, Kim, Netz 2006) Therefore, in this alumina nanopore with 10μM KCl, the ionic current is attributed by partial of the Cl^- ions in the stern layer and some K^+ ions in the diffusion region.

When positive bias was applied on the chip, it tried to adsorb more Cl^- ions on the surface inside the pore. However, there was no more counter-ions floating in the ionic solution. No matter if the inside surface can get more Cl^- ions, all the Cl^- ions became hard to move because of the increasing Electrofriction between chloride ions and the surface brought in by the bias voltage (Kim, Netz 2006, Netz 2003). Furthermore, the positive bias made it harder for the K^+ ions to go inside the pore during the ion transport. These two reasons caused a drop of ionic current on the positive bias side. On the negative bias side, Cl^- ions were still stuck on the walls and K^+ ions were still repelled by the strong surface charges so that the current level almost kept flat. The slight drop of the conductance may be caused by the release of some Cl^+ ions outside of the pore. However, for the HCl solution, it is a different story. The hydrogen ion is extremely small and light.

It got easily migrated by the negative bias inside either negatively charged or positively charged pore.

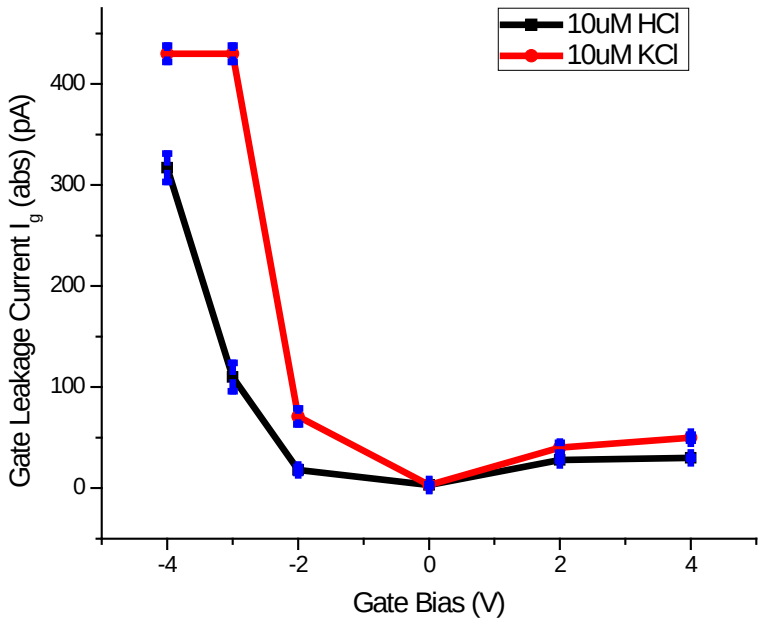


Figure 3. 14: Gate Leakage Current I_g flowing into 40nm Alumina pore substrate in 10 μM HCl (Black) and 10 μM KCl (Red) as a function gate bias.

The leakage current to the gate electrode I_g was recorded from Keithley 236 with the change of gate bias as shown in Figure 3.14. The substrate current grew rapidly when a negative bias was applied and therefore it was limited to small magnitude negative bias voltages up to -4 V. At the positive side, the leakage current was quite stable even up to +50 V. The leakage current result is similar to Dr. Zhang's paper (Zhang, Gamble et al. 2008). The 58.6 nm thermal Silicon Dioxide layer plus 10nm ALD Alumina layer provided a strong dielectric strength which could tolerate a large electrical field with is 0.77 V/nm in (Jiang, Stein 2010) without breakdown.

3.5 Summary

In this Chapter, the ion transport in both negatively surface charged SiO_2 and positively surface charged Al_2O_3 covered SOI single nanopore with gate bias modulations has been studied. The bias started to affect the ionic current through the nanopore only in low molarity solutions when the Debye layer overlapped inside the nanopore channel. In 10 μM HCl, the nanopore ionic current increased in no matter negatively or positively surface charged nanopores with negative gate bias. In both cases, the negative bias attracted more H^+ ions, mobility of which was much higher than Cl^- ions', into the nanochannel and provided a higher conductance. The depletion of H^+ ions under positive bias decreased the ionic current in the nanochannel. In low molarity KCl electrolytes, the voltage bias had no effective control on ionic current due to the similar mobility of K^+ and Cl^- ions.

4. IONIC TRANSPORT IN SOI SINGLE NANOPORE COATED WITH POLYELECTROLYTE BRUSHES

4.1 Introduction to Integration of Polyelectrolyte Brushes in Nanopores

Polyelectrolyte brushes are brush like layers which are composed of charged polymer chains, one end of which is tethered to a solid surface. They change their conformations such as charge density and hydrophilicity under different stimuli like pH of the ionic solutions and temperature.(Wei, Ngai 2012) During the last few years, varieties of polyelectrolyte brushes were integrated into solid-state nanochannels using to control the ion transport inside the channel.(Guo, Xia et al. 2010, de Groot, Santonicola et al. 2013, Zhang, Cai et al. 2011, Yameen, Ali et al. 2010, Tagliazucchi, Szleifer 2012) Yameen's group grafted pH-responsive poly (4-vinyl pyridine) brushes into the inner walls of a PET-made single nanochannel. An on/off channel conductivity switch was achieved by manipulating the surface charges of the brushes under different pH solutions (Figure 4.1).(Yameen, Ali et al. 2009) In Guo's group, temperature and pH dual-stimuli-responsive P(NIPAAm- co -AAc) copolymer brushes were dressed into polyimide nanopore. Other than the surface charges changes under different pH, the brushes also exhibited a conformational change with different temperature so as to rectify the channel ionic current. (Guo, Xia et al. 2010) Integration of environmental stimuli-responsive PE brushes into nanochannel created promising implications for nano-fludic deivces like molecular gating, stochastic DNA sequencing.

In this Chapter, poly[2–(dimethylamino) ethyl methacrylate] (PDMAEMA) polyelectrolyte brushes were grown on the inner walls as well as the surface of the thermal oxidized SOI cylindrical single nanopore using surface-initiated atom transfer radical polymerization (SI-ATRP). SI-ATRP is a uniform polymer chain growth method by forming Carbon-Carbon bond with a transition metal catalyst in Oxygen free atmosphere. After the polymerization, the electrical response of the nanopore was tested using Electrochemical Impedance Spectroscopy (EIS). EIS spectra not only extracted the conductance parameter of the nanopore but also gave capacitance information for each part of the device after equivalent circuit was built. Substrate DC bias was

added on the polymerized chip in low molarity HCl ionic solution. The ions transport in the PDMAEMA brushes nanopoore was studied under both pH and gate bias stimuli.

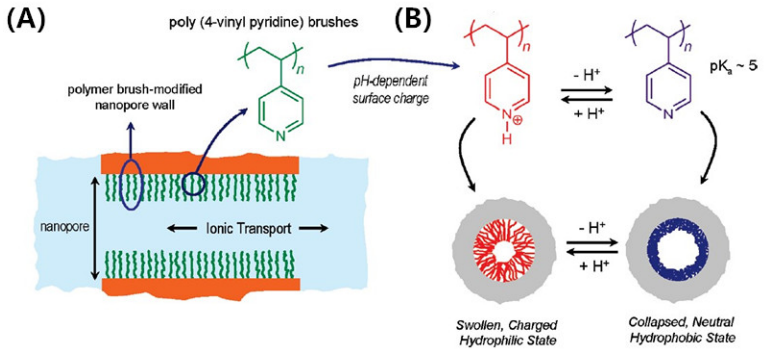


Figure 4. 1: (A) Illustration diagram of poly(4-vinyl pyridine) brushes grafted on the sidewalls of polyethylene terephthalate (PET) single cylindrical nanochannel. (B) Simplified illustration shows that polymer brushes got protonated or deprotonated with the change of environmental pH and formed charged hydrophilic state or neutral hydrophobic state. Figure is from Dr. Yameen's paper.(Yameen, Ali et al. 2009)

4.2 Experimental Flow of Polymerization of PDMAEMA Brushes on SOI Single Nanopore

The 1 cm X 1 cm thermal oxidized SOI single nanopore chip was first dipped into a piranha solution, H_2SO_4 and H_2O_2 at 1:1 ratio, for 5 mins followed by rinse in DI water to remove all the organic comtaminations on the chip. In the meantime, the chip's surface as well as the interior nanopore channel sidewalls were uniformly coated with a monolayer of silica hydroxyl groups (Fig. 4.2A). The cleaned chip was dried in a nitrogen filled oven at 80°C for 5 minutes. The amino terminal group was then immobilized on top of the hydroxyl group on the nanopore channel sidewalls by dipping the chip in 5% APTES (99%, Sigma-Aldrich) in absolute ethanol for 30 mins, followed by rinsing with ethanol and drying in nitrogen atmosphere at 80°C for 30 minutes (Fig.4.2B). The ATRP initiator solvent solution was made by mixing 1 portion of 2-Bromoisobutyryl bromide (98%,TCI) into the solution of 5 portions of anhydrous Dichloromethane (99.9%, Fisher Scientific) and 2 portions of Triethylamine (>99%, Sigma-Aldrich). The chip

reacted with the initiator solution in the borosolicate glass sample vial in nitrogen atmosphere at room temperature for 8 hours. The initiator 2-Bromoisobutyryl Bromide was linked to the amino-functionalized nanopore surface through carbon-nitrogen bond (Fig.4.2C). The initiator immobilized nanopore chip was then rinsed using Dichloromethane followed by ethanol and dried in air atmosphere under room temperature.(Zhang, Cai et al. 2011)

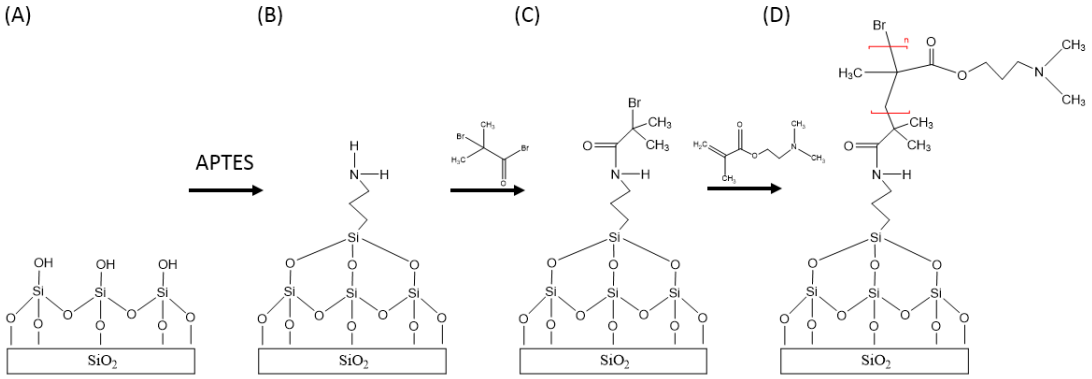


Figure 4. 2: Schematic representation of SI-ATRP of PDMAEMA polyelectrolyte brushes on thermal oxidized SOI nanopore surface. (A) Amino group was immobilized on surface after piranha clean. (B) APTES linked to OH groups and presented NH_2 groups on surface. (C) 2-Bromoisobutyryl bromide initiator was bonded to nitrogen atom. (D) DMAEMA got polymerized from the initiator in Oxygen-free atmosphere at 60°C and long chain polyelectrolyte brushes grew on the nanopore surface.

The poly[2–(dimethylamino) ethyl methacrylate] (PDMAEMA) polyelectrolyte brushes grew from polymerization of DMAEMA (99%, Acros Organics) using SI-ATRP method in oxygen-free environment with being catalyzed by Copper(I) bromide (98%, Sigma-Aldrich) at 60°C (Fig.4.2D). DMAEMA was 1:1 dissolved in methanol in a Schlenk flask and 0.3g CuBr for every 1ml reaction solution was added in the flask. After the solution was mixed and stirred, the nanopore chip was placed in the solution. The flask was then put into water bath which can be heated and nitrogen gas was fed into the flask from one side of the sidearm and outflowed though

the flask neck to the outside as shown in Figure 4.3. The reaction solution was degassed for 1 hour by the Nitrogen fill cycle. The polymerization started after water bath was heated to 60°C and lasted for 8 hrs. The whole reaction process prevented from Oxygen leakage otherwise the carbon chain would have broken by C-O reaction and the polymerization would have terminated. After the growth, the nanopore chip was rinsed with methanol and DI water.

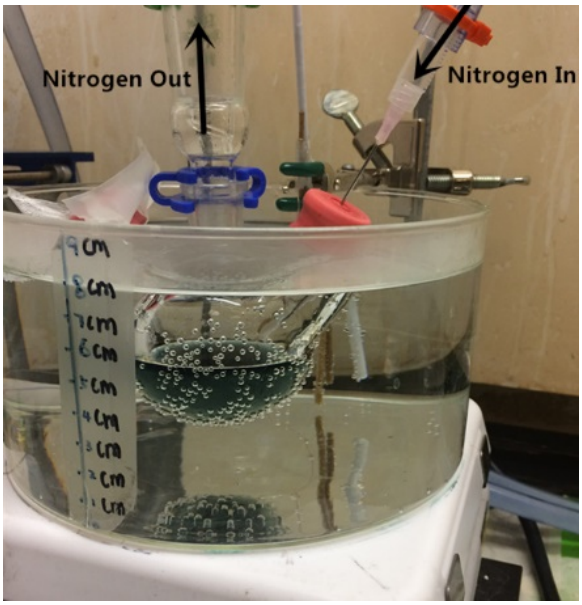


Figure 4. 3: Picture of polyelectrolyte brushes' polymerization step setups under nitrogen atmosphere.

Atomic Force Layer (AFM) was used to measure the thickness of PDMAEMA polyelectrolyte brushes on the SOI nanopore device. A gentle scratch was applied to the chip surface to locally remove the polymer layer. As shown in Figure 4.4, the polymer was coated very uniformly and an average thickness of 25nm was obtained after 8-hour SI-ATRP of DMAEMA.

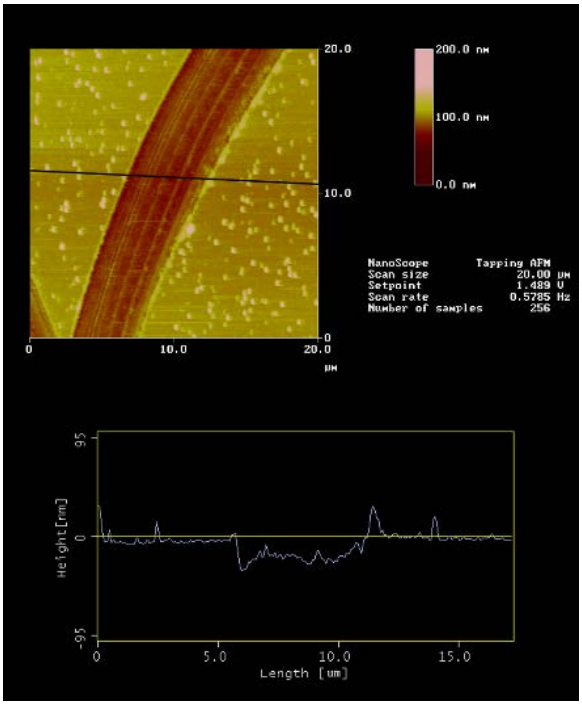


Figure 4. 4: AFM picture of scratched polymer coated nanopore chip surface showing a 25 nm-thick layer of PDMAEMA polyelectrolyte brushes.

4.3 Measurement of Ionic Transport in PE Coated Nanopore Using Electrochemical Impedance Spectroscopy (EIS)

4.3.1 Introduction to Electrochemical Impedance Spectroscopy (EIS)

Electrochemical Impedance Spectroscopy (EIS) is a widely employed electrochemical systems characterization tool in fields such as fuel cell testing and biomolecular interaction. It measures the dielectric properties of a medium as a function of frequency. The tool reads out the AC current response of a system once a small alternating potential stimulus is applied and the impedance is presented in a complex form after Fourier Transformation.

The applied AC voltage and AC current in the complex form can be expressed as

$$V(j\omega) = V_0 e^{j\omega t} \tag{4.1}$$

$$I(j\omega) = I_0 e^{j(\omega t+\varphi)} \tag{4.2}$$

where V_0 and I_0 are the amplitudes of the AC voltage and current, respectively, angular velocity $\omega=2\pi f$，φ is the phase difference of sinusoidal current with respect to the voltage and $j \equiv \sqrt{-1}$.

The complex impedance is defined as

$$Z(j\omega) = \frac{V(j\omega)}{I(j\omega)} = \frac{V_0}{I_0} e^{-j\varphi} = | Z | e^{-j\varphi} = | Z | [\cos(\varphi) - jsin(\varphi)] \quad (4.3)$$

It can be plotted as a planar vector on polar coordinates while

$$\mathrm{Re(Z)} = | Z | \cos(\varphi), Im(Z) = -| Z | \sin(\varphi) \quad (4.4)$$

As the frequency of the signal changes, different impedance vectors can be drawn on the same planar coordinates and form a Nyquist diagram as show in Figure 4.5B. The complex impedance can be also plotted as a bode plot, displaying the magnitude and the phase shift as a function of frequency as shown in Figure 4.5C and Figure 4.5D.

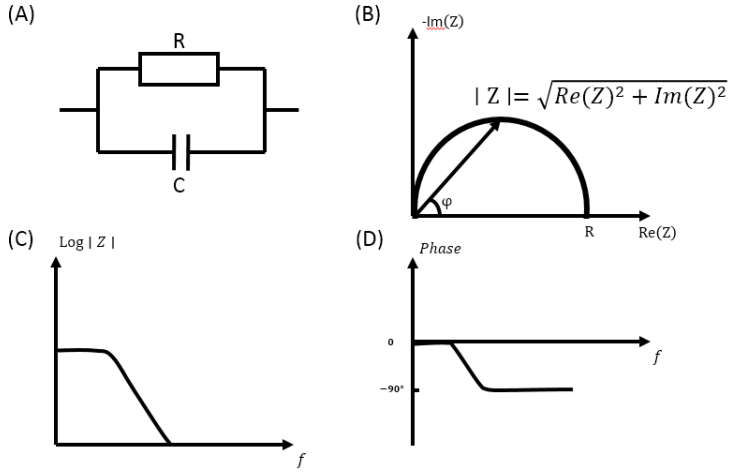


Figure 4. 5: (A) A simple resistor and capacitor parallel model. (B) Nyquist plot for the RC parallel impedance. (C) Bode plot for the impedance. (D) Phase shift plot for the impedance.

In the electrochemical experiment, the system can be interpreted by suitable equivalent circuits using parameters which are extracted from EIS plots. The circuits are built of passive elements such as resistors, capacitors and inductors which can be expressed using complex form in following equations:

$$Z_R = R \quad (4.5)$$

$$Z_C = \frac{1}{j\omega C} \quad (4.6)$$

$$Z_L = j\omega L \tag{4.7}$$

In a real system, the samples usually are coated non-homogeneously and do not show purely capacitive properties. For example, the polymer on a substrate is not uniformly coated or in an electrical double layer, the ion distribution is not uniform etc. The model then can be represents by Constant Phase Element (CPE) using following equation:

$$Z_Q = \frac{1}{Q_0(j\omega)^n}, 0 \leq n \leq 1 \tag{4.8}$$

where Q_0 is the admittance of an ideal capacitance and n is an empirical constant. When n=1, the CPE behaves as a pure capacitor and it behaves as a pure resistor when n=0. When n=0.5, the element is called Warburg Impedance (W) which shows ionic diffusion properties and commonly used in Randles circuit which describes ionic kinetics from an electrode to electrolytes.(RANDLES 1947) Q has units of $Fcm^{-2}s^{n-1}$.

With linking these elements in parallel or series, any nanofludic system is able to be represented using an equivalent circuit. After a circuit model corresponding to the measured system is set up correctly, the impedance of each element in the circuit can be found by fitting and matching the impedance Bode and Nyquist plots of the circuit to the one which is measured in EIS. The value of each electrical passive component can help to analyze the physical and electrical properties and geometry of each part which the component is corresponding to in the system. The changes of values during the experiment would also reveal the reaction mechanism of the electrochemical process which is hard to be directly characterized by other methods. An ECOChemie Autolab PGStat 302 potentiostat/galvanostat was used for the EIS measurementsin this Chapter and the RMS value of the voltage was set at 25 mV.

4.3.2 Equivalent Circuits Model of Nanopore Device

Figure 4.6A shows the cross section illustration of a PDMAEMA polyelectrolyte brush coated nanopore sample filled with electrolyte for the conductance measurement. The sample was vertically mounted between the 2.2 mm diameter O-ring and the holder which is shown in Figure 3.5C. C_{sub} stands for the substrate capacitance, which is mainly contributed from the 1 μm

thick BOX layer with an area of the O-ring inner area being exposed to electrolytes. R_{acc} represents the access resistance of the electrolyte inside and near the 100 µm diameter 450 µm long micropore channel. $R_{nanopore}$ is the equivalent resistance for the 60 nm diameter and 360 nm long cylindrical nanopore area. The conductance is contributed by the solution and polymer original conductance inside the nanopore, the counter-ions in the double layer from the nanopore interior sidewalls and the Hydrogen ions, which were originating from the protonation of tertiary amine groups in the PE brushes once it was filled with acid electrolyte. $Q_{nanopore}$ is the Constant Phase Element (CPE) of PE brushes coating on the device surface and the inside of the nanopore. It also contains the capacitive contribution from the nanopore and the 60nm thermal silicon oxide on the device layer. It is represented using a CPE rather than a pure capacitor because of the defects and voids in the polymer coating, roughness of the surface and the ion diffusion inside the PE layer during the experiment, making it an imperfect capacitor.

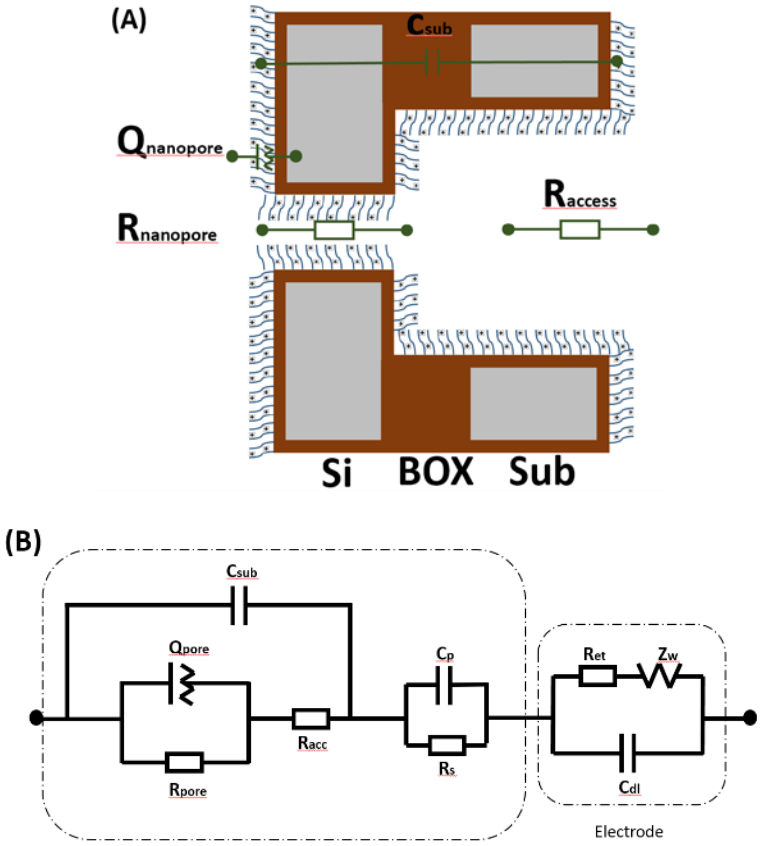


Figure 4. 6: (A) Electronic illustration of the SOI nanopore chip cross section. C_{sub}, R_{acc}, $R_{nanopore}$, $Q_{nanopore}$ stand for capacitance of the substrate, access resistance of the electrolyte inside and near the backside micropore channel, resistance of the nanopore and the CPE value from the nanopore, PE layer and thermal oxide layer on the surface and inside the nanopore, respectively (B) Equivalent circuit of filled nanopore device measured by Pt electrodes.

From the cross section view, C_{sub} is throughout the whole device so that it is parallel with the other three components. Q_{pore} and R_{pore} are parallel with each other since they both stand for the electronic passive components for the nanopore and near nanopore area. The resistance of the micropore R_{acc} is connected in series with these two so that the equivalent circuit of the SOI chip is obtained as shown on the left dashed block chart in Figure 4.6B. A resistor and capacitor parallel group (R_s and C_p) is connected next to the chip in series which stands for the solution resistance and stray or parasitic capacitance of the system. The circuit model is very similar to Kant and Feng's models of their Nanoporous alumina membranes (NPAMs) and conical glass nanopores (Feng, Liu et al. 2010, Kant, Yu et al. 2014). For the equivalent circuit at the electrode and electrolyte interface as shown on the right dashed block chart in Figure 4.6B, a double layer capacitor (C_{dl}), which is associated with the charging process of the interfacial capacitance is placed in parallel with an electron transfer resistance (R_{et}) and a Warburg impedance (Z_W), which results from the semi-infinite diffusion of electroactive species from the bulk electrolyte to the electrode interface. (Katz, Willner 2003, RANDLES 1947)

4.4.3 EIS Measurement on PE Coated Nanopores in High Molarity Electrolytes

The polymer coated 60nm pore was first tested using EIS under both high pH (100 mM KOH pH 12.98) and low pH (100 mM HCl pH 1.34) electrolytes, which the PE brushes were sensitive to. A non-PE coated 60nm nanopore was measured in the same ionic solution for comparison. Figure 4.7 shows the Bode plots of the phase and impedance spectra of a PE and a non-PE coated 60nm nanopore in 100mM KOH ionic solution. A difference at low frequency (0.1Hz to 100Hz) in both impedance and phase plots could been observed. In the impedance

curves, the PE brush coated pore had a much higher impedance at near DC range in 100mM KOH ionic solution. The PDMAEMA brushes got deprotonated in high pH KOH ionic solution and its charge turned to become neutral. The pore was likely coated with a nonconductive layer which took away the some room of the conductive electrolyte inside the nanopore, rendering a much higher impedance. The -30° phase at 0.1Hz showed that the movement of ions in the PE pore was lagging behind in the DC field compared to the simultaneous response in the non-PE nanopore, which did not have a phase shift.

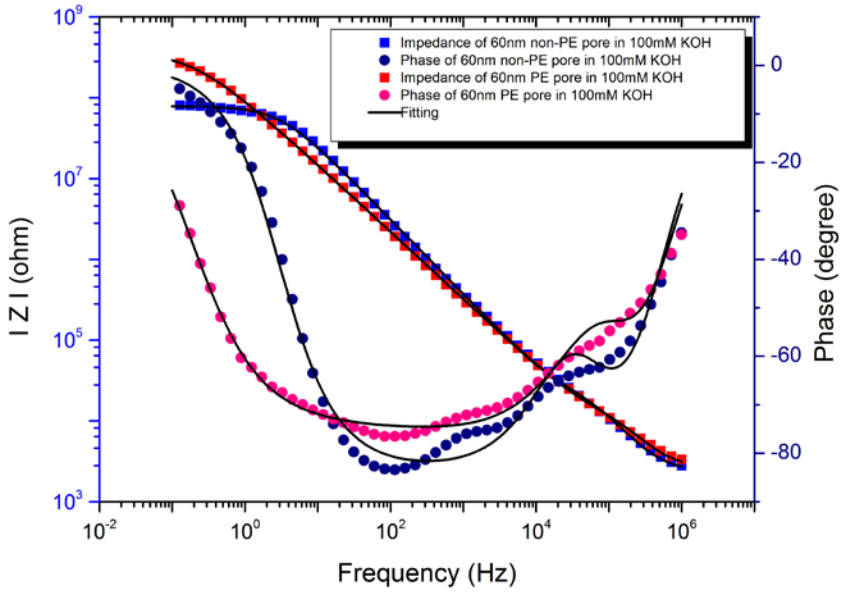


Figure 4. 7: Bode plots of EIS spectra measured in 100mM KOH ionic solution with PDMAEMA polyelectrolyte brushes coated 60 nm nanopore (red solid squares and pink solid circles) and non-polymer coated 60nm nanopore (blue solid squares and navy solid circles). The fitted curves were simulated from the equivalent circuit model and the corresponding values for each component are given in Table 4.1.

In the Nyquist plots of EIS measurement (Fig.4.8), the impedance data points were recorded with the sweep of frequency from high to low (left to right in the plot). The very left

coordinate points were the impedance measurement points at 1 MHz and the values are at around (2000 Ω, 2000 Ω) for both curves. The very right coordinate points were the impedance data at 0.1 Hz. The non-PE pore's curve shows a closed semi-ellipse in the first quadrant which was generally described by a simple RC parallel circuit. For the spectrum of the PE nanopore, the open circular arc indicated ion diffusion processes inside the polymer brushed coated on the nanopore sidewalls. The impedance values at 0.1 Hz were 264 MΩ for the real component and -122 MΩ for the imaginary component. The ion free moving path in the nanopore was quite restricted under high pH KOH solution and the chip behaved quite capacitively in DC field. A quantitative contribution of the difference is explained the equivalent circuit showing the components' values extracted from fitted curves shown in Table 4.1.

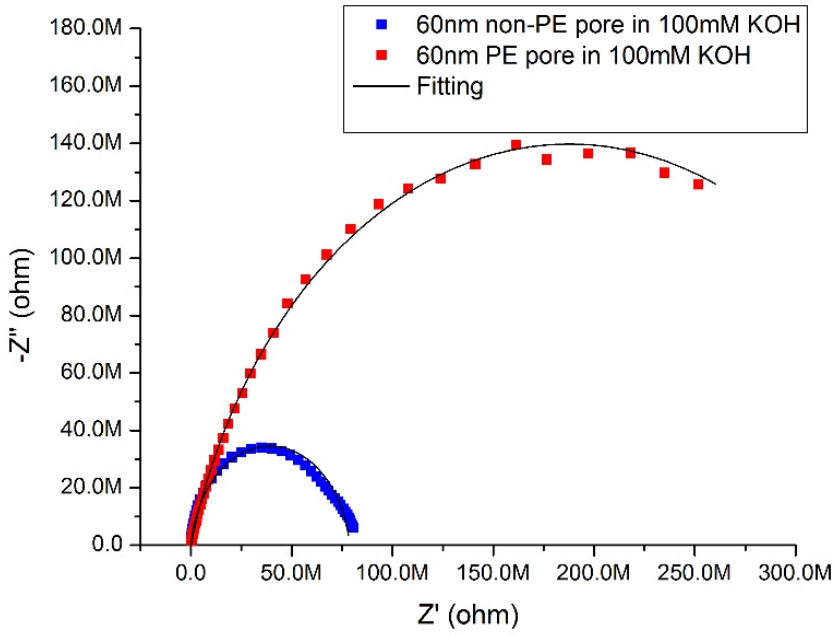


Figure 4. 8: Nyquist plots of EIS spectra measured in 100 mM KOH ionic solution with PDMAEMA polyelectrolyte brushes coated 60 nm nanopore (red solid squares) and non-polymer coated 60

nm nanopore (blue solid squares). The fitted curves were simulated from the equivalent circuit and the corresponding values for each component are given in Table 4.1.

The equivalent circuit was built as the model in left part of Figure 4.6 (B). The influence of electrode model on the right was very insignificant compared to the models of ionic solution and nanopore device. Manual adjustments on the values of R_{et}, Z_W and C_{dl} did not affect the fitting curves so that these three components were negligible in this case. The parasitic (stray) capacitor C_p was found out to be less than 5 pF for all electrolytes which was in accordance with the values of other nanopores.(Ervin, White et al. 2005, Uram, Ke et al. 2008) The solution resistance R_s was at around 2.5 kΩ for 100 mM KOH. The theoretical resistances of micropore and nanopore in 100mM KOH ionic solution are

$$R_{micro} = \frac{1}{\sigma}\frac{L}{\pi {R_{micro}}^2} = \frac{1}{15.3\frac{mS}{cm}} * \frac{450\mu m}{\pi(50\mu m)^2} = 37k\Omega$$

$$R_{nano} = \frac{1}{\sigma}\frac{L}{\pi {r_{nano}}^2} = \frac{1}{15.3\frac{mS}{cm}} * \frac{360nm}{\pi(30nm)^2} = 83.2M\Omega$$

where $\sigma_{100mM\ KOH} = 15.3\frac{mS}{cm}$, the dimensions of cylindrical micropore and nanopore are 450 μm in length, 50 μm in radius and 360 nm in length, 30 nm in radius, respectively. The fitted R_{acc} (34.8 kΩ) and R_{pore} (78.7 MΩ) values of non-PE pore turned out the same as the calculated values. The fitted value of R_{pore} of the PE-coated was 376 MΩ which is 4.7 times of resistance of the non-PE nanopore. The PE brushes on the nanopore sidewalls exhibited hydrophobic state in high pH electrolytes and substantially decreased the conductivity of the nanopore. The nanometer coating did not affect the resistance of the micropore which was kept at tens of kilo-ohm. The substrate capacitance was mainly contributed by the BOX layer and can be calculated as follow,

$$C_{sub} = \varepsilon_{SiO_2}\varepsilon_0\frac{A}{d} = 3.9 * 8.854 * 10^{-12}\frac{F}{m} * \frac{\pi(1.1mm)^2}{1\mu m} = 131pF$$

where A is the electrolyte contact area of the surface through the O-ring which is 2.2 mm in diameter, d is the thickness of the BOX which is 1 μm. Both fitted values of C_{sub} were very close to calculated one.

The CPE of the nanopore membrane turned out to be Q_{pore}=2.193 nFs^{n-1} while n=0.804 for the PE pore and Q_{pore}=0.727 nFs^{n-1} while n=0.895 for the non-PE pore. The presence of the

fractional exponent n showed existing of defects and inhomogeneity in the film. It caused deformations of the perfect semicircle curve in the Nyquist plot and a non-90° phase shift in the Bode plot. This was a consequence of the correlated forward backward jumps of the ionic charge carriers.(Abouzari, Berkemeier et al. 2009) In the regular nanopore, it was from the mobile ions moving through the defects and voids in the thermal SiO_2 layer. In the case of PE coated pore, the PE brushes layer brought more mobile ions, defects and voids which caused a smaller number of exponent n (0.804<0.895). The value of Q is not equivalent to capacitance value. The effective capacitance associated with CPE is expressed as (Hirschorn, Orazem et al. 2010)

$$C_{eff} = Q^{\frac{1}{n}} * R_f^{\frac{1-n}{n}} \tag{4.9}$$

where R_f is the resistance of the film.

For the regular pore with a layer of 60nm thick, 2.2mm in diameter area SiO_2 have a resistivity of $10^{17}\Omega$cm.

$$R_{f_{SiO_2}} = \rho \frac{l}{A} = 1.58 * 10^{13}\Omega$$

$$C_{eff_{SiO_2}} = Q^{\frac{1}{n}} * R_f^{\frac{1-n}{n}} = (0.727 * 10^{-9})^{\frac{1}{0.895}} * (1.58 * 10^{13})^{\frac{1-0.895}{0.895}} = 2.18nF$$

which is larger than the Q value 0.727.

For the PE coated pore, no good estimation could be made on the resistance of the polymer film. However, the total membrane resistance of SiO_2 + polymer was larger than one SiO_2 layer's. The C_{eff} for the polymer pore should be larger than

$$C_{eff_{SiO_2+polymer}} = Q^{\frac{1}{n}} * R_f^{\frac{1-n}{n}} = (2.193 * 10^{-9})^{\frac{1}{0.804}} * (1.58 * 10^{13})^{\frac{1-0.804}{0.804}} = 28nF$$

The effective capacitor for the nanopore membrane of the PE pore was at least 10 times larger than the one of non-PE pore in 100mM KOH ionic solution. This was due to the charges stored in the polymer layer.

Chip	Solution	Q_{pore} (nFs^{n-1})	n	R_{pore} (MΩ)	C_{sub} (pF)	R_{acc} (kΩ)	R_s (kΩ)	C_p (pF)
60 nm PE coated	100 mM KOH	2.193	0.804	376	107.2	16.01	2.609	1.215

nanopore	pH 12.98							
60 nm non-PE nanopore	100 mM KOH pH 12.98	0.727	0.895	78.7	138.5	34.8	2.409	1.987
60 nm PE coated nanopore	100 mM HCl pH 1.34	2.2	0.788	77.3	103.9	13.88	1.503	1
60 nm non-PE nanopore	100 mM HCl pH 1.34	0.733	0.892	54.4	137.8	33.6	1.422	4.59

Table 4.1: Equivalent circuit model fitting results of PE and non-PE nanopore EIS spectra in high molarity acid and alkali electrolytes.

Figure 4.9 and figure 4.10 show the Bode and Nyquist plots of measured and fitted spectra of PE and non-PE pore in 100 mM HCl. The extracted values of C_{sub}, R_{acc}, R_s and R_p were very close to KOH's as their conductivities were very close (26.4 $\frac{mS}{cm}$ for 100 mM HCl). The calculated resistance for non-PE pore is

$$R_{nano} = \frac{1}{\sigma}\frac{L}{\pi {r_{nano}}^2} = \frac{1}{26.4\frac{mS}{cm}} * \frac{360nm}{\pi(30nm)^2} = 48.2M\Omega$$

which was in accord with the measured value (54.5 MΩ). The nanopore resistance for the PE pore (77.3 MΩ) was not much larger than the non-PE's, even if most of the room for the electrolyte inside the nanopore was occupied by the PE brushes. In the plots, the impedance curves are close and both of the Nyquist curves tend to be close. In this case, the backbone of the polymer brushes which was tertiary amine groups got protonated in acid aqueous environment. Extra hydrogen ions were attached in the brushes and diffused along the potential field so that the conductivity of the polymer was enhanced to the same level as the electrolytes.

The effective capacitances from the given Q_{pore} are

$$C_{eff_{SiO_2}} = Q^{\frac{1}{n}} * R_f^{\frac{1-n}{n}} = (0.733 * 10^{-9})^{\frac{1}{0.892}} * (1.58 * 10^{13})^{\frac{1-0.892}{0.892}} = 2.27nF$$

$$C_{eff_{SiO_2+polymer}} = Q^{\frac{1}{n}} * R_f^{\frac{1-n}{n}} > (2.2 * 10^{-9})^{\frac{1}{0.788}} * (1.58 * 10^{13})^{\frac{1-0.788}{0.788}} = 36.6nF$$

The extra hydrogen ions brought into the polymer brushes also contributed to the increase of the capacitance level for the nanopore membrane part.

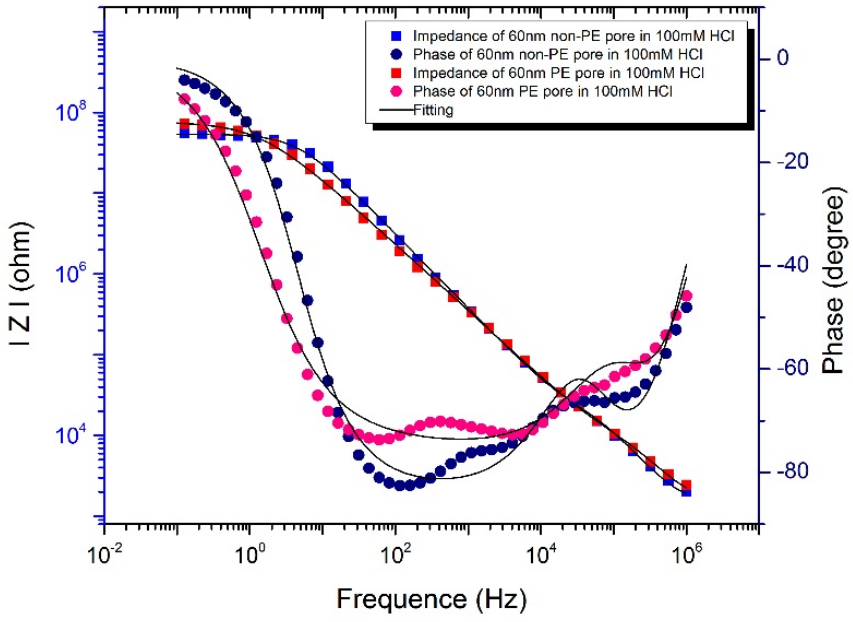


Figure 4. 9: Bode plots of EIS spectra measured in 100mM HCl ionic solution with PDMAEMA polyelectrolyte brushes coated 60 nm nanopore (red solid squares and pink solid circles) and non-polymer coated 60nm nanopore (blue solid squares and navy solid circles). The fitted curves were simulated from the equivalent circuit model and the corresponding values for each component are given in Table 4.1.

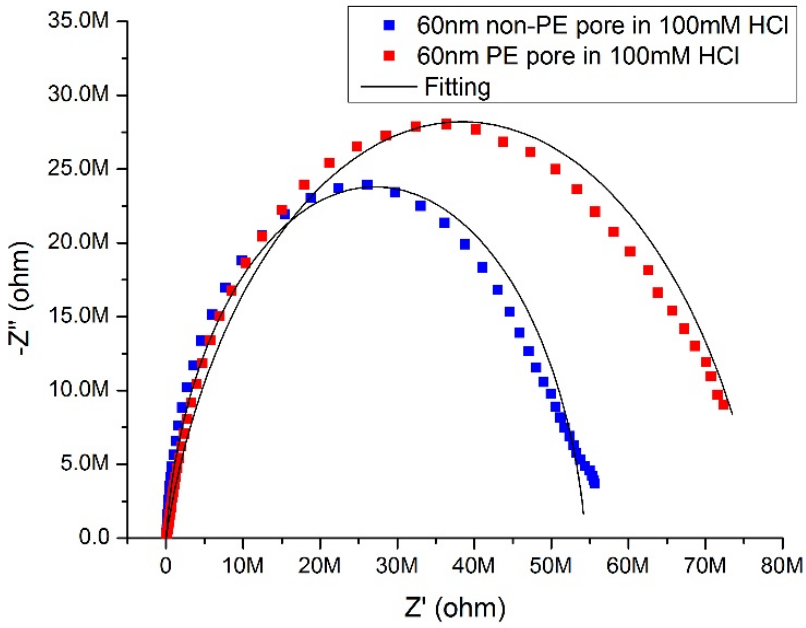


Figure 4. 10: Nyquist plots of EIS spectra measured in 100mM HCl ionic solution with PDMAEMA polyelectrolyte brushes coated 60nm nanopore (red solid squares) and non-polymer coated 60 nm nanopore (blue solid squares). The fitted curves were simulated from the equivalent circuit model and the corresponding values for each component are given in Table 4.1.

In summary, the fitting curves matched well with EIS spectra of PE and non-PE pore in both 100 mM KOH and 100 mM HCl ionic solutions. The double layer effect was not considered in 100 mM electrolytes. The extracted electrical components were in very good agreement with the calculated resistance and capacitance for each part in the experimental setup and proved that the constructed equivalent circuit at the beginning correctly illustrated the physical model of the chip. The PDMAEMA polyelectrolyte brushes got protonated in the 100mM HCl ionic solution and enhanced the conductance of nanopore to the same level as the non-PE pore's. A 1:5 ratio of PE coated nanopore resistance built a good on and off switch in acid and alkali solutions. A better sensitivity could be reached in the future with a modified PE growth process.

4.3.3 EIS Measurement on PE Coated Nanopore in Low Molarity Electrolytes with Gate Voltage Modulation

The PE and non-PE 60 nm pores were measured in low molarity acid and alkali electrolytes where the electric double layer started to play a role. From the Bode plots and Nyquist plots in Figure 4.11 & 4.12, the conductance of PE nanopore in KOH and HCl was much larger than the conductance of non-PE nanopore. This showed that the amount of mobile ions which polymer brushes brought into the nanopore was more than the counter-ions in the non-PE nanopore. To give a quantized comparison, the resistance of the nanopore part was extracted from the fitting data to be 4.7 GΩ and 2.9 GΩ for the regular nanopore in 0.1 mM KOH and HCl, 1.379 GΩ for the PE pore in KOH and 144 MΩ in 0.1 mM HCl, respectively. For the regular nanopore, the higher conductance in 0.1 mM HCl solution is because of the higher concentration of Hydrogen ions (counter-ions) induced to the negatively charged surface and higher mobility of Hydrogen ions as described in the previous Chapter. In the PE coated nanopore, protonated polymer brushes drastically increased the conductance of the nanopore. This showed that, in the same acid environment, the number of Hydrogen ions adsorbed into the polymer chain and original in the polymer was much higher than the number of hydrogen ions brought into the double layer by the zeta potential. . The conductance of the PE coated pore in 0.1 mM HCl ionic solution was even greater than the one of a regular nanopore in 10 mM HCl ionic solution. In 0.1 mM KOH ionic solution, even though the polymer chain was deprotonated, the original charges of polymer still made the conductance higher than the conductance of a regular pore in 0.1 mM KOH.

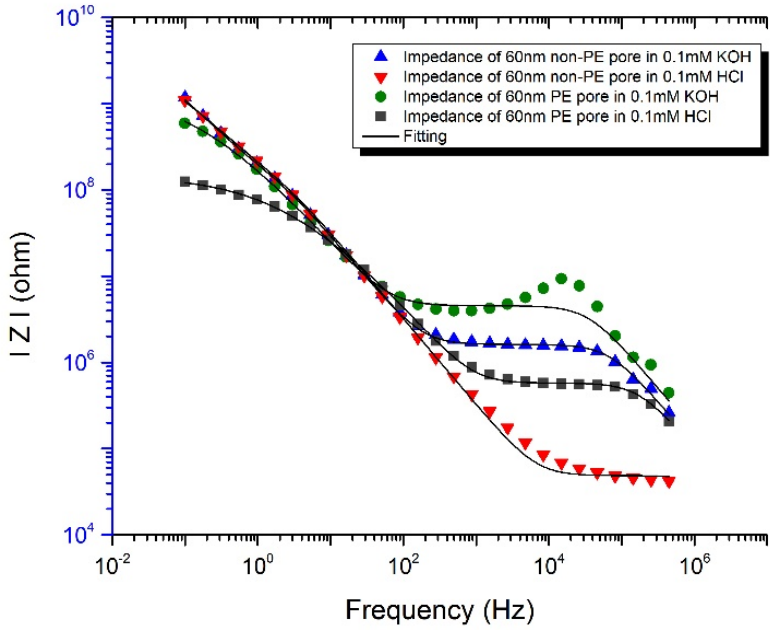


Figure 4. 11: Impedance plots of PE and non-PE 60nm pore in 0.1mM HCl and 0.1mM KOH ionic solutions, respectively. The fitted curves were simulated from the equivalent circuit and the corresponding values for each component are given in Table 4.2.

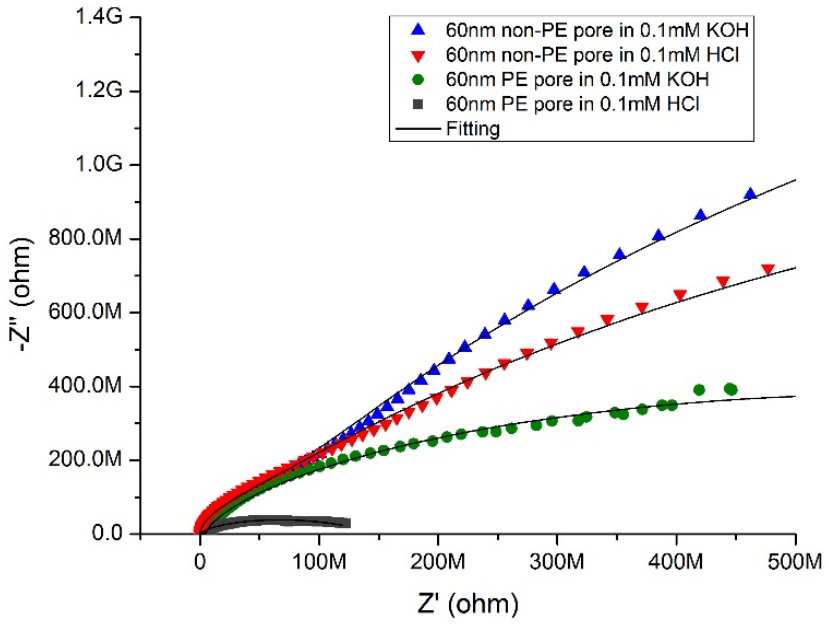


Figure 4. 12: Nyquist plots of PE and non-PE coated 60 nm nanopore chip measured in 0.1 mM HCl and 0.1 mM KOH ionic solutions, respectively. The fitted curves were simulated from the equivalent circuit and the corresponding values for each component are given in Table 4.2.

C_p was kept the values at several picoFarad range while the solution resistance R_s increased to Mega ohm for the low molarity electrolytes. The calculated values for the solution resistance in the 100 µm aperture (R_{acc}) is about 50 MΩ. In the PE coated aperture, the higher conductivity of polymer brushes rendered a smaller R_{acc} values. The deviation on R_{acc} (>200 MΩ) of the non-PE chip was affected by the Gigaohm resistance of the nanopore. Because of the involvement of the double layer, the substrate capacitance (C_{sub}) increased to 500 pF and the exponent of the nanopore CPE decreased to 0.8 from 0.9 for the non-PE aperture that consequently enhanced the value of effective capacitance of the CPE.

Chip	Solution	Bias (V)	Q_{pore} (nFs^{n-1})	n	R_{pore} (MΩ)	C_{sub} (pF)	R_{acc} (MΩ)	R_s (MΩ)	C_p (pF)
60nm non-PE nanopore	0.1 mM KOH pH 9.57	0	0.860	0.803	4700	538	260	1.614	1.419
60nm PE coated nanopore	0.1 mM KOH pH 9.57	0	1.379	0.537	1379	540	3.61	4.54	1
60nm non-PE nanopore	0.1 mM HCl pH 4.71	0	0.884	0.733	2900	492	231	0.048	1.733
60nm PE coated nanopore	0.1 mM HCl pH 4.71	0	2.805	0.521	144.1	325	5.61	0.575	1.575
60nm PE coated nanopore	0.1 mM HCl pH 4.71	+4	6.875	0.573	282.3	711	2.56	0.539	1.352
60nm PE coated nanopore	0.1 mM HCl pH 4.71	-4	2.101	0.623	126.8	716	9.09	0.531	1.264

Table 4.2: Equivalent circuit fitting results of PE and non-PE nanopore EIS spectra in 0.1 mM KOH and 0.1 mM HCl. Substrate bias was appllied on the PE chip measured with 0.1 mM HCl.

Substrate bias was applied to the front side of the PE coated chip using a Keithley 236 source measure unit using the same setup as shown in Figures 3.6&3.7. The DC leakage current was not taken into consideration since the EIS measurement unit filtered out the DC signal. KOH ionic solution is not used in the measurement due to the interaction between Potassium ions and the Silicon dioxide surface under gate bias. The bias was not applied in the High molarity measurement because it did not affect the ion distribution in a short electric double layer. Figure 4.13 shows the Nyquist plots of impedance EIS measurement of the PE coated pore in 0.1mM HCl with -4V, 0V and +4V gate bias. The nanopore resistance under V_g=+4 V bias increased by a factor of 2 (282.3MΩ) compared to the resistance with no bias (144 MΩ) and the resistance under -4 V bias (126.9 MΩ) was slightly smaller than the one without bias. When positive bias was applied, it repelled the protonated Hydrogen ions in the polymer brushes. Hydrogen ions were the dominant mobile ions which contributed to the conductance of the aperture in the HCl electrolytes. About half of the Hydrogen ions inside the nanopore were depleted to the outside of the aperture so that the conductance was decreased by a factor of 2. With negative bias, the conductance

only increased slightly because the amount of protonated Hydrogen ions was quite saturated in the polymer brushes inside the aperture compared to the concentration of Hydrogen ions in the regular nanopore where only the counter-ions dominated. The negative bias could not absorb more Hydrogen ions into the aperture.

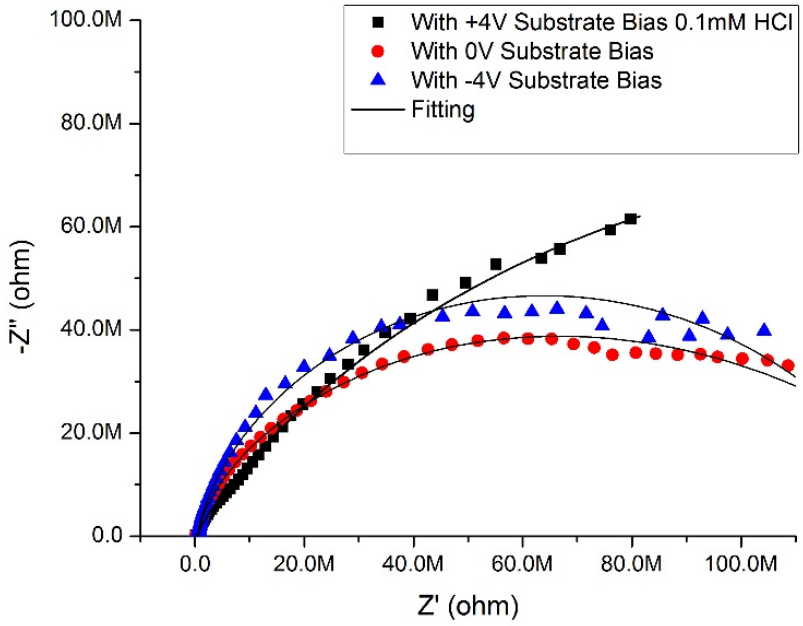


Figure 4. 13: Nyquist plots of PE 60nm pore measured in 0.1 mM HCl with -4 V (blue solid triangles), 0 V (red solid circles) and +4 V (deep gray squares) substrate bias respectively. The fitted curves were simulated from the equivalent circuit and the corresponding values for each component are given in Table 4.2.

4.4 Summary

In this Chapter, the SOI 60 nm cylindrical single nanopore was coated with pH sensitive polyelectrolyte brushes for the conductance measurement. A layer of 25 nm thick PDMAEMA brushes was uniformly grown on the surface of the chip as well as on the sidewalls of the nanopore using the SI-ATRP method. Electrochemical Impedance Spectroscopy (EIS) was

utilized to measure the chip AC impedance response in both HCl and KOH electrolytes with different molarities. An equivalent circuit model of the nanopore was built to extract the resistance and capacitance value for each part of the nanopore by fitting Bode plots and Nyquist plots spectra. The polymer got protonated in HCl ionic solution so that the conductance of a PE coated nanopore in HCl eletrolytes was much higher than the conductance in KOH ionic solution where the brushed showed a hydrophobic neutral state with the same molarity and formed an on/off switch. Ratios of 5:1 and 9.5:1 on PE nanopore conductance were observed in 100 mM HCl/KOH and 0.1 mM HCl/KOH ionic solutions, respectively. When positive gate bias was applied on the substrate, the PE nanopore conductance in 0.1 mM HCl decreased by a factor of 2 because of the repulsion of Hydrogen ions inside of the channel. When negative bias was applied on the substrate, the PE nanopore conductance in 0.1 mM HCl did not increase remarkably since the amount of Hydrogen ions from the charged polyelectrolyte and double layer in the channel already got saturated inside the nanopore channel. This result was different from the measurement of a non-PE coated pore whose conductance increased by a factor of 2-3 under negative bias from previous Chapter due to the attraction of extra Hydrogen ions into the channel.

5. CONCLUSION

The rectification of ionic current through surface modified nanopores with field effect modulation has promising applications in the form of biomolecule filtering and slowing down DNA sequencing. In this doctoral study, this rectification of ionic current through silicon-on-insulator (SOI) cylindrical single nanopore was achieved by integration of the factors such as gate bias, organic and inorganic surface modifications.

The SOI nanopores were fabricated using standard CMOS processes which have benefits of high throughput. The silicon nanopore membrane provided a conductive contact for the access of gate voltage bias and it was electrically insulated by a thermal SiO_2 layer. To avoid trapping air bubble in the cavity in the local vicinity of the silicon nanopore during electrolyte filling, nanopore patterning using Al_2O_3 hard mask was studied. The excellent selectivity of Al_2O_3 over both Si and SiO_2 in both RIE and ICP RIE processes enabled fabrication of vertical nanofluidic channels through both the Si device and BOX layer in a controlled method.

BCl_3 plasma in ICP RIE under low chamber pressure was proven to be the optimal approach for patterning sub-100 nm nanopores in the Al_2O_3 hard mask layer. BCl_3 plasma showed the highest etch rate on Al_2O_3, the highest selectivity of Al_2O_3 over PMMA compared to Cl_2, Ar, Ar/BCl_3 mixtures and anisotropic pattern transfer. Using the Al_2O_3 hard mask, nanopores exhibiting smooth vertical sidewalls were etched in the silicon device layer using a Cl_2 plasma in an ICP-RIE tool. Another anisotropic silicon etching with higher selectivity over Al_2O_3 hard mask can be attempted using SF_6-O_2 mixture. A 40:1 selectivity of SiO_2 over Al_2O_3 in the RIE tool with CHF_3: Ar plasma made it possible to continuously etch the BOX layer using the remaining alumina mask. The appearance of undercut in Si layer during SiO_2 etching addressed that improvements can be achieved by using H_2 + Fluorine-based plasma chemistry with good protection on Si sidewalls using passivation layers.

Ionic current was measured in negatively charged SiO_2 nanopore with HCl electrolyte solutions and in positively charged Al_2O_3 nanopore with both HCl and KCl electrolyte solutions under field effect modulation. The gate bias had an influence on the ionic current at low concentration (10 μM) of the ionic solution after the leakage current from the device top surface

and BOX layer was subtracted. In 10 μM HCl, the ionic current increased with negative bias irrespective of the surface charge type. The H^+ ions were attracted by the negative bias and contributed to the ionic current because of a higher mobility compared to that of K^+ and Cl^- ions. Other than this case, the I_{DS} trace stayed flat or slightly decreased with the change of bias in both SiO_2 and Al_2O_3 coated nanopores, which demonstrated the depletion of H^+ ions in the channel and the adsorption of heavier K^+ and Cl^- ions in the stagnant dynamic stern layer by the electrostatic force due to the gate bias.

The ionic rectification was further studied in 60 nm diameter nanopores coated with polyelectrolyte brushes under field effect modulation. Surface-initiated atom transfer radical polymerization generated a uniform layer of pH sensitive PDMAEMA polyelectrolyte brushes on the surface of the nanopore device. In strong acid ionic solutions like 100mM HCl, the brushes got protonated and caused a remarkable increase in the ionic conductance through the nanopore. The electrochemical impedance spectroscopy spectra were used to build an equivalent circuit model which was able to explain the electrical changes in all the parts of the PE and non-PE coated nanopores in aqueous solutions. A rectification ratio of 5:1 on PE nanopore ionic current was observed in 100 mM HCl and 100 mM KOH and it can be improved by optimizing the polymerization method. The gate bias did not affect PE coated nanopores in high molarity ionic electrolytes.

In low molarity HCl and KOH (100 μM), it showed 9.5:1 ionic rectification ratio through PE coated nanopore. In 100 μM HCl, the conductance through PE coated nanopore increase a factor of 20 compared to the conductance through non-PE coated nanopore due to the protonated H^+ ions and original charge of PE brushes. When a positive bias was applied on the substrate, the PE nanopore conductance in 100 μM HCl decreased by a factor of 2 because of the repulsion of H^+ ions inside of the channel. And different from the non-PE coated nanopore, the conductance through PE coated nanopore just slightly increased under negative bias because of the saturation of the H^+ ions inside the channel.

5.1 Future Work

The ionic transport through dual-doped silicon membrane nanopore is the next step to be studied. Dr. Gracheva's simulation results show good current rectification and filtering properties on P-N Si membrane nanopore.(Gracheva, Vidal et al. 2007, Nikolaev, Gracheva 2011) Dual layer doping can be achieved by ion-implantation. On the P-Si side of the membrane, the positive charges in the silicon generate a negatively charged depletion layer near the membrane. These negative charges combining with the original negative surface charges in the oxide layer attract positive ions in the electrolytes accumulating at the P-Si side of the nanopore channel. The positive ions screen the electrostatic potential and make themselves hard to be controlled by the gate bias V_p. On the N-Si side of the membrane, the screen effect by the negatively charged ions is not strong enough that the bias V_n can control the ions distribution in the N-Si side of the nanopore channel. When V_n =1 V, negatively charged ions accumulate in the left side of the channel as shown in Fig 6.1A and Fig 6.1B. The positive external transmembrane bias (Left to right) is not able to drive the ions moving inside channel against the built-in field and the ionic current is close to zero. The negative external transmembrane voltage is not counteracted by any internal ionic potential inside the nanochannel and it produces a proportional negative ionic current. This asymmetric I-V behavior causes a rectification effect. However, when V_n =-1 V, both sides of channel are filled with positive ions and the I-V curve shows a linear relationship.

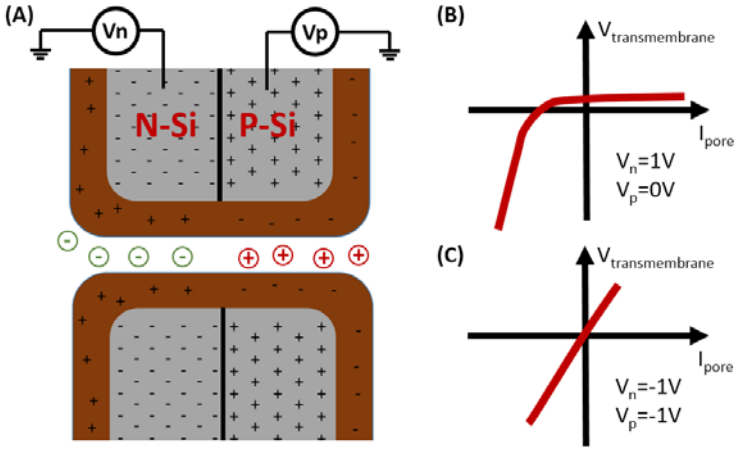


Figure 5. 1 (A) Illustration of half p-type doped half n-type doped Si nanopore membrane isolated by SiO_2 layer. Two independent bias voltages are added on the P-Si layer and N-Si layer, respectively. (B) Plot of IV curve which shows ionic current rectification under positive transmembrane potential. (C) Plot of IV curve which shows ionic current rectification under negative transmembrane potential.

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