Methodical Design Approaches to Multiple Node Collection Robustness for Flip-Flop Soft Error Mitigation

by

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ABSTRACT

The space environment comprises cosmic ray particles, heavy ions and high energy electrons and protons. Microelectronic circuits used in space applications such as satellites and space stations are prone to upsets induced by these particles. With transistor dimensions shrinking due to continued scaling, terrestrial integrated circuits are also increasingly susceptible to radiation upsets. Hence radiation hardening is a requirement for microelectronic circuits used in both space and terrestrial applications.

This work begins by exploring the different radiation hardened flip-flops that have been proposed in the literature and classifies them based on the different hardening techniques.

A reduced power delay element for the temporal hardening of sequential digital circuits is presented. The delay element single event transient tolerance is demonstrated by simulations using it in a radiation hardened by design master slave flip-flop (FF). Using the proposed delay element saves up to 25% total FF power at 50% activity factor. The delay element is used in the implementation of an 8-bit, 8051 designed in the TSMC 130 nm bulk CMOS.

A single impinging ionizing radiation particle is increasingly likely to upset multiple circuit nodes and produce logic transients that contribute to the soft error rate in most modern scaled process technologies. The design of flip-flops is made more difficult with increasing multi-node charge collection, which requires that charge storage and other sensitive nodes be separated so that one impinging radiation particle does not affect redundant nodes simultaneously. We describe a correct-by-construction design methodology to determine a-priori which hardened FF nodes must be separated, as well

as a general interleaving scheme to achieve this separation. We apply the methodology to radiation hardened flip-flops and demonstrate optimal circuit physical organization for protection against multi-node charge collection.

Finally, the methodology is utilized to provide critical node separation for a new hardened flip-flop design that reduces the power and area by 31% and 35% respectively compared to a temporal FF with similar hardness. The hardness is verified and compared to other published designs via the proposed systematic simulation approach that comprehends multiple node charge collection and tests resiliency to upsets at all internal and input nodes. Comparison of the hardness, as measured by estimated upset cross-section, is made to other published designs. Additionally, the importance of specific circuit design aspects to achieving hardness is shown.

DEDICATION

To my parents Shambhulingaiah Madaiah and Sujatha Gubbiyappa and my brother Yogesh Shambhulingaiah, for their love, encouragement and support.

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TABLE OF CONTENTS

Page

CHAPTER Page

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

The effect of soft errors in microelectronic devices was first studied in early 1970s [1]. It was predicted that cosmic rays would start upsetting the microcircuits due to heavy ion interactions when the feature sizes became small enough. Through 1970 and early 1980s the physics of these phenomena was examined. May and Woods [2] determined that the errors in the microcircuits were caused by alpha particle emission due to the radioactive decay of uranium and thorium present in the package material. They referred to these errors as "soft errors" and this was the first account of radiation induced upsets on terrestrial micro devices. It was also discovered that the upsets were also caused by nuclear reaction generated neutrons and protons [3].

1.1 Radiation Environment

In 1980s research on single event effects (SEE) increased. Numerous methods were developed to harden the ICs against SEEs. Much of the research work was focused on errors observed in DRAMs, SRAMs, nonvolatile memories, latches and registers. In the 1990's, it was discovered that natural boron and isotope boron-10 present in boro-phospho-silicate-glass (BPSG) used in the manufacturing process reacted with low energy neutrons present in the atmosphere to produce upsets in ICs [4] subsequently, BPSG was removed from most processes.

1.1.1 Trapped Particles

Charged particles that come into contact with the Earth's magnetic field can become trapped in the near-Earth environment. These particles include electrons, protons, and

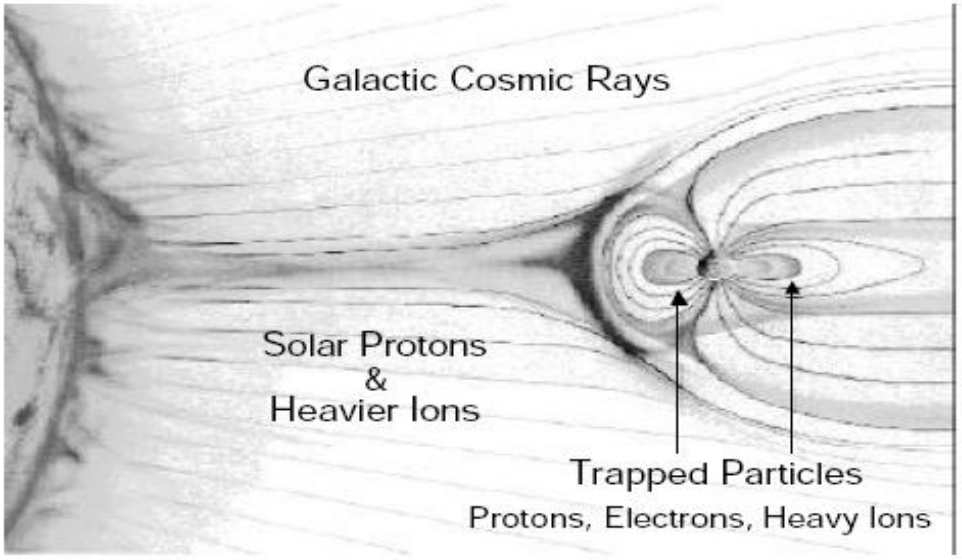


Fig. 1.1. Particles in the space radiation environment [5].

heavy ions. Fig 1.1 shows the space radiation environment. Electrons are very important components of the space environment because they inflict damage on spacecraft through spacecraft charging effects [6][7].

The trapped particle belts (Van Allen belts) consist of two regions of trapped particles, an inner belt centered at about 1.5 Earth radii, and an outer belt of particles at about 5 Earth radii, separated by a region of reduced particle flux.

Sources of radiation include the solar wind and transient solar events, cosmic ray particles from interplanetary space, and reaction products from cosmic ray collisions with the Earth's atmosphere [8].

1.1.1.1 Protons

Energetic protons exist in the near-Earth environment and are one of the most prominent sources of orbital SEE. They range in energy from tens of keV to hundreds of MeV [8]. Protons with these energies are easily able to penetrate shielding and impinge

on electronics within spacecraft. The altitude at which proton flux peaks depends on the proton energy, with high energy (>30 MeV) protons being cut off by around 3.5 Earth radii, but lower energy protons existing throughout the slot region.

1.1.1.2 Heavy Ions

The heavy ions from space are trapped by the Earth's magnetic field. The origin of these particles are cosmic rays, which are interstellar particles that drift into the solar system, become ionized by the solar wind and accelerated to 10's of MeV/nucleon, and are subsequently trapped by the magnetosphere. Recent studies have shown high heavy ion (e.g. nickel and iodine) fluencies above 10^6 particles/cm^2 can damage electronic components through ionization processes [8].

1.1.2 Transient Particles

In this section, we classify all particles in the near-Earth space environment that are not trapped in the magnetosphere. This includes particles introduced into the environment by solar events such as flares and coronal mass ejections (CMEs), as well as energetic ions incident from interstellar space.

1.1.2.1 Solar Event Protons and Heavy Ions

Solar events can be broadly classified as being either gradual or impulsive. The gradual events produce particle flux that decays slowly over several hours or even days, and have been correlated to CMEs. These events are proton-rich and can produce high-energy (>30 MeV) proton fluences higher than 10^9 protons/cm^2 accumulated over a few days. Gradual events are responsible for the majority of large proton fluence events, and occur at a frequency of about 10 per year during solar maximum conditions.

Impulsive events are of much shorter duration (hours at most), and are marked by increased fluences of heavy ions and low energy electrons. Impulsive events produce heavy ion fluences that can be orders of magnitude above the galactic cosmic ray radiation. These heavy ions have energies ranging from tens of MeV/nucleon to hundreds of GeV/nucleon [8][9].

1.1.2.2 Galactic Cosmic Rays

Solar event particles are observed only for a short time following an event, although following a large event increased levels of trapped particles are observed and in some cases can produce new trapped particle belts. In contrast, galactic cosmic rays (GCR) form a background component of radiation that shows a slow cyclical variation with solar activity. GCRs are composed of very highly energetic protons and heavy ions that come from outside the solar system.

Protons comprise about 83% of the GCR flux, He nuclei (alpha particles) account for 13%, 3% are electrons, and the remaining 1% are heavier nuclei [10]. Even though they are not very abundant, heavy ions are very important to SEE because they deposit the most energy per unit path length, as discussed in later sections. Beyond Fe, the heavy ion flux drops dramatically. This is important, because the energy deposited by an ion per unit path length depends on its atomic number. Ions heavier than Fe are more ionizing, but are much less abundant.

GCRs that come into contact with the near-Earth environment encounter the Earth's geomagnetic field. Because they are so energetic (tens of MeV/nucleon to hundreds of GeV/nucleon), they do not become trapped and are not significantly attenuated by spacecraft shielding. GCRs that hit the atmosphere form a cascade of

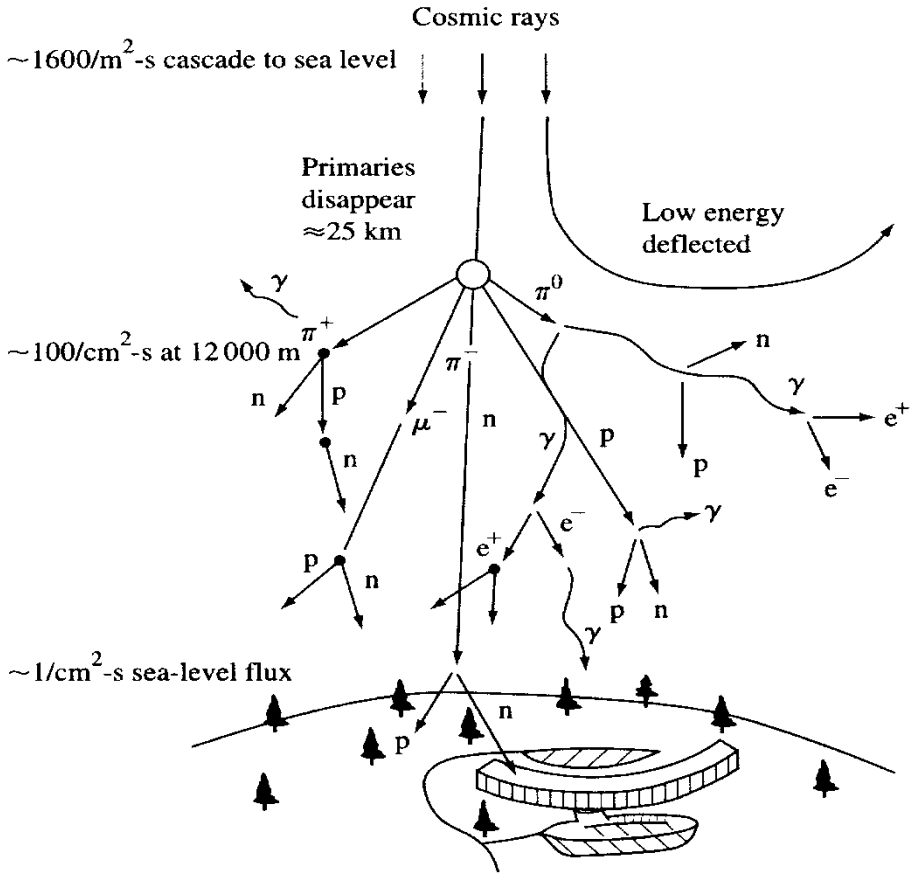


Fig. 1.2. Illustration of the terrestrial cosmic ray shower caused by the interaction of galactic cosmic rays with the Earth's atmosphere [12].

secondary particles.

1.1.3 Secondary Particles

Secondary particles are produced when GCRs strike the Earth's atmosphere and produce a shower of particles in the atmospheric environment. A radiation environment also exists in the Earth's atmosphere, and although less harsh than the space environment, it can also produce SEE.

As highly energetic cosmic rays enter the upper atmosphere they interact with oxygen and nitrogen in the atmosphere and produce a shower of daughter products

[11][12]. Some of the daughter products can reach all the way through the atmosphere to ground level, equivalent to passing through more than 13 feet of concrete [11]. A diagram of a cosmic ray shower is shown in Fig. 1.2. The daughter products primarily responsible for causing upsets in high-altitude and terrestrial electronics are neutrons and protons [12]. The fluxes of neutrons and protons have similar characteristics with respect to energy and altitude variation, with both populations extending to energies greater than 1 GeV.

1.1.4 Radiation Effects in Devices

When a component is exposed to radiation, the radiation transfers some of its energy to the component materials, changing the localized material properties. This can affect component functionality, with the end result depending on the type of radiation, where the energy deposition occurred, and the type of component.

1.1.5 Single Event Effects

SEEs are caused by the impact of either heavy ions or energetic protons and neutrons that occur naturally in space or the atmosphere, on sensitive areas in microcircuits. These particles deposit ionizing energy into the circuit that cause a soft (i.e., a non-permanent) error or in some cases permanent damage to the circuit. In this section we look at the release of mobile carriers along the path of an incident particle and the collection of these carriers.

1.1.5.1 Charge Deposition

As ionizing radiation passes through a target material electrons and holes are released along the path of ionizing particles. There are two primary methods by which

carriers are released, direct ionization by the incident particle, and ionization by secondary particles created by nuclear reactions between the incident particle and the target material.

When an energetic particle passes through a semiconductor material it frees charged carriers along its path as it loses energy. When all of its energy is lost, the particle comes to rest in the semiconductor, having traveled a total path length referred to as the particle's range. The term linear energy transfer (LET) or $\mathrm{dE/dx}$ is used to describe the energy loss per unit path length of a particle as it passes through a material. LET has the units of $\mathrm{MeV-cm^2/mg}$, because the energy loss per unit path length (in MeV/cm) is normalized by the density of the target material (in $\mathrm{mg/cm^3}$) as given by

$$LET = \frac{1}{\rho}\frac{dE}{dx} \quad (MeV - cm^2/mg), \tag{1}$$

where ρ is the material density (2.42 g/cm^3 for silicon). The charge deposited through direct ionization sufficient to cause an upset depends on the individual device and circuit that has been struck as well as the strike location and trajectory. Direct ionization is the primary charge deposition mechanism for upsets caused by heavy ions, where we define a heavy ion as any ion with atomic number $Z \geq 2$ (i.e., He and above, i.e., particles other than protons, electrons, neutrons, or pions).

Direct ionization by light particles usually does not produce a high enough charge density to cause upsets. Protons and neutrons can both produce significant upset rates due to indirect mechanisms. As a high-energy proton or neutron enters the semiconductor lattice it may undergo an inelastic collision with a target nucleus. This may result in the emission of alpha (α) or gamma (γ) particles and a recoiling daughter nucleus (e.g., Si emits α -particle and a recoiling Mg nucleus) or a reaction, in which the target nucleus is

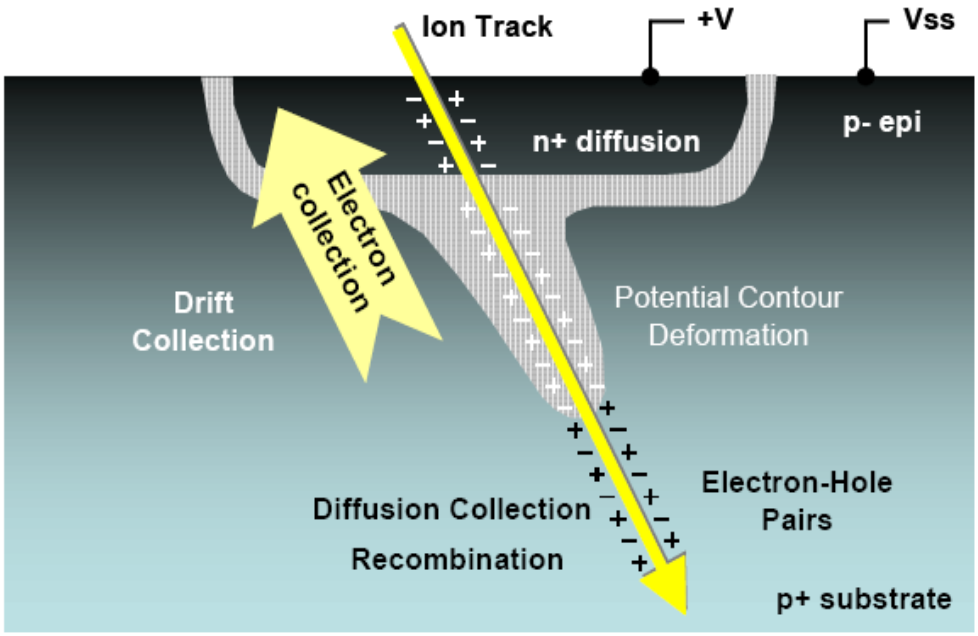


Fig. 1.3. A schematic of a reverse-biased n+/p junction struck by an ion [13].

broken into two fragments (e.g., Si breaks into C and O ions), each of which can recoil. Any of these reaction products can now deposit energy along their paths by direct ionization. Because these particles are much heavier than the original proton or neutron, they can deposit high charge densities as they travel and therefore may cause an SEU.

1.1.5.2 Charge Collection

The most sensitive semiconductor device structure is the reverse-biased junction. The collected charge (Q_{coll}) depends on the type of ion, its trajectory, and its energy over the path through or near the junction. A reverse biased n+/p junction with a positive voltage on the n+ node is shown in Fig. 1.3. At the onset of an ionizing radiation event, a cylindrical track of electron-hole pairs with very high carrier concentration is formed along the path of the energetic ion's passage. When the resultant ionization track traverses or comes close to the depletion region, carriers are rapidly collected by the electric field creating a large current/voltage transient at that node.

As the ionizing radiation passes through the substrate, the depletion region is extended into a funnel deeper into the substrate [14]. This funnel greatly enhances the efficiency of the drift collection. The depth of the funnel is a function of substrate doping. This "prompt" collection phase is completed within a nanosecond and is followed by a phase where diffusion begins to dominate the collection process. Additional charge is collected as electrons diffuse into the depletion region on a longer time scale (nanoseconds) until all excess carriers have been collected, recombined, or diffused away from the junction area. The diffusion process is much slower and typically the total charge collected from diffusion is significantly less than that collected initially by prompt collection in the case of advanced technologies.

The magnitude of the collected charge (Q_{coll}) depends on the size of the device, biasing of the various circuit nodes, substrate structure, device doping, the type of ion, its energy, its trajectory, the initial position of the event within the device, and the state of the device. The device's sensitivity to this excess charge is defined primarily by the node capacitance (C_{node}), operating voltage (V_{node}), and the strength of feedback transistors, all defining the critical charge (Q_{crit}) required to trigger a change in the data state [15].

For simple isolated junctions, a soft error will be induced when a radiation event occurs close enough to a sensitive node such that $Q_{coll} > Q_{crit}$ and Q_{crit} has the form

$$Q_{crit} = C_{node} * V_{node}$$

Conversely, if the event results in a $Q_{coll} < Q_{crit}$ then the circuit will survive the event and no soft error will occur.

1.1.6 Destructive and Non-Destructive SEEs

Single-event effects are broadly characterized as either non-destructive or

TABLE I

VARIOUS SUB CATEGORIES OF SINGLE EVENT EFFECTS (SEE) [20]

Acronym	Result	Effect Name	Description
SEU	Non-Destructive	Single Event Upset	Switching of a digital logic state
SET	Non-Destructive	Single Event Transient	Voltage transient at circuit node
SEMBU	Non-Destructive	Single Event Multiple Bit Upset	Switching logic states of adjacent cells
SEB	Destructive	Single Event Burnout	High current condition in BJTs or Power MOSFETs
SEGR	Destructive	Single Event Gate Rupture	Destruction of Insulated Gate in power MOSFET
SEL	Destructive	Single Event Latchup	High current destruction of a n-p-n-p structure

destructive SEE. SEEs that cause no observable physical effect or a temporary disruption of circuit operation (known as soft errors) are Non-Destructive. SEEs which cause permanent damage to the device or integrated circuit (known as hard errors) are Destructive. Table I lists the various sub categories of SEEs. Any of these effects can cause soft errors in space applications. A brief description of each kind of SEE is given below

1) Single Event Transients (SET)

The situation in which a single event charge collection happens at a combinational circuit node generating a temporary voltage glitch is called a single event transient as shown in Fig. 1.4(a). The SET generated depends on the circuit node logic state and diffusion type. The SET can propagate through combinatorial logic and if captured by a sequential circuit, can upset the IC architectural state.

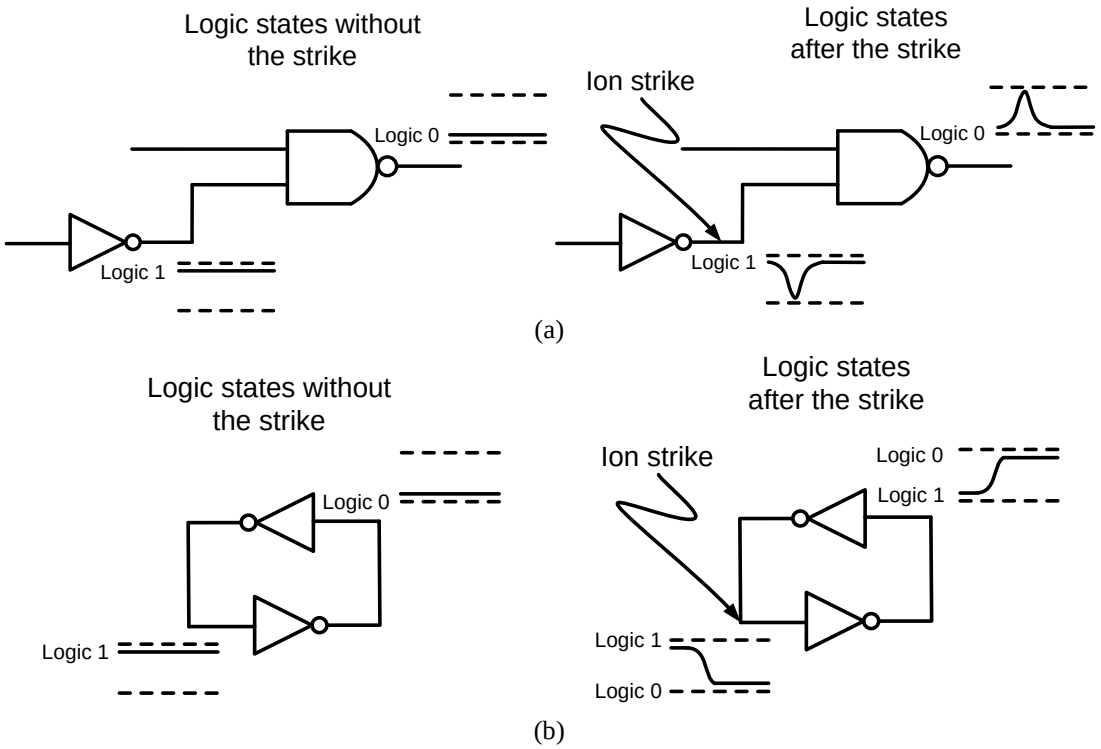


Fig. 1.4. Ionizing radiation induced charge collection at (a) a combinational circuit generating SET and (b) on a latch circuit causing a SEU. Either or both may upset IC architectural state in flip-flops.

2) Single Event Upsets (SEU)

A single event upset is charge collection at a sequential circuit storage node upsetting the logic state directly as shown in Fig 1.4(b). This can be caused either by the direct ionization from a traversing particle or by the ionization produced by charged particles and recoiling nuclei emitted from a nuclear reaction induced near the microcircuit element.

3) Single Event Multiple Bit Upsets (SEMBU)

SEMBUs occur when there is multiple node charge collection (MNCC) across multiple circuit nodes which simultaneously collect charge deposited by the same ionizing radiation particle track. MNCC can span multiple microns, greatly complicating

the design and layout of hardened sequential circuit elements [21][22]. MBU probability is strongly dependent on node spacing, feature size, and supply voltage. As feature sizes shrink, MBUs are becoming more of an issue. The LET, range, track radius, and angle of incidence of the particle inducing upset are also important. In general, particles that deposit more energy, have a longer range, and have a larger radius are more likely to induce MBU. Since a single event induces an MBU, the MBU fail pattern is typically contiguous and follows a trajectory. In accelerated experiments, care must be taken when taking data to ensure that adjacent bit errors caused by separate events are not to be considered MBUs. Statistical methods can be applied to sort out adjacent upsets that appear to be MBU as well as fast bitmapping, i.e., time stamping and rapid SRAM readout.

Fig. 1.5 shows MNCC effect on SRAMs designed at Arizona State University in a 90 nm process. Red cells indicate upset cells due to charge collection and MNCC regions are indicated in green. MNCC producing a multi-bit upset in a single EDAC word is trivially avoided in SRAMs by column interleaving, which has been standard practice for decades.

4) Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR)

The charge track from an ion traversing a power MOSFET structure causes an avalanche breakdown between the n-epi and n+ substrate regions and produces a burnout and permanent damage at this interface [23].

SEGR is permanent damage causing rupture in dielectric gate materials due to avalanche breakdown caused by the traversal of a heavy ion [24].

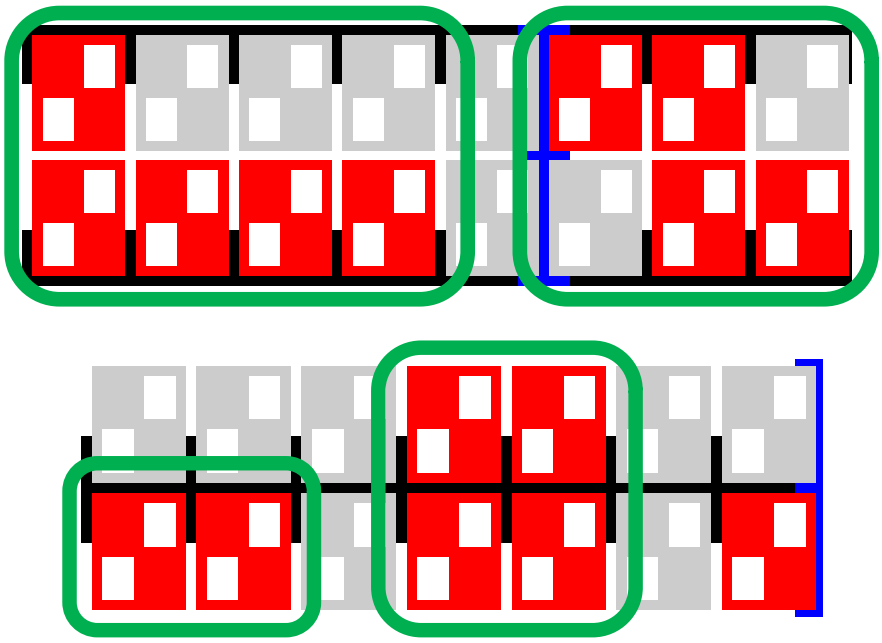


Fig. 1.5. MNCC effect on SRAMs in 90 nm process. Red cells indicate upset cells due to charge collection and MNCC regions are indicated in green

5) Single Event Latchup (SEL)

Single event latchup is a CMOS Latchup caused by the collected charge. A SEL triggers a large supply currents that results when a parasitic silicon controlled rectifier p-n-p-n structure is triggered into a regenerative forward bias [25]. Generally SER requires the device be powered down to turn off the SCR. If the current levels are high enough, permanent damage can result.

1.2 Radiation hardening

Hardness against radiation can be achieved through a variety of methods. One method is by employing special processes in the fabrication of microelectronic circuits. This can involve variation in the substrate structures or doping profiles. All methods use specialized circuit design techniques. Through specific design techniques, it is possible to

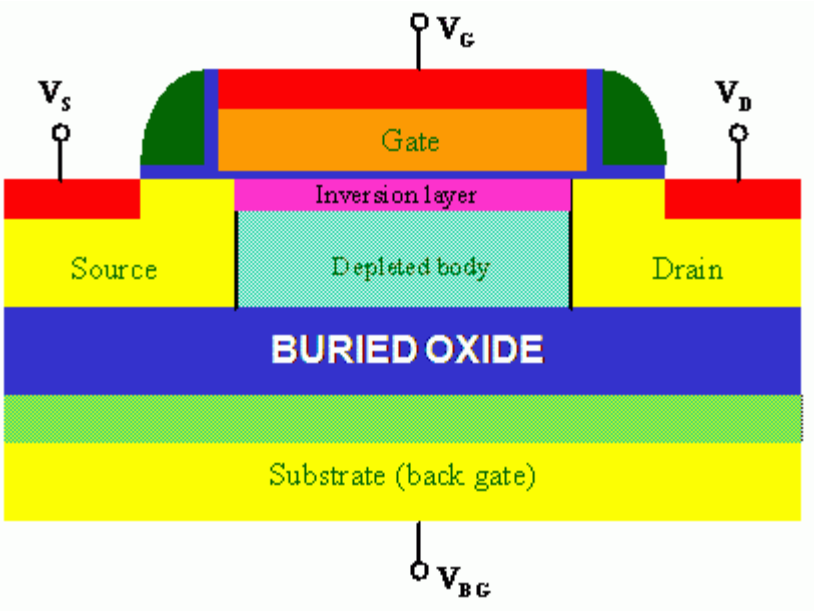


Fig. 1.6. Cross-section of an SOI transistor [26].

fabricate radiation hardened components using standard CMOS process flow known as radiation hardening by design (RHBD).

1.2.1 Process Mitigation Techniques

Substrate structures or doping profiles can have a large impact on reducing the critical charge, thus reducing SER. CMOS with buried implants can improve SER by reducing the size of the funnel formed, thereby reducing the amount collected by sensitive nodes. Following sections discusses some of these techniques.

1.2.1.1 SOI substrate

Substrates incorporating a thin silicon layer on a thicker layer of buried oxide (Fig. 1.6) have been shown to reduce SER sensitivity as compared with bulk silicon [27][28]. In SOI, the isolation provided by the isolation oxide improves the SER robustness since less charge is collected than the bulk counterpart, i.e., the track length is attenuated.

General Advantages of SOI

- Eliminates latch-up.
- Si volume reduction leads to large reduction in critical charge collection compared to bulk.
- No funneling can occur

1.2.1.2 Increasing the critical charge

SEE is a balance between charge collection and critical charge required for upset. If we increase the storage charge of a device its sensitivity to radiation can be reduced. Using either parasitic capacitance with back-end (metallization and inter-level dielectric) process tweaks or dedicated capacitor structures, critical charge can be increased. However, adding capacitance can have some negative effects on dynamic circuit response and dynamic leakage. The capacitors also require space, increasing the circuit area.

1.2.1.3 RC - Hardening

Any change which increases the critical charge while maintaining or reducing the collected charge will improve the SER performance of a device. A typical high-density SRAM cell consists of six transistors; two allowing data to be read and written to-and-from the cell and four transistors making up the two cross-coupled inverters responsible for maintaining the data state.

As shown in Fig. 1.7, resistance can be added between the two inverters so that the time to flip the cell is increased [29], thus effectively allowing the pull-up/pull-down transistors more time to restore the data state. However, this approach affects the write time of the cell. The latch or SRAM response is thus slowed so that it cannot respond to

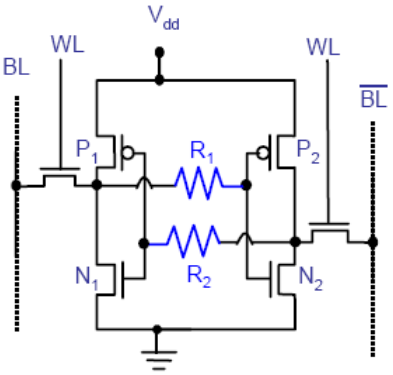


Fig. 1.7. Resistively hardened SRAM schematic [29].

the voltage pulse induced by a radiation event before the charge is removed. As the node capacitance scales down, the resistance must scale up. These approaches seem to be "running out of steam" at about the 0.25μm node.

1.2.2 Design Mitigation Techniques

Soft errors caused by ionizing particles can be overcome by solely using circuit techniques i.e., RHBD [32][35]. Sequential circuit elements like latches, flip flops and registers are hardened to radiation by one of the two well known design techniques, namely hardening by redundancy and via temporal techniques. The principles involved in these two techniques are discussed in the following sections.

1.2.2.1 Hardening by Redundancy

Redundancy hardens by duplication or triplication of the circuit elements and voting out the upset state. Redundancy operates in a way that error propagation is blocked unless two or more circuit elements are simultaneously in error. The most common spatial redundancy technique for combinational logic is the triple modular redundancy (TMR) shown in Fig. 1.8 [31]. Logic is replicated three times and then connected to a majority gate. The majority voter schematic is shown in Fig. 1.9. The

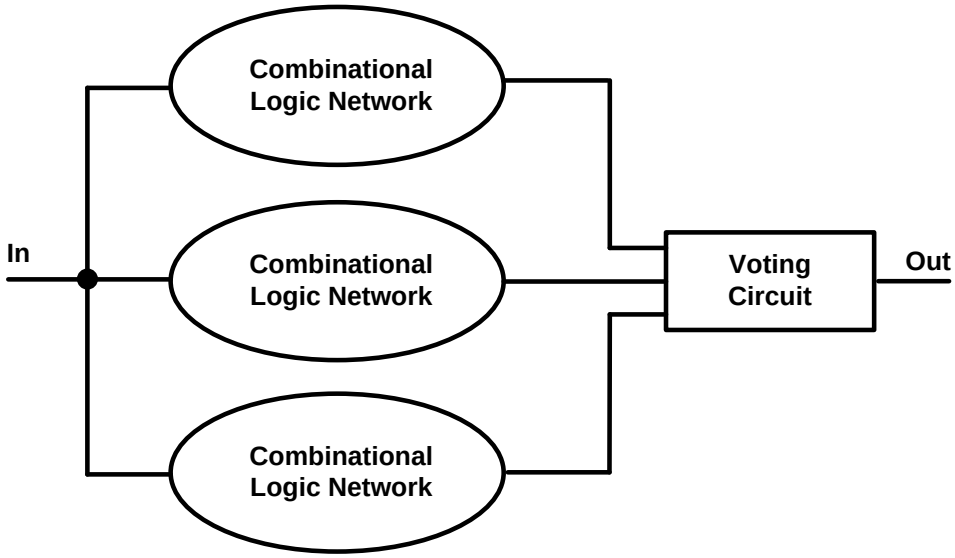


Fig. 1.8. Triple Modular Redundancy [30].

incorrect logic state resulting from the radiation strike at its input is voted out by the other two correct states.

The clear penalty in this technique is the 3X increase in area. This is an expensive technique but it does reduce soft failure rates to near zero levels, providing the necessary reliability for long term mission critical applications. It is also straightforward to implement and validate.

The DICE latch [32] shown in Fig. 1.10 is the most commonly used redundant structure, doubling the storage nodes in a configuration that requires two nodes be upset to change the state. However DICE latch based flip-flops have been shown to be susceptible to SET induced upsets [33], since input or clock errors are not mitigated. Moreover, they are increasingly susceptible to upset by MNCC, particularly on bulk technologies. The high DICE circuit density also makes it very difficult to provide adequate critical node spacing to avoid MNCC induced upsets.

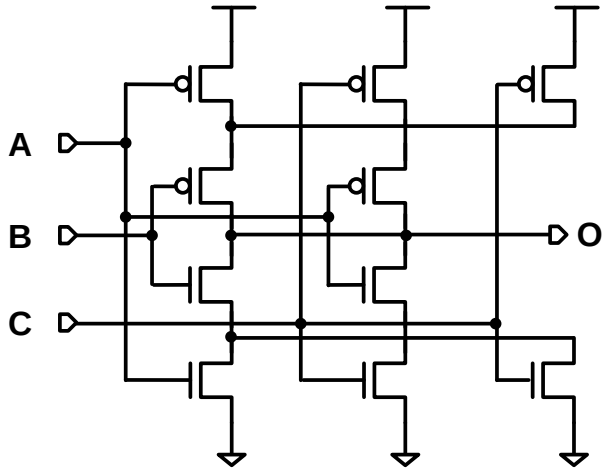


Fig. 1.9. Majority gate schematic.

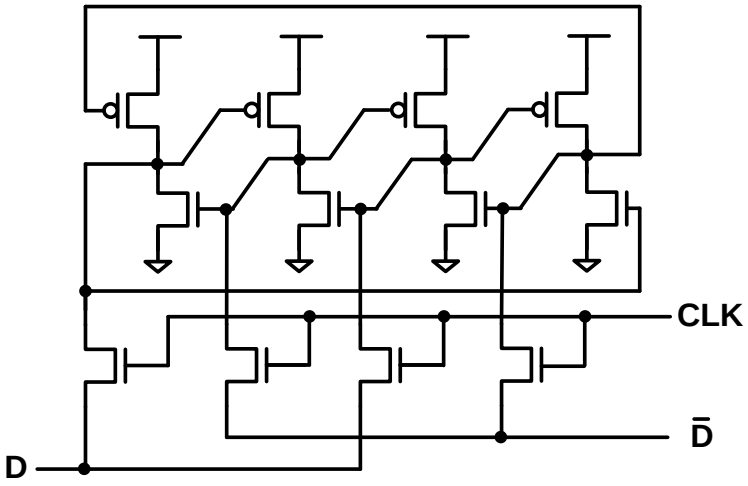


Fig. 1.10. DICE latch schematic [32].

1.2.2.2 Temporal Hardening

Temporal hardening operates by essentially placing various types of low pass filters in the logic string. Various possible designs are described in [34]. One of the ways to achieve temporal filtering is to split the output of each combinational logic string into three branches, delay two of those branches by one and two delays, respectively, and then perform a majority vote on all three. Fig. 1.11 is a block diagram illustration for this technique. To be effective, the delay of each successive element must exceed the

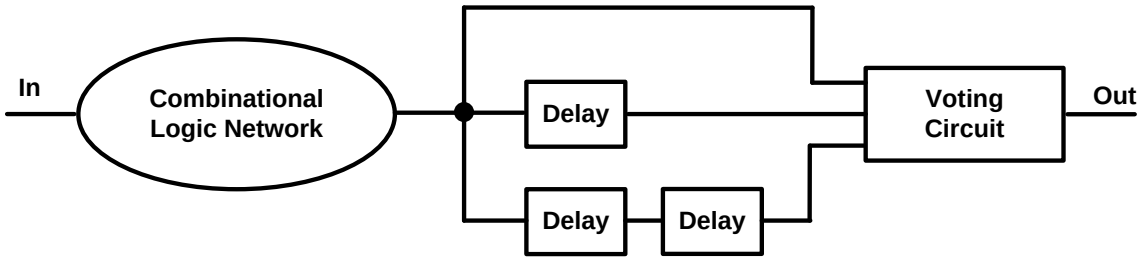


Fig. 1.11. Temporally hardened circuit [30].

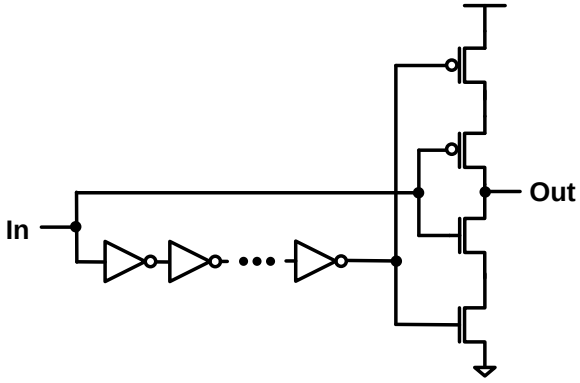


Fig. 1.12. Combination of C-element and inverter chain delay element to filter incoming SETs.

maximum pulse width of the transient.

Temporal hardening uses delay elements to filter upsets into time windows. A delay element is a circuit which delays the input signal by a particular duration. These approaches have been shown effective at mitigating SETs on the sequential circuit clock and control inputs as well as SEUs [34][35]. Delay based filters combine a C-element and a delay element to filter SETs of durations less than the delay element delay as shown in Fig 1.12. Since circuit delay reduces with scaling, a key difficulty in temporal hardening is generating a low power and area delay circuit, that itself does not produce limiting SET durations. For instance, when using current starved delay elements to measure SET durations, up to 3 ns SET durations (t_{SET}) were experimentally measured [36]. Thus, reducing the delay element usage, size, and SET duration due to the delay elements

themselves are key issues in temporal hardening. Temporal filtering the flip-flop (FF) inputs has demonstrated effectiveness when combined with a DICE latch at mitigating both SET and SEU [37].

1.3 Thesis contribution and organization

The causes and IC effects of radiation on silicon were discussed in the previous sections. Radiation hardening is a requirement for microelectronic circuits, especially in aerospace applications, as they are prone to radiation induced upsets from high altitude or orbital neutrons and ions. The most common method to SEE harden VLSI circuits is to use hardened FFs. Chapter 2 classifies different hardened FFs that have been proposed and providing a brief description of the operating principle, advantages and drawbacks for each FF. It is shown that ad-hoc design approaches frequently leave "holes" in the hardness.

Modern CMOS processes are designed to minimize gate delay, which is a key metric. In RHBD, temporal delay circuits must maximize delay. However, current starving or longer than minimum channel length devices in a delay element may also produce the limiting t_{SET}, against which the delay element is used to protect the circuit. Chapter 3 addresses this issue by proposing a dual redundant delay element which does not adversely affect the worst-case SET duration on the IC. Each redundant element is slowed by reduced gate overdrive, and the lower swing of the drain nodes provides power savings. The delay element SET tolerance is demonstrated by simulations using it in a RHBD master slave FF. Using the proposed delay element saves up to 25% total FF power at 50% activity factor. The delay element incorporates redundancy to mask long transients, which would otherwise limit the circuit hardness. A FF layout using the

proposed delay element is used in synthesis and auto-place and route experiments to confirm overall power, performance, and density. It uses a multi-bit cell interleaving the constituent circuits of four FFs to be robust to MNCC.

The design of FFs is made more difficult with increasing MNCC in advanced scaled fabrication processes, which requires that charge storage and other sensitive nodes be separated so that one impinging radiation particle does not affect redundant nodes simultaneously. In chapter 4, a correct by construction design methodology to determine a-priori which hardened FF nodes must be separated, as well as a general interleaving scheme to achieve this separation is described. Graph clustering approaches to determine effective node separation to protect against upset due to MNCC are demonstrated. The methodology is circuit simulation based, making it efficient and usable by circuit designers. The methodology is applied to radiation hardened flip-flops and optimal circuit physical organization for protection against MNCC is demonstrated. Example designs are presented to demonstrate the analysis and clustering for real flip-flop designs.

In chapter 5, a new low power and area efficient radiation hardened flip-flop design is presented. The hardness is verified and compared to other published designs through the proposed methodology that comprehends MNCC and tests resiliency to upsets at all internal and input nodes. Comparison of the hardness, as measured by estimated upset cross-section, is made to two published designs. Additionally, the importance of specific circuit design aspects to achieving hardness is shown. The FF achieves a 31% power and 35% area reduction compared to a previous design with similar hardness.

Finally, the summary of this work and conclusions are presented in chapter 6.

CHAPTER 2

RADIATION HARDENED FLIP-FLOPS

This chapter explores the different radiation hardened FFs that have been proposed in the literature and tries to classify them based on different hardening techniques and the hardness afforded, e.g., to SEU only or to SET and SEU. Radiation strikes affect the sensitive nodes in the combinational logic, by generating voltage transients that propagate through the circuit. These SETs may sometimes be masked by the feed forward logic circuitry. However, if they are captured by a sequential element, the circuit logic state may change affecting its overall functionality. Sequential logic circuits are also vulnerable to radiation strikes that directly upset the storage node logic state (i.e., SEU)

2.1 Radiation Hardened Flip-Flop Classification

By analyzing the working principles of various designs available in the literature, radiation hardened FFs can be classified into two broad categories. One is temporal hardening and the other is hardening by redundancy, both of which were explained in chapter 1. Further, most FFs in each of these categories have similar hardening principles which are mostly improvements or combinations of certain hardening techniques. For instance many FFs utilize the four node redundant storage structure seen in DICE to achieve SEU hardness on storage nodes. This enables us to further classify FFs in each of these two broad categories based on common working principles. Some FFs incorporate hardening principles from both of the two broad categories, for instance the DF-DICE [37] latch utilizes temporal hardening to filter SETs on clock and D inputs and redundant storage structure of DICE for protection against SEUs. The original authors' names are used throughout.

2.2 Redundant Non Self Correcting FFs

FFs hardened by redundancy can be further classified into self-correcting and non-self-correcting. Non-self-correcting FFs, as the name suggests, will not have mechanism to restore upsets on storage node states. Instead the incorrect storage node state is merely prevented from propagating. These circuits typically have redundant latches whose outputs are connected to a C-element or majority gate. If the storage node in one of the latches upsets due to particle strike, the C-element or majority gate inputs mismatch. In the former case, the C-element output tri-states, blocking the upset state from reaching the next stages. Three such FFs belong to this category, the prominent one being BISER proposed by Zhang [44]. The designs proposed by Yamamoto [45] and Masuda [46] are improved versions of BISER FF.

2.2.1 Built In Soft Error Resilience FF

Working principle:

The first FF in this category is the Built-In Soft Error Resilience (BISER) [44]. It consists of two D-flip-flops joined with a C-element as shown in Fig. 2.1. A particle strike can happen either in the clock low or clock high phase and can upset one of the four latches. In the clock low phase latches LB and PH1 hold the stored logic value and hence are prone to SEUs, while LA and PH2 are not error-prone as they are transparent and driven by the preceding logic stages. If a particle strike flips the logic value stored in LB or PH1, the two inputs to the C-element will differ and the error will not propagate to the C-element's output. Similarly in the clock high phase, latches LA and PH2 are holding the data and hence are prone to upsets while latches LB and PH1 are transparent.

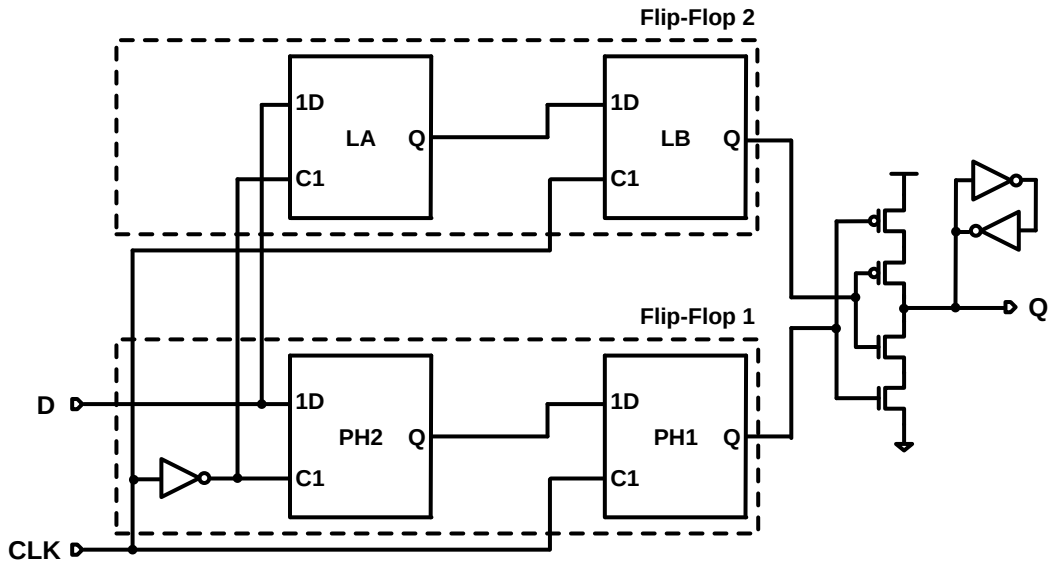


Fig. 2.1. BISER FF schematic [44].

Now upsets on LA or PH2 will be directly fed to C-element inputs, which again tri-states if they mismatch preventing the error from propagating further.

The purpose of the keeper is to fight the leakage current in the C-element when both its pull-up and the pull-down paths are shut off, which occurs only when the content of one bi-stable circuits gets flipped by a particle strike.

Advantages:

Its layout area is slightly more than twice the standard D-FF layout which is relatively small as compared to other hardened FF designs, especially temporal FFs.

Disadvantages:

It is not hard to SETs on its D and clock inputs. A major flaw in this design is the exposed storage node at the output Q which may cause data from the next stage to write back and change the current FF state. Finally, it is not self-correcting.

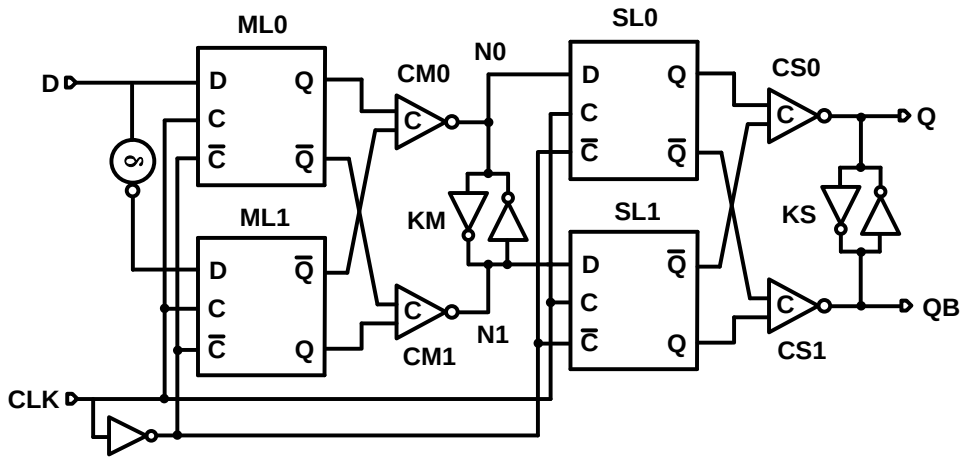


Fig. 2.2. Bi-stable cross-coupled dual modular redundancy (BCDMR) FF schematic [45].

2.2.2 Bi-stable Cross-Coupled Dual Modular Redundancy FF

Working principle:

The bi-stable cross-coupled dual modular redundancy flip flop (BCDMR) [45] shown in Fig. 2.2 is an "improved" version of BISER. It has two C-elements connecting the master to the slave latches. There is an inverting delay element between the two master latches ML0 and ML1; hence their inputs will have opposite logic states, resulting in the C-elements CM0 and CM1 to have identical logic states at their inputs. Thus this design adds temporal protection to the D input.

Similar to the BISER FF case, a particle strike can happen either in the clock low or clock high phase and can strike one of the four latches. In the clock low phase, the protection provided to upsets in latches SL0 and SL1 by C-elements CS0 and CS1 is similar to that in BISER. However, in the clock high phase, unlike BISER, the C-elements CM0 and CM1 prevent upsets in ML0 and ML1, both in hold mode, from propagating further. The C-elements must have sufficient drive strength to flip the weak keeper. The keepers need not be strong as the two C-elements will rewrite the keeper if it flips.

Advantages:

It is hard to SETs on D-input. In the clock low phase, a delay filter circuit will be formed at the D-input, as latches ML0 and ML1 become transparent, connecting the delay element to one of inputs of C-elements CM0 and CM1.

Disadvantages:

It is not hard to SETs on clock inputs. This design also has the same flaw as the BISER design where it has exposed storage node at the output which may cause data from the next stage to write back and change the current FF state. This is a common error in academic papers but absolutely never occurs in real commercially shipping industry designs. Of course it makes the timing and power look better, but is prone to coupling noise induced failure. The area advantage of the BISER FF no longer holds for this FF, as it has a delay element, three additional C-elements, and three additional keepers.

2.2.3 Bi-stable Cross-Coupled Dual Modular Redundancy FF with Adaptive Coupling

Working principle:

The FF [46] shown in Fig. 2.3 (top) is essentially BCDMR FF with the standard D latches replaced with master and slave latches of adaptive coupled flip-flop (ACFF) shown in Fig. 2.3 (bottom). Hence it is called BCDMR-ACFF. Its working principle is same as BCDMR except for the functioning of ACFF. The master latch has adaptive-coupling (AC) element, comprised of PMOS and NMOS transistors connected in parallel with both their gates connected together. The reason for having the AC element in the master latch is as follows.

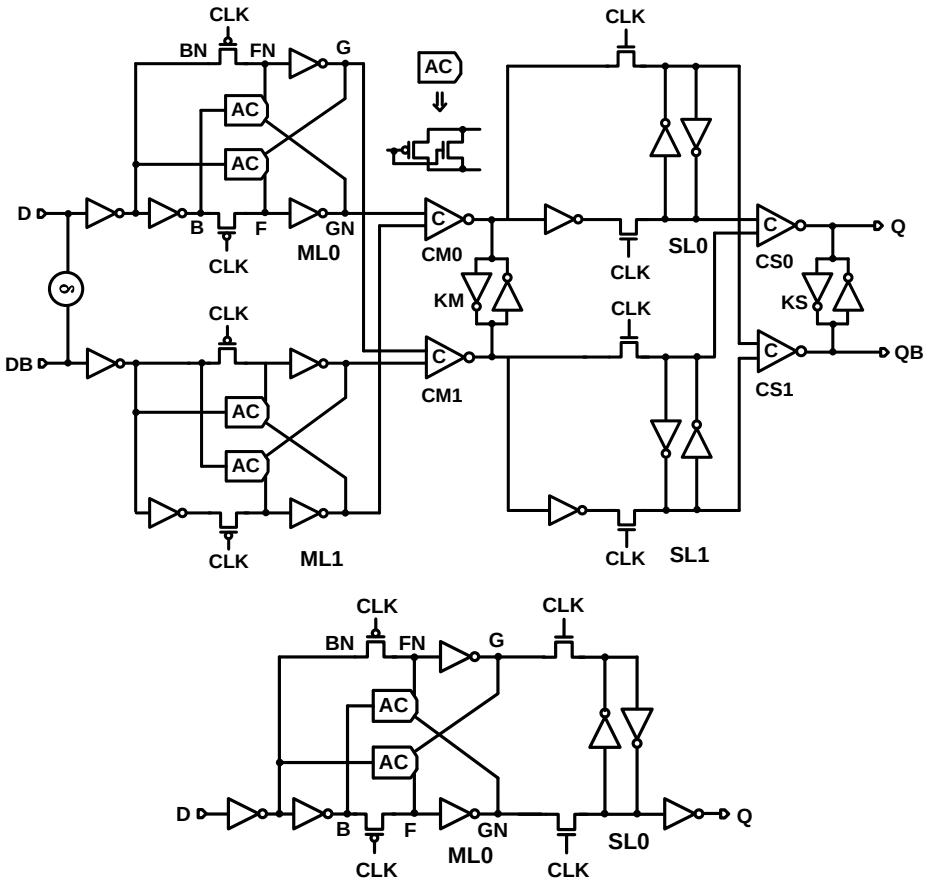


Fig. 2.3. BCDMR-ACFF (top) [46] and AC flip flop (below) [47] schematics.

Let us assume that there is no AC element. Node F will be connected to node G and node FN will be connected to node GN. Now assume node G (or node F) to be at logic 1 and node GN (or node FN) to be logic 0. Due to the weak current drive of PMOS pass gate, logic 0 (D=0) cannot be written on node G (or node F). Now consider the case when the AC element is added to the master latch as shown in Fig. 2.3. Now if logic 0 has to be written to node G, node BN should be at logic 1 and node B should be at logic 0. This causes the NMOS transistor in the bottom AC element to turn on, resulting in the state of node F to be lowered to Vdd-V_t, when the current discharges through the F-B path. Due to the lowered potential on node F, the PMOS pass gate can now pull node F and hence node G towards logic 0. However, node F will not be completely discharged. When node G goes to logic 0 by charging node FN, node F will be completely discharged

to 0V through the G-F path, as the NMOS in the AC element allows a strong discharge current.

Advantages:

This FF saves power as the ACFF operates with the single-phase clocking scheme. Power reduction is achieved by not using the local clock buffers and using pass transistors instead of transmission gates, which results in four fewer transistors than the standard transmission-gate FF.

Disadvantages:

As PMOS pass transistors have weak current drive and are used to write data into latch storage nodes, the SEU recovery time will be longer. Again since disruption of the output jam latch is independent from a soft error, the lack of output buffering is unacceptable. The use of slave jam latches makes this design problematic on modern processes with high process variation. Moreover, using NMOS pull-ups and PMOS pull-down transistors is generally banned for the same reasons.

2.3 Redundant Self Correcting FFs

In the self-correcting designs, upsets on storage node states are restored to original state by built-in circuit mechanisms. The restoration is due to positive feedback between storage nodes. Most FFs in this category base their design either on the four node storage structure seen in DICE or utilize C-elements. Hence, the self-correcting designs are further classified as the ones that utilize a DICE latch storage structure and the ones that utilize C-elements. The FFs proposed by Huang [48], Komatsu [49], Sheng Lin [51] and Omana [52] are self-correcting designs that utilize C-elements. The designs proposed by Hazucha [53], Jahinuzzaman [54], Blum [55] and Saihua Lin [56] are self-correcting

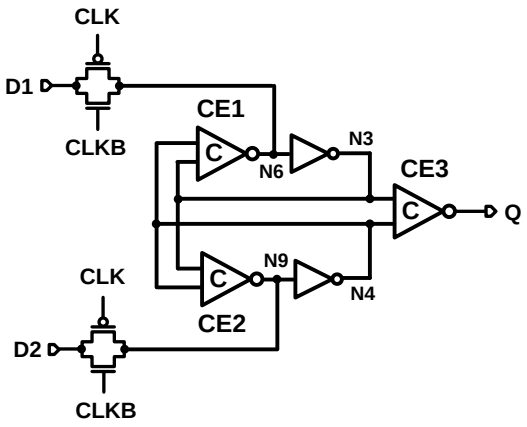


Fig. 2.4. C-Element based latch schematic [48].

designs that incorporate DICE latch storage structure. The TMR FF proposed by Hindman [43] does data correction in the clock low phase and hence can also be categorized as self-correcting.

2.3.1 Redundant Self Correcting C-Element Based FFs

2.3.1.1 Three C-Elements Based Latch

Working principle:

Fig. 2.4 shows a hardened latch design using three C-elements [48]. There are three C-elements in the latch: CE1, CE2 and CE3. CE1 and CE2 constitute a "dual interlocked" keeper for two purposes. Firstly, they can be used as keepers when the latch is not transparent to keep the correct value. Secondly, they are used to mask the radiation-induced SEU on the internal storage nodes N3 and N6. C-element CE3 is used to block soft errors from propagating through the latch. Consider an upset on node N3, when the latch is in hold mode. The C-element CE1 tri-states, and holds node N6 in its original state, eventually driving the node N3 to recover to its original state. Until that time, the C-element CE3 also tri-states and blocks the data from propagating further.

Advantages:

Its layout area is almost twice the standard D latch area, which is relatively small as compared to other hardened FF designs, especially temporal FFs.

Disadvantages:

This latch is not hard to SETs on data and clock inputs. With delay element between D1 and D2, the latch can mitigate SETs on D input. When the latch is in the hold mode, if node N6 (or N9) is upset due to particle strike, node N3 flips that causes CE1 (or CE3) to tri-state. There is no mechanism to restore node N6 to its original state and eventually, due to charge leakage nodes N6 and Q may switch to wrong state. Also, since the C-elements occupy only two polygon tracks, storage nodes will be in close vicinity making them vulnerable to multi-node charge collection. Consequently this latch is not really hard to all SEU or SET possibilities. Thus while small, it is also ineffective.

2.3.1.2 Soft Error Hardened Latch

Working principle:

Fig. 2.5 shows the schematic for the soft error hardened (SEH) latch proposed in [49]. The latch operates by complementary clocks, CK and CKB. The circuit has two bi-stable elements formed by transistors P1-N1 & P8-N2 and P1-N1 & P2-N8. DH, PDH and NDH are the three storage nodes in the circuit. When the latch opens, input data drives the DH, PDH and NDH. PDH and NDH have the same polarity as the input data while DH has inverted polarity.

Consider the latch to be in the hold mode and the node DH to be at logic 1 state. As nodes PDH and NDH are complimentary to node DH, both will be in the logic 0 states, turning on transistor P1 and holding node DH at logic 1. Now, if an upset on node

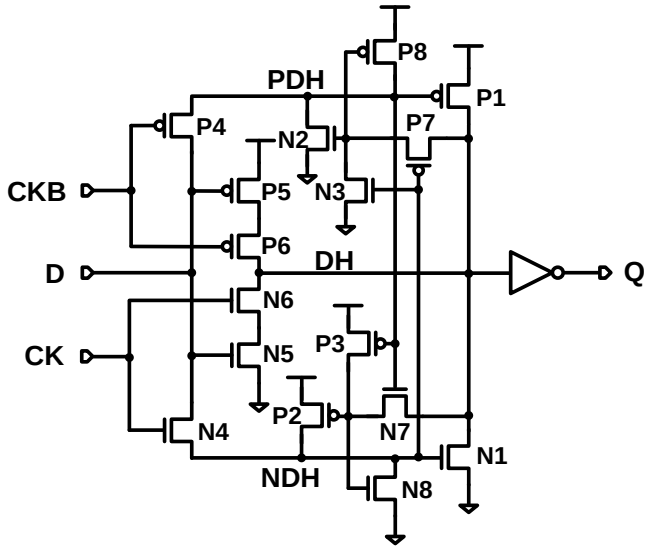


Fig. 2.5. Soft error hardened latch schematic [49].

DH pulls it to logic 0, it will be pulled back to the logic 1 state through P1. Now consider the case when there is an upset on node PDH and pulls it to logic 1 state. The logic 0 state on node NDH will turn on P7, which then turns on N2 due to logic 1 state on node DH. Eventually transistor N2 pulls the node PDH back to logic 0. Similar analysis holds good for logic 1 to 0 upset on node PDH, where P8 would restore the logic 1 state as N3 would turn on due to logic 1 state on NDH.

Advantages:

As the circuit has 18 transistors, the layout area is small as compared to other hardened designs.

Disadvantages:

This latch is not hard to SETs on data and clock inputs. Also, as the circuit is small, the storage nodes will be in close vicinity making them vulnerable to multi-node charge collection. The extensive use of NMOS pull up and PMOS pull down transistors is problematic for robustness to process variation, which is more commonly encountered than soft errors.

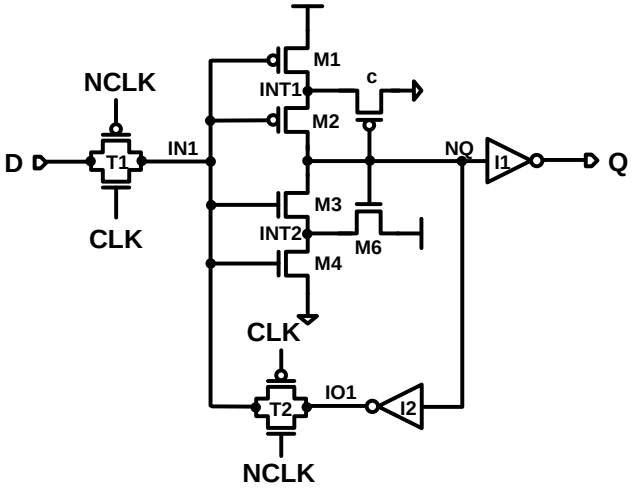


Fig. 2.6. Schmitt trigger based latch schematic [51].

2.3.1.3 Schmitt Trigger Based Latch

Working principle:

A hardened latch design based on Schmitt trigger [51] is shown in Fig. 2.6. In this latch, node IN1 is connected to a Schmitt trigger that consists of six transistors. The Schmitt trigger provides tolerance to soft errors by obviously resisting a voltage change (since this is what Schmitt triggers are designed to do), i.e., hysteresis. When node IN1 is at logic 0 state, node NQ will be in logic 1 state, M6 is on, and node INT2 is charged. Consider the latch to be in the hold mode. Now, if there is a strike on node IN1 that changes its state from logic 0 to logic 1, to affect NQ, the charge at node INT2 has to be discharged. Thus the logic state on storage node NQ will be retained until the additional charge due to parasitic capacitance on node INT2 is fully discharged. During this time the inverter I2 driving node IN1 would restore it to the original state. Similarly if the strike on node IN1 changes its state from logic 1 to logic 0, to affect NQ, the charge at node INT1 has to be discharged.

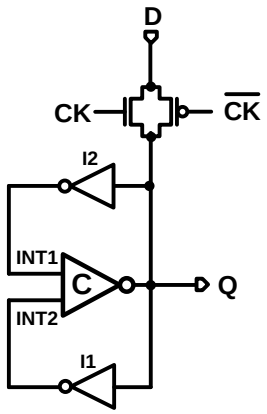


Fig. 2.7. Split internal node latch schematic [52].

Disadvantages:

This latch is not hard to SETs on D and clock inputs.

2.3.1.4 Split Internal Node Latch

Working principle:

Fig. 2.7 shows a latch [52] design based on duplicating the nodes within the latch feedback loop. When CK = 1, D propagates to the output Q and is fed back to nodes INT1 and INT2 through inverters I1 and I2, respectively. Since both of these internal nodes assume the same logic value, only one of the series of two transistors, MN1-MN2 or MP1-MP2, will be conducting. When CK = 0, the transmission gate is turned off and, consequently, the previous output value is maintained. In case of a strike affecting one of the latch feedback internal nodes INT1 or INT2, the C-element inputs mismatch and its output Q temporarily moves to a high impedance state, without changing its logical value.

Disadvantages:

This latch is not hard to SETs on D and clock inputs. The storage node is directly connected to the output (but this is easily fixed). When the latch is in the hold mode, an

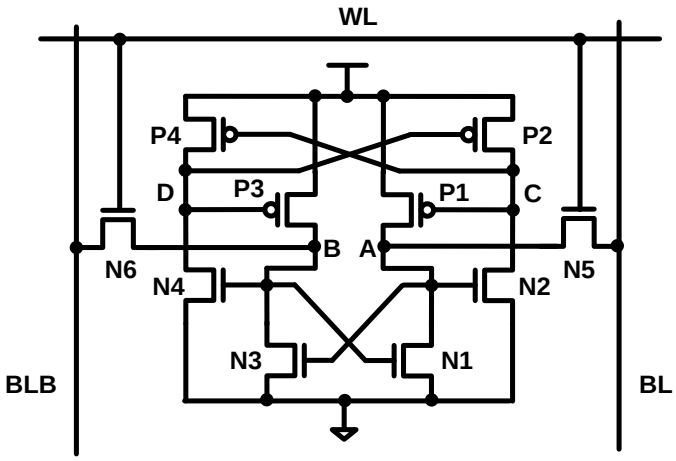


Fig. 2.8. Ten transistor hardened latch schematic [54].

upset on node Q causes it to flip to a wrong logic state and there is no mechanism to restore it to the original state. Basically it splits the feedback node into two and the design is hard to upsets on them, but the hold node is unhardened.

Advantages:

No advantages are seen in this latch as it has the above mentioned design flaw.

2.3.2 Redundant Self Correcting DICE Based FFs

2.3.2.1 Quatro Latch

Working principle:

Fig. 2.8 shows a hardened SRAM design [54] consisting of ten transistors called the Quatro latch. Two access transistors, N5 and N6, connect the bit lines (BL and BLB) to the storage nodes A and B. If the stored bit is‘0’, the logic states at nodes A, B, C, and D will be ‘0’, ‘1’, ‘1’, and‘0’, respectively. Each of these nodes is driven by an NMOS and a PMOS transistor, their gates being connected to two different nodes. If an SET pulls down (up) a node voltage, the node voltage is restored by the ‘ON’ PMOS (NMOS) transistor connected to the node and driven by an unaffected node.

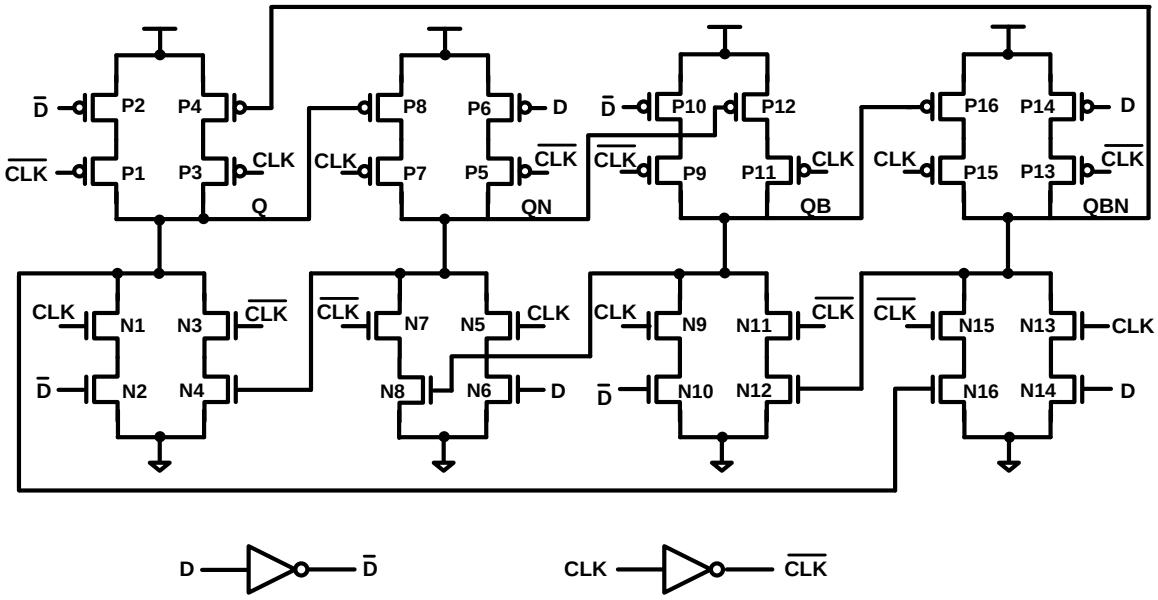


Fig. 2.9. Soft error tolerant static D latch schematic [56].

Advantages:

It is DICE latch with modifications.

Disadvantages:

The modifications from the DICE make the latch suffer than DICE. The latch is vulnerable to multiple node charge collection from a single particle strike, the worst case being two nodes at same potential (nodes A and D or nodes B and C) getting affected. Therefore, in order to reduce the possibility of upsets due to MNCC, the cell should be laid out by keeping the same potential nodes as physically apart as possible.

2.3.2.2 Static DICE Based D Latch

Working principle:

Fig. 2.9 shows another latch design based on DICE latch [56]. It essentially integrates tri-state inverters to a DICE latch which has Q, QN, QB and QBN as its storage nodes. In the clock high phase transistors P1-N1, P5-N5, P9-N9 and P13-N13 are on and

P3-N3, P7-N7, P11-N11 and P15-N15 are off, enabling the data to be written to the latch storage nodes. In the clock low phase, the latch is in the hold mode and P3-N3, P7-N7, P11-N11 and P15-N15 are on, turning the circuit to a DICE latch structure. In this phase, transistors P16-P15-N15-N16, P12-P11-N11-N12, P8-P7-N7-N8 and P4-P3-N3-N4 form the DICE structure.

In the hold mode, consider the logic states on storage nodes Q, QN, QB, and QBN to be LHLH and due to particle strike assume the pattern changes to LLLH. Now, P12 turns on trying to charge node QB to H and N4 turns off, leaving the node Q floating. The L state on node Q keeps transistor P8 on that eventually charges node QN to H, bringing the logic states on storage nodes back to LHLH.

Advantages:

This latch is similar in design to the latch described in section 2.3.2.1. It has relatively small area as compared to other hardened designs

Disadvantages:

It is not hard to SETs on D and clock inputs. As the storage nodes are in close vicinity, they are vulnerable to multi-node charge collection.

2.3.3 Triple Mode Redundant FF

Working principle:

The last design [43] in the self-correcting category is shown in Fig. 2.10. It is the most robust of all the FFs seen so far but by far the largest. It has the normal D-FF replicated three times with a modified slave latch. The slave latch feedback path uses a majority gate driven by the other redundant copies. When the clock rises, the slave latch holds the data and the master latch is transparent. In this clock high phase, the state of the

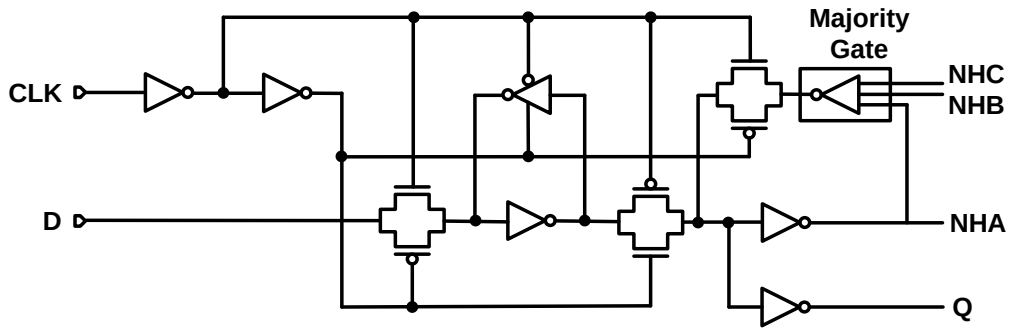


Fig. 2.10. Triple Mode Redundant FF schematic [43].

slave latch is voted to be the same as the majority of the triple redundant copies. This provides the self-correcting feature, which allows clock gating, in the FF. Node NHA in the slave latch and nodes NHB and NHC from other two copies are fed to the majority gate. Similarly, nodes NHA NHB and NHC are fed to the majority gates in the other two latches. The added capacitive loading on the NHA node does not affect the circuit timing as the slave latch has the entire clock high phase to propagate the slave latch feedback signals.

Advantages:

It is hard to SETs on D and clock inputs. The circuits using this FF will have full commercial speed performance, except for slightly longer local routing. A variation of these FFs that have correcting master latches has been used extensively in FPGA based designs [63].

Disadvantages:

Since the circuits using this FF are replicated three times there is a threefold increase in area and power as compared to the same unhardened circuits.

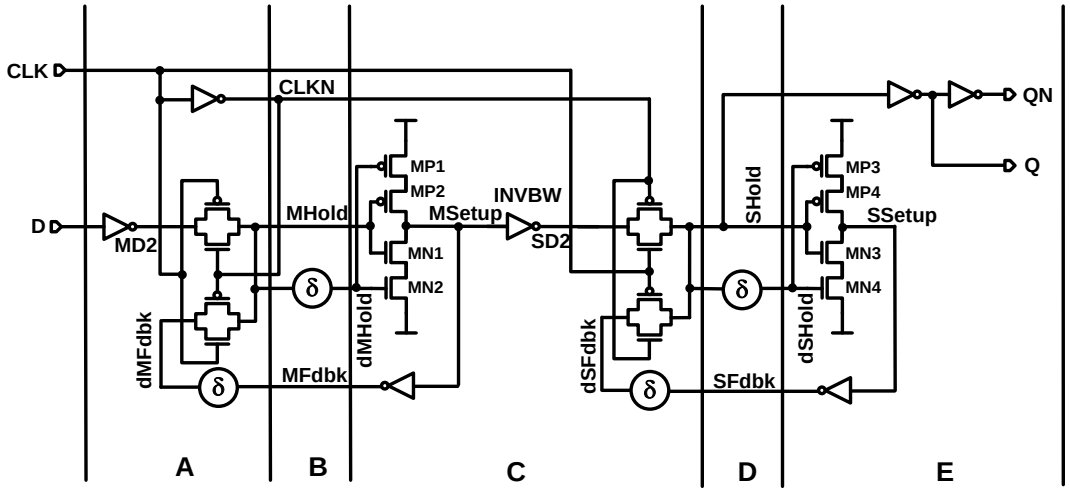


Fig. 2.11. Temporal FF schematic [35].

2.4 Temporal FFs

Temporal designs' working principle was explained in chapter 1. All temporal FFs utilize delay filters to filter SETs in time domain. As was shown in chapter 1, the delay filter combines a delay element with either a C-element or a majority gate and can filter SETs on clock, data and other control signals. For the delay filter to be effective the delay element delay should be more than the expected SET duration.

The delay filter in Matush's [35] design incorporates C-elements while that in Mavis's [34] design incorporates majority voter. The designs proposed by Knudsen [39] and Naseer [37] although classified as temporal designs, utilize DICE redundant storage structure in their master and/or slave latches. The delay elements occupy most of the FF area and dissipate most of its power. Hence designing a low power area efficient delay element is essential to these designs - that is covered in chapter 3.

2.4.1 Four Delay Element FF

Working principle:

Fig. 2.11 shows a temporal FF [35] schematic comprised of two temporal latches acting as the master and slave. In this design, there are four delay elements, two for each latch. The latch uses dual redundancy, in the form of one delayed and one non-delayed node, driving the C-element storing the latch value. The delay assures that the effect of an SET on the hold nodes, or preceding nodes, does not flip the latch. The first delay element, combined with the C-element, mitigates SETs at the pins D, CLK, and CLKN that are less than the delay element delay. The second delay element in the feedback loop protects the latch nodes, MSetup and SSetup, from SEUs. Without this delay, a hit on a logically high setup node would cause a low value to be fed back to the C-element, causing the C-element to tri-state. When tri-stated, the C-element cannot restore the setup node to the correct value. The second delay element allows the C-element to remove any charge collected on the setup nodes before it tri-states. The inverter INVBW between node MSetup and the slave latch input node SD2 prevents charge sharing failures.

Advantages:

This FF is very robust as it is hard to SETs on D and clock inputs and to SEUs on the storage nodes.

Disadvantages:

The drawback of this FF (and all temporal FFs) is the increased circuit size and power dissipation due to the delay elements. It has four delay elements. Delay elements are composed mostly of inverters driving two large capacitances with a buffer at the end.

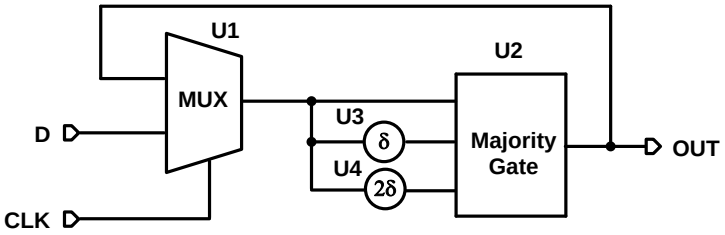


Fig. 2.12. Temporal latch employing majority gate [34].

The FF setup time increases by an additional delay element delay to account for an SET during the setup time.

2.4.2 Temporal Latch Incorporating Majority Gate

Working principle:

Fig. 2.12 shows the temporal design [34] incorporating majority gate. It has a two-input MUX (multiplexer) with its output fed back to one of its input, the data fed to its other input, and the select line controlled by the clock signal. The MUX (UI) output is sampled using a majority gate (U2) along with sampling delays (U3 and U4) and then the majority of the sampled data is fed back to the input. An SET at the D-input passing through the MUX reaches the majority gate at three separate times t, t+δ and t+2δ. Hence at any given time, the majority gate sees the transient at only one of its inputs. The other two inputs will not have transients and hence the SET is voted out. By using the MUX at three separate times, the temporal latch is effectively replicated not in space, but in time. This temporal latch is also immune to transients occurring on the input clock node. Any clock transient momentarily switches the selected MUX input producing a possible transient at the MUX output. Since this is just the data input to the temporal sampling circuitry, it is eventually rejected by the voting circuitry.

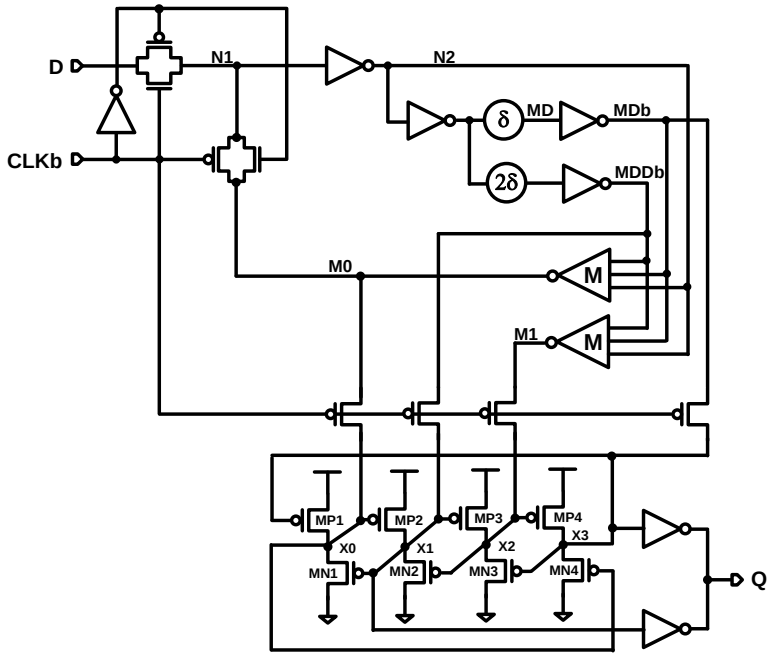


Fig. 2.13. Temporal FF schematic incorporating DICE latch [39].

Advantages:

This latch is hard to SETs on D and clock inputs and to SEUs on the storage nodes.

Disadvantages:

This latch has three delay elements and has greater circuit size and power dissipation than a conventional DFF, as well as a much larger the effective setup time.

2.4.3 Temporal FF Incorporating DICE Latch

Working principle:

The temporal FF [39] shown in Fig. 2.13 comprises a temporal master latch discussed in section 2.4.2 and a DICE slave latch. As explained in previous section, the temporal latch is not susceptible to SEU or SET induced upsets on the D and CLK inputs. The temporal master latch generates three signals M0, MDb, and MDDb, which are combined by the feedback majority gate and connected to DICE slave latch. The fourth

DICE input M1 is generated through a second majority gate. M0 and M1 have the same signal polarity while MDb and MDDb have opposite signal polarity. The PMOS pass transistors connect the master latch to the DICE slave latch. The DICE latch PMOS to NMOS ratio is sized to allow the PMOS to overcome the NMOS feedback. Two separate output inverters connected in parallel to drive a common output, splits the capacitive loading of the output inverter transistors across two of the DICE storage nodes, improving the clock to Q delay.

Advantages:

This latch is hard to SETs on D and clock inputs. The DICE slave latch replacement for a temporal slave latch results in reduced circuit area and power dissipation compared to other temporal designs.

Disadvantages:

It utilizes three delay elements in the master latch resulting in increased circuit size as compared to conventional FF designs. Since the clock closes the slave latch before the inputs are able to recover, the incorrect logic state is captured.

2.4.4 DF-DICE Latch

Working principle

Fig. 2.14 shows a temporal latch [37] hard to SETs on input, clock and control signals as the incoming clock, data, preset and clear signals pass through the delay filter. This latch essentially has the DICE structure with preset and clear control signals integrated to the four standard PMOS-NMOS structures seen in DICE. CLKB1 and CLKB2 are the inverted version of the CLK signal. Nodes I1, I2, I3 and I4 are the DICE latch storage nodes. In the clock high phase, the latch is transparent, transmission gates

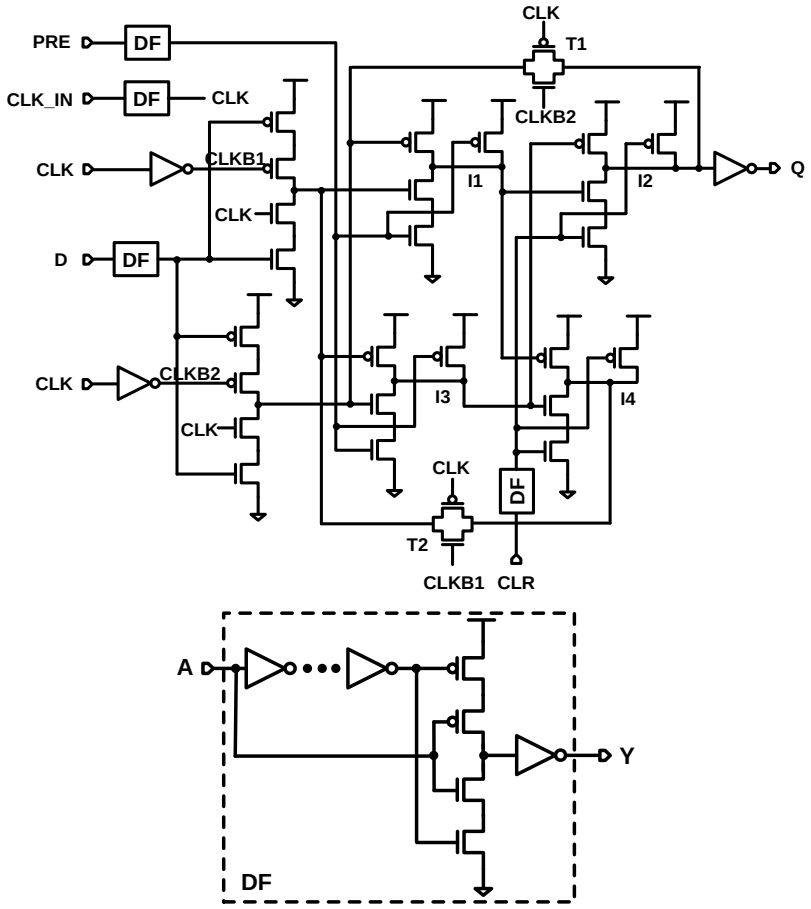


Fig. 2.14. DF-DICE latch schematic [37].

T1 and T2 are turned off and data is written on nodes I1 and I3. In the clock low phase, the latch holds the data as the transmission gates T1 and T2 are turned on completing the four node feedback structure of DICE latch. Now upsets due to particle strikes on any of the four storage node are restored by the self-correcting feature of the DICE latch.

Advantages:

This latch is hard to SETs on clock, data and control signals. Due to the DICE latch storage structure it is hard to SEUs on storage nodes.

Disadvantages:

This design uses four delay elements leading to increased area and power penalty. Also as the output of the C-element is a dynamic node, it can lose its state if left floating

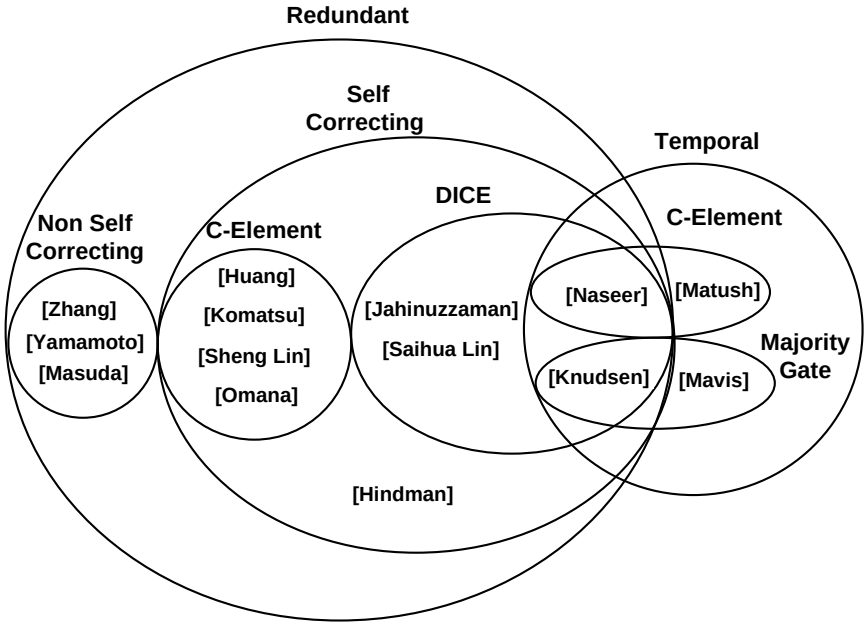


Fig. 2.15. Venn diagram representation of FF classification.

for longer times. To overcome this problem, a weak inverter which provides feedback and maintains the output state should be used at the output node.

2.5 Summary

In the previous sections, the working principle, advantages and disadvantages of different hardened FFs were discussed and they were categorized based on common hardening principles. This classification can be better represented as a Venn diagram as shown in Fig. 2.15. The FFs in each category are represented by the first author names in the papers that proposed the designs.

As seen in the diagram, hardening by redundancy and temporal hardening are the two major groups. Four designs that are temporally hardened combine delay elements either with C-element or majority gate to achieve hardness. Hence two subgroups can be seen inside temporal hardening. The designs by [Naseer] and [Matush] employ C-

elements and designs by [Mavis] and [Knudsen] employ majority gate; hence they are put together in the sub groups named C-element and majority gate respectively.

Hardening by redundancy is a much larger group consisting of twelve designs of which nine are self-correcting and three are non-self-correcting. Hence two subgroups comprise the redundancy group. The designs by [Yamamoto] and [Masuda] are improved versions of BISER FF which is proposed by [Zhang] and hence all three are put in the non-self-correcting group. The designs by [Jahinuzzaman], [Sainua Lin], [Naseer] and [Knudsen] are derived from classic self-correcting DICE latch, which forms a group of its own. The designs by [Huang], [Komatsu], [Sheng Lin] and [Omana] are self-correcting but employ C-elements. The design by [Hindman] is self-correcting but does not employ C-element or DICE latch; hence it is outside these groups but inside the self-correcting group. The designs by [Naseer] and [Knudsen] are temporally hardened but incorporate DICE structure for storage node protection and hence they are in the intersection of two broad categories.

All temporal FFs by definition utilize a delay element. Measured SET pulse widths have varied significantly in different experiments [36]. Those relying on current starved delay elements (which ease these experiments by making the delay programmable) exhibit very large t_{SET}. This presents a conflict in designing the delay elements, which must simultaneously achieve large delay but with high drive strength.

In the next chapter we propose a RHBD delay circuit that does not increase worst-case IC SET duration by providing redundant current starved delay paths.

CHAPTER 3

TEMPORAL SEQUENTIAL LOGIC HARDENING BY DESIGN WITH A LOW POWER DELAY ELEMENT

In the previous chapter, different temporal FFs were discussed which employed majority gate voters or C-elements coupled to delay elements. The delay element is a circuit that postpones the input by an amount at least exceeding the duration of the SET to be filtered.

As mentioned in Chapter 1, RHBD delay elements, are comprised of CMOS circuits. Thus they can collect charge. The delay elements in a RHBD temporally hardened master slave flip-flop occupy nearly 80% of the area and consumes 80% of the active power [35]. Thus, reducing the delay element power is very desirable. However, it must not increase the design susceptibility to SETs. The SET duration is a function of the driving circuit's ability to rapidly remove the charge [57]. This charge removal ability is severely impaired by current starved driving elements. For instance, SET durations up to 3 ns [36] (Fig. 3.1) have been measured with temporal latches using current starved inverters far exceeding that for standard logic on those technology nodes. Consequently, using these delay circuit elements creates worst-case SET durations far in excess of what would otherwise occur on the IC.

Since the MSFF setup time is increased by 2 t_{SET} for hardened operation [35][39], it is important not to increase the design SET duration via the hardening approach itself. We attempt to address these issues with the low power, SET tolerant delay element proposed in this chapter.

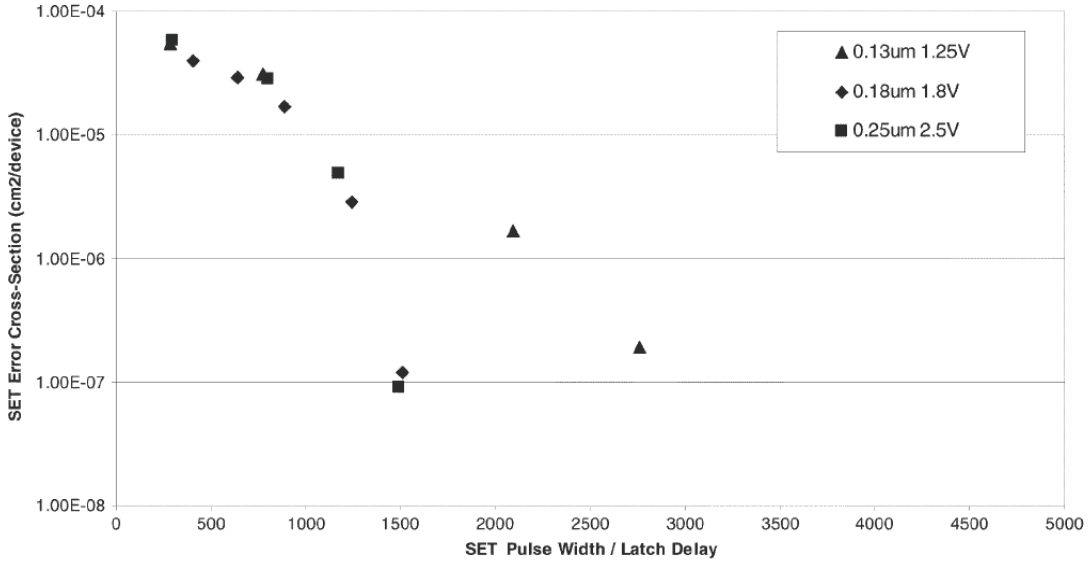


Fig. 3.1. Measured SET durations with temporal latches using current starved inverters [36]

3.1 Delay Element Possibilities

A delay element is a circuit that produces a digital output delayed by a specified amount of time. Delay elements can be broadly categorized as cascaded inverter based and voltage controlled (also known as current starved inverters). The important parameters that have to be considered while designing the delay element are its layout area, power dissipation and charge removing ability which determines the SET duration.

3.1.1 Effect of Transistor Drive Strength on SET Duration

Before looking into the different delay element possibilities, the charge removal ability of the transistor which determines the worst-case t_{SET} of the circuit has to be understood. The current through the transistor is defined as its drive strength, i.e., proportional to the transistor width (W) and a function of the gate-to-source voltage (V_{gs}) that affects gate overdrive $V_{gs} – V_T$, where V_T is the transistor threshold voltage. Fig. 3.2 illustrates these effects by simulating the SET duration t_{SET} vs. transistor W/L and V_{gs} for

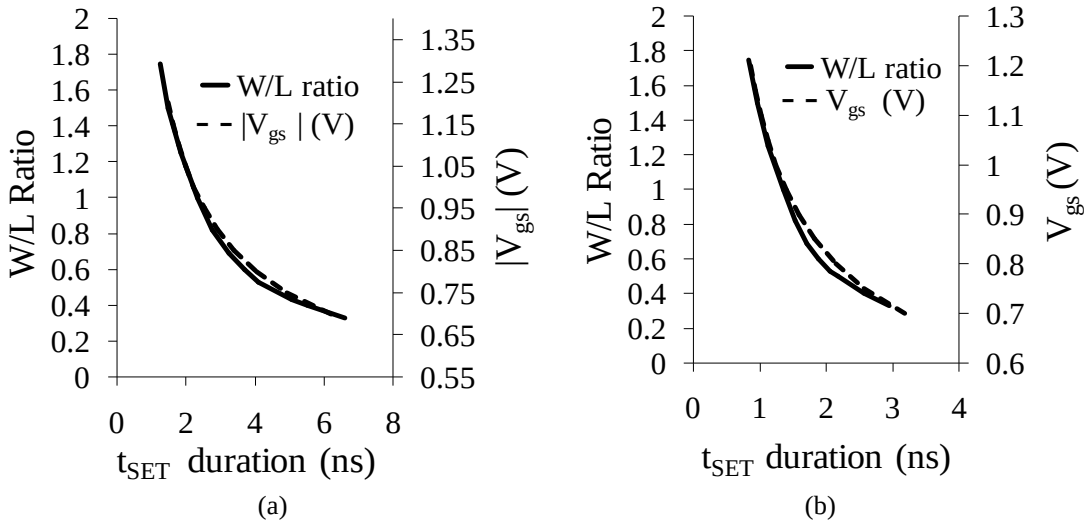


Fig. 3.2. The variation of SET duration as of function of drive strength and gate bias for a (a) PMOS transistor and (b) NMOS transistor.

both PMOS and NMOS (see Figs. 3.2(a) and 3.2(b), respectively). The SET is induced by charge deposition to the transistor drains using a charge conserving Verilog-A charge collection model, as was used in [35]. The basic equivalence between transistor width and gate overdrive is evident for both PMOS and NMOS. In the worst-case, standard gates will have narrow devices, which may be stacked, producing a sub-minimum design rule equivalent W/L, yielding the worst-case t_{SET} for a particular RHBD integrated circuit. Modern CMOS processes are designed to minimize gate delay, which is a key metric. However, current starving or longer than minimum channel length in a delay element will produce the limiting t_{SET}, against which the circuit is hardened.

3.1.2 Cascaded Inverter Based Delay Element

Cascaded inverters shown in Fig. 3.3 (a) can function as a simple delay element that delays the input signal by an amount equal to their combined propagation delays. The propagation delay of an inverter depends upon the time taken to discharge/charge the

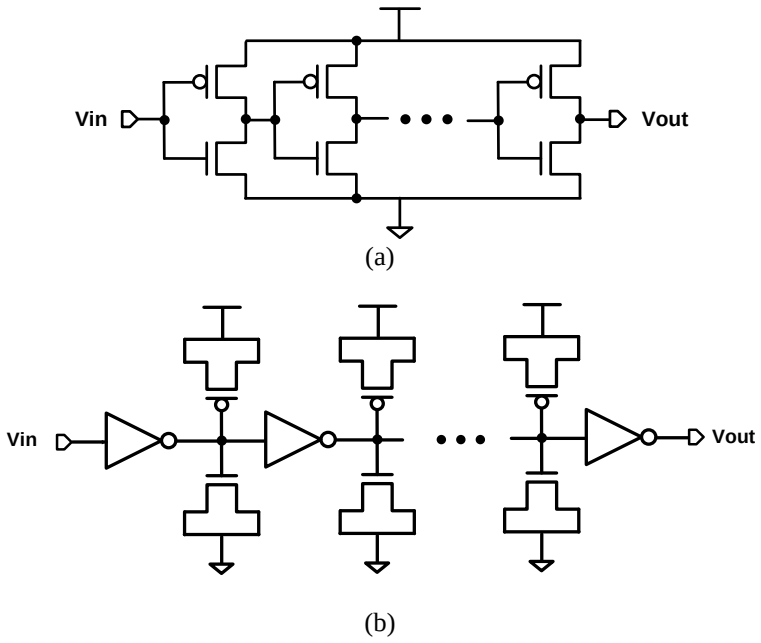


Fig. 3.3. (a) Cascaded inverter based delay element (b) and its variant which has additional capacitance at the intermittent nodes.

load capacitance. The load capacitance can be increased by adding additional gate capacitances by connecting the transistor gates at the inverter output nodes as shown in Fig. 3.3(b). The delay produced is directly proportional to the number of inverter stages.

Since the PMOS and NMOS transistors are never on simultaneously in steady-state operation, the static power consumption in an inverter occurs only due to leakage currents and is generally small. Most of the power is consumed during switching. This dynamic power consists of two components. The major component is due to charging and discharging of the load capacitance. During a low-to-high transition, half of the power is dissipated in the PMOS transistor and the other half stored on the load capacitance. During a high-to-low transition, the stored energy in the load capacitance is discharged and dissipated in the NMOS transistor. This power depends quadratically upon VDD and linearly upon load capacitance C_L and switching frequency f. The second component of dynamic power arises due to nonzero rise and fall times of the input signal, which results

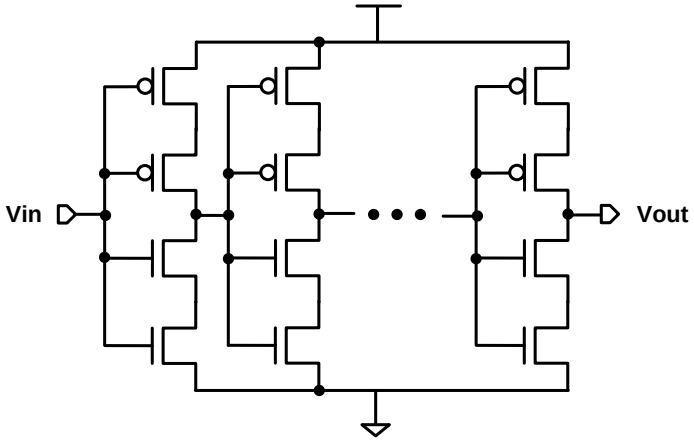


Fig. 3.4. Two transistors stacked cascaded delay element.

in both NMOS and PMOS transistors being on briefly.

Since the inverters are driven from rail to rail, they provide maximum drain current through the transistors thereby maximizing the charge removing ability of this delay element. This does not adversely affect the SET duration of the circuit.

3.1.3 Stacked Transistors Cascaded Inverter Based Delay Element

This delay element has m series-connected NMOS and PMOS transistors in its pull-down and pull-up networks, respectively. Fig. 3.4 shows the two series- connected cascaded inverters. The gates to all of these transistors are connected to the input. Increasing the fan-in not only increases the effective discharging/charging resistance, but also increases the gate and diffusion capacitances, which contribute to more capacitance at the input and output respectively. Further, it increases the delay of the fan-in gate by presenting it a larger load capacitance. Consequently, more delay per unit area may be obtained by using a generalized inverter with m series-connected transistors than by using a chain of m simple inverters. An m-transistor cascaded inverter requires 4mN transistors, where N is the number of stages.

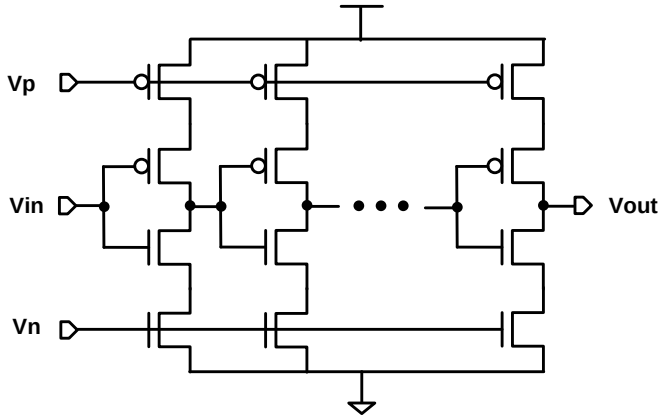


Fig. 3.5. Voltage controlled cascaded inverter delay element.

3.1.4 Voltage Controlled (Current Starved) Cascaded Inverter Delay Element

This delay element (Fig. 3.5) consists of a cascaded inverter pair with an additional series-connected NMOS transistor in the pull-down path and PMOS transistor in the pull-up path of each inverter which are controlled by global control voltages V_n and V_p respectively. There are three ways to change the delay of this circuit. First is by changing the transistor sizes. The second is by changing the fan-in similar to the series connected cascaded inverter case. The third way is to change the control voltages V_n and V_p. The delay is inversely proportional to the discharging drain current through the control transistor.

This delay element requires 4N transistors, where N is the number of stages. If V_n and V_p connections are shared the total transistors required will be less than $N. If the control voltages are below VDD for NMOS and above 0 for PMOS, the transistor drain current will be limited; thereby weakening the charge removing ability of this circuit. The SET duration will be worse than the simple cascaded inverter for the same amount of deposited charge. SET durations up to 3 ns (Fig. 3.1) have been measured with temporal latches using this delay element [36].

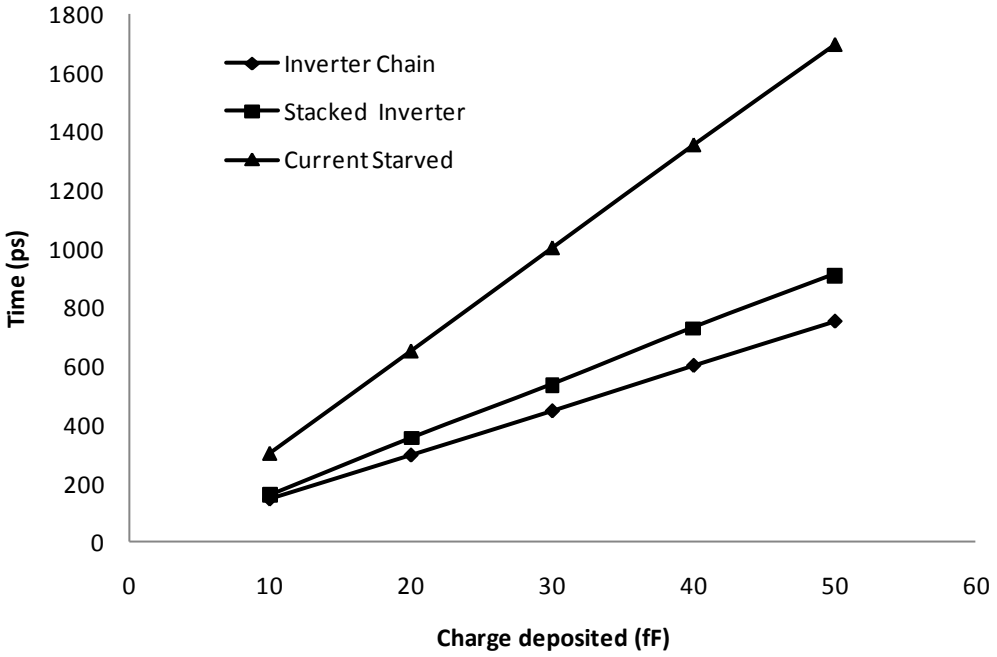


Fig. 3.6. Comparison of t_{SET} durations for the three delay elements.

3.1.5 Delay Elements Comparison

In this section the t_{SET} duration (the time taken by the circuit to remove the deposited charge), area occupied and energy dissipation of the three delay elements discussed in the previous sections are compared. The simulations and layouts are done in TSMC 90nm technology.

All three delay elements were designed to produce a delay of 140ps. This required having 10, 4 and 2 stages of cascaded, stacked and current starved inverters respectively. The t_{SET} durations of the three delay elements for deposited charges ranging from 10fF to 50fF in steps of 10fF are plotted in Fig. 3.6. As evident from the graph, the cascaded inverter delay element has the shortest t_{SET} duration as compared to the other two. Its t_{SET} duration is about 750ps for 50fF deposited charge. The current through the stacked inverter delay element is less than the inverter chain delay element due to series transistor resistance, resulting in its t_{SET} duration to be more than the inverter chain delay which is

TABLE 2.1

DELAY ELEMENTS AREA AND ENERGY/CLOCK CYCLE COMPARISON

Design	Area (μm^2)	Energy/clock cycle (fJ)
Cascaded Inverter	10.98	76.9
Stacked Inverter	7.13	63.1
Current Starved	3.84	44.5

about 900ps for 50fF deposited charge. For the current starved inverter which has bias voltages V_p and V_n of 0.8 and 0.4V respectively, the currents through the pull up and pull down transistors are severely limited, resulting in a large t_{SET} duration which is about 1.7 ns for 50fF deposited charge.

The delay elements' areas and the energy dissipation per clock cycle are shown in Table 2.1. Since the cascaded inverter based delay element has ten back to back connected inverters, it occupies the highest area. This is followed by stacked inverter based design having four stages and current starved design having two stages, which respectively occupy 35% and 65% less areas as compared to the inverter based design. For the current starved delay element design, the circuit area to generate bias voltages V_p and V_n are not included in the total area computation.

The energy/clock cycle of the cascaded inverter design is the highest due to ten charge/discharge cycles as it as ten stages. This is followed by stacked inverter and current starved designs which respectively dissipate 18% and 42% less energy as compared to the cascaded inverter design. Although the current starved inverter design has only two stages, it dissipates 60% energy of the cascaded inverter design due to the excessive crow bar current.

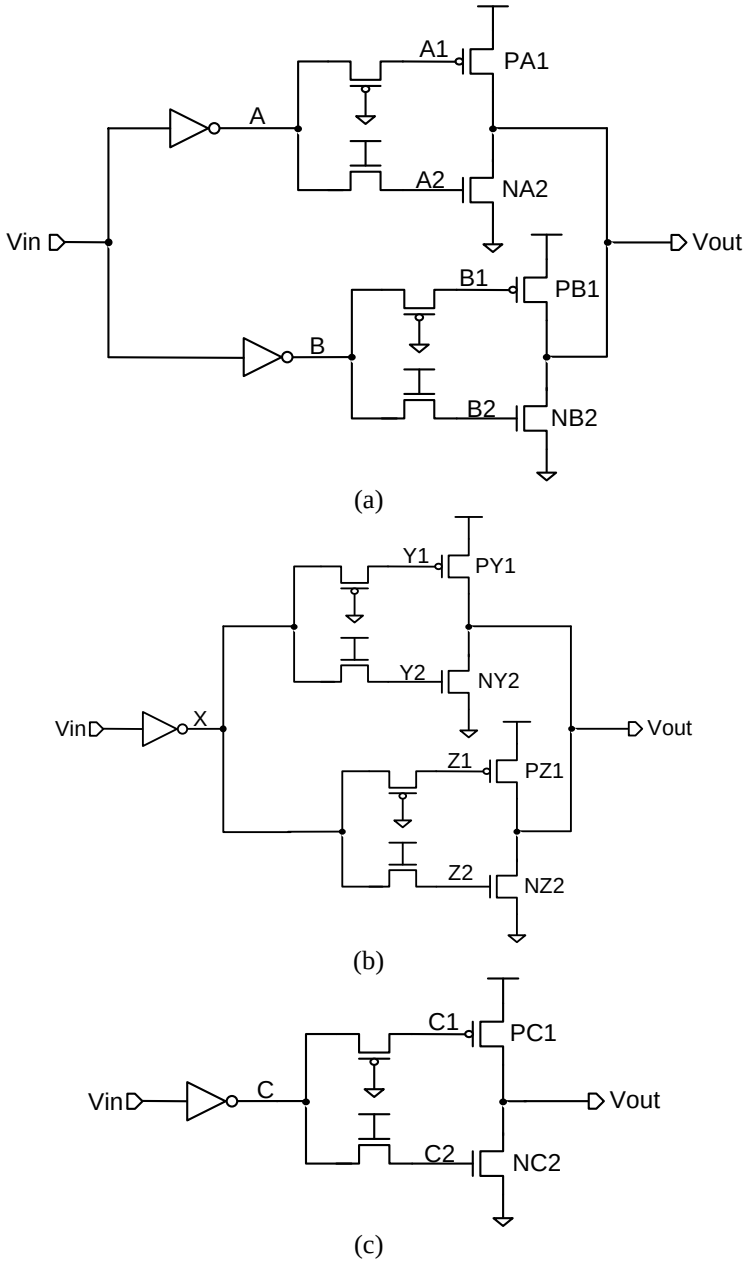


Fig. 3.7. Proposed delay elements (a); its variant (b); and without dual redundancy (c).

3.2 Proposed Delay Element

It was seen that in the current starved inverter design t_{SET} durations were greater than 1 ns. These becomes the limiting t_{SET} duration on the IC. In this section a dual redundant delay element is proposed which does not adversely affect the worst-case SET duration on the IC. Each redundant element is slowed by reduced gate overdrive, and the

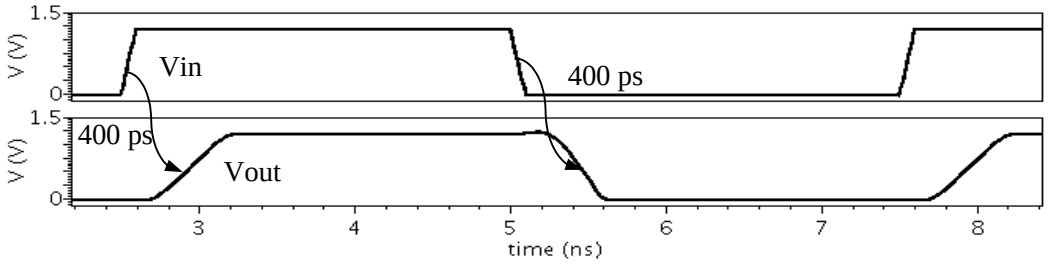


Fig. 3.8. The proposed delay element transient response producing a delay of 400 ps.

lower swing of the drain nodes provides power savings.

3.2.1 Circuit Design

The proposed delay element circuit is shown in Fig. 3.7(a). This design has two identical redundant paths from the input to the output, evident as inverter output nodes A and B. The gate of the PMOS pass transistor is connected to the low supply rail (V_{SS}) and the gate of the NMOS pass transistor is connected to high supply rail (V_{DD}). Hence, both pass transistors are always turned on.

Low swing is achieved at the output of the pass transistors, i.e., at nodes A1, A2, B1 and B2, since it is nominally V_{DD} to V_{TP} for the PMOS path and V_{SS} to $V_{DD} - V_{TN}$ through the NMOS path. These low swing nodes save power and are slow, additionally causing node V_{out} to be driven slowly by transistors PA1, NA2, PB1 and NB2. Fig. 3.7(b) shows a variant that has one less inverter, further reducing power dissipation and Fig. 3.7(c) shows the delay element without redundancy. Fig. 3.8 shows the transient response of the delay element and its variant, whose pass transistors are sized to produce a delay of 400 ps.

3.2.2 Power Reduction

The dynamic power in a delay element is directly proportional to the number of

driven nodes, their capacitances, and the voltage swing on those nodes. Hence, minimizing the power requires reducing these circuit parameters. The proposed delay element has only two diffusion nodes, A and V_{out}, for each path. The capacitance seen at node A is the sum of the diffusion capacitances of the two driving transistors and the pass transistors. The latter have reduced swing. The inverter and pass transistor lengths are increased to increase their delay, but PA1, PB1, NA2, NB2 are minimal so that SET duration due to charge collected at the output does not result in long SET durations at the output node V_{out}.

3.2.3 SET Tolerance

As discussed earlier, the delay elements comprise most of the temporally hardened FF area. With such a large physical cross-section, the delay element must thus itself cause SETs no worse than the standard logic, whose SETs it filters. In the proposed delay element, this hardness is achieved through the dual redundant delay paths. Charge collection occurs across reverse biased source/drain diodes in the MOS transistors. Hence referring to Fig. 3.7 (a), node A1, a P-type diffusion, can only be pulled high, and conversely, node A2, an N-type diffusion, can be only be pulled low, while nodes A and B can be pulled in either direction. A nodes and B nodes are spatially separated, so they cannot simultaneously collect charge from a single impinging particle.

To demonstrate the efficacy of the redundant delay paths, we first examine the case where the delay element has no redundancy (see Fig. 3.7(c)), i.e., it has only one path from input to the output, where node C is driven low by a radiation strike. Node C2 is pulled low through the pass transistor and turns off transistor NC2 and turning on PC1, driving V_{out} high for the SET duration (see Fig. 3.9(a)). Moreover, if the strike is at node

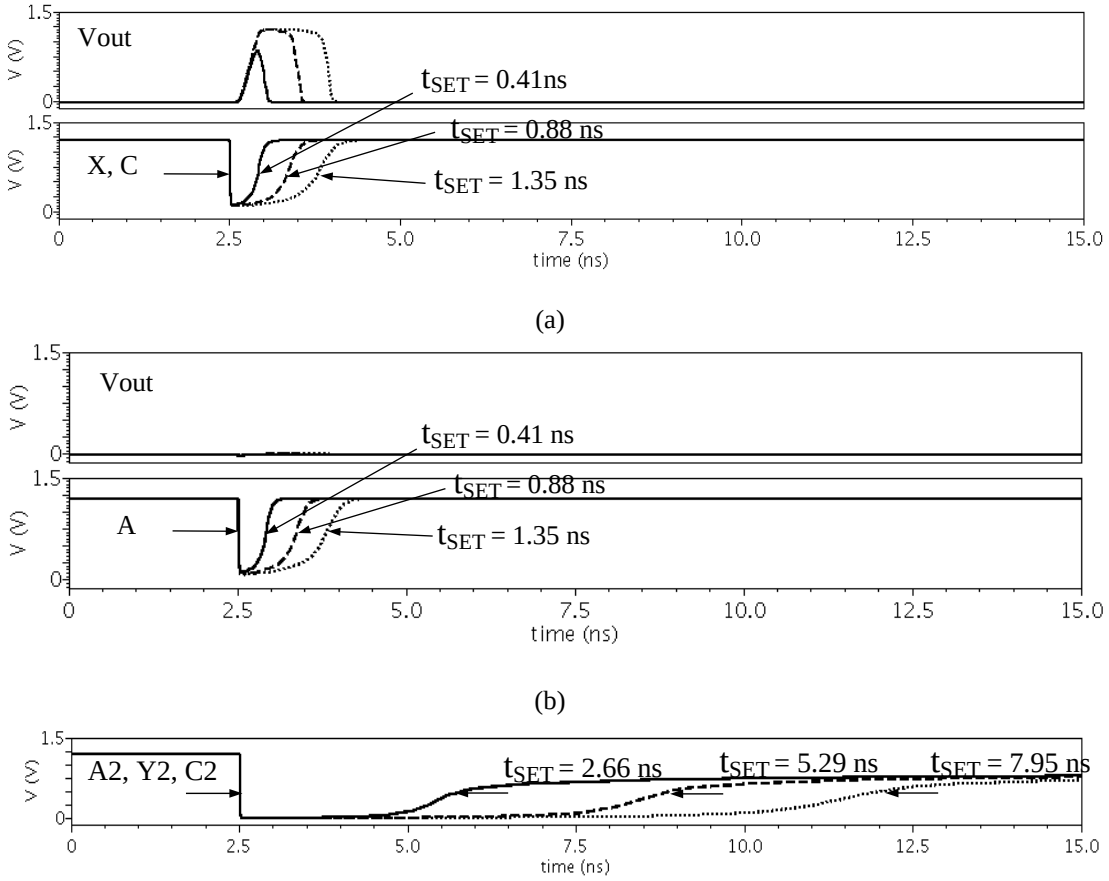


Fig. 3.9. Effect on delay element output due to simulated SETs of various LET: (a) on nodes X and C and (b) on node A.(c) SETs of same total charge on nodes A2, Y2, and C2. The redundancy eliminates the long SETs within the delay elements, which plagues current starved delay circuits.

C2, the charge must be removed via the low swing path, resulting in a much longer SET duration than can occur in the standard (full swing) logic.

In the proposed delay element, the output node V_{out} is driven by redundant parallel pull-up and pull-down transistors PA1, PB1 and NA2, NB2, respectively (see Fig. 3.7(a)). If a collected radiation strike charge pulls node A low and turns off transistor NA2, the output node is held by transistor NB2. A contention state does result between PA1 and NB2, but this is only during the SET. Fig. 3.9(b) shows node A pulled low by collected charge producing three different SET durations, and the output node remains

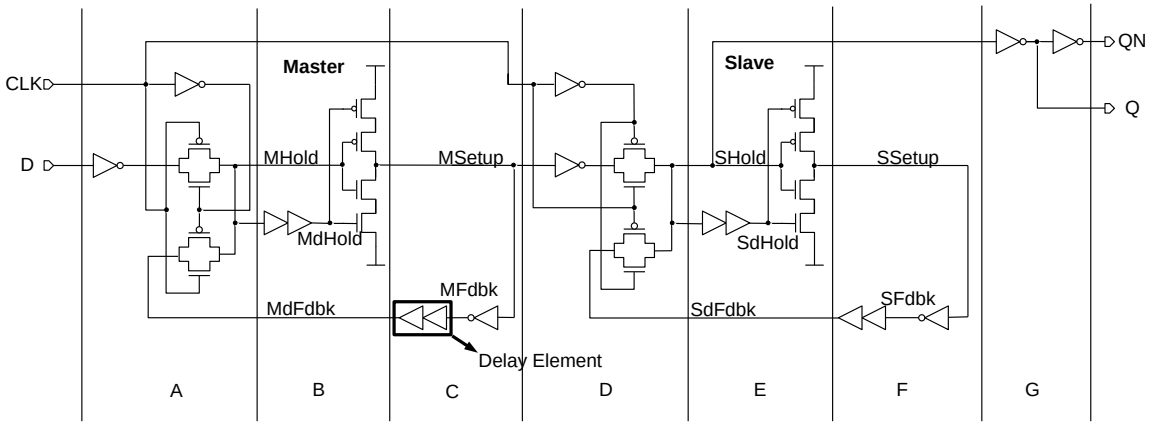


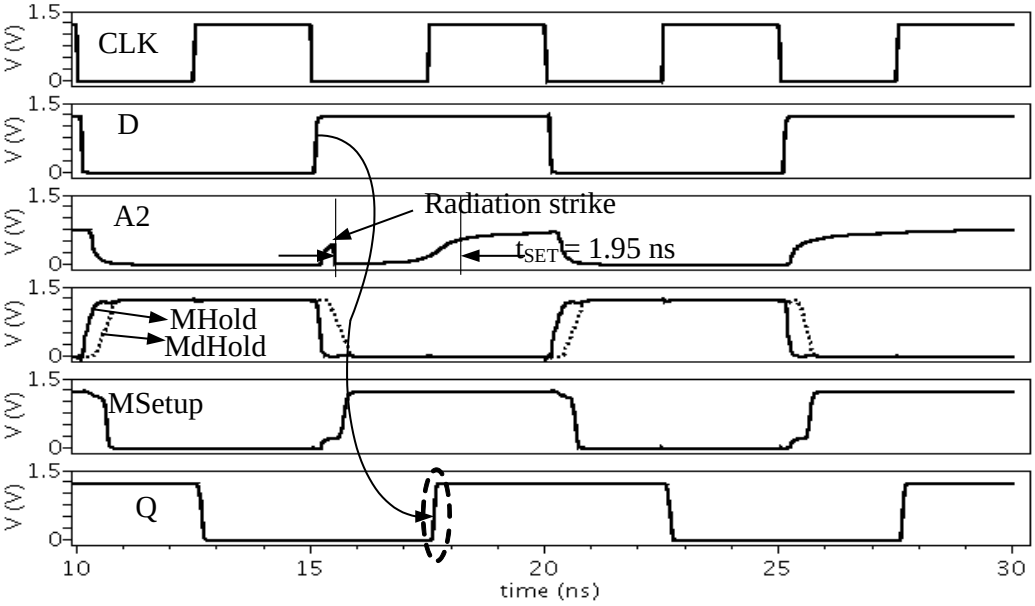
Fig. 3.10. Temporal FF [35] schematic using the proposed delay element.

static for the SET duration. Since node A2 can only be pulled low, a strike on node A2 turns transistor NA2 off, but V_{out} remains strongly driven by NB2. Just as in the current starved inverter case, nodes A1, A2, B1 and B2 have very slow SET charge dissipation, as shown in Fig. 3.9(c). However, since there is a redundant path, the resulting very long SET duration does not significantly affect the delay element output timing. The proposed delay element thus provides a long delay without adversely affecting the worst-case SET duration of the IC.

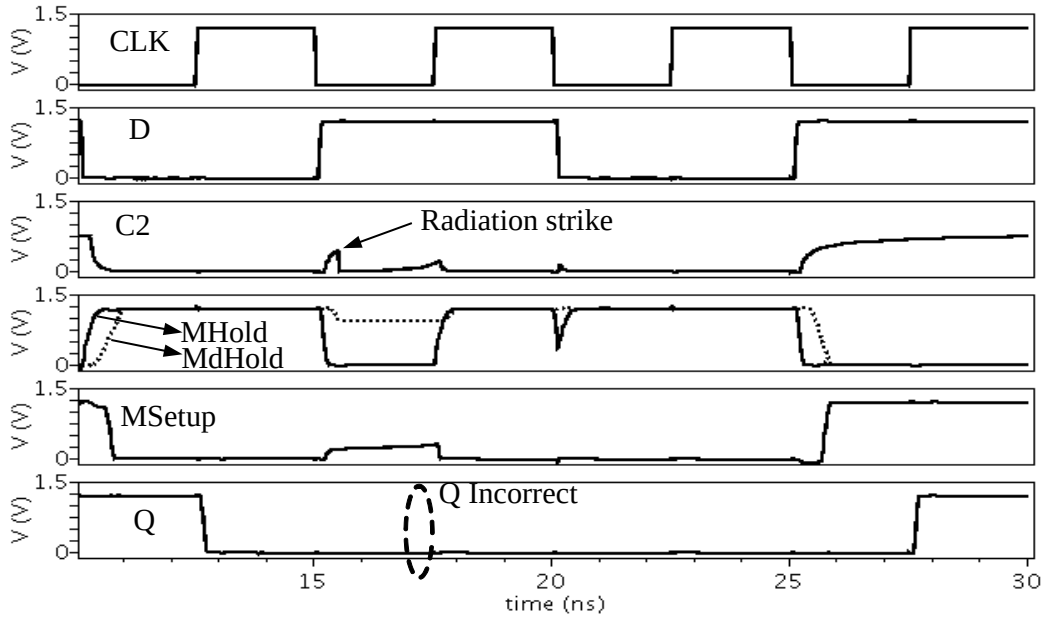
Referring to the alternate design in Fig. 3.7(b) an SET driving node X low, transistors NY2 and NZ2 are turned off and the output is held high for the duration of SET without contention. The effect on its output will be the same as an SET at the input (see Fig. 3.9(a)) as the transient propagates to the output.

3.3 Delay Element Impact on a temporal Flip-Flop

In this section, the proposed delay element is used in a temporal flip-flop to assess its power and size impact. The baseline FF [35] uses cascaded inverter delay elements. Both delay elements produce the same 400ps delay. Fig. 3.10 shows the temporally



(a)



(b)

Fig. 3.11. Waveforms showing the effect of two radiation hits on the MSFF using (a) the proposed delay element and (b) one lacking redundant paths at the low-voltage swing, current starved nodes.

hardened FF circuit.

3.4 Flip-flop SET Tolerance

To compare the FF SET mitigation, SETs depositing the same total charge are induced on each of the two flip-flops as shown in Figs. 3.11(a) and 3.11(b) for the

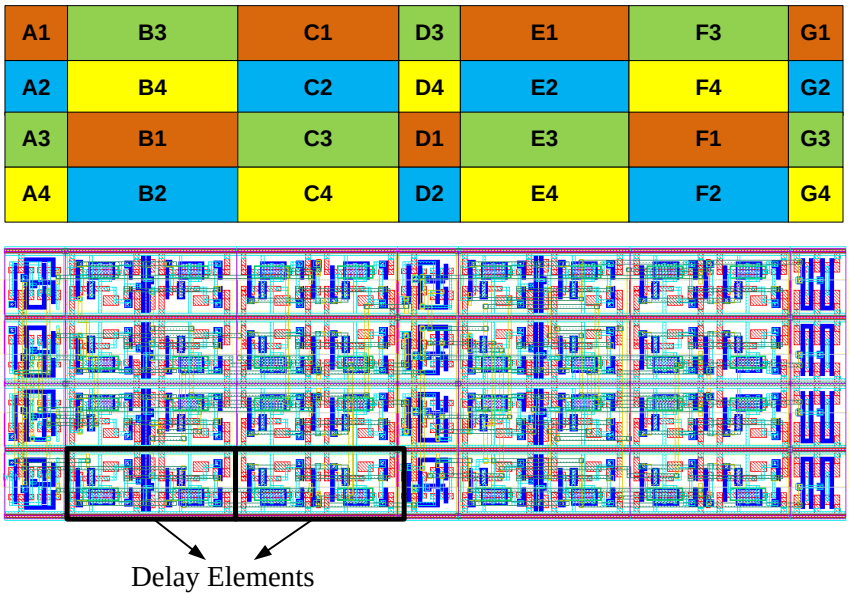


Fig. 3.12. Layout arrangement of the sub-blocks of Fig. 3.10 illustrating the constituent cell interleaving.

proposed delay element (Fig. 3.7(a)) and one without redundant paths (Fig. 3.7(c)) respectively. As shown in Fig. 3.11(a), in the FF using the proposed delay element, node MdHold closely follows node MHold. Referring to Fig. 3.11(a), at 15.5 ns both the values on nodes MHold and MdHold are low and hence the C-element sets the node MSetup high. Thus, output node Q is able to capture a correct value at the rising edge of the clock at 17.5 ns. Without the redundancy, the long SET creates a fail, which is due to the delay element itself, producing abnormally long SETs when these nodes are struck, indicated by the oval on the last waveform in Fig. 3.11(b).

3.5 Flip-flop layout

Upset due to multi-node collection can be avoided by interleaving the constituent circuits across four standard cell rows [35], [39], [40]. This ensures that nodes which could cause upset due to multi-node collection are separated by at least one cell row. It was alleviated in [41] by simply adding empty space between the nodes, which essentially wastes the IC area.

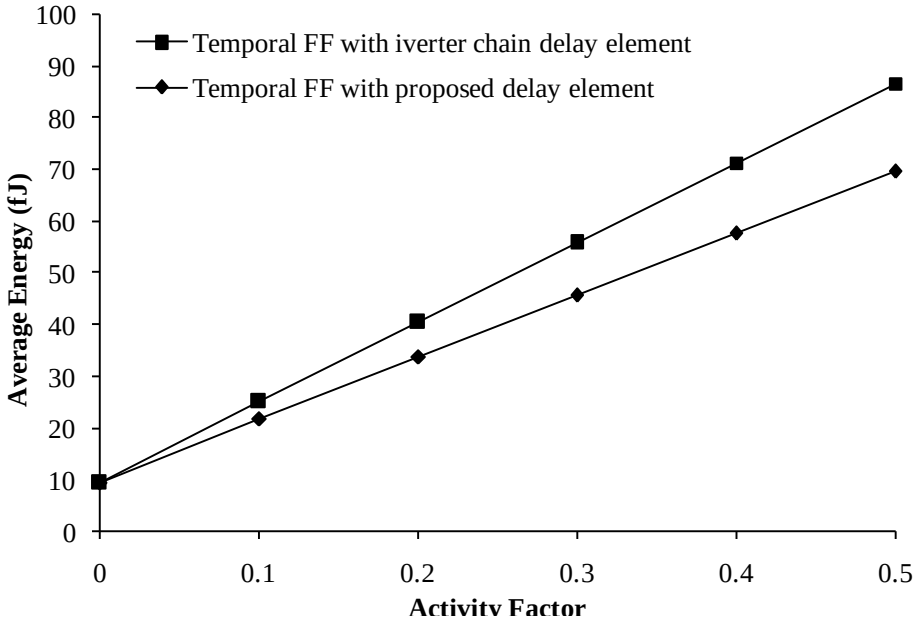


Fig. 3.13. Comparison of average energy consumption per clock cycle of the MSFF [35] using both the inverter chain and the proposed delay element.

To determine the resulting amenability to auto place and route (APR), the FF is implemented in the 130 µm bulk CMOS process. The layout follows [40] interleaving four FFs in a multi-row, multi-bit cell (see Fig. 3.12). It occupies an area of 727 μm^2 (48.64 µm × 14.96 µm)

3.5.1 Power Comparison

As seen from Fig. 3.13, the proposed delay element saves energy over the same design using cascaded inverters. At activity factor (α) = 0.5 the baseline (cascaded inverter delay) design dissipates 86.81 fJ per clock cycle while the one with the proposed delay element dissipates 69.74 fJ per bit. Thus the proposed design dissipates 19.6% less power than the baseline circuit using inverter chain delay element.

3.6 8051 Implementations

In the section 3.2, a low power, SET tolerant delay element was presented. In this section, the temporal FF [35] using both the proposed and the cascaded inverter delay elements are used in implementing a 8-bit, 8051 with 128 bytes of random access memory (RAM) designed in the TSMC 130nm bulk CMOS process to compare area, speed and power characteristics. All of the 128 bytes RAM is synthesized using FFs.

3.6.1 Synthesis

Encounter Library Characterizer (ELC) was used to characterize the FFs using layout extracted netlists to produce the liberty timing files. The setup and hold times were modified to force an SET hard setup time of 800ps for the 400ps SET duration.

Both 8051 versions use synchronous reset, 8 bit data, 128 byte RAM and 512 byte ROM. Cadence RTL Compiler (RC) was used for synthesis. The combinational standard cells used are the standard foundry 130 nm standard cell library, which are not TID hardened. To minimize power, the clock gating capability in RC was enabled, inserting clock-gaters in the clock trees. The timing for both 8051 versions is exactly the same as both designs use the same FF design except that one uses the proposed and the other uses the cascaded inverter delay elements, both of which produce the same delay. The maximum clock frequency at the nominal 1.2V V_{DD} for both designs was determined to be 240 MHz, using Synopsys Primetime and post-layout extracted netlists.

3.6.2 Auto Place and Route (APR)

Both designs utilized Cadence Encounter as the APR tool and followed the standard (commercial flow) placement procedure. The foundry 130-nm process has eight

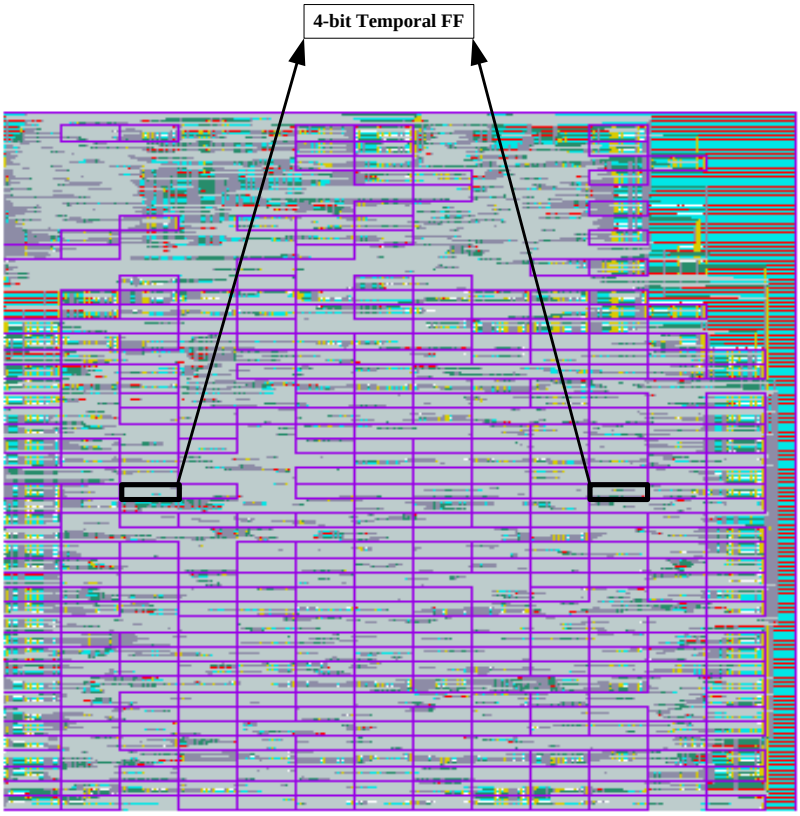


Fig. 3.14. 8051 layouts of the two temporal versions. The data memory, which uses master-slave flip-flops, dominates the overall size.

metal layers, with even numbered metal layers running vertically and odd numbered metal layers running horizontally. M2 to M6 were used for routing, with M7 and M8 used only for top level power.

3.6.3 Layout

Fig. 3.14 shows the final layout of both 8051 designs. Since the two temporal FF versions have the same circuit design but different delay elements constrained to fit in the same FF layout area, the overall 8051 areas are exactly the same. The highlighted rectangles in Fig. 3.14 show the cell boundaries. The standard cells areas for both implementations are shown in Fig. 3.15. Table 3.1 shows the total standard cells utilization and metal densities. Of the total 8051 cell area, the FFs occupy 73%.

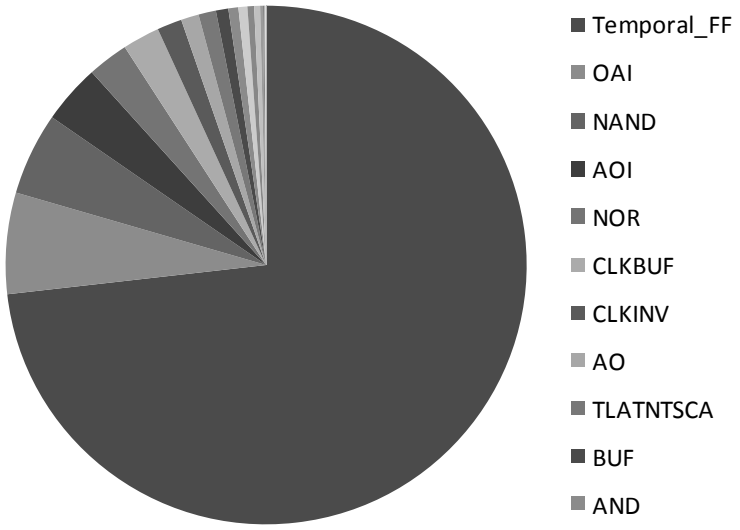


Fig. 3.15. Standard cells areas in both temporal designs

TABLE 3.1

STANDARD CELLS AREAS FOR BOTH TEMPORAL DESIGNS

Design Information	Temporal
Total Std Cells	10515
Total Area (μm^2)	0.478
Cell Density (%)	76.42
Total M2 routing density (%)	11.9
Total M3 routing density (%)	17.2
Total M4 routing density (%)	20.4
Total M5 routing density (%)	23.7
Total M6 routing density (%)	12.3

3.6.4 Comparison

3.6.4.1 Timing and Area

TABLE 3.2

COMPARISON OF AREA, TIMING AND CLOCK FREQUENCY

FF Setup time (ns)	FF Hold time (ns)	Critical path Delay (ns)	Clock Frequency (MHz)
1.131	0.076	4.16	240

Table 3.2 shows the setup and hold times of both temporal designs as computed by Primetime. The final layout area of both designs is 0.478 μm^2. The two temporal FFs with different delay elements have the same timing as both use the same circuit design and have the same drive strength. The critical path delays that determine the clock period are also shown.

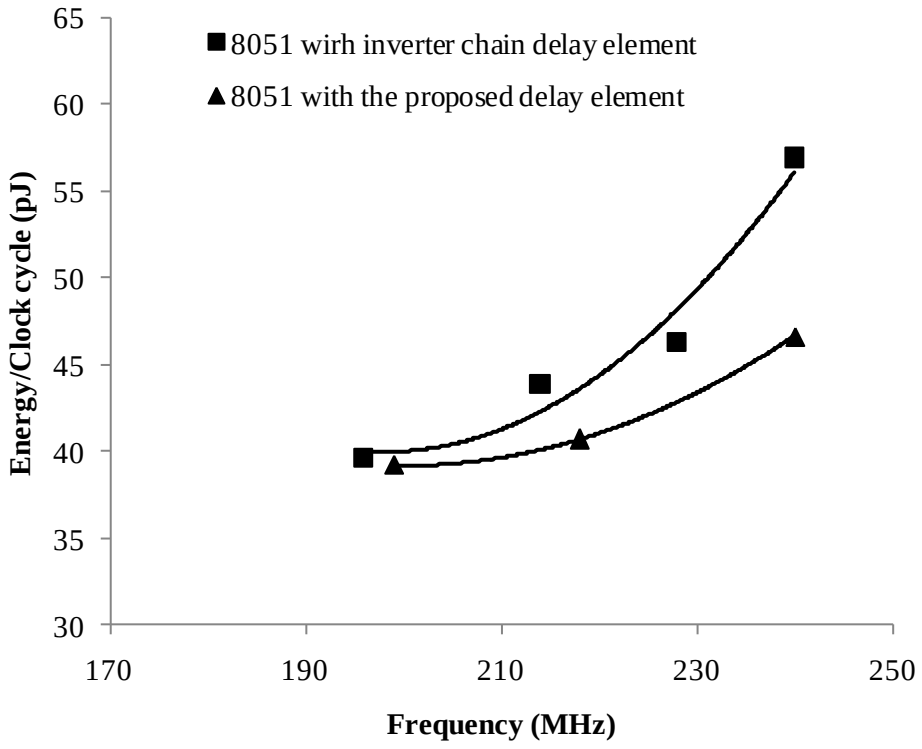


Fig. 3.16. Average energy/clock vs. maximum operating frequency for the two 8051 implementations. Each curve has its maximum at 1.2V V_{DD}, and each point is separated by 100 mV

3.6.4.2 Power

A program to calculate the Fibonacci series, requiring approximately 5000 clock cycles, was used to compare the power dissipation of the designs, using circuit simulation (Cadence Ultrasim) of fully extracted netlists. As the supply voltage is scaled down, the FF dead time increases, which decreases the maximum operating frequency. This effect is exacerbated as the delay element's delay increases, very rapidly for the low-power delay element. Fig. 3.16 shows the maximum operating frequency versus energy per clock with V_{DD} scaled down from 1.2 V until the FFs are unable to latch the correct input data. The inverter based and the proposed low power designs operate correctly to 0.9 V and 1.0 V, respectively. Both designs operate at a maximum frequency of 240 MHz (Table 3.2). From Fig. 3.16, it can be seen that the energy per clock by both temporal designs are 56.89 pJ/clock and 46.63 pJ/clock respectively. Hence the 8051 using the proposed delay element dissipates 18% less power than the cascaded inverter based delay element.

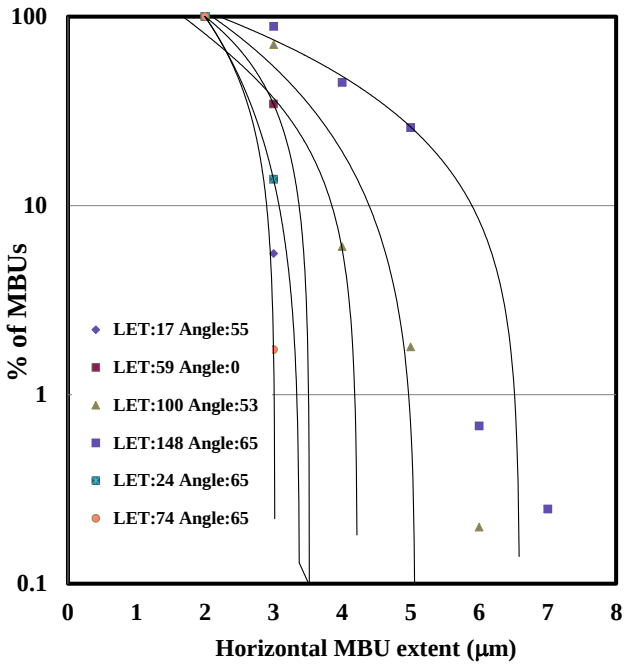
CHAPTER 4

METHODOLOGY TO OPTIMIZE CRITICAL NODE SEPARATION IN HARDENED FLIP-FLOPS

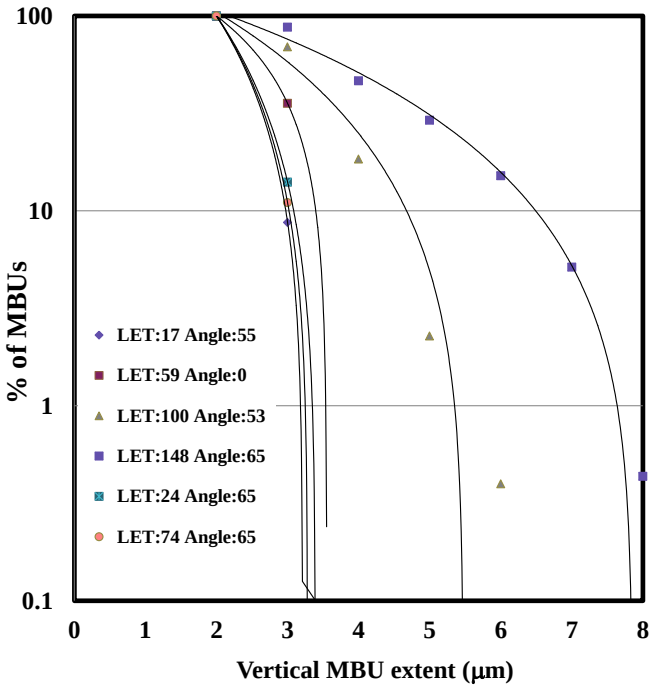
From discussions in chapter 1, we understand that radiation hardening is a requirement for microelectronic circuits used in aerospace applications as they are prone to radiation induced upsets from high altitude neutrons and ions. The most common method to harden VLSI circuits is to use hardened FFs. In chapter 2, different FF hardening techniques were discussed. The design of these FFs is made more difficult with increasing multi-node charge collection (MNCC) in advanced scaled fabrication processes, which requires that charge storage and other sensitive nodes be separated so that one impinging radiation particle does not affect redundant nodes simultaneously. In this chapter we describe a correct by construction design methodology to determine a-priori which hardened FF nodes must be separated, as well as a general interleaving scheme to achieve this separation. We apply the methodology to radiation hardened flip-flops and demonstrate optimal circuit physical organization for protection against multi-node charge collection.

4.1 Multiple Node Charge Collection

Soft error susceptibility increases as circuits areas diminish the critical charge required for an upset while the charge deposited by an ion is unchanged, since it is based on the physics of charge deposition and collection [58][59]. The likelihood of multiple node charge collection (MNCC) has increased dramatically with fabrication process scaling, since circuit nodes become more closely spaced.



(a)



(b)

Fig. 4.1. Experimentally measured SRAM multiple node upset extents in the (a) horizontal and (b) vertical directions.

4.1.1 Experimental Analysis

MNCC results on a 90-nm SRAM designed with logic rules are shown in Fig. 4.1.

The results are obtained after subjecting the SRAM test chip to ion broad beams at different LETs and orientations at the Texas A&M cyclotron as indicated in the figure. SRAM results can provide useful guidance for the hardening of other circuits. In particular, MNCC is easily analyzed using SRAMs. Moreover, the restoring current drive is similar to that in modern FFs which have NMOS feedback node transistor sizes very close to those in the logic rule SRAM cell: SRAM NMOS transistor sizes are W/L = 190/100 nm, vs. 200/100 nm in the FFs.

Referring to Fig. 4.1, the horizontal (along the N-well) and vertical (across the N-well) simultaneous multiple bit upset (MBU) extents, due to MNCC are shown in Figs. 4.1(a) and 4.1(b), respectively. Note that low LET_{EFF} vertical extents are nearly all less than two standard cell heights (3.92 μm).

4.1.2 MNCC Impact on FFs

With a high likelihood of MNCC, SEU hardness requires placing storage nodes far enough apart so that simultaneous upset of such critical nodes is unlikely. Note that a single strike at the right solid angle (directly passing through the nodes) can always disturb multiple nodes—separation makes such strikes, which can impinge at any angle, less likely, but not impossible. Some designs have struggled through multiple iterations of design and broad beam testing to ensure adequate hardness [33]. Thus, a design method to analyze the hardness and provide guidance to the FF physical design would be very helpful.

4.2 Critical Node Separation Methodology

4.2.1 Interleaving Circuit Blocks to Avoid MNCC

The FFs we discussed in chapter 2 all utilize circuit redundancy and/or temporal filtering. In prior work, MNCC has been addressed by grouping the sensitive nodes and separating them. Warren, *et al*., utilized a brute-force approach, systematically increasing node separation (adding unused space) as indicated necessary by iterative design/beam testing results [33]. Providing larger critical node separation, while avoiding wasted area has been accomplished by interleaving the constituent circuits of multiple FFs [35][39]. In such multi-bit designs, the overall area is the same as the regular FF area, but additional metal routing is required. Excellent hardness is obtainable. However, such multi-bit FFs do slightly complicate the ASIC design methodology.

4.2.2 SET Upset Simulation

Radiation induced collected charge at a node gives rise to a SET or a SEU. Our goal is to determine the upset sensitivity of the FF nodes and their vulnerability to MNCC. We perform a rigorous analysis on the circuit nodes by simulating node upsets by inducing temporary voltage reversals first on all charge collecting FF nodes and then on all possible nodes pairs (to determine MNCC vulnerability). In this manner the effects of both SETs, caused by collection at internal clock or reset connected gate diffusions, as well as transients to the associated input, as well as SEUs, caused by collection at the storage nodes are analyzed. Note that an apparent SEU can be due to an SET—an example is inadvertent transfer from the slave to the master latch due to a clock node transient internal to the FF cell.

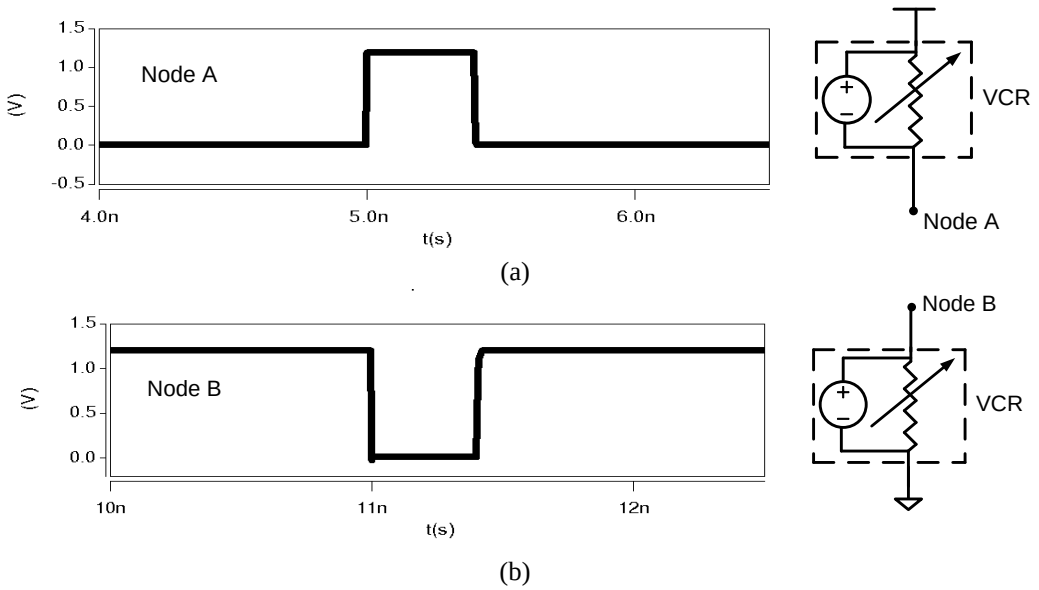


Fig. 4.2. Voltage Controlled Resistor (VCR) induced (a) high and (b) low SETs on the circuit nodes.

SETs are modeled using a SPICE voltage controlled resistor (VCR) element. The VCR is set to have negligible impedance when asserted and very high impedance otherwise. A SET-high pulse is generated by the VCR driving a node to V_{DD} and similarly, a SET-low pulse is generated by driving the node to V_{SS} (see Fig. 4.2).

4.2.3 Simulation Based MNCC Collection Analysis

Fig. 4.3 illustrates the proposed methodology. All transistor diffusions can collect charge except for those connected to power rails. We begin by identifying these non-power diffusions. Nodes are grouped based on the following heuristics (see Fig. 4.4): First, all hardening element output nodes should be in different groups. In Fig. 4.4, group C has C-Element which is a hardening element. Other hardening elements include the outputs of delay, majority voting circuits, or DICE nodes. Second, nodes that are connected to each other via combinational logic should be in the same group. This follows intuitively—if one of the early stage nodes is hit, it may affect others, subsequent in the logic paths, with minimal delay. Thus, they may be treated as one "super-node". In

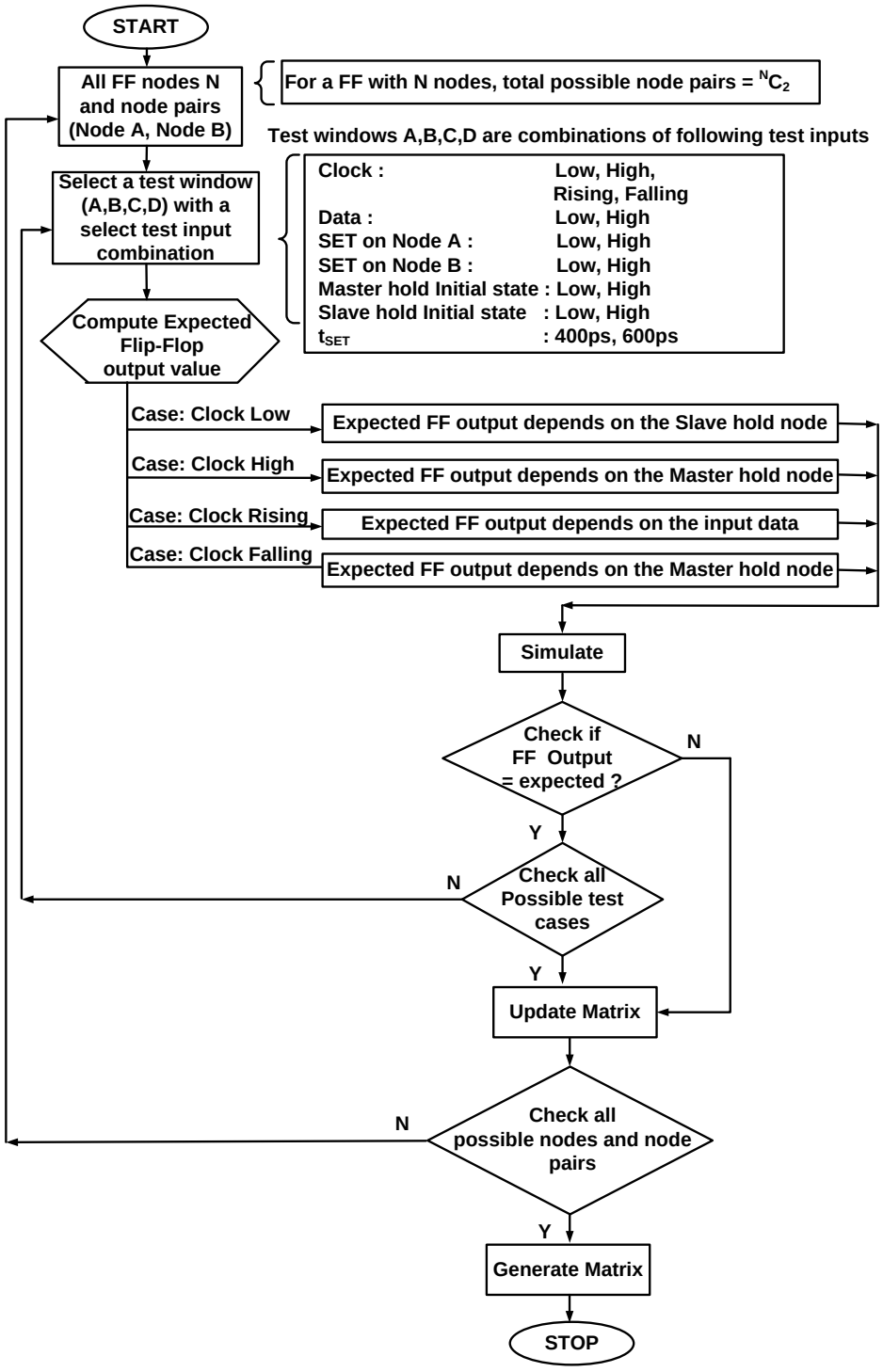


Fig. 4.3. Flowchart illustrating the methodology

Fig. 4.4, nodes in groups A, B, and D contain combinational logic and fall into this case.

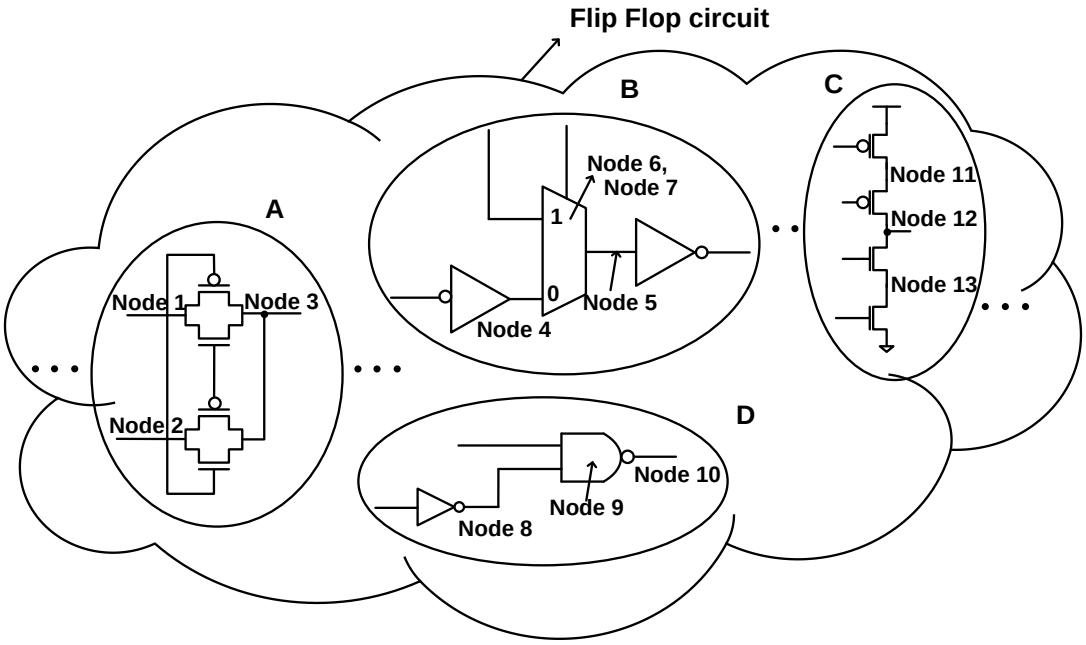


Fig. 4.4. Circuit node grouping in a hardened FF. Nodes connected by combinational logic are grouped together.

We begin the analysis by simulating node upsets on all FF nodes (N nodes). To account for all possible flip-flop states when a strike happens, the node flips induced at each node are induced at clock rising, clock high, clock falling and clock low as shown by windows A, B, C, D respectively (Fig. 4.5 (a)), for both the input logic states. The FF output depends on the master and slave hold nodes states, so for each of these conditions the master and slave hold nodes are initialized to each of the possible logic values as well. For each simulation run, the expected output for that case is computed by simply not inducing any upsets. Following the basic conditions shown in Fig. 4.5 (a), each node pair is simulated in each of the possible cases. An upset is flagged for runs with node flips that mismatch expected values.

The analysis approach (pseudo-code) is:

for each node (N nodes)

  for each clock states (low, rising, high, falling)

    for each data inputs (logic 0, logic 1)

      for each SETs on Node A (low, high)

        for each Master latch hold node (logic 0, logic 1)

          for each Slave latch hold node (logic 0, logic 1)

            Run HSpice simulations

              Record the Flip-Flop stored state

if (FF output != Expected?)

                Update node matrix showing upset (fail)

else

                Update node matrix showing no upset (pass)

The analysis is extended to MNCC impact by simulating simultaneous temporary node voltage reversals on all of the possible collecting node pairs (Fig. 4.5 (b)). We select one pair at a time and induce SETs. Since nodes may collect positive or negative charge, i.e., for P-type or N-type diffusions, respectively, for each clock and data condition, all four combinations of node reversals are induced on node pairs, i.e., low-low, low-high, high-low and high-high A flip-flop containing N nodes has ${}^{N}C_{2}$ total node pairs, changing the outermost loop to

  for each node pair A & B (N choose 2 node combinations)

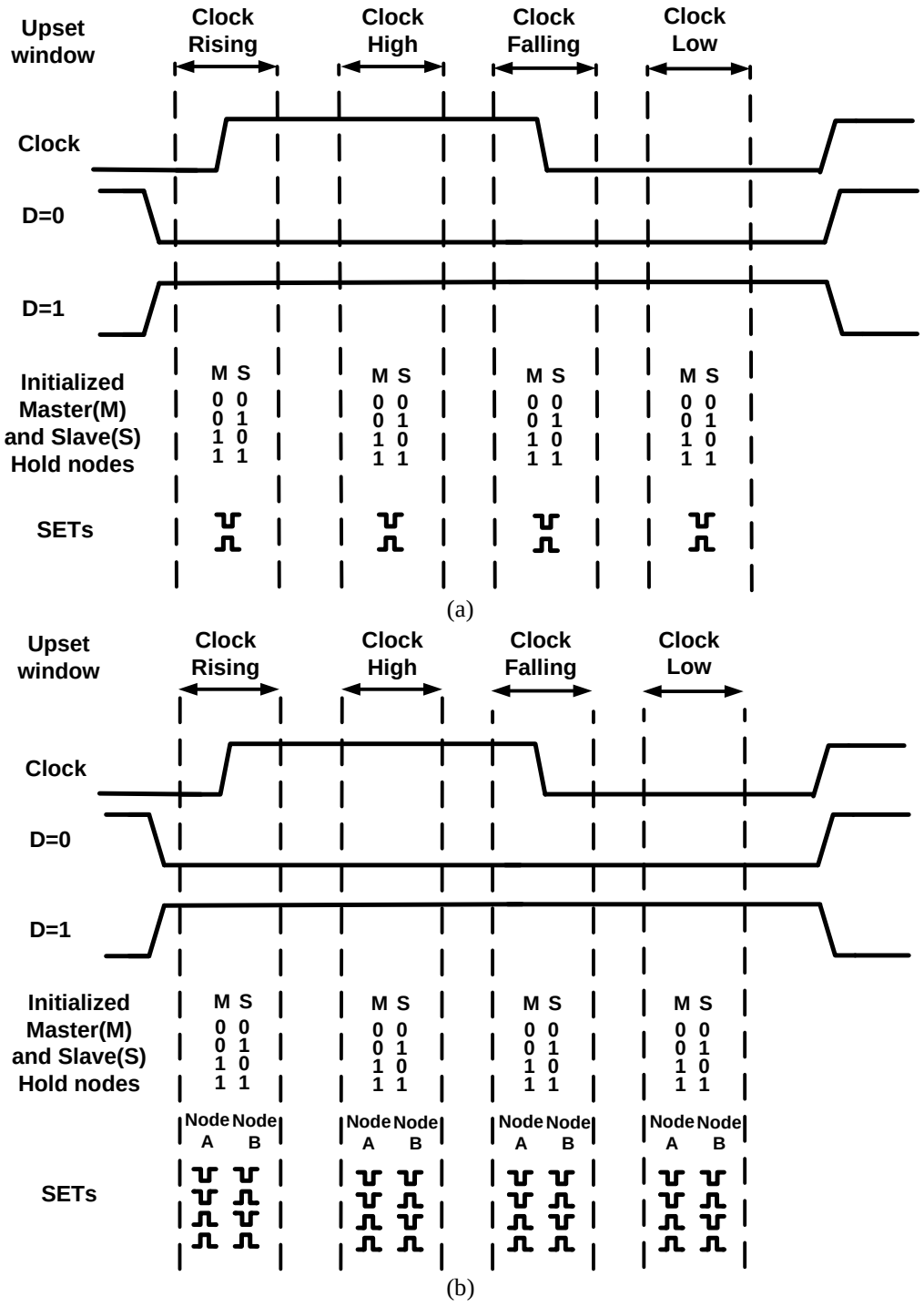


Fig. 4.5. SET simulations on (a) all FF nodes and (b) node pairs at windows A, B, C and D for both data inputs and for the master and slave nodes initialized to the stated values

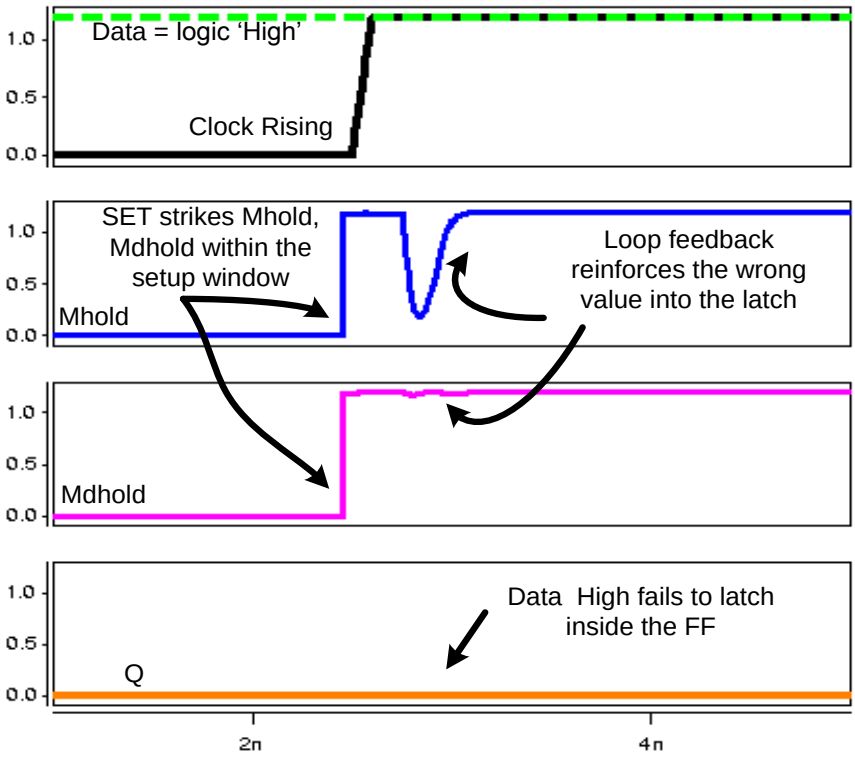


Fig. 4.6. Waveforms showing data failing to capture the correct value when two high SETs are induced on nodes Mhold and Mdhold of a temporally hardened FF at 2.5 ns

Fig. 4.6 illustrates an example hardened MSFF failure to capture the expected output due to MNCC. For this FF, the output value Q is the compliment of MHold node. The FF input data is a logic one and hence after the clock rising edge, the correct output at Q is also a logic one. A high going, i.e., logic zero to logic one, charge collection induced dual SET combination on nodes MHold and MdHold at 2.5ns drives both Mhold and MdHold high, latching a zero at Q. The master latch pass transistors briefly try to restore MHold, but the loop feedback pushes it back to the wrong state as evident in the figure.

The results of the node pair voltage upset simulations can be visualized as a lower diagonal matrix as shown in Fig. 4.7. A simulated but passing node pair (i.e., where the simulated MNCC caused no upsets) is marked in grey and failing node pairs (i.e., where

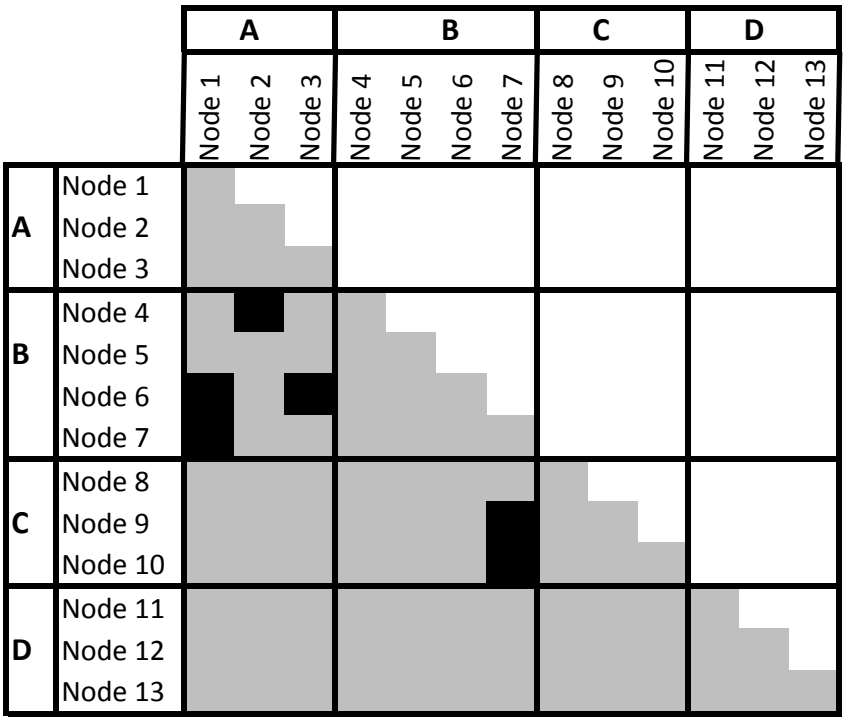


Fig. 4.7. Node matrix showing failing node pairs marked in black and the passing node pairs marked in grey

the simulated collected charge upset the FF state) are indicated in black. The upper diagonal is symmetric, so need not be simulated. Squares represent the circuit groups, i.e., nodes that are laid out together. The following information can be obtained from the matrix:

- Since nodes in the same group may affect each other via combinational logic paths, and thus may presumably be physically laid out in close proximity, squares along the diagonal should not have any failures. Failures along the diagonal indicate nodes should be moved to other groups or another grouping should be formed.
- Non-diagonal groups can have failures. The coincidence of failures indicates which circuit groups should be separated from each other as they are prone to MNCC defeating their redundancy. For example, referring to Fig. 4.7, groups A-B and B-C may not be adjacent.

- Group pairs which do not have failures may be adjacent. Again referring to Fig. 4.7, groups A-C, A-D, B-D and C-D are examples of legal adjacencies.

4.2.4 Node Group Ordering

Based on the information from the matrix, the circuit blocks ordering in the layout can be determined. The total possible group combinations for N groups is N!. A script has been written to find N! combinations and eliminate groups, which have illegal adjacencies, given the group names and the illegal adjacencies. The script gives the groups which have legal adjacencies. Of these, one which requires the least inter group metal routings will be the most efficient interleaving for the circuit's layout.

The table in Fig. 4.7, has four groups and hence the total possible group combinations are 4!/2 = 12 (since the matrix is symmetric across the diagonal). Of these group pairs, A-B, B-C and A-C are illegal adjacencies. Hence all the group combinations with these adjacencies will be eliminated. The legal adjacencies obtained after running the scripts are ADCB, BADC and BDCA. Of these groups, the group with the least inter group routings will be the most efficient layout.

4.3 Application to Radiation Hardened FF Designs

In this section the critical node separation methodology is applied to three radiation hardened FFs whose functionalities were discussed in chapter 2. First is the commonly used DICE FF, second is the classical temporal FF proposed by Mavis *et al*., and lastly the temporal FF requiring fewer delay elements proposed by Matush *et al*. All simulations are done using post layout extracted spice netlists.

4.3.1 DICE Protected Master Slave FF

Fig. 4.8 shows the DICE flip-flop [32] circuit and node grouping. The master and slave latches are identical, so only the master internals are shown. Since the DICE latch has four storage nodes, each has to be in different group. Each latch is divided into six groups as shown.

The DICE is not hard to upset clock inputs, but with proper layout is hard to MNCC in the hold mode. Thus, node reversals were induced only within the clock high and clock low phases and not at the rising or falling edges. Fig. 4.9 illustrates the results. Fig. 4.9 shows that nodes in slave groups G, H, I, J, K and L have no failures with any of

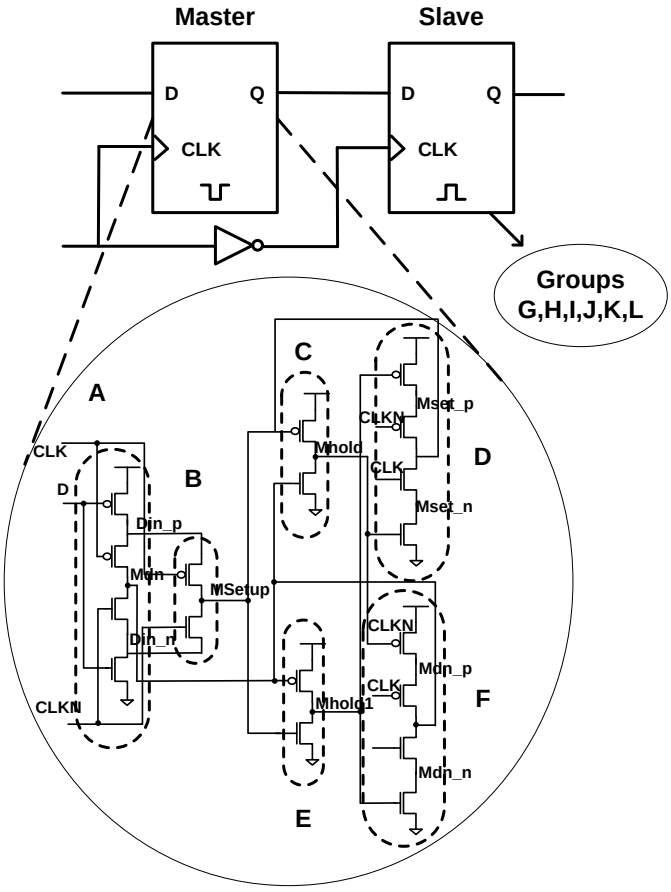


Fig. 4.8. DICE FF schematic and node grouping. The slave follows the master with internal nodes having the same naming convention (and order).

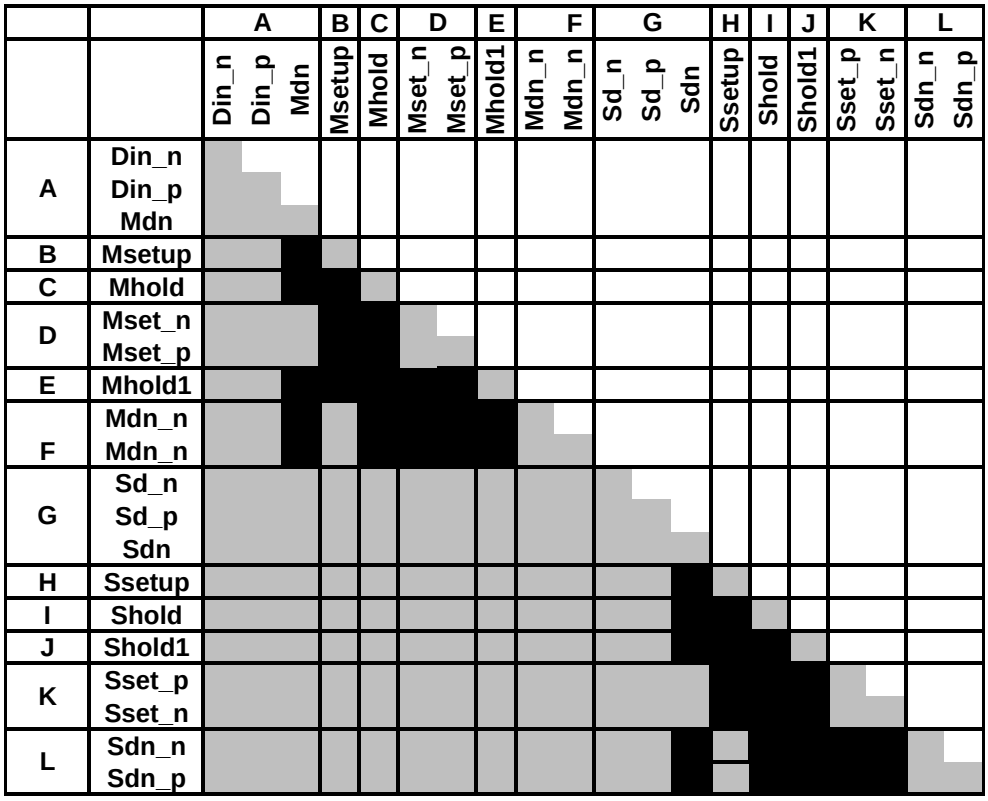
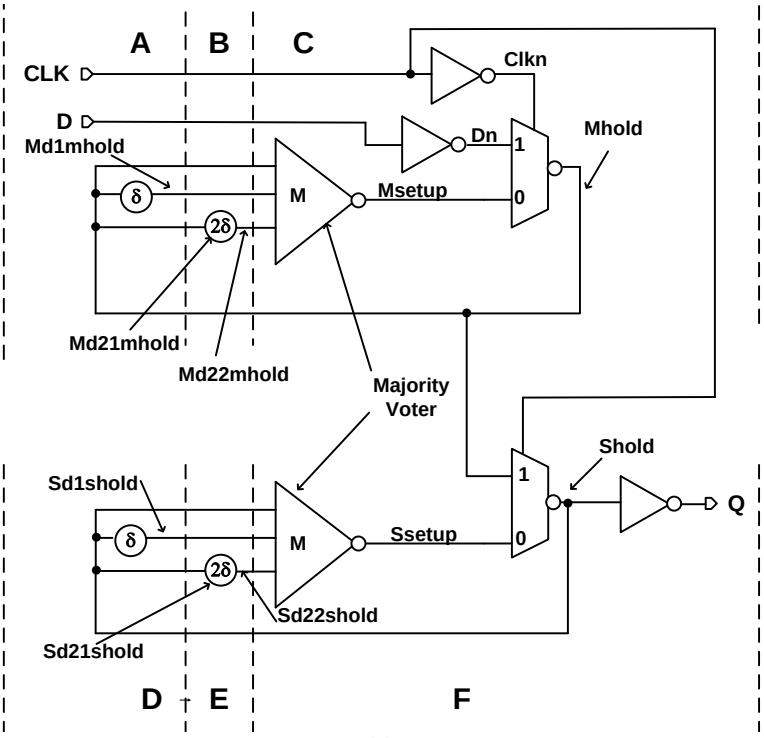


Fig. 4.9. Matrix showing the response of the DICE FF after MNCC simulations with SETs induced only at clock high and low, i.e., in the hold state.

the master group nodes. Hence a simple layout arrangement to harden the DICE against MNCC interleaves the master nodes with the slave nodes, resulting in an ordering A-G-B-H-C-I-D-J-E-K-F-L. Note however, the DICE elements are quite small, many occupying only two to four poly pitches. Thus, that the ordering does not guarantee that sufficient separation is achieved, only that it is improved.

4.3.2 Majority Voter Based Temporal FF

The methodology is applied to the temporal FF, (Fig. 4.10a) that uses majority voting in the feedback, with three unit delay elements per latch [34]. This FF functionality was discussed in chapter 2. The delay elements provide temporal filtering, whereby propagating voltage upsets of duration less than the delay element delay are



(a)

		A	B		C				D	E		F	
		Md1mhold	Md21mhold	Md22mhold	Clk	D	Mhold	Msetup	Sd1shold	Sd12shold	Sd22shold	Shold	Ssetup
A	Md1mhold												
B	Md21mhold Md22mhold												
C	Clk D Mhold Msetup												
D	Sd1shold												
E	Sd21shold Sd22shold												
F	Shold Ssetup												

(b)

Fig. 4.10 (a) Temporal FF with majority voting schematic and (b) the node matrix obtained after SET simulations. Note that the 2d delay element is produced with two series unit delays in the actual circuit, and hence has two collection nodes.

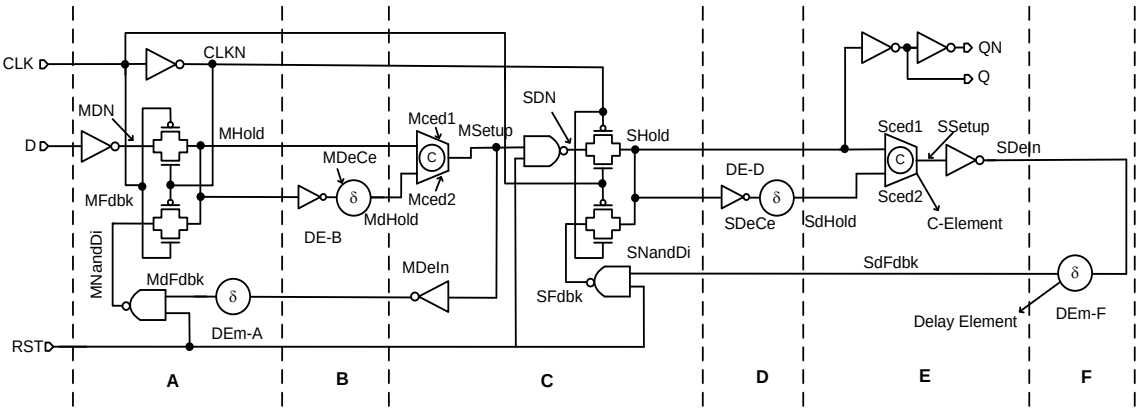
filtered and cannot propagate through the majority gate. Since the induced glitch appears at the majority gate inputs serially, an upset of the feedback loop is averted. Referring to

the schematic in Fig. 4.10 (a), circuit groups B and E have two delay elements connected in series and nodes Md21mhold and Sd21shold are respectively the intermediate nodes connecting the two delay elements. The delay elements combined with the majority voter protect the storage nodes Mhold and Shold against SEUs. This design is particularly interesting since it similarly protects against input SETs, e.g., those on CLK and D inputs, since they are also filtered in the feedback path.

The initial node grouping is done by circuit analysis. Since the delay elements are hardening elements, they have to be in separate groups as mentioned in section 4.2.3. Groups A, B, D and E contain the delay elements. The majority voter, inverters and the mux in both the master and slave latches form a combinational logic and are thus grouped together, comprising groups C and F. The analysis results produce the matrix shown in Fig. 4.10(b). As required, there are no failures in the diagonal groups, indicating a correct grouping. To determine the group ordering for the layout, first the illegal adjacencies are determined. There are six groups to be interleaved and hence there are 15 possible group adjacencies. Referring to Fig. 4.10(b), the illegal adjacencies are found to be A-C, B-C, C-E, D-F and E-F. One legal ordering for the full FF is ADEBFC.

4.3.3 Area Efficient C-Element Based Temporal FF

Fig. 4.11(a) shows a temporal FF using Muller C-Elements [35] that was also discussed in chapter 2. It has six hardening elements: four delay elements and two C-Elements, all of which are placed in separate groups. Combinational logic paths that feed into or are driven by these hardening elements are grouped as circuit groups A through F. The C-Element tri-states if the inputs mismatch. Hence, in both the master and slave latches, the combination of C-Element and delay element act as SET filters protecting



(a)

		A						B		C										D		E				F
		mdn	clkn_m	mhold	mdfdbk	mnandi	mfdbk	mdhold	mdece	mced1	mced0	msetup	mdein	sdn	clkn_s	snandi	sfdbk	shold	m_s_nandi	sdece	sdhold	sced1	sced0	ssetup	sdein	sdfdbk
A	mdn																									
	clkn_m																									
	mhold																									
	mdfdbk																									
	mnandi																									
	mfdbk																									
B	mdhold																									
	mdece																									
C	mced1																									
	mced0																									
	msetup																									
	mdein																									
	sdn																									
	clkn_s																									
	snandi																									
	sfdbk																									
	shold																									
	m_s_nandi																									
D	sdece																									
	sdhold																									
E	sced1																									
	sced0																									
	ssetup																									
	sdein																									
F	sdfdbk																									

(b)

Fig. 4.11 (a) Temporal FF schematic using Muller C-elements and (b) node matrix of the response obtained after SET simulation methodology.

both the CLK and D inputs. The delay elements in the feedback paths protect nodes MSetup and SSetup against SEUs.

Fig. 4.11(b) shows the node matrix obtained from the SET simulations depicting

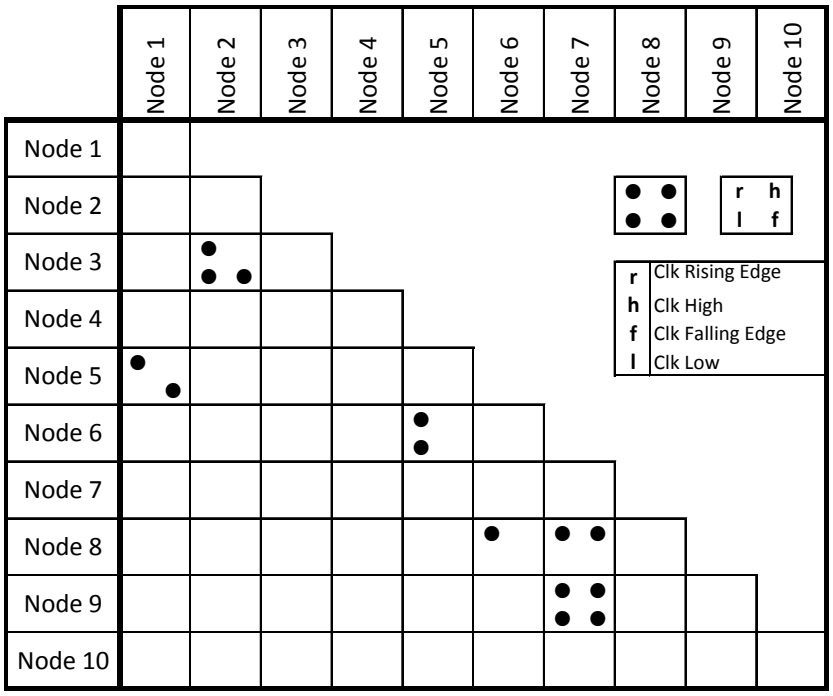


Fig. 4.12. Node matrix showing failing node pairs with black dots. Dots in the top left, top right, bottom right and bottom left reflect node pair failures during the clock rising edge, clock high, clock falling edge and clock low, respectively.

the MNCC vulnerability of all node pairs. Again, as required the groups (bold squares) along the diagonal have no failures. As in the previous case, there are six groups to be interleaved and hence 15 possible orderings. The legal group ordering is again determined by eliminating the illegal adjacencies found from the matrix, i.e., A-B, A-C, B-C, C-D, C-E, D-E, D-F & E-F. This leaves only four possible group orderings, namely C-F-A-D-B-E, C-F-A-E-B-D, C-F-B-D-A-E and C-F-B-E-A-D. Which of these orderings is best is chosen based on the one providing the least intergroup routing.

4.4 Improved Matrix Representation

Fig. 4.12 shows an improved representation of failures as compared to that shown in Fig. 4.7. Dots in the top left, top right, bottom right and bottom left correspond to failures at the clock rising edge, during clock high, at the clock falling edge and during

clock low, respectively. Noting the type of fail, i.e., clock high, low, or edge, aids in the design process allows more accurate hardness determination, e.g., SETs have a small time window in the rising/falling clock phase, while an upset that occurs in the clock high or low phase is sensitive ½ of the time. The matrix diagonal comprises the single node failures. Ideally, a hardened FF design would have none, leaving it susceptible only to upsets caused by MNCC.

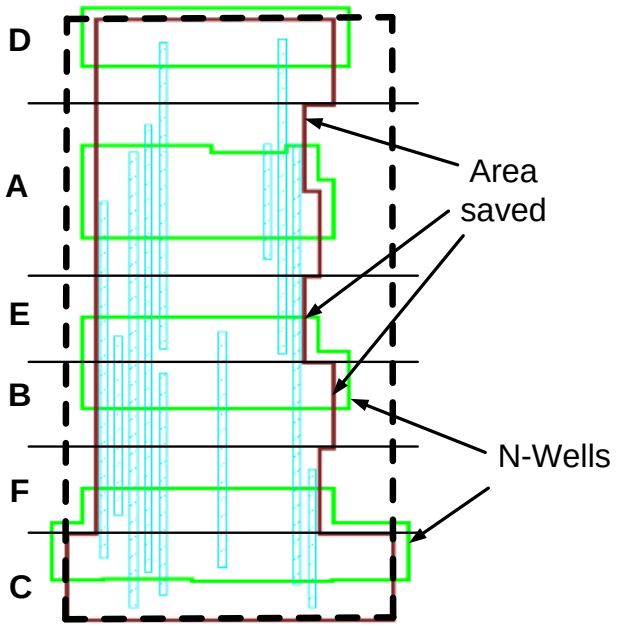
This new representation will be utilized in the circuit hardness analysis of a new FF that will be compared with few more FFs in chapter 5

4.5 Non Rectangular Vertical Cell Interleaving

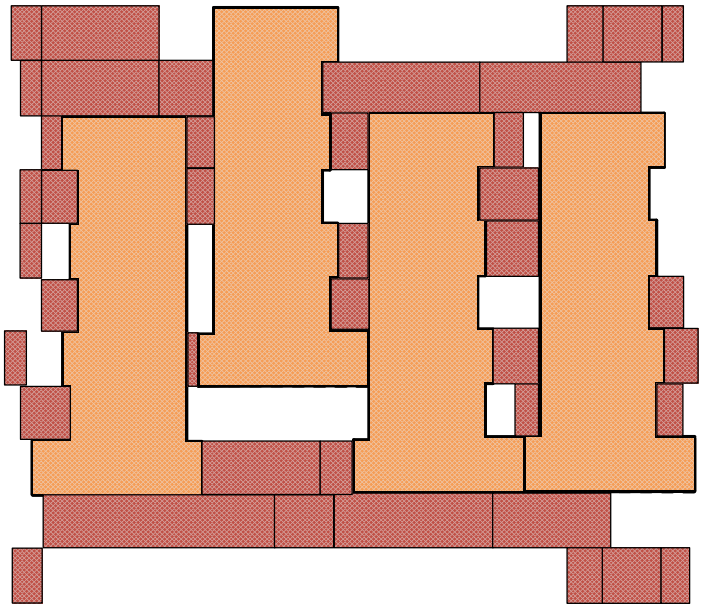
As explained in section 4.2.1, interleaving circuit blocks is a very area efficient hardening technique against MNCC. Interleaving cells vertically has the added advantage of providing well separation between nodes, which has been shown to be very effective in SRAMs, where well crossing MBUs are much rarer than those in a single well. It is thus desirable to spatially separate critical nodes across wells and diffusions in the vertical axis. This vertical interleaving provides very effective protection against MNCC as the N-wells have the correct bias to collect diffusing charge in the P type substrate. Substrate charge cannot propagate to P type junctions in the N-wells and a very shallow angle is required to pass through two adjacent N wells, making PMOS MNCCs less likely.

4.5.1 Vertically Interleaved Cell Layout and APR Compatibility

Fig 4.13(a) shows the layout for the temporal FF (Fig. 4.11(a)). Only the M2 connecting the circuit groups and well layouts are shown. Layers above M2 are not used.



(a)



(b)

Fig. 4.13. (a) Vertically interleaved temporal FF layout, showing the area savings as compared to rectangular cell (b) APR tool utilizing the area saved to abut standard cells.

The ordering C-F-B-E-A-D is chosen to provide critical node spacing by interleaving the master and slave circuits, each of which is separated into three sub-cells (cell A occupies two rows, to simplify the routing and optimize the cell footprint). This provides full

multiple node collection separation of one N-well (providing at least 3.92 µm of critical node separation). The layout uses novel non-rectangular cells allowing standard cells to be placed into the gaps and standard APR tool flows are modified to effectively use the saved area, as shown in Fig. 4.13(b). The area saved is up to 20% versus a rectangular cell (Fig. 4.13(a)). The sub-cells fit in the smallest available standard cell height, at 7 M3 tracks, 1.96 µm. The vertical M2 tracks used to connect the sub-circuits are shown. The M2 tracks are sparse and shared where possible to limit their impact on top level routing.

CHAPTER 5

A REDUCED POWER AND AREA FLIP-FLOP WITH HIGH SOFT ERROR IMMUNITY

In chapter 1 we saw how a single impinging ionizing radiation particle is increasingly likely to upset multiple circuit nodes and produce logic transients that contribute to the soft error rate. Consequently, hardening flip-flops to transients at the data and control inputs, as well as to single event upsets, due to either single or multi-node upsets is increasingly important.

This chapter presents a low power and area efficient radiation hardened flip-flop design. The FF achieves a 31% power and 35% area reduction compared to a previous temporal design [35] with similar hardness. The hardness is verified and compared to other published designs (described in chapter 2), via the systematic simulation approach (described in chapter 4) which comprehends multiple node charge collection and tests resiliency to upsets at all internal and input nodes. Comparison of the hardness, as measured by estimated upset cross-section, is made to two FF designs. Additionally, the importance of specific circuit design aspects to achieving hardness is shown.

5.1 Proposed Hardened Flip-Flop

5.1.1 Hardened FF Circuit Approach

Since the proposed design has four C-elements we abbreviate it as 4CE. Fig. 5.1(a) shows the proposed 4CE FF circuit that is hard to upsets on D and CLK inputs as well as SEU. The design is based on [35] but halves the number of delay elements, significantly reducing the size and power dissipation. The master and slave latches are

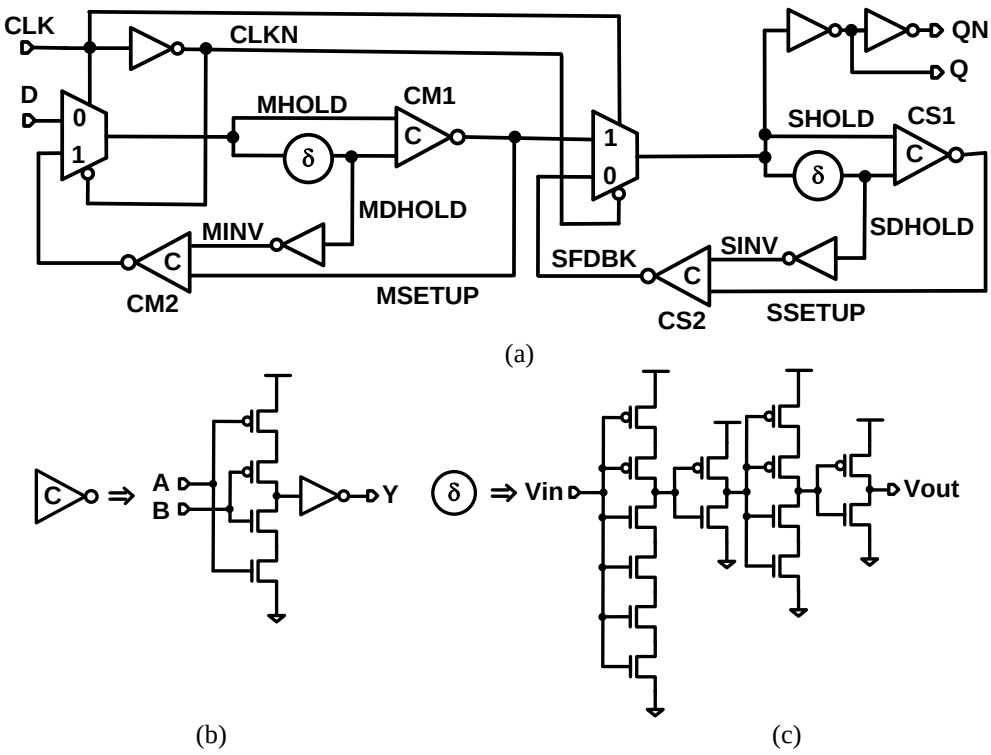


Fig. 5.1.(a) Initial proposed 4CE FF design with (b) C-Element and (c) delay element schematics.

hardened similarly. Referring to the master latch, upsets of the setup and hold nodes MSETUP and MHOLD, respectively, having duration less than delay element (δ) delay are filtered by the delay element and C-element combinations in the latch feedback path.

The feed forward delay and C-element (CM1) combination comprise a delay filter that blocks the forward propagation of transients of duration less than δ to the MSETUP node. In the feedback path, a transient at MSETUP is filtered by the feedback C-element CM2, which keeps the transient from propagating to the other storage node, MHOLD. Consequently, transients at either the setup or hold node cannot propagate to upset the latch state, providing SEU mitigation. Since a transient at the hold node could also be due to a transient error on the D or clock input, i.e., a logic SET, those errors are also mitigated. The feedback C-element (CM2) is required since in its absence, an SET at node MSETUP can propagate around the feedback loop, tri-stating Muller C-element

CM1.When tri-stated, the C-element will fail to remove the charge to restore MSETUP. This would allow an upset to propagate when the δ delay is elapsed.

Like any temporally hardened design, the FF has large setup time approximated by 2δ [39]. Basically, an SET of duration δ may occur near the end of the setup time, which is bounded by the δ delay to the setup node, adding a second δ time duration to t_{SETUP}.

The delay element and the C-element schematics are shown in Figs. 5.1(b) and 5.1(c) respectively. The delay produced by the delay element exceeds 350ps in post-layout simulations. It is difficult to produce long delays with minimal area and power, since delay τ is proportional to C/I_{DS}. Moreover, an SET at any circuit node has a duration that is also set by the drive at that node [38]. Chapter 3 described different delay element variants. The delay element here uses transistor stacks to produce a long delay, but we force the SET restoring current to be equal to that of the cell library NAND and NOR gates. This is a compromise between the area, power, and SET duration to be mitigated—shorter delays reduce power consumption but negatively impact hardness.

5.1.2 Design Details

We targeted a foundry low standby power 90 nm seven track library for the design. Conventionally, FF circuit nodes are grouped to provide the smallest area by maximizing contiguous diffusions in the layout. The resulting circuit implementation of the proposed FF master latch with the best layout density is shown in Fig. 5.2(a). Note that conventionally, the D input should comprise the outermost devices on the stack, but this device ordering results in a less optimal layout. The C-element, multiplexer and tri-state inverter have contiguous diffusions. However the three deep NMOS and PMOS

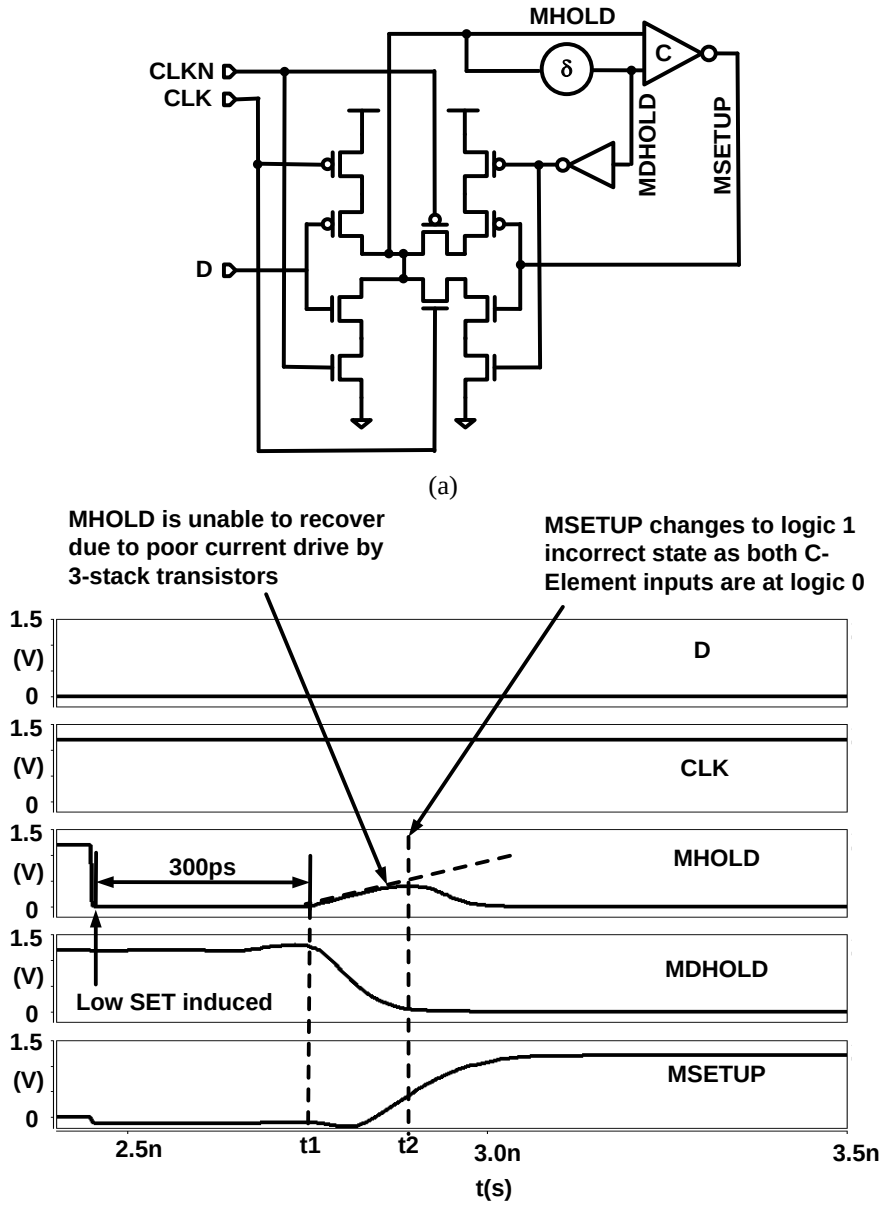
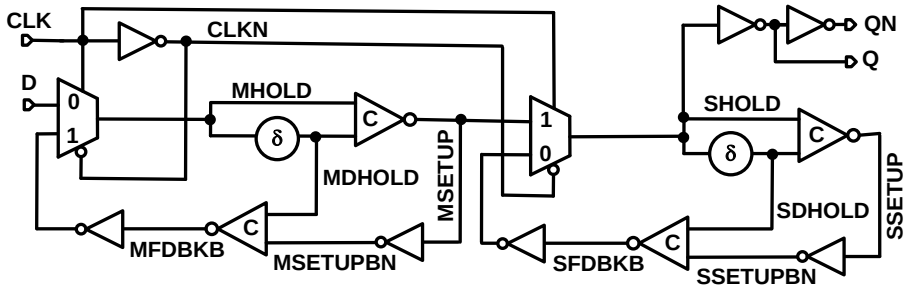


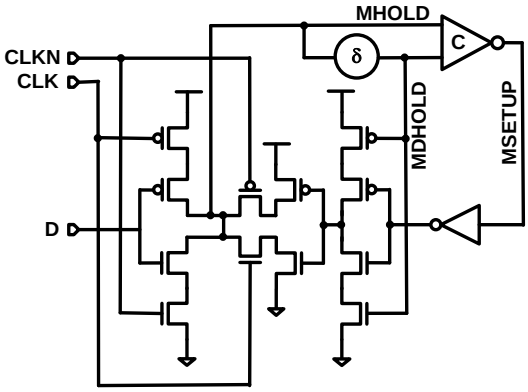
Fig. 5.2. (a) Initial proposed FF master latch circuit and (b) waveforms showing MHOLD node vulnerable to SET of duration 300ps.

stacks provide very poor drive current. Analysis (explained later) showed that the reduced stack drive current made the MHOLD node vulnerable to upset.

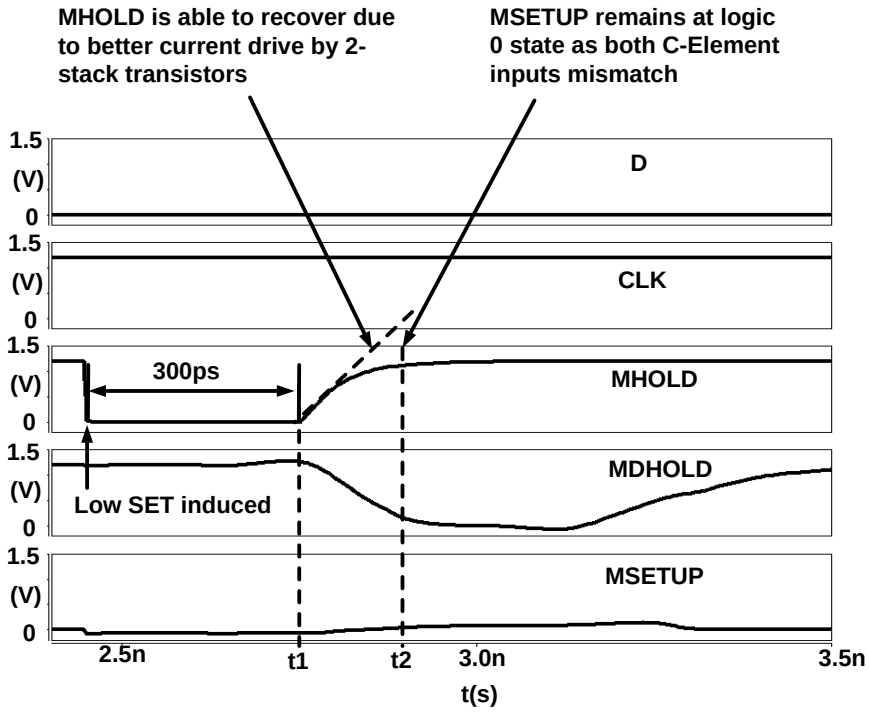
Fig. 5.2(b) shows a low SET of duration 300ps induced on MHOLD in the clock high phase with logic 0 on data input. At time t1, MHOLD node starts to recover to its original logic state (logic 1). However, due to the poor current drive provided by the three



(a)



(b)



(c)

Fig. 5.3. (a) Modified FF design that (b) removes the previous three stack transistors by adding an inverter before and after the C-Element to master and slave latches (c) and waveforms confirming the MHOLD node robustness to SET.

stacked transistors, the recovery time is excessive (as shown by the slope in dotted lines).

At time t2, the logic state (logic 0) on MHOLD node fully propagates to MDHOLD node after passing through the delay element. Moreover, at this time, the MHOLD node voltage is still below the switching threshold of the C-element. Since both C-Element inputs are at logic 0, its output (MSETUP) switches to the logic 1 state. Positive feedback drives node MHOLD back to logic 0, retaining the incorrect state.

Fig. 5.3(a) shows a modified circuit implementing the same function, but with reduced stack depth. The three transistor stack is removed by adding an inverter subsequent to each C-element as shown in Fig. 5.3(b), resulting in a stack depth of at most two. The feedback loops now have four inversions, but the overall setup time, which is dominated by the delay elements, remains similar. Fig. 5.3(c) shows the MHOLD node now properly recovering under the same simulation conditions. At t2, due to better two deep stack current drive (evident by the improved slew rate), the MHOLD node voltage is sufficient to cause inputs of the C-element to be in opposite logic states, causing MSETUP node to remain at logic 0 state. The modified design thus protects MHOLD node against SEUs. The removal of the second delay element from both the master and slave latches reduces the FF energy per cycle at full activity factor by 31% as compared to that in [35] implemented on the same technology.

5.2 FF Hardness Verification and Layout

The circuit simulation based methodology described in chapter 4 is used to identify MNCC sensitive FF nodes. By determining which nodes can be grouped together without producing an upset due to MNCC, the layout can be optimized to provide high MNCC immunity.

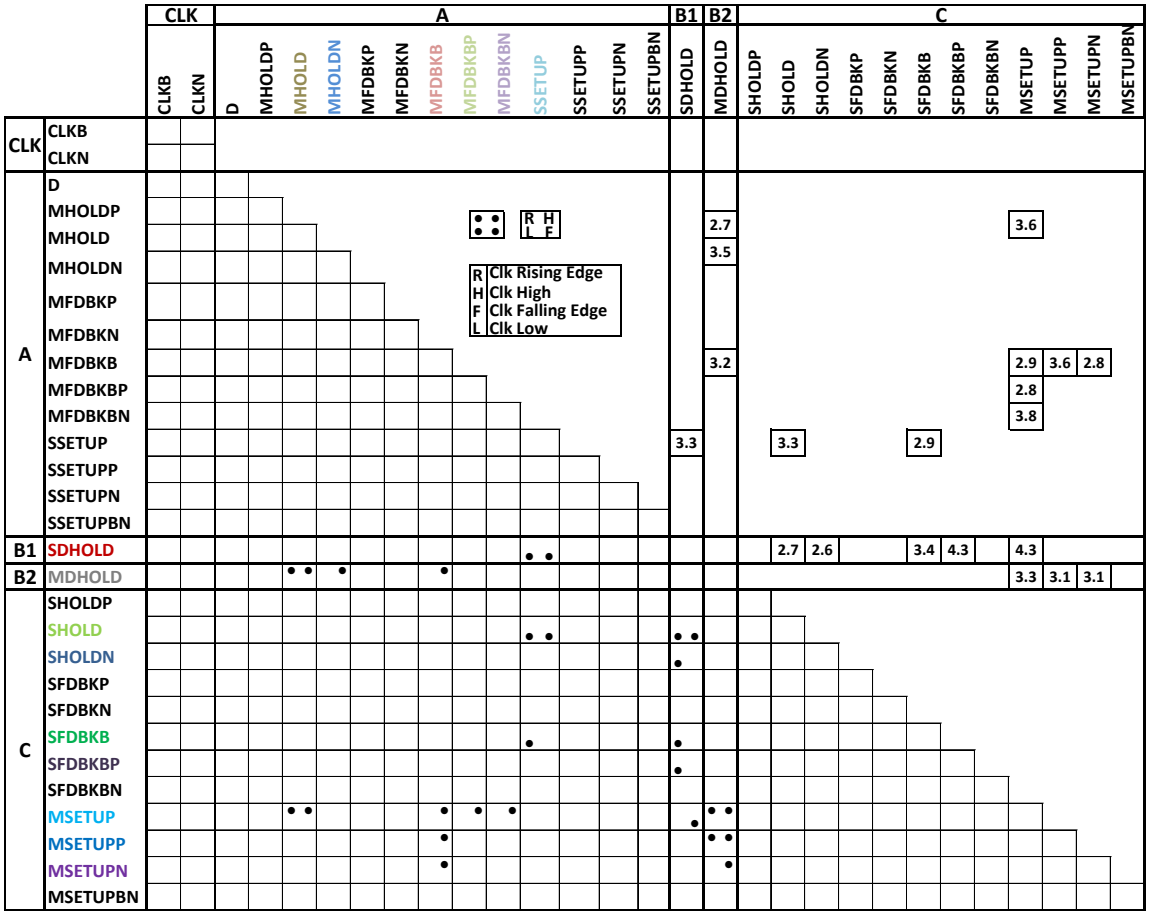


Fig. 5.4. Matrix showing the failing node pairs in the proposed 4CE FF at different clock phases when SETs are simultaneously induced on each node pair.

The results of the single node upset analyses comprise the diagonal entries and dual fault simulations of the proposed FF comprise the lower triangular matrix shown in Fig. 5.4. All intermediate nodes, including diffusions within transistor stacks are analyzed and represented. We refer to nodes that when simultaneously upset can affect the FF state as critical nodes.

5.2.1 Node Grouping Heuristics

The FF nodes are divided into five groups CLK, A, B1, B2, and C as shown in Figs. 5.4 and 5.5. Details of the grouping approaches are described in [60]. Referring to Fig. 5.5, these groups correspond to the bold squares along the matrix diagonal and can

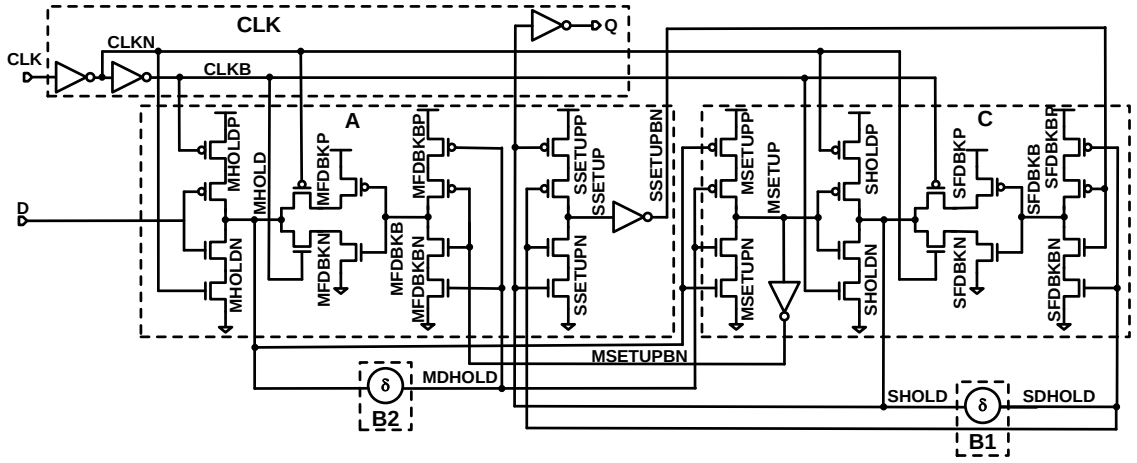


Fig. 5.5. Proposed FF schematic showing node grouping to efficiently separate critical nodes based on the groupings in the double node upset matrix.

have no upsets—single node vulnerabilities dominate the final FF SER. Since nodes in the same group are in close proximity, the likelihood of MNCC among them is high. Consequently, a node cannot be in the same group with another node if their combination causes an upset.

MSETUP, SSETUP, MFDBKB, and SFDBKB are the FF storage nodes driven by the C-elements. The C-element is the crucial hardening circuit—if both its inputs are simultaneously incorrect its output may transition erroneously. Consequently, the gates driving each C-element input must be located in different groups (or minimally at opposite ends of one group). The gates driving the C-element driving node SSETUP in group A are placed in groups B1 and C. Similarly the gates driving the C-element driving node MFDBKB in group A are placed in groups B2 and C. For layout efficiency, the inverters in the feedback paths driven by nodes MFDBKB and SFDBKB (Fig. 5.3(a)) are merged with the pass gate transistors resulting in the final FF circuit in Fig. 5.5. The latch feedback multiplexers are comprised of two tri-state inverters as shown.

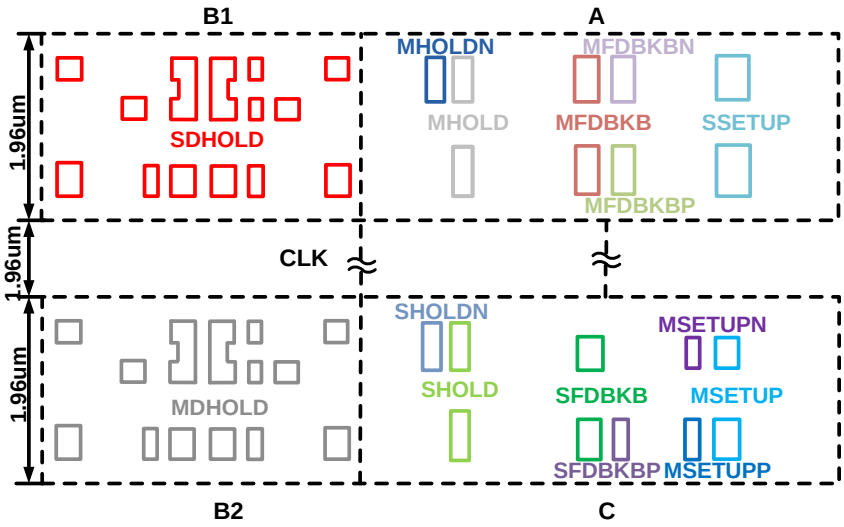


Fig. 5.6. Proposed FF layout showing the sensitive nodes corresponding to the color coded nodes in the matrix. Note the middle block height is compressed for brevity.

5.2.2 FF Layout and APR Compatibility

Appropriate hardened FF layout is essential for MNCC robustness since it determines the critical node location and separation. Vertical separation is ideal, since it places N wells between the critical nodes. Since they are biased at V_{DD}, N wells make good sinks for substrate charge. Charge tracks within the N wells are attenuated by the depth of the wells.

From the matrix in Fig. 5.4, it can be seen that there are multiple critical node pairs, two such being SDHOLD-SSETUP and MDHOLD-MHOLD. Fig. 5.6 shows the critical node locations in the FF (color codes correspond to the matrix in Fig. 5.4). The separation distances between the critical nodes are shown in the upper triangular matrix in Fig. 5.4. For instance, the separation distance between SDHOLD and SSETUP is 3.3 μm.

The matrix indicates that blocks A and C cannot be adjacent as they have multiple critical node pairs. Hence blocks A and C are separated by the CLK block in the layout.

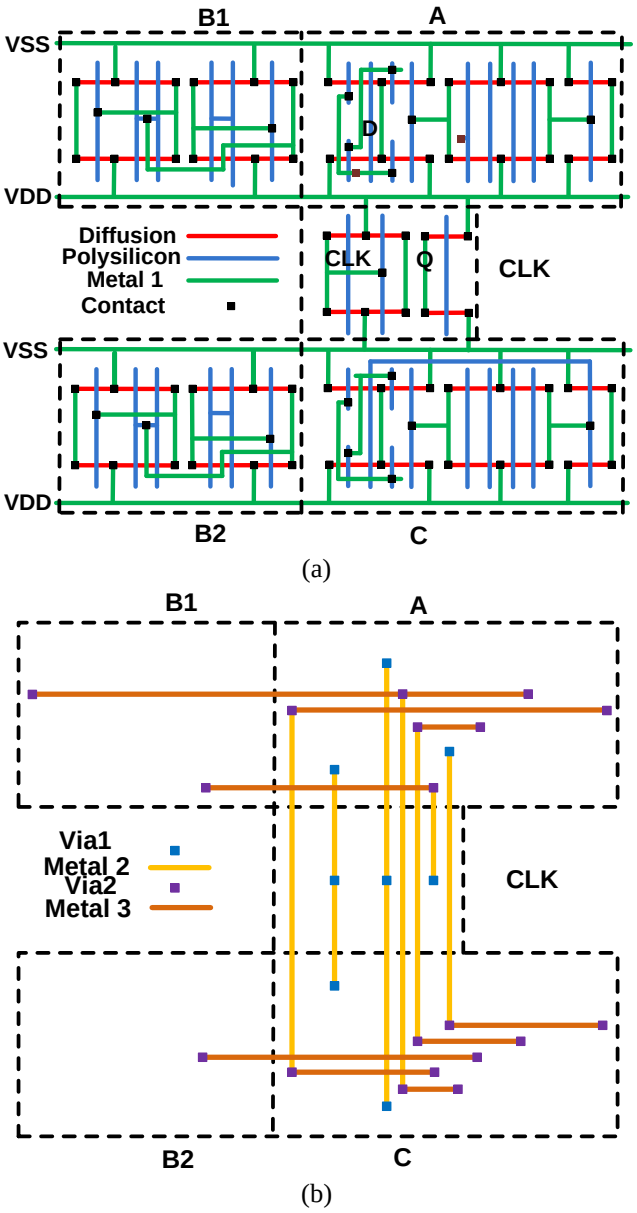


Fig. 5.7. (a) Stick diagram representing the FF layout. (b) The metal routes connecting the blocks.

Blocks A and C cannot be next to blocks B1 and B2 respectively, as the node SSETUP in block A fails with node SDHOLD in block B1, and nodes MSETUP, MSETUPP and MSETUPN fail with node MDHOLD in block B2. However, B1-A and B2-C combinations are possible by placing the MSETUP/SSETUP nodes at the far right end in blocks A and C layouts (Fig. 5.6), providing separation distance of at least 3.1 μm from

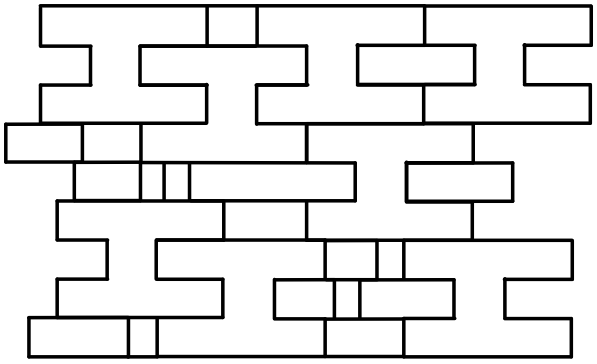


Fig. 5.8. FF placement in a synthesized design abutting standard cells.

the MDHOLD/SDHOLD nodes. Blocks B1 and B2 are the layouts for the delay element shown in Fig. 5.1(c). Since the delay element is a combinational circuit, charge collection on any of its constituent diffusions will propagate to the output. Hence, these diffusions are clustered together and considered as one node. Fig. 5.7 is a stick diagram of the complete FF layout showing that metals 2 and 3 used to interconnect the FF blocks. All routes are kept within the cell borders, and care is taken to avoid blocking the standard cell pins above and below, as well as within of the CLK block. The proposed FF achieves an area reduction of 35% vs. that in [35] when implemented in this technology.

A cartoon depicting FF placement in a final APR design is shown in Fig. 5.8. With minor APR flow modifications, standard cell gates can be automatically placed into the FF gaps using standard tools (e.g., Cadence Encounter). Noting that the CLK block may be adjacent to any other, a conventional single row height hardened design is possible. This layout places the constituent circuit groups in the order B1-A-CLK-C-B2. This is in contrast to the hardened design in [35] where a single row height layout compromised some critical node spacing [61].

5.3 Hardness Comparison

We have shown the proposed FF to be hard to incoming SETs on the D and clock

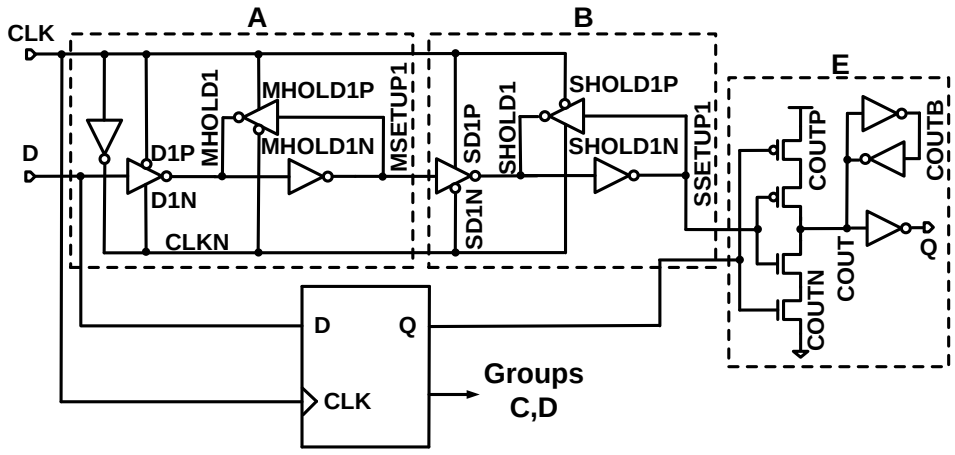


Fig. 5.9. BISER FF schematic showing sensitive node groups. The layout interleaves the groups to avoid simultaneous charge collection from single impinging radiation strike.

inputs, direct upset of storage circuit nodes (SEUs), as well as to MNCC. In this section the proposed FF cross-section is estimated and compared to two hardened FFs using the circuit simulation based methodology. Both designs' functionality were explained in chapter 2 and briefly repeated here for brevity.

5.3.1 BISER FF

Fig. 5.9 shows the BISER FF schematic [44] divided into its sensitive node groups. This design uses dual redundant standard D-FFs connected to a C-element. If one of the FFs is upset, the inputs to the C-element would mismatch causing it to tri-state protecting the stored state. The jam latch at the C-element output maintains the logic state. We modify the original design to buffer the C-element jam latch. This avoids exposing this storage node to coupling noise on the output node, which is more typical of commercial standard cell designs—note that when one D-FF has been upset, this latch state is critical—a noise failure would render the design soft. This change has a small (one poly pitch) impact on the BISER size.

A possible group interleaving for the BISER FF layout is A-C-E-B-D.

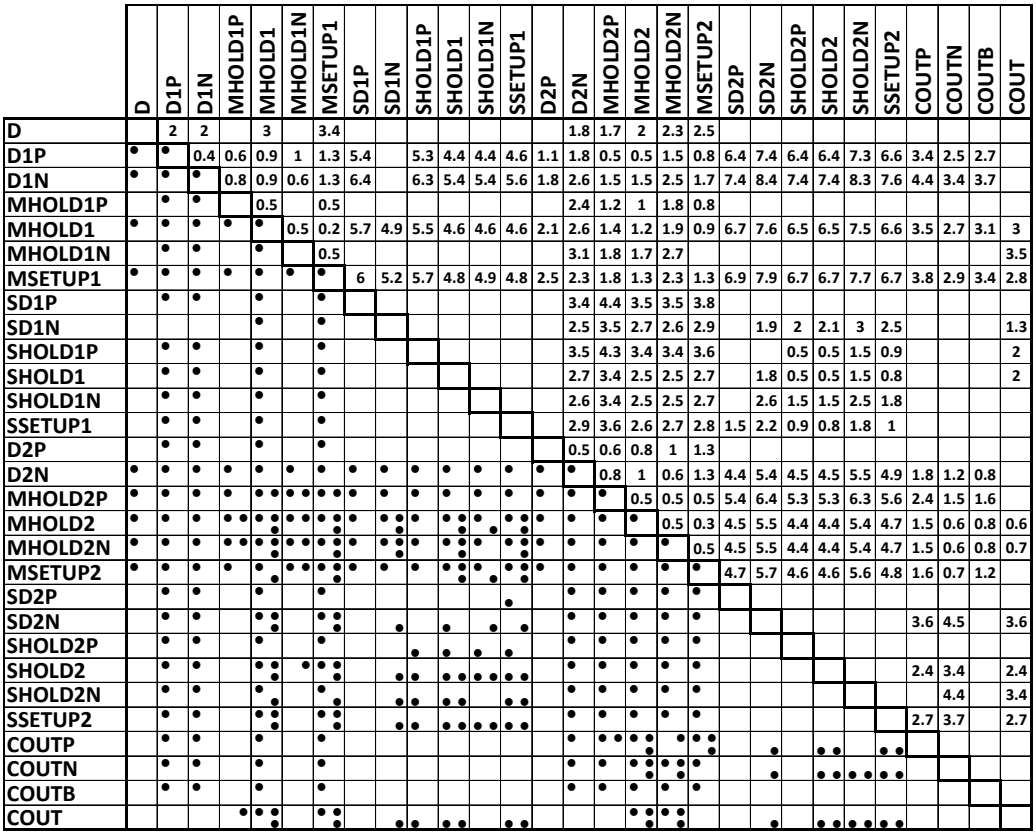


Fig. 5.10. Matrix showing single and two node failures in BISER FF to induced simulated SETs of δ duration. The upper triangle shows the separation distances between the upset node pairs expressed in μm for vertically interleaved node groups.

Interleaving the groups vertically as in the previous design is straightforward. The groups can also be interleaved inline. Fig. 5.10 shows the BISER dual fault analysis matrix. The upper triangle shows the separation distances between the upset node pairs expressed in μm for vertically interleaved node groups. Unlike the proposed 4CE FF, the BISER FF is not hard to upsets on clock inputs, hence CLK and CLKN nodes are not shown in the matrix. The number of failures is significantly greater than in Fig. 5.4. It can be noticed that the majority of failures occur in the clock rising edge, where the BISER FF is vulnerable to upsets in the setup time window.

The BISER area is equal to two FFs and one latch. For the former, the designs of

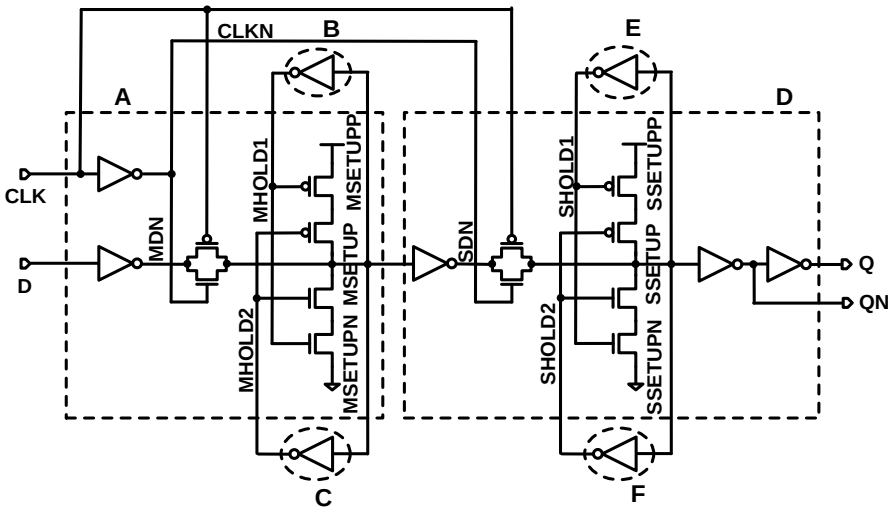


Fig. 5.11. SIN FF schematic showing sensitive node groups with groups interleaved in the layout to avoid simultaneous charge collection from single impinging radiation strike.

our commercial 7 track library are slightly altered. For instance, the slave latch input is a tri-state inverter rather than CMOS pass-gate. This reduces some transient errors due to back-writing from the slave to the master at a single poly pitch cost. The C-element jam latch combination fits into the same number of poly pitches as a library clocked latch. The BISER area is 15% smaller than our proposed 4CE FF design.

5.3.2 Split Internal Node (SIN) FF

Fig. 5.11 shows a FF schematic based on the hardened latch proposed in [52], with its sensitive nodes grouped. In this design, setup nodes are protected by dual redundant HOLD nodes. The feedback C-elements protect if one of the HOLD nodes is upset. However, setup node upsets are unprotected. Lacking delay elements, this design is also unprotected to input SETs.

A possible vertical or inline group interleaving for the FF layout is A-E-C-D-B-F. Fig. 5.12 shows the dual fault analysis matrix. It can be seen that MSETUP and SSETUP nodes have failures to both single node upsets and to all two node upset combinations.

	D	MDN	MHOLD1	MSETUPP	MSETUP	MSETUPN	MHOLD2	SDN	SHOLD1	SSETUPP	SSETUP	SSETUPN	SHOLD2
D	●	2	6.8	2.8	3	2.8	3.1	4.8	1.4	5.1	5.2	6	9
MDN	●	●	6.6	0.6	0.8	0.6	2.9	4.5	1.5	4.4	4.4	5.4	8.7
MHOLD1	●	●	●	6.8	6.9	7.8	2.9	0.8	4.7	2	1.4	1.2	1
MSETUPP	●	●	● ●	●	0.5	0.5	3.3	4.7	2.2	4.5	4.5	5.4	8.8
MSETUP	● ●	● ●	● ●	● ●	● ●	0.5	3.5	4.7	2.4	4.6	4.5	5.5	8.9
MSETUPN	●	●	● ●	●	● ●	●	4.2	5.6	2.7	5.5	5.6	6.4	9.8
MHOLD2	●	●	●	● ●	● ●	● ●	●	0.8	0.8	1.3	1.6	2	4.9
SDN	● ●	● ●	● ●	● ●	● ●	● ●	● ●	●	2.6	0.6	0.8	0.6	2.8
SHOLD1	● ●	● ●	● ●	● ●	● ●	● ●	● ●	● ●	●	2.8	3	3.7	6.8
SSETUPP	●	●	●	●	● ●	●	●	● ●	● ●		0.5	0.5	3.8
SSETUP	● ● ●	● ●	● ●	● ●	● ●	● ● ●	● ●	● ●	● ●	● ●	● ●	0.5	3
SSETUPN	● ●	● ●	● ●	● ●	● ●	● ●	● ●	●	● ●	●	● ●	●	3
SHOLD2	● ●	● ●	● ●	● ●	● ●	● ●	● ●	●	●	● ●	● ●	● ●	●

Fig. 5.12. Matrix showing single and two node failures in SIN FF to induced simulated SETs of δ duration. The upper diagonal matrix shows the separation distance between the upset node pairs expressed in μm for vertically interleaved node groups.

Similar to BISER FF, the SIN FF is also not hard to upsets on clock inputs, hence CLK and CLKN nodes are not shown in the matrix. The table illustrates its poor upset tolerance. The distances shown in the matrix (Fig. 5.12) are for the vertical interleaving case. Due to small circuits' sizes, the distances using horizontal interleaving are severely compromised.

5.3.3 Cross-Section Comparison

Circuit hardness is measured experimentally by determining the circuit upset cross-section σ, that is, the relative target area determined by

$$\sigma = \frac{Errors}{Fluence}. \quad (1)$$

where the fluence is measured in particles/(cm^2·s). Broad beam testing is directional but ionizing particles causing upset in normal IC operation impinge from any direction (are

isotropic). Secondaries from proton or neutron testing are also isotropic. The analysis thus assumes particles impinging from any direction.

The tables generated by the analysis are used to analyze the hardness. The total FF cross section is computed by summing the individual node cross-sections as given by

$$\sigma_{FF} = \sum_{i=0}^{N} \sigma_{NODE_i}. \quad (2)$$

If a node upsets when hit singly, its cross-section is computed by multiplying the node area with the sum of the timing window weights. The computation differs for clocked and hold modes. In the clocked mode, node reversals are considered for all the four clock phases i.e., rising (r), high (h), falling (f) and low (l) and the cross-section is given by

$$\sigma_{NODE_{Single-Clocked}} = NODE_{Area} \sum_{weight}^{r,h,f,l} Timing\ Window_{weight}. \quad (3)$$

The cross-section computation in the hold mode, considers node reversals only for clock high and low phases as given by

$$\sigma_{NODE_{Single-Hold}} = NODE_{Area} \sum_{weight}^{h,l} Timing\ Window_{weight}. \quad (4)$$

We use 5% to 15% weights for rising and falling edge susceptibility and 30% to 45% weights for each of clock high and clock low, to account for the clock activity factor and SET capture window. This number should vary the clock activity factor.

For the MNCC case (two node upsets) the cross section computation is illustrated in Fig. 5.13, where two nodes, A and B are sensitive to MNCC. Particle incidence is isotropic, but MNCC requires the incident ionizing radiation particle to pass through or near both nodes. Each node has a sensitive (collection) volume, which extends some distance below it, shown by the collection depth. This accounts for charge tracks that are below the node, where collection may also be due to diffusion. By centering a sphere at

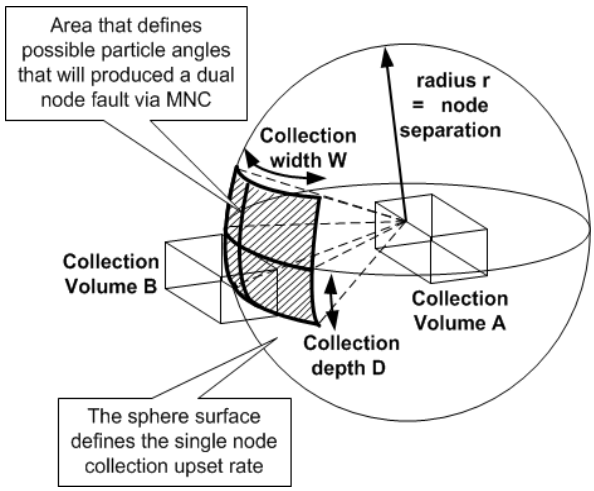


Fig. 5.13. The effective cross section seen by an ionizing particle that simultaneously strikes two nodes A and B causing upset. Only a limited solid angle can pass through the collection region of both nodes, providing a straightforward estimate of the upset probability.

node A, with a radius r defined by the distance to the collection volume of node B, the relative reduction in circuit cross-section σ afforded by the critical node separation can be estimated. A node susceptible to upset by itself (i.e., a single node upset) can be upset from any angle. Thus, the single node hit σ can be defined as proportional to the area of the surface of the sphere. The shaded box subtended by collection width in Fig. 5.13 is extended vertically to twice the collection depth to account for particles striking node B and being collected at node A (i.e., charge tracks in the opposite direction). This box defines the area on the sphere's surface that a particle must pass through to cause MNCC upset via nodes A and B. Therefore, node separation affects the node σ by

$$\sigma_{NODE_{MNCC}} = (\sigma_{SIM}.W.D)/(4\pi r^2), \quad (5)$$

where σ_{SIM} is the simulated failure rate adjusted for the timing window given by either equation (3) or (4) depending on whether σ is computed in the clocked or hold mode.

The node separation is based on the physical design. Our initial designs used vertical interleaving, which can afford better hardness since the N wells collect charge

TABLE 5.1

CROSS-SECTION REDUCTIONS OF FFS IN CLOCKED AND HOLD MODES FOR DIFFERENT TIMING WINDOW WEIGHTS NORMALIZED TO NORMAL D-FF

DESIGN	MODE	TIMING WINDOW WEIGHTS (%) (RISING, HIGH, FALLING, LOW)	CROSS-SECTION REDUCTION (%) INTERLEAVED (VERTICAL, INLINE)
SIN	Clocked	5,45,5,45	13.4, -0.1
SIN	Clocked	10,40,10,40	2.3, -14.1
SIN	Clocked	15,35,15,35	-7.6, -27.1
SIN	Hold	5,45,5,45	35.5, 26.4
SIN	Hold	10,40,10,40	44.5, 36.7
SIN	Hold	15,35,15,35	53.1, 46.4
BISER	Clocked	5,45,5,45	52.6, 75.1
BISER	Clocked	10,40,10,40	40.2, 62.4
BISER	Clocked	15,35,15,35	28.5, 50.2
BISER	Hold	5,45,5,45	69.9, 90.1
BISER	Hold	10,40,10,40	73.9, 91.3
BISER	Hold	15,35,15,35	77.8, 92.6
4CE	Clocked	5,45,5,45	97.7, 99.2
4CE	Clocked	10,40,10,40	97.8, 99.3
4CE	Clocked	15,35,15,35	98.0, 99.3
4CE	Hold	5,45,5,45	97.8, 99.3
4CE	Hold	10,40,10,40	98.1, 99.4
4CE	Hold	15,35,15,35	98.3, 99.5

and thus mitigate diffusion in the substrate. For the MNCC cases and vertical interleaving, we chose r as 1, 2, 3, or 4 cell heights, based on the number of intervening cells. For inline separation the node distances can be lesser or greater than for vertical interleaving depending on the design. In most cases the constituent circuits are wider than they are tall, providing greater critical node separation.

Table 5.1 shows the calculated cross-section reductions of all three FFs in both clocked and hold modes normalized to the unhardened standard cell library D-FF. Different timing window weights are used. Cross section reductions are shown for layouts which have groups interleaved both vertically and inline. The analysis is not adjusted for vertical interleaving, but SRAM results have consistently shown that well

crossing collection is considerably less probable [62].

The SIN and BISER designs are not hardened to input SETs. Consequently, the SIN FF shows poor σ improvements in the clocked mode where its hardness to upsets, i.e., -7.6% and -27.1%, is actually worse than the baseline unhardened D-FF. The SIN and the BISER FFs are harder to upsets in the hold mode as compared to the clocked mode, showing σ reductions of 26% to 53.1% and 70% to 92.6%, respectively for both layout designs. BISER FF provides almost 2xσ reduction in the hold mode compared to the SINF FF. For both the clocked and the hold modes, the proposed FF provides σ improvements of over 97% for vertical interleaving and over 99% for inline interleaving, thus exhibiting superior hardness as compared to the other two designs.

The σ reduction for the SIN FF for inline interleaving is worse when compared to vertical interleaving as groups B, C, E and F (Fig. 5.11) are composed of only one inverter, providing negligible critical node separation. However for both BISER and the proposed FFs the inline σ is better owing to the layout aspect ratios.

CHAPTER 6

CONCLUSIONS

This work provides methodical design approaches to mitigate radiation effects on hardened by design flip-flops and also provides low power circuit design solutions. Different hardened FFs proposed in the literature were analyzed giving a brief description of the operating principle, advantages and drawbacks for each FF.

Measured SET pulse widths have varied significantly in different experiments. Those relying on current starved delay elements exhibit very large t_{SET}. This presents a conflict in designing RHBD FF delay elements, which must simultaneously achieve large delay but with high drive strength. We have proposed a novel RHBD delay circuit that does not increase worst-case IC SET duration by providing redundant current starved delay paths. If one delay path collects charge, the overall delay is only marginally increased, despite very slow transient dissipation by current starved transistors, since the redundant path discharges the output. FFs, using proven interleaved layout techniques, dissipate up to 19.6% less power than inverter chain delay based temporal FFs. Two 8-bit, 8051s were designed in the TSMC 130 nm bulk CMOS process using two temporal FFs with two different delay elements. The first used an inverter chain based delay element, and the other the proposed delay element. The 8051 using the proposed delay element dissipates 18% less power than the cascaded inverter based delay element.

Interleaving constituent circuit blocks provides excellent critical node separation, but has previously required multiple bit designs or wasted space in radiation hardened FFs. The circuit groups and their ordering have heretofore been determined through circuit inspection and experiment. We have presented systematic analysis methodology for

determining the susceptibility of FF nodes to upset due to both single and multiple node charge collection We identify the critical nodes as those that when simultaneously upset cause a circuit failure. We group these critical nodes so that no two are adjacent and algorithmically determine an optimal group ordering such that the sensitive nodes are separated by another circuit group. The efficacy of the methodology has been demonstrated on different radiation hardened FF designs. A limitation of the approach is that the constituent elements must have a finite number and be of reasonable size. For instance, the DICE FF presents difficulty on both counts.

A new temporally hardened FF circuit that is both hard and energy efficient has been presented. The design achieves a 31% power and 35% area reduction compared to a temporal FF with similar hardness. Specific circuit design aspects and their importance in achieving hardness have also been described. The FF hardness was verified and compared to other designs by the proposed systematic upset simulations that quantify the susceptibility to upsets due to both single and multiple node charge collection. Different layouts to mitigate MNCC by providing the required separation between critical nodes have were proposed and quantitatively compared.

Below is the summary of the contributions of this work:

The major contributions include the developments of

- A novel low power delay element that does not increase worst case IC SET duration and which saves 19% power as compared to inverter chain delay element
- A systematic analysis methodology that determines the susceptibility of FF nodes to upset due to both single and multiple node charge collection. It identifies and provides efficient critical nodes separation in radiation hardened FFs

- A new temporally hardened FF that saves 31% power and 35% area as compared to temporal FF with similar hardness

Minor contributions of this dissertation include

- Two 8051s designed in the TSMC 130nm bulk CMOS process using two temporal FFs, one using the proposed delay element and the other using cascaded inverter based delay element. The 8051 using the proposed delay element saves 18% power than the cascaded inverter based delay element
- Classifying different hardened FFs proposed in the literature based on the hardening techniques and providing a RHBD FF taxonomy giving a brief description of the operating principle, advantages and drawbacks for each FF
- Applying the proposed methodology to different radiation hardened FF designs and determining their vulnerability to single and multi node upsets by computing circuit upset cross-section
- Test structures of FFs using the proposed and inverter chain delay elements, D-FF, BISER FF and the proposed FF for beam testing and comparing the upset cross-sections

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