

On-Chip Transformer Design and Modeling for
Fully Integrated Isolated DC/DC Converters

by

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ABSTRACT

Isolated DC/DC converters are used to provide electrical isolation between two supply domain systems. A fully integrated isolated DC/DC converter having no board-level components and fabricated using standard integrated circuits (IC) process is highly desirable in order to increase the system reliability and reduce costs. The isolation between the low-voltage side and high-voltage side of the converter is realized by a transformer that transfers energy while blocking the DC loop. The resonant mode power oscillator is used to enable high efficiency power transfer. The on-chip transformer is expected to have high coil inductance, high quality factors and high coupling coefficient to reduce the loss in the oscillation. The performance of a transformer is highly dependent on the vertical structure, horizontal geometry and other indispensable structures that make it compatible with the IC process such as metal fills and patterned ground shield (PGS). With the help of three-dimensional (3-D) electro-magnetic (EM) simulation software, the 3-D transformer model is simulated and the simulation result is got with high accuracy.

In this thesis an on-chip transformer for a fully integrated DC/DC converter using standard IC process is developed. Different types of transformers are modeled and simulated in HFSS. The performances are compared to select the optimum design. The effects of the additional structures including PGS and metal fills are also simulated. The transformer is tested with a network analyzer and the testing results show a good consistency with the simulation results when taking the chip traces, printed circuit board (PCB) traces, bond wires and SMA connectors into account.

DEDICATION

To My Parents

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CHAPTER 1

INTRODUCTION

1.1 Background

Isolated DC/DC converters, which realize the isolation using a high frequency transformer, have a wide use in many applications such as DC motor control, Programmable Logic Controller (PLC) and medical equipment [1]. The popular applications of isolated DC/DC converter are shown in Figure 1.1. For applications like DC motor control and PLC, the control circuit side needs to be isolated from the high voltage side to avoid the damage caused by the spikes of the operation of DC motors or magnetic contactors. For the medical equipment that has components directly contacting the patients, the patient should be isolated from the equipment power supply in case of something goes wrong with the AC power supply.

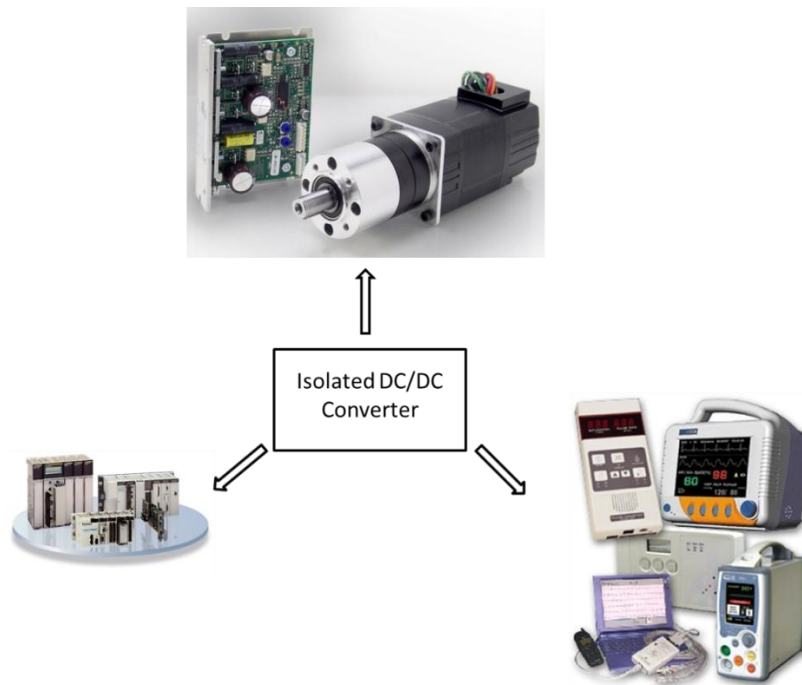


Figure 1.1. Popular Applications of Isolated DC/DC Converter

The transformer isolates the secondary side (output) from the primary side (input) electrically, realizing two DC voltage domains that can have different supply rails. This broken ground loop will protect the low-voltage side circuits from the electrical shock and over-voltage hazards caused by the high-voltage side circuits operation [1]. Besides, the noise conducted in the ground will be eliminated. The block diagram of an isolated DC/DC converter is shown in Figure 1.2. The converter consists of DC supply, oscillator, rectifier and regulator. The oscillator converts the steady DC voltage to alternating AC voltage and hence the AC current flowing through the primary side coil of the transformer. The varying current creates varying magnetic flux in the core (including air core) which induces a varying electromotive force or voltage across the secondary side coil [2]. For this reason, the primary side DC component cannot pass through the transformer and have an impact on the secondary side, and neither the secondary side to the primary side. After passing through the transformer, the AC voltage is rectified by the rectifier and then an optional regulator to the DC voltage again.

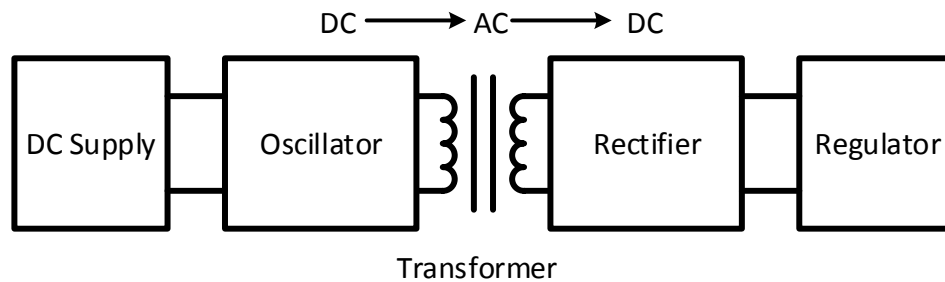


Figure 1.2. Block Diagram of Isolated DC/DC Converter

1.2 Overview of Isolated DC/DC Converter

Isolated DC/DC converters have a wide use in the industry world. Different kinds of such converters have been researched for specific purposes, some of which are readily

available on the market [3]. The converters can be basically categorized into three groups by the location of the transformer: Discrete Type, Partially Integrated Type and Fully Integrated Type.

1.2.1 Discrete Type

This kind of isolated DC/DC converter uses an external transformer which will be usually soldered on the printed circuit board (PCB). This external transformer can give isolation voltage rating from 1 to 6kV depending on the transformer's specs [4]. It provides flexibility for designers as they can optimize the transformers according to the requirements.

However, such a kind of converter also has certain drawbacks. The external transformer usually uses an iron core to provide tight electromagnetic coupling between the primary and secondary coils, which makes it bulky and may occupy a large board area. Although bringing flexibility that can allow the designers to choose the transformer by themselves, it also brings design difficulties that require the designer to have component selection experience in order to choose the proper transformer to meet the requirements. Also, the whole converter's reliability is not guaranteed since the transformer types are different, meaning it requires additional reliability test which will cost time as well as money. Figure 1.3 shows such a kind of converter.



Figure 1.3. Discrete Type Isolated DC/DC Converter (after [5])

1.2.2 Partially Integrated Type

To reduce the cost and make the system more compact and reliable, the partially integrated type isolated DC/DC converters come into picture. This kind of converter has an internal transformer in together with primary and secondary side circuits on the chip. The circuits and the transformer are usually fabricated separately and then assembled on the chip by using bond wires as inter-connections. Some high-end products of this type also has a feedback control circuits for high transfer efficiency [6]. Due to this integration, only a few peripheral components (basically decoupling and bypass capacitors) are required, thus the overall reliability can be guaranteed and the size of the converters can be reduced comparing with the discrete type.

The main drawback of such converter is that the isolation voltage rating and the output power is lower than the discrete type. And the transformer is fabricated separately which requires additional assembly work to connect it with other circuit blocks using bond wires. Figure 1.4 shows such a kind of converter.

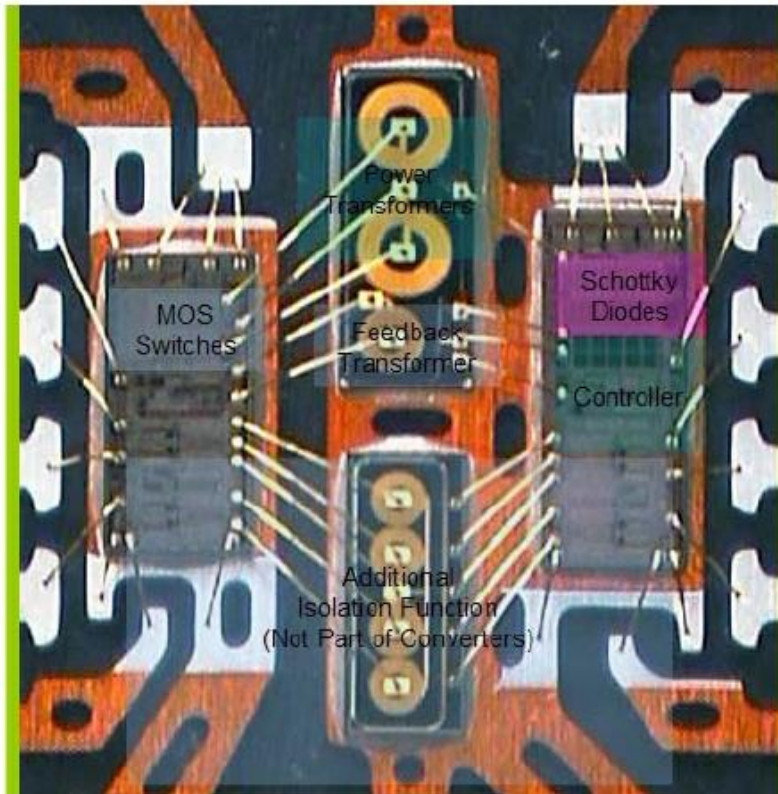


Figure 1.4. Partially Integrated Type DC/DC Converter (after [6])

1.2.3 Fully Integrated Type

Although the Partial Integrated DC/DC converter provides an on-chip solution to reduce the complexity of application, the cost of connecting circuit dies and transformer block using bond wires is still very high and is difficult to be synthesized in the standard IC process. Thus, a type of DC/DC converter that uses the same standard IC process for the circuits as well as the transformer has come to picture. This type reduces the cost of assembling different circuit blocks and transformer and makes the whole system more compact. Such a kind of transformer has already been applied in RF applications for impedance matching or providing interface between balanced and unbalanced circuits (balun) [7], [8]. Since the transformer is fabricated using the IC process, certain design

rules will limit the shape, structure and size of the transformer. Figure 1.5 shows an example of the on-chip transformer for balun application.

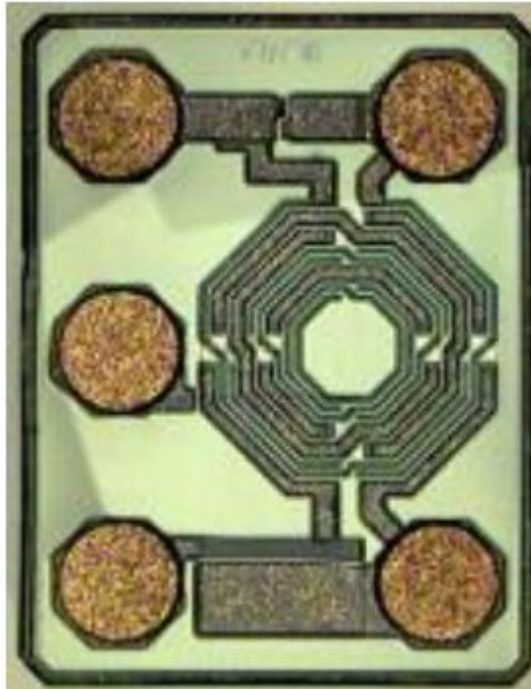


Figure 1.5. An Example of On-chip Transformer for Balun Application (after [9])

1.3 Thesis Organization

The organization of the thesis is as follows:

Chapter 2 shows the prior work of the isolated DC/DC converter and the on-chip transformer model. Chapter 3 shows the HFSS modeling and simulation results of the transformer. Chapter 4 shows the testing results of the test board and the comparison to the previous simulation results. Chapter 5 summarizes the thesis.

CHAPTER 2

PRIOR WORK OF DC/DC CONVERTER AND TRANSFORMER

2.1 Prior Work of Isolated DC/DC Converter

The block diagram of the isolated DC/DC converter is shown in Figure 1.2. Since the transformer can only pass AC power, the converter needs an oscillator to convert the steady DC voltage to the AC voltage across the primary coil. Two types of oscillators have been proposed: (1) the cross-coupled LC tank type and (2) the H-bridge driver type.

2.1.1 Cross-Coupled LC Tank Type Structure

A design of DC/DC converter with cross coupled LC tank oscillator is proposed in [6]. The block diagram is shown in Figure 2.1. The converter consists of LC self-resonant tank (including the primary side of the transformer), power transformer, rectifier with smoothing capacitor, voltage regulator and an optional feedback path for optimal power transfer.

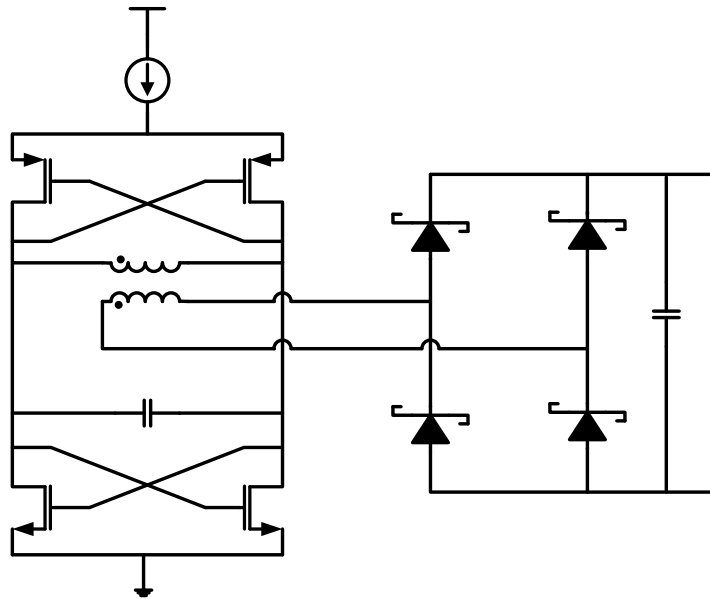


Figure 2.1. Cross-Coupled LC Tank Type Converter Schematic

One pair of PMOS switches and one pair of NMOS switches are cross-coupled to cancel the resistive loss and sustain the oscillation of the LC tank [6] [10]. The CMOS pair is used to achieve more positive gain because both the NMOS and PMOS are used to sustain the oscillation. Since the tank's inductor is the primary side coil of the power transformer which is coupled with the secondary side coil, the oscillation frequency will not only depend on the self-inductance of the primary coil and the primary capacitance, but also the mutual inductance and the secondary side load. The expression of the oscillation frequency will be discussed in section 2.3.

The rectifier consists of four Schottky diodes forming a full-wave bridge rectifier. The Schottky diode has a lower forward voltage comparing to the general purpose diode, thus it can provide lower forward voltage drop in the rectification which can provide higher system efficiency. Besides, the Schottky diode can turn on and recover faster if sized properly [6], thus it can operate at high frequencies which is important for this application since the operating frequency of the transformer is high due to the limitation of the size.

To obtain the optimal power transfer efficiency, an optional feedback path can be added. The feedback path consists of a PI controller, PWM controller, encoder, data transformer and decoder. The PWM signal controls the switching action of the CMOS switches and will not change the operation frequency of the LC tank.

2.1.2 H-Bridge Driver Type Structure

The cross-coupled LC tank does not have an interface for changing the resonant frequency. As shown in section 2.3, the resonant frequency changes with the load of the secondary side but cannot be changed by the switches. This characteristic, however, will

cause the EMI noise issue due to the single tone oscillation [11]. Besides, the voltage swing is limited because the cross-coupled pair and tail current source need certain voltage headroom to maintain their normal operations in the oscillation [10].

Thus, another type of DC-DC converter based on H-Bridge driver has been proposed to overcome the EMI noise and voltage swing issues. The schematic is shown in Figure 2.2. The overall structure is similar as the one shown in section 2.1.1 except a different primary side circuit.

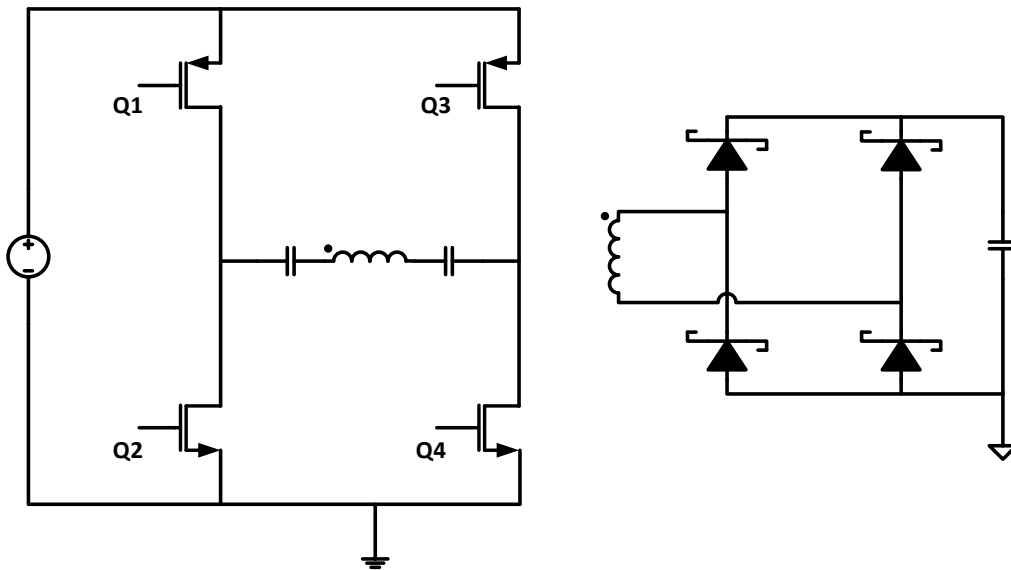


Figure 2.2. H-Bridge Type DC/DC Converter Schematic

The H-bridge consists of four switches: a pair of PMOSs at the top side and a pair of NMOSs at the bottom side. The control signal waveforms are shown in Figure 2.3. The non-overlapping clock signals are used to avoid creating short circuit path from supply to ground at the primary side. The MOS switches should be sized properly such that they have low series resistance to obtain less power consumption. The power transfer efficiency will be higher by using series LC tank since the current flowing through the

capacitor will also flow through the primary coil of the transformer. However, a parallel LC tank will have an issue that a large current will flow through the capacitor due to large dV_C/dt and consume more power.

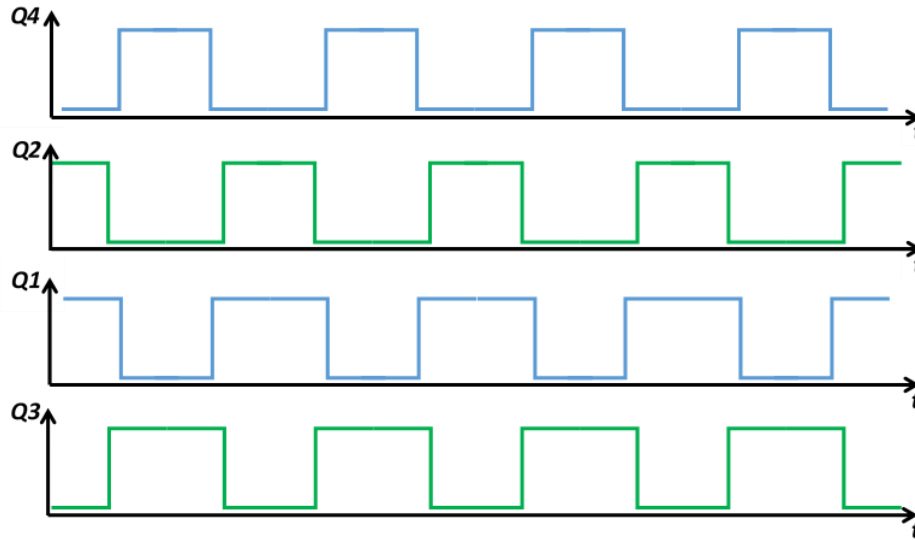


Figure 2.3. Non-Overlapping Clock Waveform

The structure shown in section 2.1.1 uses a global feedback scheme by using a data transformer to pass the encoded PWM control signal. The feedback network senses the output DC voltage and generates a PWM control signal based on the error signal between the sensed DC signal and the reference signal. This control signal passes through the data transformer after encoding at the secondary side and will turn on or off the cross-coupled LC tank after decoding at the primary side. This global feedback structure will provide optimal power transfer efficiency [6] at the cost of additional data transformer which may occupy a large chip area and hence a higher cost.

For our isolated DC/DC converters, we use local feedback. The idea is to change the clock frequency according to the sensed voltage amplitude across the primary side coil such that the driving frequency will sustain the maximum amplitude oscillation.

Also, the frequency can be changed using spectrum splitting technique to mitigate the EMI noise. The switching frequency is controlled by a ring oscillator based VCO, which has two input signals: (1) control signal from the primary side amplitude monitor and (2) control signal from spectrum spread circuits. The primary side circuits in together with the feedback circuit is shown in Figure 2.4.

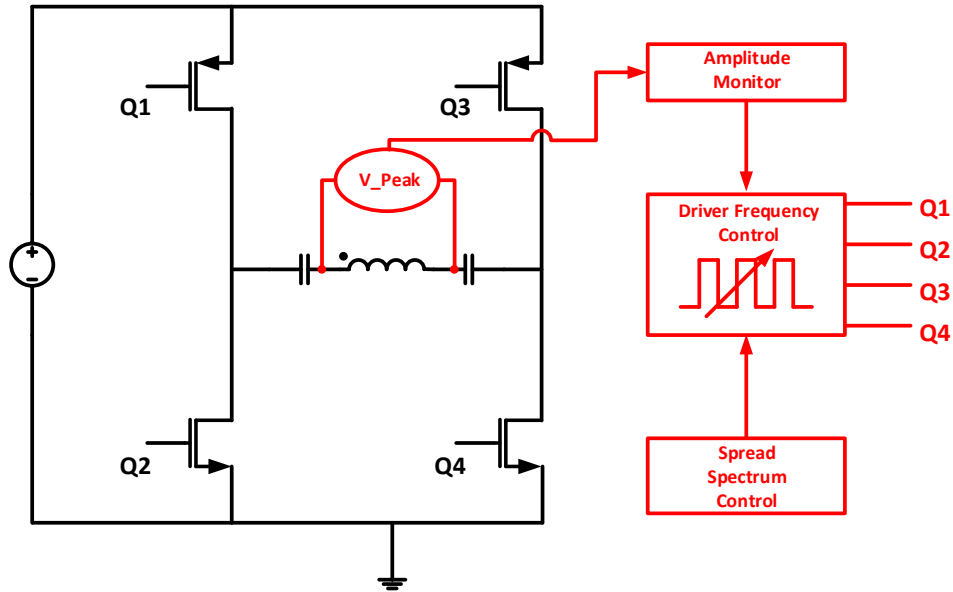


Figure 2.4. Primary Side Circuit with Local Feedback Circuit

2.2 Fundamentals of the Transformer

Figure 2.5 shows an ideal transformer circuit model. The transformer can be treated as an electromagnetic energy converter [12] which consists of two or more magnetically coupled coils. A time-varying voltage applied at the primary side causes a time-varying current to flow, thus causing a changing magnetic flux in the core. The changing magnetic flux will induce a voltage at the secondary side. The core, for most of the low frequency applications, is made of ferromagnetic metals which have high permeability that increase the magnetic field. However, for high frequency applications

like our case, the ferromagnetic core is not compatible with the process and will have magnetic saturation and core losses which degrade the Q factor of the transformer.

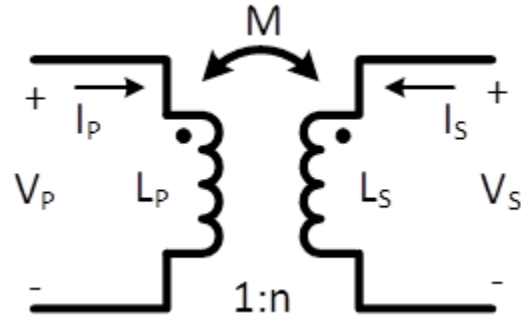


Figure 2.5. Ideal Transformer Circuit Model

The ideal transformer model can be treated as a two port network with the following terminal voltages and currents relationship:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} j\omega L_P & j\omega M \\ j\omega M & j\omega L_S \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (2.1)$$

where L_P and L_S are the self-inductance of the primary and secondary side coil. M is the mutual inductance between the two coils. For ideal transformer, the power transfer will be lossless and magnetic flux is confined in the magnetic core [2] [12], thus the following identity holds:

$$\frac{V_P}{V_S} = \frac{I_S}{I_P} = \frac{N_P}{N_S} = \sqrt{\frac{L_P}{L_S}} = n \quad (2.2)$$

where V_P and V_S are the primary and secondary voltage, I_P and I_S are the current flowing through the primary and secondary coil, N_P and N_S are the primary and secondary number of turns, n is for the turns ratio of transformer. Another important parameter to characterize a transformer is the coupling coefficient which is defined by:

$$k = \frac{M}{\sqrt{L_P L_S}} \quad (2.3)$$

If the two coils are perfectly coupled, $k=1$. Due to the leakage of magnetic flux caused by a lack of high permeability magnetic core in practical, the k for most on chip transformers is in the range of 0.3~0.9 [7] [13]. Other than imperfect coupling, non-idealities such as metal losses and substrate losses will be discussed in section 2.4.

2.3 Coupled Resonator Model

Before going to the practical model of the transformer, we develop a coupled resonator model based on the ideal transformer model. The coupled resonator model shows the power transfer principle of the transformer-based isolated DC/DC converters. As shown in Figure 2.6, the model consists of two LC tanks with coupled inductors. The model is simplified by ignoring the serial resistance of the inductors. This simplification is valid for studying the resonant frequencies since the resistance only causes the energy loss and will not affect the oscillation frequencies.

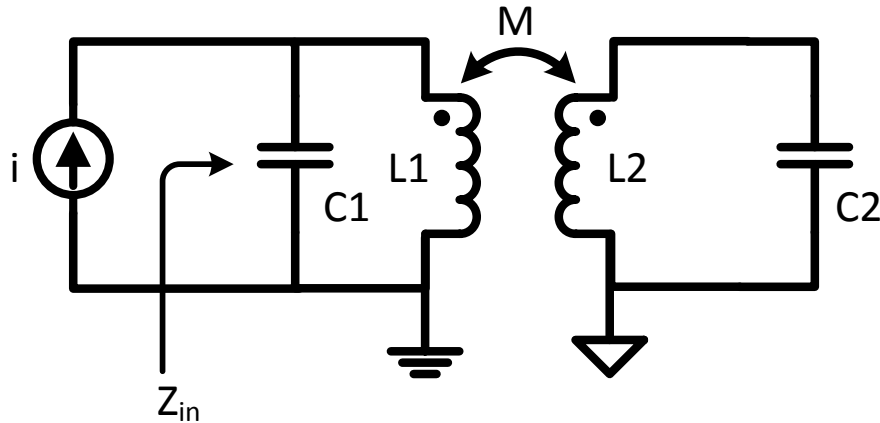


Figure 2.6. Coupled Resonator Model

The circuit oscillates at the frequency where the input impedance Z_{in} reaches its maximum value. To find out the expression for the input impedance seen at the primary

side, we need to equalize the model to the structure shown in Figure 2.7 based on the two-port network characteristics [14].

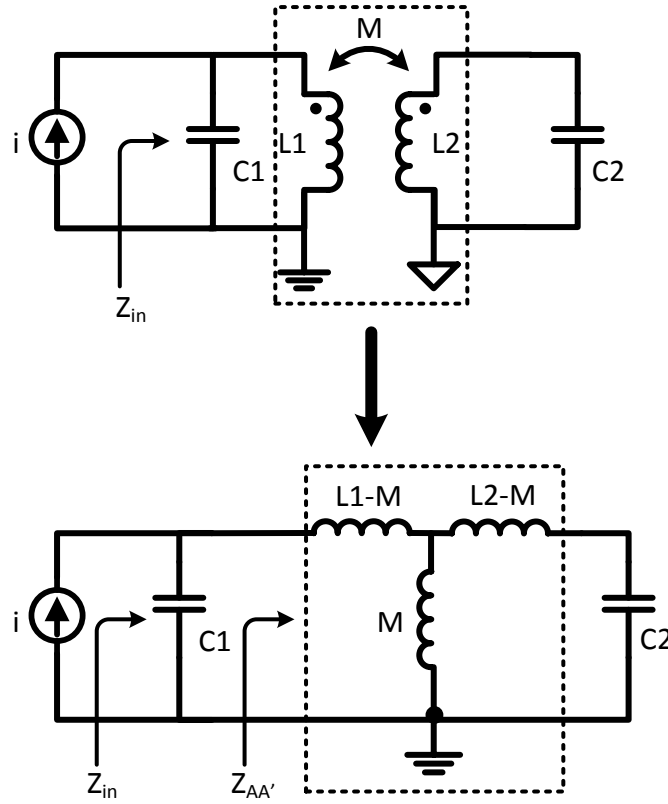


Figure 2.7. The Equivalent Circuit to Calculate Z_{in}

Then we can calculate the impedance seen at port AA':

$$Z_{AA'} = s(L_1 - M) + \left[s(L_2 - M) + \frac{1}{sC_2} \right] // sM \quad (2.4)$$

The overall input impedance is:

$$Z_{in} = Z_{AA'} // \frac{1}{sC_1} \quad (2.5)$$

From (2.4) and (2.5) we can get:

$$Z_{in} = \frac{sL_1 - s^3(C_2M^2 - C_2L_1L_2)}{(C_1C_2L_1L_2 - C_1C_2M^2)s^4 + (C_1L_1 + C_2L_2)s^2 + 1} \quad (2.6)$$

$|Z_{in}|$ reaches the maximum value when the denominator reaches zero, by solving equation (2.7)

$$(C_1C_2L_1L_2 - C_1C_2M^2)s^4 + (C_1L_1 + C_2L_2)s^2 + 1 = 0 \quad (2.7)$$

We get:

$$-\omega_{1,2}^2 = s_{1,2}^2 = \frac{(L_1C_1 + L_2C_2) \pm \sqrt{(L_2C_2 + L_1C_1)^2 + 4C_1C_2(M^2 - L_1L_2)}}{2C_1C_2(M^2 - L_1L_2)} \quad (2.8)$$

Equation (2.8) shows that equation (2.7) has 4 roots. However, $\omega > 0$ for the physical system. Thus, it has two roots:

$$\begin{cases} \omega_1 = \sqrt{\frac{-(L_1C_1 + L_2C_2) + \sqrt{(L_2C_2 + L_1C_1)^2 + 4C_1C_2(M^2 - L_1L_2)}}{2C_1C_2(M^2 - L_1L_2)}} \\ \omega_2 = \sqrt{\frac{-(L_1C_1 + L_2C_2) - \sqrt{(L_2C_2 + L_1C_1)^2 + 4C_1C_2(M^2 - L_1L_2)}}{2C_1C_2(M^2 - L_1L_2)}} \end{cases} \quad (2.9)$$

Equation (2.9) shows that there are two resonant frequencies for this resonant tank.

Specially, if $L_1=L_2=L$ and $C_1=C_2=C$, we can derive the following results:

$$\begin{cases} \omega_1 = \frac{1}{\sqrt{(L+M)C}} \\ \omega_2 = \frac{1}{\sqrt{(L-M)C}} \end{cases} \quad (2.10)$$

ω_1 can be treated as the resonant frequency of a capacitor with capacitance C and a inductor with inductance $(L+M)$; ω_2 can be treated as the resonant frequency of a capacitor with capacitance C and a inductor with inductance $(L-M)$. If the serial resistance R is considered, the Q -factor can be calculated as:

$$Q = \frac{1}{R} \sqrt{\frac{L}{C}} \quad (2.11)$$

It is obvious that the higher the inductance the higher the Q-factor when R and C remain the same. Thus, ω_1 has a higher Q than ω_2 .

2.4 Loss Mechanisms in Practical Transformer

Loss mechanisms of transformer are worth to be studied when designing high-Q transformer in order to have high power transfer efficiency. The performance of an on-chip transformer depends on its vertical structure (stack or planar), coil shape, trace width, trace thickness, trace separation, metal material and the size of the transformer [10] [13]. The losses can be categorized into metal losses and substrate losses.

2.4.1 Metal Losses

For practical transformers, the inductors will have series resistance and there is loss in the oscillation. According to the definition of quality factor Q shown in equation (2.12):

$$Q = 2\pi \frac{E_{stored}}{E_{dissipated}} = \frac{\omega L}{R} \quad (2.12)$$

where E_{stored} is the maximum energy stored per cycle, $E_{dissipated}$ is the energy dissipated per cycle, L and R are the inductance and resistance, we know the quality factor is infinity for ideal transformer and finite value for practical transformer. The higher the quality factor, the less the energy loss. When fabricating the transformers, the metals of finite conductivity are used. For the process we are using, the metal is aluminum whose conductivity is around 3.5×10^7 S/m. Some processes use gold [6] [10] and the conductivity is higher. The transformer coils are wound with such metals and will have resistance in series with the coil inductance that will dissipate power in the oscillation and make the quality factor a finite value. The resistance is dependent on the geometry of the

coil, such as trace length, cross-sectional area, especially at DC to lower frequencies. For a cubic conductor, the resistance can be expressed as:

$$R = \frac{l}{\sigma wt} \quad (2.13)$$

Where σ is the conductivity, l is the length of the metal trace and w is the metal width and t is the thickness of the metal layer. To achieve a lower resistance and hence a high-Q transformer, most of the IC processes give the option to build inductors or transformers using metal layers that are thicker and of higher conductivity [10].

At low frequencies, the resistance is dependent on the geometry of the metal trace and the conductivity of the metal only. The current density is distributed evenly as shown in Figure 2.8 (a). However at higher frequencies, there will be an AC resistance in series with the low frequency resistance. The AC resistance is formed due to the current density redistribution caused by skin effect, proximity effect at higher frequencies.

As shown in Figure 2.8 (b), when conducting alternating current, the current density is largest near the surface of the cross-section of a metal trace and decrease with increasing depths in the conductor, which is called the skin effect [10] [15]. The skin effect reduces the effective cross-section area of the conductor and will increase the resistance. In normal cases, the skin depth δ can be approximated by:

$$\delta = \sqrt{\frac{2}{\omega \mu \sigma}} \quad (2.14)$$

where ω is the frequency in rad/s, μ is the permeability in H/m and σ is the conductivity in S/m. This equation shows that the added resistance is dependent on the operating frequency. At high frequencies, the skin depth becomes smaller and the resistance is higher.

When a metal conductor is conducting alternating current, it creates an alternating magnetic field around it. This alternating magnetic field induces eddy current in adjacent metal conductors which will also change the current density distribution inside it. As shown in Figure 2.8 (c), for two adjacent metal conductors, the current density is higher at the outer edge than the inner edge. Similar as the skin effect, it reduces the effective cross-sectional area of the conductor and causes a resistance increasing with frequency [6]. This effect is addressed as proximity effect. In addition to the resistive loss, the proximity effect can also reduce the inductance since the eddy current generates a magnetic field that opposes the original change in the magnetic field [16].



Figure 2.8. Visual Representation of the Effect on Current Density Distribution in the Cross-Section of the Transformer Coil: (a) DC, (b) Skin Effect, and (c) Proximity Effect

2.4.2 Substrate Losses

On-chip transformers have to reside above a substrate. For standard IC process, the transformer is in parallel with the substrate with silicon dioxide layers in between, thus the flux generated by transformer will be perpendicular to the substrate and an electric field can also form between the transformer layer and the substrate. Since the Si substrate conductivity is in the range of 5~10S/m, current can be conducted in it and thus become lossy [6].

The substrate loss mainly comes from two aspects. The first aspect is the capacitive coupling between the metal conductor of the transformer and the substrate. Since the metal coil and the substrate can be treated as conductors and the oxide layer be treated as insulator, a parasitic capacitor is formed and will couple the electric energy from the coil to the substrate in the form of the displacement current [6]. This displacement current will flow through the lossy substrate to the ground.

The second aspect is the inductive coupling between the metal conductor of the transformer and the substrate. The conductive substrate is acting as an imaginary coil that couples the flux generated by the transformer coil and induces eddy current. Thus, the eddy current can flow through the lossy substrate. The displacement current and eddy current flowing through the lossy substrate generates ohmic losses. In addition, the eddy current flowing in the substrate will induce magnetic field that oppose the change of original magnetic field and hence reduce the inductance of the transformer coil. It is reported in [6] that the substrate losses increase with substrate conductivity and operation frequency.

To reduce the substrate loss, many approaches have been proposed. In [17], a 3-D transformer has been proposed as shown in Figure 2.9. The transformer is perpendicular to the substrate such that the generated magnetic field is in parallel with the substrate thus less flux will penetrate into the substrate. As a result, the eddy current reduces and so does the substrate loss. However, this approach is not compatible with most of the standard IC process. Another approach is to reduce the substrate conductivity by using GaAs substrate that is commonly used in RF processes. The GaAs substrate has conductivity in the range of $1 \times 10^{-6} \sim 1 \times 10^{-5} \text{S/m}$, thus the current will be reduced. To

reduce the substrate loss in the standard IC process using Si substrate, a Patterned Ground Shield (PGS) is always built to reduce the substrate loss. The detailed discussion on PGS is presented in Chapter 3.

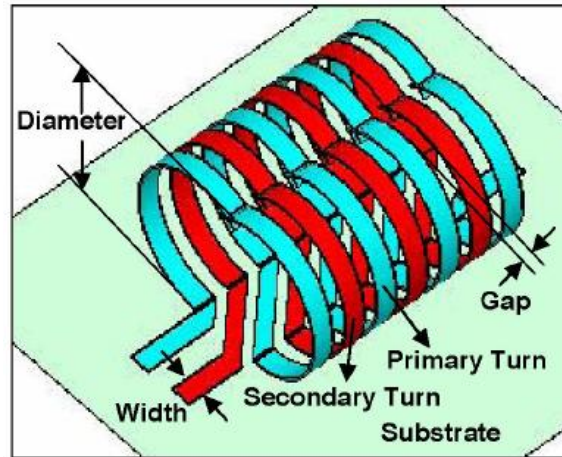


Figure 2.9. A 3-D Transformer Structure

2.5 Practical Transformer Model

According to the analysis of metal losses and substrate losses shown above, we build a practical transformer model that mimics the behavior of on-chip transformer at high frequencies shown in Figure 2.10. The model has resistance in series to mimic the metal loss of the inductor (R_P and R_S), the resistance is frequency dependent to emulate the skin and proximity effect. Other than mutual inductance M , the model also shows the mutual capacitance effect by C_M since the two coils are separated by silicon-dioxide layer and the capacitor can be formed. C_P and C_S show the terminal-to-terminal capacitance which may short the inductor at high frequencies. To emulate the substrate loss, the block consisting C_{OX} , C_{SUB} and R_{SUB} is used which shows the substrate current loss and capacitive coupling between the coils and the substrate.

Although we can build circuit model consisting of resistors, capacitors and inductors to emulate the on-chip transformer for a certain frequency range, it is still difficult for using the model and relying on the simulation results of this model since the values for the resistance, capacitance and inductance are not easily and accurately calculated. For example, the self-inductance L_P and L_S highly depend on the geometry of the coils; the mutual-inductance is dependent on the structure of the transformer (planar or stack structure); the series resistance R_P and R_S are dependent on the cross-sectional area, coil length and the material of the metal at DC to lower frequencies but will be frequency dependent at higher frequencies. Thus, it is better to use 3-D EM simulation software such as HFSS to get the accurate results.

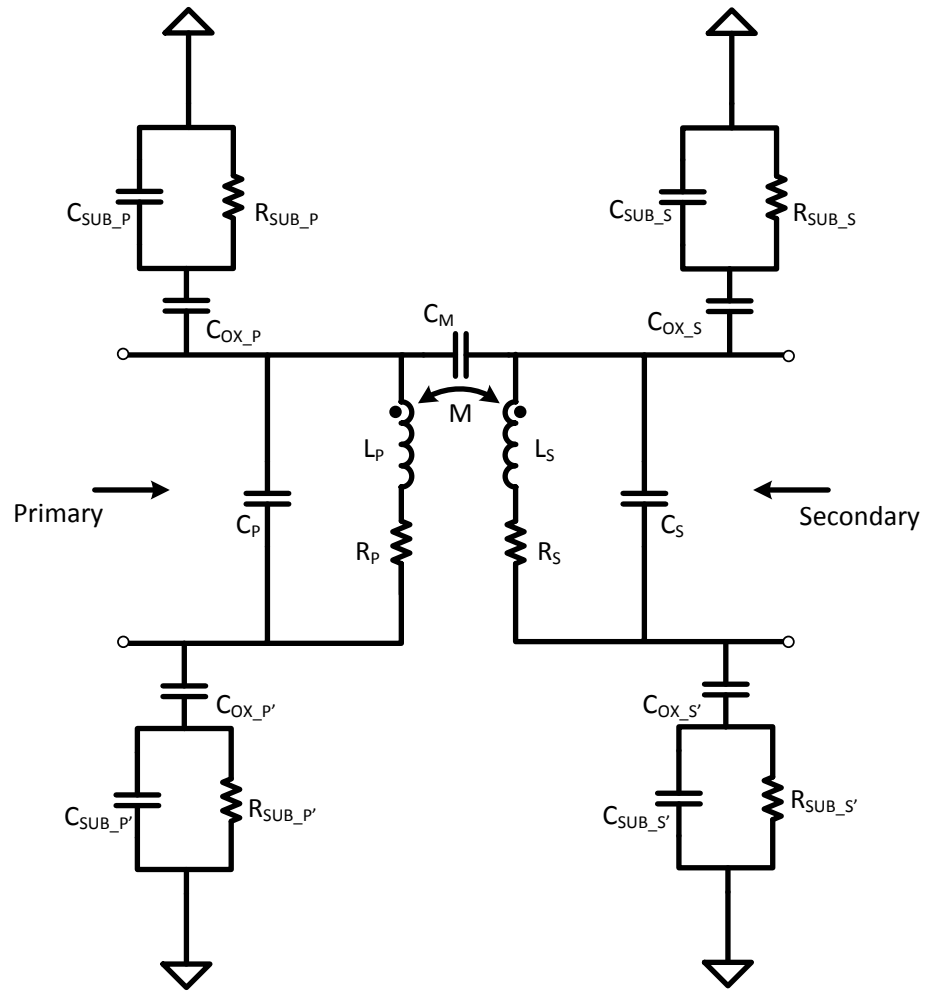


Figure 2.10. A Practical Transformer Model.

CHAPTER 3

HFSS MODELING AND SIMULATION

3.1 Transformer Modeling and Simulation Tool: HFSS

As discussed in section 2.5, a 3-D EM simulation software is needed to get an accurate transformer model. There are many different kinds of commercial EM simulation software available on the market and among them we choose HFSS. HFSS is a full 3-D modeling and simulation software that is believed to have high accuracy. For our case, we need to draw the 3-D structure of the transformer, specify material characteristics for each object and identify the excitation ports. HFSS then solves the model using finite-element-method and generates S-parameter matrix. We can either choose to solve the model at a specific frequency or at several frequencies within a range.

The specifications of the transformer can be calculated by the S-parameters, among which we focus on the coil inductance L , quality factor Q and coupling coefficient k . In the simulation, we set the primary side port to be port 1 and the secondary side port to be port 2. Thus the specifications can be calculated by:

$$L_P = \frac{im(Z_{11})}{2\pi f} \quad (3.1)$$

$$L_S = \frac{im(Z_{22})}{2\pi f} \quad (3.2)$$

$$Q_P = \frac{im(Z_{11})}{re(Z_{11})} \quad (3.3)$$

$$Q_S = \frac{im(Z_{22})}{re(Z_{22})} \quad (3.4)$$

$$k = \frac{\sqrt{im(Z_{12})im(Z_{21})}}{\sqrt{im(Z_{11})im(Z_{22})}} \quad (3.5)$$

where L_P , L_S , Q_P , Q_S and k are respectively for the primary side inductance, secondary side inductance, primary side quality factor, secondary side quality factor and coupling coefficient between the two coils.

For the on-chip transformer of the isolated DC/DC converter, we need high coil inductance. As discussed in section 2.3, the resonant frequency ω_0 and inductance value L have a relationship:

$$\omega_0 \propto \frac{1}{\sqrt{L}} \quad (3.6)$$

thus, higher inductance value will give lower resonant frequency and hence the H-bridge driver can drive the LC tank at a lower frequency. This will reduce the switching loss happening at higher frequencies and also avoid transformer's non-idealities such as skin effect, proximity effect and substrate eddy current that come with high frequencies.

Since the transformer operates at the oscillation frequency of the coupled resonant tank shown in section 2.3. We need high Q inductors such that the energy loss is small in the oscillation. Equation (2.12) shows that the lower the dissipated energy, the higher the quality factor. Thus, we use quality factor to compare different transformers' energy loss.

For the on-chip transformer, we need high coupling coefficient k between the two coils. In [18], one approach to calculate the power transfer efficiency η is given:

$$\eta = \frac{(k \cdot Q)^2}{[1 + \sqrt{1 + (k \cdot Q)^2}]^2} \quad (3.7)$$

where k is the coupling coefficient and Q is the quality factor. Figure 3.1 shows the power transfer efficiency versus coupling coefficient for different Q values. We can observe that efficiency increases with increasing coupling coefficient.

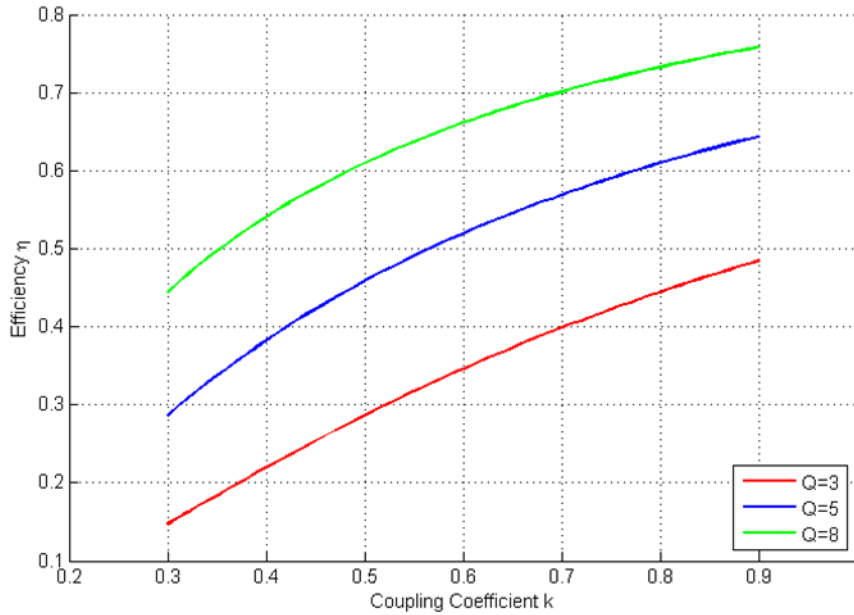


Figure 3.1. Efficiency vs. Coupling Coefficient for Different Q

According to the analysis shown above, we set the operating frequency of the transformer to be around 100MHz and expect high coil inductance, high Q-factor and high coupling coefficient between the two coils.

3.2 Vertical Structure Comparison: Planar Type vs. Stack Type

The on-chip transformers can be categorized into two types according to the vertical structure: planar transformer and stack transformer. It has been reported in [7] [13] [19] that the stacked transformer has the advantage of smaller coil area and higher coupling coefficient but has the disadvantage of lower Q comparing to the planar transformer especially for the processes that only have one thick metal layer.

We use a 180nm high voltage process based on the isolation requirement of the converter. The process has 6 layers of metal with the thickest metal layer at the top. And also, the thickest metal layer sits on the thickest oxide layer, making it far away from the

lower level metals. The five lower level metals have much thinner thickness than the top level metal and have certain metal density rules. The process has a poly-silicon layer that sits just on top of the substrate and the conductivity is lower than metal. In HFSS model design, the thickness of each metal and insulate layer is set to be the nominal value shown in the PDK manual. However, in the practical case, the thickness has a range to vary and this may cause some discrepancies between the simulation and measurement results. In the PDK manual, the conductivity of the metal layer is given in the form of sheet resistance. It is converted to bulk conductivity by equation (3.8) since HFSS material library can only accept this parameter.

$$\sigma = \frac{1}{R_S \cdot t} \quad (3.8)$$

Where σ is the bulk conductivity, R_S is the sheet resistance and t is the thickness of the layer.

To compare the performance in our frequency range, we build one stack transformer and one planar transformer shown in Figure 3.2. For the stacked transformer, it uses AM layer to build the secondary coil, MT layer for the under pass structures of the primary and secondary coils, and M4 for the primary coil. The vertical distance between the coils is 5.13 μm . For the planar transformer, it uses AM layer for both of the coils and MT, M4 for the under pass structures.

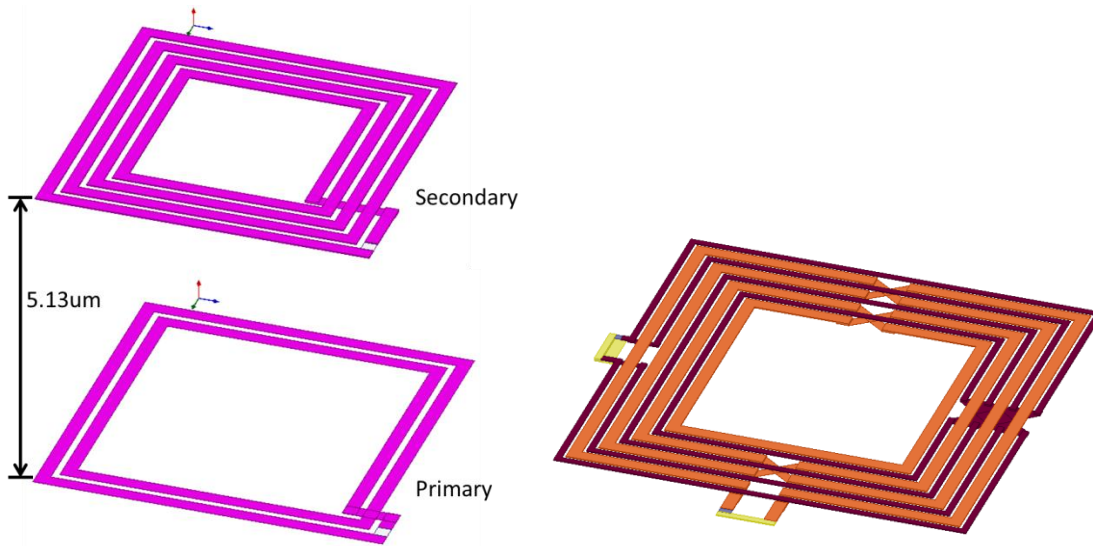


Figure 3.2. Two Vertical Structures of On-Chip Transformer: (a) Stack Type and (b) Planar Type

In the vertical structure, the stack transformer using two metal layers separated 5.13 μm away to build the coils; a metal layer to build underpasses is also required. Thus, 3 layers are used to build this transformer. For the planar transformer, both of the coils are built in the same layer. Two lower layers of metal are used to build the underpasses. Also, it will take 3 layers of metal to build the planar transformer.

For the horizontal geometry, we introduce the parameters: number of turns n , outer dimension d_{out} , inner dimension d_{in} , trace width w and adjacent trace separation s to describe the geometry of the spiral coil, the definitions of these parameters are shown in Figure 3.3. For the planar transformer, we use interleaving technique to split the primary coil into two parallel coils, the total trace width of whom is the same as the one of the secondary coil. Both of the transformers have a winding turns ratio $n=2$ with 2 turns at the primary side and 4 turns at the secondary side. Although shown in the stack type transformer, the definition is also applied to planar type transformer.

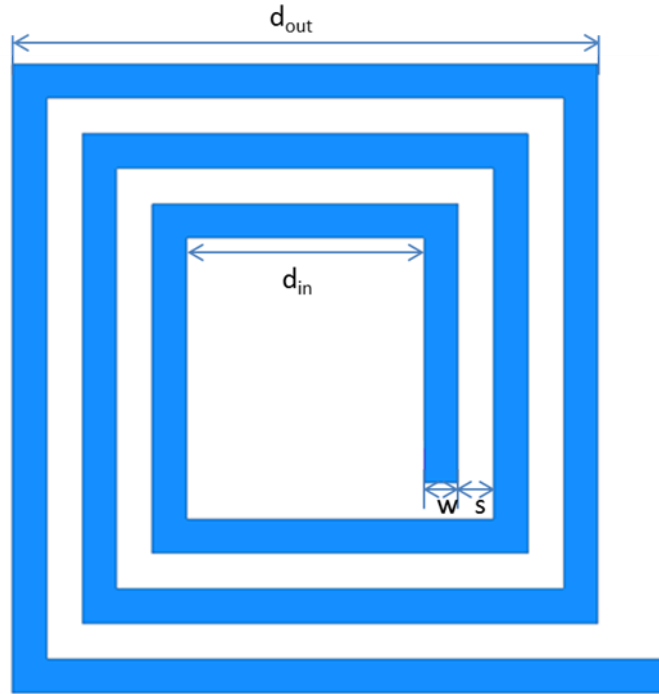


Figure 3.3. Horizontal Geometry of the Coil

The geometry parameters for the two transformers are listed in Table 3.1 and the simulation results at 100 MHz are shown in Table 3.2. The simulation results show that the stack type transformer gives higher primary side inductance with a smaller covering area comparing to the planar type, which is an advantage of lowering the operation frequency of the coupled resonant tank. However, the Q-factor for primary side coil is quite low comparing to the planar type. This is because the primary side coil is fabricated using M4 layer (0.48 μm thick) making the series resistance quite large, which causes metal loss as discussed in Chapter 2. Besides, the coupling coefficient of stack type is smaller than planar type, which is caused by the increased separation between the two coils due to the sandwiched layer for underpasses and the thick oxide layer (4.1 μm thick). As a result, we should use planar type transformer for better coil Q-factor and better coupling coefficient.

Table 3.1. The Geometry Parameters for the Stack and Planar Type Transformers

		$d_{out}/\mu\text{m}$	$d_{in}/\mu\text{m}$	$w/\mu\text{m}$	$s/\mu\text{m}$
Stack Type	Primary	917	550	50	25
	Secondary	917	142	50	25
Planar Type	Primary	1783	1091	2×26.6	106
	Secondary	1702	958	53.2	53.2

Table 3.2. Simulation Results: Stack and Planar Type Transformers

	k	L_P	L_S	Q_P	Q_S
Stack Type	0.75	20.8nH	45.3nH	0.93	6.60
Planar Type	0.86	14.4nH	53.0nH	3.81	5.74

3.3 Horizontal Geometry Comparison: Octagonal Type vs. Square Type

For the horizontal geometry of the transformer, we can choose not only the square shape but also the octagonal shape according to the IC process design rule. The octagonal shape has the advantage of smaller covering area and short trace length comparing to its square shape counterpart, which allows us to build other circuits in the blank area at the corners. We simulated these two models in the frequency range that our transformer will work in. Figure 3.4 shows the top-down view of the two transformers. For both of the transformers, $N_P:N_S=2:4$, $d_{out}=1.782\mu\text{m}$, $d_{in}=958\mu\text{m}$, $w=53.2\mu\text{m}$, $s_{Pri}=79.8\mu\text{m}$, $s_{Sec}=53.2\mu\text{m}$. The simulation results at 100 MHz are shown in Table 3.3 as below. The simulation results show that the coupling coefficient of the two transformers are close to each other. The square transformer has a primary inductance 1nH and secondary 5.2nH higher than the square shape. The contribution of the mutual inductance between the

segments in the octagonal shape is not so significant comparing to the longer trace length and larger covering area of the square shape transformer. For Q-factors comparison, square shape is slightly better than the octagonal one at 100MHz and will be much higher at higher frequencies. Thus, we choose the square shape to obtain higher inductance and lower losses.

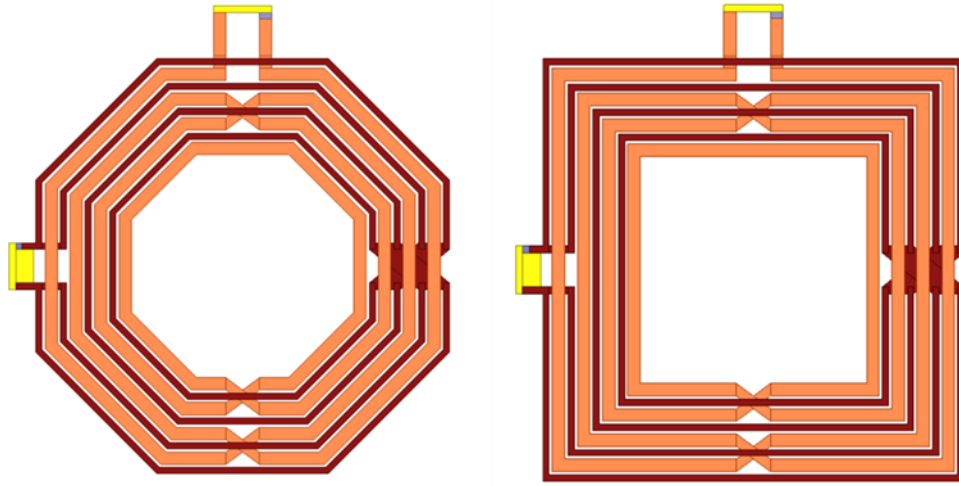


Figure 3.4. The Top-Down View of the Transformers: (a) Octagonal Type and (b) Square Type

Table 3.3. Simulation Results: Octagonal and Square Shape Transformers

	k	L_P	L_S	Q_P	Q_S
Octagonal	0.87	13.4nH	47.8nH	3.7	5.5
Square	0.86	14.4nH	53.0nH	3.81	5.74

3.4 Patterned Ground Shield (PGS) Effect

At higher frequencies, the magnetic field generated by the transformer will induce eddy current on the lossy substrate. To reduce the loss, we need a ground shield to reduce the eddy current and provide a ground connection. Thus, a PGS is often built underneath

inductors and transformers for high frequency applications. To block the eddy current loop on the shield, it is slotted in the pattern shown in Figure 3.5. The X pattern provides connection of each segment to ground. To see the effect of the PGS in our transformer, we built 3 models for simulation: (1) transformer without a PGS; (2) transformer with a metal M1 layer PGS, and (3) transformer with a poly-silicon layer PGS. The width of the strip is 36um and the width of the slot is also 36um.

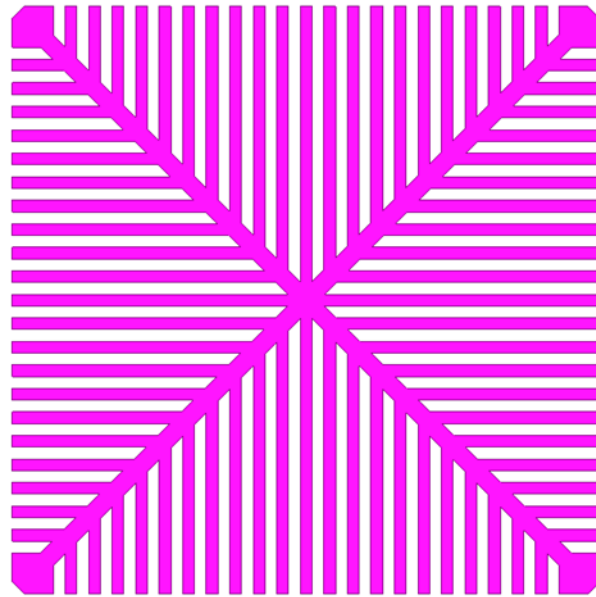


Figure 3.5. Patterned Ground Shield Structure of the Transformer

The simulation results at 100MHz are shown in Table 3.4. From the simulation results we observe that the transformers with PGS have a higher inductance value comparing to the one without a PGS; for transformers with metal PGS, the quality factor will be degraded comparing to the one with poly-silicon PGS and the one without a PGS. The reason for this degradation is that the metal layer sits closer to the coil layer than the poly-silicon, creating a higher capacitance with the coil. The parasitic capacitance will degrade Q. In addition, the PGS can reduce the effect of eddy current but cannot

eliminate it. A portion of the eddy current still exists. The metal layer has a higher conductivity than the poly-silicon, thus will have a higher residue eddy current and more loss. As a result, we use a poly-silicon PGS in our design.

Table 3.4. Simulation Results: without PGS, with Poly-Silicon PGS and with Metal PGS

	k	L _P	L _S	Q _P	Q _S
No PGS	0.84	9.8nH	33.3nH	3.34	5.87
Poly-silicon PGS	0.86	14.4nH	53.0nH	3.81	5.74
Metal PGS	0.83	11.2nH	37.8nH	2.31	2.8

3.5 Metal Fills Effect

Many standard IC processes require uniform metal density in the chemical-mechanical polishing (CMP) process [20]. Thus, the metal fills are put in the metal layers being used (except for the top layer where the transformer coils are built). The metal fill consists of an array of small dummy floating metal squares. To study the effect of the metal fills to the performance of the transformer, we firstly finish the layout in cadence and add the metal fills to meet the density rules, and then we add the metal fills in the simulation model at the same position as the layout. The only different thing is the single dummy metal square's size. The simulation time will be long if we use the same metal fill size as the one in the layout, thus we enlarged the individual metal fill by merging every 3×3 array to be a solid fill. This simplification of the model can give us a hint on the metal fill effect and save the simulation time. Figure 3.6 shows the areas where to put the metal fills. The PGS is not shown for simplicity. The green square shows the metal fills consisting of M2~MT layers and the blue square area shows the metal fills of M1

layer. Where M2~MT are the 2nd to 5th layers of metal from substrate and M1 is the 1st layer of metal.

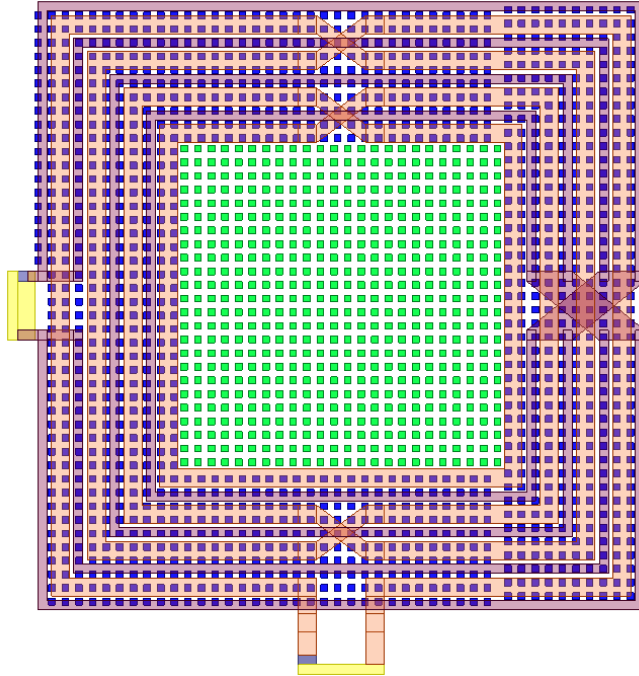


Figure 3.6. The Metal Fills Position of the Transformer Chip

The results of the simulation is shown in Table 3.5. We can observe that the metal fills almost have no effect to the performance of the transformer in the sense of inductance value, Q-factor and coupling coefficient. This is mainly because the size of the metal fill is too small to generate significant eddy current. Thus the loss caused by eddy current is small. The M1 layer fills area is overlapped with the transformer coil area, which will decrease the distance from the coil to the PGS and substrate since M1 layer has physical thickness. Thus, the parasitic capacitance will increase with decreased distance due to the sandwiched metal layer. However, this effect is also not so significant since the M1 layer is thinner than the other metal layers.

Table 3.5. Simulation Results: with Metal Fills and without Metal Fills

	k	L _P	L _S	Q _P	Q _S
With Metal Fills	0.86	14.6nH	53.5nH	3.9	5.9
Without Metal Fills	0.86	14.4nH	53.0nH	3.8	5.7

CHAPTER 4

TESTING RESULTS

The proposed on-chip transformer together with the Schottky diode based full-wave rectifier are implemented in high voltage AMS H18A6 0.18 μm CMOS process. The die micrograph is shown in Figure 4.1. The chip size is 2.236mm by 2.236mm. The transformer block size is 1.783mm by 1.783mm.

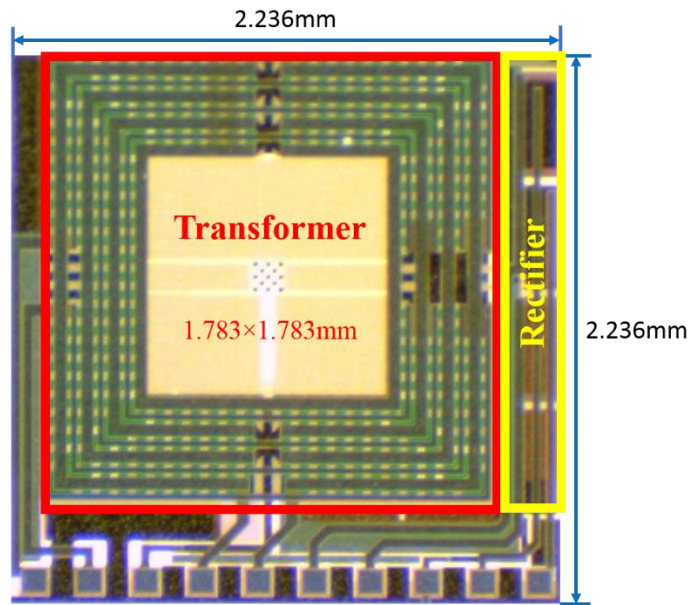


Figure 4.1. Test Chip Die Photo

4.1 PCB Design and Test Setup

A test printed circuit board (PCB) is designed for testing the transformer with network analyzer and using external components to verify the structure of the H-bridge type DC/DC converter. The PCB has two metal layers and the copper thickness is 34.79 μm . The size of the PCB is 7.4cm by 6.7cm. The photo of the PCB with all components assembled is shown in Figure 4.2.

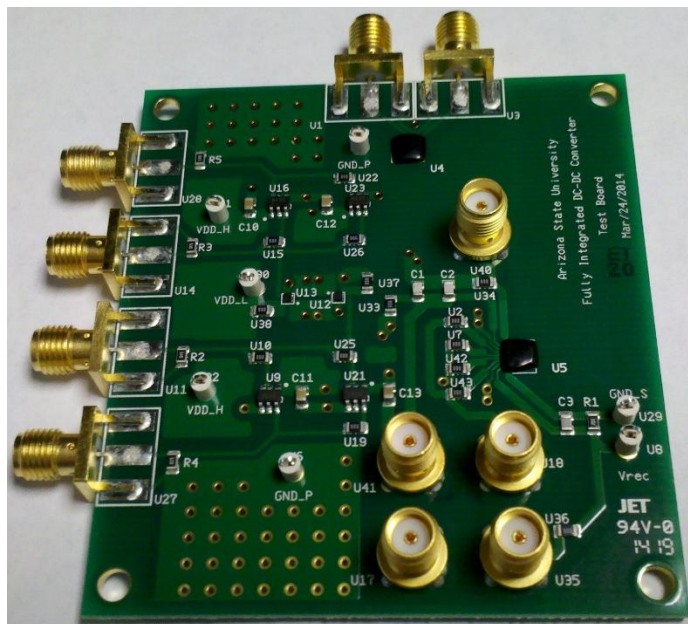


Figure 4.2. Test Board Photo

The boards can be configured using zero-ohm resistors for different purposes of testing including comprehensive testing for the whole DC/DC converter, transformer testing and rectifier testing.

The lab setup for the transformer testing is shown in Figure 4.3. The network analyzer is used for testing with its port 1 connected to the primary coil and port 2 connected to the secondary coil. The SMA cables and connectors are used for connection. The network analyzer is calibrated with these additional cables and connectors before testing. The Network analyzer is set to the average mode during the test.

The Network analyzer sweeps the frequency from 10MHz to 500MHz to measure the S-parameters. It generates a *.s2p file containing the s-parameter matrix which is exported to the Matlab script for calculations. The script convert the S-parameters to Z-parameters and calculates the k, Q and coil inductance.

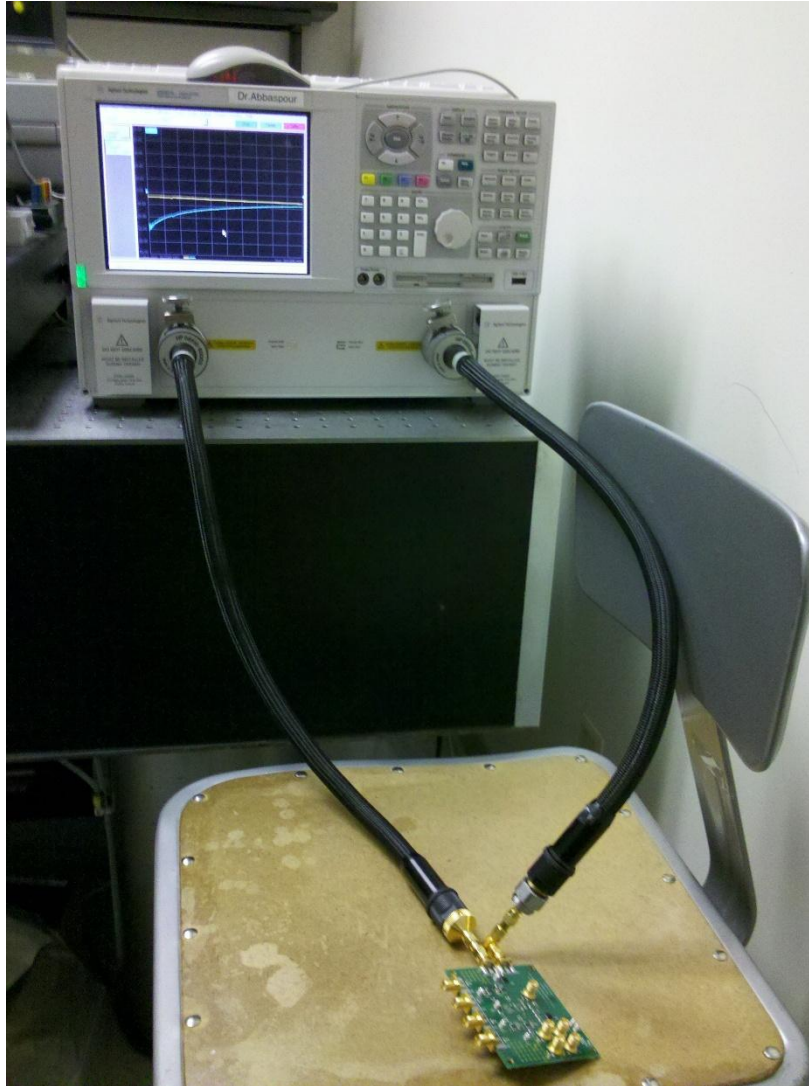
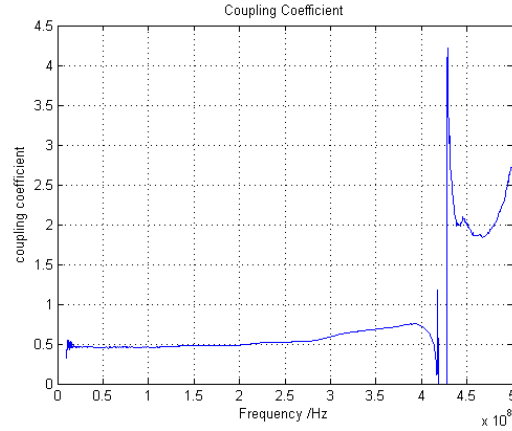


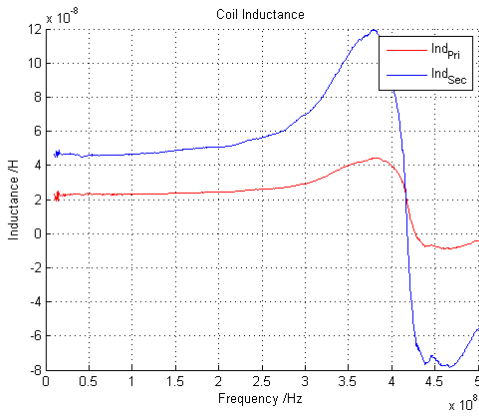
Figure 4.3. Lab Setup for Transformer Testing

4.2 Measurement Results

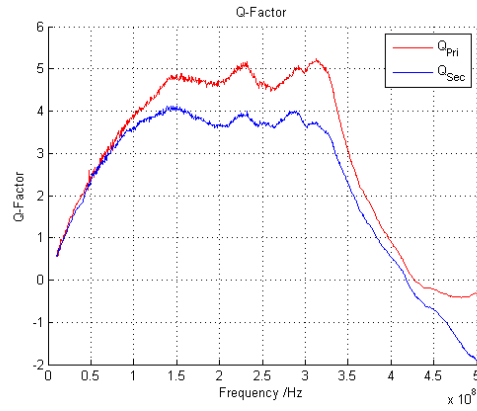
Five PCBs are manufactured, assembled and tested. The following measurement results show the typical data we collected. The measurement results got from Network analyzer is shown in Figure 4.4. At 100MHz, $k=0.46$, $L_P=23.0\text{nH}$, $L_S=46.7\text{nH}$, $Q_P=3.9$ and $Q_S=3.65$.



(a)



(b)



(c)

Figure 4.4. Testing Results of the Transformer: (a) Coupling Coefficient, (b) Coil Inductance and (c) Q-Factor

We can observe that the coupling coefficient decreases to 0.46 at around 100MHz, which is much lower than the simulation results. The reason for this discrepancy is the additional inductance contribution of the bond wires and the PCB routing traces. For example, the PCB traces contribute around 10nH for each side while having no mutual inductance between the two sides. Thus, according to equation (2.3), the k will be decreased.

4.3 Comparison of the Simulation Results and the Measurement Results

To make the simulation model of HFSS comparable to the real chip tested with network analyzer, we add the bond wires, PCB routing traces and SMA connectors similar as the actual layout of the PCB. The test chip also has on-chip traces to route the transformer terminals to the bond pads, which are also added in the simulation model. Certain simplifications are applied to reduce the complexity of the model and save the simulation time. For example, the bond wire shape is simplified as shown in Figure 4.5. The cross-sectional view of the bond wire is changed from round to octagonal shape.



Figure 4.5. Bond Wire Model Simplification

The 3-D model for HFSS simulation is shown in Figure 4.6. The model includes test chip, bond wires, PCB traces and SMA connectors. The SMA connectors' pins are coated with solder and the ground pin of the test chip is connected to the SMA ground pin using solder. This emulates what we did in the test board and can give accurate results. The metal fills are not added according to the analysis in section 3.5. This helps reduce the complexity of the model while maintaining the same accuracy. The simulation sweeping frequency range is from 10MHz to 500MHz to make it comparable with the measurements.

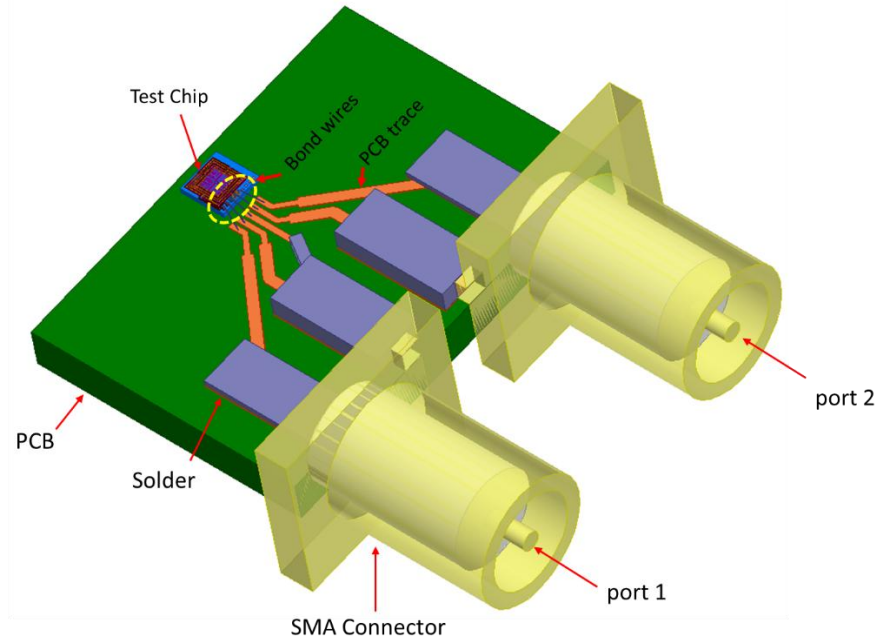
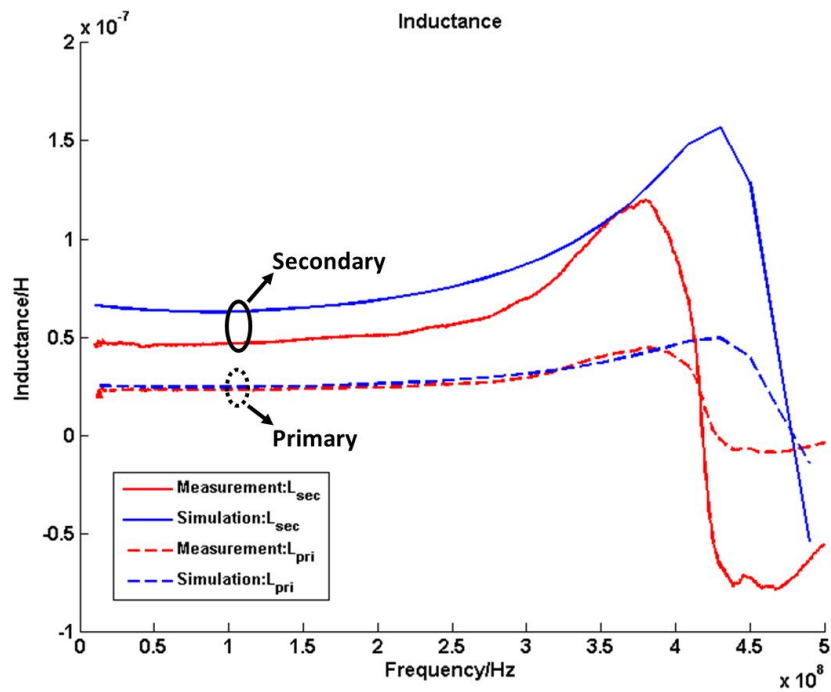
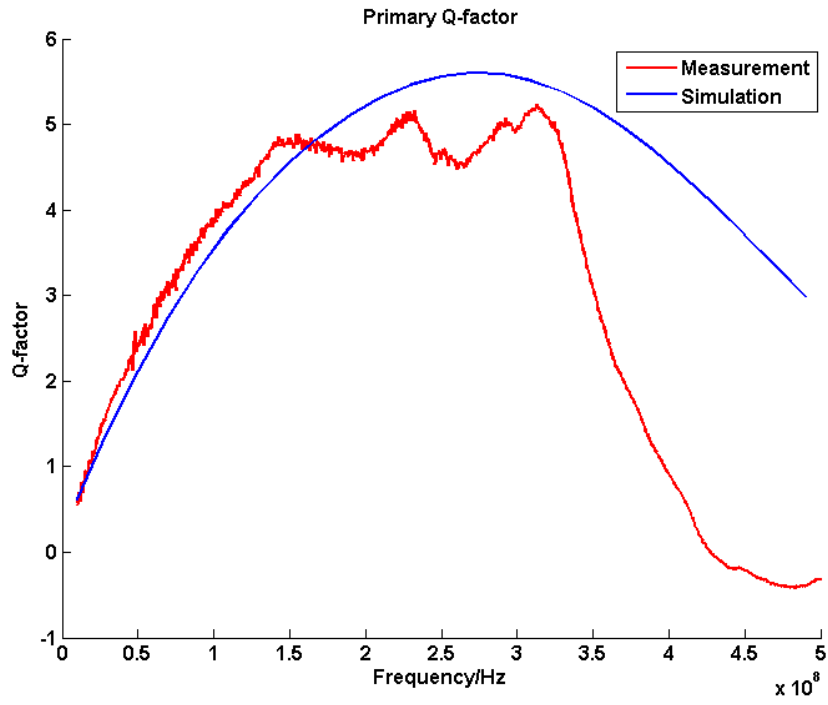


Figure 4.6. Model for HFSS Simulation

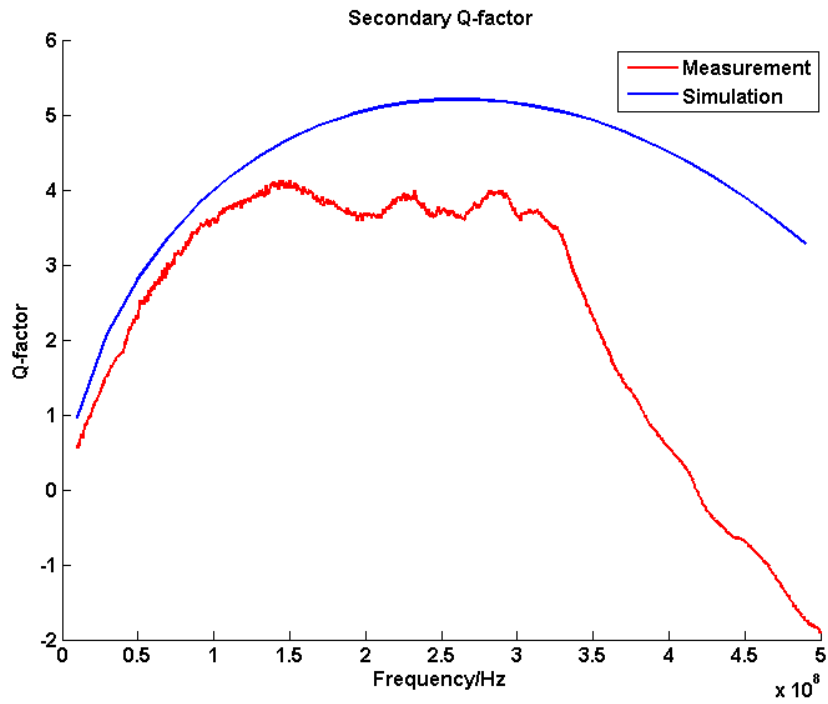
The testing and simulation Results are shown in Figure 4.7.



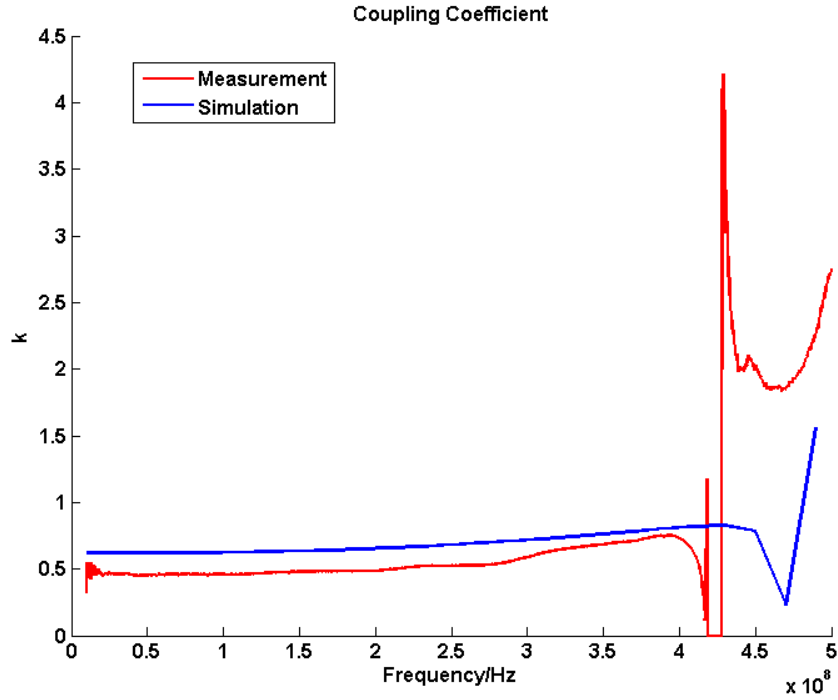
(a)



(b)



(c)



(d)

Figure 4.7. Measurement and Simulation Results Comparison: (a) Primary and Secondary Inductance, (b) Primary Q, (c) Secondary Q and (d) Coupling Coefficient

The data at 100MHz is shown in Table 4.1. We can observe that the difference between the measurement and simulation is small at 100MHz around which will the H-bridge operate.

Table 4.1. Measurement and Simulation Results Comparison

	k	L_P	L_S	Q_P	Q_S
Measurement	0.46	23.1nH	46.7nH	3.9	3.6
Simulation	0.62	24.5nH	63.0nH	3.53	4.0
Δ	0.16	1.4nH	16.3nH	0.37	0.4

CHAPTER 5

CONCLUSION AND FUTURE WORK.

An on-chip transformer for an isolated DC/DC Converter is developed. To get an accurate model, the 3-D EM simulation software HFSS is used to design and simulate the transformer model. The simulation results on coupling coefficient, coil inductance and coil quality factors of different vertical structures, horizontal geometry shapes are compared to select the optimal design that is compatible with the IC process. The planar vertical structure with square horizontal structure is selected for higher quality factor and coil inductance. Other structures' effects such as PGS and metal fills are also simulated. PGS made by poly silicon layer shows a better result in the sense of high quality factor and inductance. The metal fills don't have significant effect to the performance of the transformer in the frequency range we expect the transformer to operate. The on-chip transformer test chip has been fabricated and tested with PCB board. The measurement is performed by network analyzer and the result is compared with the simulation result of the model that has on-chip trace, bond wires, PCB traces and SMA connectors. The simulation results show a good consistency with the measurement.

To directly test the transformer without de-embedding the contribution of on-chip traces, bond-wires, PCB traces and SMA connectors, it is better to use the probe station with ground-signal-ground (GSG) probe to test it. To further reduce the chip area, the other circuit blocks can be implemented in the center hallow area. The effects of this implementation is worth studying in the future.

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APPENDIX A

MATLAB CODE FOR PROCESSING S2P FILE


```

%%% This script converts the *.s2p file to the z-parameters
and
%%% s-parameters matrix and then calculate the Q,
inductance and coupling
%%% coefficient based on z-parameters.

%%%-----
-----
%%% Step_1: Import S-parameter file and convert it to Z-
parameter matrix
%%%-----
-----

% Enter the directory of the S-parameter file. MUST be the
same dir.
hz = zparameters('YOUR_s2p_FILE_DIRECTORY');
hs = sparameters('YOUR_s2p_FILE_DIRECTORY');

% zpara is a (2*2*Num_of_Freq_Points) complex matrix that
holds zParameters
% spara is a (2*2*Num_of_Freq_Points) complex matrix that
holds sParameters
zpara = hz.Parameters;
spara = hs.Parameters;

% Frequency Points: Start @10MHz, Stop @200MHz, 801 pts
(step=237.5KHz)
Freq = linspace(10e6,200e6,801);

%%%-----
-----
%%% Step_2: Calculation of the parameters based on Z-
parameter matrix
%%%-----
-----

Cpl_Coe = zeros(1,801);
Ind_Pri = zeros(1,801);
Ind_Sec = zeros(1,801);
Q_Pri = zeros(1,801);
Q_Sec = zeros(1,801);

for n = 1:1:801

    % Coupling Coefficient

```

```

    Cpl_Coe(n) =
sqrt((imag(zpara(1,2,n))*imag(zpara(2,1,n)))...
    /(imag(zpara(1,1,n))*imag(zpara(2,2,n))));

    % Primary Inductance
    Ind_Pri(n) = imag(zpara(1,1,n))/(2*pi*Freq(n));

    % Secondary Inductance
    Ind_Sec(n) = imag(zpara(2,2,n))/(2*pi*Freq(n));

    % Primary Q-Factor
    Q_Pri(n) = imag(zpara(1,1,n))/real(zpara(1,1,n));

    % Secondary Q-Factor
    Q_Sec(n) = imag(zpara(2,2,n))/real(zpara(2,2,n));

end

%%%-----
%%% Step_3: Plot the calculated parameters
%%%-----

%clf % All previous plots will be removed

% Plot the coupling coefficient
figure;
plot(Freq,Cpl_Coe);
title('Coupling Coefficient');
xlabel('Frequency /Hz');
ylabel('coupling coefficient');
grid on

% Plot the inductance
figure;
hold on
plot(Freq,Ind_Pri,'r');      %Primary inductance is plotted
                             in red line
plot(Freq,Ind_Sec,'b');     %Secondary inductance is
                             plotted in blue line
hold off
title('Coil Inductance');
xlabel('Frequency /Hz');
ylabel('Inductance /H');
legend('Ind_P_r_i','Ind_S_e_c');
grid on

```

```

% Plot the Q-factor
figure;
hold on
plot(Freq,Q_Pri,'r');      %Primary Q is plotted in red line
plot(Freq,Q_Sec,'b');     %Secondary Q is plotted in blue
line
hold off
title('Q-Factor');
xlabel('Frequency /Hz');
ylabel('Q-Factor');
legend('Q_P_r_i','Q_S_e_c');
grid on

%%%-----
%%% Step_4: Plot the original S-parameters
%%%-----

dB_S11 = zeros(1,801);
dB_S21 = zeros(1,801);
dB_S12 = zeros(1,801);
dB_S22 = zeros(1,801);

% Calculate S-parameters in dB scale

for n = 1:1:801

    dB_S11(n) = 20*log10(abs(spara(1,1,n)));

    dB_S12(n) = 20*log10(abs(spara(1,2,n)));

    dB_S21(n) = 20*log10(abs(spara(2,1,n)));

    dB_S22(n) = 20*log10(abs(spara(2,2,n)));
end

figure;
hold on
plot(Freq,dB_S11,'b');
plot(Freq,dB_S21,'r');
hold off
title('dB(S11) and dB(S21)');
xlabel('Frequency /Hz');
ylabel('dB');
legend('dB(S_1_1)','dB(S_2_1)');
grid on

```

```
figure;
hold on
plot(Freq,dB_S22,'b--');
plot(Freq,dB_S12,'r--');
hold off
title('dB(S22) and dB(S12)');
xlabel('Frequency /Hz');
ylabel('dB');
legend('dB(S_2_2)', 'dB(S_1_2)');
grid on

disp('END')
```