Implementation of Pilot Protection System for Large Scale Distribution System like The Future Renewable Electric Energy Distribution Management Project

By

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ABSTRACT

A robust, fast and accurate protection system based on pilot protection concept was developed previously and a few alterations in that algorithm were made to make it faster and more reliable and then was applied to smart distribution grids to verify the results for it. The new 10 sample window method was adapted into the pilot protection program and its performance for the test bed system operation was tabulated. Following that the system comparison between the hardware results for the same algorithm and the simulation results were compared. The development of the dual slope percentage differential method, its comparison with the 10 sample average window pilot protection system and the effects of CT saturation on the pilot protection system are also shown in this thesis. The implementation of the 10 sample average window pilot protection system is done to multiple distribution grids like Green Hub v4.3, IEEE 34, LSSS loop and modified LSSS loop. Case studies of these multi-terminal model are presented, and the results are also shown in this thesis. The result obtained shows that the new algorithm for the previously proposed protection system successfully identifies fault on the test bed and the results for both hardware and software simulations match and the response time is approximately less than quarter of a cycle which is fast as compared to the present commercial protection system and satisfies the FREEDM system requirement.

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LIST OF SYMBOLS

A	Ampere
A/D	Analog to Digital Converter
AC	Alternating Current
ARP	Address Resolution Protocol
CT	Current Transformer
$\frac{dv}{dt}$	Voltage gradient with respect to time
D/A	Digital to Analog Converter
DAQ	Data Acquisition System
DC	Direct Current
DESD	Distributed Energy Storage Device
DGI	Distributed Grid Intelligence
DHCP	Dynamic Host Control Protocol
ESD	Energy Storage Device
FCL	Fault Current Limiter
FID	Fault Isolation Device
FREEDM	Future Renewable Electric Energy Delivery and Management
GPS	Global Positioning Satellite
IEEE	Institute of Electrical and Electronics Engineers
IEM	Intelligent Energy Management
IFM	Intelligent Fault Management
IGBT	Insulated-gate Bipolar Transistor
IP	Internet Protocol
IRIG	Inter-range Instrumentation Group
J_c	Critical Current density of Superconductor
k	Kilo ($1x10^3$)
kA	Kilo Ampere
kbyte	Kilo Byte

kOhm	Kilo Ohm
kV	Kilo Volt
kVA	Kilo Volt Ampere
K	Kelvin
m	Milli (1x10-3)
mH	Milli Henry
ms	Milli Second
mV	Milli Volt
M	Mega (1x106)
Mbps	Mega bits per second
MHz	Mega Hertz
MS	Microsoft
MVA	Mega Volt Ampere
MW	Mega Watt
n	Nano (1x10-9)
ns	Nano Second
NSF	National Science Foundation
OP AMP	Operational Amplifier
p.u.	Per unit
rms	Root mean square
RC	Resistor-Capacitor
RSC	Reliable and Secured Communication
SNTP	Simple Network Time Protocol
s	Seconds
SEL	Schweitzer Engineering Laboratories Company
SST	Solid State Transformer
TCP	Transmission Control Protocol
u	Micro (1x10-6)

uF	Micro Farad
uH	Micro Henry
US	United States of America
V	Volt
W	Watt

CHAPTER 1

INTRODUCTION

1.1 Brief Introduction

- In the future, the need for power will increase so will the need to increase power generation. Renewable energy is a very interesting and upcoming field. There is a growing interest to develop distributed renewable electric generation, distributed control of energy management and also energy storage. The graph below shows the US primary energy consumption since 1775 [1].

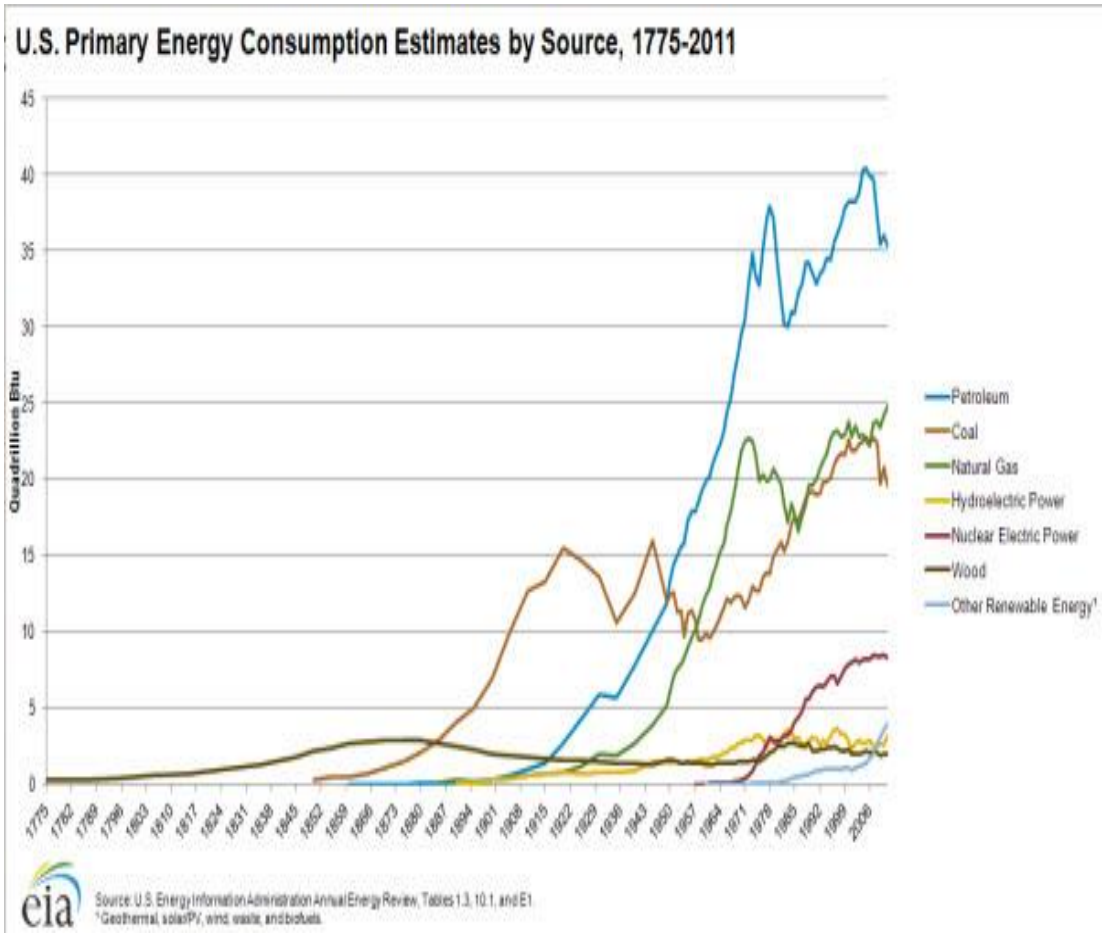


Figure 1.1. Energy Consumption from 1775-2011 (taken directly from [1])

- Thus the in the future we will have lot of renewable resources contributing to the grid. But creating all renewable grids can not only be expensive, but would require new expertise and resources for integrating these sources into the grid. It would rather be more efficient to connect renewable energy sources to existing distribution grids.
- But these renewable energy sources have a lot of power electronic devices used in them like inverters, rectifiers, dc-dc converters; also these power electronic devices change the voltage as well as current profile due to which these devices bring new issues and challenges to the protection system.
- The Fault characteristics of power electronic devices is very different from traditional distribution systems like the fault level in a solar PV panel inverter is so less that sometimes it cannot be even detected as a fault [2].
- Also the fault current level will also be limited due to these devices as well, and also other issues like power harmonics can come into play [2].
- So in the future we are looking at a grid which will be a modernized electrical grid that uses information and communications technology to gather and act on information, so as to balance the generation of both renewable as well as non-renewable sources of energy. There by providing protection concepts for such smart grids will be the next step.

The FREEDM loop, a National Science Foundation (NSF) enterprise, is an experimental power grid which aims to provide a few answers and solution to these question asked. It claims to remove the requirement for enhancing the existing power system equipment at the distribution level and also talks about the renewable energy generation and distribution concerns. The inclusion of many new loads with renewable energy will place an added pressure on the electrical infrastructure. The FREEDM system's plan is to operate

distributed generation and energy management through advanced power electronics and communications is demonstrated in this research topic [3].

1.2 The FREEDM system

The FREEDM system was formulated as a grid infrastructure with not only renewable resources integrated in to the grid, but with capabilities to operate in faulted conditions (islanding), and capabilities to react to system depending upon the change in load, demand automatically based on the data received through digital communications. This system will help assimilation of renewable energy generation into the power system grid. The system helps us develop break-through technologies in energy storage, distributed grid intelligence and power semiconductor devices. To show the various research developments, a 1 MW green energy hub loop supplied by renewable energy resources is under development. The FREEDM system is designed at allowing the customers to plug in renewable resources that generate power but also use devices that have storage capabilities, such devices are placed at residences and commercial / industrial factories, and also has the ability to manage their energy consumption through the load management system [3]. A single line diagram of the proposed FREEDM system is shown in Figure 1.2.

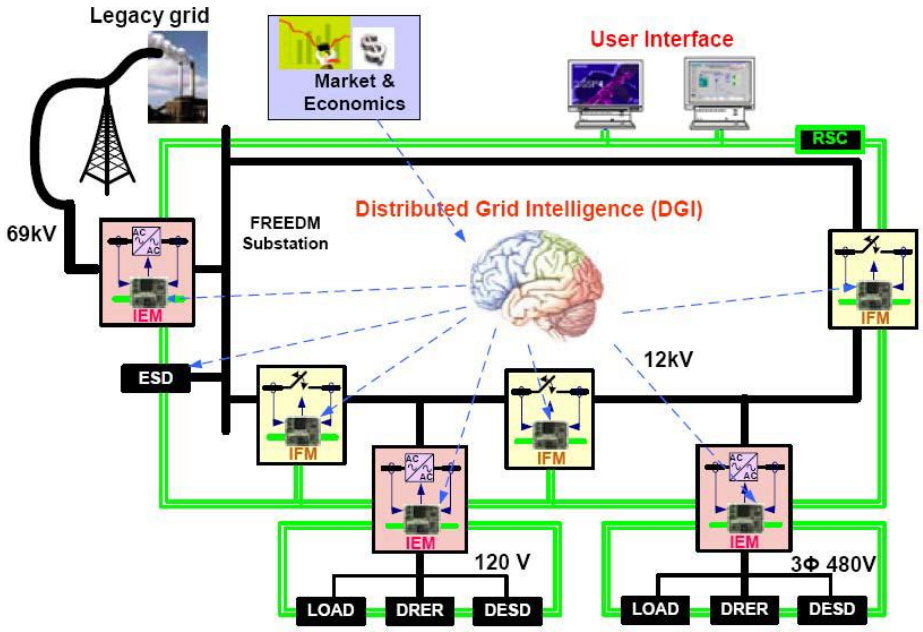


Figure 1.2. FREEDM System (taken directly from [3])

The FREEDM system includes advanced power electronic features combined with information relaying technology to develop a futuristic distribution grid which will include many features. One of the features will be plug and play of DRER (Distributed Renewable Energy Resource) and DESD (Distributed Energy Storage Device). While managing such DRER's, DESD's and loads using DGI (Distributed Grid Intelligence). This system also include revolutionary solid devices like FID (Fault Isolation Devices) able to clear faults extremely fast. The distribution system has the capability of being totally isolated from the main grid and still run perfectly in the islanded mode of operation. [3].

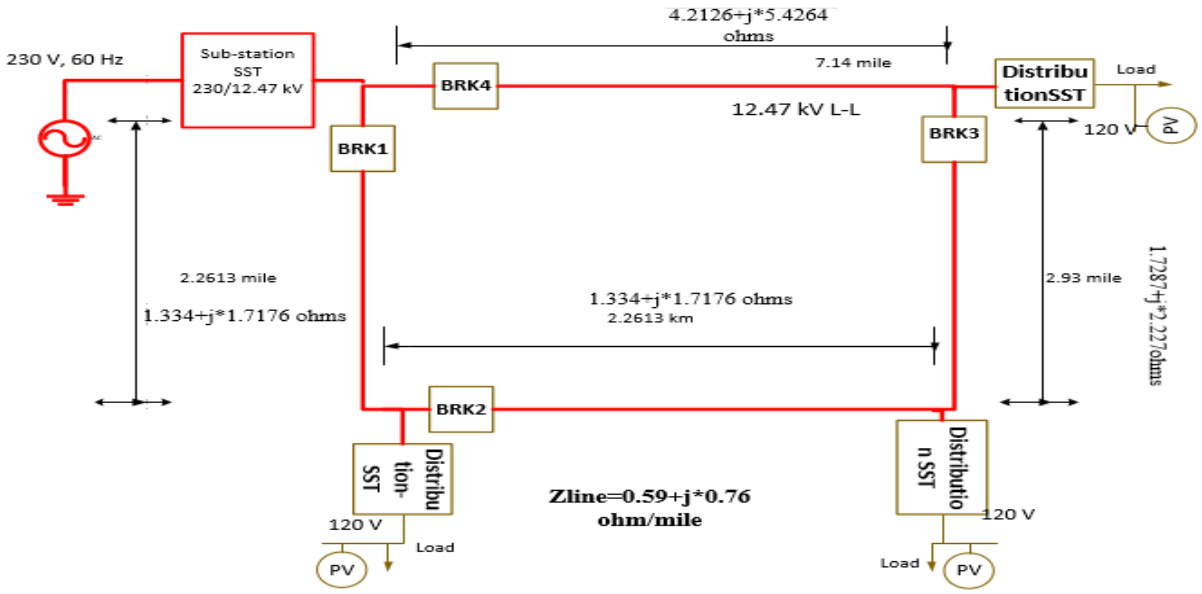


Figure 1.3 Figure of the FREEDM system (taken directly from [4])

- A figure of the FREEDM system is shown above. In this the loads are connected to 120 V AC regulated supply feeder. The DRER, DESD can be directly connected to the DC link of the SST. The SST is a 3 level/layer device which has AC-DC-AC link. So the SST is allowed bidirectional power flow control and controls other cases of power administration authority, fault current limitation and voltage ride through needed for dynamic plug and play system. An ultra-fast FID is used to isolate faults throughout the 12 kV system so as to supply uninterrupted good quality power to the consumer. All the FID's and the SST's coordination is done with the help of DGI or IEM (Intelligent Energy Management) software coded in each SST and FID. The DGI/IEM communicate with the SST's and FID's through the RSC (Reliable and Secured Communication network) [3]

- As shown in the figure 4, the system has FCL (Fault Current Limiters) places at various points in the loop system. The loads, DRERs and DESDs are joined to the loop through the SST's. The loop is then segregated in to different sections/zones. Each zone will contain a fixed number of SST's. And every zone is protected by FID which are the electronics CBs of the system.

The IFM (Intelligent Fault Management system) is used to help protect the FREEDM loop system by isolating faults in the 12 KV distribution system. The renewable sources and the storage devices are connected through the IEMs to the loop. Both the IEM and the IFM are connected through the RSC .In the event of a fault the FREEDM system can operate independently in the islanded mode of operation [5].

1.3 Motivation and Objective

The standard distribution system is framed in a branched layout and is protected by the traditional 3 division overcurrent protection: The primary grid feeder is protected by a circuit breaker at the substation terminal. In the middle section of a feeder a recloser is placed. Fuses are used to protect the smaller branch feeders in a normal distribution system. Using proper settings for coordination timings, each section contributes to the backup protection for the lower section. On occurrence of a fault on the main feeder, the entire feeder will have to shut down, and this is one of the biggest disadvantages of these types of protection schemes [6] On account of outage of fuses, momentary outages are caused which damage sensitive electronic component devices [6]. Most distribution systems are

radial systems. But because of DG, as fault current will be supplied by both the DG and the grid, in that case such systems are considered as loop systems. The FREEDM system is also such a loop system. Thus traditional over current protection systems cannot work and so the un-faulted DG feeder might trip.

For higher quality power closed loop distribution system are now being used. As a result fault in one section cannot cause outage down the line as in case of radial/open loop system. Moreover closed loop systems provide more rigid voltage support and has better capacity of load rising. Hence loop systems are an ideal choice for future distribution system [7] [8]. Conventional over current relays cannot be used because of bidirectional power flow in the network because of the presence of DG in the system. Also fault clear time will ensure whether DG's will lose stability or not. Moreover closed loop systems have higher short circuit currents and also increase the dips in voltage as well as frequency. Thus making these systems more sensitive to power system oscillations and fault expansion [7] [8].

The FREEDM grid being a smart grid, it will be able to operate for both grid connected condition as well as islanded condition. Such modes of operation question standard over current protection schemes for distribution systems. Hence it is extremely important to develop protection schemes that involve communications [9]. The challenges posed by protection systems in micro grids like the FREEDM system are the problems that are linked with bidirectional power flow, meshed structure and continuously changing level of fault current levels because of discontinuous attributes of the DGs and also reduced levels of fault current during islanded mode of operation [10] [11].

The other issue with the protection system is the operation time. The current distribution protection system can identification and interruption time is around more than a second. One of reasons for this could be that classical mechanical circuit breaker, are capable to turn off the fault current only at zero crossing current point, and hence the require at least a cycle to interrupt/cut off the circuit. The advancements of Solid State technology gives a rather unique explanation of interrupting a fault, i.e. the solid state circuit breaker (SSCB/FID) Fault isolation devices depend on swift switching solid state switches. SSCB/FID is able to interrupt fault current inside a millisecond because of its capability to switch thousands of times per second [12]. Based on this approach the differential pilot protection system was developed previously at ASU. The concept, theory, practical implementation of the pilot differential protection is shown in [12.].

The objective of this thesis is to implement the pilot differential protection system which complies with the brisk operation and precise fault isolation requirements of the multi-source FREEDM loop system, into larger distribution system so as to verify the results based on the hardware and the software simulations. Also the algorithms performance was evaluated based on a few changes made to the algorithm and test conducted on the test bed were compared to the simulated results.

1.4 Thesis Outline

The key content of this thesis has been divided into 6 Chapters. Chapter 1 provides an introduction of the key issues faced today and presents the answer in form of the pilot differential protection system. The background of the thesis on the FREEDM system is also explained in this chapter.

In Chapter 2, a complete literary analysis which includes stating problems and its mitigation strategies in the form of the pilot differential protection are presented. For a comparison of traditional protection scheme, common protection schemes are described. A contrast of the advantages and drawbacks of the proposed scheme are made.

Chapter 3 determines zonal protection, IFM (intelligent fault management) concepts as well as differential protection concept developed earlier. After that in Chapter 3 ,the existing over current protection standards used in distribution systems is tested on an existing industrial relay by setting up a scaled model of a protective zone and applying one of fastest commercial relay that has been used widely in the industry for over current protections i.e. the SEL351 S over current relay on it. The new pilot differential protection system (which includes both the counter method and the 10 sample average window concept) is shown by altering the original pilot protection algorithm later in the same chapter. The simulation results of the new algorithm on the same test bed on PSCAD are shown in this section of the chapter. Chapter 3 studies the implementation of the new algorithm on hardware system and the results of the hardware and the software simulations are then compared with the hardware results.

In Chapter 4 the new multi slope differential protection scheme formulation, testing, simulation and results are explained. Lastly in chapter 4 the effect of current saturation is explained and the results of the pilot protection system affected by current saturation are shown.

In Chapter 5, the implementation of the pilot protection system in the GreenHub model is explained and the results are discussed. Next the implementation of the pilot

protection system in the IEEE34 node system with PQ loads is discussed and the results shown. Later implementation of the pilot protection system in the modified IEEE34 node system or LSSS system with SST loads is discussed and the results tabulated. And lastly the working of the substation and load type SST developed at FSU and the role of the pilot protection system in its protection are explained. The results of the pilot protection system for the protection of the modified LSSS system utilizing the above mentioned SST models are also tabulated. In the end, the conclusions and possible extensions as future work are shown in Chapter 6.

Appendices A-C provides basic information on the studies carried out in this thesis. Appendix A is the PSCAD simulation files that are used for chapter 2 and 3 experiments for the test bed, dual slope/ point method, and the current saturation experiment. Appendix B presents the PSCAD simulation files for the GreenHub, IEEE 34, LSSS system and the modified LSSS system experiment.

CHAPTER 2

LITERATURE REVIEW

2.1 Solid State Transformer [13]

The SST is used for active control and management of connected renewable resources and loads to its secondary. The primary side is connected to the FREEDM Loop. It is speculated that the SST will allow the increment in power delivery and power quality. The SST allows the plug in and generation of various DGs and also allows the increment/decrement of loads into the grids without having any detrimental effects.

2.1.1 SST Design [13]

Utilizing the 15 kV SiC IGBT, higher frequency chopping is possible which is speculated to decrease the size, weight, and losses thereby making it a conceivable idea to replace traditional transformers. The material cost would also be lesser as the use of copper in such SSTs, would be much lesser as compared to traditional transformers.

2.1.2 SST converter stages and its simulation parameters

The SST consists of 3 stages i.e.

1. AC-DC rectifier
2. DC-DC Dual active H bridge (DAB)
3. DC-AC inverter

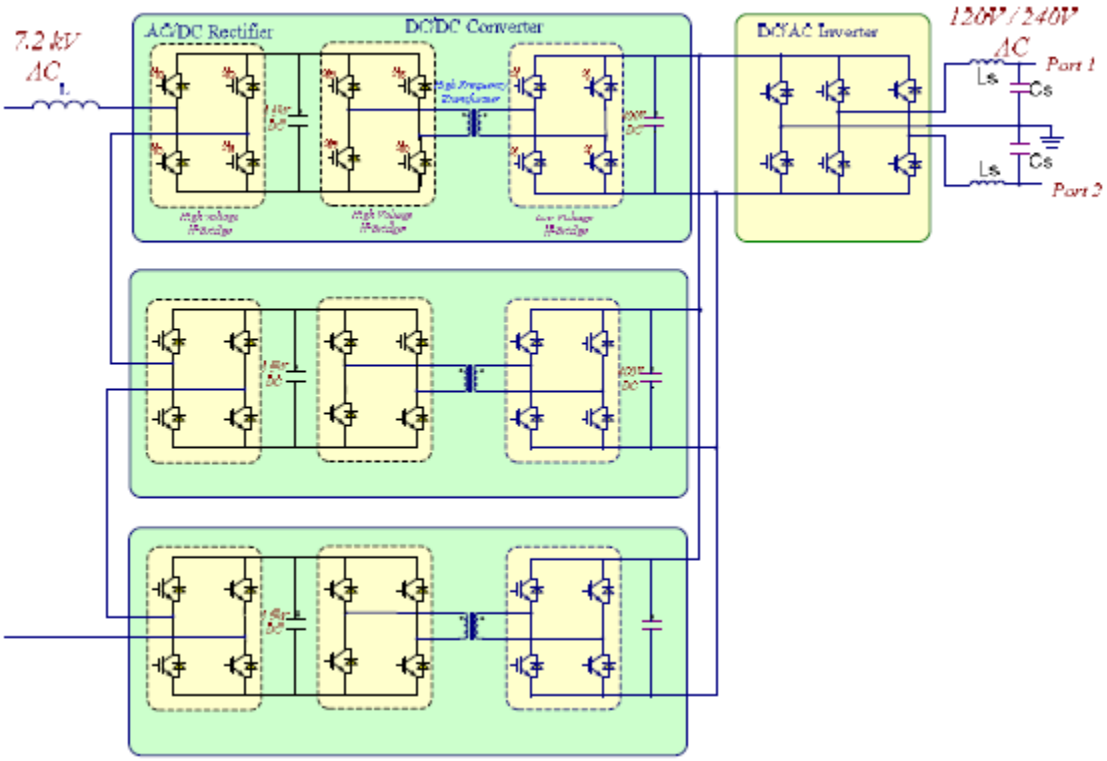


Figure 2.1. SST topology [13]

The model is replaced by an average simulation model by substituting the switching variable with continuous values which are averaged for 1 period of a switching cycle. In its basic system setup, the SST is a 20 kVA transformer connected to a 12 kV distribution system with a single phase output of 120 V. Single phase input voltage: 7.2 kV AC, 3 DC-DC link that convert 3800 V DC (HV side) to 400 V DC (LV side) and voltage source inverters that converts 400 V DC to 120/240 V AC at 60 Hz for 1 phase 3 wires. The switching devices that are used for the H bridges in the DAB and inverter are 6.5 kV silicon IGBT for the high voltage H bridge ($f_s = 1\ kHz$) and 600 V IGBT for the low voltage H bridge ($f_s = 10\ kHz$). 20 kVA model can be considered as a building block and can be used to make large 200 kVA models.

2.1.3 Rectifier modelling

The AC/DC rectifier converts the single phase 7.8kV AC voltage to 3 DC output of 3.8 kV while maintaining unity power factor at the input side. Utilizing the two current and voltage equation

$$L.\frac{di}{dt} = v_L(t) \qquad (2.1)$$

$$C\frac{dv_c}{dt} = i_C(t) \qquad (2.2)$$

Voltage equation for the circuit

$$L_s\frac{di_a}{dt} + V_{pcca} + R_s.i_a = 3Ed_a \quad (2.3)$$

$$\frac{di_a}{dt} = \frac{3E}{L_s}d_a - \frac{V_{pcca}}{L_s} - \frac{R_s i_a}{L_s} \qquad (2.4)$$

Where $i_a = AC\ side\ input\ current, V_{pcca} = AC\ side\ input\ voltage, L_s = AC\ side\ input\ inductor,$

$$E = voltage\ of\ the\ dc\ bus, d_a = rectifier\ duty\ cycle\ for\ the\ PWM$$

For the next current equation

$$C\frac{dE}{dt} + \frac{E}{R_L} + d_a i_a = 0 \qquad (2.5)$$

$$\frac{dE}{dt} = \frac{-E}{R_L C} - \frac{d_a i_a}{C} \qquad (2.6)$$

Where $C = rectifier\ DC\ capacitance$

Based on these equations the equivalent average model is given

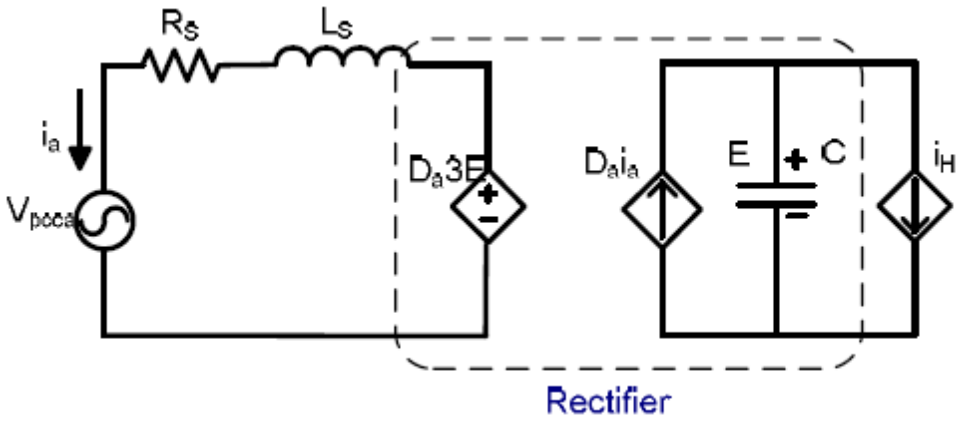


Figure 2.2. Equivalent average model [13]

In this case d-q control is used for the rectifier. An imaginary phase is developed which is 90 degrees lagging to the main phase A is hypothesized. Now the differential equation for the voltage and current for the imaginary phase will be

$$\frac{di_m}{dt} = \frac{3E}{L_s} d_m - \frac{V_{pccm}}{L_s} - \frac{R_s i_m}{L_s} \qquad (2.7)$$

$$\frac{dE_m}{dt} = \frac{-E_m}{R_L C} - \frac{d_m i_m}{C} \qquad (2.8)$$

Where i_m is input current for the imaginary phase, combining equation sets 1.4, 1.6, 1.7 and 1.8 we get

$$\frac{\overrightarrow{di_{am}}}{dt} = \frac{3E}{L_s} \overrightarrow{d_{am}} - \frac{\overrightarrow{V_{pccam}}}{L_s} - \frac{R_s \overrightarrow{i_{am}}}{L_s} \qquad (2.9)$$

$$\frac{dE_m}{dt} = \frac{-E_m}{R_L C} - \frac{\overrightarrow{d_{am}} \overrightarrow{i_{am}}}{C} \qquad (2.10)$$

Where $\overrightarrow{i_{am}} = \begin{bmatrix} i_a \\ i_m \end{bmatrix}$, and $\overrightarrow{d_{am}} = \begin{bmatrix} d_a \\ d_m \end{bmatrix}$, $\overrightarrow{V_{pccam}} = \begin{bmatrix} V_{pcca} \\ V_{pccm} \end{bmatrix}$ (2.11)

The single phase dq transformation is applied to the equations 1.9 and 1.10, and the differential equation is obtained

$$[x]_{dq} = [T].[x]_{am} \qquad (2.12)$$

Where $T = \begin{bmatrix} \sin(\theta) & -\cos\theta \\ \cos\theta & \sin(\theta) \end{bmatrix}, \theta = 2\pi f_L \ , f_L \ is \ line \ frequency$ (2.13)

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{3E}{L_s}\begin{bmatrix} d_d \\ d_q \end{bmatrix} - \frac{1}{L_s}\begin{bmatrix} v_{pccd} \\ v_{pccq} \end{bmatrix} - \begin{bmatrix} \frac{R_s}{L_s} & -\omega \\ \omega & \frac{R_s}{L_s} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} \qquad (2.14)$$

$$\frac{dE}{dt} = -\frac{E}{R_L C} - \frac{1}{2C}\begin{bmatrix} d_d \\ d_q \end{bmatrix}^T \begin{bmatrix} i_d \\ i_q \end{bmatrix} \qquad (2.15)$$

Using the phase locking loop in figure 2.3 below , the voltage vector is adjusted according to the direction of d axis during the steady state. Hence the grid voltage component in the q axis will be zero, while for d axis it will be equal to the grid voltage. Hence the d axis is the control for the active current, and q axis is for the reactive current component.

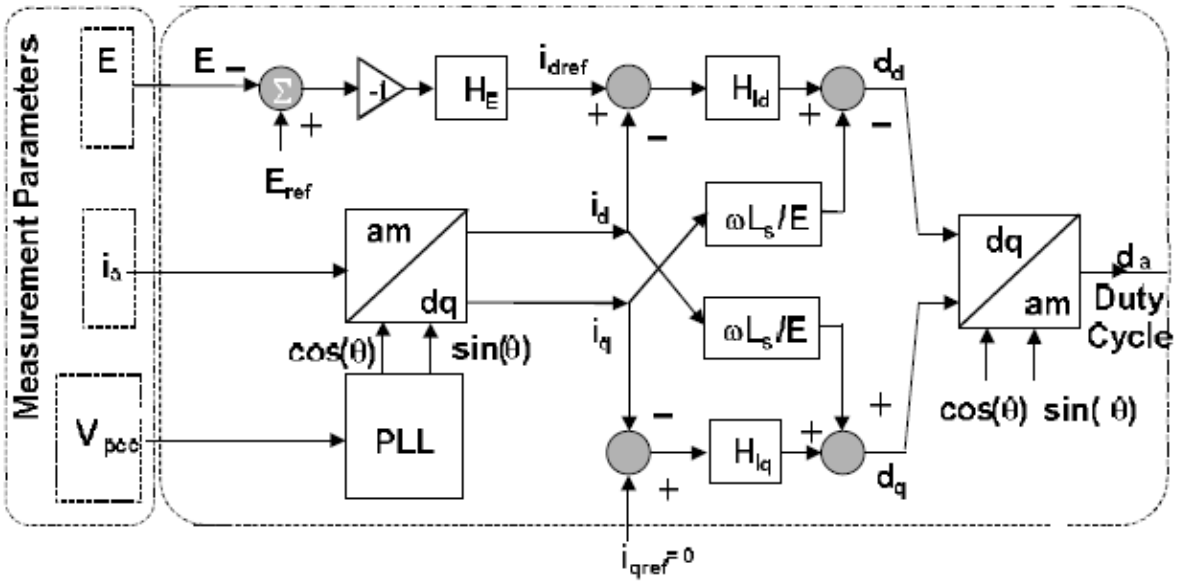


Figure 2.3. Dq controller for rectifier [13]

2.1.4 Modelling of the dual active bridge

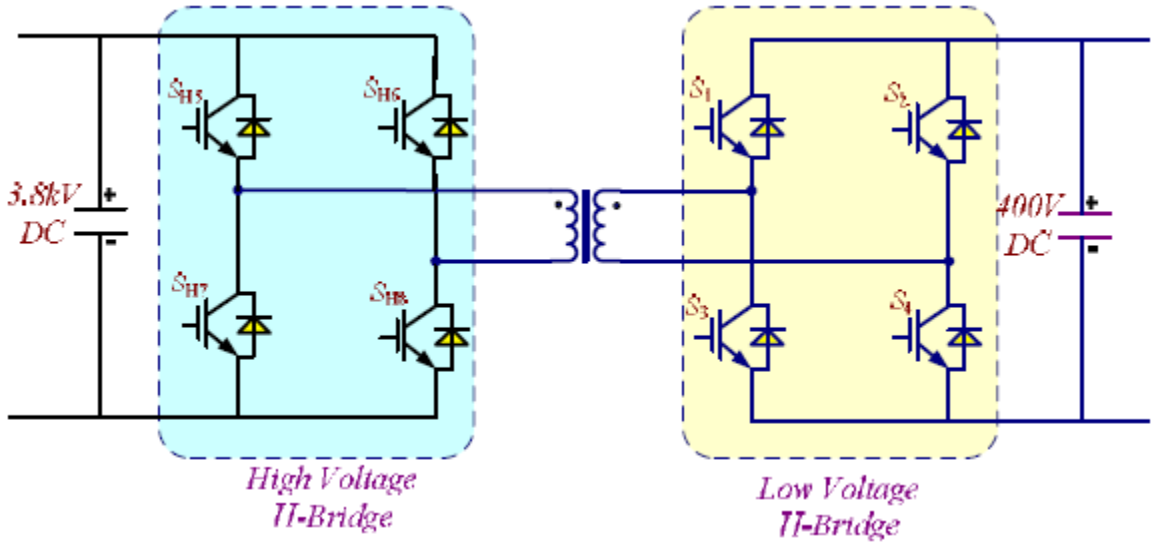


Figure 2.4. Dual active bridge [13]

The DAB has 2 parts i.e. the HV Bridge and the LV Bridge. The rectifier regulates the high voltage side DC link voltage and the AC current is controlled to be sinusoidal. The low voltage DC link is controlled by the DAB converter. The dual active bridge scheme

provides zero voltage switching for all the switches, lesser voltage disturbances for the switches. The amount of power transferred being controlled by the phase angle difference and the magnitudes of the dc voltages at the two sending and receiving ends are given by the following equation.

$$P_o = \frac{V_{dc} V_{dc\_link}}{2Lf_H} d_{dc}\left(1 - d_{dc}\right) \tag{2.16}$$

V =input side high voltage DC voltage, H f is switching frequency, L is leakage inductance, dc _link V is the secondary side low voltage DC link voltage referred to the primary side and d_{dc} *is ratio of time delay between the two bridges to one half of switching period.*

2.1.5 Modelling of the inverter stage

The DC/AC inverter changes the 400V DC to 240/120V AC, 1 phase/3 wires. The topology is shown in Fig.2.5 below. The inverter consists of six switches with three phase legs. The neutral point is joint to the third leg of the phase. The other two phase legs consists of four-switch inverters that are regulated by Sinusoidal Pulse Width Modulation (SPWM). The third leg connected to the phase in the six-switch inverter normally is regulated to give a square waveform to deliver as the neutral phase and at same time achieve the maximum employment of the DC bus voltage.

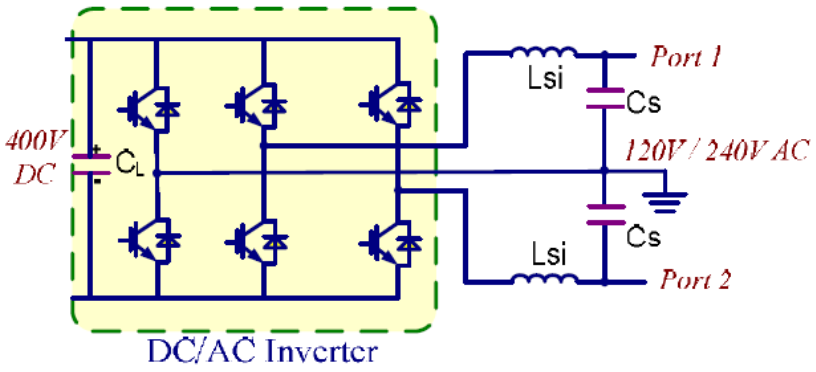


Figure 2.5. DC/AC inverter topology [13]

2.2 Relay protection design [6]

The protective relay system design usually has circuit breakers, current transformers and relays which must coordinate together to function properly. Protective relays or systems are usually not required to operate during normal operation, but must be able to act swiftly during fault incidence so as to avoid serious outages and damages. Usually a relay system's operating life will not be more than a few seconds, even when they might be connected to the system for many years. So testing becomes a very important part for these relays where they are put through immense conditions for long periods of time.

In normal day to day use there are four factors that ***influence protection applications*** are

1. Economics-*Operation and maintenance cost*

2. Magnitude and level of Fault-*Fault levels and positioning of voltage and current transformers*

3. Operating Practices-*Accepted and practiced standards for efficient and strong performance*

4. History of the type of fault that usually occur-*Past History on the type of fault occurring and the forecast of likely such events*

2.3 Design criteria for protection applications [6]

In most cases the power system is divided into several zones of protection, each requiring its own set of relays, CT's and PT's. The following points are considered for ***designing a protection system***

a. Reliability-The Reliability of the system includes two elements dependability and security. Dependability is the correct operation in response to a problem in a system. Security is the amount of certainty that the relay will not operate in an inappropriate manner. Unfortunately both these aspects oppose one another, increasing security decreases dependability and vise a versa.

b. Speed- As it takes only a couple of seconds to destabilize a system, so speedy operation of protection system becomes very important. But by increasing the speed, there can also be increase in unwanted or unexplained operations. High speed mostly indicates that the trip times are not higher than 50 ms (around 3 cycles of a 60 Hz system).

c. Performance and Economics-Relays usually have set zones of protection provide better selectivity but they cost more in such cases [6].

2.4 Zones of Protection [6]

In power systems, a more general system configuration is to divide a system into protective zones. Now if a fault occurs inside the protective zone, appropriate action will be taken to isolate the particular zone from the rest of the system [6].

- Zones are usually defined for:

a) Generators,

b) Transformers,

c) Buses,

d) Transmission and distribution lines, and

e) Motors.

Shown in Fig 6 is the concept of zone protection. Each zone is characterized by a closed, dashed line. Zone 1, for instance, has a generator and a transformer leads. Usually a zone might have more than one component. For example, zone 3 contains a generator-transformer unit and a bus connection leads, and zone 10 has a transformer and a line.

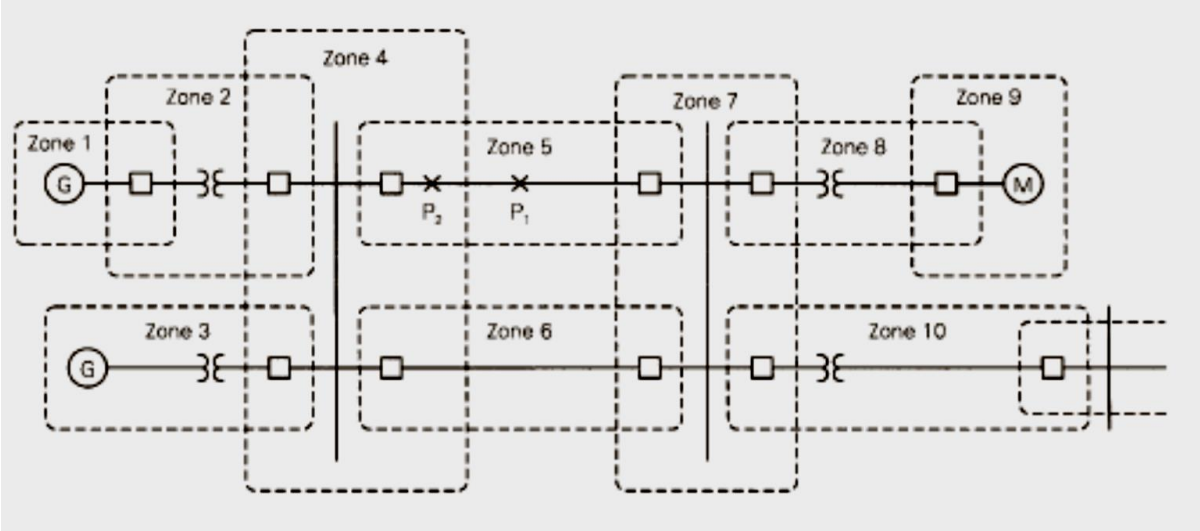


Fig 2.6. Protection Zones in a power system [6]

Following are a few characteristics of Zones of protection [6]

- Zones are always overlapped.
- Circuit breakers are located in the overlap region.
- For a fault in a particular zone, all the CB in that zone open up to isolate the fault.
- Usually one CB to another CB can be used to define a protective zone.

- Neighboring zones are overlapped to escape the option of unprotected areas. With no overlap the area between two adjacent zones would not be in any zone and hence would not be protected.
- As isolation during faults is done by circuit breakers, they should be placed in between devices in a zone and connections to the system i.e. breakers should be placed in each of the overlap region [6].

2.5 Different types of protection schemes used

2.5.1 Overcurrent protection [12]:

Mostly, there are two kinds of overcurrent relays used in the industry:

1. Instantaneous overcurrent relay: These relays operate as the name suggest instantaneously /immediately. The sensing relay trips when the current reaches the threshold limit. They are popularly utilized in bus/feeder protection. The instantaneous overcurrent relay is very helpful for protecting electrical units against high short circuit fault currents [14] [15].
2. Time-delayed overcurrent relays: a time-order system is applicable to implement the back-up protection system. Time-current curve are applied in such a manner that the operation time is inversely proportional to the fault current. If the fault current is lager, the relay will operate even faster. The general equation for the time overcurrent relay is:

$$\tau = \frac{K}{[(PSM)^n - 1]} \qquad (2.17)$$

τ = operation time PMS= plug multiplier setting K, n= preset constants.

There two most important settings for the time-delay overcurrent relay are the pickup value, and the other is the time delay. Time-delay overcurrent relays operate at a faster rate at high current as compared to slow operation at lower levels of fault current. Thus the curve follows an inverse time characteristic shown in the figure 2.7 below. Time overcurrent relays have five different types of curves that are based on the slope of the time-overcurrent characteristic.

- Definite time
- Moderately inverse
- Inverse
- Very inverse
- Extremely inverse

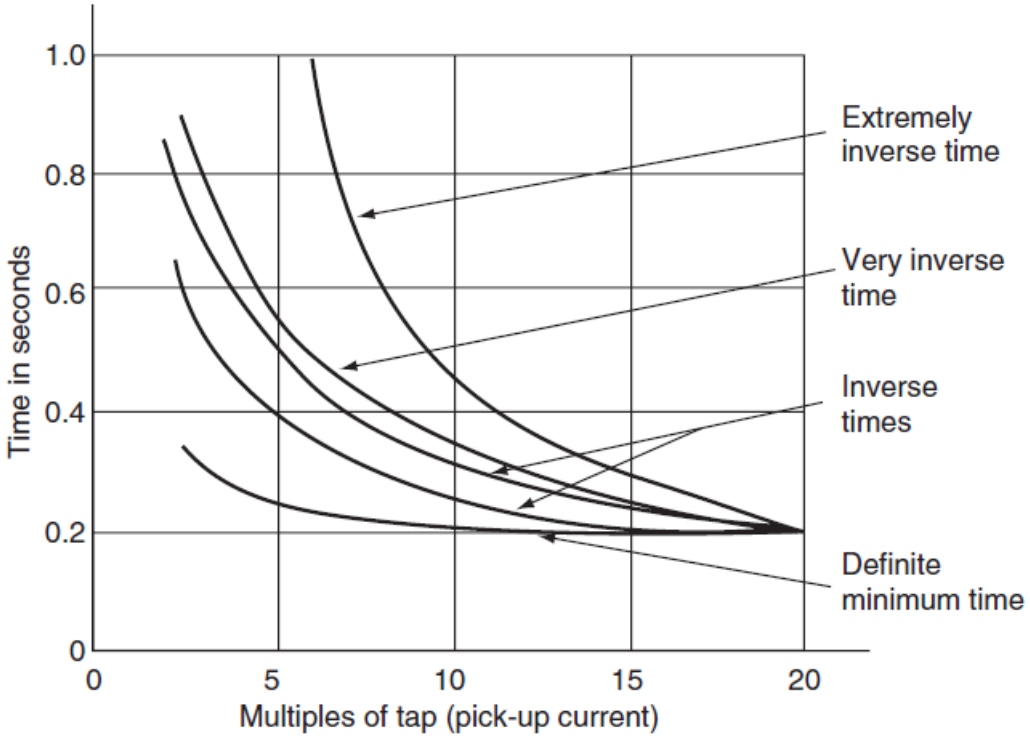


Fig 2.7. is the graph for a general inverse-time–overcurrent relay characteristics. The curves are set for a fault current with time delay of 0.2 sec and fault current around 20 times minimum pickup current [6].

2.5.2 Differential Relays

Differential protection scheme is a widely used protection scheme especially for unit protection like key component protection in power system like bus, generator, and transformers.

2.5.3 Principle of current differential relay

The operating principle for a traditional differential protection scheme is that the pickup current should be equal to the difference of the currents coming through the operating coil, and its working principle is based on Kirchhoff's current law.

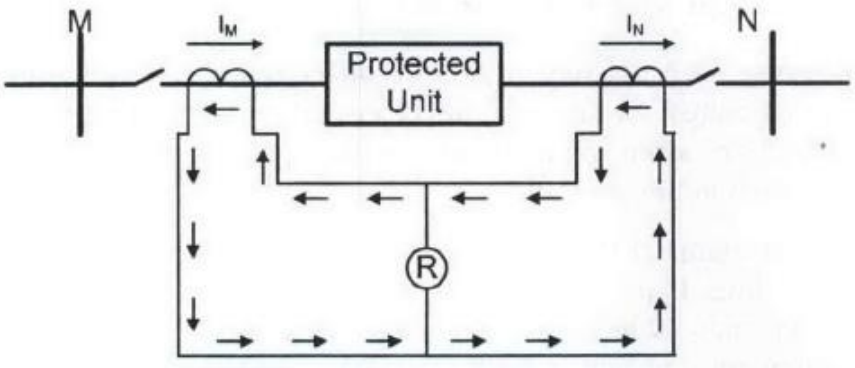


Figure 2.8. Currents in the differential system during normal operating condition when there is no fault [17]

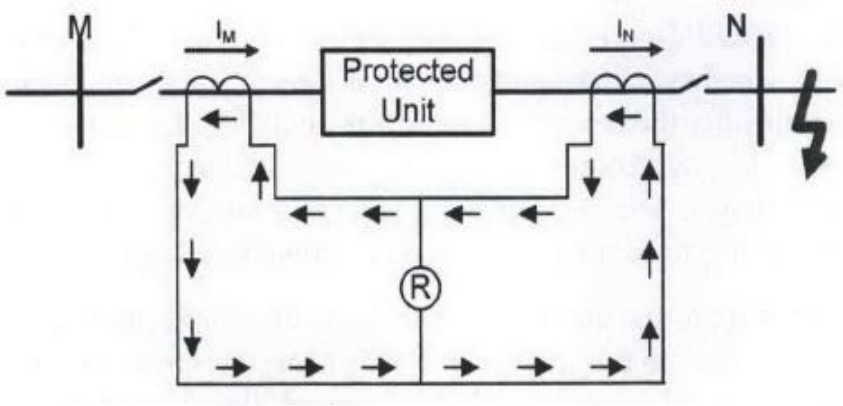


Figure 2.9. Currents in the differential system during in case of external fault [17]

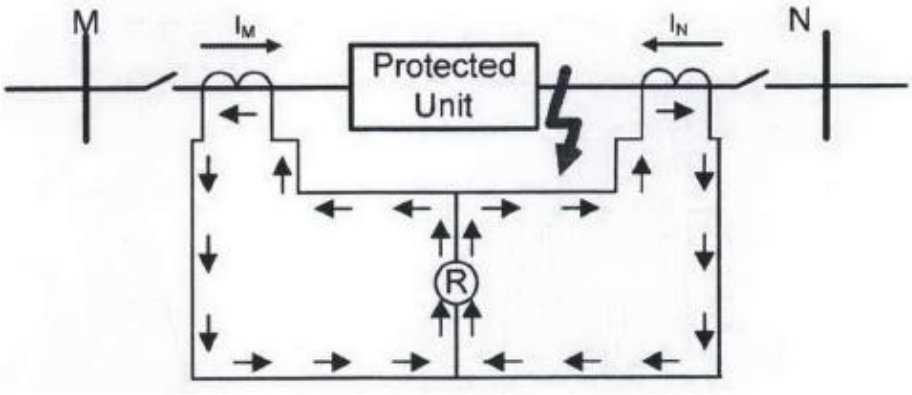


Figure 2.10. Currents in the differential system during in case of internal fault [17]

For the normal condition (shown in figure 2.8.), the currents at each side of the CTs are exactly equal in magnitude and opposite in phase. Thus, the secondary current that circulates in the pilot wire circuit doesn't produce a trip. On a fault taking place outside the zone of protection (shown in figure 2.9.), the differential relay still has no current flowing into the relay as the currents in both the CTs rises in magnitude at the same time. Hence no trip is produced. When a fault actually happens inside the zone of protection, the current

I_M (shown in figure 2.10.) will no longer be equal to I_N, as hence, the imbalance current flow through the operating coil, after which the trip is generated.

2.5.4 Percentage Differential Relay

The traditional percentage differential has two coils as shown in figure 2.11 below: One is the biased coil that acts as the restraining coil, while the other is the operating coil. The bias or percentage differential is defined as the following quantity

$$Bias = \frac{(i1 - i2)}{(i1 + i2)/2} \qquad (2.18)$$

The operating condition is defined as

$$Iop = \frac{(i1 - i2)}{(i1 + i2)/2} > \ bias\ current \qquad (2.19)$$

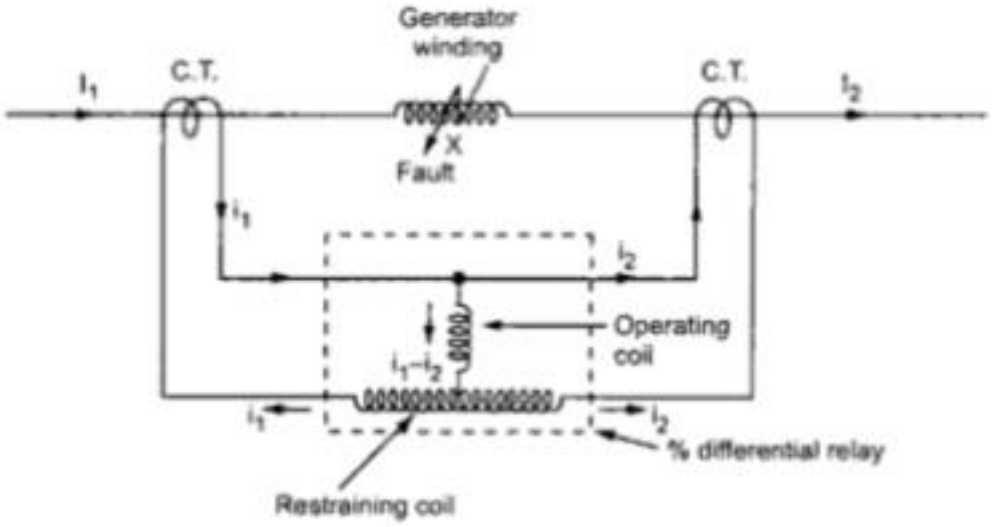


Figure 2.11. Percentage differential relay schematic (18)

Differential relays either have fixed or variable restraint that help to operate the relay. These restraining coils may have fixed or variable percentages, and general percentage

differential slope characteristic s are shown in Figure 2.12. The X axis is the restraining current I_R. The Y axis is the operating current I_{OP} required to operate the relay. Fixed percentage of the relays are usually between 10 % and 50% and they might have tap changers to modify the percentage.

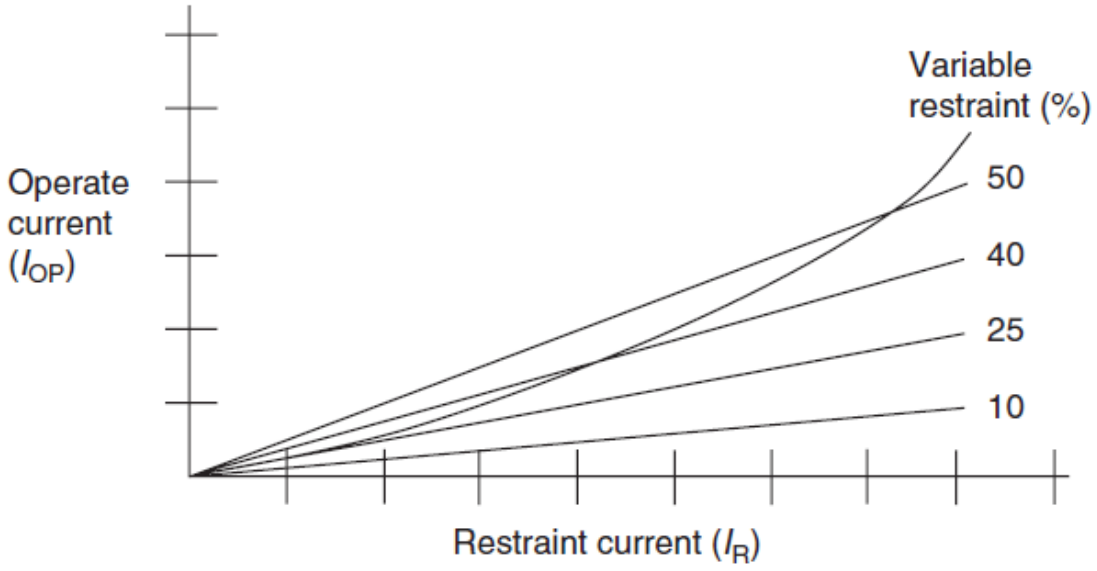


Figure 2.12. Common percentage differential protection characteristic [6].

2.5.5 Pilot Protection

Pilot protection utilized for line protection gives high-speed instantaneous detection of phase-type and ground-type faults for 100% of the protected section from all terminals. This is the optimal primary protection intention. These systems utilize a communication path to send signals from the relaying system from one end of the line to the other end. The functioning principle is to compare the two relays for their currents at each terminal of the transmission line. If the two currents are equal, there is no fault on the transmission line, else when the two currents are not equal, there is a fault in the transmission line.

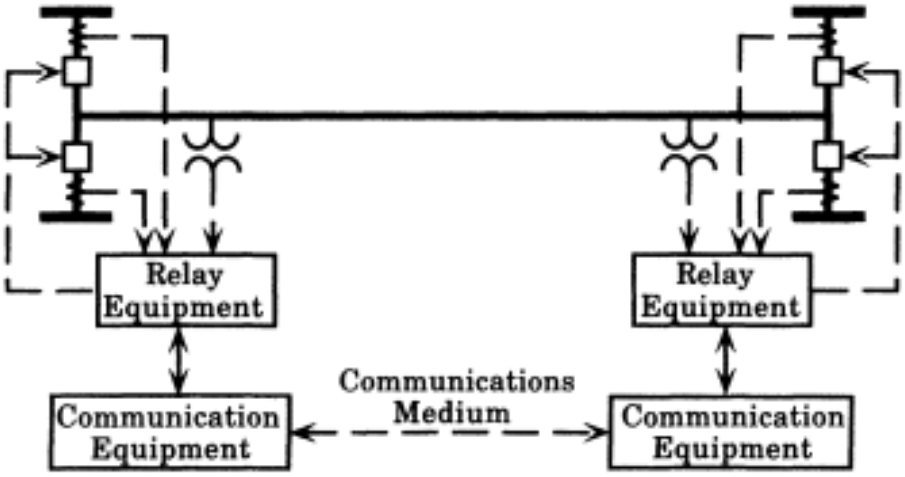


Figure 2.13. Topology schematic of pilot protection [19]

The pilot protection systems can be divided into two categories:

1. with use of channel:

a. Channels is not vital for trip operations; also known as blocking systems

b. Channels is required for trip operations; also known as transfer trip systems

2. With use of fault detection principle i.e. the comparison at the following quantities at several terminals:

a. Power flow is measure between the terminals, also known as directional comparison

b. The relative phase position of the currents are measured between the terminals, also known as phase comparison

2.5.6 Directional overcurrent protection

The directional overcurrent relays depends upon a reference voltage phasor, for estimating the direction of the fault. For all functional purposes, the system voltages do not change their phase positions much when a fault takes place. In comparison, line currents can deviate about 180 degrees (approximately reverse to the direction or flow) for faults that

take place on one side of the CT relative to a fault on the other side of the CT. After a fault occurs, the fault current has a characteristic phase angle approximately analogous to the voltage phasor. Hence the fault direction is decided by analyzing the current phasor with respect to the reference voltage phasor measured at the measurement location on the power line. This requires measurement of both current and voltage, hence it is costlier.

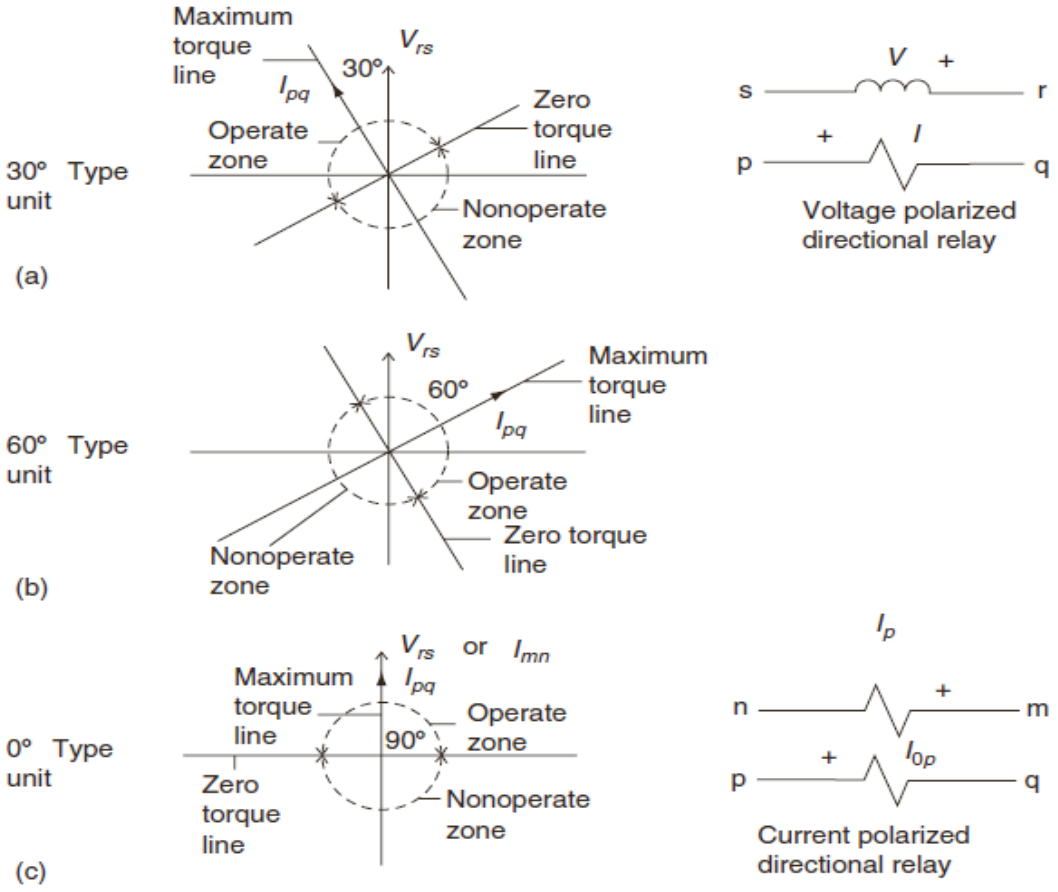


Figure 2.14. Directional relay operating characteristics [6].

2.6 Use of pilot line differential protection: a comparative study

This is a compilation of literary papers to justify the use of differential protection with communication link being fast, selective, reliable and robust in smart grid systems like the FREEDM system.

Definitions

Micro grid: The term micro grid is used for a low-voltage (LV) network smart grid with island-operation capability.

Smart grid: A smart grid is a modern electrical grid that utilizes digital information and communications technology to collect and operate on that data, in a programmed manner to better the efficiency, reliability, robustness, and cost effectiveness of the generation, transmission and distribution of electricity

1. **Differential protection of micro grids with central protection unit support [20]:**

Traditional fault current detection usually fail in micro grid systems because of a number of reasons like loop systems, higher fault current levels in looped system, and other factors [7] [8] . It is an extremely important aspect to estimate the fault currents due to inverter based DGs. Using differential protection system is advantageous as the system doesn't require prior knowledge of fault currents and value. Hence due to the ever changing fault current levels, differential protection is favored as it can easily adapt to such changes. It doesn't require prior knowledge or previous working's data. The differential protection system is also immune to operate without voltage fluctuations. The differential system can also easily adapt to the new configurations, new developments and infrastructure. Thus differential protection is considered to be one of the main contenders for development of

protection systems for micro grids. However long transmission/distribution lines require communication setup for employing differential protection. The differential protection can be applied to an entire system by using an advanced communication link for data processing.

2. Universal pilot wire differential protection for distribution systems [21]

This paper shows a unique pilot wire differential protection scheme for distribution systems. The ideas and principle of the traditional pilot wire differential protection is adopted here. After which many varieties of numerical differential protection schemes utilizing the pilot wires as communication channels have been shown in the paper. Current differential protection has always been accepted in power systems because of high robustness, precision, and sensitivity. Current differential based on application can be classified as the following types of protection system.

1. Pilot wire protection
2. Micro wave communication protection
3. Optical fiber communication protection
4. Power line carrier protection

3. Communicating line differential protection for urban distribution networks [22]

Increasing reliability of system is of paramount importance, as most systems are changing from radial systems are changing from radial systems to closed loop/ meshed systems. Using communication links, the paper authors have developed a type of protection using

differential current protection principle. The differential protection scheme is adopted because for loop systems with continuously varying line conditions the following protection methods can be used.

1. Directional over current protection
2. Distance relay
3. Line differential protection

Selectivity is an extremely important factor i.e. a particular part of the network remains unaffected by faults outside its zone of protection. Considering this fact, for the above mentioned statements will have the following differences.

- Distance protection will require a PT/VT for voltage measurement, and is not recommended for short lines without communication and back up protection. But they can act as good back up protection with over reaching capability. Also a (V/F) protection is also required with this unit.
- Directional over current protection also requires a VT/PT for voltage measurements. Mostly it requires communication channel for internal communication between several related function making the communication channel heavily loaded. Also the specifications are difficult to calculate and also the trip times are not extremely fast.
- As compared to the mentioned lines above, the pilot differential protection system has extremely fast trip timings. The relays require communication link between them. It cannot be used for large distances without communication link. The functionality is well tested and observed. Over current protection is also required

as an added protection. Earth fault protection application also can be included into the protection system.

Considering all the factors, the authors concluded that for the modern power system with loop/meshed networks line differential protection is a good fit.

4. **Protection principles for future micro grids [23]**

Traditional fuse protection systems cannot be used in LV micro grid distribution systems because of limited fault current feeding capabilities of converters/limiters limiting the fault current [23]. Hence the protection system for a micro grid must include the following properties.

- Adaptive capabilities
- High speed communication
- High speed trip detection and operation inside the micro grid
- Unnecessary tripping of micro grid for fault on network and vise a versa

Based on the following literary reviews it shows that utilizing a fast differential pilot protection scheme could be an answer to the some of the problems faced by protection systems in smart grids/micro grids.

CHAPTER 3

UPDATED ALGORITHM AND THE COMPARISON OF THE HARDWARE TEST AND SIMULATION RESULTS

3.1 Intelligent fault management system theory [12] [24]

The IFM (Intelligent Fault Management system) is an algorithm for the application of distributed grid sense for the FREEDM system architecture. The algorithm is a complete protection system that is running in the background constantly by the central processing unit. The Intelligent Fault Management system detects and isolates fault on the 12.47 kV side i.e. the main loop of the FREEDM system. The Intelligent Energy Management (IEM) communicates with the IFM through RSC channels. The IEMs record the power flow injections in the load distribution system. Both the solar and wind injection are integrated through the IEMs. Hence the IEMs can provide consultative process request on real time energy basis future market forecasts as well. So when a fault occurs, the IFM detects the fault location and the trip signal is sent to the corresponding Fault Isolation Devices (FIDs) which isolate the fault.

Distributed Grid Intelligence (DGI) controls the entire operation of the FREEDM system. The DGI is assigned to the IEM and IFM devices. So both the IEM and IFM devices will run the DGI software.

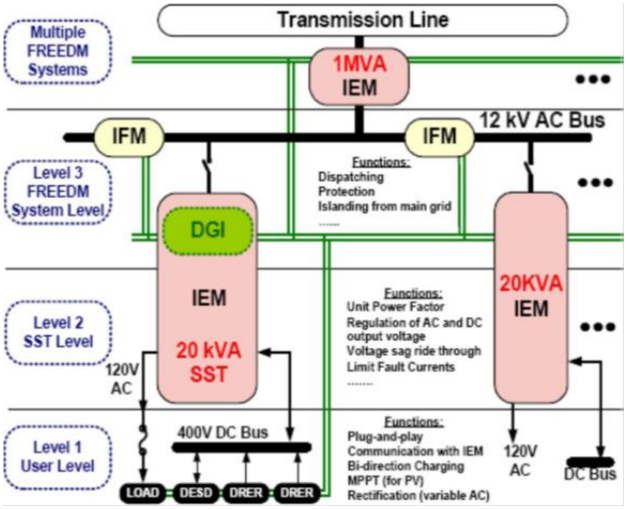


Figure 3.1. FREEDM model with multiple levels of control put reference [24]

Above shown is the FREEDM control system architecture of the FREEDM control system architecture. The levels are explained as following [24].

1. Level 1- This is the user level , where in residential loads, batteries and other DESDs connected to the grid are shown
2. Level 2-This level is at the SST (Solid State Transformer) level. In this the IEM regulate , manage and control the power flow of different DRERs (solar, wind).
3. Level 3- This is the level for the FREEDM system control and is present in all the IEM and IFM devices through the DGI software.

3.2 Protection Zone Concept

Protective zone concept is applied to the FREEDM system in which the system is divided into multiple zones, using the FIDs. The FIDs act same as a normal Circuit Breaker, the only difference being that the FIDs are capable of extremely fast current interruption in matter of micro seconds [Put reference]. The loads, DRERs and the DESDs are maintained

through the SST. So if a fault were to occur inside the zone, the FIDs at the end of the zone will operate to isolate the fault from the main loop. And also the SST connected to that zone will shut down, so that the local distributed generation is not affected by this fault. The FREEDM protection strategy is shown in the figure below.

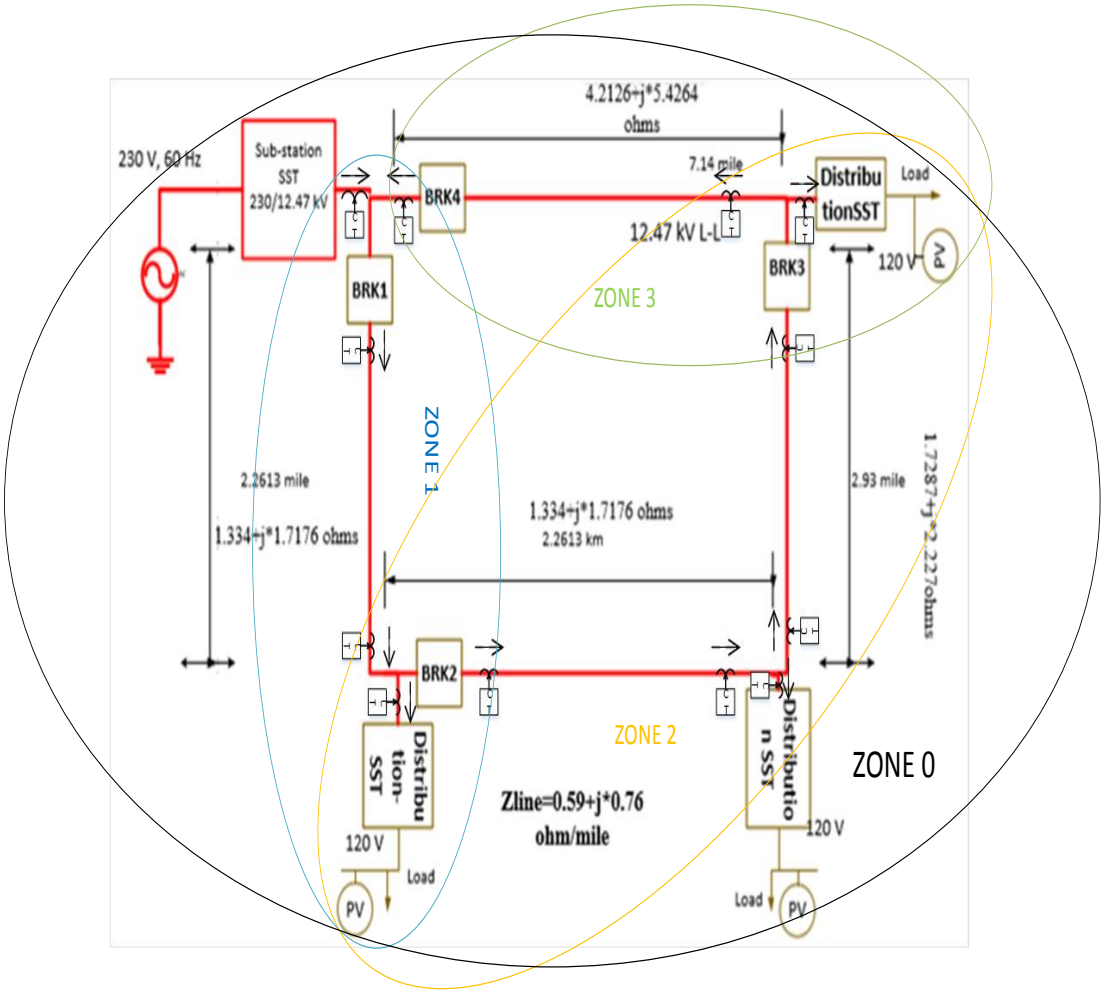


Figure 3.2. IFM zones of protection strategy [4]

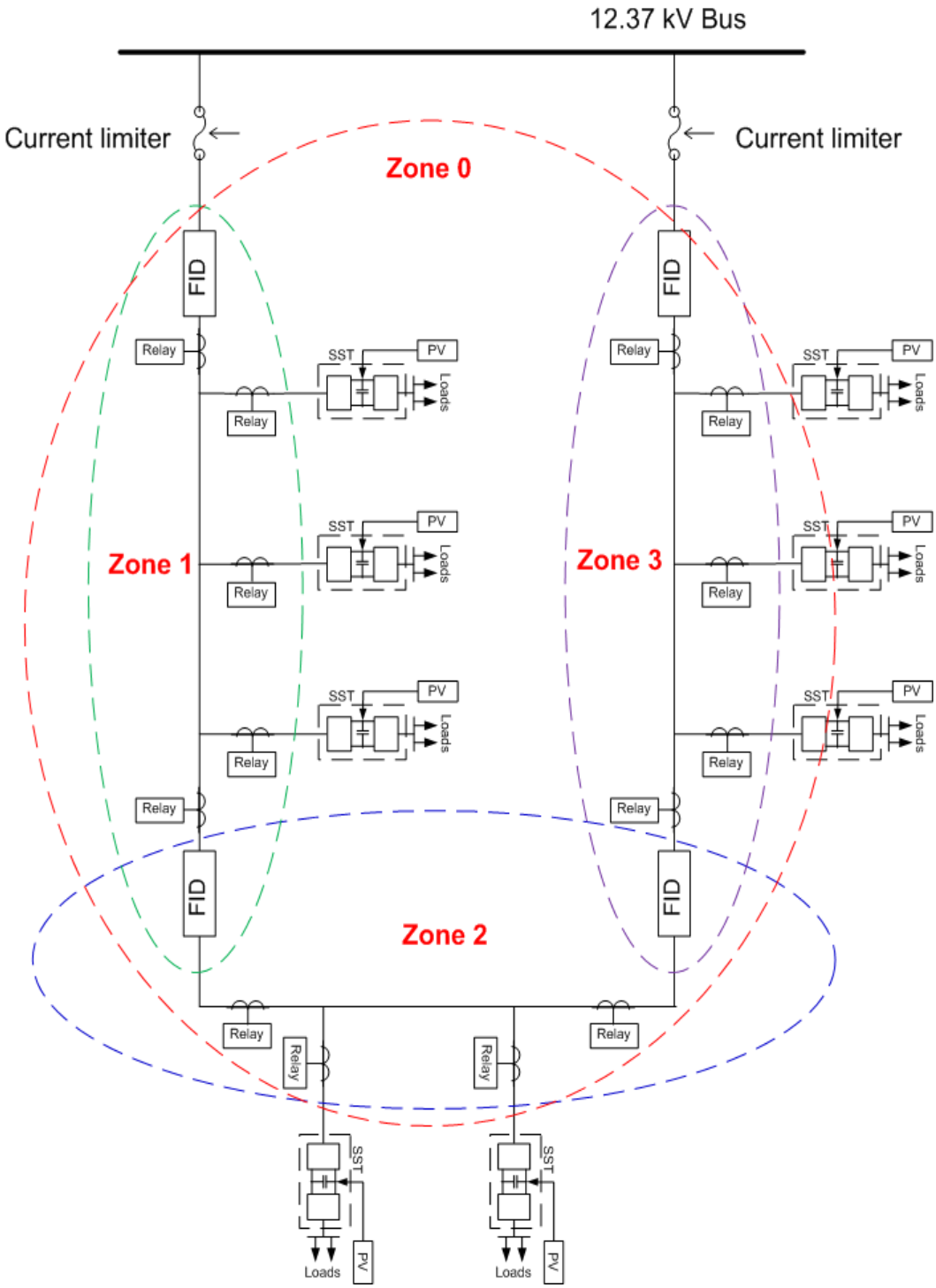


Figure 3.3. Alternate concept of the IFM zones of protection in FREEDM [5].

Above shown is the FREEDM zones of protection strategy in which there are 3 zones of protection and 1 large protection zone which includes the other 3 zones called Zone 0. The Zone 0 protection scheme will be seen as a backup protection scheme for the FREEDM system. The Novel fast pilot differential protection developed previously developed will be employed in each of the three zones. The Analog Merging Units (AMU) are connected to each of the terminals of the FIDs, SST primaries to record and digitize the magnitude of the current, and transmit the data back to the IFM. Every Zone has a separate IFM which will be running the DGI software with the pilot protection algorithm embedded in it [put reference].

The primary protection scheme is based on differential protection employed in each zone [5] [12]. The sum of currents in any particular zone should be zero. This demonstrates that either there is no fault inside the zone or fault exists outside the zone (also for which the protection unit doesn't trip). Now if the sum of currents in the zone is not zero, in that case, the faults exists within the zone, and then the IFM transmits the signals to the terminal end FIDS and SST in that particular zone to open up the zone and clear the fault on the main loop. All the samples sent from the AMU to the IFM have GPS time stamps to ensure the accuracy of the protection system algorithm. Here the SST acts as C.B /switch between the main loop and the secondary distribution system, and so the firing angle of the SST is made

zero during a fault, so as to disconnect the SST. The switching delay time for the SST is very less.

The IFM collects all the samples values from the AMU with identical time stamps and sums up all the currents in the zone and is the sum is zero in that case there's no fault, now if the sum is not zero, it holds the samples and analyses the next incoming data. For the next 10 samples, if the sum is still not zero, in that case the IFM declares a fault and sends a trip signal. If for the next 10 samples, the sum of the currents is zero in that case, there is a fault declared and the IFM resets the counter. The protection algorithm is employed through microprocessors [12].

The secondary protection algorithm is an overcurrent protection algorithm. In this scenario the IFM analyses all the current samples, and then compares it to a preset value that is 3-5 times the rated current. If the sample is greater than the prefixed value for the next 15-20 samples, in that case the IFM issues a trip signal to the FIDS. And if it doesn't last for 15-20 samples, then no trip signal is issued by the IFM. Zone 0 will act as backup protection of Zones 1, 2, and 3. Usually the measured values of the current in zone1, 2, and 3 are compared and the difference of the magnitude and direction of the currents are sent to the IFM. The coordination between Zone 0 and Zones 1, 2, and 3 are done in such a way that the protection algorithm is exactly the same, but the evaluation time is 5-10 times that of other zones/ so it will only operate when the zones 1, 2, and 3 protection algorithms fail to operate. So I this case the IFM provides both primary and backup protection.

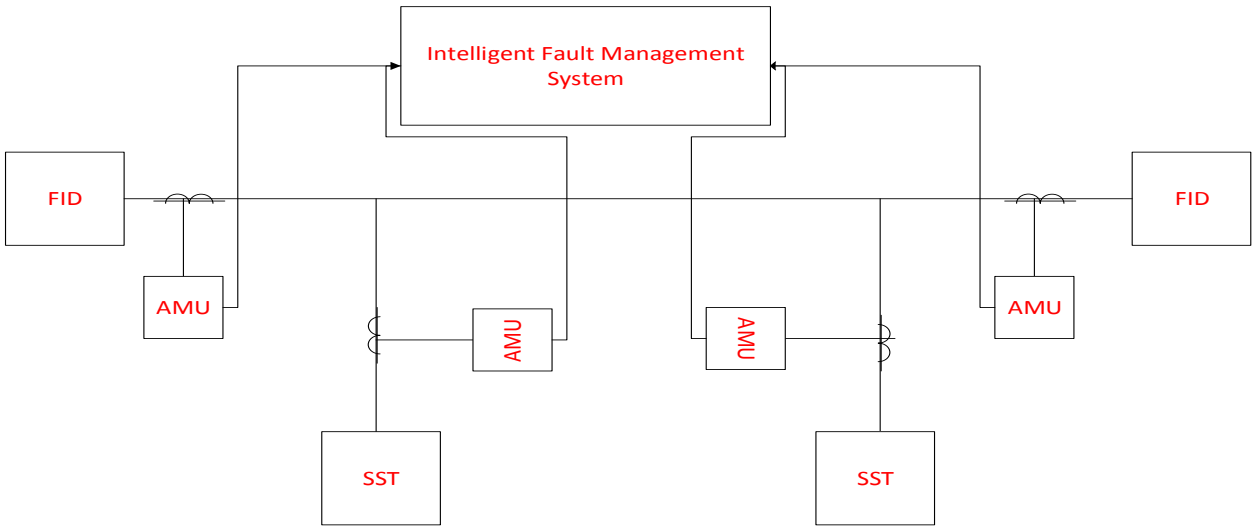


Figure 3.4. IFM system with the in cooperation of the AMUs

3.3 Sampling data

The speed, accuracy and precision of the IFM protection algorithm depends on the execution, sampling and communication method. The current from the CT is converted into a voltage signal by keeping a small resistor on the secondary side of the CT. The AMU consists of a microcontroller, which samples the analog voltage signal and gives data in a digital form. GPS (time stamps) are also added by the AMU, so that only data with similar time stamps are used in the algorithm by the IFM. So the IFM collects the sampled data with similar time stamps. It makes a sum of these sampled values from continues measurements, to see if the sum is zero or not. A tolerance of 5 % is assumed which defines the minimum operation current for the protection algorithm. For a fault, the IFM will hold down and count the next incoming samples. It will make a sum of the next 10 samples with time stamps, which would be 2 ms for a 100 samples/cycle measurement. If the sum of the

samples is not zero for all the 10 time stamps, it means that there is a fault in the zone and a trip signal is sent to the FID. If any of the 10 samples yields a sum of zero, the IFM declares that “no fault has occurred” and it resets the counter and starts recounting. This is supposed to be the primary protection. The AMUs are capable of sampling at a max rate of around 3.33 kHz. For this we have used the Ni CRio data acquisition unit, the working of whom and its slave measuring units is explained in upcoming sections. The communication channel used is Ethernet and it is IEC 61850 compatible (Substation automation communication regulations). The Ethernet connects the microcontroller (master) to the measuring units (slaves).

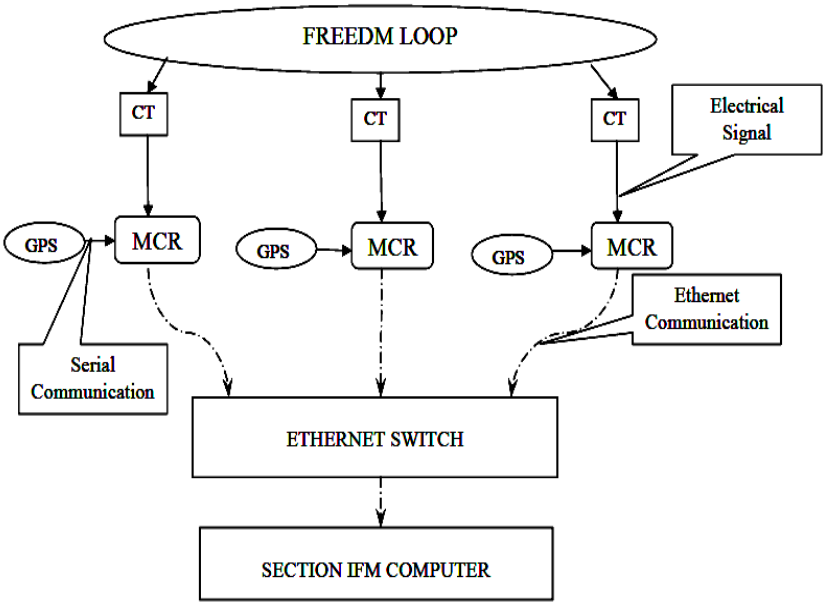


Figure 3.5. Schematic of protection system explained above [12].

3.4 Explanation of current differential algorithm

The novel pilot differential pilot protection algorithm was previously developed at ASU. The basis of this algorithm is actually developed from percentage differential protection used very widely and commonly in the power industry. It is used for bus protection/ transformer protection. So essentially the sum of currents flowing in a particular unit equals the sum of currents flowing out during normal operation.

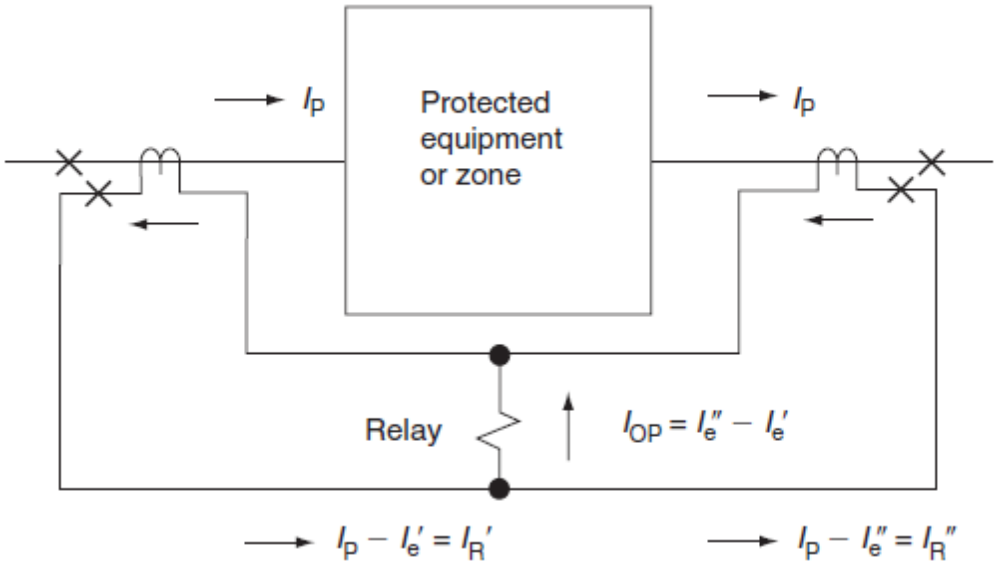


Figure 3.6. Differential current protection circuit diagram put reference [6]

Based on the figure above, the primary current is I_p and the secondary current is $I_p - I_e$, hence for the same ratio and type of current transformer

$I_{op} = I_e^{"} - I_e' \cong 0$ Under normal operation [6]

Usually this value not zero, but very small. This is actually the mismatch between the two CTs on each end. The current in these inhibit the operation of these currents.

A previously developed novel pilot differential protection algorithm with percentage slope characteristic is shown below. The differential protection scheme includes I_{op}(operating quantity) which is the summation of all the currents from all the recording/measuring points, and I_{res} (restraining quantity) which is the sum of the absolute values of the currents from all measuring points. A differential slope is also defined as the ratio of the operating quantity to the restraining quantity.

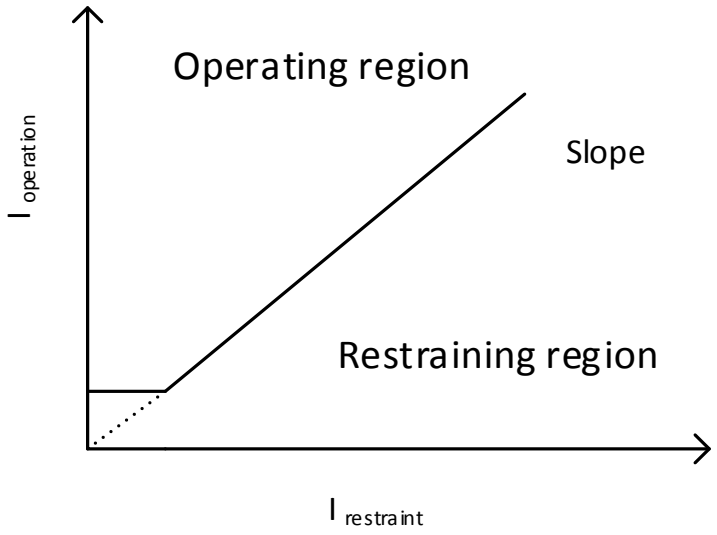


Fig 3.7. Slope percentage characteristic [12]

The operating and restraining quantities are initially calculated, and then the differential slope characteristic is calculated. If the slope is greater than a prefixed value, it will be in the fault region and if the slope is less than the value, it's in the blocking region of the diagram shown above. The mathematical expression for the percentage slop characteristic can be defined as follows [6].

$$I_{op} - S_0 . I_{\ res} > 0 \qquad (3.1)$$

$$and \quad I_{op} > I_0 \qquad (3.2)$$

Where $I_{op} = \left|\sum_{i=1}^{m} \dot{I}_\iota\right|$

$$I_{\ res} = \sum_{i=1}^{m} \left|\dot{I}_\iota\right|$$

m is equal to the total number of measuring points

I_i is the current amount at each measuring point

S_0 is the standard slope coefficient

I_0 is the minimum operating current (10 percent of rated current)

Now in comparison to I_{op} and $I_{\ res}$, I_0 is small, and hence we can write equation (3.2) as

$$I_{op} - S_0 . I_{\ res} - I_0 > 0 \qquad (3.3)$$

Now hence in equation 3.3 , both equation 3.1 and 3.2 are satisfied, hence we can write it as

$$\left|\sum_{i=1}^{m} \dot{I}_\iota\right| - S_0 . \sum_{i=1}^{m} \left|\dot{I}_\iota\right| - I_0 > 0 \qquad (3.4)$$

Now using the equivalent slope defined as

$$Let\ S\ be\ defined\ as\ S = \left|\sum_{i=1}^{m} \dot{I}_\iota\right| - I_0 \Big/ \sum_{i=1}^{m} \left|\dot{I}_\iota\right| \qquad (3.5)$$

Hence the expression can now be written as

$$S > S_0 \qquad (3.6)$$

This is very convenient for the calculation of the slopes [12].

So the equation 3.6 can be used for more practical applications like fault detection. The slope characteristic prevents mis trips in case of abnormal power system condition like load switching, CT saturating during fault, CT erode, transformer inrush current etc. [12].

3.5 Traditional over current protection using the SEL-351 S relay

This section includes the test experimental setup for the over current protection scheme with a commercial relay of Schweitzer Engineering Labs. This experiment will show the current benchmark for protection in the industry and also show the need for a faster, accurate and precise protection scheme. The figure for the single phase test setup is shown below.

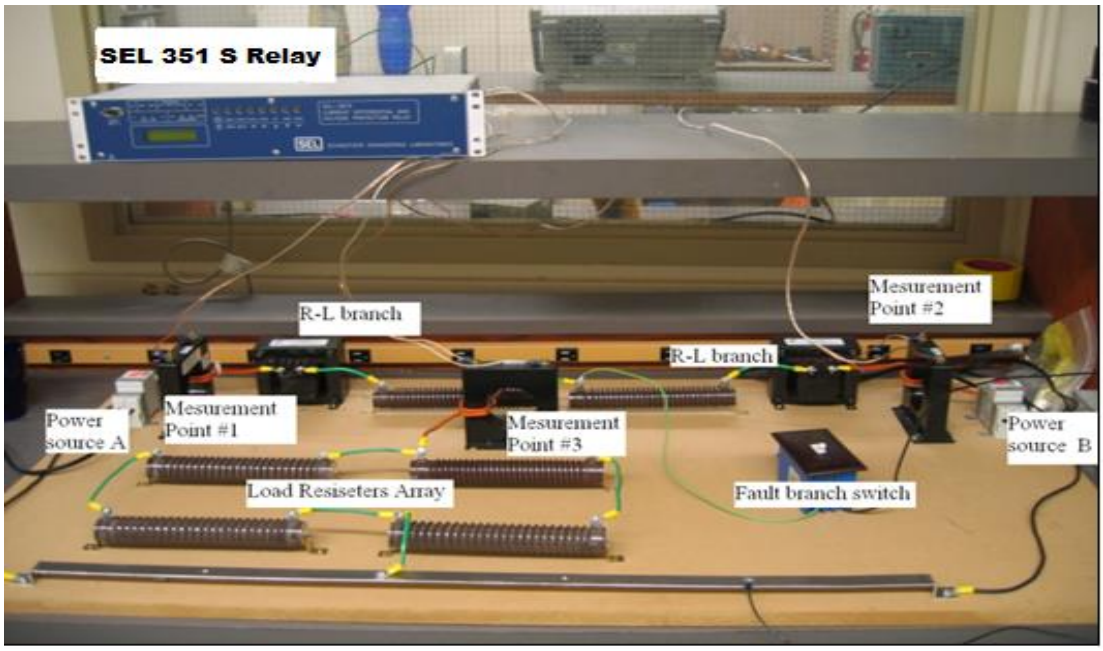


Figure 3.8. Single phase test setup for the SEL 351S relay

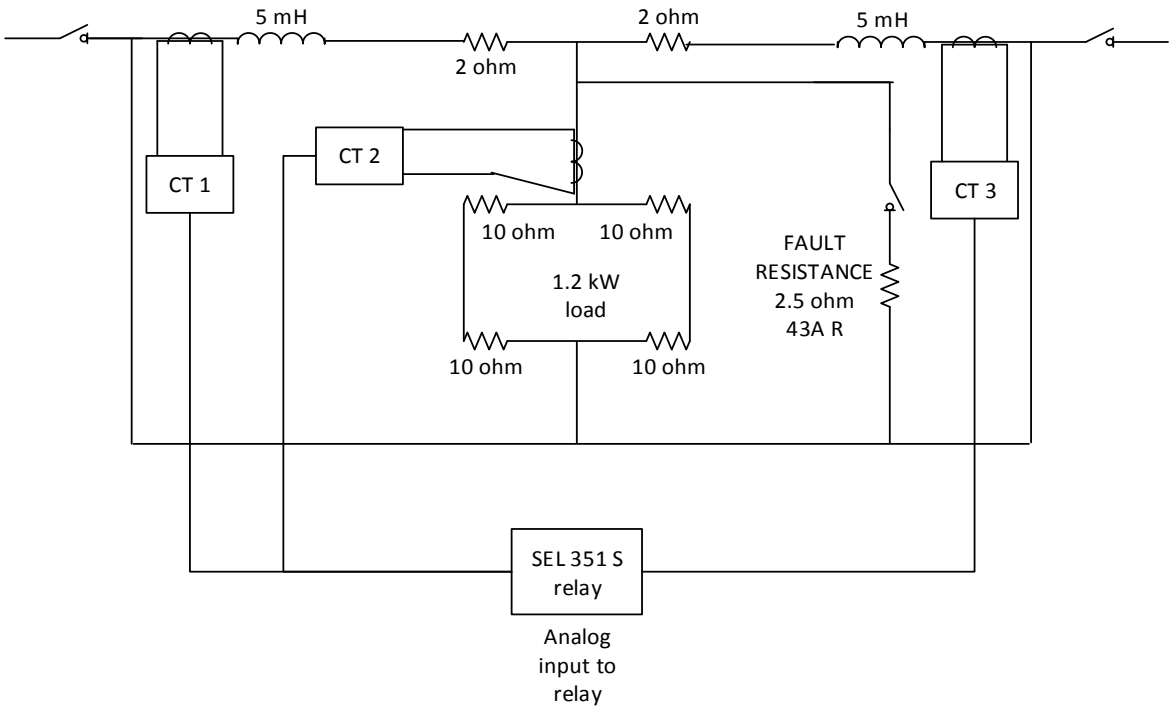


Figure 3.9. Schematics of the test setup for the SEL 351 S relay

As shown above, the test setup was developed at ASU [12]. The figure shows that it has two sources i.e. two basic 120 V, 60 Hz, utility grid sources (supplied at ASU). These sources are connected to SW1 and SW2. These are then connected to equal R-L circuits which contain a 2 ohm resistor and a 5mH inductor, which indicates a 1 mile distribution line which supply the loads. The rating of the load is 10 ohm, 1.2 kW which is arranged by setting up (2X2) 300 W 100 ohm resistor bundles. The fault branch is 2.5 ohm 1 kW resistor connected through a switch SW3 which is in parallel to the load to create a shunt fault. The CTs are rated for a (100:5) ratio and are connected at the two source terminals and the load terminals.

The three CTs measure current at each point mentioned above. The CT primaries are double wound, so that adequate current is produced in the secondary, thereby making the equivalent ratio as 50:5 for each CT.

For pre fault condition:

In the initial case, the switches SW1 and SW2 are closed while SW3 is open. The grid source feeds the load and this is defined as the normal operating condition/ pre fault condition. The currents $I_1, I_2\ and\ I_3$are measured by CT1, CT2 and CT3 respectively. During normal operation

$$I_1 + I_2 = I_3$$

When SW3 closes, the loads are bypassed and no longer the equation $I_1 + I_2 = I_3$ holds true. The fault current is approximately 3 times the rated/nominal current. The table below shows the pre fault and fault condition currents.

Table 3.1: pre fault and fault condition currents

	I1	I2	I3
Pre-fault	6.4A	6.4A	12.8A
Fault	16.7 A	16.7A	6.7A

From the table shown in Table 1, utilizing the RMS value and the power flow current direction as reference direction. Based on the CT equivalent ratio, the secondary current input from the CT is calculated and listed in table 2.

Table 3.2: CT output current

	I1	I2	I3
Pre-fault	0.64A	0.64A	1.08A
Fault	1.67 A	1.67A	0.67A

3.6 SEL 351 S relay

The SEL 351 S relay has a multitude of protection schemes including over current, instantaneous, time varying, inverse, directional and other protection schemes. It is the most selling unit for SEL and can be used in a variety of systems/models. It can be used for distribution protection, unit protection, line protection etc. The SEL 351 S has Ia, Ib and Ic inputs as shown in the figure below. i.e. it has 3 phase current input, along with Va,Vb and Vc inputs i.e. 3 phase 1 feeder voltage input.

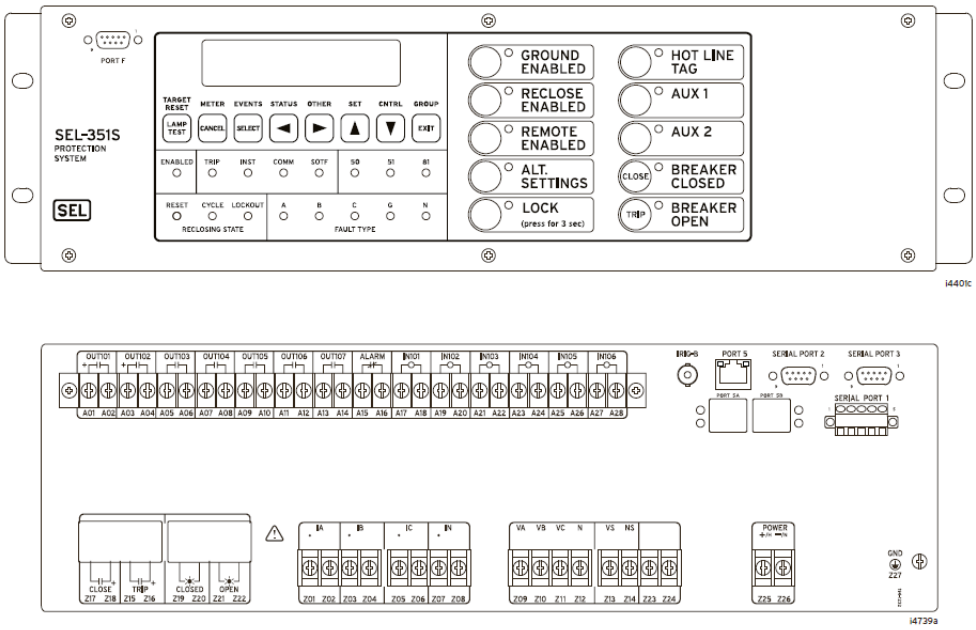


Figure 3.10. SEL 351 S schematic for front and back panel [25]

For the test bed setup, we are only going to connect I_1 to I_a input of the SEL 351 S relay. The relay is configured by using the AcSELerator software. For our purposes we will be using the instantaneous over current protection scheme. There are four levels of the instantaneous over current elements available in the SEL 351 S. For the instantaneous O.C

protection, the setting of the 50P1P bit for the relay is to be set which will be the pickup current value.

Setting range for the 50P1P: 0.25 – 100 A (5A nominal phase input current) [25].

Now for our setting we set the bit value as 1.5 times the nominal secondary current, and when the switch is opened the following fault event is created which is shown below.

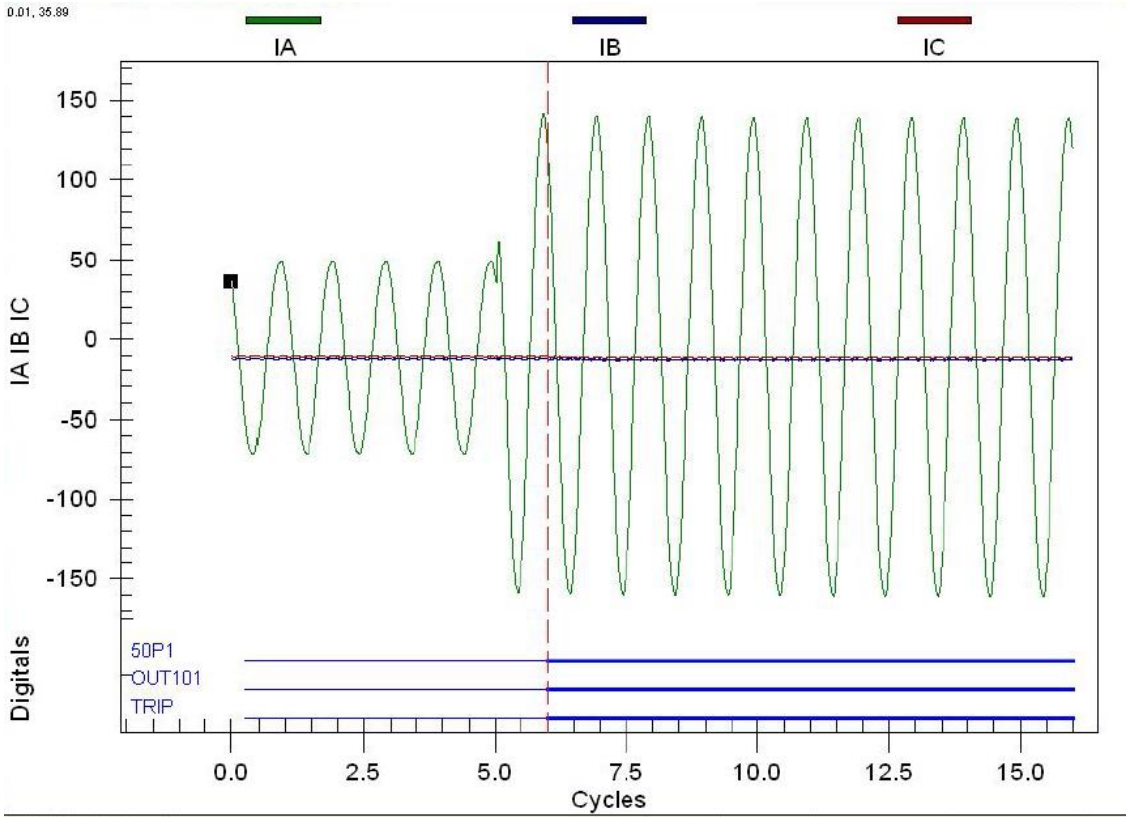


Figure 3.11. Fault inception and detection timing as shown in the AcSELerator software

The event manager records an event in the relay whenever a trip, or any other such command is issued. This event graph is stored in the relay and can be viewed any time later on. The graphs show that the detection time for the SEL 351 S relay is around 1 cycle. This

operation time is one of the fastest as compared to any relay in the power system industry. This gives us the set standard for protection time for the instantaneous O.C relay in the existing commercial protection system. This is not fast enough to catch up with the operation speed of the FID system [12] which can interrupt faults extremely fast in the FREEDM system.

Drawbacks of the SEL 351 S:

- The SEL 351 S is only capable of one 3 phase input for current and voltage, so it's not possible to protect multiple 3 phase feeder lines with this relay [25].
- The relays can communicate with each other using the mirror bit communication, but the amount of data that can be sent is minimal and industry experts still prefer SCADA for communication setup. Hence a need for a better, faster, reliable and more data capacity handling communication method is required [26].
- Also the mirror bits can lose information because of loss of fiber or loss of DC power. The delay due to mirror bit communication can be up to 6 cycles.
- The relay also only accepts analog signals, so it can be used only for unit protection, particular section of line but it can't be used for protecting a large distribution system.
- Based on these questions, ASU developed the previously mentioned pilot protection scheme with slope differential characteristic. This method uses digital sampling and could communicate with FID's, SST's. Using the AMU, the data from the CT is transmitted to the IFM with little or no loss of information. The new

developments in the previously developed pilot protection scheme and the implementation of the new pilot protection scheme for large systems/ large distribution systems will be explained in the upcoming sections [12].

3.7 New pilot protection algorithm and its simulation on the test bed

In the previous sections, the pilot differential protection was designed to operate on the main loop of the FREEDM system i.e. the high voltage side of the SST. The system has an algorithm to find out the location of fault within a certain zone/section of the loop and to send the trip signal to the FIDs located at the two terminal end. This achieved by digitally sampling the current waveform at different measuring points in a given zone and a fault is conclude when the differential protection algorithm equation doesn't hold true for a given se t of samples. The figure below represents how a fault is detected in the counter method.

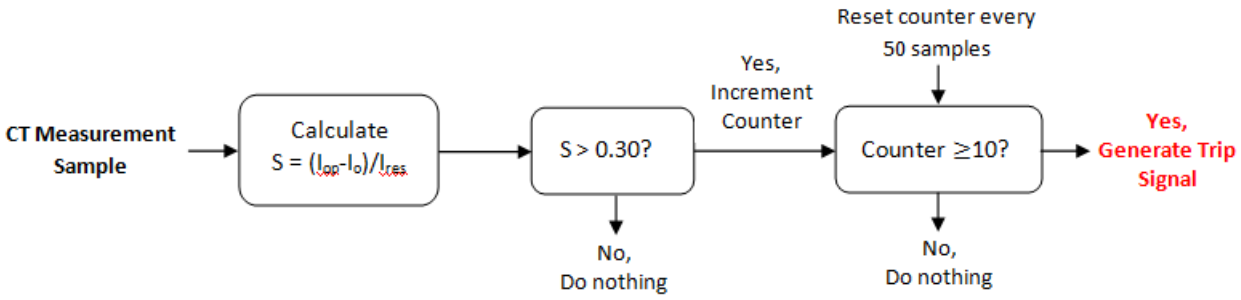


Figure 3.12. Counter method algorithm

A fault is said to exist in the particular zone when the left side expression evaluates to be greater than the set parameters S_0explained in the earlier section for 10 consecutive samples. The counter is reset after every 50 samples to prevent transient and other disturbances over long periods of time to cause false trips.

This algorithm is basically an extension of Kirchhoff's current law , i.e. if the sum of currents in a zone no longer equals zero in that case, there must be a current existing in that

zone that is unaccounted for and that's how a fault is concluded. The quantity S_0 is set to a prefixed value of 0.3 to make sure that the fault is only concluded when the vector sum is at least or greater than 30 % than the magnitude sum of all currents in that zone. The quantity I_0 term helps remove zero crossing disturbances and hence is kept around 10 % of normal operating line current.

$$\frac{I_{operation} - I_o}{I_{restrain}} \leq S_o \qquad (3.7)$$

This equation shows that the overall value of that equation should be less than S_0 so that there is no trip.

The delay between the actual fault occurrence and the trip signal generation is affected by two components. The communication delay between the main CPU module and the AMU units and the delay associated with the physical hardware performing the complex computations. The hardware which will be explained in the next section in detail, consists of the NI CRio 9022 main CPU module, NI 9144 chassis housing the NI 9215 Analog to Digital converter slave measuring modules. These are connected to the CT to measure the current. The hardware is connected in a daisy chain network.

3.8 Pilot protection model simulation is PSCAD

The pilot protection system module was constructed, tested and simulated in PSCAD with 2 control switches for activating the primary differential protection and an O.C backup protection. Both the main pilot protection and the backup protection work independently of each other, and hence each of them have a separate trip signal designed. The input receives the CT outputs. For the simulation testing a similar test bed is developed in

PSCAD using the data from the real test bed explained in the previous section. The fault currents, and the CT currents all match the values that were used for the SEL 351 S relay experiment. This will help us examine closely the results for the simulation and the actual testing on the same test bed. The test setup diagram in PSCAD is shown below.

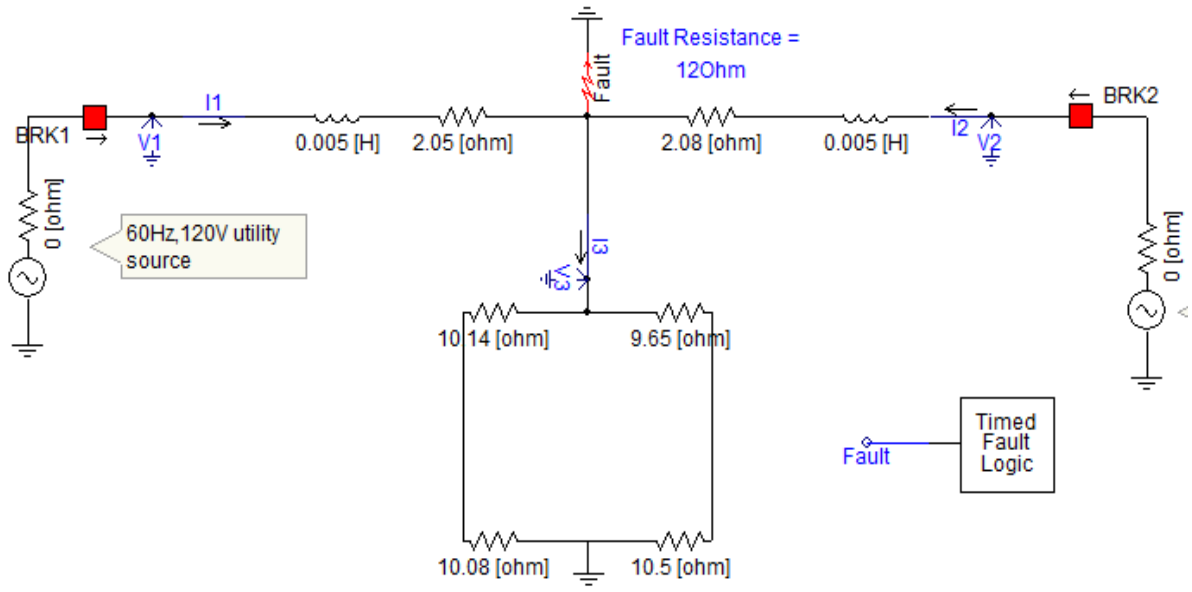


Figure 3.13. Test set up for simulation is PSCAD.

The figure of the protection block using the ‘counter system’ is shown below

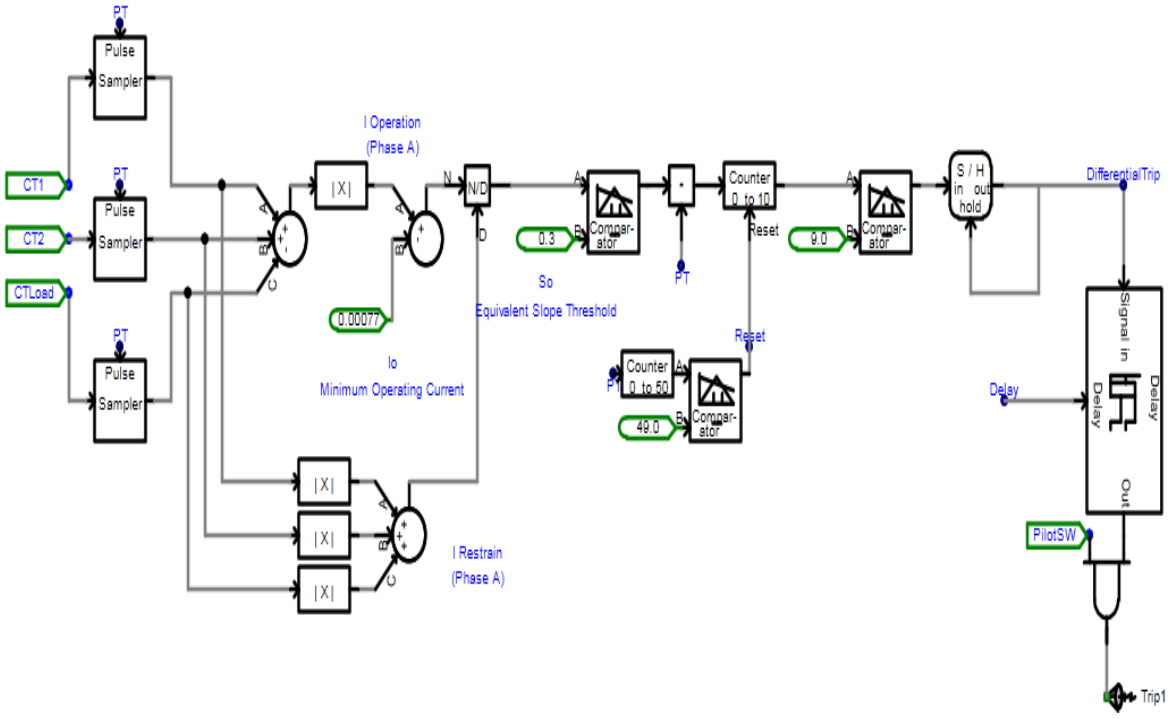


Figure 3.14. Pilot differential protection using the counter method

The above figure shows the internal working of the 'counter system' pilot differential protection system. On the extreme left, the CT inputs are sampled by multiplying them with the impulse train. The impulse train is usually set at a standard frequency at which sampling is done. From the sampled values the vector sum of current ($I_{opereation}$) and magnitude sum of currents ($I_{restraint}$) are calculated. I_0 is subtracted from $I_{opereation}$ and the ratio of this value to $I_{restraint}$ is sued to calculate the equivalent slope S. The value is then compared to $S_0 = 0.3$. If $S > S_0$

Then the counter is augmented by 1 for every sample until it reaches 10 and then a trip signal is generated. The counter is reset after every 50 clock cycles to ensure that only a genuine fault will generate a trip signal. When a trip signal occurs a DC output of 1 is generated and held till a reclosing action is not given or commanded. The sampling rates

have a varying effect on the fault detection times. The final trip signal output is then delayed by the value calculated by the hardware delay calculation implemented to model the delay imposed by the NI cRIO -9022 and its connected slave modules.

3.8.1 Construction and Testing of Backup Overcurrent Protection Component

The overcurrent portion of the pilot protection system simply serves as a backup protection to the differential system. It compares the instantaneous current received at the CT measurement modules to a preset value of 3+ times the normal rated current. Similar to the pilot system, it increments a counter for every sample that is above the preset threshold value. When the counter reaches 20, a trip signal is generated. An additional counter resets the trip signal counter every 200 samples to prevent false trip signal generation. The objective of this backup system is to provide system protection in the event that a fault is not detected by the differential system. Consequently, when a fault is on the low voltage side of the SST, the backup system will also generate a trip signal since the differential system will not consider this a fault.

The backup overcurrent system is not selective, and thus cannot properly isolate a fault in its respective zone. The system only requires one of the CTs to measure above the threshold in order to generate a trip signal. As this is a backup protection system, this is not necessarily of any concern. The backup system PSCAD circuit is shown below in figure 15.

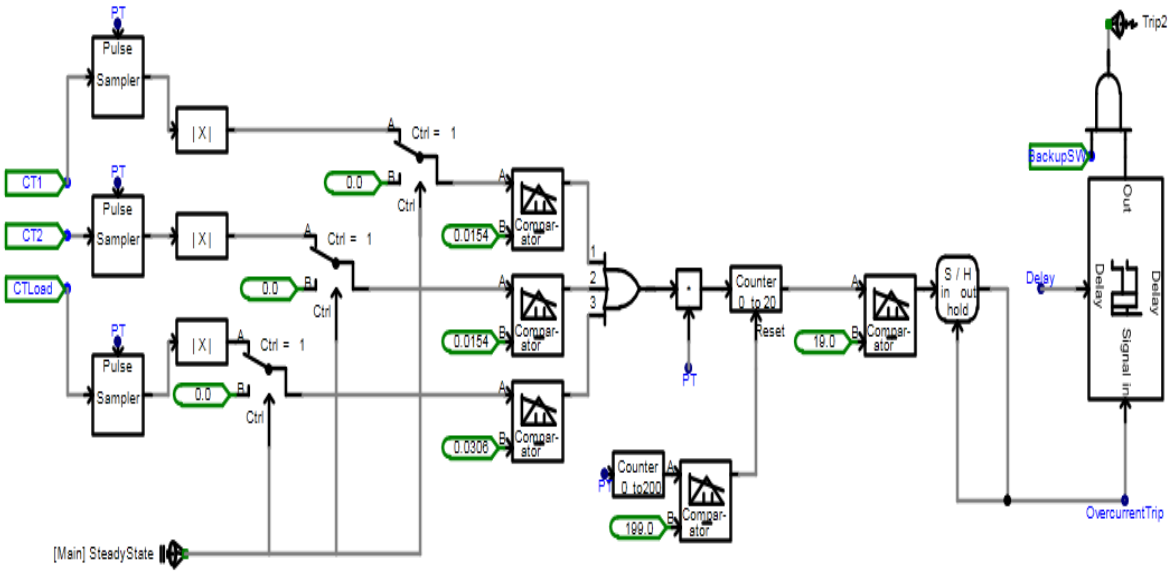


Figure 3.15. Backup Overcurrent Protection PSCAD Circuit.

3.8.2 Investigation of Hardware Communication and Processing Delay

Based upon data and benchmark tests published by NI, the delay associated with the hardware utilized in the prototype test bed system manifests in two ways: “slave cycle” time and “program update” time. The “slave cycle” time is the amount of time required for all of the sampled data from the CTs to arrive back to the primary module after it has been requested from the primary module. The “program update” time refers to the time it takes for the primary module to process the data. This delay is affected by the number of sample points or slave modules, and the length of the communication cable. Both operations occur simultaneously in the hardware, so whichever process is slower is the limiting factor. Therefore, the maximum sampling clock speed of the CT waveforms is limited by the total number of measurement points (from CT waveforms) and the total length of communication wiring.

The delay time calculations and model delay implementation is performed by utilizing data given by NI, available at [27] and [28]. The NI cRIO-9022 module is the primary module currently being used in the prototype test bed. The basic delay computation is made using the following data. As shown in the table below, this module will only allow up to 10 measurement modules to be utilized while sampling at the desired speed of 6000Hz, or 100 samples per 60Hz cycle. This indicates that a maximum of 10 SSTs per zone could be implemented using this hardware configuration at 6000Hz sampling speed. This does not necessarily represent a problem, as 10 SSTs per load is an unlikely scenario.

Delay data for NI PXI-8106 Module:

BASE cRIO-9022 Logic Delay: **0.111 ms**

Additional Delay Per I/O: **5.1377µs**

Table 3.3. Maximum Measurement Modules Supported at 1200Hz and 600Hz Sampling Speed for cRIO-9022

Sampling Speed:	Maximum Measurement Modules
1200Hz (20 samples/cycle, 17ms trip response)	140
6000Hz (100samples/cycle, 1.9ms trip response)	10

While this module is not currently being used in the test bed system, a quick investigation into the advantages of using a more advanced piece of hardware was performed. The NI PXI-8106 is a considerable more powerful primary module, at an approximate 25%

increase in cost over the cRIO-9022. This module offers a 21 times increase in supported measurement modules at the desired sampling speed of 6000Hz. This increase performance would allow for an even faster sampling speed if desired, as there is no practical need for the ability to implement 211 SSTs per zone.

Delay data for NI PXI-8106 Module:

BASE PXI-8106 Logic Delay: 0.036 ms

Additional Delay Per I/O: .6171μs

Table 3.4. Maximum Measurement Modules Supported at 1200Hz and 600Hz Sampling Speed for PXI-8106

Sampling Speed:	Maximum Measurement Modules
1200Hz (20 samples/cycle, 17ms trip response)	1,291
6000Hz (100samples/cycle, 1.9ms trip response)	211

The slave cycle time is the amount of delay associated with the communication between the daisy chained current transformer measurement modules and the primary module. This data is for an NI 9144 chassis with NI 9215 module. The total delay is the sum of the delay due to Ethernet cable length and the delay due to each measurement module.

Delay data for NI 9144 Chassis with NI 9215 Module:

Base Delay: 8.096μs

Delay per measurement module: 3.476 μs

Ethernet Cable Length Delay per meter: 5 ns

Table 3.5. Slave Cycle Limitations for NI 9144 Chassis with NI 9215 Modules

Max Modules at 0 meters of Ethernet Cable	
Sampling Speed:	Maximum Measurement Modules
1200Hz (20 samples/cycle, 17ms trip response)	2,317
6000Hz (100samples/cycle, 1.9ms trip response)	462
Max Ethernet Length at 3 Measurement Modules	
Sampling Speed:	Maximum Ethernet Length
1200Hz (20 samples/cycle, 17ms trip response)	≈ 148,100 meters
6000Hz (100samples/cycle, 1.9ms trip response)	≈ 26,933 meters
Max Ethernet Length at Max Supported Number Modules	
Sampling Speed:	Maximum Ethernet Length
1200Hz (20 samples/cycle, 17ms trip response)	≈ 59,500 meters
6000Hz (100samples/cycle, 1.9ms trip response)	≈ 22,500 meters

This delay data computation is included in the PSCAD Pilot Protection component and adds the computed amount of delay time to the time of the final trip signal generation. Also included in the model are two error outputs, which indicate if the amount of delay

time for either the program update or slave update is longer than would be allowable by the sampling frequency. This delay segment of the PSCAD component is shown below.

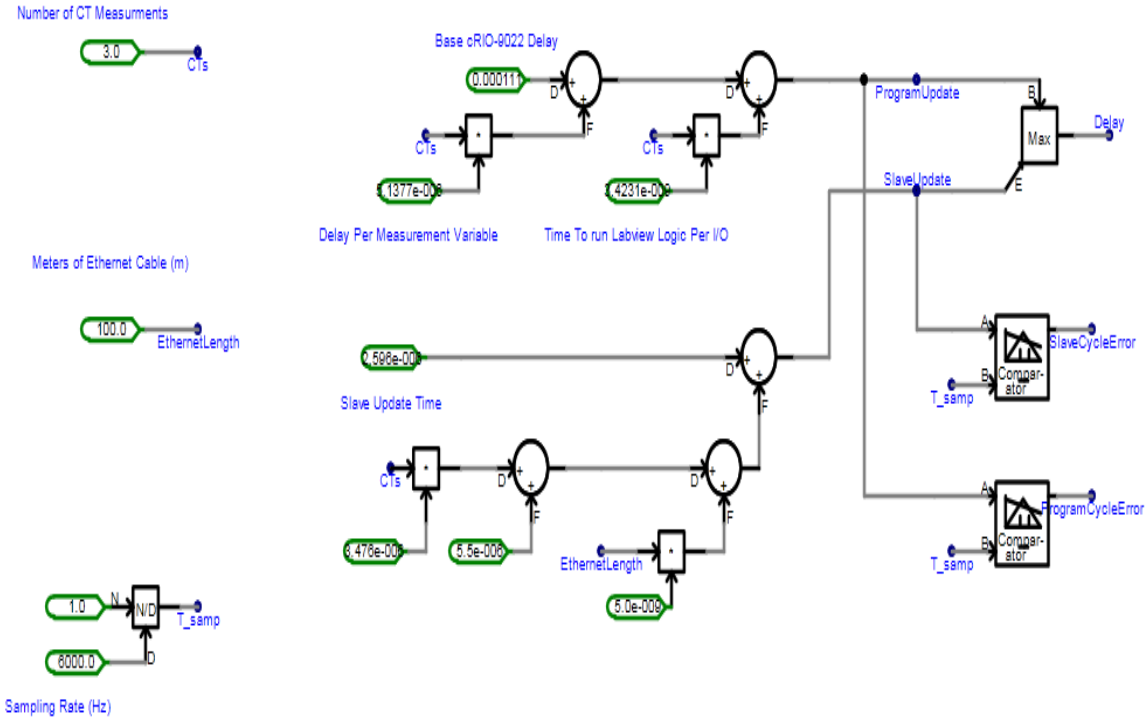


Figure 3.16. Hardware/Communication Delay Computation Circuit.

In order to test the effect of this delay, two test cases are presented. One test case investigates the amount of additional delay if 4 SSTs are included in one zone of the FREEDM Loop, while the other test case shows the additional amount of delay if 8 SSTs are included in one zone. These simulations are running at 6000Hz, with a fault occurring at precisely 1 second, a zero-crossover point. The delay data utilized is for the crRIO-9022 with NI 9144 / NI 9215. For reference, the amount of delay to generate a trip signal with 1 SST is shown below.

For the 4 SST/Load case, the theoretical hardware processing/communication delay time should be **0.111ms** base delay + **(6)5.1377µs** delay for 6 I/Os since there are 6 total CT measurements being made. This will result in a total hardware delay time of: **0.1418 ms.** Figure 3.17 below shows the simulation result, which closely matches the calculated time delay.

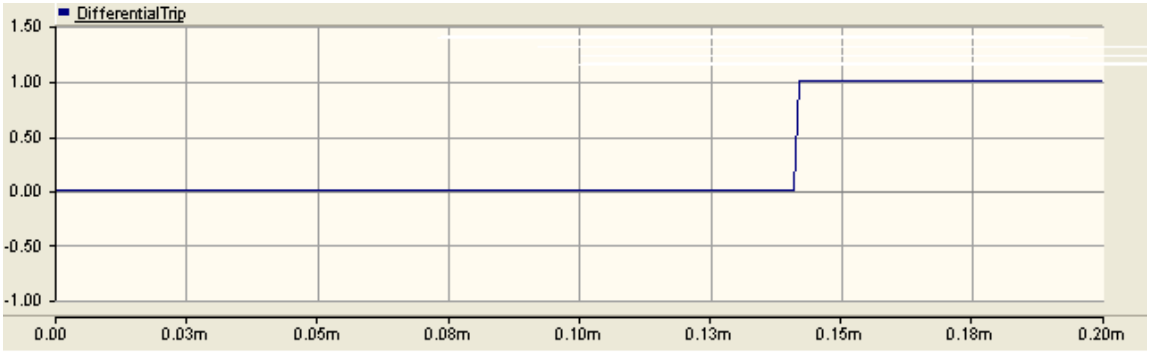


Figure 3.17. 4 Load Communication/Processing Delay

For the 8 SST/Load case, the theoretical hardware/communication time should be **0.111ms** base delay + **(10)5.1377µs** delay for 10 I/Os since there are 10 total CT measurements being made. This will result in a total hardware delay time of: **0.1624ms.** Figure 3.18 below shows the simulation result, which closely matches the calculated time delay.

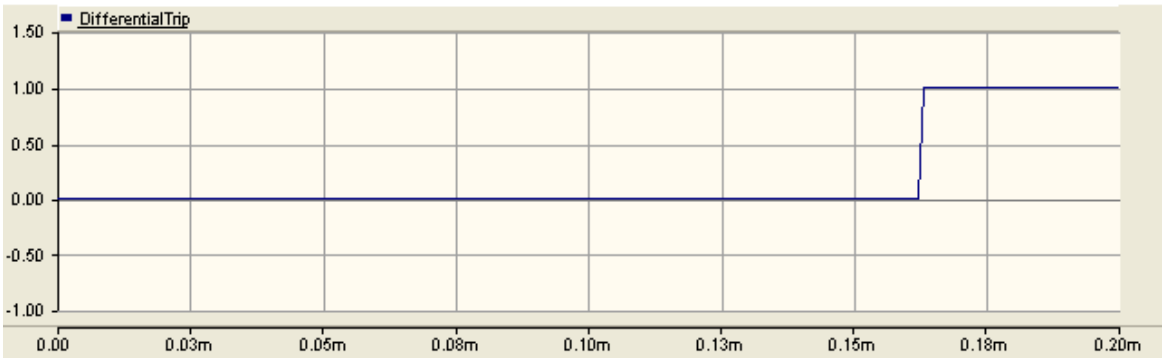


Figure 3.18. 8 Load Communication/Processing Delay

These results demonstrate the algorithm's ability to accurately delay the trip signal by the calculated results. These delay calculations are based upon test bench data from NI, and the parameters can be easily modified to simulate the delay for any other NI hardware configurations.

3.8.3 Rolling Window concept [30]

A new method of the rolling 10-sample or more average was proposed and implemented into the system. This is performed by using the existing formula to calculate the value of the slope for each sample, and saving the value. The previous 9 samples are then added to the present slope value and averaged. Once this average rises above the 0.30 slope threshold value, then a fault is concluded and a trip signal generated. This method eliminates the need for a reset counter while protecting the system from transients or other non-fault occurrences which have the potential to generate an unwanted trip signal. Furthermore, to increase reliability while maintaining fast operation speed, the sampling speed and number of averaged sampled can be increased. A pictorial depiction of what is being done is shown in figure 19 below, and a snapshot of the actual circuit constructed is shown in figure 20.

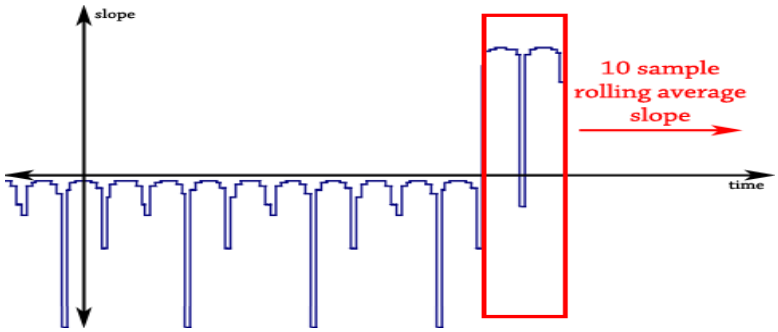


Figure 3.19. Rolling Slope Average

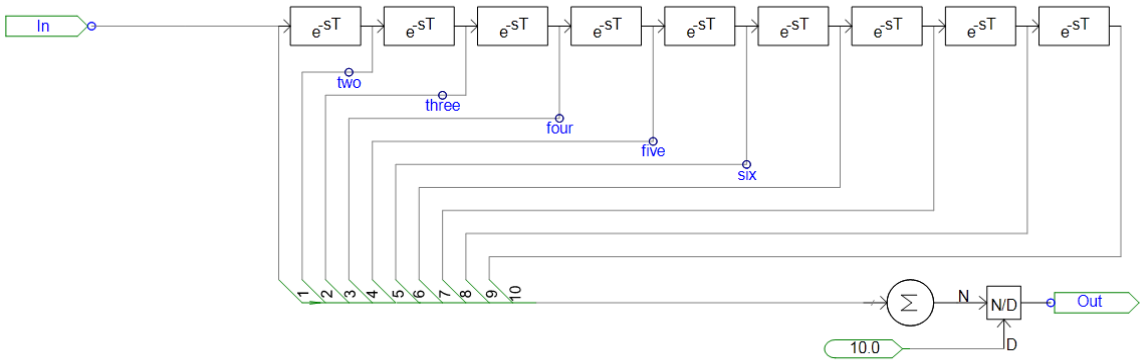


Figure 3.20. 10 Sample Rolling Average Block [29]

3.8.4 Investigation of Fault Timing on Pilot Protection Algorithm Reliability and Consistency for the test bed simulation in PSCAD

In order to test the consistency and reliability of the pilot protection system and the backup overcurrent protection, an investigation into the impact of fault timing and the overall delay until trip signal generation needed to be completed. To test the system, faults were simulated in standardized increments over several periods in order to test how the system reacts when a fault occurs at different points of the 60Hz cycle waveform on the test bed setup shown above in figure 13. These tests were carried out at both 1200Hz and 6000Hz sampling speeds, and the delay incurred due to the physical hardware communication (which is investigated in previous section) was neglected. The following tests were run in order to test for system consistency:

1. Differential System at 6000Hz sampling speed for 4 cycles.
    - Reset Counter On,
    - Reset Counter Off,
2. Backup Overcurrent System at 6000Hz sampling speed for 4 cycles
    - Reset Counter On,
    - Reset Counter Off,
3. Differential System at 1200Hz sampling speed for 4 cycles.
    - Reset Counter On,
    - Reset Counter Off,
4. Backup Overcurrent System at 1200Hz sampling speed for 4 cycles
    - Reset Counter On,
    - Reset Counter Off,
5. Differential System at 1200Hz sampling speed for 4 cycles.
    - Reset Counter On,
    - Reset Counter Off,
6. Differential System with 10-sample Rolling Window Average Slope for 4 cycles
    - 6000Hz sampling speed,
    - 1200Hz sampling speed,

- 1000Hz sampling speed,

7. Backup Overcurrent System with 10-sample Rolling Window Average Slope for 4 cycles

    - 6000Hz sampling speed,
    - 1200Hz sampling speed,
    - 1000Hz sampling speed,

The 6000Hz differential protection system results show that the differential protection portion averaged at a delay of 0.0019911 with a standard deviation of 0.0005295.

It is clear from analyzing these results that the action of the reset counter has the ability to nearly double the amount of delay that one would anticipate the system to exhibit if the timing of the fault occurs just before a counter reset. Because of this, this is perhaps not the best method of protecting the system from false fault tripping. Neglecting the timer resetting affects, the differential system displays very little change in the amount of time it takes for the system to generate a trip signal and the point at which the fault occurs on the current waveform period. The overcurrent system does, however, does exhibit some change in trip generation time over the course of the current waveform period. This occurs because instantaneous current measurements are used to increment the overcurrent fault counter. A consequence of this is that the counter does not increment at or around a zero-crossover while the current is below the overcurrent threshold setting. A possible solution

to this issue will be to utilize the RMS current value instead of instantaneous current. And hence the 10 sample rolling window average method was developed.

The following table displays all of the pertinent results from the tests conducted. The results suggest that faster sampling speeds result in smaller standard deviations, indicating increased reliability and predictability of system behavior. The bolded results show the fastest response times for both the differential system and the backup overcurrent system while maintaining very low standard deviations.

Table 3.6. System Reliability Test Results

Test Description	**Avg Trip Delay**	**Standard Dev.**
Differential System at 6000Hz sampling speed, Reset Counter On	0.0019911 s	0.0005295
Differential System at 6000Hz sampling speed, Reset Counter Off	0.0019266 s	0.0002101
Backup Overcurrent System at 6000Hz sampling speed, Reset Counter On	0.017650 s	0.0060235
Backup Overcurrent System at 6000Hz sampling speed, Reset Counter Off	0.0075732 s	0.0016938
Differential System at 1200Hz sampling speed, Reset Counter On	0.011573 s	0.003042

Differential System at 1200Hz sampling speed, Reset Counter Off	0.008750 s	0.000259
Backup Overcurrent System at 1200Hz sampling speed, Reset Counter On	0.0810013 s	0.002291
Backup Overcurrent System at 1200Hz sampling speed, Reset Counter Off	0.0810013 s	0.002291
Differential System with 10-Sample Rolling Average at 6000Hz	**0.001397 s**	**0.000432**
Differential System with 10-Sample Rolling Average at 1200Hz	0.005521 s	0.000237
Differential System with 10-Sample Rolling Average at 1000Hz	0.007378 s	0.000485
Backup Overcurrent System with 10-Sample Rolling Average at 6000Hz	**0.011334 s**	**0.00059**
Backup Overcurrent System with 10-Sample Rolling Average at 1200Hz	0.016824 s	0.001036
Backup Overcurrent System with 10-Sample Rolling Average at 1000Hz	0.020453 s	0.000982

3.9 Hardware test setup and comparison with PSCAD simulations [30]

The hardware model was initially developed at ASU, and the latest addition to the algorithms on the hardware setup as explained in [30]. The necessary changes were made

to obtain faster and more accurate results. The new algorithm was also applied to the hardware to verify the simulation results.

3.9.1 System Hardware and Description

The system is built using NI modules, and in the next few paragraphs the NI modules used and their workings are described.

1.NI CRio 9022: The compact reconfigurable input output (CRio) hardware module is the master controller and will send out directives to its slave modules/AMU units to sample data. The master and the slave units are connected to each other through the Ethernet cable and can be programmed using NI Lab view software. The processor speed is around 533 MHz with 2 GB nonvolatile storage and 256 MB DDR2 memory. With this large amounts of data can be stored and processed equally fast.

2. NI 9144: This is a hardware chassis module which can house up to 8 modules of the NI 9215 (slave modules). The three NI 9144 modules are connected in a daisy chain network with the CRio. These 9144 modules are compatible with EtherCAT, and hence have greater speed as compared to other Ethernet connected system. The single programming ability, so that the module can be programed for custom timing, in line processing and closed loop control are some of its other features.

3. NI 9215: These are the slave units, which consist of analog input module channels, which sample the current measured at the CT. These modules are housed to the NI 9144's chassis module and hence can send sampled data to the CRio through the EtherCAT cable. The max rate of sampling is 100,000 samples/sec/channel. The units (NI 9144+NI 9215)

together comprise of the Analog Merging Unit (AMU) and act as slave to master controller CRio 9022.

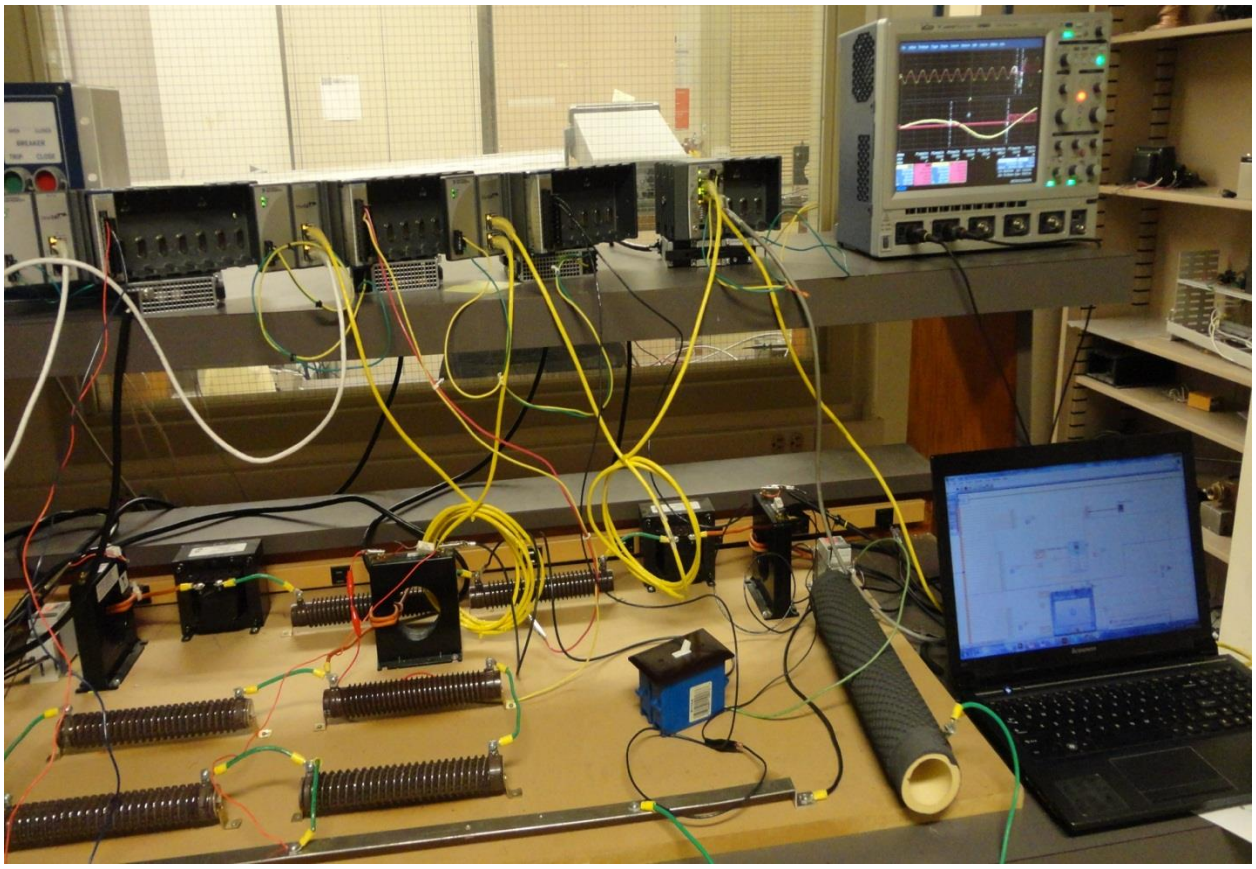


Figure 3.21: Picture of the NI hardware as connected on the test-bed [30]

3.9.2 System Functioning

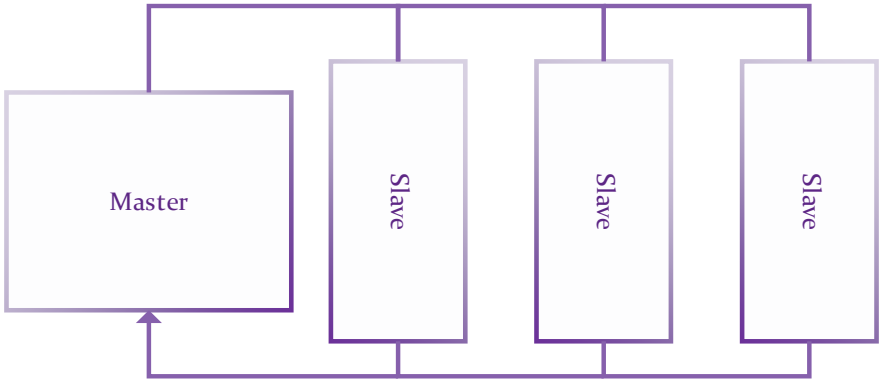


Figure 3.22. Flow of data

A single message is delivered by the master to the three AMUs. As the message is delivered in a daisy chain and back towards the Master, each AMU reads its input and adds its output to the message. When the message carries back to the master CRio, by then every AMU has received new input data from the Master and returned new output to the Master. And because of this the data reaches the master almost instantaneously from all the AMUs and thus it applies excellent coordination in data procurement. The figure 3.22 shows the flow of data in the system.

Only the data is samples, it is processed through the pilot protection algorithm to identify a fault and generate a trip signal. This process can be achieved in two ways.

1. Scan Mode 2. FPGA mode

3.9.3 Scan Mode:

The basic programming of the NI CRio is done through the NI Lab view software using the scan engine. It's an interface in Lab view that allows access to the module with default configuration, by using block diagram default algorithm in the program. In this case, the slave modules don't utilize their individual clocks, but only measure or sample data when a command is issued by the master controller.

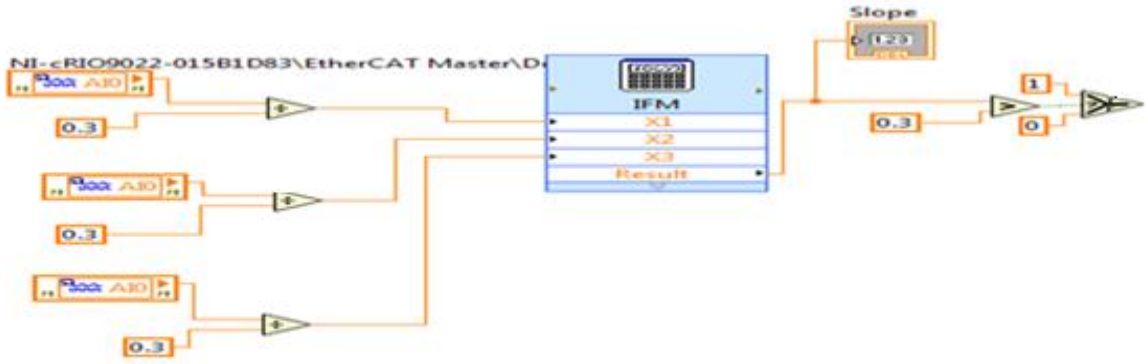


Figure 3.23. Example of the differential protection algorithm in Lab View software [30]

3.9.4 FPGA mode:

This mode also called the Field Programmable Gate Array modeling can direct the NI 9215s to sample current on their own. In this method, the current is sampled autonomously without any interference from the master controller. The master controller only accesses these samples at a fixed frequency. FPGA allows for higher sampling frequencies and hence results in faster trip time detection and generation. The samples once acquired, are processed in the micro controller based on the protection algorithm.

3.9.5 Timer and counter:

In this case the system has a timer and a counter. The system resets to its default state as soon as the timer expires. This prevents the system from tripping when there is no genuine fault. The performance of the system also largely depends on the counter in place. Whenever the sample values are such that it crosses the threshold of 0.3, the counter value is increased by 1. When the counter value exceeds 10, a trip signal is generated. So basically when a fault is generated in the system, it takes 10 samples to confirm it and then generates a trip. The timer is reset after every 20 cycles and clears the counter.

3.9.6 Protection algorithm:

The NI CRio collects the data from the 3 CTs using the 3 AMUs (NI 9144+NI 9215). These samples are then evaluated in the IFM algorithm which applies the following formula:

$$\frac{abs(X1 + X2 + X3) - .1}{abs(X1) + abs(X2) + abs(X3)} \quad (3.8)$$

Here X1, X2 and X3 are analog output of the modules.

3.9.7 Over current protection:

This is the backup protection for the system and acts when the primary protection fails to act/operate. The samples are taken into processing and based on a fixed value above which if 20 samples are recorded in that case a trip signal is generated.

Now the time are counter together help prevent unnecessary trips. The timer runs for 20 loops and resets the program counter and the counter gain counts from 0. Now even if the counter is incremented by a transient, the counter will be reset after 20 cycles. So a trip due to transient action is avoided.

3.9.8 Timed Loop:

The whole structure is enclosed within a loop called Timed Loop. This is a while loop that can be stopped on pressing the stop button. Now the loop period (the time it takes for the loop to go from one iteration to next) is synchronized to scan engine. With the default FPGA coding, the fastest the scan engine can go is 1KHz. So the timed loop executes the code placed inside it ones every 1 milli second. The frequency of sample acquisition can be increased to a maximum of 3.3kHz by altering the FPGA bitfile at NI 9144. This

maximum is limited by the 'NI Industrial Communication for EtherCAT' configuration [30].

3.9.9 Averaging window concept implementation on the NI CRio:

The slope is determined after obtaining a sample from the 3 AMUs. Now 10 such readings are taken and averaged. If the average is greater than 0.3, the trip signal is generated, if there is no trip generated, in that case the first reading out of the 10 is discarded and included the lastest sample and then calculates the average. The result from the IFM block is then passed to the next loop iteration and finds the average of the 10 samples. Initially it takes 10 samples to fill the window, after that window it takes in a new reading for every iteration and finds the average of the 10 samples. The result is then compared with $S_0 = 0.3$, if it is greater than a trip signal is generated and if not the window moves by one reading. Similarly for the O.C backup protection 20 sample window is created and averaged and then the current sample is compared to a prefixed value and if the average value of the window is greater than a trip is initiated, otherwise the rolling window concept continues.

3.9.10 Need for Rolling Window in the real time simulation:

In the timer and counter algorithm, there might be an event when the timer could reset the counter even when there is a fault and the counter is counting. In this case the time taken to detect a fault could be longer than usual cases. Because of the reset of the counter after fixed intervals, the trip timings are not constant and hence the experiment yielded varying results with no apparent reason.

Now based on the same test bed mentioned before in the earlier section, the NI CRio and its AMU's are connected to the system as shown in figure 36. The following algorithms are implemented on the Ni CRio and test results for these are shown in a later section.

3.10 Results

The performance of the system is different for the two different algorithms that is scan mode and FPGA mode. The rolling window algorithm is clearly faster than the algorithm where a counter and a timer are used.

3.11 Scan Mode [30]

The system was initially programmed to work in Scan Mode. The two algorithms were tested and compared in terms of delay times. The faster algorithm is then implemented using the FPGA mode.

1. **With a Timer and Counter [30]**

Numerous readings were taken correctly evaluate the system's working. Table 7 shows these readings with the time it takes for the trip signal to be generated after a fault at a particular phase angle is generated.

Table 3.7. Delay for various positions of fault [30]

Phase angle at which fault was generated(degrees)	Delay (ms)
19.33	9.895
36.51860744	10.28
38.67947179	8.645
42.14	10.405
53.59	10.625
65.90636255	10.665

66.99	8.635
72.38895558	14.385
79.51980792	13.785
81.9	10.175
88.6	9.65
91.08043217	9.525
93.35	15.98
95.94237695	11.275
112.36	14.445
126.19	16.405
160.3361345	9.105
162.4969988	9.33
193.8295318	15.69
199.23	9.422
200.2	14.76
202.47	14.275
207.0108043	10.11
208.9555822	13.285
230.46	9.14
237.8	14.135
249.36	8.5
251.5246098	10.7
264.7058824	16.675
274.2136855	9.615
284.66	11.01
292.69	13.855
300.2521008	9.4
301.12	10.025
302.6290516	9.36
313.54	11.145
320.13	9.75
326.94	9.695
327.4789916	10.665
330.5	16.215
335.2581032	19.35

340.120048	9.215

From the above data, the following results have been calculated.

Mean=11.65 ms

Standard Deviation=2.79

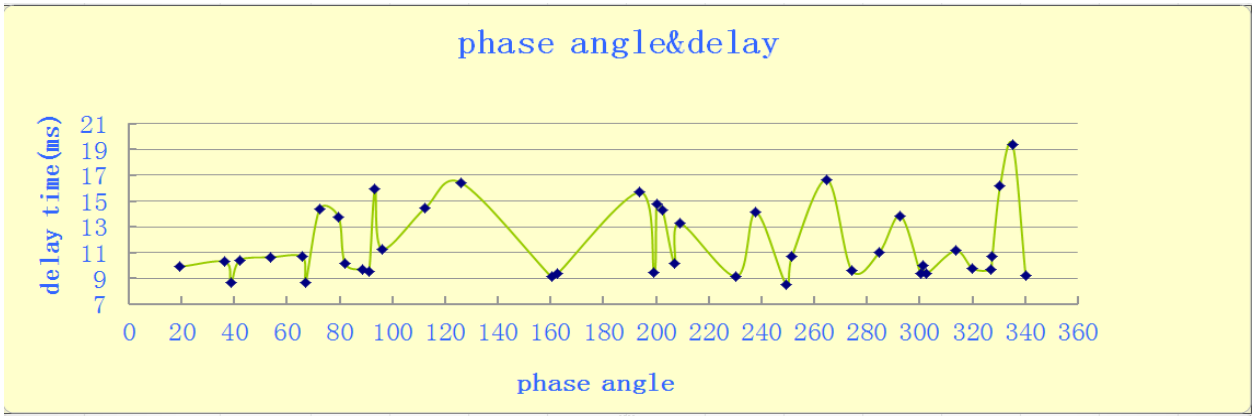


Figure 3.24. Delay vs phase angle graphical representation [30]

From the observations, a comparative graph is plotted as shown. As seen from the graph and the observations, there are some random peaks, i.e. there is too much delay at some points. A possible reason for this may be the reset algorithm applied in the program. The reset might have set in at the same time as the counter reached around 9. So it took almost twice the time to generate the trip signal.

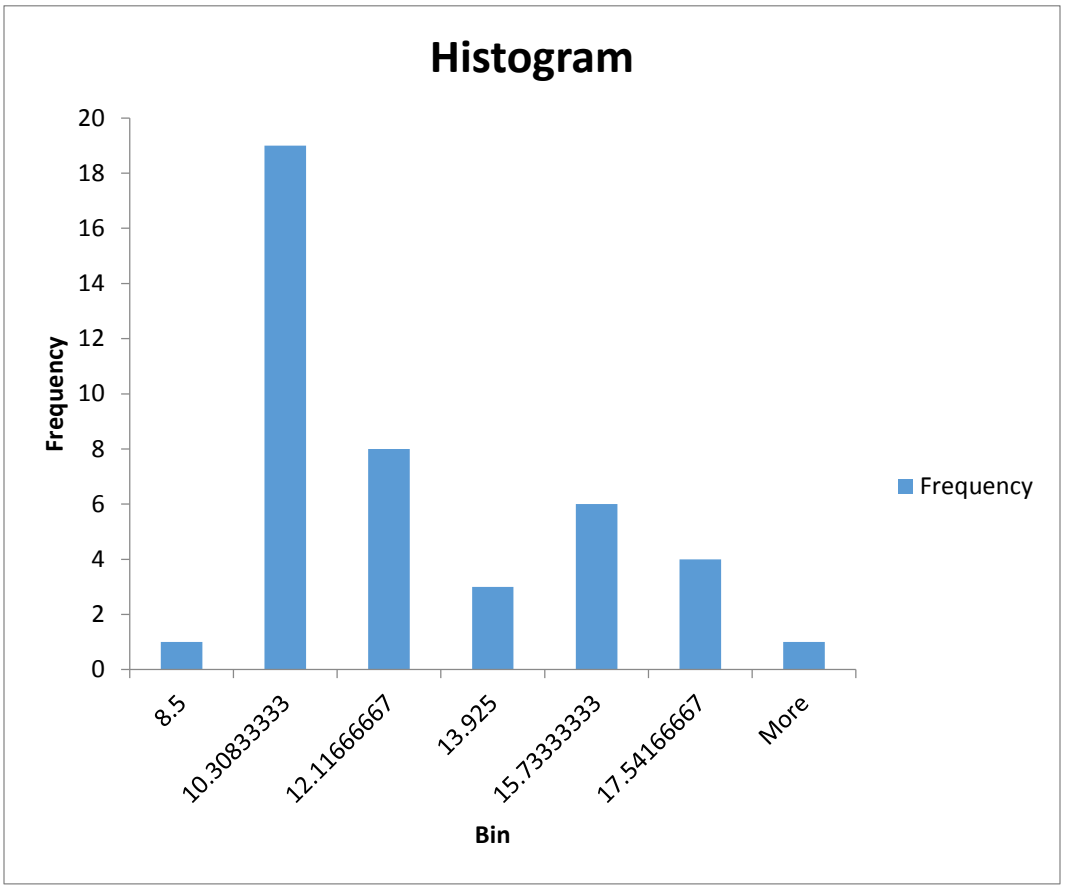


Figure 3.25 Histogram data for trip delay times for the timer and counter method

This chart shows the value of the trip timings to lie between 10.31 ms and 12.12 ms are extremely high which also match with the standard deviation and mean values suggested above

2. With an averaging window

Similar to the timer and counter algorithm, numerous readings were also taken for the averaging window algorithm.

Window with 10 samples: Table 8 shows these readings with the time it takes for the trip signal to be generated after a fault at a particular phase angle is generated.

Table 3.8. Delay for various positions of fault [30]

Phase angle at which fault was generated(degrees)	Delay (ms)
0	7.672
18.2736739	8.004
10.1520401	5.972
11.9232479	6.446
20.9520831	7.648
26.7409066	6.218
33.0049322	7.446
45.9649836	6.74
57.5858304	6.212
72.6194908	6.808
73.6994948	7.134
92.5347704	7.318
97.4163897	8.084
100.267601	5.592
102.902816	6.884
108.130035	5.66
112.666057	5.812
114.804452	5.79
115.560462	5.936
119.491678	8.148
124.978099	7.334
126.576503	6.866
139.234159	5.92
212.486529	7.22
214.387335	6.092

216.331343	6.556
223.588974	6.666
224.107374	6.42
226.526581	6.288
249.552272	6.714
262.253129	6.042
267.134785	5.572
272.145966	5.002
281.952408	7.094
297.418067	6.256
299.491678	5.952
306.965379	7.68
310.637325	7.032
317.765351	7.204
326.923787	6.312
329.818193	6.144
331.762207	6.266
335.607024	4.61
340.445448	7.234

From the above data, the following results have been calculated.

Mean=6.6 ms

Standard Deviation=0.80

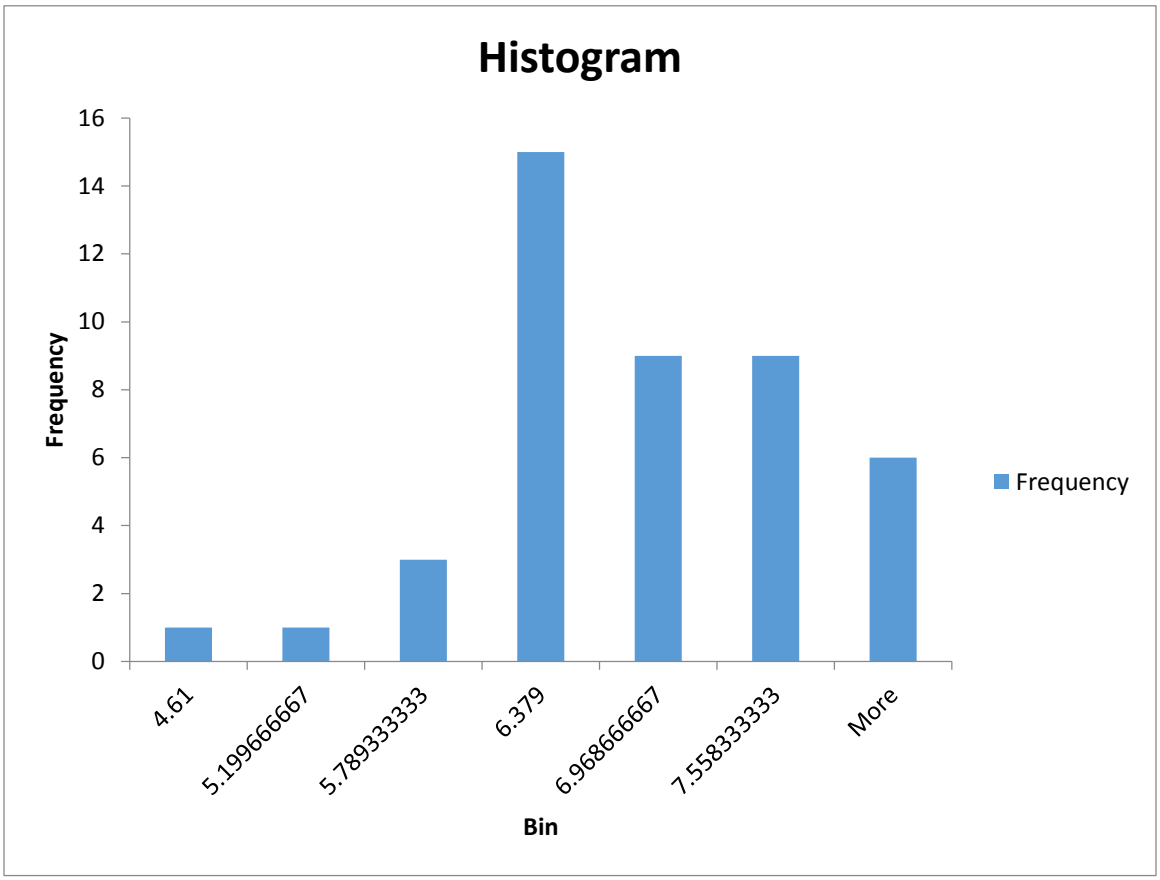


Figure 3.26 Histogram data for trip delay times for the 10 sample rolling window method

This chart shows the value of the trip timings to lie between 6.38 ms and 6.97 ms are extremely high which also match with the standard deviation and mean values suggested above.

3.12 Comparative Study of the two algorithms

As seen from the results in sections before, the averaging window algorithm is much faster than the other one. The average time it takes for a trip signal to generate once a fault is there in the system is 6.59 ms, which is 5.05 ms lesser than the timer and counter algorithm.

Also the standard deviation of the averaging window algorithm is .80 compared to 2.79 of the other algorithm. So we can conclude that the averaging window algorithm is faster and more reliable compared to other.

3.13 FPGA Mode

Clearly, as the results from the Rolling Window algorithm are much better than the Timer and Counter algorithm, it is implemented in the FPGA more. The samples are collected at the slave at 10kHz. These samples are accessed by the master microcontroller at 3.33kHz. Following are the results obtained for a 10 sample window.

Window with 10 samples: Table 9 shows the readings for the time it takes for the trip signal to be generated after a fault has occurred. The table consists of a series of tests and the trip timings for 40 such consecutive test are shown below.

Table 3.9: Time taken for trip signal generation [30]

S.No.	Delay
1	3.88
2	3.376
3	3.626
4	3.986
5	5.54
6	4.526
7	3.854
8	4.694
9	4.404
10	3.726
11	3.002

12	3.288
13	3.442
14	3.73
15	3.904
16	3.304
17	3.276
18	4.424
19	3.912
20	3.426
21	3.608
22	3.954
23	4.544
24	3.844
25	3.574
26	3.088
27	3.422
28	3.006
29	2.996
30	3.606
31	3.248
32	3.736
33	3.75
34	4.462
35	4.466
36	3.628
37	3.346

38	4.38
39	3.29
40	3.886

From the above data, the following results have been calculated.

Mean= 3.78 ms

Standard Deviation= 0.55

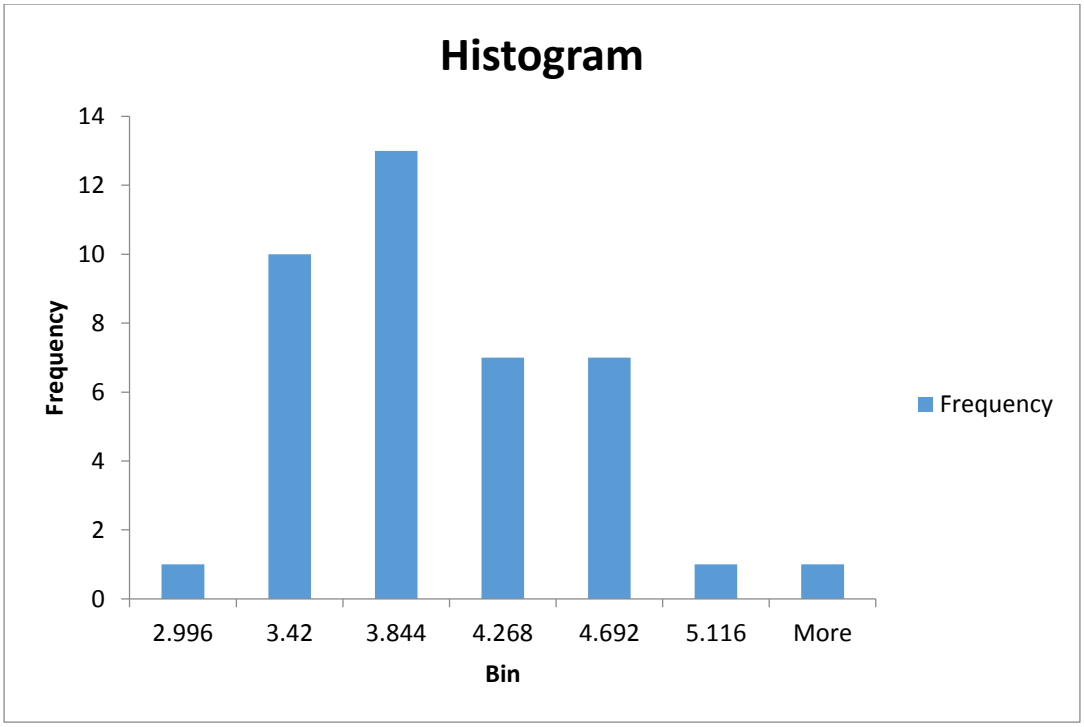


Figure 3.27 Histogram data for trip delay times for the 10 sample rolling window method is shown for the FPGA method

This chart shows the value of the trip timings to lie between 3.42 ms and 3.84 ms are extremely high which also match with the standard deviation and mean values suggested above.

3.14 Conclusion:

Based on the results shown in this section for the hardware and the results shown for the software in the previous section, when similar test bed was simulated in PSCAD and hardware simulations performed. The results show that both hardware and software simulation results match and hence prove that the pilot protection algorithm and the entire setup can be used in real world applications.

CHAPTER 4

MULTI SLOPE DIFFERENTIAL PROTECTION AND CT SATURATION EFFECT ON THE PILOT PROTECTION SYSTEM

4.1 Multi slope differential protection or point form differential protection

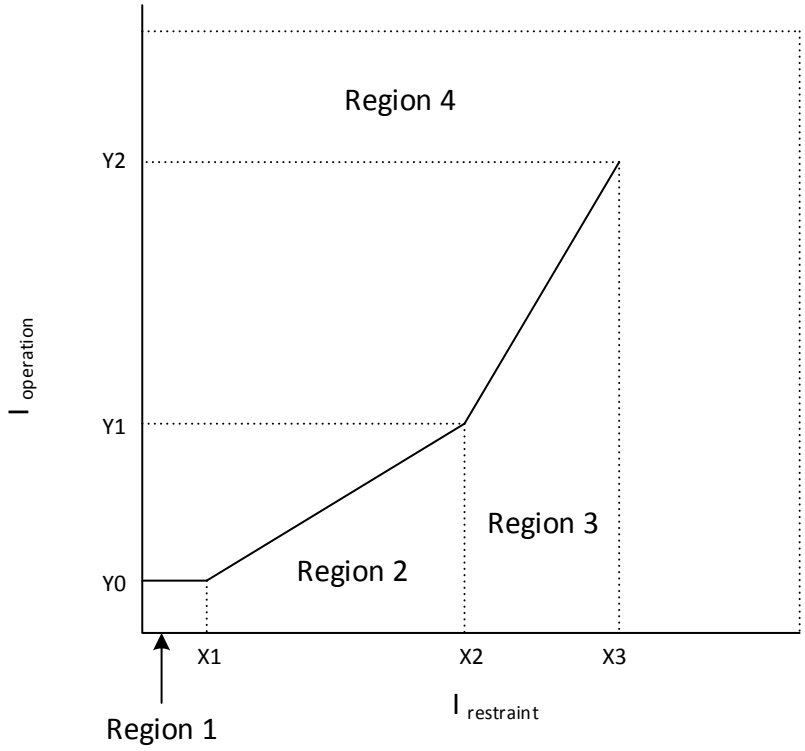


Figure 4.1. Multi slope differential protection characteristic curve

Percentage restrained differential protection is one of the forbearer in forms of flexible protection algorithms. The slope characteristic provides high sensitivity when low currents are flowing in the zone of protection but has lesser sensitivity when high amounts of current are flowing , when false differential current due to current transformer (CT) saturation is more likely [31] [32] [33].Hence this is traditionally used to counter problems like CT saturation, inrush current etc.

The slope characteristic settings must incorporate transient differential current from CT saturation. The percentage restraint characteristic that declares whether the operate-versus-restraint ratio is in the restraining region or the tripping region influences the settings. Small minimal pickup current and minuscule slope ratios are advantageous to distinguish partial winding faults in transformers conducive to trip before the fault increases and creates more large scale damage and loss. This is based on the paper in [33]

This section talks about a new algorithm which was developed. In order to determine a trip, the actual use of coordinates in the (x, y) graph of $I_{op}\ vs\ I_{res}$, instead of the slope. This new dual slope approach as explained above has its own advantages and the explanation of the algorithm is given below.

In this as shown in figure 4.1 above, the $I_{op}\ vs\ I_{res}$ graph is plotted. The graph is divided into 4 regions/zones as shown in the graph. If for that region/zone the (x, y) coordinate is registered in the operation field, a trip is generated, and if it's registered in the restraint field then no trip is generated. The description of all the four regions/zones is given below.

Region 1:

For all the regions certain parameters are assumed like $X_2, X_3, Y_0, slope1\ and\ slope2$ where

$$X_2 = Y_0\ , X_3 = 2.X_2, slope1 = 0.25, slope2 = 0 \ldots . (4.1)$$

$$X_1\ is\ calculated\ using\ the\ following\ formula$$

$$X_1 = {}^{Y_0}/_{slope1} \qquad (4.2)$$

Hence for Region 1 if the following conditions are met, then R1 will go high

$$I_{op} > Y_0 \; and \; I_{res} > X_1 \; holds \; true \; then \; R1 \; will \; become \; high \qquad (4.3)$$

Region 2:

For Region 2 i.e. with slope=0.25, the following parameters are to be calculated. Y_1 can be calculated using X_1.

$$Y_1 = Y_0 + slope1.(X_2 - X_1) \qquad (4.4)$$

Hence for Region 2, if the following conditions are met, then R2 will go high

$$I_{res} > X_1 \; and \; I_{res} > X_2 \; and \; I_{op} > (I_{res}.slope1 + (Y_0 - X_1.slope1))$$

$$holds \; true \; then \; R2 \; will \; become \; high \qquad (4.5)$$

Region 3

For Region 3 i.e. with slope=0.6, the following parameters are to be calculated. Y_2 can be calculated using $X_2, X_3, slope2 \; and \; Y_1$.

$$Y_2 = Y_1 + slope2.(X_3 - X_2) \qquad (4.6)$$

Hence for Region 3, if the following conditions are met, then R3 will go high

$$I_{res} > X_2 \; and \; I_{res} > X_3 \; and \; I_{op} > (I_{res}.slope2 + (Y_1 - X_2.slope2))$$

$$holds \; true \; then \; R3 \; will \; become \; high \qquad (4.7)$$

Region 4:

Rest of the operation region is set as region 4.

Hence for Region 4, if the following conditions are met, then R4 will go high

$$I_{op} > Y_2 \qquad (4.8)$$

The trip signal is an OR output of R1, R2, R3 and R4 signal bits. If any one of them or multiple bits go high in that case a trip is detected as shown in the figure below. Here in this case both I_{op} and I_{res} are calculated by using the 10 sample average method i.e. the 10 sample averages of both I_{op} and I_{res} are used in the calculation for the (x,y) coordinates and also whether the bits of R1, R2, R3 and R4 are high or not. Here also I_{op} is the vector sum of currents while I_{res} is the absolute magnitude sum of currents in that zone. Below shown is the PSCAD modelling of the algorithm.

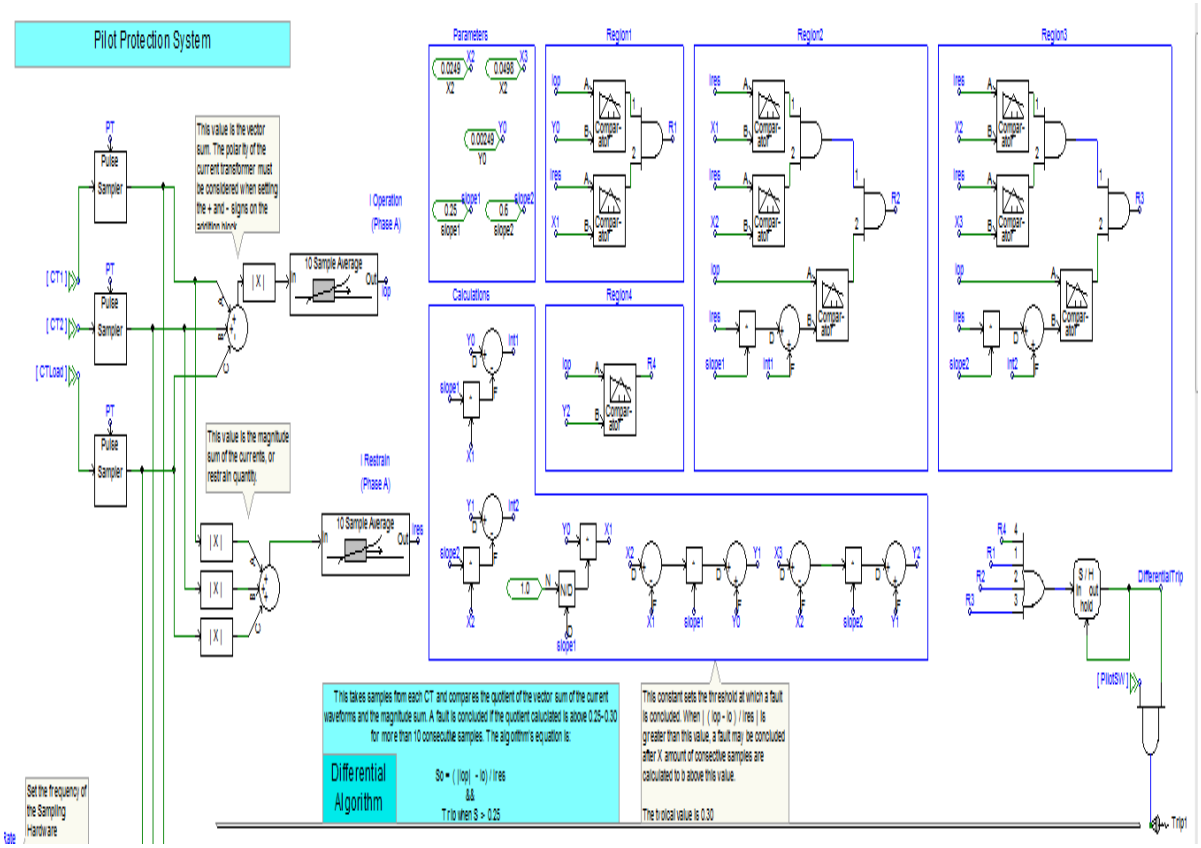


Figure 4.2. Algorithm for the multi slope differential characteristic in PSCAD

The following algorithm was tested in same test bed mentioned in the previous sections in PSCAD. The test bed details the fault current, trip timing figures, $I_{operation}$, $I_{restraint}$ graphs, and the graphs for the bits R1, R2 , R3 and R4 are shown below. The fault analysis was done to determine the trip timings for each fault occurring at intervals of 0.001 sec over 1 cycle period. The results for both the dual slope method and the previously described 10 sample average slope differential algorithm results are shown for comparison.

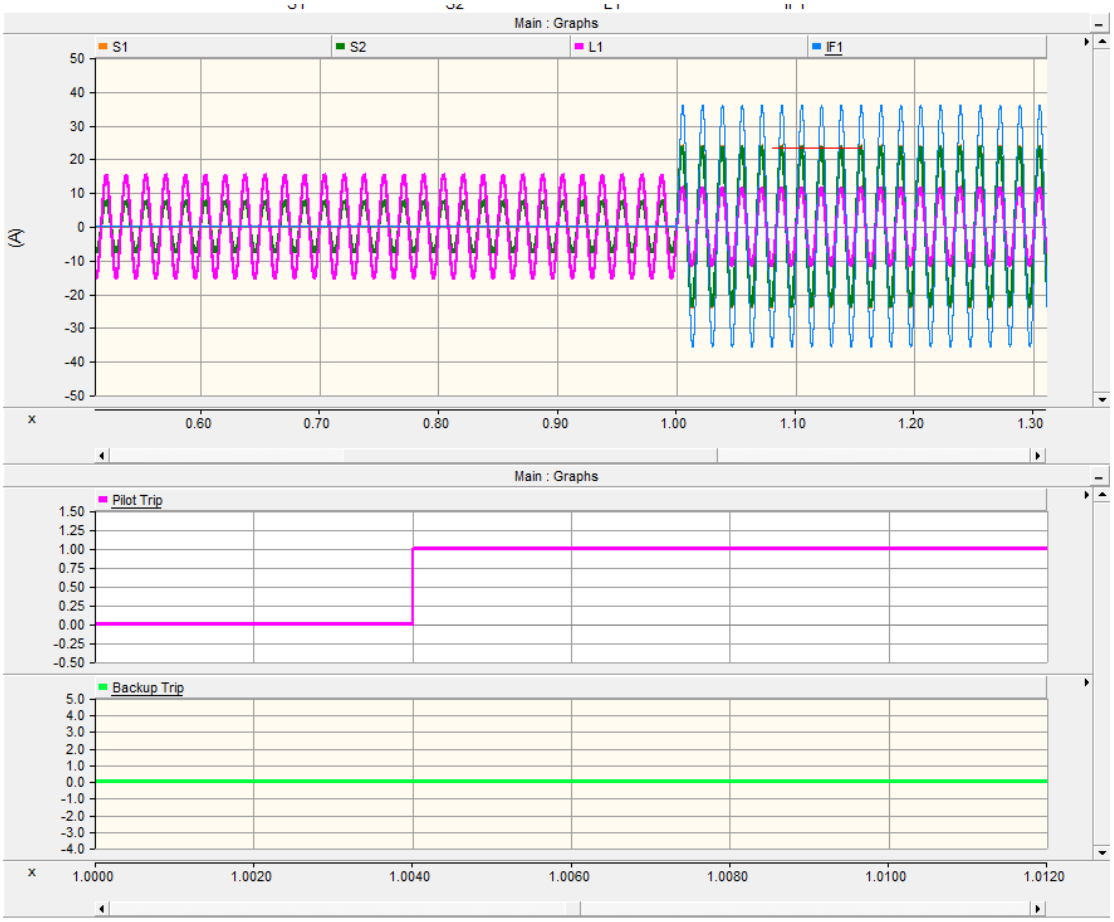


Figure 4.3. S1, S2 are the source currents while L1, IF1 are the source and fault current respectively. The trip timings for the dual slope pilot differential trip is shown in the figure for fault at t=1 sec.

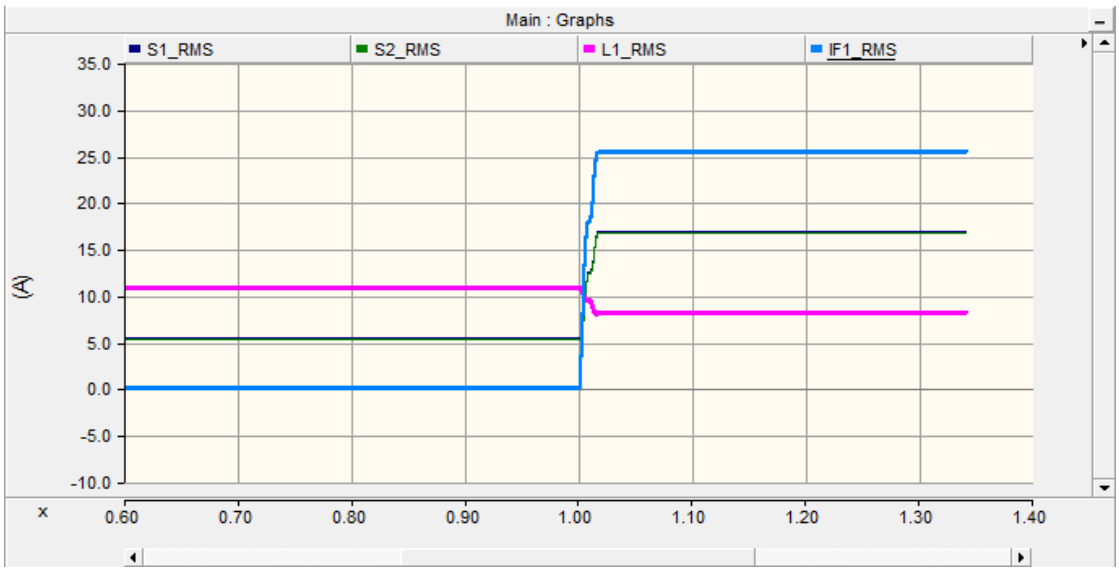


Figure 4.4. S1_RMS, S2_RMS are the source RMS currents while L1_RMS, IF1_RMS are the source and fault RMS currents respectively.

Figure 4.5. Digital bits R1, R2, R3 and R4 are shown going high after fault at t=1sec.

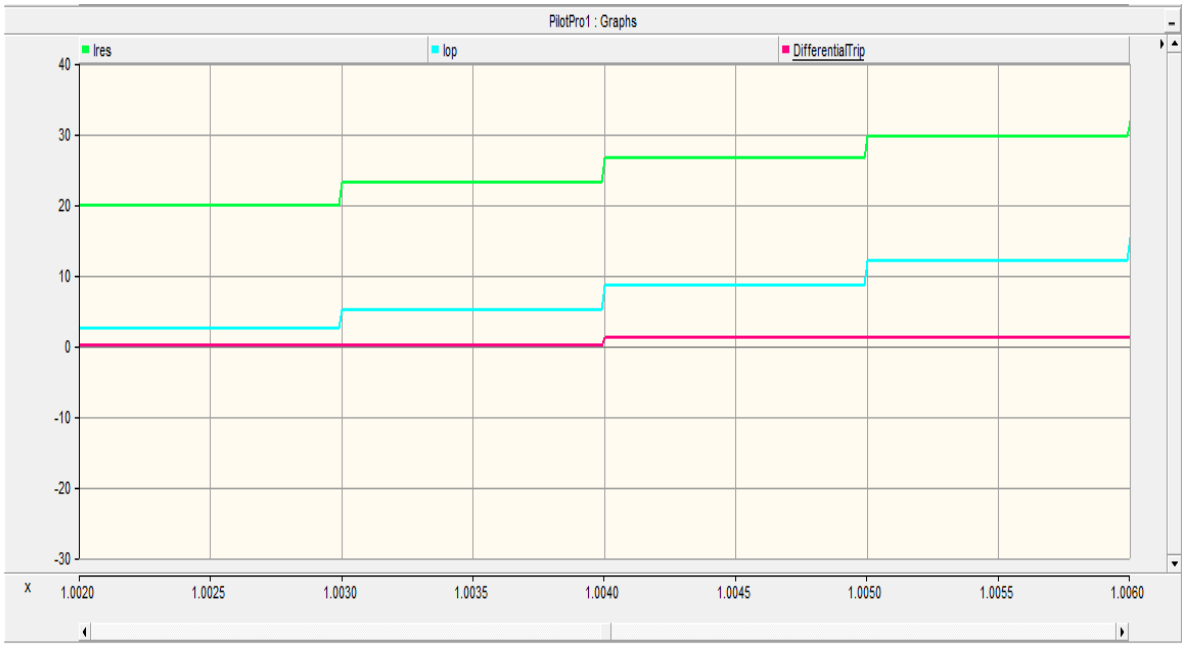


Figure 4.6. This shows the $I_{operation}$, $I_{restraint}$ calculation on graph and differential trip signal at fault at t=1 sec

4.2 Results for dual slope method:

Table 4.1. Statistical Summary of the dual slope method based on 17 Runs.

Tfault represents the fault timing, T_trip represents the trip signal response and the delay table is the timing difference between the two.

Run #	Tfault (sec)	T_trip (sec)	Delay(ms)
1	1.000000000	1.004010000	4.010000000
2	1.001000000	1.005010000	4.010000000
3	1.002000000	1.005010000	3.010000000
4	1.003000000	1.006010000	3.010000000

5	1.004000000	1.007010000	3.010000000
6	1.005000000	1.010010000	5.010000000
7	1.006000000	1.012010000	6.010000000
8	1.007000000	1.012010000	5.010000000
9	1.008000000	1.013010000	5.010000000
10	1.009000000	1.013010000	4.010000000
11	1.010000000	1.013010000	3.010000000
12	1.011000000	1.014010000	3.010000000
13	1.012000000	1.015010000	3.010000000
14	1.013000000	1.017010000	4.010000000
15	1.014000000	1.020010000	6.010000000
16	1.015000000	1.021010000	6.010000000
17	1.016000000	1.021010000	5.010000000

Mean for trip time signal: 4.25 ms

Standard Dev for each trip time: 1.15 ms

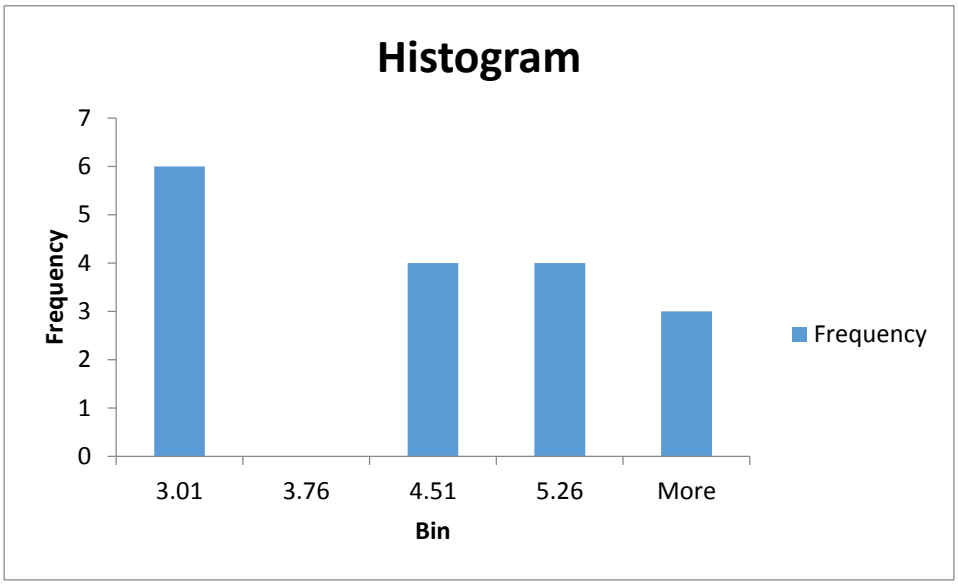


Figure 4.7 Histogram for trip timing delay for the dual slope method.

This chart shows that most of the trip delay timings lie between 0 and 3.01 ms , but as the peak is not very high compared to other ranges, the mean and standard deviation in this case are different.

4.3 Results for the same test using the percentage differential slope with 10 sample rolling window

The same test was conducted on the same test bed for the algorithm for the same sampling frequency i.e. f=1 kHz mentioned in the previous section. The results for that test are displayed in the bottle below.

Table 4.2. Statistical Summary of the dual slope method based on 17 Runs. Tfault represents the fault timing, T_trip represents the trip signal response and the delay table is the timing difference between the two.

Run #	Tfault	T_trip	Delay(ms)
1	1.000000000	1.007010000	7.010000000

2	1.001000000	1.008010000	7.010000000
3	1.002000000	1.010010000	8.010000000
4	1.003000000	1.011010000	8.010000000
5	1.004000000	1.012010000	8.010000000
6	1.005000000	1.013010000	8.010000000
7	1.006000000	1.014010000	8.010000000
8	1.007000000	1.014010000	7.010000000
9	1.008000000	1.015010000	7.010000000
10	1.009000000	1.016010000	7.010000000
11	1.010000000	1.017010000	7.010000000
12	1.011000000	1.018010000	7.010000000
13	1.012000000	1.019010000	7.010000000
14	1.013000000	1.020010000	7.010000000
15	1.014000000	1.021010000	7.010000000
16	1.015000000	1.022010000	7.010000000
17	1.016000000	1.024010000	8.010000000

Mean delay time: 7.36 ms

Standard Dev for delay time: 0.49 ms

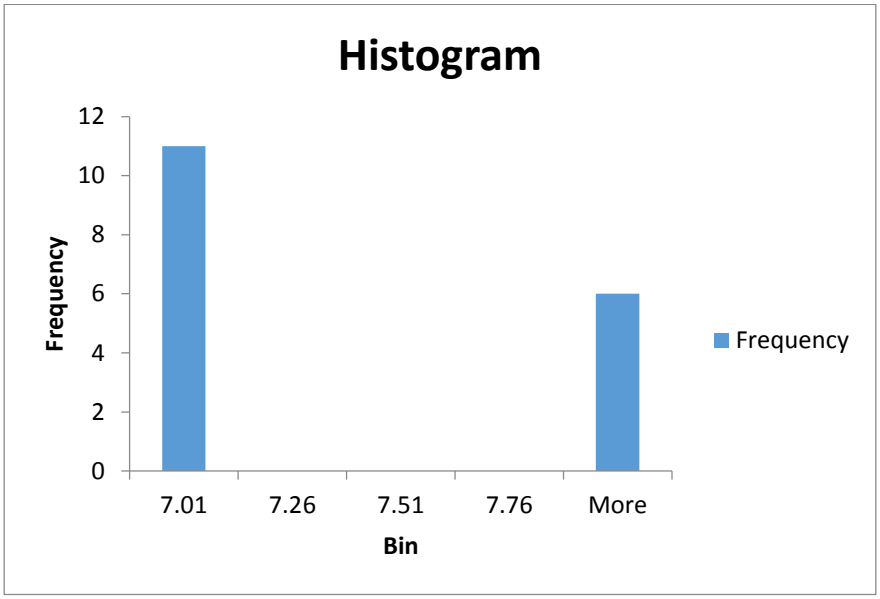


Figure 4.8 Histogram for trip timing delay for previous 10 sample rolling window method

This chart shows that most of the trip delay timings lie between 0 and 7.01 ms. This values tally with average mean and standard deviation in this case.

Based on the results shown here the mean delay time for the dual slope method is lesser but the standard deviation as double compared to the older method for the same sampling frequency. The results show that even though it's faster, but reliability may still be a concern.

4.4 CT saturation phenomenon and the performance of the percentage slope differential protection with 10 sample window average module

What is CT saturation ?

CT saturation is described as the phenomenon where in the CT is no longer able emulate secondary current proportional to the primary current (according to its own ratio). The CT can saturate because of either very high primary current or open circuit in secondary/high

burden at secondary. CT saturation ca take place even when the ratings are not properly matched. The ratio has to be matched is such a manner that the maximum fault current to the rated current should be less than 20 [6]. Also the (X/R) ratio should be known for calculating the DC component in the fault current and the time delay. If the time constant is small, saturation will take place in the first few moments. Sometimes CT saturation can even take place due to the lead wire resistance can add to the CT burden and thereby cause CT saturation. The CT saturation is mainly dependent on two component that is the AC saturation component and DC offset component [6] [34]

4.4.1 Saturation of CT due to DC offset

This is usually a function of the power system and very little in the practical sense can be done to avoid its effect by CT design [6]. The output of the CT will be shown in the figure for different levels of saturation.

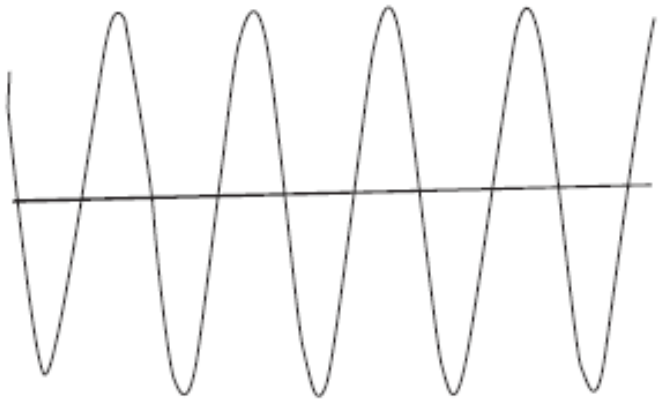


Figure 4.9. CT output with no saturation [6]

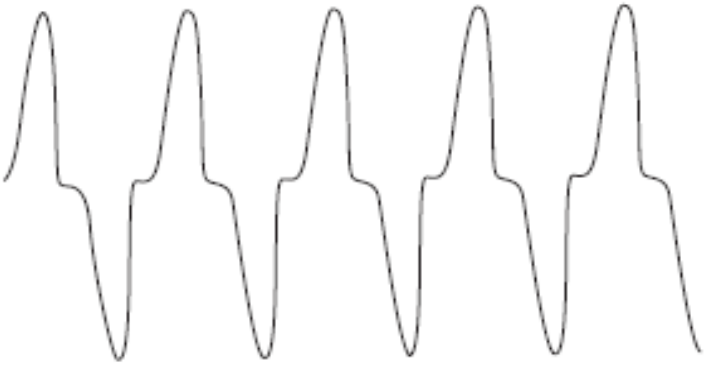


Figure 4.10. CT output with part saturation [6]

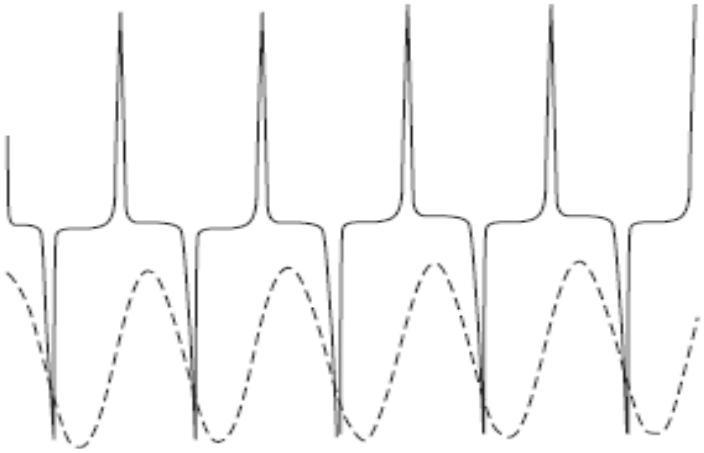


Figure 4.11. CT output with severe saturation [6]

The effect of saturation for differential protection can be extremely critical. In most cases DC saturation may not likely be too large, but it should be kept in check. In many cases the high speed relay will act before the DC CT saturation will take place. If the saturation does take place a delay is given until the CT recovers to permit adequate operation. So in these cases, there is a tendency to under reach for a very short period of time. One of the problems with differential protection is that for an external fault, the differential trip should not operate. But for a large enough fault, the CT gets saturated and the protection system gets

affected by it. As compared in over current protection somewhat level of saturation is allowed, and results show based on data in [32] that CT saturation will not greatly delay overcurrent protection for better settings.

4.4.2 Explanation of the CT saturation

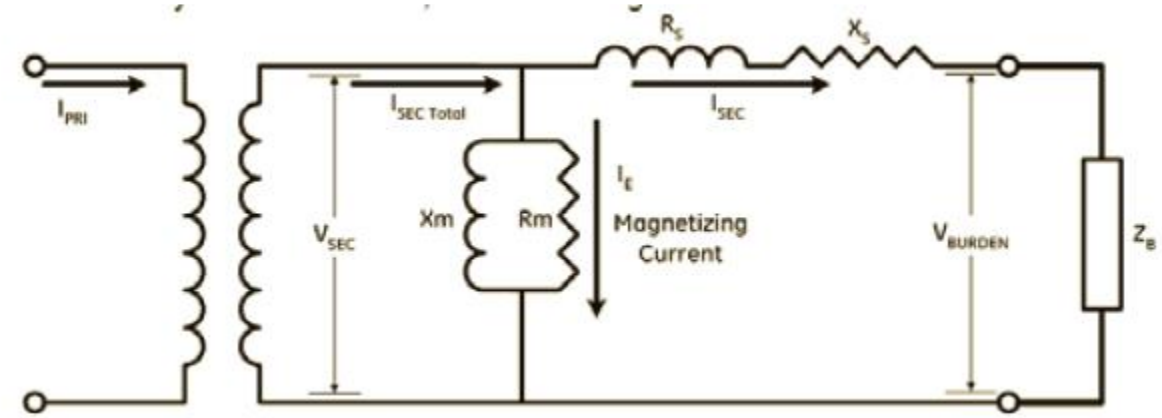


Figure 4.12. CT primary and secondary winding [32]

Shown in the figure 4.10 above is the secondary side of a current transformer. The current transformer saturation takes place due to the voltage drop across the burden and also the DC component in the fault. When the V_{sec} voltage reached the saturation voltage of the transformer, the high flux will need a high $I_e(excitation\ current)$. This I_e may very well reach $I_{s\ total}$ based on the figure below. Hence very little current goes through the burden/measuring device.

$$I_{s\ total} = I_e + I_s \qquad (4.9)$$

$$but\ during\ saturation \quad I_{s\ total} \cong I_e \qquad (4.10)$$

$$Hence\ I_s \cong 0 \qquad (4.11)$$

The DC offset is created due to the inductive-resistive characteristic of the power system and will cause the CT current saturation at a lower magnitude as compared to a symmetrical waveform [32]. The DC offset causes the poorest performance of the CT. Now as it take time for the DC component to decay (depending on the time constant) it can cause a loss of coordination between upstream and downstream devices. CT size is also very important, now if the fault current is almost 10-1000 times the rated current, in that case for a small core, the CT is bound to be saturated. In many cases the CT after some time might not come out of saturation, and thereby prevent operation of the protection logic.

4.4.3 Test results of CT saturation on PSCAD

The results of different CT ratios for a fixed type of standard CT unit is PSCAD

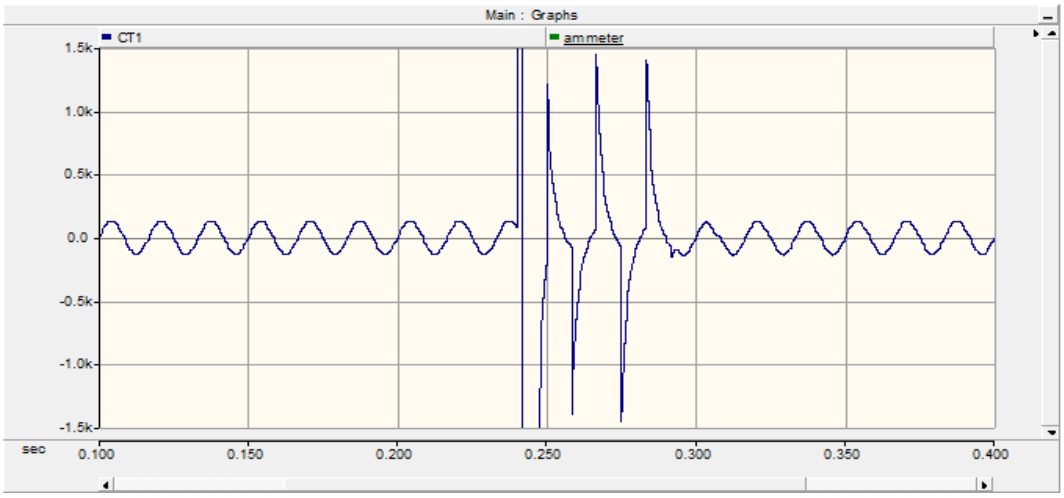


Figure 4.13. CT secondary current for ratio 2:20 for the CT, fault current for a 100kV , 1000 ohm load 1 phase system actual and saturated current reading

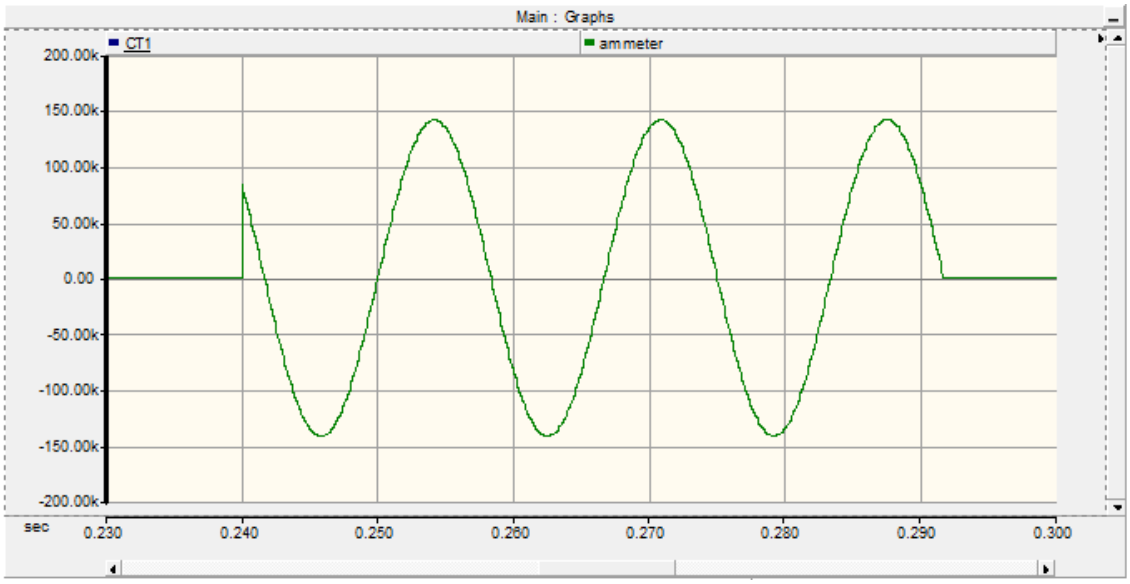


Figure 4.14. Actual circuit current for ratio 2:20 for the CT, fault current for a 100kV , 1000 ohm load 1 phase system actual and saturated current reading

Based on this, the pilot protection module was applied to the test bed mentioned in Chapter 3, and in this case we have utilized the CT standard model that is available in PSCAD. The simulation was conducted for different trip signal delay times for different fault incident angles. Below represented are the currents and trip timing modules. The table below show the results of the trip delay times for various CT ratios. The fault occurs at t=1 sec.

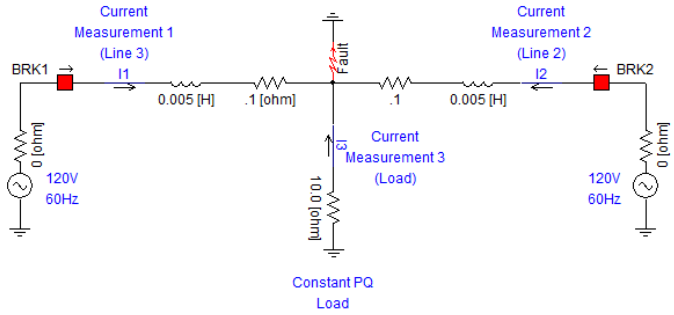


Figure 4.15. Test bed circuit for the CT saturation test for the pilot protection module

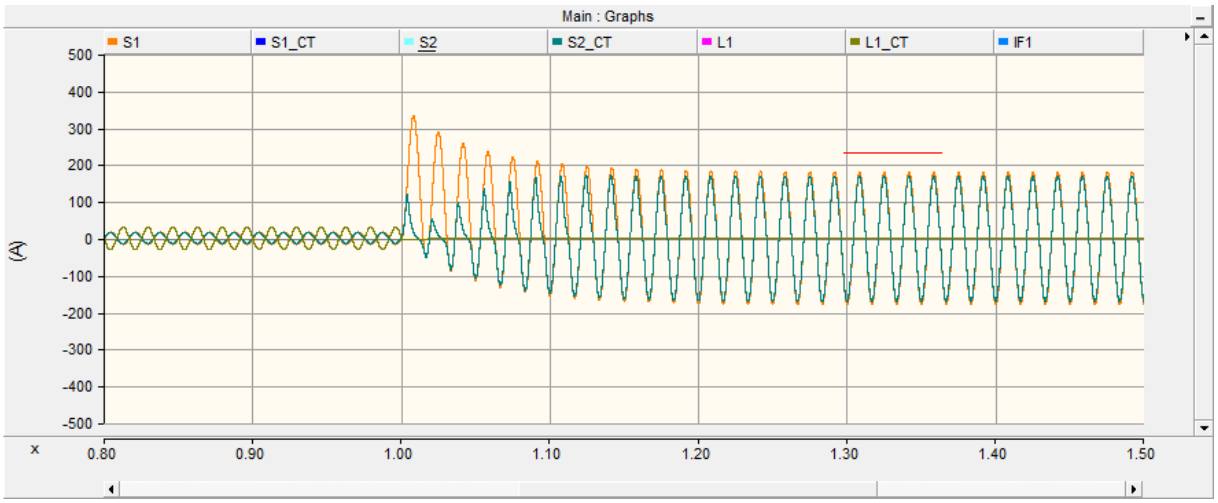


Figure 4.16. S1, S2 and L1 are actual currents on the primary while S1_CT,S2_CT and L1_CT are secondary CT currents referred to primary

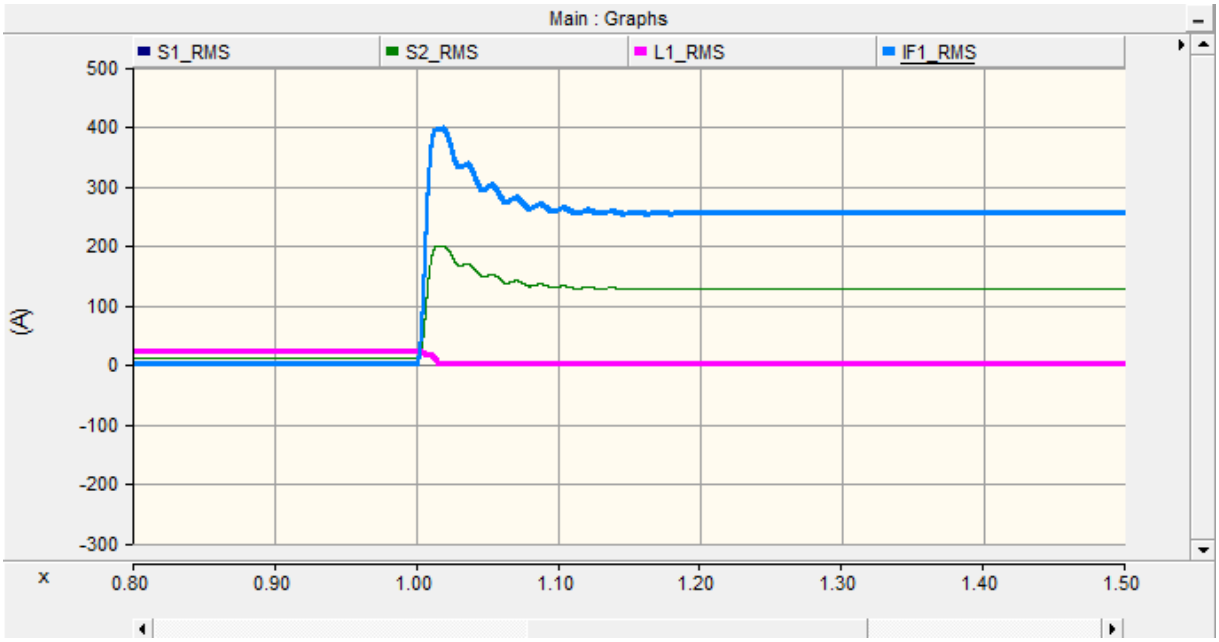


Figure 4.17. Rms currents through the system before and after fault

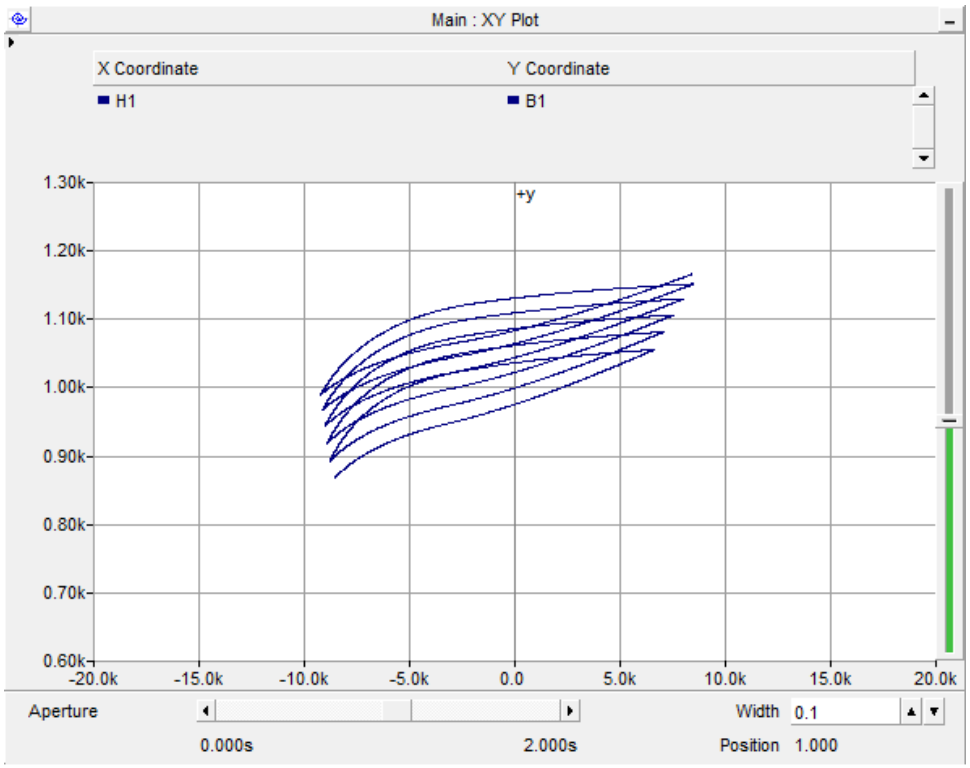


Figure 4.18. BH curve before fault

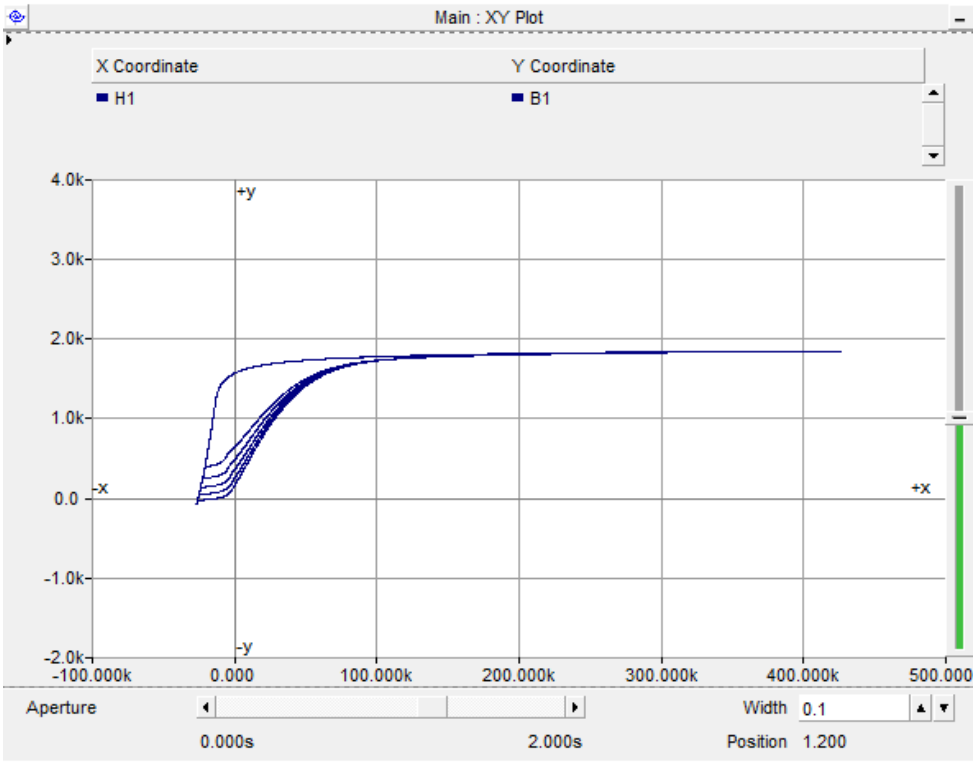


Figure 4.19. BH curve after fault

Below are tabulated results for the trip signal delays for different CT ratios

Table 4.3. The trip signal delay timings for the pilot protection system on the tested circuit for CT ratio 20:2

Run #	Tfault (sec)	T_trip (sec)	Delay(ms)
1	1.000000000	1.000910000	0.9100000000
2	1.001000000	1.001510000	0.5100000000
3	1.002000000	1.002410000	0.4100000000
4	1.003000000	1.003920000	0.9200000000
5	1.004000000	1.004820000	0.8200000000
6	1.005000000	1.006020000	1.020000000
7	1.006000000	1.006620000	0.6200000000
8	1.007000000	1.007820000	0.8200000000
9	1.008000000	1.008720000	0.7200000000
10	1.009000000	1.009620000	0.6200000000
11	1.010000000	1.010520000	0.5200000000
12	1.011000000	1.011720000	0.7200000000
13	1.012000000	1.012620000	0.6200000000
14	1.013000000	1.013820000	0.8200000000
15	1.014000000	1.014720000	0.7200000000
16	1.015000000	1.015620000	0.6200000000
17	1.016000000	1.016820000	0.8200000000

Mean Delay: 0.718 ms

Std Dev in the delay 0.16 ms

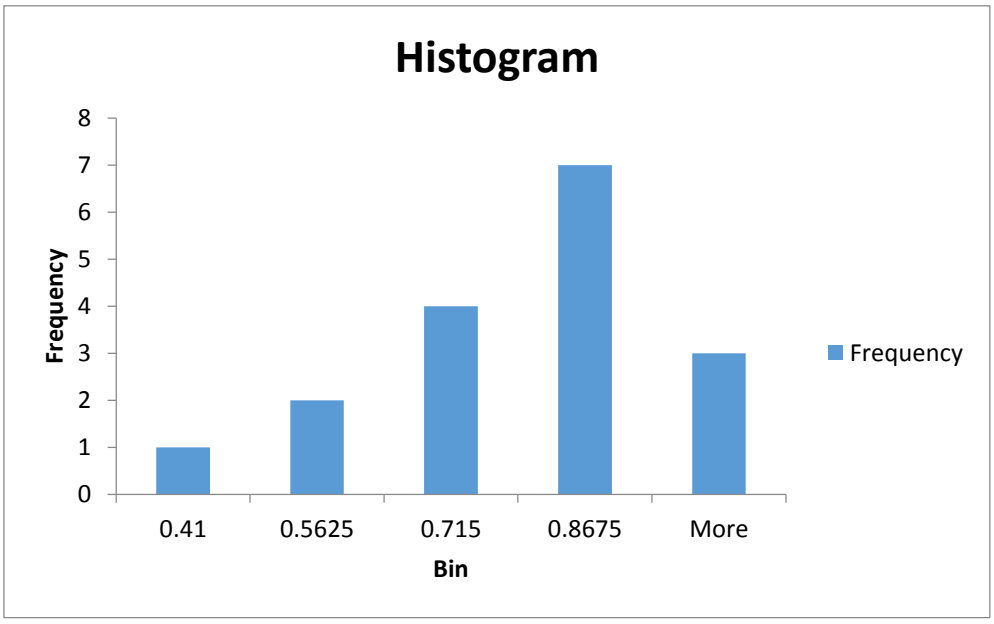


Figure 4.20 Histogram for trip timings for the pilot protection system on the tested circuit for CT ratio 20:2

This chart shows that most of the trip delay timings lie between 0.715 ms and 0.8675 ms.

These values tally with average mean and standard deviation in this case.

Table 4.4. The trip signal delay timings for the pilot protection system on the tested circuit for CT ratio 200: 20

Run #	Tfault (sec)	T_trip (sec)	Delay(ms)
1	1.000000000	1.001220000	1.220000000
2	1.001000000	1.002120000	1.120000000
3	1.002000000	1.003020000	1.020000000
4	1.003000000	1.003920000	0.9200000000
5	1.004000000	1.005120000	1.120000000
6	1.005000000	1.006020000	1.020000000
7	1.006000000	1.006920000	0.9200000000
8	1.007000000	1.008120000	1.120000000
9	1.008000000	1.009020000	1.020000000
10	1.009000000	1.009920000	0.9200000000

11	1.010000000	1.011120000	1.120000000
12	1.011000000	1.012020000	1.020000000
13	1.012000000	1.012920000	0.9200000000
14	1.013000000	1.014120000	1.120000000
15	1.014000000	1.015020000	1.020000000
16	1.015000000	1.015920000	0.9200000000
17	1.016000000	1.017120000	1.120000000

Mean for trip delay timings: 1.04 ms

Std Dev for trip delay timings: 0.095 ms

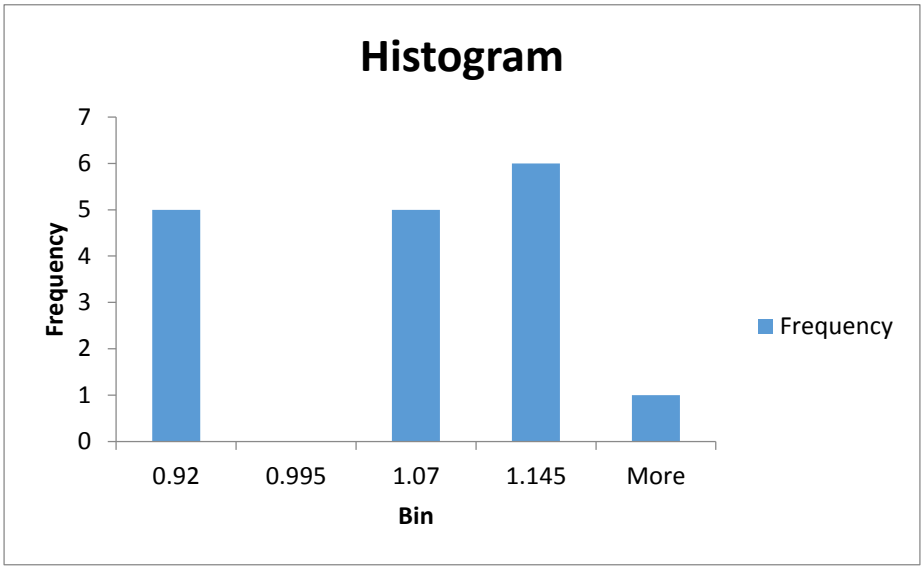


Figure 4.21 Histogram for trip timings for the pilot protection system on the tested circuit for CT ratio 200:20

This chart shows that most of the trip delay timings lie between 0.715 ms and 0.8675 ms.

These values tally with average mean and standard deviation in this case.

The results show that the pilot protection module is successfully able to detect the fault even during saturation for a sampling frequency of 3333 Hz

CHAPTER 5

IMPLEMENTATION OF THE PILOT PROTECTION SYSTEM FOR LARGE DISTRIBUTION SYSTEMS

5.1 Green Hub Model III (modified to get v4.3) [35] [36]

The Green hub model is one of the first models that is primarily used to check the functioning of the pilot protection system. It was developed at NCSU. Here the explanation of the Green hub model function and working of the solid state transformer and the PV system utilized in the model is given

The Green hub is defined as a residential distribution system, in which the household has roof top PV. It is assumed that each PV can produce up to the maximum load of the residential unit. In this case we shall be explaining the Green hub III model in which all the substation and distribution transformers are SSTs and also the system is looped.

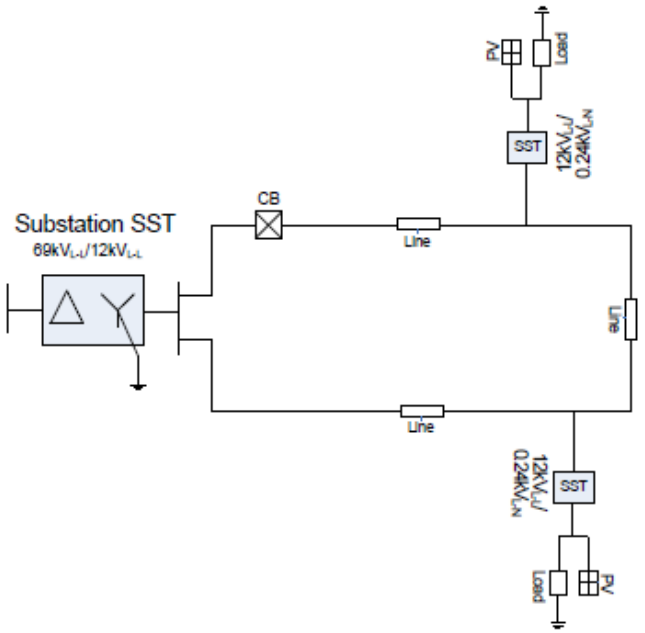


Figure 5.1. Green Hub 3 system diagram [35]

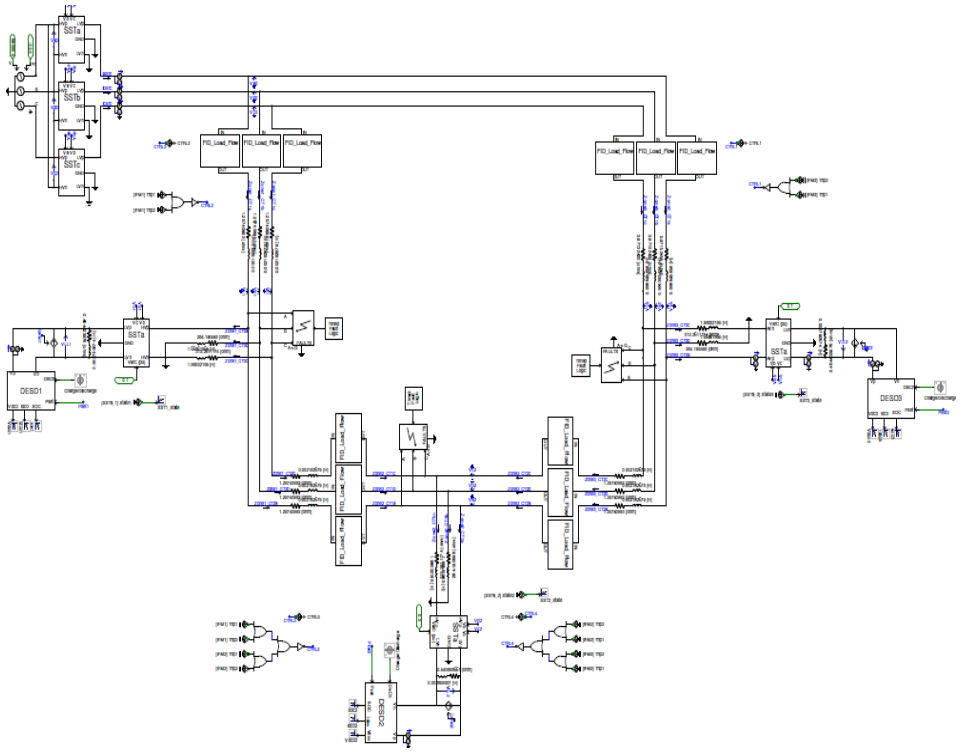


Figure 5.2. Green hub model v4.3 in PSCAD [36]

5.1.1 PV system.

The PV system is developed with a MPPT algorithm and other power electronics to convert the DC power generator the AC power for the grid. This model for the PV has been developed and adopted for the PV model simulated, at Colorado boulder [35]. The main components in this are shown on the figure.

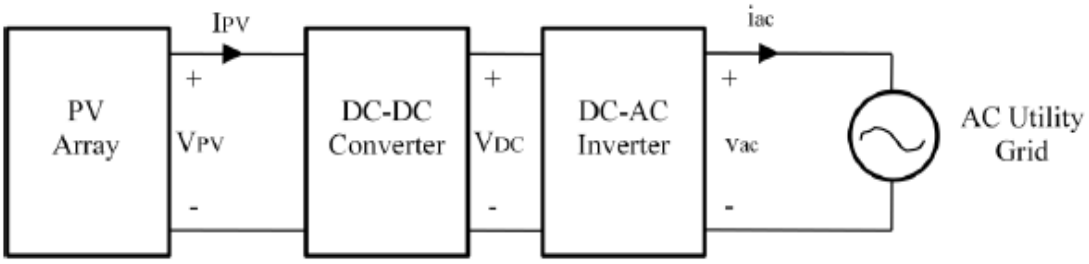


Figure 5.3. Topology of the PV system [35]

The Inverter for the PV has its own d-q control and it can limit the fault current up to two times the rated current. The PV shut down after 0.1 sec is due to the internal under voltage protection scheme.

The V-I characteristics of the PV is also shown below in figure 5.4. For low levels of V, the I is limited to 2pu, as the inverter is operating under the constant current mode, while for higher V the inverter operates under constant power mode.

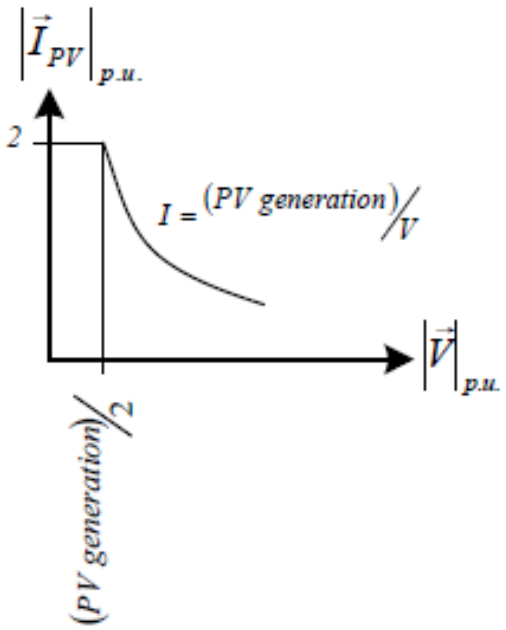


Figure 5.4. VI characteristic curve of the PV [35]

5.1.2 Solid State Transformers

For the involvement of DERs i.e. (Distributed Energy resources) in the distribution system, the FREEDM system center developed a SST. An average model of the SST has been developed for this test case [35]. The SST has its own internal protection which utilizes the DC bus voltage at its input. Hence in case of a fall on the primary/high voltage side of the

SST, it will stay on line, so as to provide active power support to the load. If it cannot provide the active power, voltage on the DC bus drops and the protection system trips and switches off the SST. The main system schematics are shown below.

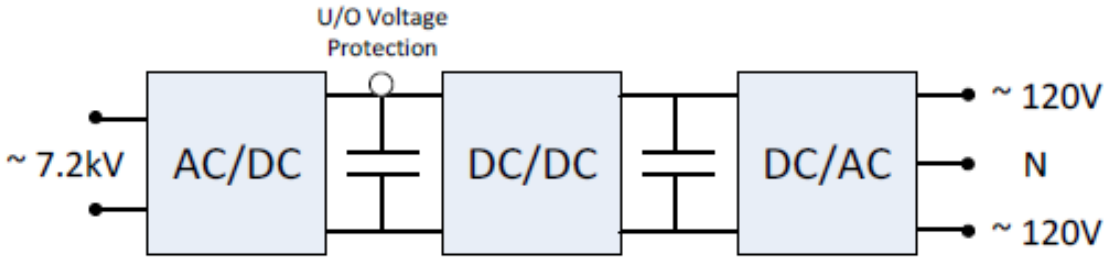


Figure 5.5. Topology of the SST [35]

Here in this case the power stage rectifier controller, inverter controller, the P-Q measurement blocks and the protection block are show in figure 5.5 above.

5.1.3 Results

For the testing of the pilot protection differential scheme we have switched off the internal protection system of the SST. Now as shown in the figure 5.6 we have divided the Green hub model into three zones of protection.

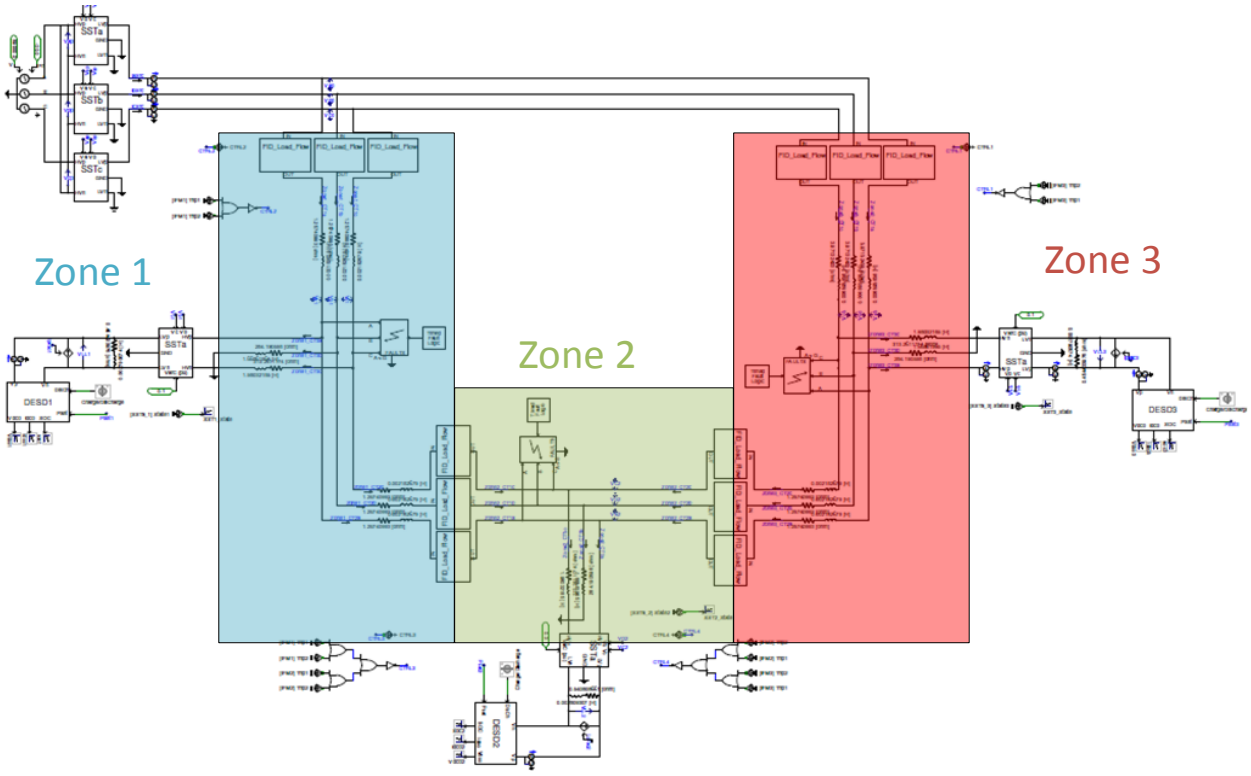


Figure 5.6. Zones of protection in the green hub model for the pilot differential protection system

And for the each zone we have developed a pilot protection model for each phase, as is shown in the figure 5.7.

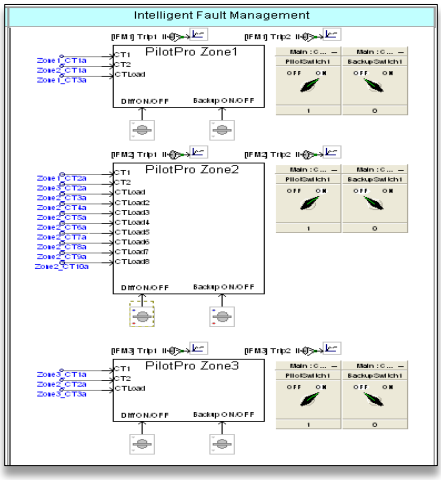


Figure 5.7. Pilot protection module in PSCAD

An investigation into the systems behavior when additional SSTs/Loads were added was conducted following the system reliability testing. The following tests were completed at 1000Hz with a maximum of 10 CTs. This series of tests began with 2 SSTs located in zone 2, while adding 1 SST in zone 2 with each test run until a maximum of 8 SSTs in zone 2 was achieved. Each test run consisted of incrementally timed faults occurring in zone 2 over an entire 60 Hz cycle (or a period of 0.016 seconds). This was achieved by incrementing the fault timing by 0.001 seconds each loop until a total of 16 loops was completed per test run.

The final schematic of the FREEDM Green Hub v4.3 with 8 SSTs in zone 2 is shown below in Figure 5.8.

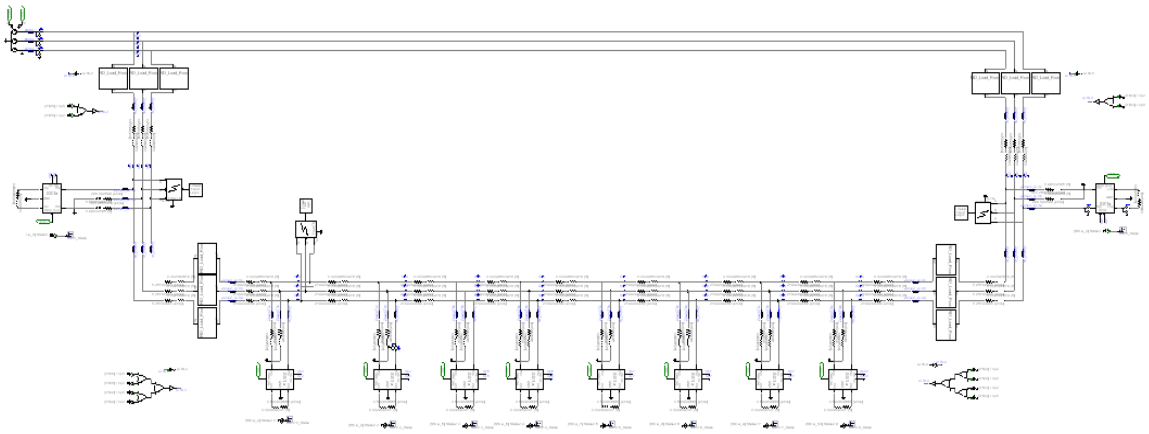


Figure 5.8. Modified Green Hub v4.3 with 8 SSTs in Zone 2

These initial test results are shown in Figure 5.9 below. The sine wave is simply shown as a reference figure for where the fault was initiated during the 60 Hz cycle. These results show very little impact on system performance with the addition of each successive SST. The results seem to suggest that the relative speed of the system increases slightly with the addition of SSTs, but the standard deviation also increases.

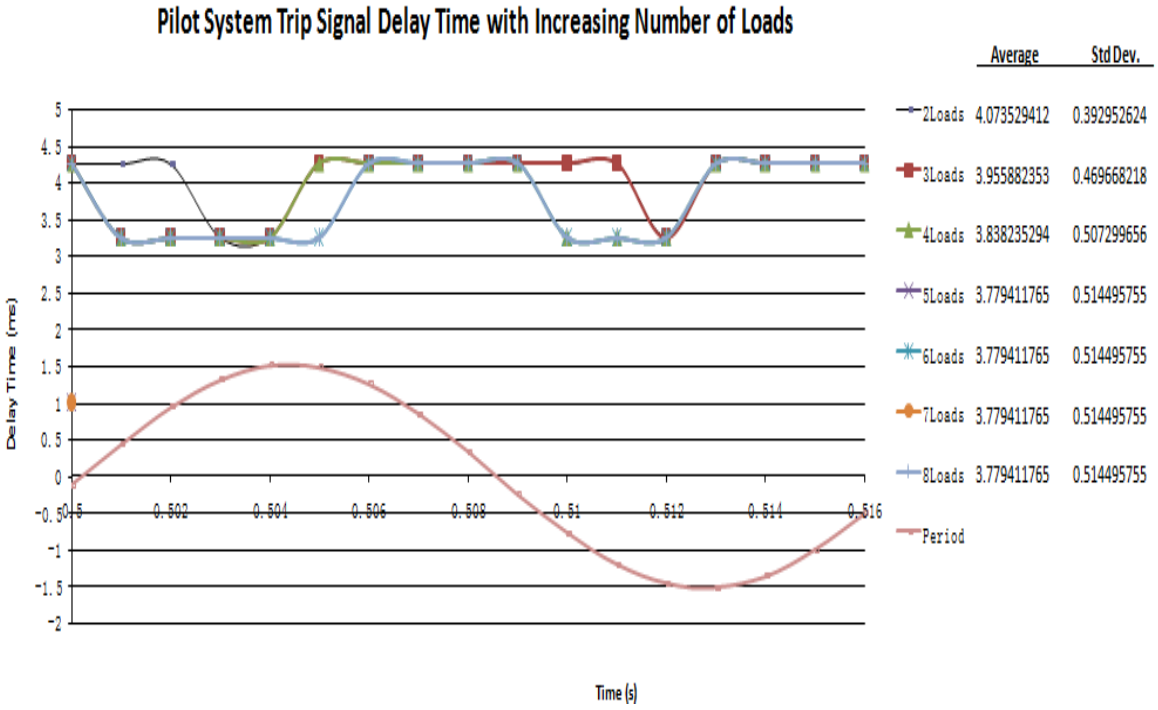


Figure 5.9. 1000Hz Differential Trip Signal Timing Results With Increasing Number of SST/Loads in Zone 2

Table 5.1. Trip signal timing results for faults in various locations with 8 loads in zone 2

Fault Location	Trip Signal Time/Location		
	Zone 1	Zone 2	Zone 3
Zone 1	4.0 ms	-	-
Zone 1 & 2 Overlap	4.0 ms	4.2 ms	-
Zone 2	-	4.2 ms	4.0 ms
Zone 2 & 3 Overlap	-	4.2 ms	4.0 ms
Zone 3	-		4.0 ms

5.2 IEEE34 test system

The implementation of the pilot protection system was needed to be done on a larger system. The IEEE34 test system was thus selected for this purpose.

5.2.1 Background on IEEE34 Test system

The IEEE34 test feeder is a distribution test feeder that integrates all imaginable rational structures and load characteristic, such as symmetry for both single and three phase

distributed loads. The mentioned IEEE34 model also has a local wind generation module in it [37].

The IEEE34 is a widely accepted system model for distribution system in the multiple nodes for three phase balanced main feeder with fixed or spot load at these nodes. The IEEE distribution system analysis subcommittee had developed this test system for use for software engineers and field engineers for validation and testing for current/voltage/power studies. The IEEE34 test system represents an actual feeder in Arizona and it has the following real world features

1. All the sections of the distribution line have been modeled by actual real world phase impedance values.
2. The system contents both single and two phase laterals.
3. Loads on each phase and sections have real and reactive power specifications.
4. The load modes that are used, reproduce load on feeders with intimately distributed load tops.
5. This system include voltage regulation and captive VAR compensation.
6. The system has a long distribution line and is comparatively light loaded.
7. There are a few transformers that convert the voltage to 4.16 kV for a very small section of the feeder.

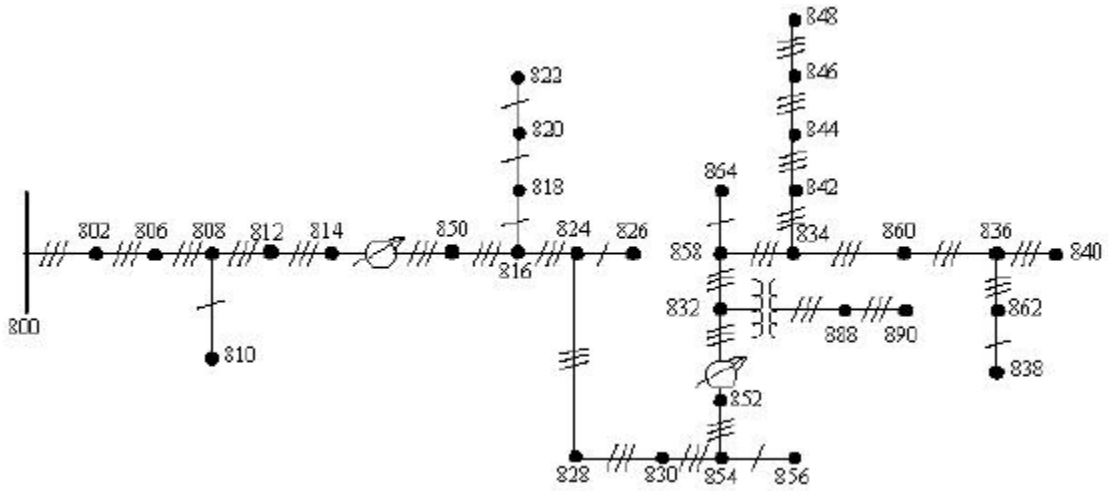


Figure 5.10. IEEE34 node test feeder schematic [37]

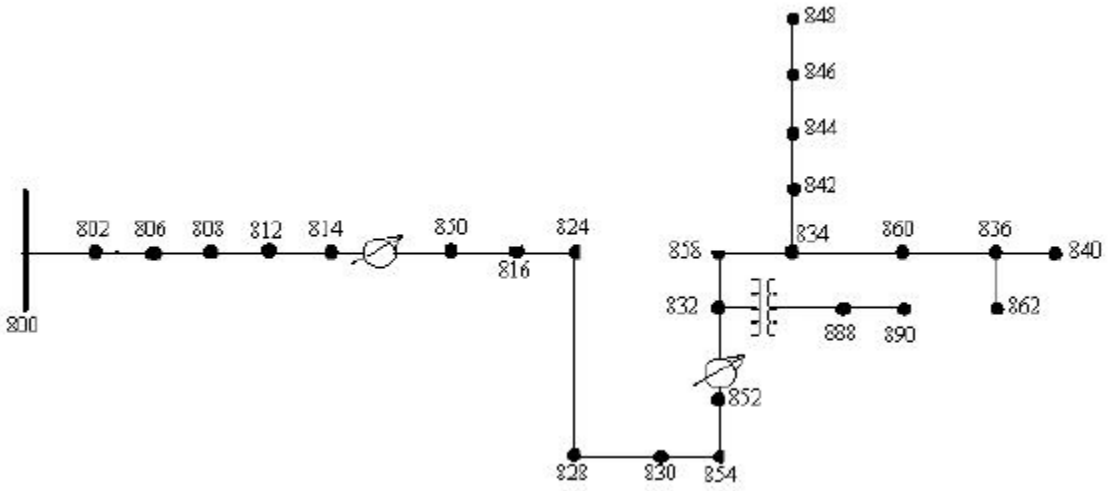


Figure 5.11. Three phase main feeder for the IEEE34 test system after simplification [37]

The IEEE34 system has under gone certain simplification to produce figure 5.11 (from figure 5.10). Hence the reduced section has 25 section as compared to the 33 before. The rules of the reduction/simplification are given in the following reference paper [37]. The two local wind generator which are simulated as large induction machines. They produce 660 kW at 480 V rated voltage.

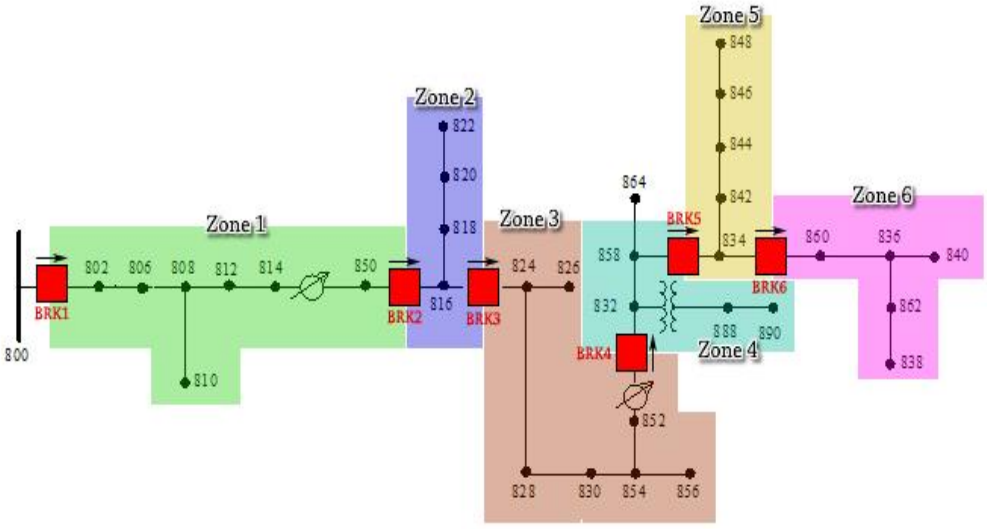


Figure 5.12. Zones of protection for the pilot protection system for the IEEE34 model [29]

For the implementing system the pilot protection system, the IEEE34 has been divided into six protection zones shown in figure 5.12. Now in this case for the division of zones, we have utilized ideal circuit breakers. As explained in the section above the current measurement module measures current at each of the circuit breakers and loads. Each phase of the system is protected independently in the pilot protection system, hence for 6 zones of protections we will be requiring 18 pilot protection system modules in total to be placed in the large system.

5.2.2 Results

Now in order to test the reliability every type of fault (including three phase, two phase faults) was simulated in all the zones over two 60 Hz cycle, such that fault would occur in 1ms time steps so as to investigates every possible fault angle. These test results are shown

in the next few below. The sine wave is simply shown as a reference figure for where the fault was initiated during the 60 Hz cycle.

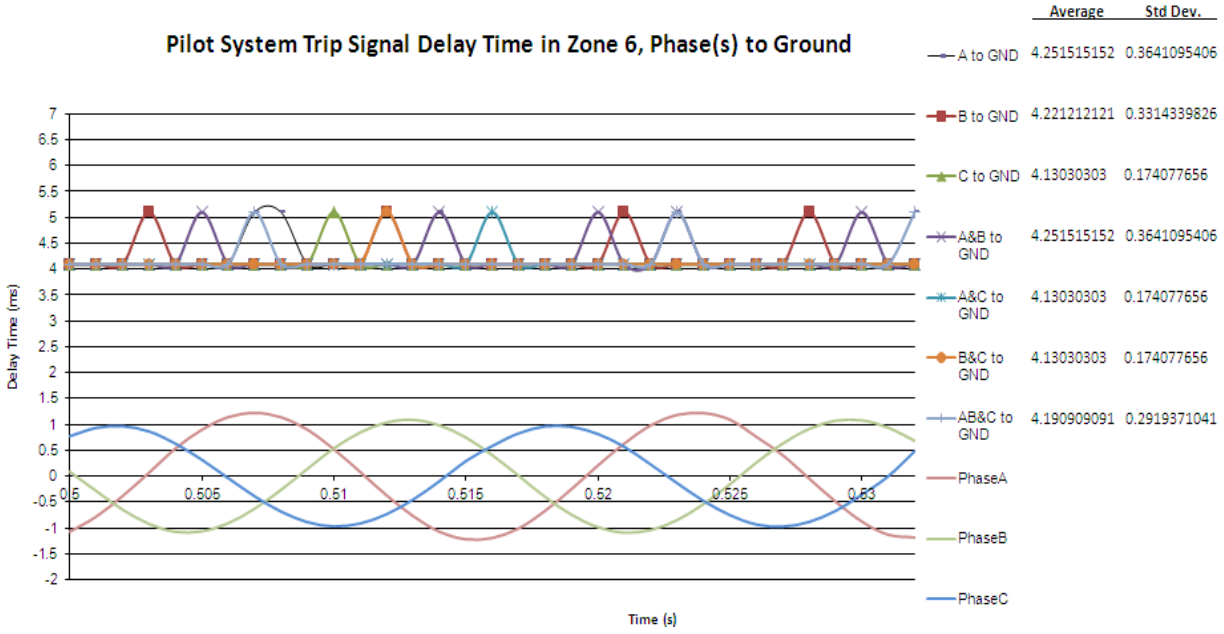


Figure 5.13. Zone 6 Trip delay times for single line to ground, double line to ground and 3 phase fault.

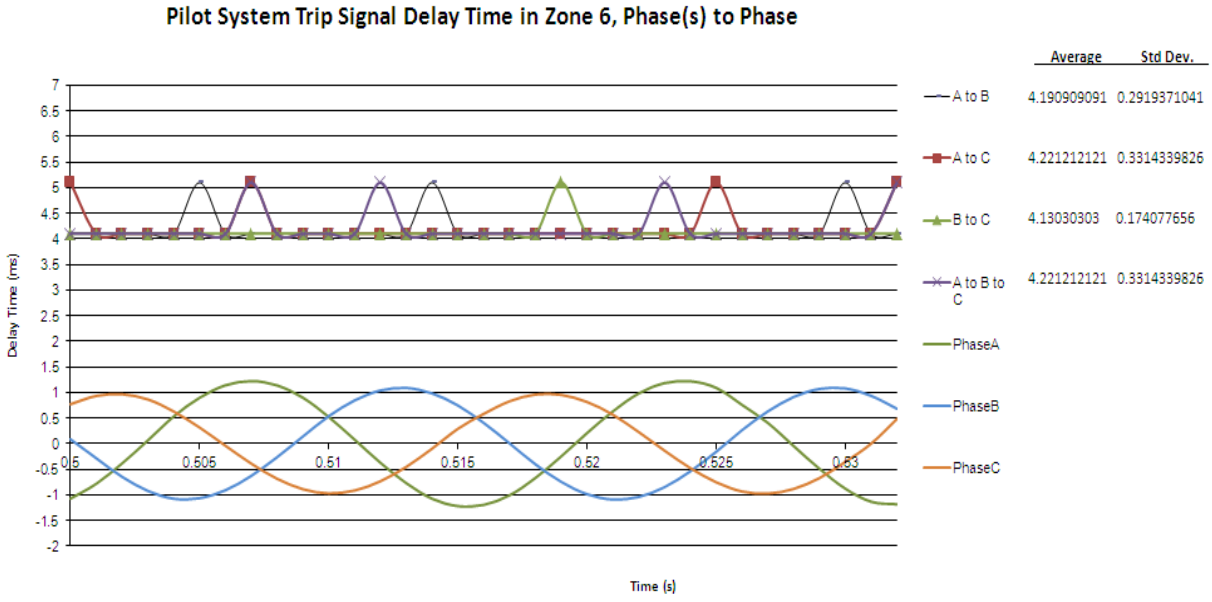


Figure 5.14. Zone 6 Trip delay times for line to line faults.

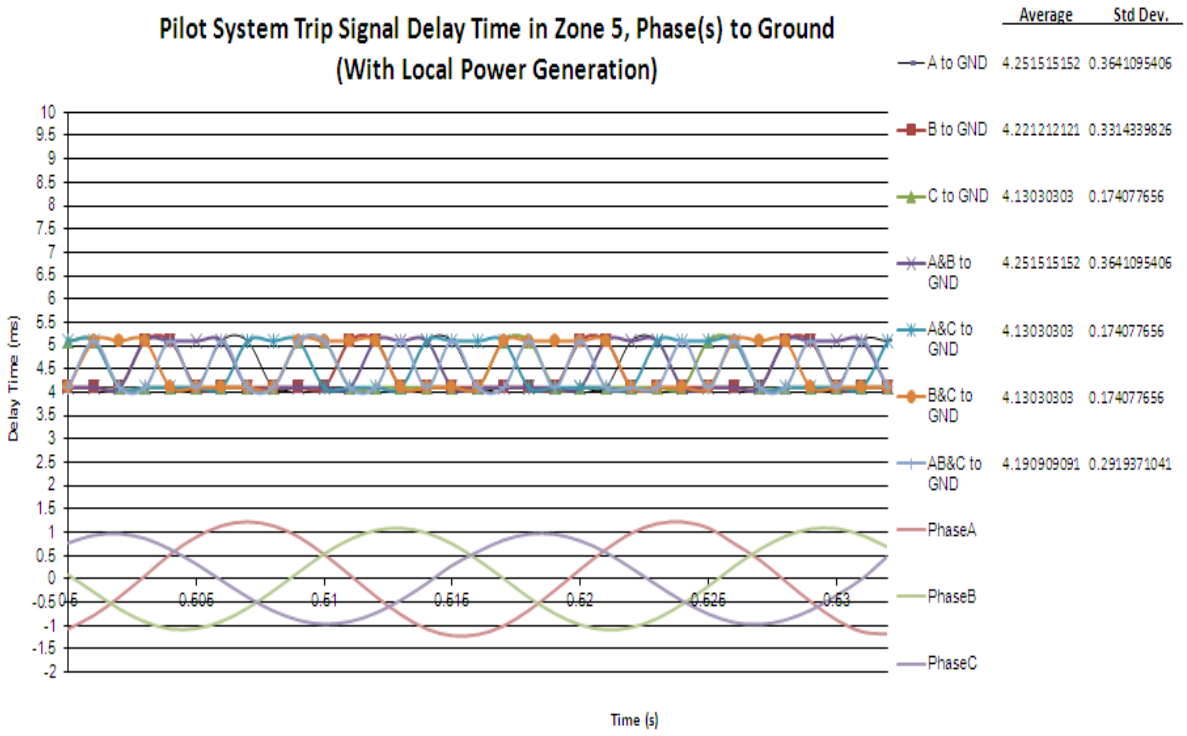


Figure 5.15. Zone 5 Trip delay times for single line to ground, double line to ground and 3 phase fault.

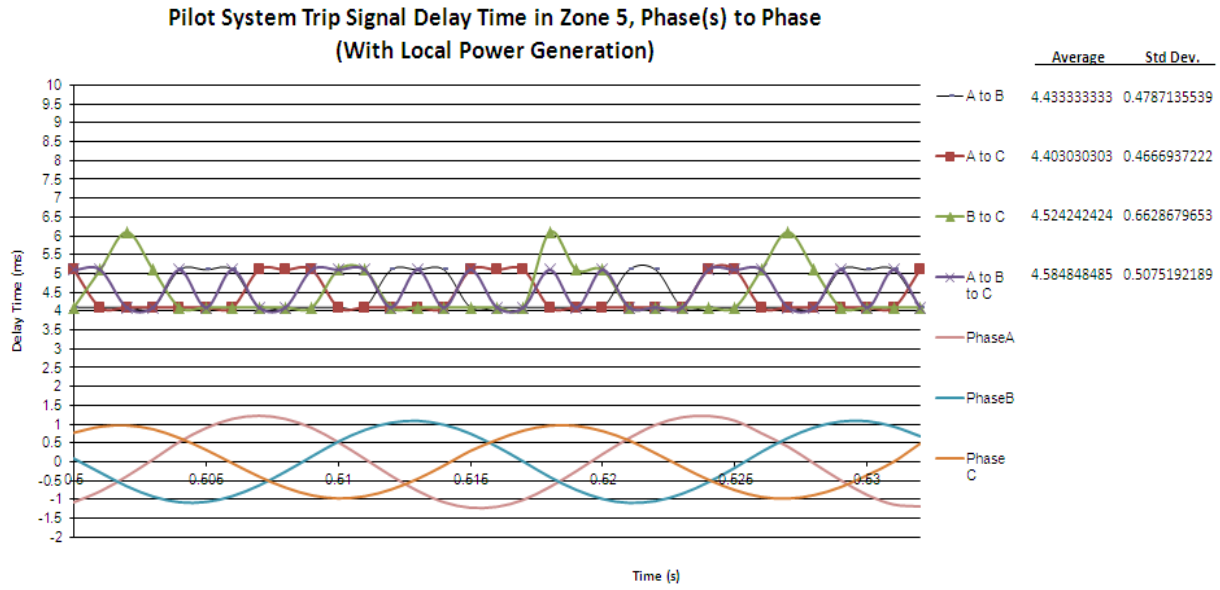


Figure 5.16. Zone 6 Trip delay times for line to line faults.

A collective tabular result for all the trip delay timings for various faults in zone 1,5 and 6 is shown in the table below.

Table 5.2. Trip signal delay times for the IEEE34 model for zones 1, 5 and 6 [29]

Protection Zone	**Fault Type**	**Average Delay (ms)**	**Standard Deviation**
1	A to GND	4.2818	0.3917
1	B to GND	4.2818	0.3917
1	C to GND	4.2515	0.3641
1	A&B to GND	4.5242	0.5019
1	A&C to GND	4.5242	0.5019
1	B&C to GND	4.3727	0.4523
1	A&B&C to GND	4.4939	0.4962
1	A to B	4.2515	0.3641
1	A to C	4.2818	0.3917
1	B to C	4.5242	0.6623
1	A to B to C	4.3727	0.4523
5	A to GND	4.2515	0.3641
5	B to GND	4.2212	0.3314
5	C to GND	4.1303	0.1740
5	A&B to GND	4.2515	0.3641
5	A&C to GND	4.1303	0.1741
5	B&C to GND	4.1303	0.1741
5	A&B&C to GND	4.1909	0.2919
5	A to B	4.1909	0.2919
5	A to C	4.2212	0.3314
5	B to C	4.1303	0.1741
6	A to B to C	4.2212	0.3314
6	A to GND	4.3424	0.4352
6	B to GND	4.3424	0.4352
6	C to GND	4.3424	0.4352
6	A&B to GND	4.5242	0.5019
6	A&C to GND	4.5242	0.5019
6	B&C to GND	4.5545	0.5056
6	A&B&C to GND	4.4939	0.4962
6	A to B	4.4333	0.4787
6	A to C	4.4030	0.4667
6	B to C	4.5242	0.6629
6	A to B to C	4.5848	0.5075

The fault current simulated for this system are about 10 times the rated current, here in this case , the sampling rate is kept as 1000Hz. Zones 1,5 and 6 are primarily chosen as they are the nearest and furthest from the generation and zone 5 is selected because it has the wind generator model, providing power to that particular zone. In all of the test one thing is certainly proved that there is no trip detection for zones, other than the one having the fault.

The result shows that the pilot protection system was able to study the effect of fault incidence angle and fault type on the trip signal response of the protection scheme. The result shows the trip response timings are fairly consistent between 4.13 to 4.5848 ms and Standard deviation is around 0.17 to 0.66ms, and no anomalies are experienced in this system.

5.3 Reclosing algorithm in PSCAD [29]

In the pilot protection system, we have also enclosed reclosing module, which does up to 3 reclosing (reclosing timings are user defined) which is then pursued by a system lockout. This reclosing unit have been developed as per the IEEE Standard P 37.60 reclosing [29].

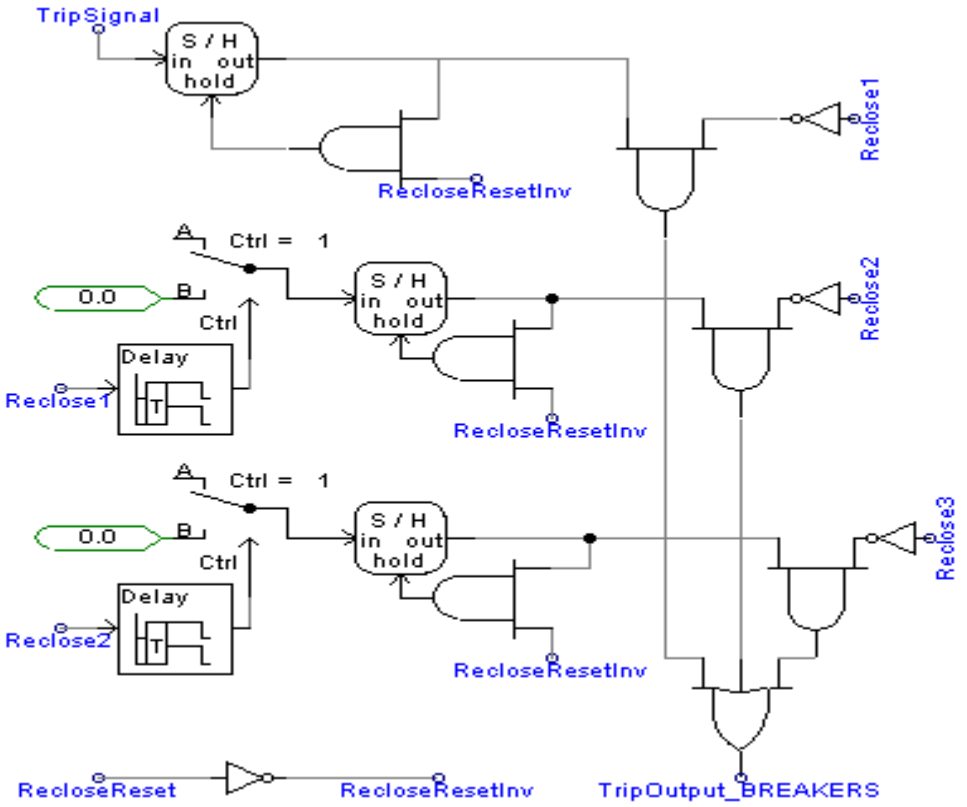


Figure 5.17. Reclosing logic included with the trip logic [29]

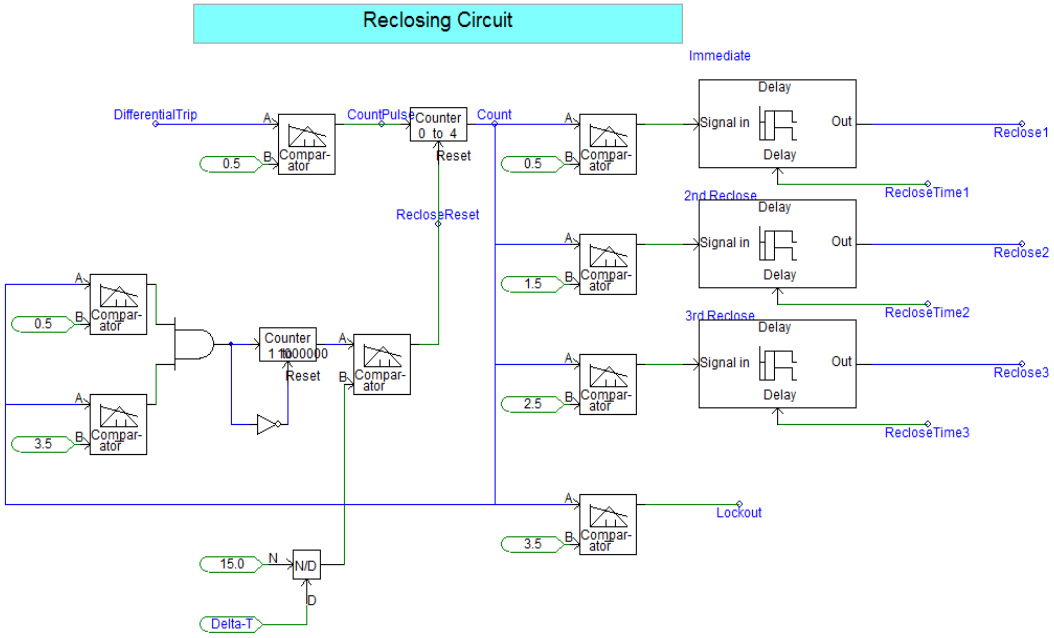


Figure 5.18. Logic to determine reclosing timings 1, 2 and 3

So as shown in the logic diagram, the trip signal is sampled and the trip signal is held till the reclose reset (for lockout) bit is low. Once it is low, then in that case the signal is first compared with inverse Reclose 1. If Reclose 1 is high, in that case, the trip is reduced to zero immediately, after a small delay Reclose 2 is compared with the trip signal and Reclose 2 is high in that case trip is reduced to zero. In third Reclose 3 after a certain delay after Reclose 2 the trip signal and Reclose 3 are compared, if Reclose 3 is high, trip is reduced to zero or in that case there is permanent lock out.

5.4 Implementation of the Pilot Protection Scheme for the large scale system simulation loop or modified IEEE 34 system [38][39]

After establishing the results of the pilot protection system for the traditional large scale distribution system. It was necessary to implement it for larger system with a variable solid state transformer load, capable of producing distributed renewable energy. For this purpose LSSS loop (Large scale system simulation) is implemented with the pilot differential protection system.

Even though the Pilot projection system was developed for the FREEDM Green hub distribution project, the LSSS Loop presents a new challenge, with new SST model, developed at MS&T. The new results for the LSSS loop will help develop a primary protection scheme, which will also be used by the team at MS&T for the LSSS Loop.

5.4.1 Development of the modified IEEE 34 Loop (LSS Loop) from 24.9KU to 12.47KL line to line voltage [38]

The LSSS Loop has been created by modifying the original IEEE 34 distribution system. While the IEEE 34 distribution system is originally a 24.9 kV system, the LSSS or the modified IEEE34 is made to be a 12.47KV system. Here in this case the 12.47KV rating is

obtained by dividing the original impedance value by four in order to keep the per unit for impedance constant for both the 24.9KV and 12.47KV system. But the capacitance is multiplied by 4 due to reduction in voltage between and the loads remain the same.

Now as the length of the lines is divided by four, over all capacitance of each line hence remains constant.

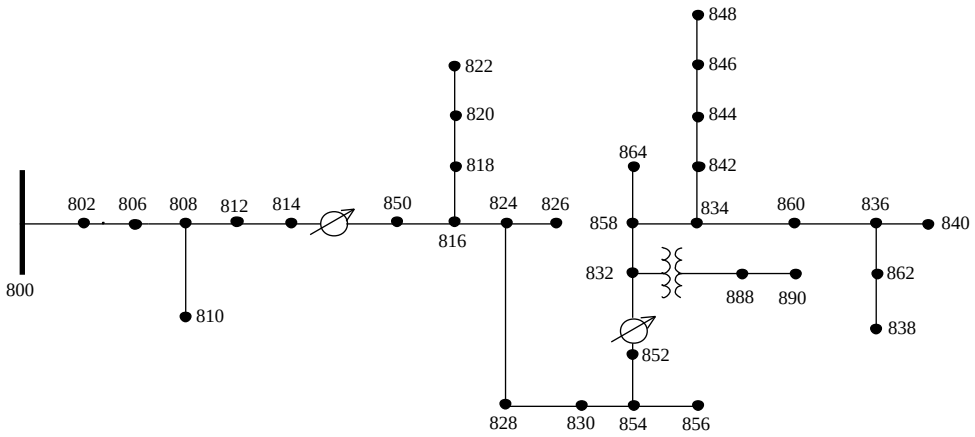


Figure 5.19. IEEE 34 (original model) schematics [37]

In this modified version of the IEEE 34, the voltage regulator located between node 814 and 850 and voltage regulator situated between nodes 854 and 832 are removed. Also the capacitor banks between 844 and 848 have also been removed.

Load information for the newly developed 12.47 kV system is given below

Table 5.3. Load information for the 12.47 kV system [38]

Node A	Node B	Load Model	Load Type	Ph-A kW	Ph-A kVAr	Ph-B kW	Ph-B kVAr	Ph-C kW	Ph-C kVAr	SST Connected	Number of SSTs
802	806	Y-PQ	Distributed	0	0	30	15	25	14	Yes	2
808	810	Y-PQ	Distributed	0	0	16	8	0	0	Yes	1
818	820	Y-PQ	Distributed	34	17	0	0	0	0	Yes	1
820	822	Y-PQ	Distributed	135	70	0	0	0	0	Yes	1

816	824	Y-PQ	Distributed	0	0	5	2	0	0	Yes	1
824	826	Y-PQ	Distributed	0	0	40	20	0	0	Yes	1
824	828	Y-PQ	Distributed	0	0	0	0	4	2	Yes	1
828	**830**	**Y-PQ**	**Both**	**17**	**8**	**10**	**5**	**25**	**10**	**Yes**	**3**
854	856	Y-PQ	Distributed	0	0	4	2	0	0	Yes	1
832	858	Y-PQ	Distributed	7	3	2	1	6	3	Yes	3
858	864	Y-PQ	Distributed	2	1	0	0	0	0	Yes	1
858	834	Y-PQ	Distributed	4	2	15	8	13	7	Yes	3
834	**860**	Y-PQ	**Both**	**36**	**24**	**40**	**26**	**130**	**71**	**Yes**	**3**
860	836	Y-PQ	Distributed	30	15	10	6	42	22	Yes	3
836	**840**	Y-PQ	**Both**	**27**	**16**	**31**	**18**	**9**	**7**	**Yes**	**3**
862	838	Y-PQ	Distributed	0	0	28	14	0	0	Yes	1
842	**844**	**Y-PQ**	**Both**	**144**	**110**	**135**	**105**	**135**	**105**	**Yes**	**3**
844	846	Y-PQ	Distributed	0	0	25	12	20	11	Yes	2
846	**848**	Y-PQ	**Both**	**20**	**16**	**43**	**27**	**20**	**16**	**No**	3
890	**890**	Y-PQ	**Spot**	**150**	**75**	**150**	**75**	**150**	**75**	**No**	3

From Table 5.3, it is seen that there are in total 40 solid state transformers connected/brought online together after l sec of the simulation time. “Load type – both “refers to the fact that spot and distributed load have been added to the system in order to restrict the number of load type SSTS. This module does not contain PV and energy storage schematic modules

5.4.2 Solid State Transformer Module Development

As has been explained before the SST has multiple stages which include the 20 kVA AC/DC rectifier (converting 7.2 kV AC to 4800 volt DC) then a DC-DC convertor HF transformer with DAB to 3800 volts DC covert to 400 volt DC and in the end an inverter is used to obtain a 420/240 volts AC output.

Active rectifier in the SST [38]

The active rectifier in the SST is a numerous leveled rectifier which converts the AC into DC power, also giving reactive power control on the primary/high voltage side of the SST. Based on the hardware developed at NCSU [p.r.], the SST is rated for 20 kVA for this case and 10 parallel such SST's have been connected to total a rating of 200 kVA. So the reactive power control of all the 200 kVA is done together. Here below shown in figure 5.20 is the control source circuit diagram connected in series with RL filter DQ control is used for rectification.

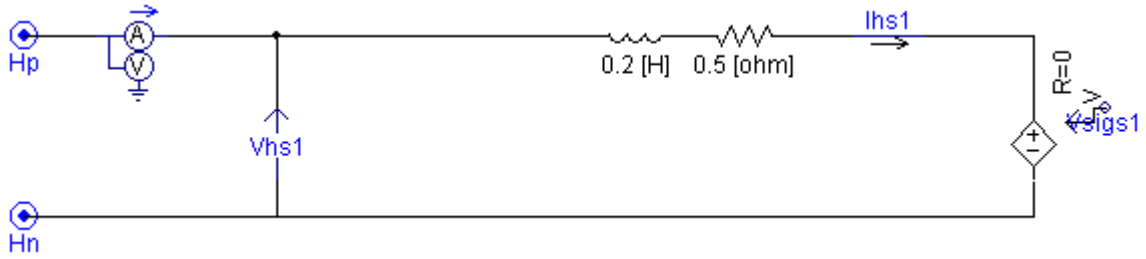


Figure 5.20. The figure above represents active rectification i.e. nonlinear rectified with power electronic switches [38].

But the performance of the rectifier is actually successfully achieved through power balance. The multi meter shown in figure gives the angle between the voltage and the current. Filter impedance at the input side set at 30% at the rated impedance.

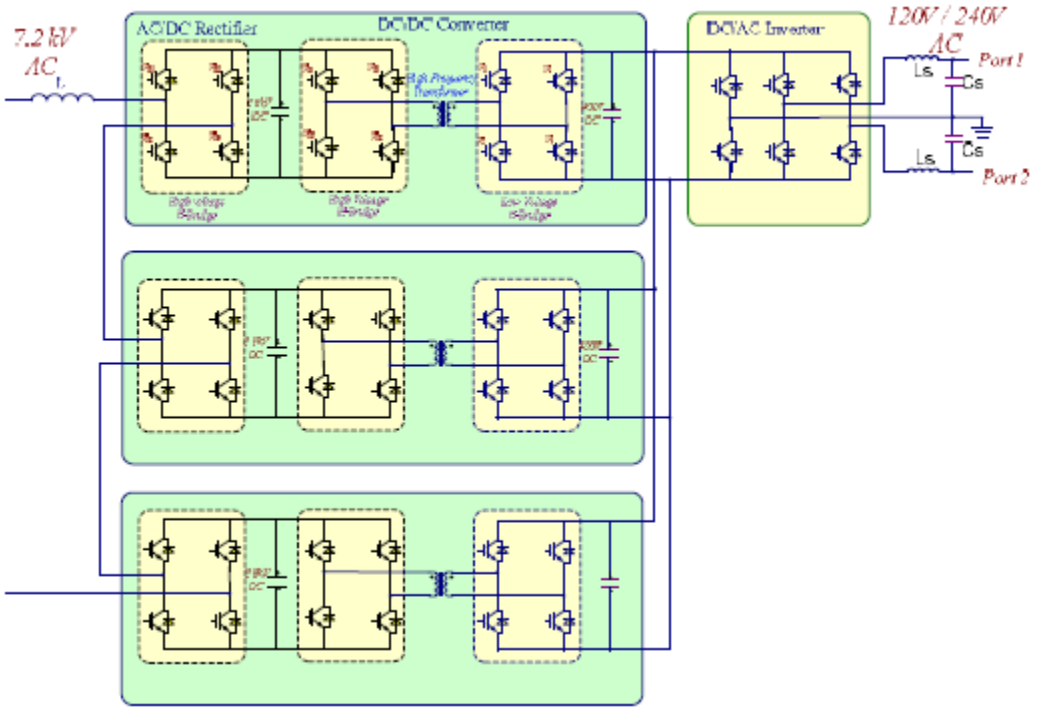


Figure 5.21. SST topology used for the average model simulation [13]

Based on the NCSU SST model paper shown in figure 5.21. , the 20 kVA SST has 3 cascaded H bridge rectifiers and each of them is connected to a dual active bridge converter. High voltage DC rating is 3800V DC and as they are connected in series, hence the total high voltage rating in DC is 11400V. The rectifiers are mainly responsible to maintain this DC link voltage. Hence for a 200 KVA rating, there are in total 30 DAB converters.

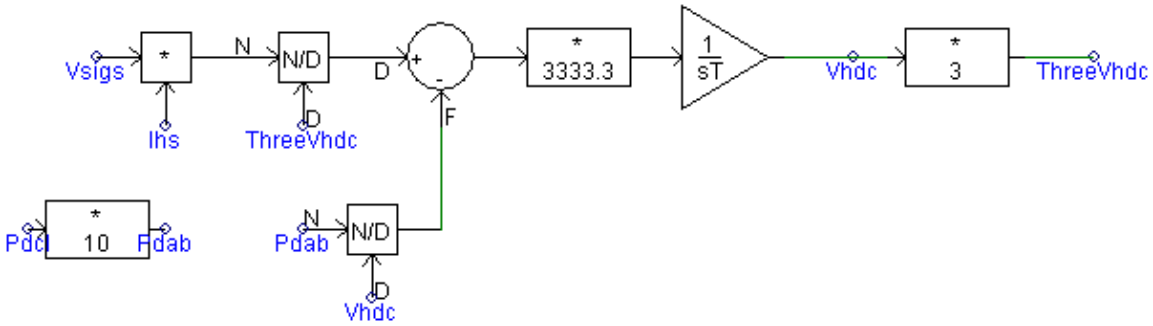


Figure 5.22. Power balance equation block for the rectifier [38]

The figure 5.22 above shows the power balance equation from the DC link voltage (High voltage side 3800V DC) denoted by V_{HDC}. The product of the primary side of the voltage and primary side current divided by 3 times the high voltage DC gives the total DC current for the 200 KVA system. i.e.

$$V_{pri}I_{pri} = 3V_{HDC}I_{HDC} \qquad (5.1)$$

Each 3800 V DC link capacitor is connected to 10 parallel DAB convertor. Power of the output stage of the rectifier is calculated for 1 DAB, and for 10 DABs, the value is multiplied by 10, so that the Kirchhoff's current law can be validated at that node where the DC link capacitor is linked, the DAB power is then divided by V_{HDC} and subtracted from the total DC current.

The residual value is then divided by the equivalent capacitor value of the DC link capacitor. The input capacitor magnitude for each DAB is 30 micro farad (uF) so for 10 it will be 300 uF. Final result is integrated to give DC voltage value. . Power balance equation is now followed by control stage which is shown in Fig. 5.23.

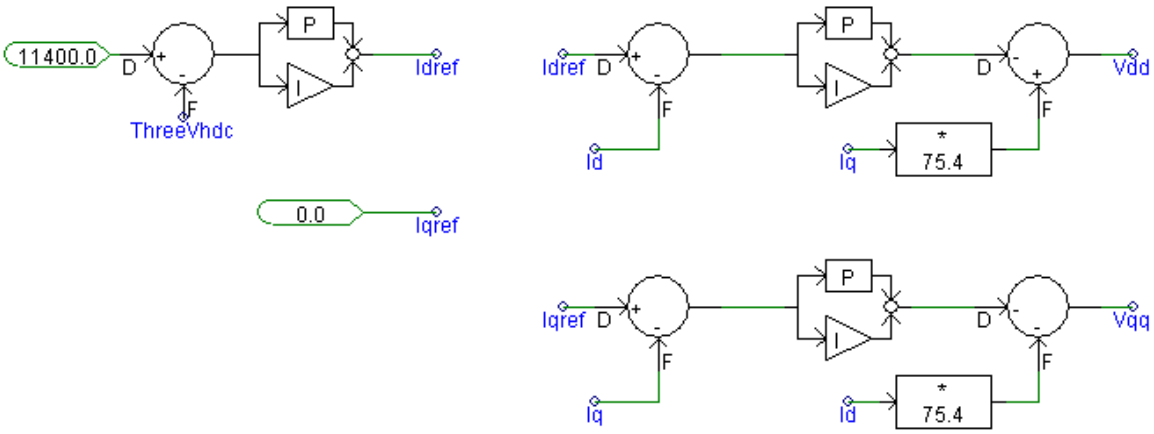


Figure 5.23. Control Stage in rectifier [38]

'Vdd' and 'Vqq' calculations are based on the control stage given in small signal space models of active rectifiers [38]. For proper tuning of controller, procedures given in [38] were followed. Using [2], equivalent resistive load was first connected instead of DAB and inverter in order to make calculations for state transition matrix simple. For example, an operating point of 200 kW was considered. Since there are three cascaded rectifiers, output of each DC link is 66.66 kW at a voltage of 3800 volts and so resistance is 216.6021 ohms. This value is used for DC load modeling. While calculating elements of state transition matrix, the only change made is the multiplication factor '3' multiplied to 'Vdc'. Also filter for SST rectifier is simple R-L filter. For stable operation, eigen values of this matrix should be on the left half plane.

Given the amount of reactive power to be absorbed or injected, corresponding 'Iq' is send to the control stage. Fig. 5.24 shows 'wt' calculation using grid voltage angle. Fig. 5.25 shows 'Id' and 'Iq' calculations which are required for control stage in Fig. 5.26.

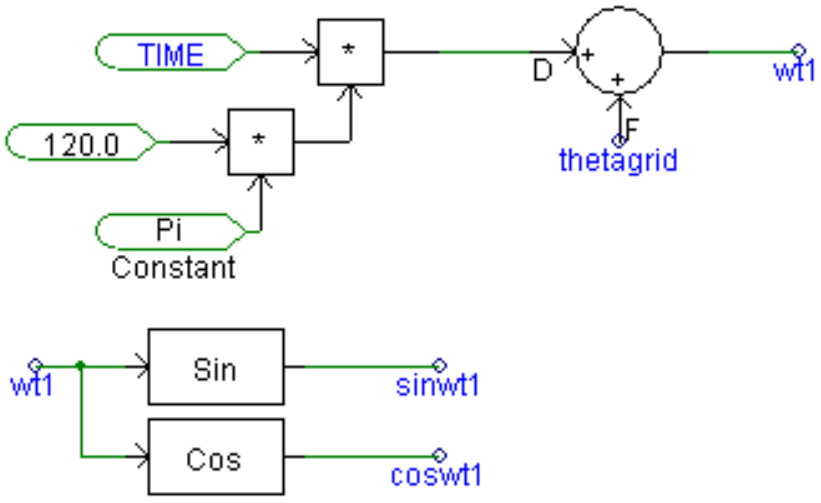


Figure 5.24. Calculating ωt angle using grid voltage angle [38]

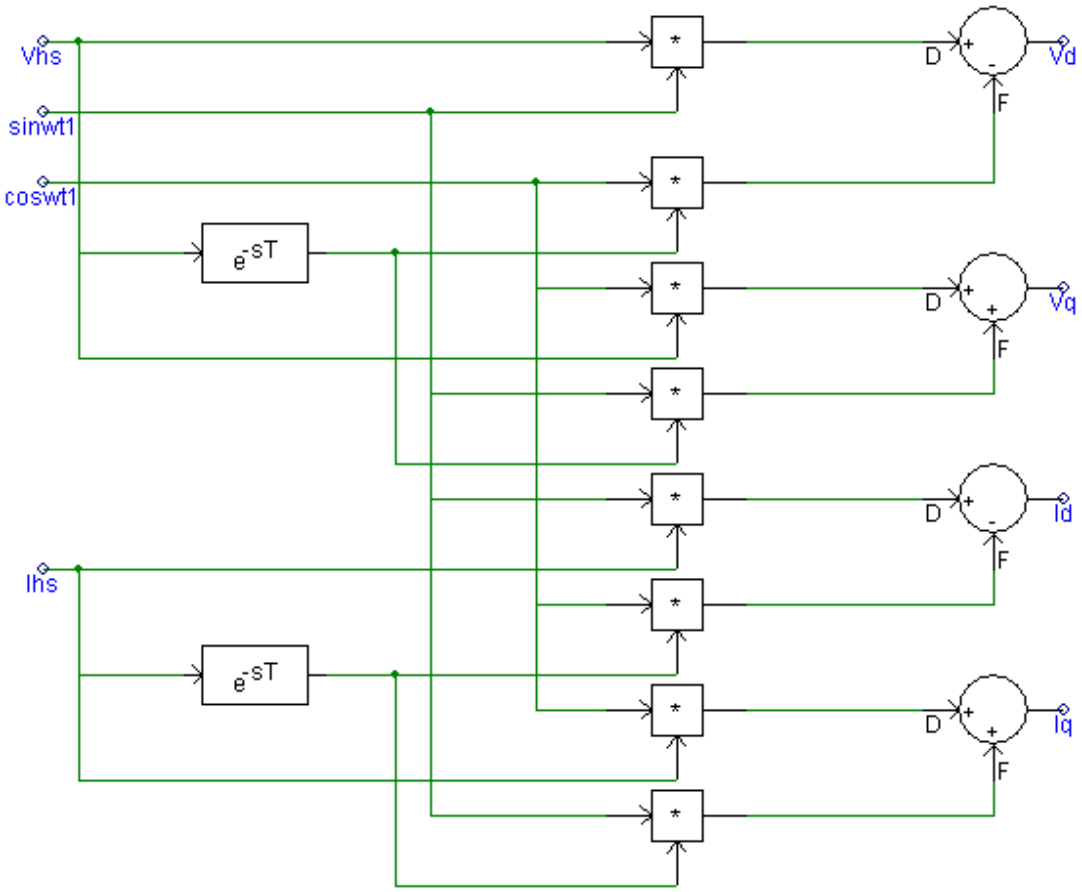


Figure 5.25. $I_{d,}I_q$ Calculations [38]

Fig. 5.26 (below) shows equivalent AC voltage calculation using the values of 'Vdd' and 'Vqq'.

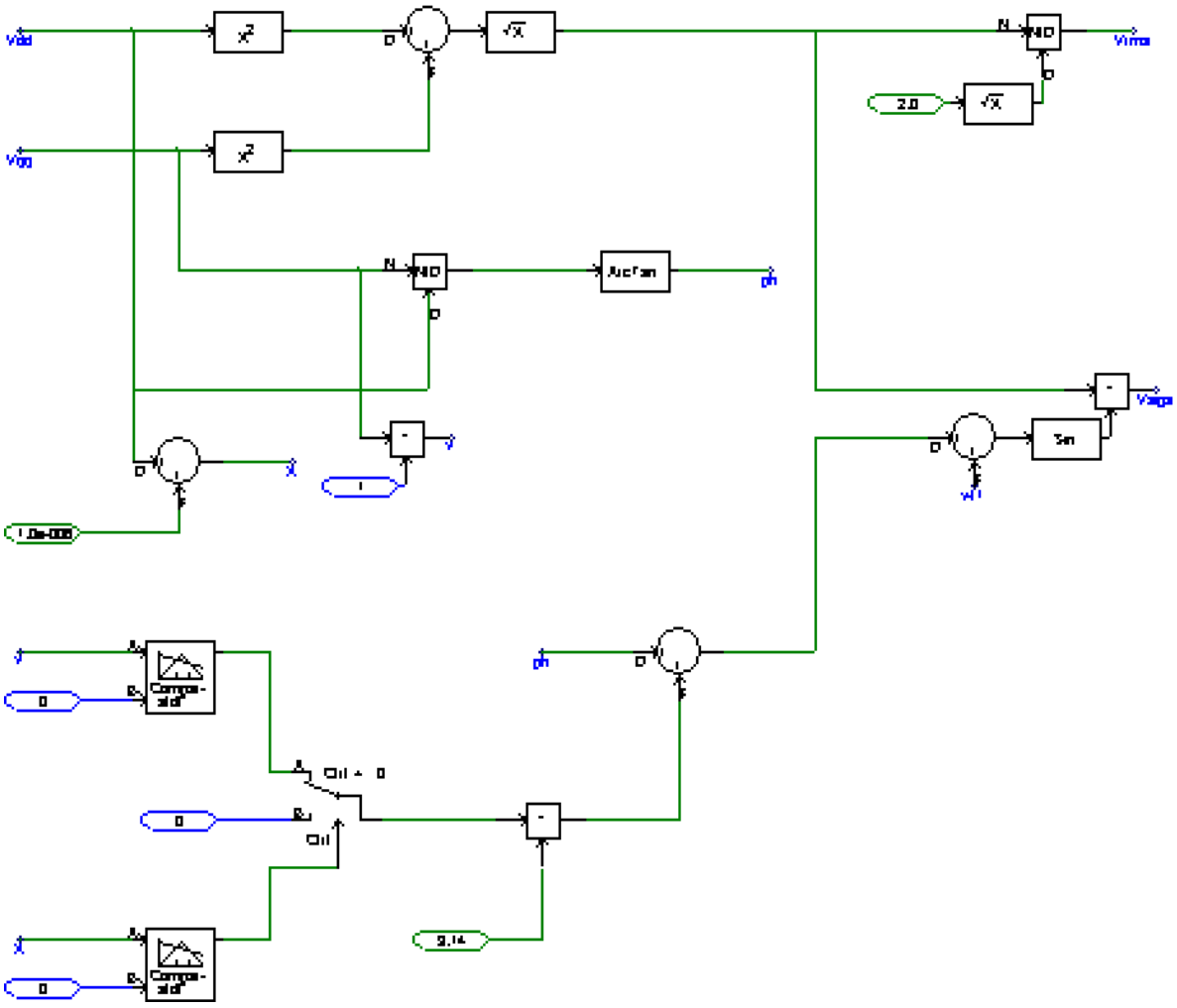


Figure 5.26. V_{dd} and V_{qq} Calculation [38]

5.4.3 Implementation of the Pilot Protection System for the LSSS System or the modified IEEE 34 System.

The modified IEEE 34 or the LSSS system has been divided into five zones of protection as shown in the figure 5.27.

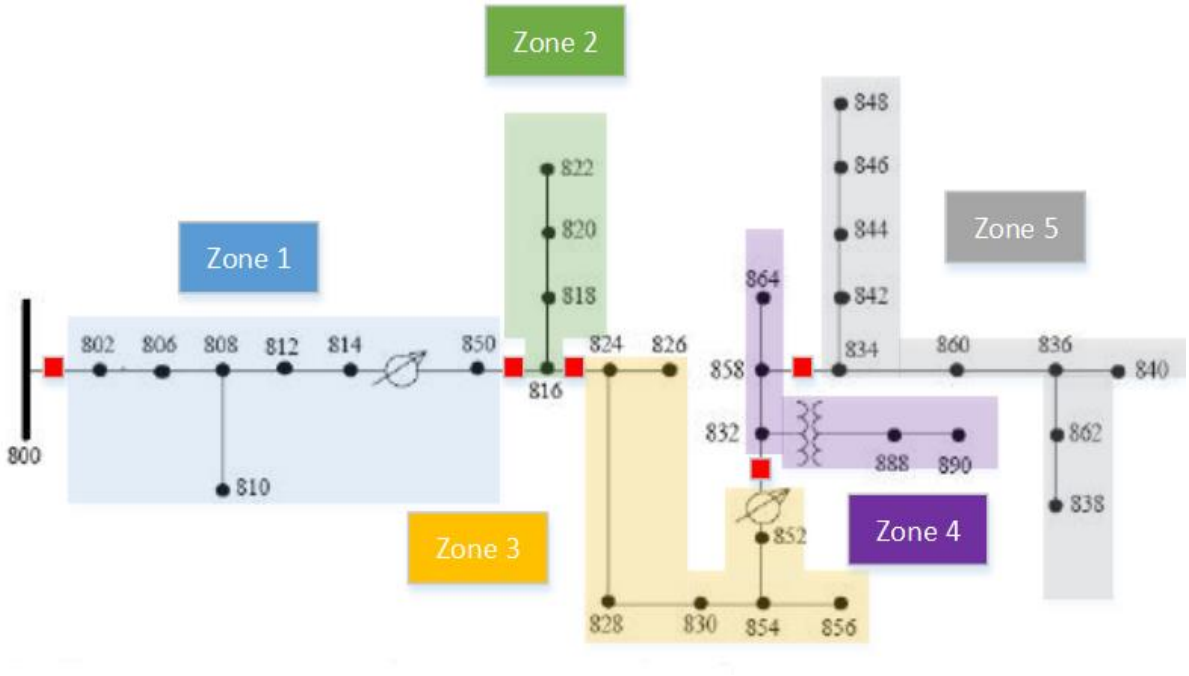


Figure 5.27. Zones of protection for implementing the pilot protection system for the LSSS system [39].

The division of zones is done by using conventional breaker on border of adjacent zones. The sampling frequency for the pilot protection module is kept as 1000 Hz. As the pilot protection modules protect individual phase for each zone and hence in total for 5 zones, we will have 15 pilot protection modules. Below shown are the schematic in PSCAD software used for simulation for this model and seven type of faults including 3 phase (single phase to ground and double line to line have been investigated all the for zones 1,2,3,4,5 and the graph for the trip times are shown below. Results shows that the trip timings are consistent and for all the faults, there are no mis trips from any other zone, except for the one which has it. No reclosing has been deployed here in this case and hence this result does not include reclosing of the load type SSTS after clearing the fault.

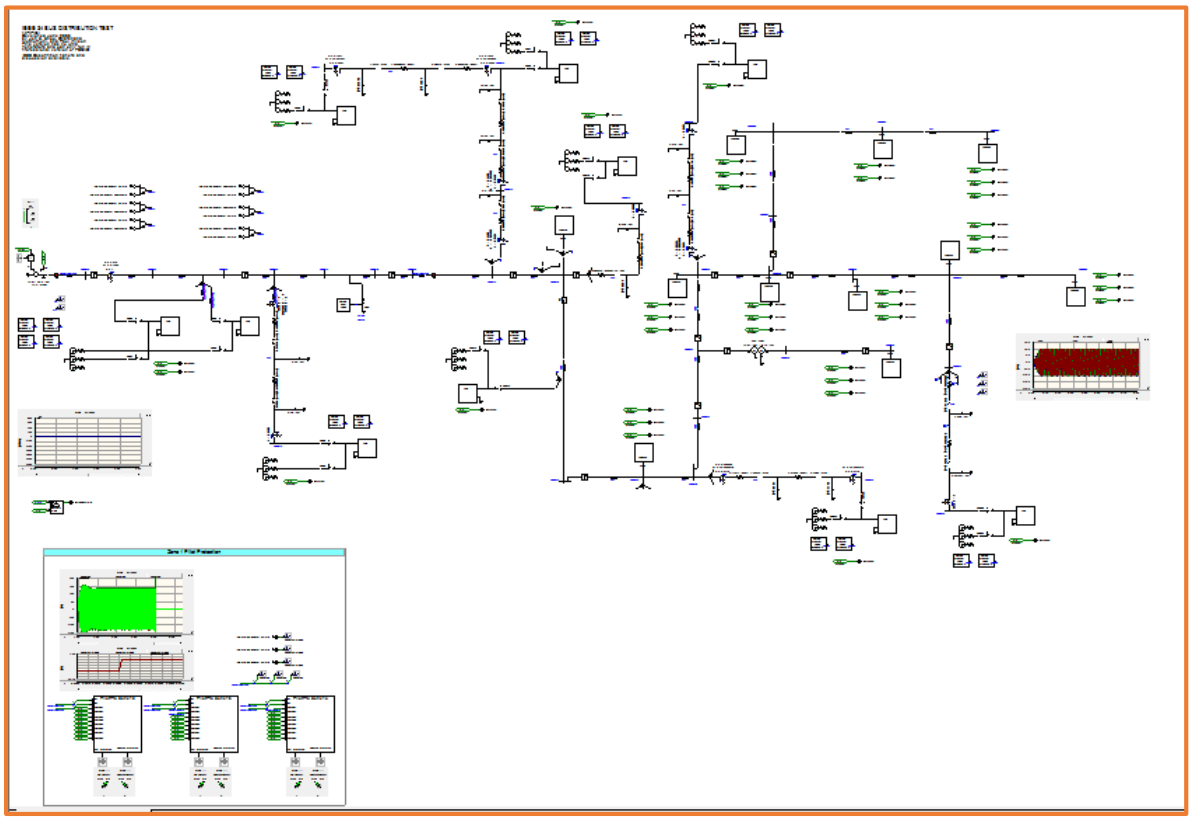


Figure 5.28. Schematic of LSSS loop on PSCAD

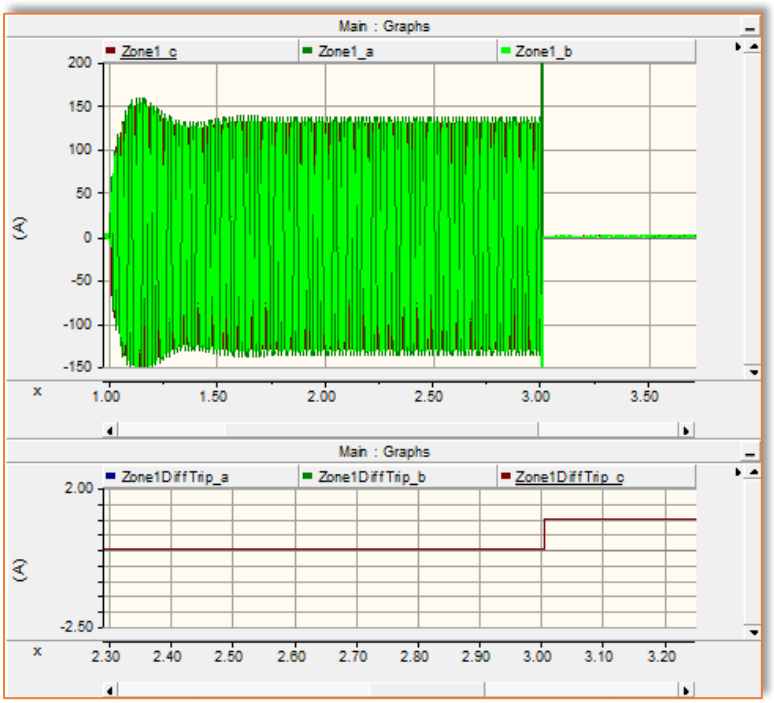


Figure 5.29. Three phase fault in Zone 1 for IEEE 34 with SST at time 3 sec

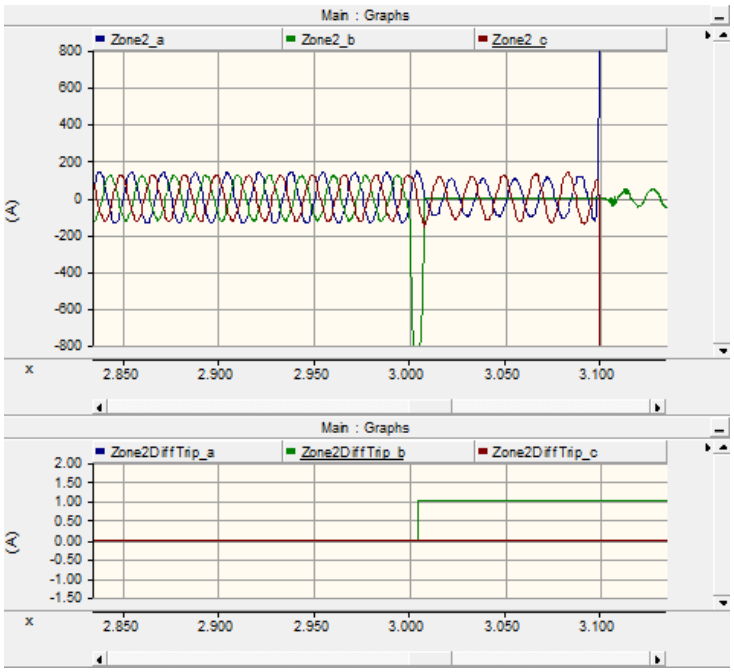


Figure 5.30. Phase B to ground fault in Zone 2 for IEEE 34 with SST at time 3 sec

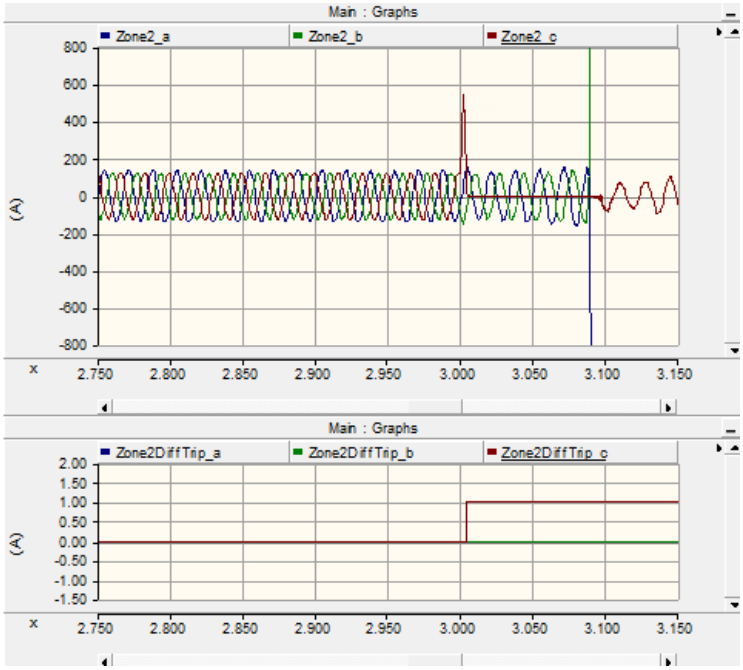


Figure 5.31. Phase C to ground fault in Zone 2 for IEEE 34 with SST at time 3 sec

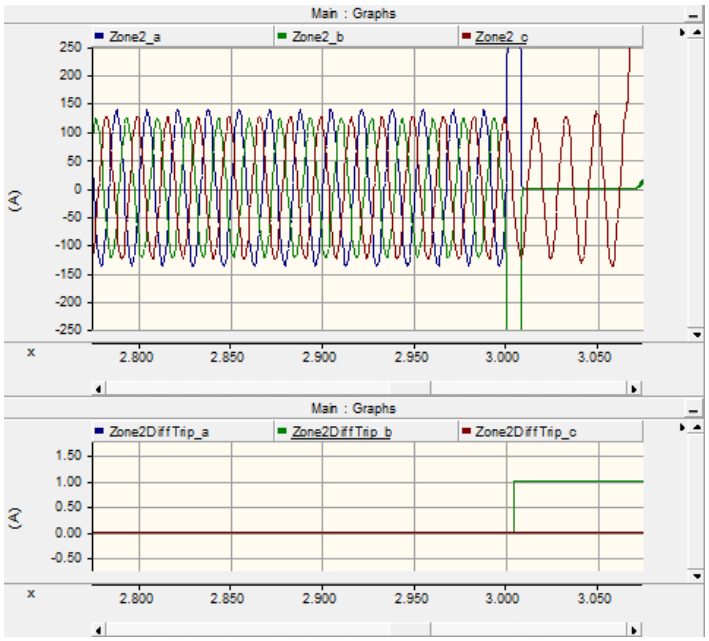


Figure 5.32. Phase A to B fault in Zone 2 for IEEE 34 with SST at time 3 sec

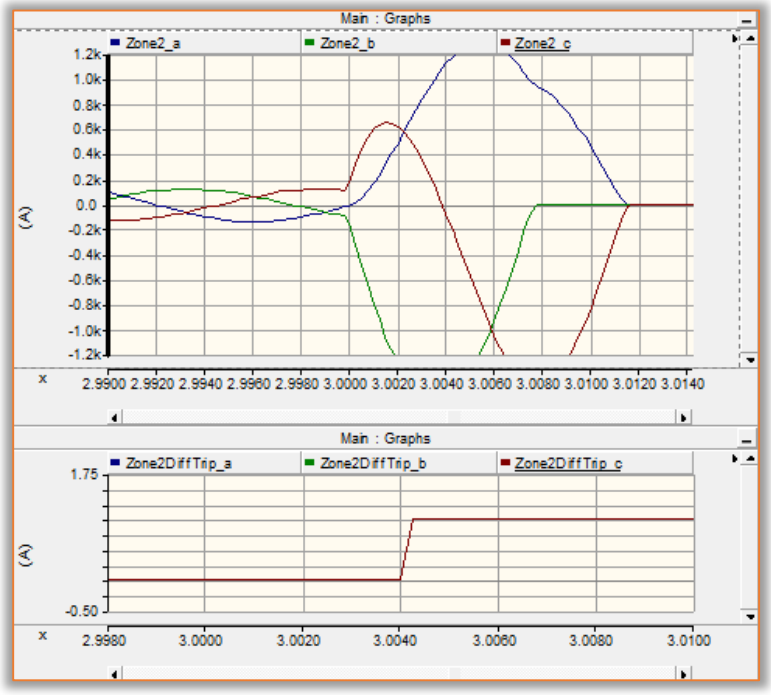


Figure 5.33. Zoom in on the trip signal activation for a fault at t=3 sec in zone 2.

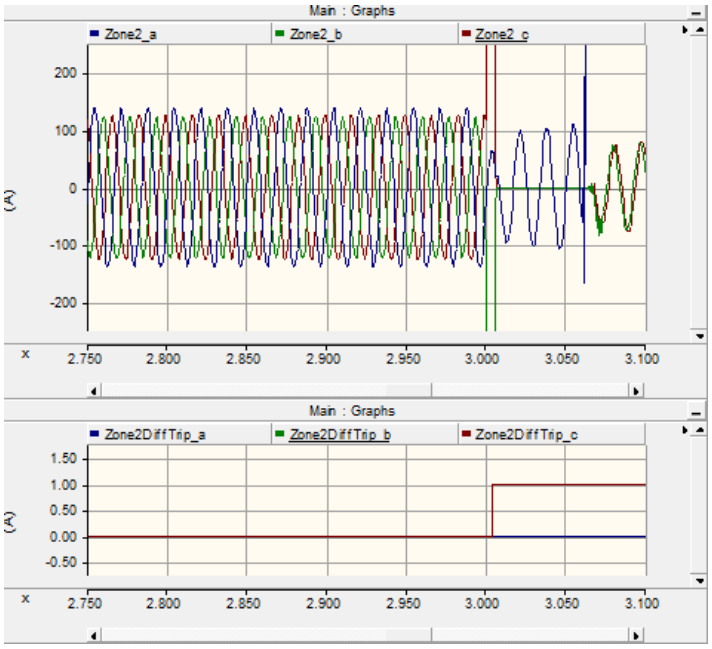


Figure 5.34. Phase B to C fault in Zone 2 for IEEE 34 with SST for fault at time 3 sec

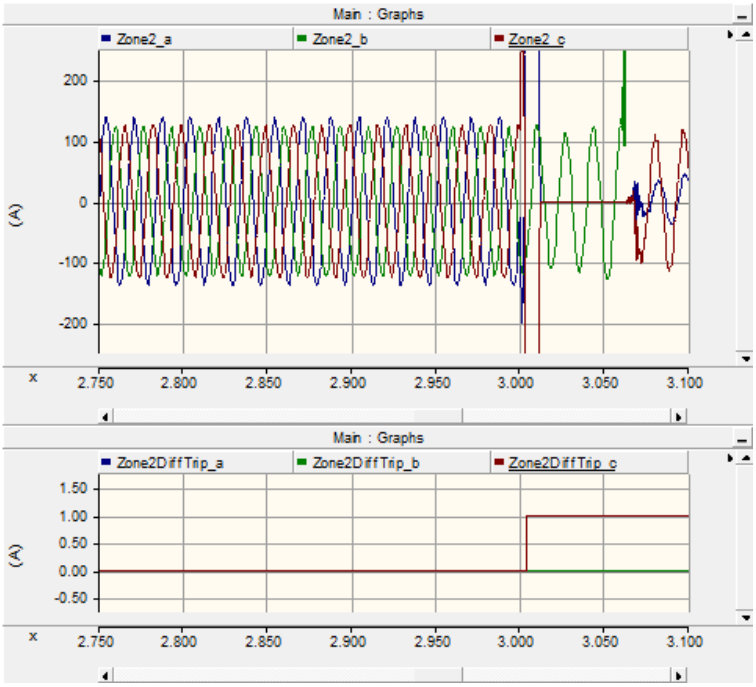


Figure 5.35. Phase C to A fault in Zone 2 for IEEE 34 with SST for fault at time 3 sec

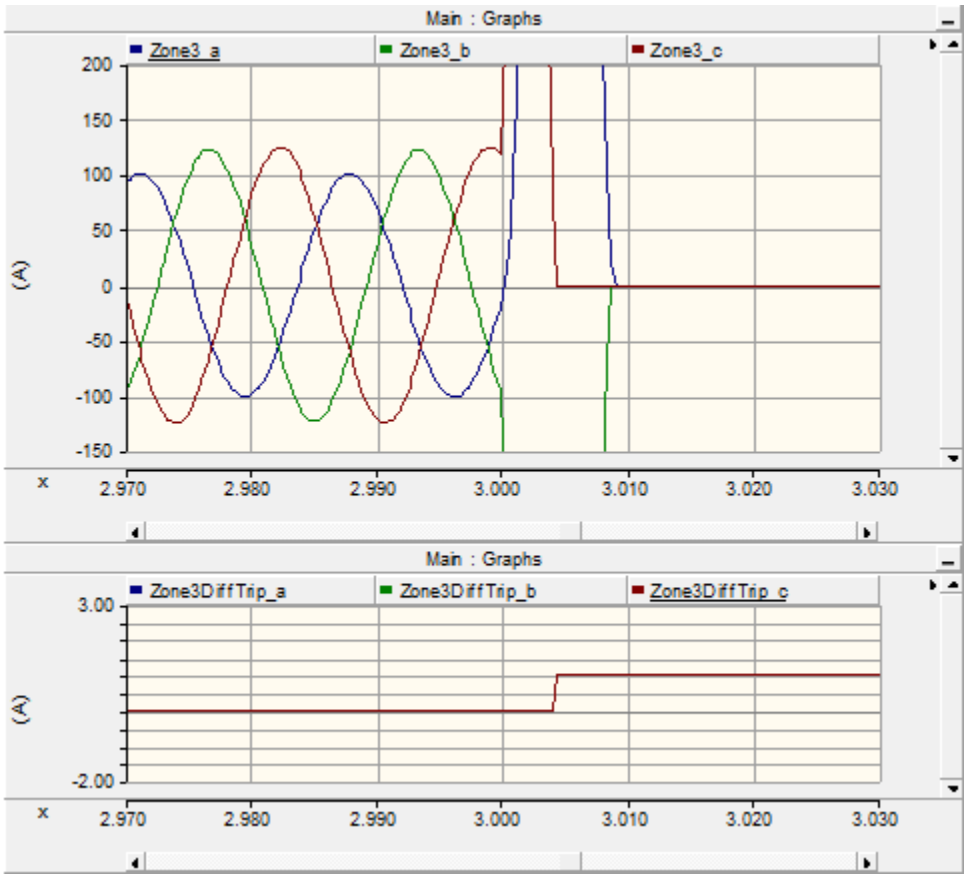


Figure 5.36. 3 phase fault in Zone 3 for IEEE 34 with SST for fault at time 3 sec

Based on the results above, the pilot protection algorithm is successfully able to detect the fault for the LSSS loop utilizing the SST models developed at MS&T.

5.5 Implementation of the pilot protection system for the solid state transformer model developed at FSU at both substation type and load type SST [40].

A PSCAD model of substation SST and load SST model was developed at FSU so that the model could be used for PSCAD Green Hub simulations.

The main characteristics of this SST models are.

1. Both the substation and load type SST have current sourcing capabilities, and they can stop sourcing current within a specified time period.

2. The source type SST will source current base on the system and grid voltage at rated conditions.

3. The load type SST will lock/latch into the phase grid voltage and inject voltage at a constant power. (Based on the current for the user defined load).

4. During the fault/on occurrence of fault, both types of SST will source a limited fault current i.e 2 pu and then shut off after certain designated period. (Long enough for the protection system to detect the fault.)

5. On clearing the fault and restoration of fault, both types of SST's must be brought back on line (Reclosing). Reclosing is SST's has not been discussed before sections.

   Based on these characteristics the substation SST and load type SST's are defined below.

1. Substation SST model

The substation SST model on PSCAD is an average model which is basically a current source model. To source the required current the substation SST relies on the error between the pu voltage magnitude and pu voltage reference. A PI controller is used to inject current into the system. The substation SST continues to source the rated/nominal current as long as the current is 2pu.

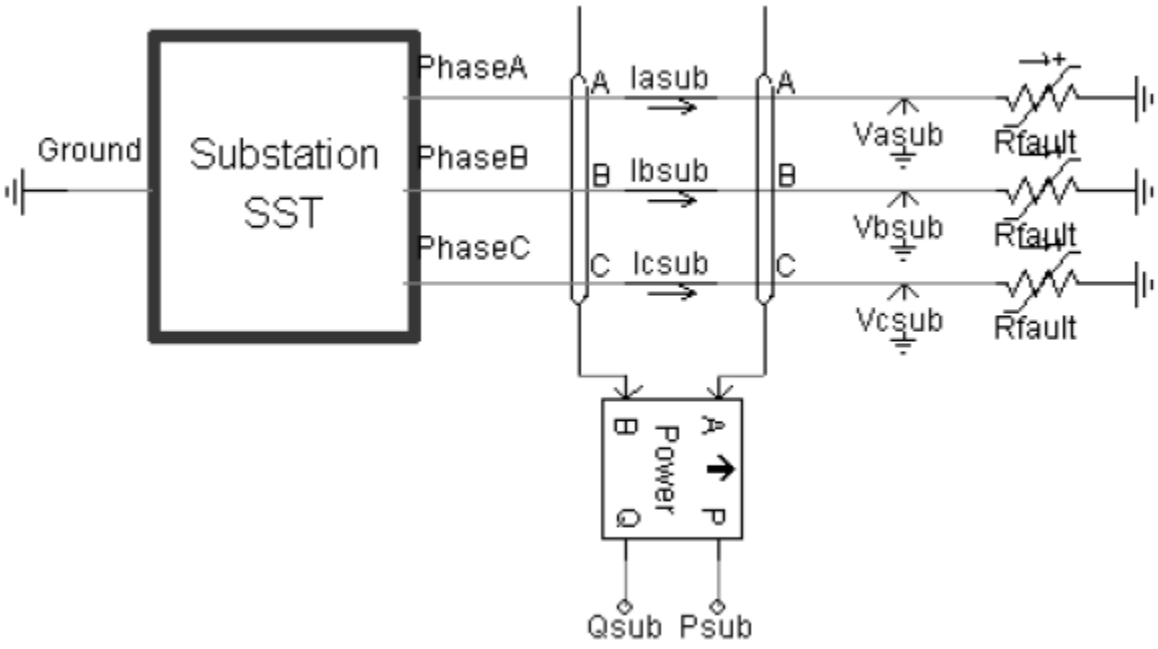


Figure 5.37. Test circuit for the SST model [40]

Here in the figure 5.37 the test circuit for the substation type SST is shown. When the substation SST is connected to R fault. Once the SST model starts sourcing current (up to its limit 2pu) now on occurrence of a fault/or as the impedance/resistance starts falling, the SST will source a current up to the limit of 2pu, also the output voltage falls. The internal logic of the SST has a certain delay logic, in which after the grid voltage falls below 0.8pu, the SST will stop sourcing current. Now for the restarting the SST, the integrator on the PI controller for the SST, must be reinstated or set to the initial value and also the logic with which the current sourcing, must be reset. So when the reset tag is high the under voltage and over voltage systems are neglected by the control logic and it allows for the voltage to return based on injected current under nominal condition i.e. all the faults are cleared.

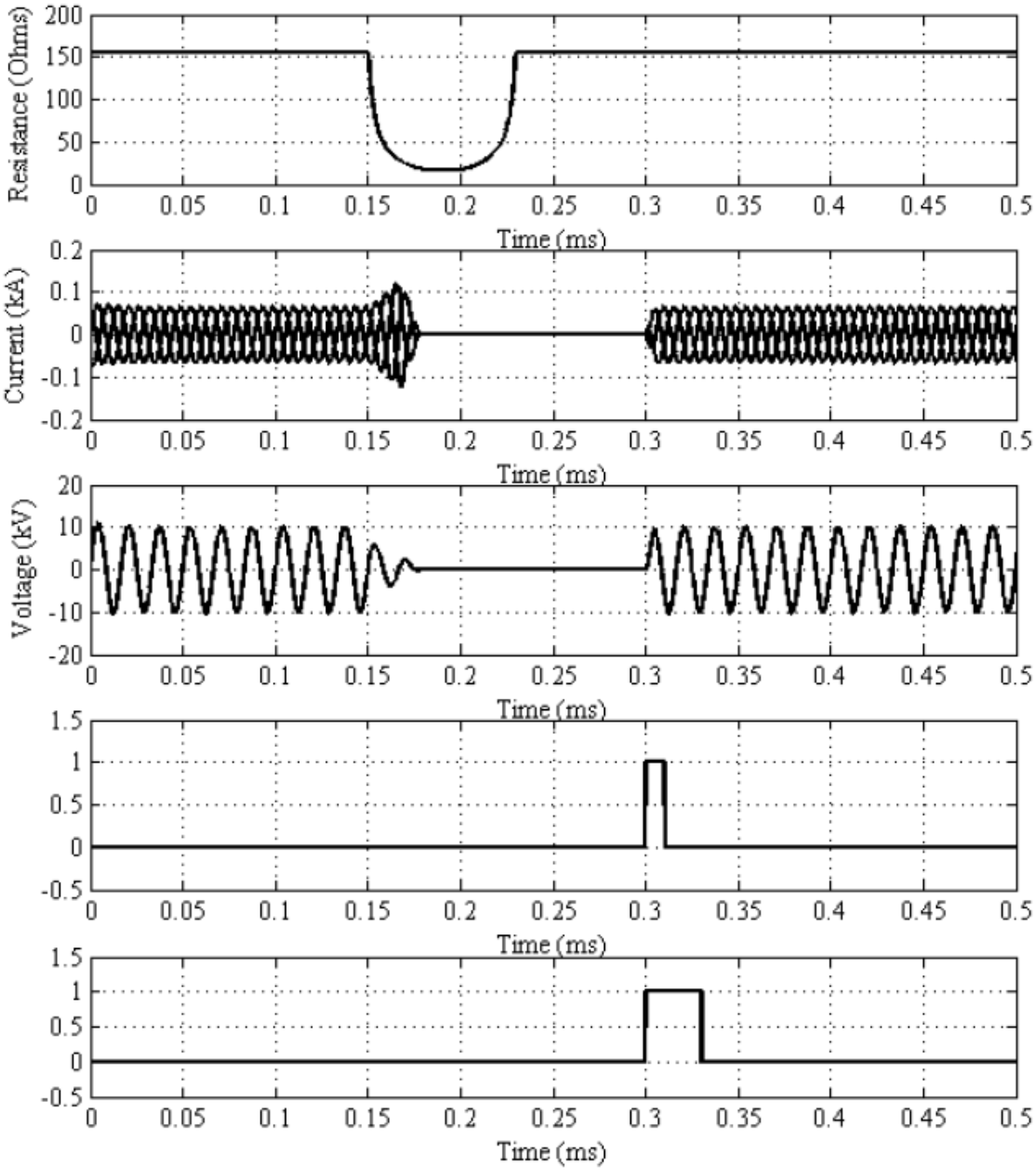

Resistance (Ohms)
200
150
100
50
0
0 0.05 0.1 0.15 0.2 0.25 0.3 0.35 0.4 0.45 0.5
Time (ms)
Current (kA)
0.2
0.1
0
-0.1
-0.2
0 0.05 0.1 0.15 0.2 0.25 0.3 0.35 0.4 0.45 0.5
Time (ms)
Voltage (kV)
20
10
0
-10
-20
0 0.05 0.1 0.15 0.2 0.25 0.3 0.35 0.4 0.45 0.5
Time (ms)
1.5
1
0.5
0
-0.5
0 0.05 0.1 0.15 0.2 0.25 0.3 0.35 0.4 0.45 0.5
Time (ms)
1.5
1
0.5
0
-0.5
0 0.05 0.1 0.15 0.2 0.25 0.3 0.35 0.4 0.45 0.5
Time (ms)

Figure 5.38. Substation SST behavior for faulted condition to check upon injected current I, grid voltage V, PI clear (clearsubtime) and substation SST reset signal (resetsubtime) [40]

Based on the figure 5.38, here you can see that when the fault occurs, the S-SST reset signal is sent so as to restore the SST. Now based on this theory, the pilot protection system successfully can be used to detect a fault and send a signal to the SST for shutting down the sourcing and a reclose signal can be sent by pilot protection module based on the Reclosing algorithm explained earlier. Hence the pilot protection can successfully detect a fault, isolate and restart a substation SST.

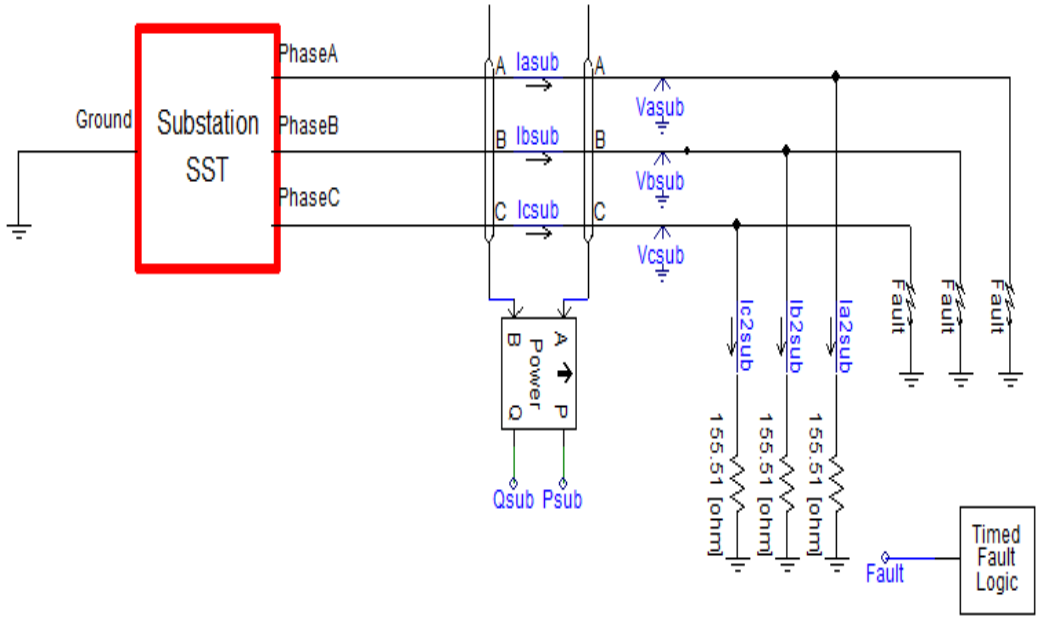


Figure 5.39. Circuit diagram for applying pilot protection to the substation SST

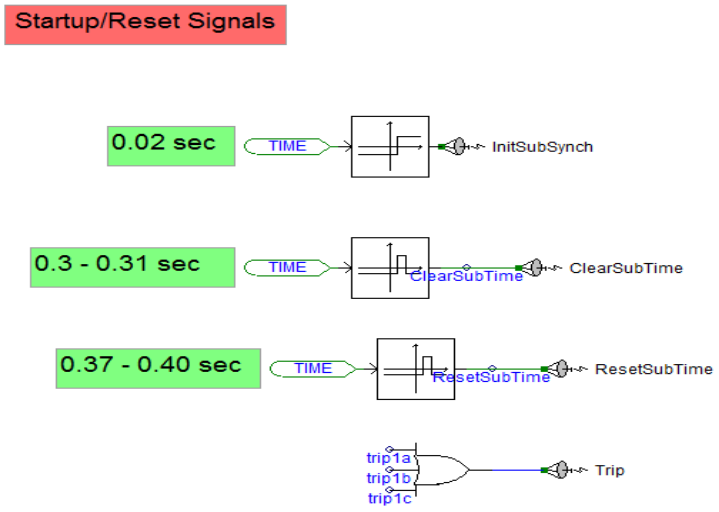


Figure 5.40. Signals required by the substation SST for fault clearing and reclosing

The substation SST has three major signal.

Initsubsynch:

Initial signal given to the start the simulation by sourcing current to the load.

Clearsubtime:

The signal given to the P1 controller to reset and setback to its initial condition

Resetsubtime.

The signal given to the SST to know when to restart

Now for out stimulation instead of the tripping taking place for the SST, when the voltage falls to 0.8 Pu, the trip signal from the pilot protection module is replaced.

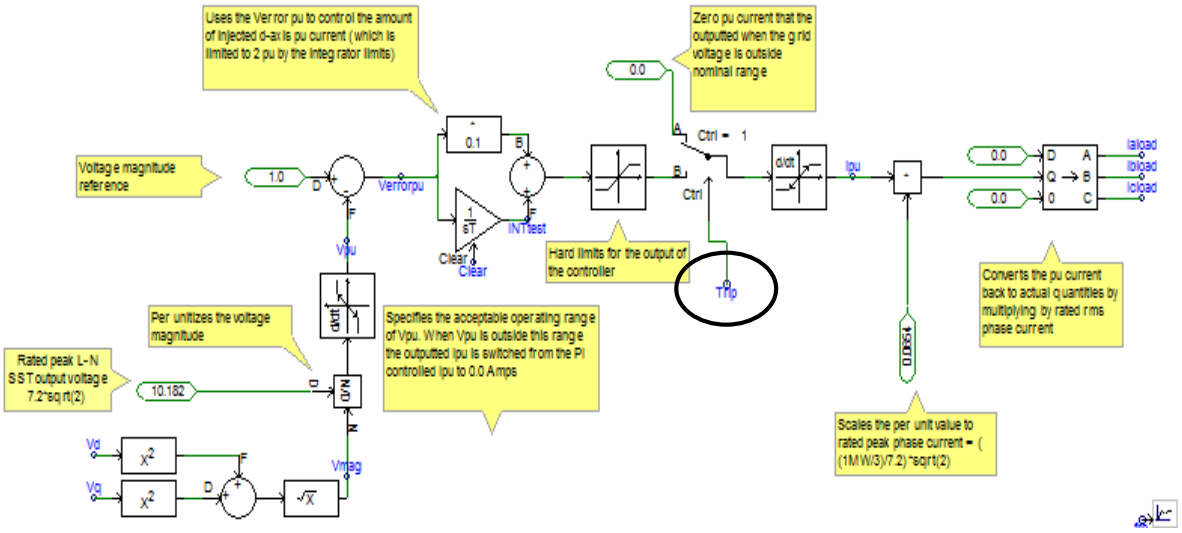


Figure 5.41. Trip signal from pilot protection being utilized for clearing the fault for the substation SST

So instead the SST will stop sourcing current, when the trip is initiated from the pilot protection system. Now for the Reclosing, the Reclosing signal from the pilot protection module is used where in the Reset sub signal is replaced by the Reclosing signal from the pilot protection module i.e. when the Reclosing signal is sent from the pilot protection module, the SST will start up once again. The results for the pilot protection module implementation for substation type SST is shown below.

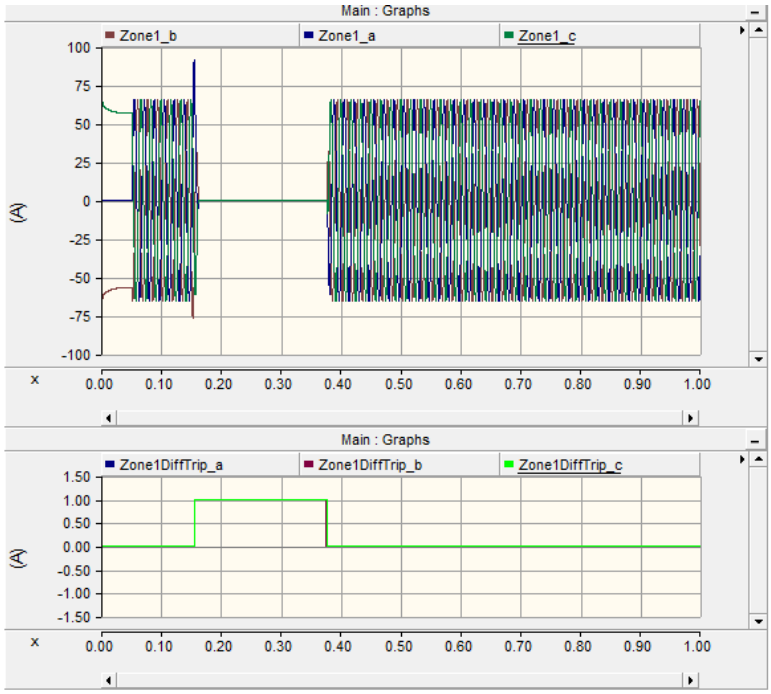


Figure 5.42. The fault is successfully detected at 0.18 second and cleared 0.37 second (successfully) for substation type SST.

2. Load type SST

During normal voltage conditions and system operations, the Load type SST is locked in phase with the grid voltage, Fig. 5.43 below shows that, and sources a current that is dependent on the grid voltage, Fig. 5.44, obtained from a constant power source. As shown in Fig. 5.44, when the grid voltage starts decreasing, the injected current increases based on the load type SST functioning, based on the constant power loading condition, up to its current limits of 2 pu. Once the under-voltage condition barrier is breached, the Load type SST will stop injecting current after a fixed delay. After the voltage comes back up again, a resetting signal is applied.

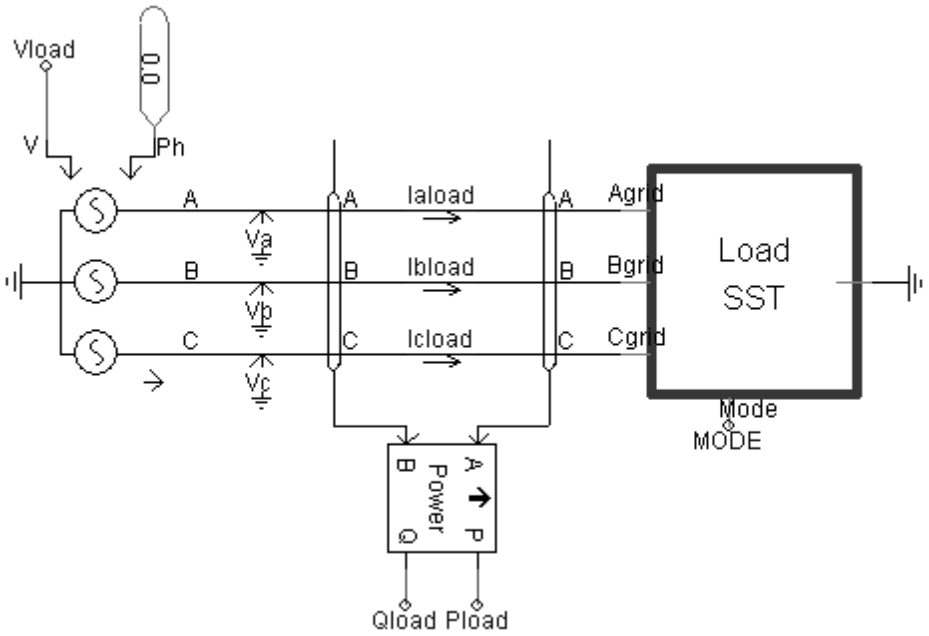


Figure 5.43. Load type SST test circuit [40]

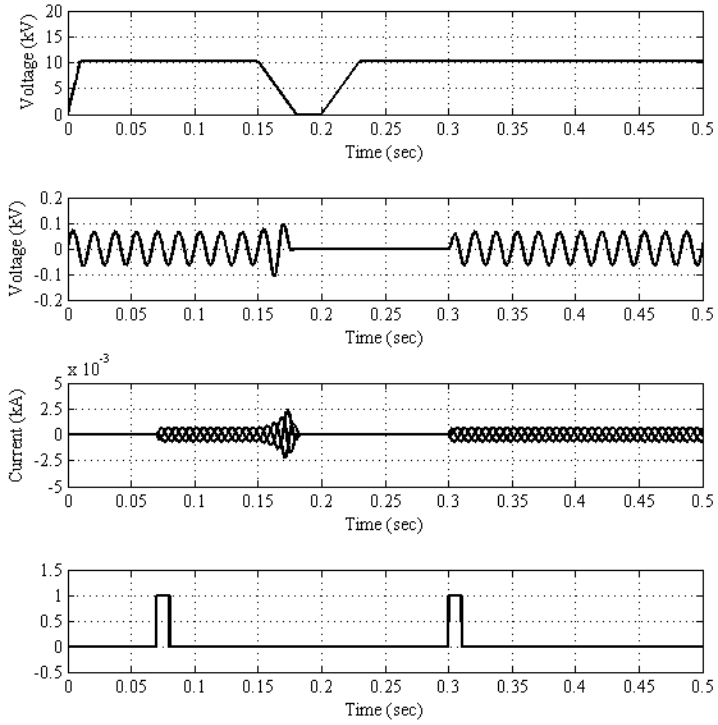


Figure 5.44. Characteristic of the load type SST during faulted condition. User defined grid voltage profile, grid voltage, injected current and the reset signals are shown here [40].

5.6 Modified LSSS model [41]

Utilizing the substation SST and load SST model discussed above the modified LSSS model was made at FSU. Based on the results before the pilot protection system could be implemented for this system.

5.6.1 Modified LSSS Model design [41]

A modified Large Scale System Simulation (LSSS) test bed in here is developed to examine the effect of adding multiple SSTs (both and their interaction in the system is studied. The original IEEE 34 bus system (explained in earlier section) was scaled down from 24.9 kV to 11.9 kVL-L to match the FREEDM loop voltage level, 12 kV L-L, shown in Figure 5.45. Instead of the traditional loads, all the loads are connected to the main bus through D-SSTs (load type SSTs). The main source giving power to the model is connected through the S-SST (substation SST). In the LSSS model obtained from modifying the voltage regulator 1 between nodes 7 and 25 and voltage regulator 2 between nodes 26 and 16 are eliminated in the original IEEE 34 model. The data in Table 5.4. Shows the nodes at which the distributed SSTs are connected. The rating of the load type SSTs is 200 kVA.

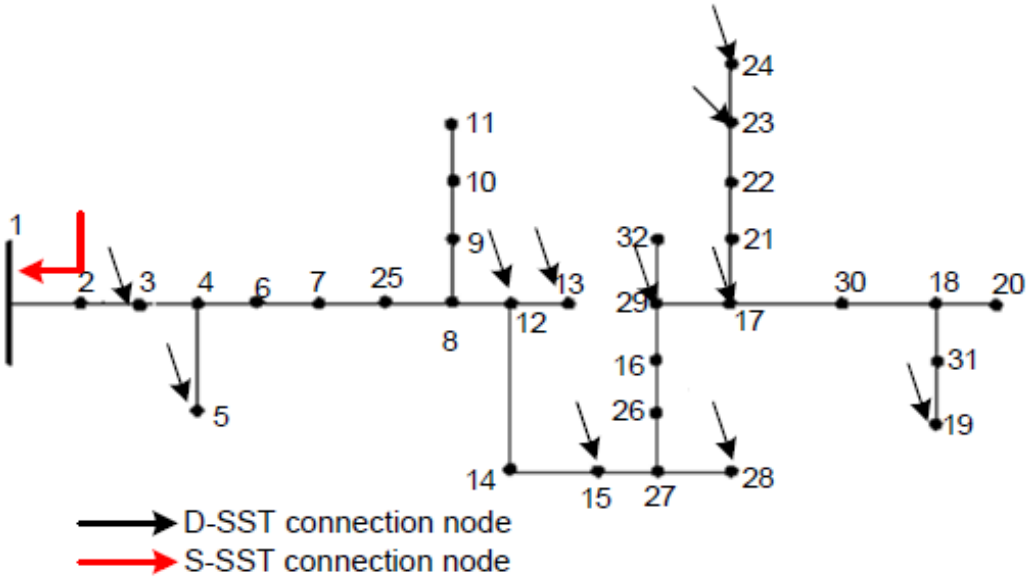


Figure 5.45. Schematic of the modification made to the original IEEE 34 and the placement of D-SSTs is also shown here [41].

Table 5.4. Distribution SST placement on various nodes of the modifies LSSS system [41]

Node	**SST connected**	**Number of SSTs connected**
3	Yes	1
5	Yes	1
12	Yes	1
13	Yes	1
15	Yes	1
17	Yes	1
19	Yes	1
23	Yes	1

24	Yes	1
28	Yes	1
29	Yes	1

System Substation rating: 1MVA/7.2kV

200kVA load SST ratings: only three connected in the system, each should be drawing 1PU load current so that the system voltage can be kept between 0.95 and 1.05PU during normal operation. The voltage will be decreasing from the substation to the end of the feeder.

5.6.2 Results

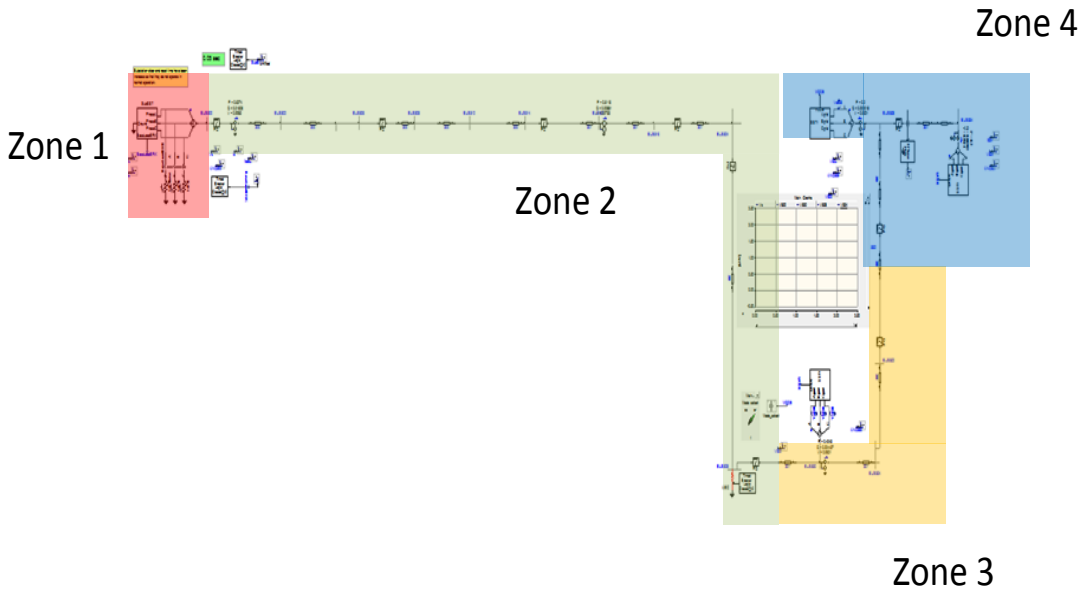


Figure 5.46. Zones of protection for the implementation of the pilot protection system for the modified LSSS loop system [41]. The tests were conducted for all 4 zones. Sampling frequency for the system is kept at 1000 Hz. The results for the various types of faults and the response of the pilot protection system are shown below.

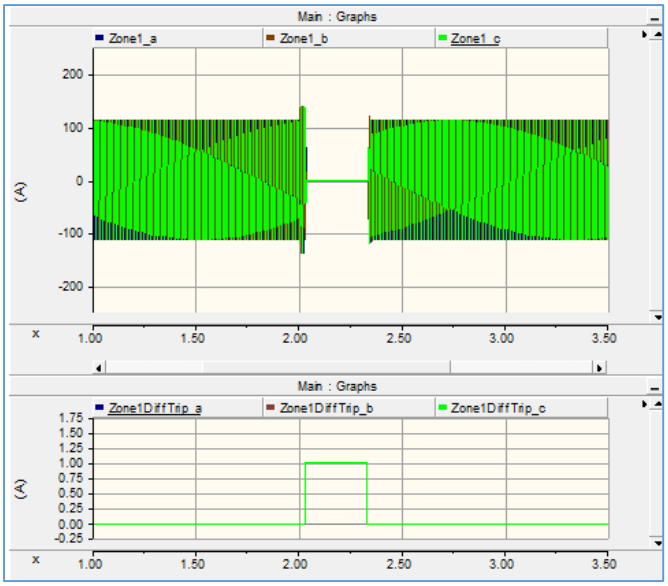


Figure 5.47. Fault Analysis for three phase bolted fault in zone 1

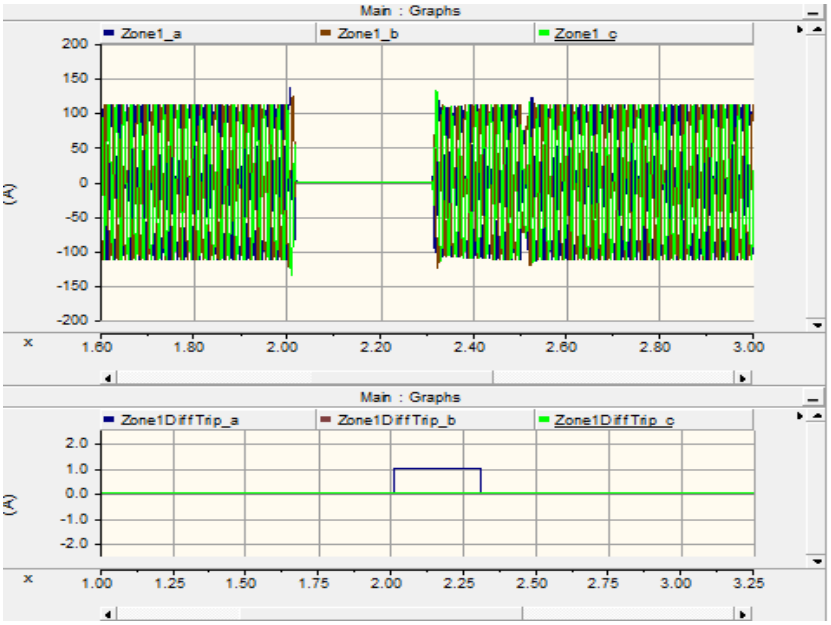


Figure 5.48. Fault Analysis for AB type fault in zone 1

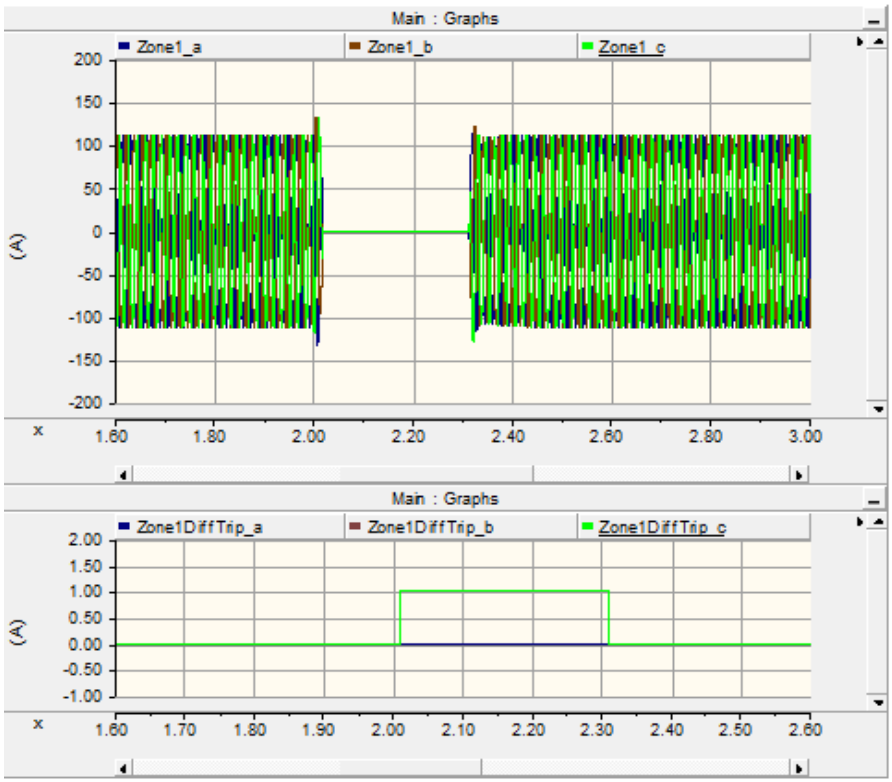


Figure 5.49. Fault Analysis for BC type fault in zone 1

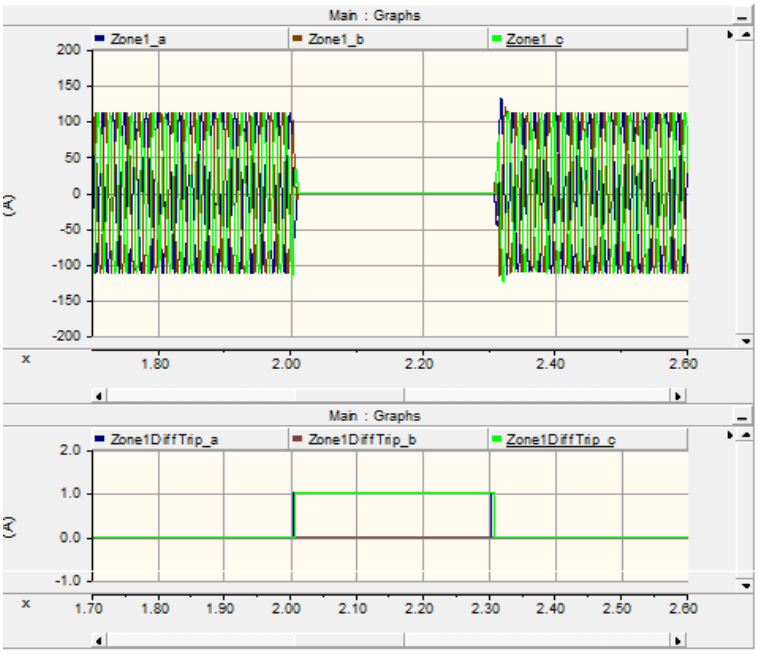
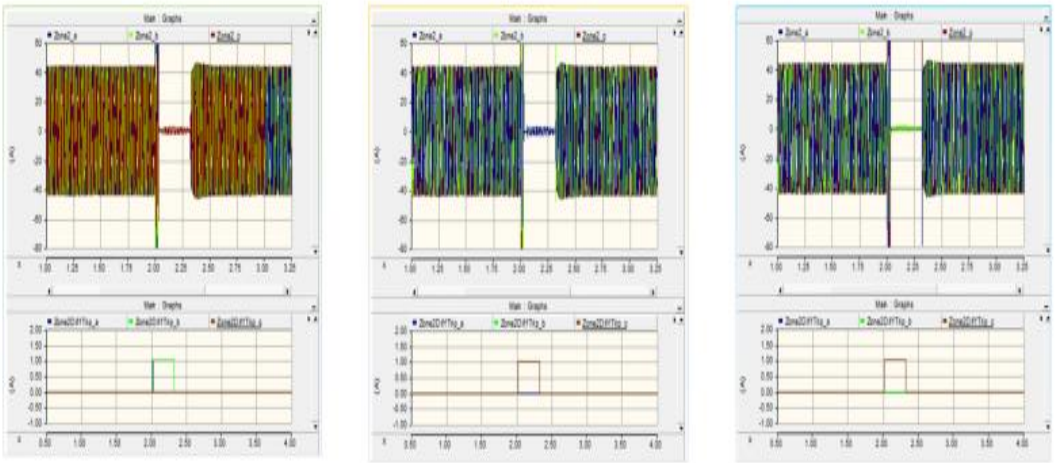


Figure 5.50. Fault Analysis for CA type fault in zone 1

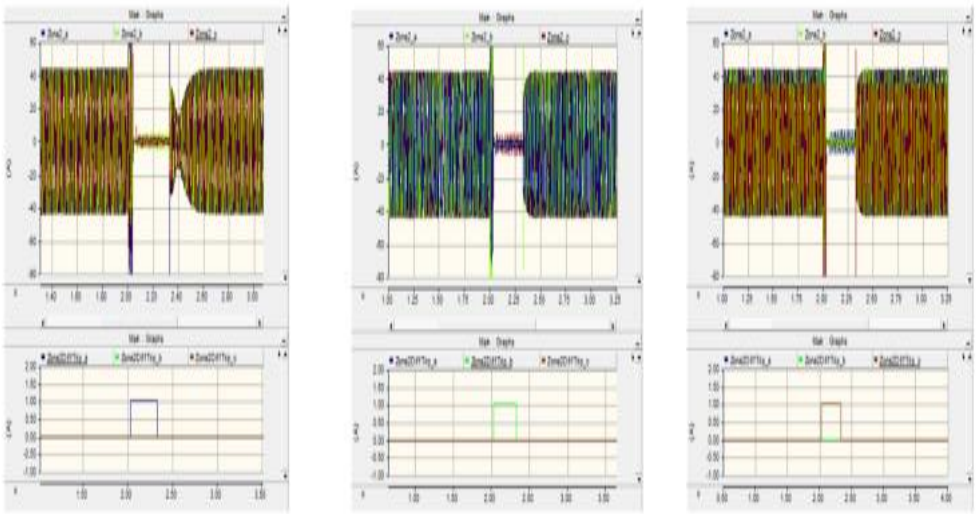


A-B type fault

B-C type fault

C-A type fault

Figure 5.51. Zone 2 faults for A-B, B-C, and C-A Faults



A-G type fault

B-G type fault

C-G type fault

Figure 5.52. Zone 2 faults for A-G, B-G, and C-G Faults

The results show that the pilot protection system is successfully able to detect the fault, clear it and perform reclosing action. The trip detection signal average delay is 5.8 ms, standard deviation is 0.388 ms for a sampling frequency of 1000 Hz for the 3 phase fault in zone 1.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Main Conclusions

The goal of this research work is to modify the previously developed pilot protection system and to implement the pilot protection system with large scale distribution network which include other power electronics components like Solid State Transformer, Fault Isolation Devices just like the FREEDM system which is a smart distribution power network. A new adaptation is done to the existing protection strategy that enables faster, reliable trip times. A very fast protection response time is achieved. For the research works done in this particular project, conclusions can be drawn as follows.

- The new 10 sample rolling window sampler is developed which helps not only in faster trip times but also gives more secured and reliable results with very little standard deviation

- A hardware system based on micro-controller with Ethernet communication is implemented utilizing the new algorithm. The results of this hardware model is compared with software simulation with the same test bed with the exact same data in PSCAD. The results show similar results for both experiments. The details of which are mentioned in [29]

- A new dual slope pilot protection algorithm was also developed and its simulation results on the test bed were compared to the older pilot protection algorithm. The results show that for the same data trip delay time reduces but the reliability increases. The

pilot protection algorithm was also tested for CT saturation and results show that it is able to operate under heavy CT saturation

- The pilot protection was successfully implemented to large distribution system like the Green hub v4.3, IEEE 34 model, LSSS model and the modified LSSS model. The results prove that protection is effective, fast and reliable. Reclosing was also implemented in several of these models. The details of which are in [39].

6.2 Future Work

The future work for this project consists of the following aspects:

- The reclosing model is still not developed for certain distribution networks, this can be implemented once the issue of resynchronizing of the SSTs with the grid on reconnection is solved
- To develop an Ether CAT based system for 8 or more units, which will be sufficient for a protective zone.
- To develop an Ether CAT based system for wireless communication, which will help save expenses on long lengths of Ethernet cable.
- To implement substation communication and protection protocols for the current system like IEC 61850.

List of publications:

- G. G. Karady, *Fellow, IEEE,* Andrew Rogers, Varun Iyengar**,'** Feasibility of Fast Pilot Protection for Multi-Load Distribution Systems, IEEE PES GM 2013.
- V. Iyengar, G. Karady, D. Crow, D. shah 'Implementation of pilot protection system for IEEE 34 load system with SST Loads', FREEDM Industry meeting conference 2014.

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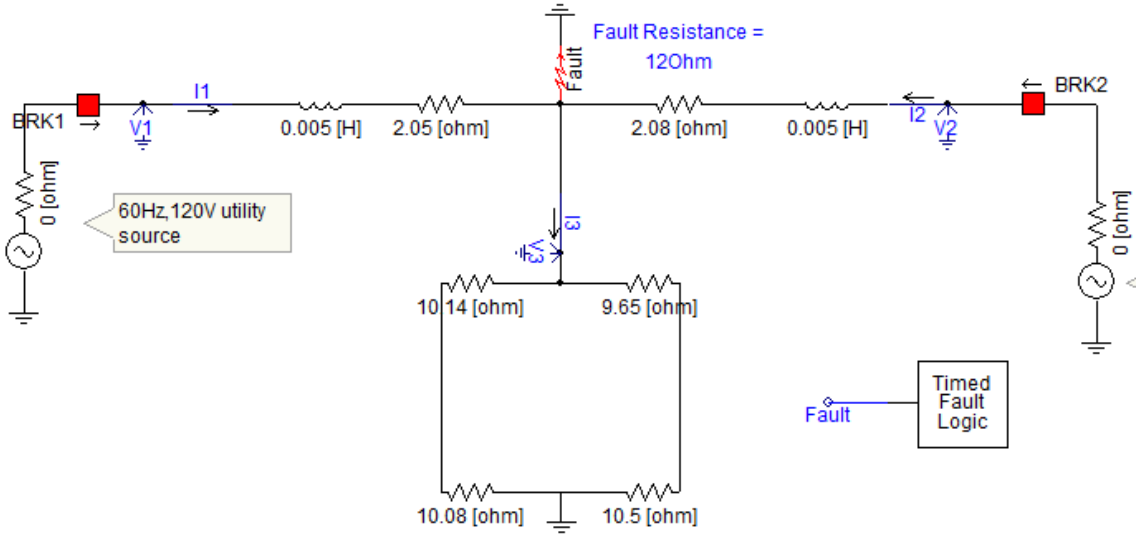
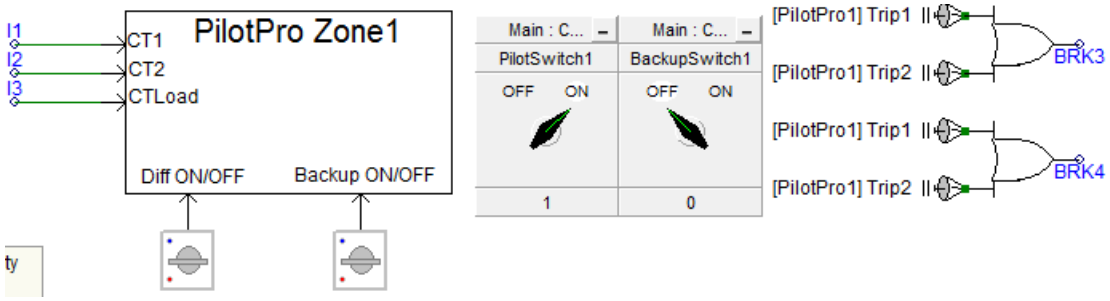
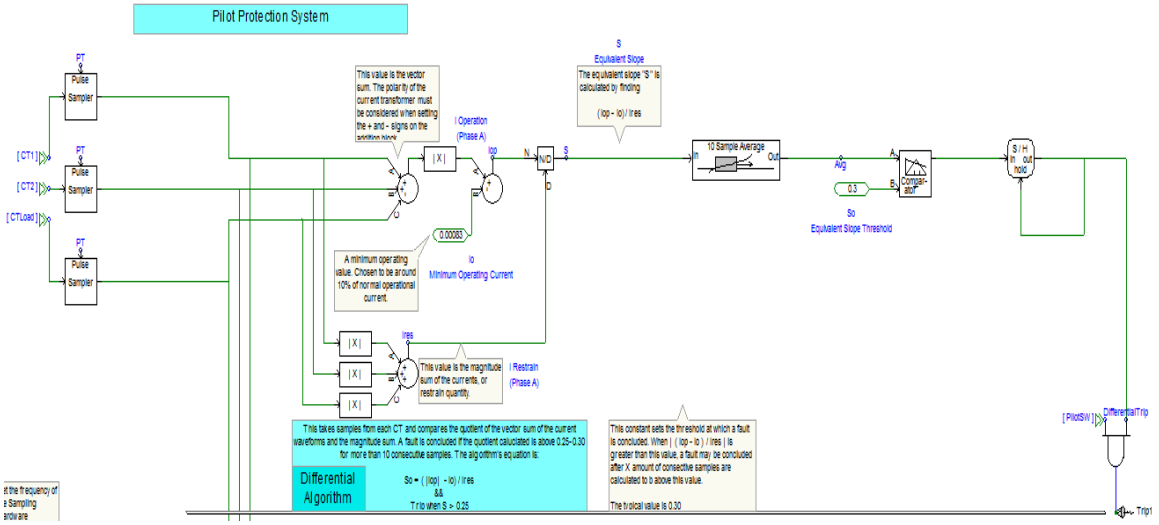
APPENDIX A

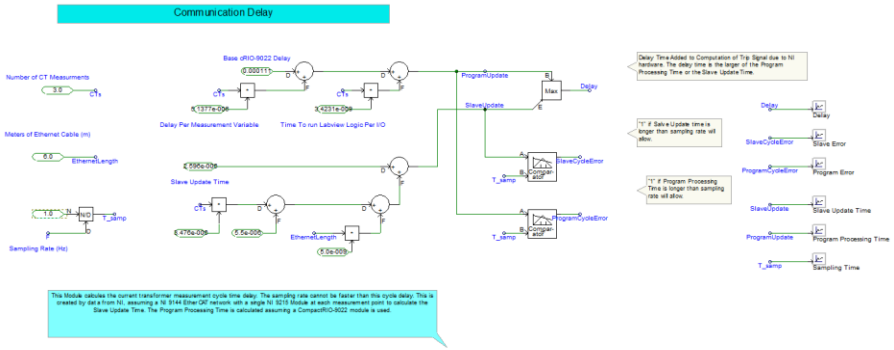
PSCAD SIMULATION FILES FOR CHP 2,3,4

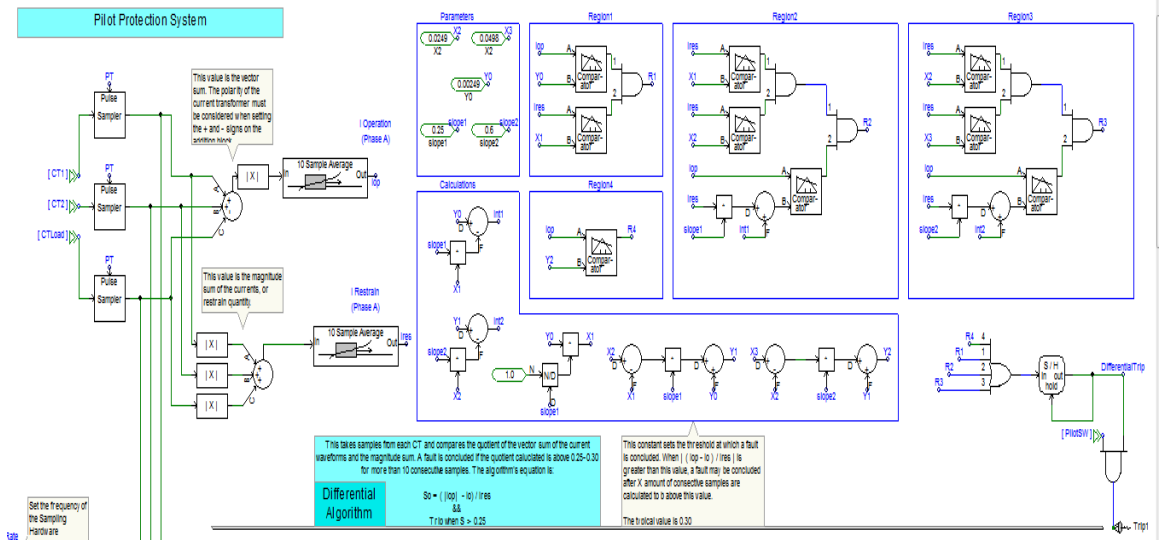
Below shown are the PSCAD simulation files for the test bed system for the rolling window test setup. Also shown are the PSCAD files for the point form and the CT saturation experimental files.

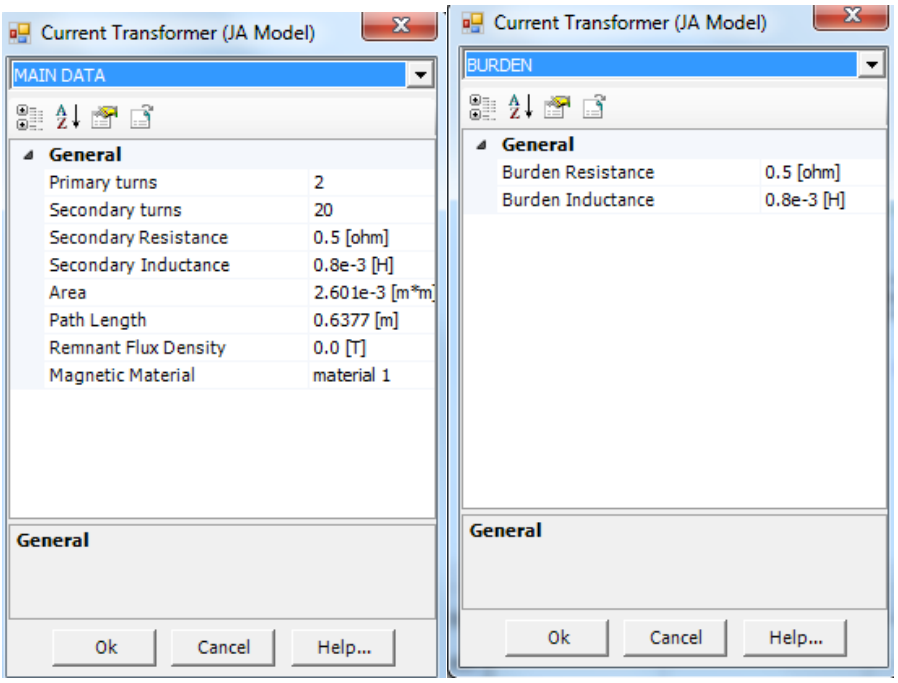





Pilot Protection System
PT
Pulse Sampler
[CT1]
[CT2]
[CTLoad]
This value is the vector sum. The polarity of the current transformer must be considered when setting the + and - signs on the partition block
I Operation (Phase A)
Iop
N
S
D
S
Equivalent Slope
The equivalent slope "S" is calculated by finding
(Iop - Io) / Ires
10 Sample Average
In
Out
Avg
0.3
So
Equivalent Slope Threshold
S / H
In
out hold
0.00083
Io
Minimum Operating Current
A minimum operating value. Chosen to be around 10% of normal operational current.
Ires
This value is the magnitude sum of the currents, or restrain quantity.
I Restrain (Phase A)
This takes samples from each CT and compares the quotient of the vector sum of the current waveforms and the magnitude sum. A fault is concluded if the quotient calculated is above 0.25-0.30 for more than 10 consecutive samples. The algorithm's equation is:
Differential Algorithm
So = (|Iop| - Io) / Ires
&&
Trip when S > 0.25
This constant sets the threshold at which a fault is concluded. When | (Iop - Io) / Ires | is greater than this value, a fault may be concluded after X amount of consective samples are calculated to b above this value.
The tr ical value is 0.30
[PilotSW]
DifferentialTrip
Trip1


Communication Delay
Base cRIO-9022 Delay
Number of CT Measurments
Delay Per Measurement Variable
Time To run Labview Logic Per I/O
Meters of Ethernet Cable (m)
Slave Update Time
Sampling Rate (Hz)
ProgramUpdate
SlaveUpdate
Delay
SlaveCycleError
ProgramCycleError
Delay Time Added to Computation of Trip Signal due to NI hardware. The delay time is the larger of the Program Processing Time or the Slave Update Time.
"t" if Slave Update time is longer than sampling rate will allow.
"t" if Program Processing Time is longer than sampling rate will allow.
Slave Error
Program Error
Slave Update Time
Program Processing Time
Sampling Time
This Module calcules the current transformer measurement cycle time delay. The sampling rate cannot be faster than this cycle delay. This is created by dat a from NI, assuming a NI 9144 Ether CAT network with a single NI 9215 Module at each measurement point to calculate the Slave Update Time. The Program Processing Time is calculated assuming a CompactRIO-9022 module is used.


Pilot Protection System
Parameters
Region1
Region2
Region3
Region4
Calculations
PT
Pulse Sampler
[CT1]
[CT2]
[CTLoad]
This value is the vector sum. The polarity of the current transformer must be considered when setting the + and - signs on the partition block
I Operation (Phase A)
10 Sample Average
This value is the magnitude sum of the currents, or restrain quantity.
I Restrain (Phase A)
This takes samples from each CT and compares the quotient of the vector sum of the current waveforms and the magnitude sum. A fault is concluded if the quotient calculated is above 0.25-0.30 for more than 10 consecutive samples. The algorithm's equation is:
Differential Algorithm
So = (|Iop| - Io) / Ires
&&
Trip when S > 0.25
This constant sets the threshold at which a fault is concluded. When | (Iop - Io) / Ires | is greater than this value, a fault may be concluded after X amount of consective samples are calculated to b above this value.
The tr ical value is 0.30
[PilotSW]
DifferentialTrip
Trip1


Current Transformer (JA Model)
MAIN DATA
General
Primary turns 2
Secondary turns 20
Secondary Resistance 0.5 [ohm]
Secondary Inductance 0.8e-3 [H]
Area 2.601e-3 [m*m]
Path Length 0.6377 [m]
Remnant Flux Density 0.0 [T]
Magnetic Material material 1
General
Ok
Cancel
Help...
Current Transformer (JA Model)
BURDEN
General
Burden Resistance 0.5 [ohm]
Burden Inductance 0.8e-3 [H]
General
Ok
Cancel
Help...

APPENDIX B

PSCAD SIMULATION FILES FOR CHP 5

Below shown are the PSCAD simulation files for the GreenHub test bed system, IEEE34 , LSSS loop and the modified LSSS for the rolling window algorithm.