Total Dose Simulation for High Reliability Electronics

by

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ABSTRACT

New technologies enable the exploration of space, high-fidelity defense systems, lighting fast intercontinental communication systems as well as medical technologies that extend and improve patient lives. The basis for these technologies is high reliability electronics devised to meet stringent design goals and to operate consistently for many years deployed in the field.

An on-going concern for engineers is the consequences of ionizing radiation exposure, specifically total dose effects. For many of the different applications, there is a likelihood of exposure to radiation, which can result in device degradation and potentially failure. While the total dose effects and the resulting degradation are a well-studied field and methodologies to help mitigate degradation have been developed, there is still a need for simulation techniques to help designers understand total dose effects within their design.

To that end, the work presented here details simulation techniques to analyze as well as predict the total dose response of a circuit. In this dissertation the total dose effects are broken into two sub-categories, intra-device and inter-device effects in CMOS technology. Intra-device effects degrade the performance of both n-channel and p-channel transistors, while inter-device effects result in loss of device isolation. In this work, multiple case studies are presented for which total dose degradation is of concern. Through the simulation techniques, the individual device and circuit responses are modeled post-irradiation. The use of these simulation techniques by circuit designers allow predictive simulation of total dose effects, allowing focused design changes to be implemented to increase radiation tolerance of high reliability electronics.

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experience many great things growing up, and always there for me. Erica, you have been a great big sister, and I can truly say you are a best friend. Finally, to the love of my life Marisa, our journey has only just begun. While we may only be on our first stop along the way, I'm so very excited to see where life takes us next. To all I love you and thank you.

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CHAPTER 1

INTRODUCTION

High Reliability Electronics

High reliability electronics are at the heart of some of the greatest technological advancements today. From deep space exploration, telecommunications, aerospace and defense as well as implantable medical devices, highly reliable electronics allow assurance that critical systems will operate as designed for the duration of their intended lifetime. Scientists, medical doctors and engineers will continue to employ electronics to advance society, exploring our universe, enabling lighting fast communications as well as extending and improving quality of life. As new technologies come to fruition, it is imperative that they are as reliable as possible.

It is important to understand the commonalities among high reliability electronics. First, high reliability electronics are mission-critical and cannot easily be replaced in the field. One can see the difficulty of replacing a failed integrated circuit on a satellite in space or a medical device implanted in a patient. High reliability electronics are also expected to operate within design specifications over multiple years. Another characteristic of high reliability electronics is that they are often manufactured at low volumes. Due to the nature of their applications, specifically space, defense and medical, high reliability electronics are not fabricated in the same volume as the majority of commercial electronics. Finally high reliability electronics can also have longer design cycles compared to commercial electronics, sometimes lasting tens of years.

While many applications can fall under the categorization of high reliability electronics, we focus here on medical devices. This emphasis is chosen since radiation effects within medical device electronics is a growing concern; and, moreover, the

majority of the work presented here was performed specifically for medical device applications. However, the techniques developed and presented are believed to be widely valid, appropriate for implementation as part of a design-for-reliability program in other applications and environments.

Medical Devices

In the last 60 years, the world has seen development of implantable medical devices that serve to improve patient quality of life. This has led to the development of a multi-billion dollar industry. Through collaboration between medical professionals and engineers, implantable device technology has evolved into complex systems capable of such activities as patient monitoring, drug delivery, neurological stimulation and support of heart function through artificial pacing and defibrillation [1]. These devices currently serve to treat a wide array of diseases, and continued breakthroughs in the medical and engineering fields will expand their usage going forward [2-4].

All electronics designed for medical devices are constructed with a primary goal of increased battery life through ultra-low power consumption while maintaining a high standard of reliability. In fact, reliability and device lifetime are the primary product differentiation factors [4]. Today, the U.S. Food and Drug Administration (FDA) regulate medical devices to ensure quality and protect patients. Field failures of implanted devices are unacceptable, as a fault could require device replacement involving surgery or, in extreme cases, put the patient's life in danger. Great care is taken in the front-end design and qualification process to ensure a reliable product.

Since the medical device market is rather low volume in comparison to the commercial electronics industry, medical device companies have employed a "fast follower" approach by leveraging new integrated circuit (IC) processes only after they have been developed by higher volume industries such as consumer electronics. This approach allows for medical device companies to have a better understanding of product reliability and reduce development times.

IC designs are primarily fabricated in silicon based CMOS processes due to the low standby power consumption and high device reliability. The continued tracking of CMOS technology with Moore's Law has allowed designs to increase the complexity of systems without swelling power consumption or device size. Additionally the integration of multiple functional blocks into a single system-on-a-chip (SOC) serves to limit current draw in comparison to older designs, which relied on inter-chip communication in the system requiring more power. As device feature size shrinks at each successive technology node, overall maximum supply voltage shrinks as well. However, with decreased supply voltage, the device threshold voltage is also lowered. This is undesirable as reduction in threshold voltage leads to increased off-state leakage. So, selection of the CMOS process must balance the benefits of shrinking feature size with the requirements of ultra-low power consumption.

Another undesired aspect for the medical device industry related to shrinking geometries is the reduction in standard gate oxide thickness. Most if not all pacemaker designs require the use of large output voltage (5-20V) for pacing, for which the newest technology nodes' ultra-thin gate oxides cannot reliably support. To solve this issue many companies employ technologies that provide devices of different gate oxide thicknesses

within the standard process. This allows circuit designers the option to use transistors with thicker oxides for use in high voltage output sub-circuits while still having the opportunity to employ thin gate oxide transistors in lower voltage digital sub-circuits. The requirement of thicker oxides and high circuit voltages is deleterious when considering susceptibility to ionizing radiation, as will be shown and discussed in Chapter 2.

A typical pacemaker device uses a non-rechargeable battery as the system's sole power source. Battery supply voltage is usually targeted near 3 V with design considerations made to accommodate an end-of-life battery voltage reduced as low as 1.7 V. To maximize battery life, all systems operate at currents as low as 10 μA and a leakage for off-state transistors targeted to be less than 1 pA per micrometer of gate width. This is a difficult task as system designs often include a microcontroller IC, on-chip read only memory (ROM) with static random access memory (SRAM), a mixed-signal IC for biological sensing and generating output signals, a protection IC to shield against interference, a large SRAM for storage of diagnostic data and possibly very-high voltage electronics for generation of defibrillation signals [5].

The main figure of merit for implantable medical devices, specifically pacemakers, is the device's expected lifetime and reliability. Many of the reliability concerns of implantable device designers are not exclusive to the medical device field. These include the deleterious device effects of gate-induced drain leakage (GIDL), stress-induced leakage current (SILC), negative-bias temperature instability (NBTI) as well as other material and packaging related reliability concerns [4-7]. However, many of these concerns are well monitored and are of utmost consideration during the front-end design

process. Additionally, all devices undergo stringent qualification and “burn-in” testing to check for defects before reaching doctors and surgeons for use in patients.

However one area of medical device reliability that has not been significantly explored by medical device engineers is the effect of radiation on implanted devices. Exposure of implanted devices to ionizing radiation is possible during diagnostic x-rays or through the use of radiation therapy for cancer treatment. Traditionally, the effects of ionizing radiation in semiconductor devices and integrated circuits were a concern for engineers designing for space and nuclear applications only. However, as implantable devices continue to grow in usage, there is a need to address radiation effects in these devices in more depth.

Currently, some pacemaker device manufacturers list relatively low thresholds (1-5 Gy) for acceptable device exposure levels, with some manufacturers stating that no level of exposure is acceptable [8]. Therapeutic dose for tumor treatment can range from 10 to 70 Gy, although it is assumed that the pacemaker device will see only a fraction of the total dose, thus should maintain full functionality [9]. It is considered “best practice” to avoid directly exposing the device to radiation during cancer therapy, with many recommendations going as far to say that patients with implantable medical devices need to have their pacemakers relocated, or that the plan of cancer therapy should be re-evaluated to avoid radiation exposure [10-12]. Numerous clinical studies which test commercial pacemaker devices for their radiation tolerance report mixed results [8, 13-15].

Generally it is concluded that the use of radiation therapy for patients with implantable devices is safe, but only if extreme caution is taken. Additionally,

recommendations are made to a) consider other treatment options, b) surgically relocating the device, c) attempt to exclude the pacemaker from the radiotherapy portal and d) attempt to calculate dose to the pacemaker. It is also recommended that device manufacturers make radiation data for their devices more readily available.

The drawback of most clinical studies of radiation effects on implantable medical devices is that they all approach the problem from a medical perspective. The studies focus on a "pass/fail" methodology for device performance post-irradiation, only monitoring external electrical signals as would be seen by the heart. As such, they do not explore radiation effects on internal circuitry to analyze the true effect of ionizing radiation and consider if latent reliability issues exist, or if the expected device lifetime has been significantly reduced. If design specifications such as current draw are affected and exceed specification after exposure, battery life would be reduced and surgical replacement of the pacemaker could potentially be needed years earlier than originally predicted.

As the medical technology, surgical techniques and device designs advance the likelihood that implanted devices will see increased exposure levels during therapy could increase. This necessitates preemptive steps be taken to improve device radiation tolerance. The primary reason ionizing radiation effects warrant serious consideration in implantable electronics is the nature of device technologies and designs, specifically:

- Medical devices must utilize technologies with thicker dielectrics and lower doping levels. It is well known that these properties make high voltage MOS technologies more susceptible to ionizing radiation [16].

- Higher voltage requirements of pacemaker sub-blocks such as voltage multiplication circuitry and high voltage output generators result in larger electric fields throughout the circuit, particularly in the device oxides, which will enhance radiation-induced defect buildup [17, 18].
- Ionizing radiation is known to cause increases in off-state currents, reduce threshold voltage in n-channel devices and cause parasitic inter-device leakage [16], all of which are damaging to the low-power consumption design goals.
- Tolerance of field failures of implantable devices is unacceptable and the consequences are severe. Radiation induced failures, or even battery life degradation, could result in surgical replacement of devices and put patient health in jeopardy.

The mechanisms of ionizing radiation effects in CMOS integrated circuits are explored in detail in Chapter 2, while the remainder of this work describes methodologies to analyze ionizing radiation effects at the device and circuit levels, with the end result being circuit simulation techniques that capture radiation response characteristics. The capability for predictive radiation effects simulation allows designers to examine sensitive circuitry, and enables design changes to be made early in the product development process that would serve to increase radiation tolerance.

Total Dose Hardening Approaches

Chapter 2 will provide details on total dose effects in CMOS technologies, and later chapters will illustrate the impact of total dose on devices and circuits. However, it

is important to briefly highlight the effects here before reviewing radiation-hardening approaches. Total dose effects in CMOS devices can be placed in two categories: intra-device and inter-device effects. Intra-device effects consist of total-dose induced degradation of both the gate oxide as well as the isolation oxide sidewalls. These mechanisms are classified intra-device as both affect the drain-to-source current-voltage characteristics within a field effect transistor (FET). Specifically, gate oxides are degraded by buildup of both positive oxide trapped charge as well as interface traps. Oxide trapped charge is also a significant issue in isolation oxide sidewalls of n-channel field effect transistors (NFETs), resulting in parasitic off-state drain-to-source current from conduction along the isolation oxide sidewall. Buildup of oxide-trapped charge is also the root cause of inter-device effects, as charge buildup along the base of isolation oxides results in the undesired loss electrical isolation.

To mitigate the total dose effects, many methods and approaches have been developed to increase radiation hardness. However this does not mean that a given hardening technique is always appropriate for all applications. Engineers must consider the dose level expected, the likelihood of exposure, as well as the place total dose reliability concerns in context with other design and reliability goals. This section outlines current methods that can be used to increase radiation hardness.

Hardening by Process

Radiation hardened foundries, have been developed specifically to produce radiation-resilient circuits via specially tuned manufacturing processes. For applications in which a high total dose can be anticipated (i.e. deep space missions and defense

applications), utilization of radiation-hardened processes are common. However, these processes are not generally accessible for commercial purposes, and often restricted only to government and military design groups. Additionally, utilization of trusted foundries can be highly cost prohibitive due to the low-volume nature of their business.

Commercial processes, however, offer inherent radiation hardening through device scaling. The semiconductor industry's continued respect for Moore's law has led it to continually scale devices at each successive technology node. This scaling has reduced oxide thickness so much that positive charge trapping within ultra-thin gate oxides is now uncommon, as will be detailed in Chapter 2. This benefit is widely exploited for hardening purposes, as transferring designs into a scaled technology node not only improves general circuit performance but also improves total dose hardness [16, 19] [19]. Additionally, as device geometry has scaled, supply voltages in new technology nodes have also been scaled, as ultra-thin oxides cannot support voltages above their dielectric breakdown limit. Scaling of supply voltages is advantageous from a power perspective; so many applications gladly exploit all benefits related to porting circuit designs to smaller technology nodes.

However, hardening by process options are often impractical for manufacturers of integrated circuit applications in which total dose hardening is not the most critical reliability concern, for example implantable medical devices. Due to the low-volume nature of "rad-hard" foundries, they are often highly cost prohibitive for all except cases where extreme radiation tolerances are required. Since medical device radiation exposure levels are expected to be low, rad-hard processing is not a prudent option. As described previously, current commercial state-of-art technologies have been shown to be more

radiation tolerant than older processes. However, medical device designs still require high device reliability and ultra-low power consumption. Additionally, high voltage design requirements preclude the use of the most advanced technologies, as ultra-thin oxides cannot support these supply voltages. Due to these stringent requirements, medical device manufacturers adopt a "fast follower" approach to new technologies, and will not adopt a new process unless thoroughly vetted [4, 5, 7].

Hardening by Design

Radiation hardening can also be accomplished in circuit design, utilizing layout and operation specifications to mitigate total dose radiation effects. Compared to radiation hardening by process, radiation hardening by design (RHBD) can be considerably less expensive and can be implemented on a per-design basis. Many of these strategies are realized through adherence to process design kit design rules, implemented throughout the entire design.

As mentioned previously, intra-device effects consist of degradation of either (or both) the gate oxide or the isolation oxide sidewall. Mitigation of gate oxide degradation is best handled via process hardening as described previously. However, designers can also limit the damage to gate oxides by limiting electric fields within the oxides during exposure, as the field dependency degradation is a well-known effect [18, 20]. This is accomplished by minimizing transistor-gate-to-body bias. However, one can see the limitation of this strategy, as modifying circuit operation (i.e. completely powering off the circuit) at the instance of exposure in the field is impractical or impossible. Completely powering off a potentially application-critical system is obviously

undesirable. In theory, a designer could design low-bias “safe mode” for critical sub-circuits, to be triggered during exposure to limit damage. To this end, predictive simulation of total dose degradation like that presented in this dissertation would empower designers to anticipate damage and design in safe modes.

The other intra-device effect to be mitigated is parasitic off-state drain-to-source leakage due to oxide-trapped charge in NFET isolation oxide sidewalls. As this is a predominant total-dose effect, much work has been performed to mitigate this effect by way of specialized NFET device layout. The parasitic current post-irradiation is due to the proximity of the isolation oxide sidewall to the NFET channel. Buildup of oxide trapped charge in the sidewall results in parasitic current in parallel to the as-drawn NFET channel. So-called “enclosed gate” layouts have been demonstrated to be significantly more resilient to total dose effects, as isolation oxides are moved away from the NFET channel, mitigating the intra device parasitic current. However this strategy comes with area and performance penalties, as enclosed gate NFET layouts are significantly larger than a standard layout. The increase in layout area then, in turn, degrades transistor performance through increased gate capacitance; reducing device switching speed. However the effectiveness of enclosed gate layout designs for total dose hardening is undeniable.

Inter-device effects between n-type regions on-chip can also be effectively mitigated via layout modifications. The addition of “channel stops” to field regions surrounding a transistor will prevent leakage between devices. The channel stop is implemented via a highly doped p-type diffusion, which raises the local threshold voltage significantly. Even with significant oxide trapped charge buildup in the isolation oxide

base, the local threshold voltage in the region remains high, eliminating currents between inter-device n-type regions. Mitigation via channel stops also comes at a cost, as cell area is increased when this additional layout element surrounding the transistors is included [19, 21, 22].

In one published study, hardening by design is implemented on a two-input NAND cell, utilizing edgeless transistors and p+ guard rings to mitigate intra- and inter-device total dose effects, as seen in Fig. 1.1 [21]. In this study, it was shown that the implementation of RHBD strategies in a 0.35 µm technology dramatically increased the cell size. It was found that the total cell area of the RHBD NAND cell has increased by 73%, and was comparable in size to a NAND from a 0.5 µm technology. Additionally, it was found that the power dissipation (in µW/MHz) had increased 120% for the RHBD NAND compared to the unhardened 0.35 µm NAND cell. While effective in mitigating TID effects, the penalties are evident.

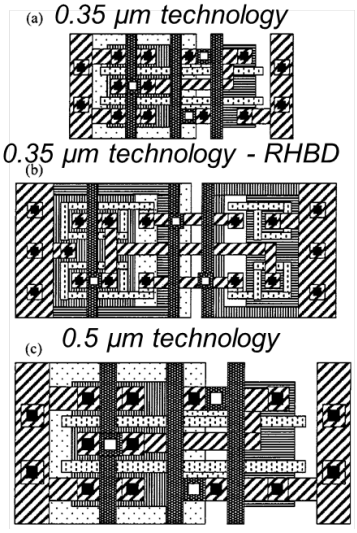


Fig. 1.1 Example of a 2 input NAND cell. Examples of an unhardened (a) and a Radiation Hardening by Design (b) cell in a 0.35 µm technology. For reference an unhardened (c) cell in 0.5 µm technology is shown [21].

It is apparent widespread implementation of hardening by design techniques will impact the size and performance of any circuit. In cases for which a large total dose in the application is expected and unavoidable, hardening by design is an absolute necessity. However, in cases for which total dose levels may be lower and exposure is not guaranteed, such as in implanted medical devices, designers may choose not to sacrifice for radiation hardening. Because of these reasons, medical device manufacturers are advised to implement radiation hardening by design in a strategic and measured fashion. By making the most minimally invasive design and layout changes, while working within current circuit design goals and constraints, a targeted level of radiation tolerance can be achieved. In this work, modeling techniques are presented to both replicate and predict total dose response of circuits in simulation. Designers then can use these simulations early in the development cycle and implement measured RHBD design changes to improve total dose hardness while maintaining other design goals.

Approach and Goals

The dissertation is divided into six chapters, focusing on total dose effects and their impact on circuits. The early chapters serve as introduction and motivation for the work, establishing the need for simulation of total dose effects as part of a design-for-reliability approach. The remaining chapters focus on describing and validating simulation techniques to successfully capture the various effects of total dose degradation within the normal circuit simulation design flow. Case studies presented to provide real-world examples of both the degradation that can occur, as well as provide perspective to the simulation methodologies.

Chapter 2 discusses the effects of ionizing radiation, and its damaging effect on CMOS circuits. A brief history is presented, covering the establishment of the radiation effects field. Then the physics of total dose damage are described, explaining how ionizing radiation degrades silicon dioxide. The effect is then correlated to its effect on the electrical operation of CMOS devices and circuits. Understanding the basic physical mechanisms of total dose degradation establishes a basis for the simulation techniques presented in the following chapters.

Chapter 3 focuses on simulating the effects of inter-device effects related to total-dose irradiation. A case study, completed as part of my Master's Thesis, is reviewed, setting the stage for follow-up work completed to further analyze inter-device effects [23]. In a presented case study, an analysis of a dual charge pump circuit, radiation-induced charge buildup in the base of LOCOS isolation oxide results in inter-device current flow between NFETs and the n-type substrate. This loss of isolation leads to collapse of the charge pump output voltage, which serves as a primary supply rail for the rest of the circuit. Through a combination of experimental, modeling and simulation techniques the observed voltage collapse of the charge pump circuit is reproduced. Follow up work is then presented, in which specialized total-dose test structures were created to analyze the parasitic transistors in depth. This study serves as a guide for the modeling and simulation of inter-device total dose effects in other applications.

In Chapter 4 a ring oscillator case study is presented, showcasing another primary outcome of total dose degradation in CMOS technologies; intra-device effects such as threshold voltage shifts and increased off-state leakage. In the case study of interest the combined effect of both NFET and p-channel field effect transistor (PFET) threshold

voltage shifts, along with parasitic inter-device edge leakage in the NFET lead to changes in oscillation frequency and supply current draw in the ring oscillator. The novel analysis methodology presented successfully investigates the observed response, replicating it via simulation. Not only does this give greater insight into the operation of the ring oscillator, the techniques and findings are useful in the analysis of oscillators in other applications. Additionally the use of a ring oscillator as a health monitor circuit is proposed.

Chapter 5 is a special circumstance of design-for-reliability analysis, for which no irradiation characterization data is available. Instead, a combination of TCAD modeling, analytical extraction and compact modeling techniques allow for predictive modeling of potential post-irradiation inter-device edge leakage. Predictive datasets generated from the technique provide inexpensive and rapid access to potential reliability pitfalls in a given circuit design. This allows designers to make hardening changes on-the-fly improving radiation hardness early in the design cycle.

The final chapter recaps the dissertation, discusses my contributions, and suggests future work. With respect to my contributions, the primary goals are to:

- Detail total dose simulation techniques which are verified on real-world case studies, but widely applicable in other process technologies and designs.
- Advance the use of commercially available processes for high reliability applications. Total dose simulation techniques like those presented could be implemented in a design for reliability flow making commercial processes a cost effective yet trustworthy option for high-reliability designs.

- Illustrate the use of simulation techniques and TCAD modeling as a rapid yet effective substitute for experimental data, which can be expensive and time consuming to acquire.
- Empower those designers to increase total dose hardness of designs without being experts in the radiation effects field. Make simulation techniques easily accessible for application to new designs early in the design cycle.

CHAPTER 2

TOTAL DOSE EFFECTS

Brief History

Research on the effects of ionizing radiation has been ongoing for more than 60 years, studying the consequences of exposing electronics to harsh environments, like space and nuclear systems. Work began after the failure of seven satellites in 1963. On July 9th, 1962 the Atomic Energy Commission and Defense Atomic Support Agency detonated a thermonuclear warhead above Johnson Island in the South Pacific Ocean. This experiment and similar nuclear tests by the Soviet Union were identified as causes of an increased amount of nuclear particles in the Earth's Van Allen belt [24-27].

It was later determined that the failure mechanism for the satellites could be attributed to the ionization of particles in the bipolar transistor packages, leading to trapped charge accumulating on the silicon die surface. This resulted in increased leakage currents, causing circuit failure [24]. At that time, it was believed that complementary metal-oxide-semiconductor (CMOS) transistors would be more radiation tolerant compared to bipolar transistors; as their transfer characteristics are not dependent on minority carrier lifetime [26]. However, testing of CMOS device radiation sensitivity at the Naval Research Laboratory (NRL) in 1964 revealed otherwise. It was reported that both n- and p-channel MOS devices exhibited sensitivity, which was linked to buildup of oxide-trapped charge and interface traps in device oxides [28, 29]. These results motivated the federal government to fund multiple research groups to investigate radiation effects and their impact on military space systems.

In the 1970s programs were established to develop radiation hardened CMOS integrated circuits. Sponsored by the Defense Nuclear Agency, these programs focused

on altering gate dielectrics through oxide growth techniques; annealing and doping modifications [28]. Additionally during this time, electronic spin resonance (ESR) on CMOS silicon dioxide films at NRL helped identify the primary damage mechanism, which was related to oxygen vacancy defects in silicon dioxide [28, 30]. Through the collaborative work of numerous research groups, the basic mechanisms of total dose degradation in silicon dioxide were identified.

Over time, the scaling of state-of-the-art digital technologies has reduced gate oxide thicknesses to less than a few nanometers. This has made degradation of gate oxides caused by ionizing radiation exposure in CMOS less of a concern. However for designs that require thicker gate oxides such as mixed-signal, power CMOS and Flash Memory, threshold voltage shifts in gate oxide MOS systems are still a major concern [31-33]. Moreover, even thicker isolation oxides are still significantly affected by ionizing radiation in modern CMOS devices, making inter-device leakage, so-called device "edge" leakage, a continued limitation to the radiation tolerance of commercial processes [16, 19, 34].

Effects of Total Dose Irradiation

Ionization is the process for which exposure to radiation in solid-state materials causes electrons to be liberated from atoms in a material. This occurs through the absorption of energy in the material from charged particles (i.e., electrons, protons, alpha particles, and heavy ions) and/or high-energy photons [35]. The quantity of energy converted into ionization can be determined by the linear energy transfer (LET) function, which gives the energy loss per unit length (dE/dx) of a particle in a given material. LET

is a function of the mass and energy of the particle as well as the target material density. The LET is expressed in units of MeV-cm^2/g, or in simple terms, the energy loss per unit length normalized to the density of the material exposed [35, 36]. Fig. 2.1 illustrates the LET in SiO_2 versus particle energy for electrons, protons, and secondary electrons generated by 10 keV x-rays and 1.25 MeV ^{60}Co γ-rays [37].

The interaction between charged particles and a material generates electron-hole pairs (ehps) that lead to direct ionization. Alternatively, ionization due to photons is indirect. During indirect ionization ehps are created along the track of secondary electrons emitted during the photon interaction with the material. In both indirect and direct ionization, the density of ehps generated along the tracks of the charged particles is proportional to the energy transmitted to the material [38].

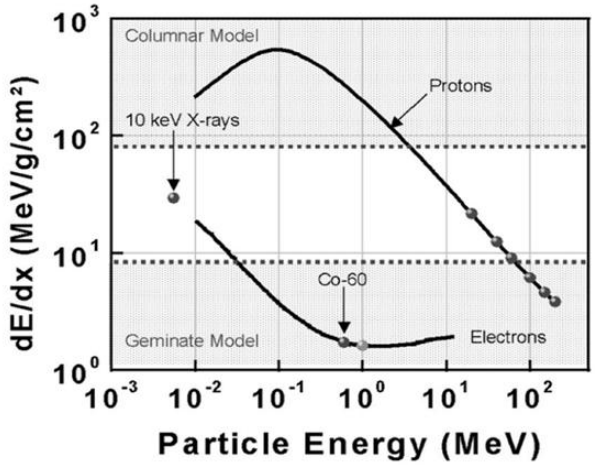


Fig. 2.1 LET in SiO_2 vs. particle energy for electrons, protons, and secondary electrons generated by 10 keV x-rays and 1.25 MeV ^{60}Co γ-rays [37].

Energetic secondary electron generation from photon exposure occurs through three different processes. The dominant process depends on the photon energy and the material exposed. For low-energy photons (~10-100keV) interacting with SiO_2, the photoelectric effect dominates as a photon excites an electron to a high enough state to be emitted free

of the atom. For higher energy photons (0.1-10MeV) the Compton effect dominates. Similar to the photoelectric effect, a photon excites an electron to a higher, free state. However, with Compton scattering, a lower energy photon is also created, which is free to interact with other atoms. Pair production occurs only at very high photon energies (>3MeV). In this process the high-energy photon creates an electron-positron pair. The positron has the same properties as an electron, except that the charge is positive [18].

The total amount of energy deposited by a particle that causes the generation of ehps is quantified as total ionizing dose (TID). A typical unit of TID is the rad (radiation absorbed dose)**,** which signifies the energy absorbed per unit mass of a material (1 rad = 100 ergs absorbed per gram of material) [36]. The SI unit for TID is a gray (1 Gy = 100 rad). Gray is the commonly used while discussing ionizing radiation in medicine; however the rad is the conventional unit used by the electronic radiation effects community.

In SiO_2, immediately after the generation of electron-hole pairs, many of the electrons rapidly transport out of the dielectric leaving behind the slower holes. Depending on the electric field in the oxide during exposure, some electrons will recombine with holes. The fraction of the holes that do not recombine is known as the fractional hole yield. These remaining holes will transport along localized states in the oxide. During this transport process, some of the holes will be trapped, forming positive oxide-trapped charge, primarily near the SiO_2-Si interface. Additionally, during the hole hopping and the charge trapping processes, hydrogen ions (protons) can be released. These ions can also drift or diffuses to the interface where they can cause the formation

interface traps in the silicon bandgap. These four processes are illustrated in Fig. 2.2 [18, 35].

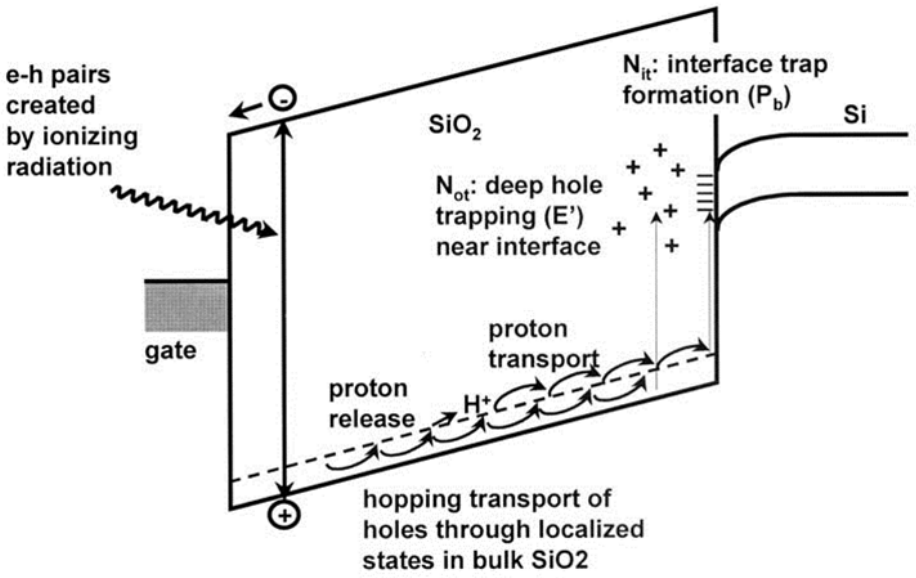


Fig. 2.2 Energy band diagram of MOS capacitor which illustrates the main processes for radiation induced charge generation [18][35].

Charge Yield

The four processes of ionizing radiation induced charge generation are all the result of conversion of dose (energy absorbed per unit mass of the material) into the generation of ehps. The amount of free holes generated can be expressed analytically using the following formula [18, 39]:

$$N_h \left[\frac{\#\ ehp}{cm^2}\right] = f_y(E_{ox}) g_o D t_{ox}, \qquad (2.1)$$

which gives the total number of holes generated per unit area of the material, N_h, as a function of the charge (or hole) yield, $f_y(E_{ox})$, the pair density conversion factor, g_o, the dose, D, and the oxide thickness in centimeters, t_{ox}. This equation is can be easily

understood when related to the qualitative description the four processes illustrated in Fig. 2.2.

As described above, part of the energetic particle's kinetic energy is transferred to the material for ehp generation. The minimum energy required for creating an electron-hole pair, E_p, depends on the bandgap of the material. The pair density conversion factor, g_0, which relates ehps generated to total dose can be calculated using following formula: [40]:

$$g_o\left[\frac{\#\ ehp}{cm^3 \cdot rad}\right] = 100\left[\frac{erg}{g}\right]\left[\frac{1}{rad}\right] \cdot \frac{1}{1.6\times10^{-12}}\left[\frac{eV}{erg}\right] \cdot \frac{1}{E_p}\left[\frac{\#\ ehp}{eV}\right] \cdot \rho\left[\frac{g}{cm^3}\right] . \qquad (2.2)$$

The relationship between ionization energy, material density, and generated carriers are listed in Table 2.1 for both Si, and SiO_2 [18, 39].

Table 2.1 Minimum electron-hole pair creation energy, density and pair density generated per rad for a given material [18, 39]

Material	E_p (eV)	Density (g/cm^3)	Pair density, g_o ($ehp/cm^3 \cdot rad$)
Silicon	3.6	2.328	4×10^{13}
Silicon Dioxide	17	2.2	8.1×10^{12}

Once the generation of ehps has occurred, a fraction of the ehps are almost immediately annihilated through either columnar or geminate recombination [38]. The fraction of ehps that avoid initial recombination is the charge yield, f_y. If an electric field is present during this process, it separates electrons and holes and reduces recombination. It then follows that charge yield is dependent on the magnitude of the local electric field in the material. The charge yield can be approximated as

$$f_y(\vec{E}) \approx \left(\frac{|\vec{E}|}{|\vec{E}|+E_0}\right) \quad , \qquad (2.3)$$

where $\vec{E}$ is the local field vector and E_0 is the threshold field constant (= 5.5 × 10^5 V/cm) [20, 40]. For two common radiation sources used for experimental testing, ^{60}Co gamma rays and 10 keV x-rays, $f_y(\vec{E})$ can be expressed as [41],

$$f_y(\vec{E})_{\,Co-60} = \left(\frac{0.55}{|\vec{E}|} + 1\right)^{-0.7} \tag{2.4}$$

and

$$f_y(\vec{E})_{x-ray} = \left(\frac{1.35}{|\vec{E}|} + 1\right)^{-0.9}, \tag{2.5}$$

respectively, where the local field vector ($\vec{E}$) is expressed in units of MV/cm. The charge yield is plotted for various radiation sources in Fig. 2.3 [18, 20, 40].

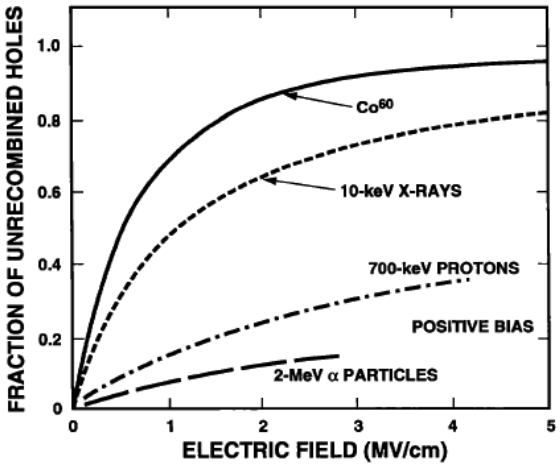


Fig. 2.3 Fraction of uncombined holes vs. electric field for various incident particles [18, 20, 40].

It is of note that the fractional hole yield plotted in Fig. 2.3 actually increases with decreased energy of the incident or secondary particle. This can be explained by observing that a strongly ionizing particle forms dense columns of charge, in which the ehp recombination rate is high because of the decreased average spacing between pairs

[18]. It is also obvious in Fig. 2.3 that with increased electric field the probability of recombination decreases.

Hole Transport

After ehp generation and initial recombination, the holes and electrons that do not recombine can transport through the silicon dioxide due to the local electric field. Since electrons have a higher mobility (e.g., μ_n = ~20 cm^2/Vs at 300K) they are able to transport out of the oxide, on the order of picoseconds [35, 36, 42]. However holes have a lower mobility (μ_p = ~1.6 × 10^{-5} cm^2/Vs at 300K), and consequently remain in the oxide for much longer periods. Holes still transport through the oxide, some toward the SiO_2-Si interface. However, this process is a great deal slower than electron transport, and is temperature and electric field-dependent [40].

As holes transport through the oxide, they causes a distortion of the localized potential field in the lattice due to their charge, as described by the continuous-time-random-walk (CTRW) hopping transport formalism [43, 44]. This model suggests that holes move by hopping between localized shallow trap states in the oxide. As a hole transports through the oxide, it causes distortion of the local lattice in the SiO_2 layer. This distortion also serves to increase the effective mass of the hole and decrease its mobility. The combination of the charged hole and its strained field is known as a polaron; and it is said that hole transport occurs through the lattice via "polaron hopping" [40, 44].

Once the trap depth increases past a certain limit, there is a possibility the hole could become trapped, where they form the previously mentioned positive oxide-trapped charge (N_{ot}). These trapping sites are thought to be primarily the result of neutral oxygen

vacancies in the SiO_2 (E' centers) [45, 46], although other works have proposed that hydrogen containing defects in the oxide may also trap holes [47, 48]. Reactions between holes and defects in the oxide can also lead to the creation of interface traps (N_{it}) [49]. The nature of positive oxide-trapped charge and interface traps generated due to ionizing radiation will be discussed further in later sections.

Positive Oxide Trapped Charge

Holes generated via ionizing radiation can transport toward the SiO_2-Si interface in the presence of a positive gate bias. Due to lattice mismatch and the out-diffusion of oxygen, there are a large number of oxygen vacancies near the interface [50]. These vacancies can also be thought of as "excess" silicon near the interface that did not completely oxidize during fabrication. As the holes approach the interface, these vacancies trap some fraction of the holes. This fraction is a function of the capture cross section of these defect precursors. The capture cross section depends strongly on the fabrication process, as fraction of trapped holes can vary from ~3% for radiation hardened processes to as high as 50-100% for soft oxides [18].

Two oxygen vacancy defect types play a role in the transportation toward the interface and subsequently trapping of the hole as positive oxide-trapped charge. These defects, or E' centers, are classified as either E'_δ or E'_γ centers [16]. The E'_δ center is a shallow trap that impacts hole transport, as most of the E'_δ centers have energies located in the SiO_2 bandgap less than 1.0 eV from the oxide valence band. Alternatively, the E'_γ center is a deep trap, located at energy levels greater than 3 eV above the oxide valence band, and is responsible primarily for fixed positive charge buildup in the oxide [39]. Fig.

2.4 illustrates an energy band diagram of SiO_2 showing of the main E' centers and their relative position in the oxide.

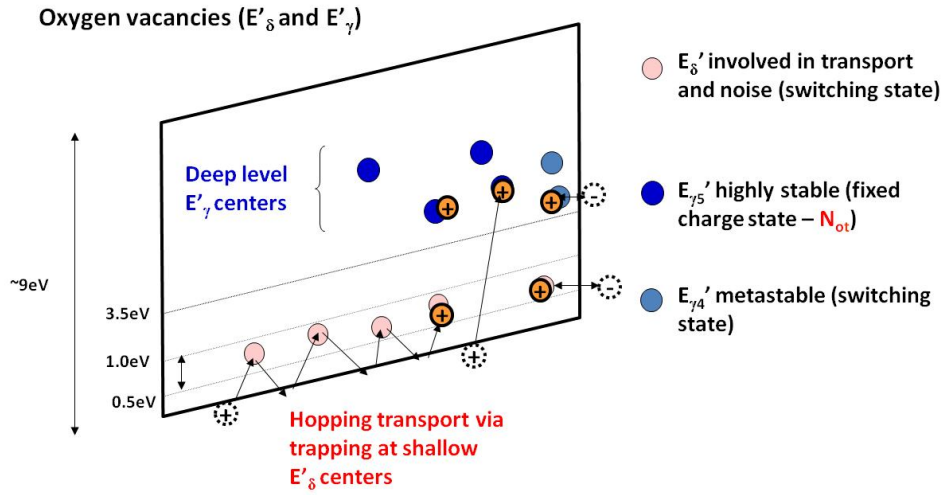


Fig. 2.4 Band Diagram of SiO_2 illustrating possible oxygen vacancies [39].

Following the trapping of charge in the oxide, neutralization of the charge can occur. The rate at which charge neutralization occurs has been shown to be time, temperature and electric field dependent. It is found experimentally that the voltage shift due to oxide-trap charge (ΔV_{ot}) exhibits logarithmic decrease in magnitude as a function of time during post-irradiation anneal. Additionally this logarithmic decrease is shown to be independent of the irradiation dose rate, however the magnitude of total recovery (total decrease in magnitude of ΔV_{ot}) is highly process dependent with some commercial processes exhibiting little charge neutralization [18, 51]. Elevated temperature anneals have shown that that for some technologies neutralization is a strongly thermally activated process, with time to 50% neutralization varying by approximately an order of magnitude between anneal temperatures of 25°C to 125°C [18, 51]. Finally charge neutralization shows a strong bias dependency, with experimental data indicating that it is

possible for charge neutralization under a large positive bias during anneal to be double that of neutralization seen in an unbiased anneal [18, 52].

It has also been illustrated in experiments that some of the charge neutralization seen is reversible by switching to a negative anneal bias. This indicates that the defect centers associated with the oxide-trapped charge are still present after anneal, and some of the appeared neutralization is actually just charge compensation [18]. There are two physical mechanisms that are used to describe the time, temperature and bias dependence of charge neutralization seen in experiment. Charge neutralization can occur from the tunneling of electrons from the silicon or the thermal emission of electrons residing in the oxide valance band to the oxide traps. The effects on transistor operation caused by positive-oxide trapped charge will be discussed further in this chapter.

Interface Traps

Ionizing radiation also produces interface traps, which form in the silicon bandgap. Since the radiation induced traps are develop physically at the SiO_2-Si interface, traps can either be charge positive, neutral or negative as the trap easily donates or accepts electrons from the silicon, subject to the trap location in the bandgap and the applied external bias. Interface traps that fall in the upper half of the silicon bandgap, i.e., above the intrinsic Fermi energy, are generally considered acceptor-like. For these defects, if the Fermi level is above the trap energy level, the defect accepts an electron from the silicon and is negatively charged. If the trap energy falls in the lower half of the bandgap, i.e., below the intrinsic Fermi energy, the defects are typically denoted as donor-like. For donor-like traps, if the Fermi level is below the trap level, an electron is

donated to the silicon leaving behind a positive charge. If the intrinsic Fermi energy is equal to the Fermi level at the interface (a midgap voltage is applied to the gate), there is no net charge contributed by the interface trap [18].

Interface states resulting from ionizing radiation exposure are identified as dangling bond defects called P_b centers [39, 53]. These P_b defects are classified by two center types, P_{b0} and P_{b1}. P_{b0} centers are common to the (111) silicon surface, with the dangling bond defect extending normal to the oxide. The P_{b1} center is closely related to the P_{b0} defect but common to (100) silicon [39]. A graphical representation of the two common defect centers is provided in Fig. 2.5.

The build-up of interface traps following irradiation is a relatively slow process, with trap generation occurring in seconds to thousands of seconds after exposure. It is believed trap formation occurs by way of a two-step process. The process begins in a similar fashion to that of the oxide-trapped charge formation, with the ehp generation due to ionization. Again, the fraction of holes that do not immediately recombine are capable of transport through the oxide. As previously discussed, the hole can be trapped or it may interact with oxide defect centers containing hydrogen (DH centers). These defect centers are found to be naturally occurring in the oxide or formed during fabrication processing. This results in the release of positively charged hydrogen atoms, also known as protons (H^+) [47, 54]. It is thought that the majority of the protons are released when a hole is captured or released from a hydrogen-passivated oxygen vacancy during the hole hopping process [54]

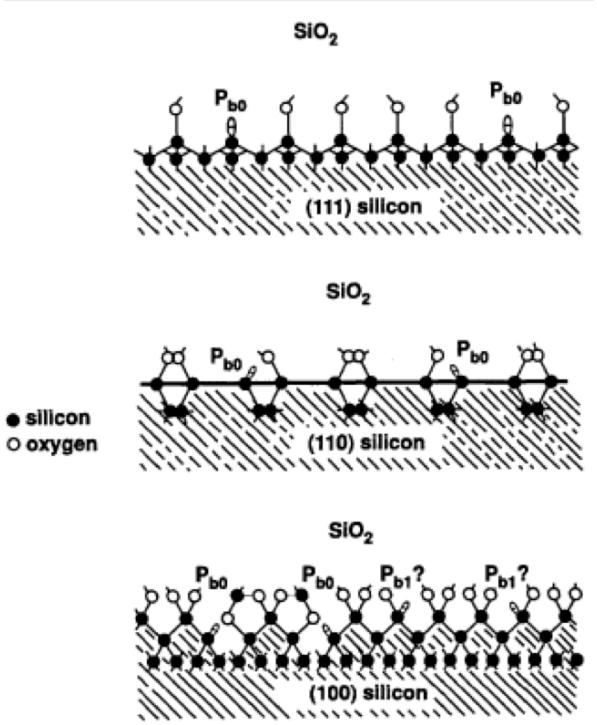


Fig. 2.5 Model of P_{b0} and P_{b1} interface trap centers on (111), (110) and (100) silicon [39, 55].

The released proton (H^+) can transport toward the interface in a manner similar to the hole hopping process under the influence of a positive electric field. At the interface the protons can serve to break the Si-H bonds, form in H_2 and a dangling Si-bond. This reaction can be expressed as [39, 49],

$$SiH + H^+ \rightarrow D^+ + H_2. \tag{3.6}$$

The product of this reaction is an interface trap defect (D^+). As discussed previously, the interface traps (N_{it}) can interchange charge with the silicon due to the close proximity of the trap to the interface, leaving no barrier to charge exchange. The use of hydrogen is prevalent during CMOS processing thus the possibility of hydrogen-passivated silicon dangling bonds is highly likely.

Device Response Considerations

Effects on Gate Oxides

Both positive oxide-trapped charge and interface traps resulting from ionizing radiation can be seen manifested in the DC characteristics of both n- and p-channel MOSFETs as a reduction of the threshold voltage and increase in the subthreshold swing. This is illustrated by example in Fig. 2.6 and Fig. 2.7.

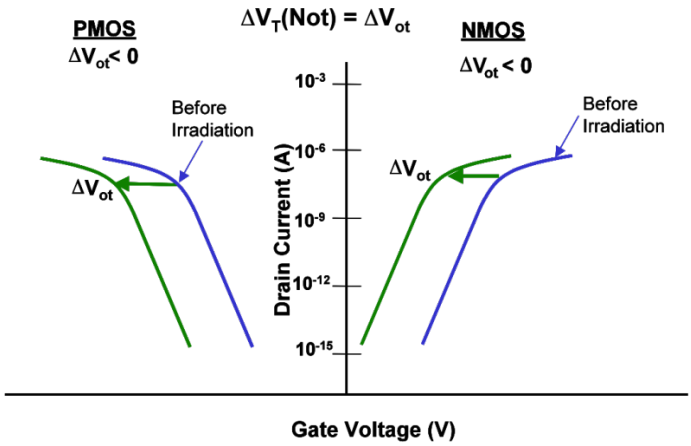


Fig. 2.6 Illustration of the shift in the drain current vs. gate voltage characteristics of n- and p-channel MOSFETs as a result of positive oxide-trapped charge [39].

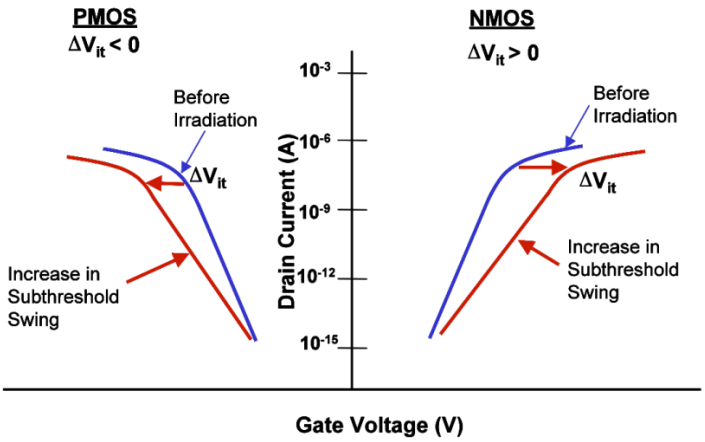


Fig. 2.7 Illustration of the shift in the drain current vs. gate voltage characteristics of n- and p-channel MOSFETs as a result of interface traps [39].

As seen Fig. 2.6 the buildup of positive oxide trapped charge in the gate oxide reduces the threshold voltage for both n and p-channel MOSFETs. Additionally the shift in threshold voltage for n-channel MOSFETs results in an increase in off-state and drive currents, while in p-channel MOSFETs off-state and drive currents are reduced. As seen in Fig. 2.7 interface trap buildup serves to decrease the subthreshold slope, or as it is often described an increase the subthreshold swing, of a CMOS device. Additionally an increase in threshold voltage is seen for n-channel MOSFET while the threshold voltage of a p-channel MOSFET is reduced (becomes more negative) with the increased presence of interface traps. The bias dependency of the interface trap charge state (i.e. positive, negative or neutral) explains this decrease in subthreshold voltage swing. During the current-voltage characterization, the silicon surface at the Si-SiO_2 interface is swept from accumulation to inversion by the gate voltage. Increased interface trapping inhibits the gate's ability to invert the silicon surface.

It is seen in Eq. 2.1 that the magnitude of holes generated from ionizing radiation shows a linear dependence on oxide thickness (t_{ox}). The amount of holes generated directly determines the amount of oxide-trapped charge (ΔN_{ot}) and interface traps (ΔN_{it}) generated in the oxide as discussed previously. This indicates that the magnitude ΔN_{ot} and ΔN_{it} will both drop with decreased oxide thickness due to device scaling. Additionally, it is understood that the magnitude of the radiation induced voltage shift (ΔV_{ot}) due to oxide-trapped charge (ΔN_{ot}) can be calculated using the following formula [16]:

$$\Delta V_{ot} = -\frac{t_{ox}}{k_{ox}\epsilon_o} q \Delta N_{ot}. \tag{2.7}$$

Eq. 2.7 includes constants for elementary charge (q), dielectric constant for SiO_2 (k_{ox}) and permittivity of free space (ϵ_o). The ΔN_{ot} dependence on oxide thickness in Eq. 2.7 shows that negative threshold voltage shifts caused by fixed oxide trapped charge buildup is proportional to the square of oxide thickness, i.e.,

$$-\Delta V_t(\Delta N_{ot}) = -\Delta V_{ot} \propto t_{ox}^2 \tag{2.8}$$

This indicates that device scaling and the corresponding reduction of gate oxide thicknesses will serve to limit the effect of ionization damage on gate oxides in deep submicron CMOS technologies. Indeed device scaling has increased the radiation hardness in the most state of the art technologies making threshold voltage shifts due to gate oxide degradation a minimal concern, as verified through experiment [19].

Effects on Isolation Oxides

While the hardness of gate oxides to ionizing radiation has been greatly increased due to device scaling, isolation oxides still remain relatively soft. In both older (LOCOS) and later (STI) isolation technologies, the buildup of oxide-trapped charge and interface traps are on-going concerns due to very thick of oxides and relatively poor oxide quality compared to gate dielectrics. Of chief concern is oxide-trapped charge with isolation oxides, as it can result in significant parasitic leakage currents [16, 18, 30, 34, 35, 38, 56, 57].

Possible leakage current paths are identified in Fig. 2.8. Intra-device drain-to-source (so called “edge”) leakage in n-channel MOSFETs can result from the buildup of oxide-trapped charge near the active device edge, as seen in Fig. 2.9 This edge leakage

can be thought of as a separate parasitic edge transistor acting in parallel with the gate oxide transistor. This is illustrated in current-voltage characteristics of Fig. 2.10.

Additionally the buildup of oxide-trapped charge in the base of the isolation oxide can result in inversion of silicon causing inter-device leakage current (paths 2 to 4 of Fig. 2.8). Oxide trapped-charge buildup is enhanced by the presence of a local electric field in the isolation oxide. High bias voltages on polysilicon and metal device interconnections on top of isolation oxides serve to generate this field. Parasitic current between active transistors can result in loss of device isolation, increased drain on voltage supplies, and the collapse of desired node voltages [16, 18, 25, 34, 57].

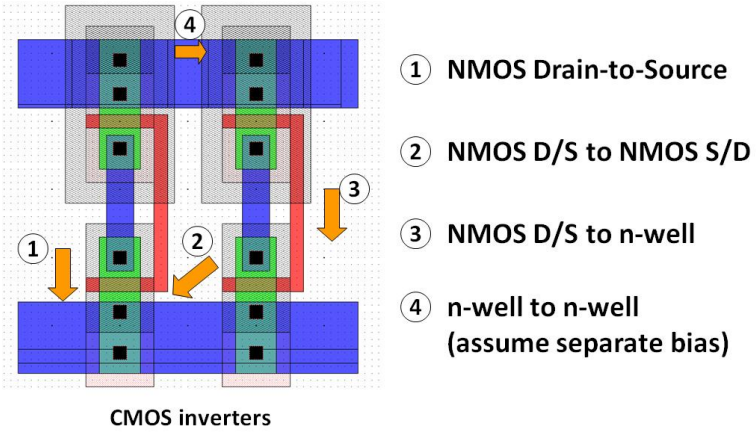


Fig. 2.8 Possible intra- and inter-device leakage current path resulting from oxide trapped charge buildup in LOCOS or STI isolation oxides [39].

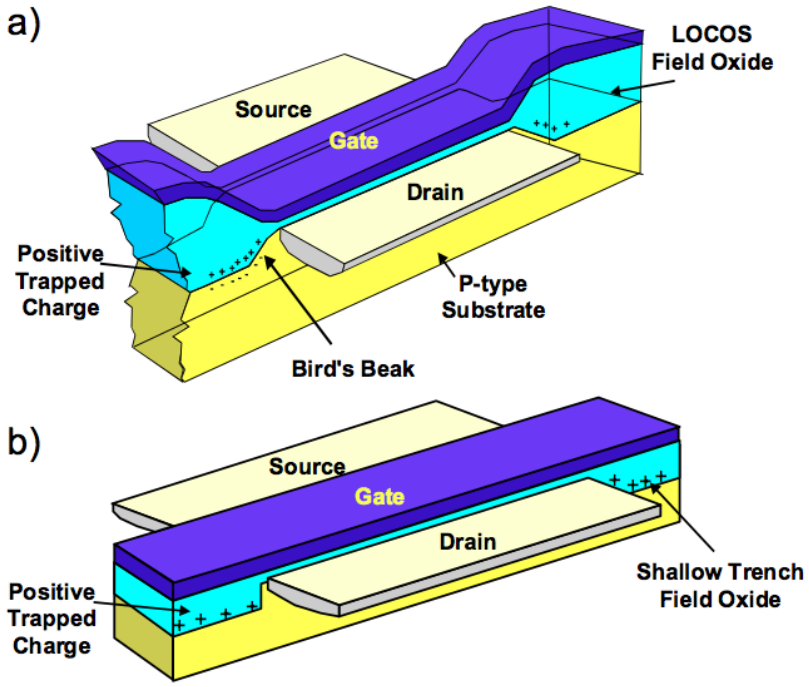


Fig. 2.9 Cross section of a) LOCOS isolated and b) STI isolated transistor showing trapped-charge location corresponding with intra-device edge leakage current [18, 58].

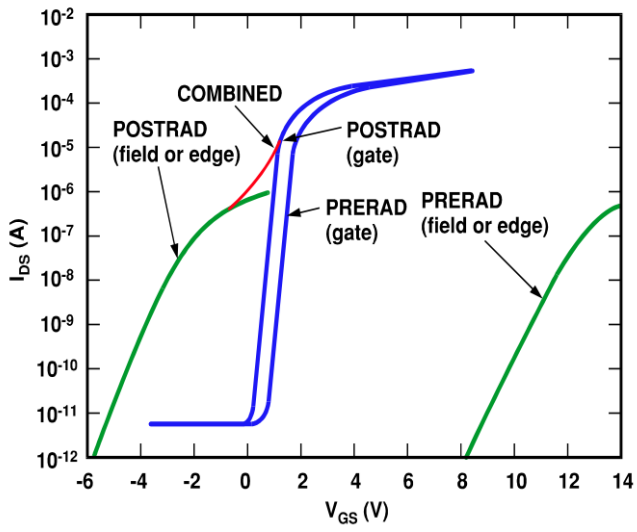


Fig. 2.10 Current-voltage characteristics of gate-oxide and a parasitic "edge" transistor showing increase in current post-irradiation due to the parasitic edge transistor [18].

CHAPTER 3

SIMULATION OF INTER-DEVICE EFFECTS

As explained in Chapter 2, inversion below field isolation oxides can result in significant inter-device leakage current. This current can, at minimum, hinder circuit operation and reduce battery life and at maximum, cause circuit failure. In order to design radiation-hardened circuits extreme care is taken to prevent inter-device leakage between active circuit elements. This includes adding highly doped "channel stop" implants as well as tightly controlled routing schemes of polysilicon and metal interconnect layers. Channel stop implants will inhibit creation of parasitic inter-device current paths by increasing inversion threshold voltage in these regions.

One alternative to channel stop placement is the use of careful routing of polysilicon or metal interconnects to avoid high electric fields in isolation oxides. Minimizing electric field is a worthwhile total dose hardening method for two reasons. First, reduced electric field decreases initial charge yield during irradiation, which then reduces defect buildup near the SiO_2/Si interface. Second, applied bias (electric field) increases the likelihood of parasitic inversion of silicon beneath the oxide. However, both channel stop placement and routing schemes add complexity to the design, and hurt design efficiency by increasing cell layout size.

Instead of implementing these techniques uniformly across the entire design, it would be advantageous for designers to be empowered to choose these techniques only when necessary. To do this, designers must be able to predictively model and simulate a given circuit, including the effect of parasitic inter-device current flow, and weigh the resulting circuit performance against design metrics. Predictive simulation capability

allows targeted hardening decisions to be made, implementing such hardening by design changes only when necessary.

In this chapter a charge pump case study, first presented in my Masters' Thesis, is reviewed to illustrate simulation of inter-device effects [23]. Moreover, the charge pump case study establishes context for follow-up work, presented in the second half of this chapter, specifically investigating geometric effects of inter-device parasitic structures. Together both works effectively illustrate techniques to effectively simulate inter-device effects.

Charge Pump Case Study – Background and Methodology

To develop and validate a design strategy for simulation of inter-device leakage, an integrated circuit, which is part of an implantable pacemaker design, is presented as a case study. The IC is used to provide electrical impulses, delivered by electrodes contacting the heart muscles, to regulate the beating of the heart. The IC has multiple functional digital and analog blocks used to provide multi-chamber pacing and recharge support for the pacemaker device. However the focus of this study is on a single block of the IC, the negative supply pumps. Fig. 3.1 illustrates the charge pump implementation in the overall integrated circuit scheme. The charge pump is used to generate two supply rails, -1×VDD and -3×VDD, from a single VDD supply. A simple schematic representation of the charge pump is shown in Fig. 3.2.

The choice to investigate the negative supply pumps, implemented as a charge pump topology, is particularly appropriate as a) charge pumps are widely used in implantable device and medical applications for voltage generation and b) high circuit

bias conditions serve to enhance ionizing radiation damage. High voltage switched capacitor charge pump topologies are becoming increasingly implemented in such applications as non-volatile memory and medical devices to generate a range of potentials from a single battery voltage [59-61]. In many cases, existing supply voltages in low power ICs are insufficient for some application specific operations, such as floating gate programming, as an LCD driver or simply to generate battery-multiplied supply rails on chip.

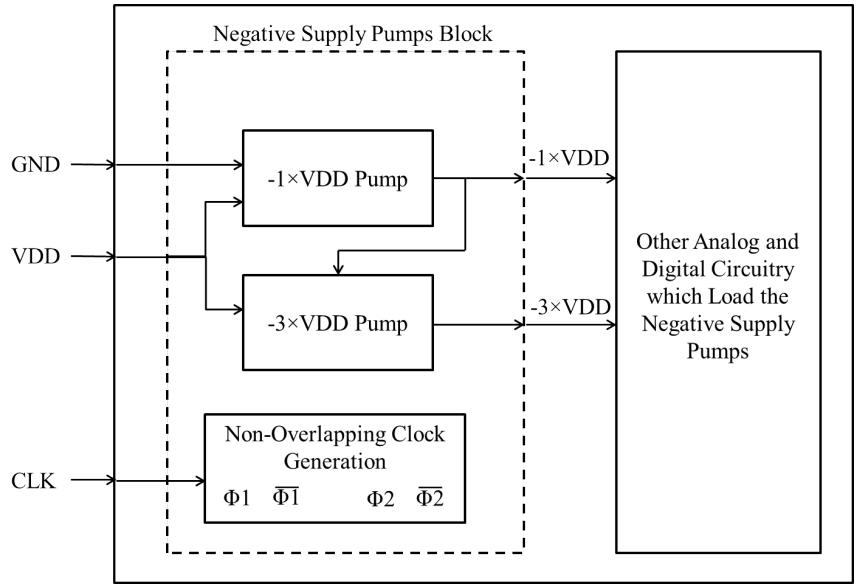


Fig. 3.1 Simplified block diagram of integrated circuit implementation of Negative Supply Pumps.

Charge pumps used in these types of applications are particularly susceptible to radiation-induced degradation because their higher voltage specifications typically require the utilization of devices manufactured with thicker dielectrics and lower doping levels. It is well known that these properties make high voltage CMOS technologies more susceptible to TID damage than advanced low power CMOS processes [16]. Moreover,

the higher voltage requirements result in larger electric fields, particularly in isolation (field) oxides, which will enhance radiation-induced defect buildup [17, 18]. The combined impact of lower doping and high electric fields leads to greater levels of field oxide leakage that, as will be shown, increases current draw at the charge pump output.

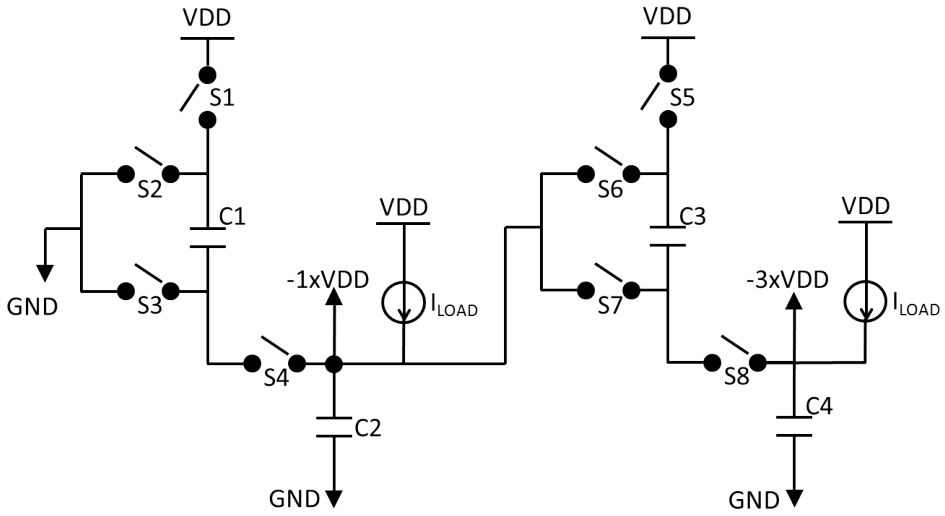


Fig. 3.2 Dual charge pump configuration implemented to generate -1×VDD and -3×VDD from the externally available VDD and GND voltages.

Experimental Irradiation Results

For the total dose failure analysis of the charge pump, the focus was on degradation in the high voltage -3×VDD output node. The radiation response of the -3×VDD with applied total dose is shown in Fig. 3.3. Pre-irradiation and after the first total dose stress step the output voltage remains constant at -9 V (-3×VDD). However at the second of total dose exposure stress step, the output has reduced by more than 1 V, and after third total dose stress step the output has reduced 50% from the operation specification. Such a reduction in the charge pump output is considered unacceptable for the integrated circuit design. These results serve as motivation for the failure analysis

case study, and represent the dataset that is to be recreated via a radiation-enabled simulation.

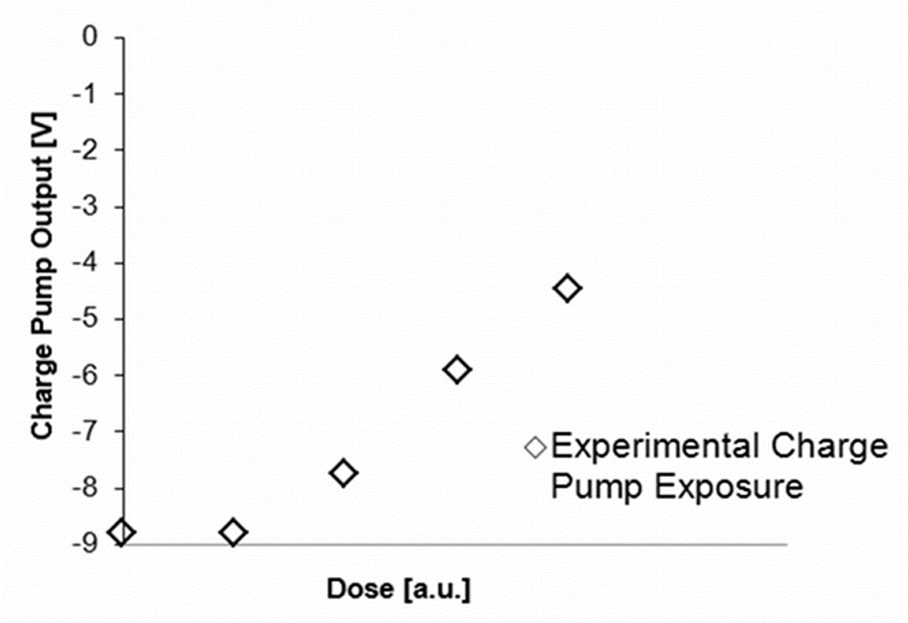


Fig. 3.3 Experimental results showing voltage collapse of the -3×VDD charge pump output versus applied total dose. Total dose increases from left to right.

Charge Pump Analysis Approach

The goal of the charge pump analysis case study is to explain the degradation exhibited as a collapse of the -3×VDD charge pump output with increasing total dose exposure. To accomplish this, extensive experimental work, device modeling and circuit and layout analysis are needed. The analysis approach, to be detailed in following sections, is represented graphically in the flowchart of Fig. 3.4.

First the inputs to the radiation enabled simulation must be determined, specifically compact models representing the most sensitive elements of the charge pump, parasitic inter-device field-oxide FET (FOXFET) structures. Compact models are generated for the FOXFETs through modeling a combination of experimental and TCAD

datasets. Then, the charge pump circuit and layout are analyzed, pinpointing numerous FOXFET-like structures within the charge pump layout. Back-annotation of FOXFETs into the circuit schematic combined with a FOXFET compact model set establishes the basis for a radiation enabled simulation test bench. Utilizing the charge pump test bench, the simulation dose level can be assigned by selecting the appropriate FOXFET compact model. Since the models were created after a specific dose exposure level, the model represents the device's operation at that exposure level. By selecting a particular exposure level (compact model set) for all devices in the schematic, we then simulate the circuit at that exposure level.

For the charge pump circuit we run a transient simulation of the pump operation as the -3×VDD node voltage builds up on the hold capacitor. We then note the final steady state voltage for the node at the chosen simulated exposure level. Next we select a compact model library set at the next exposure level, and repeat the simulation. Simulating the charge pump circuit with dose specific compact model sets models the effect of increasing total dose exposure.

Once the final total dose exposure level is reached, we now have a dataset of the steady state -3×VDD node voltage for each of the simulations. By plotting that dataset of node voltage versus total dose for the simulations, we then recreate the experimental collapse due to irradiation.

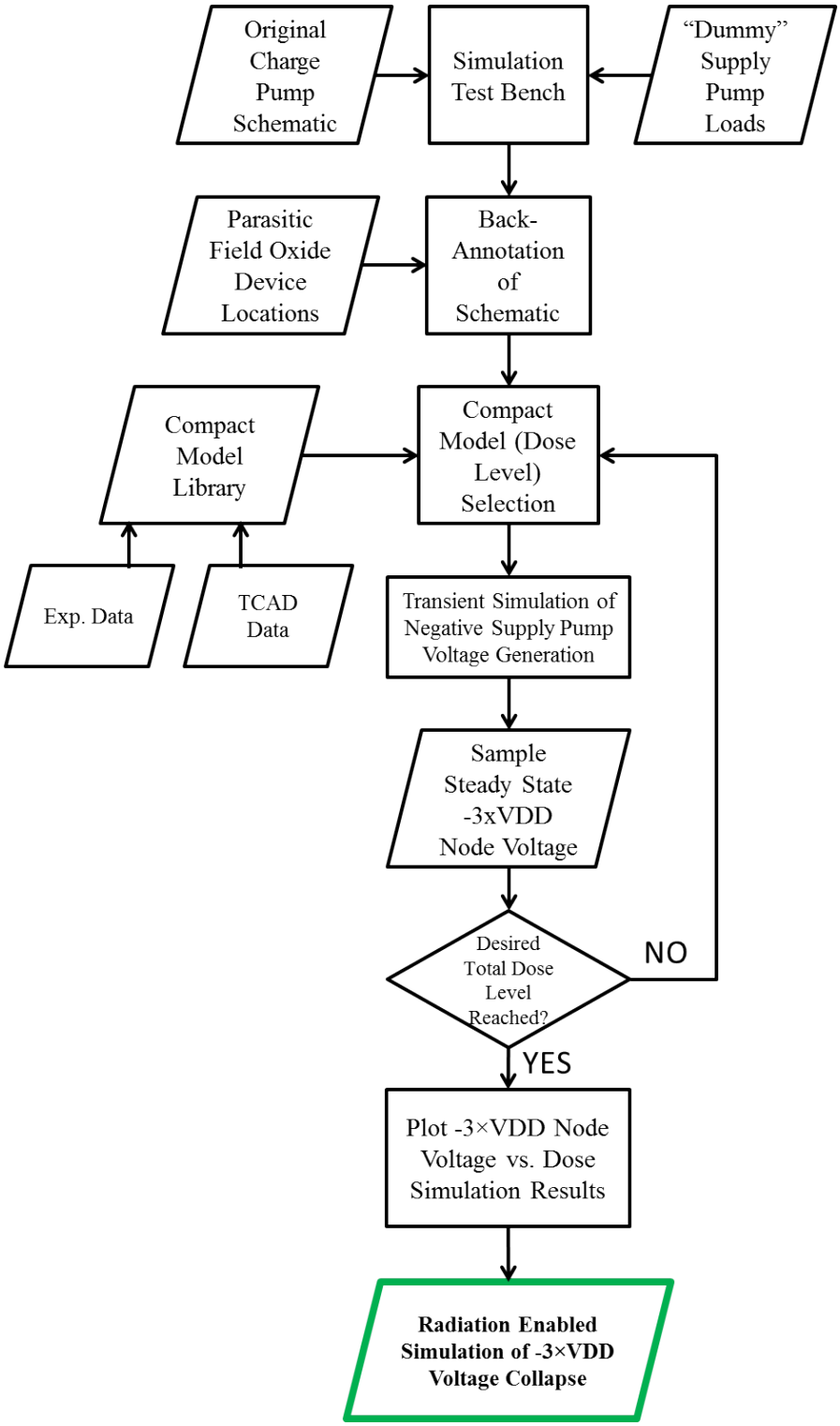


Fig. 3.4 Flowchart detailing steps to generate the -3×VDD collapse vs. dose via radiation enabled simulation.

Charge Pump Case Study - Results and Analysis

The analysis methodology is employed to investigate the collapse of the -3×VDD voltage node due ionizing radiation. By following the analysis process and constructing a radiation-enabled simulation that successfully recreates the voltage collapse seen in experiment, the root cause of failure is found and the methodology is validated.

Test Device Characterization

To investigate the effect of ionizing radiation on MOSFETs within the charge pump IC, the TID response of process monitor test devices are characterized. The use of test devices allow for device terminal bias conditions during irradiation to be easily controlled, and simplifies post-irradiation current-voltage characterization. To understand the full effect of ionizing radiation in the gate oxide of the n- and p- channel MOSFETs, devices were irradiated with "worst-case" bias conditions that would maximize charge yield in the gate oxides, within the constraints of realistic bias conditions used by the charge pump circuit.

It is seen that the NFET and PFET (Fig. 3.5) current-voltage characteristics are minimally affected by dose even after the highest total dose level. Thus both devices exhibit only minor amounts of oxide-trapped charge (N_{ot}) and almost no interface trap (N_{it}) accumulation in the gate oxide. Moreover, the radiation induced-voltage shifts still fall within the acceptable process model corners, Slow-Slow (SS) and Fast-Fast (FF), as used by circuit designers. Conversely full circuit irradiation data illustrated collapse of the output voltage at the same level of total dose. Based on this result, degradation of "as-

drawn" transistors due to ionizing radiation was discounted as the primary mechanism leading to the collapse in the charge pump.

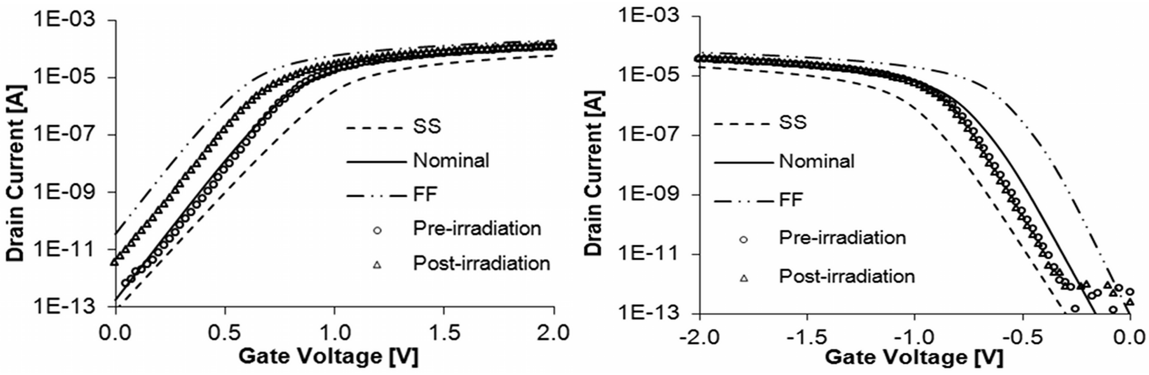


Fig. 3.5 Current-voltage characteristics for the 50 µm /3 µm NFET (left) and PFET (right) transistors. Additionally, model corners (SS, FF and nominal) are provided for comparison.

With MOSFET test results exhibiting minimal ionizing radiation degradation in gate oxides, it is then necessary to investigate degradation in isolation oxides. Also available were process monitor FOXFETs, which are useful in characterizing the isolation oxides for the technology. For this technology, LOCOS is used as the isolation oxide structure. The FOXFET structure is similar to a standard MOSFET structure, with highly doped n+ drain and sources and a single polysilicon stripe acting as a control gate. However in the FOXFET, the "gate" oxide is actually the thick LOCOS oxide giving the test device a very high pre-irradiation threshold voltage.

Irradiating and characterizing the FOXFET quantifies the radiation hardness and potential for inter-device leakage current under isolation oxides. Again, bias conditions for the FOXFET structure were chosen to maximize the charge yield by generating a high electric field in the oxide. Since the FOXFET is actually a parasitic transistor (i.e. not part of the schematic design of the circuit), the bias conditions of interest in the charge pump

is actually the maximum voltage seen on device interconnect that routes over the isolation oxides. By replicating this "worst-case" condition in the FOXFET, the maximum amount of radiation-induced damage in these sensitive regions is measured.

Results of the n-channel FOXFET irradiations are shown in Fig. 3.6. These results illustrate significant buildup of oxide-trapped charge (N_{ot}) in the LOCOS base, as seen by the large reduction in FOXFET threshold voltage. Additionally some accumulation of interface traps (N_{it}) is also shown, with minor increase in the subthreshold swing. From these results it can be determined that exposure to ionizing radiation results in parasitic inter-device leakage currents due to isolation oxide degradation from oxide-trapped charge buildup. In fact, at the highest dose level achieved, off-state current (e.g. gate voltage=0 V) is approximately 10 nA. This is a multiple order of magnitude increase in comparison to the pre-irradiation characteristics. From these results, it is reasonable to infer that inter-device leakage is the primary mechanism resulting in voltage collapse in the integrated circuit. To validate this hypothesis, further work is needed via device modeling, layout investigation and circuit simulation.

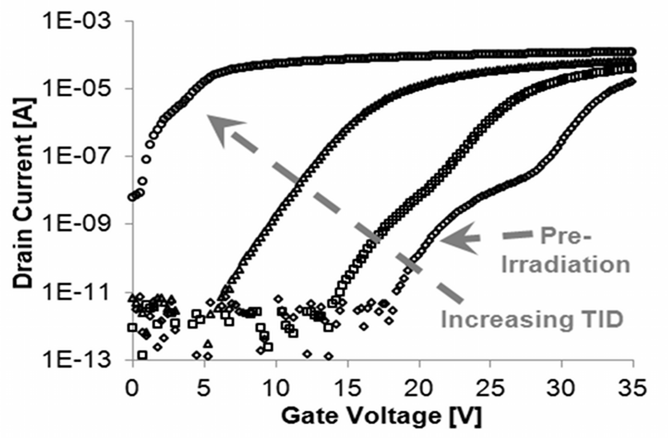


Fig. 3.6 Typical radiation response for the specialized n-channel field oxide FETs (FOXFETs) (W=50 μm, L=3 μm).

It is theorized that the non-linearity in the subthreshold region of three of the four dose levels shown in Fig. 3.6 are the result of a secondary parasitic FET structure, with less drive current and a lower threshold voltage, in parallel with the primary FOXFET structure that has a greater drive current and higher threshold voltage. The radiation then alters these parallel devices at slightly different rate, causing distinct threshold voltage shifts toward 0V. However, this hypothesis was not fully validated in experiment. Subsequently, for the purposes of the failure analysis and modeling, an approximation is made that the only parasitic of concern is the primary FOXFET due to the high drive current which would have a more deleterious effect on the output node. Thus the secondary parasitic is neglected in all further modeling and simulation work.

Device Modeling

To further investigate the effects of ionizing radiation on the isolation oxides, 2-D TCAD modeling was performed. By generating a Silvaco model of the parasitic FOXFET structure and simulating with the Radiation Effects Module (REM) within the Silvaco ATLAS simulator the experimental FOXFET results can be validated. Additionally the development of a calibrated 2-D FOXFET structure allows for the generation of additional current-voltage data suitable for compact model generation.

A 2-D TCAD structure representative of the FOXFET tested in experiment, with n+ drain and source regions (n+ to n+), was constructed. Inputting process technology information and adjusting the virtual FOXFET structure to match pre-irradiation data enables proper calibration of the parasitic device. Once a pre-irradiation structure is calibrated, the REM was employed. Using REM inside of ATLAS allows further

calibration of the 2-D structure using FOXFET data for dose step stress levels and bias conditions achieved in experiment.

REM calibration is realized by fine-tuning REM radiation parameters such that TCAD simulation matches closely to the known experimental electrical characteristics for the pre-irradiation dataset and one of the post-irradiation datasets. Then simulating with the tuned REM parameters at remaining dose levels the model fit can be verified against experiment. By showing good agreement at all dose levels, a calibrated TCAD model is achieved. Simulation results of the 2-D n+ to n+ FOXFET structure are compared to experimental data in Fig. 3.7.

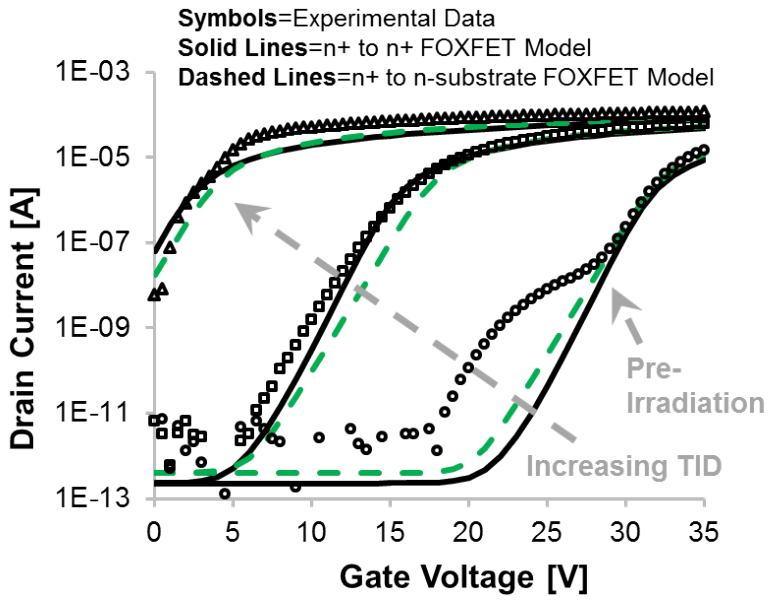


Fig. 3.7 Comparison of Silvaco ATLAS simulation (solid lines) to experimental data (symbols) for the n-channel FOXFET structure.

Layout investigation of the charge pump integrated circuit found that no parasitic inter-device regions exist in layout similar to that of the test FOXFET with n+ source and drains (n+ to n+). However, since the circuit was developed in an n-substrate/p-well

technology, numerous FOXFET-like parasitics exist with an n-substrate drain and an n+ source. The formation of this region in layout will be discussed in detail later.

Since a fully calibrated 2-D ATLAS structure with REM simulation has been achieved for the n+ to n+ FOXFET structure, it is now possible to construct a new n+ to n-substrate structure and assume the same REM parameters controlling fixed oxide charge buildup. Generation of the new n+ to n-substrate FOXFET structure and subsequent simulation shows good agreement with experimental data and simulation performed on the n+ to n+ FOXFET, as seen in Fig. 3.7. These results confirm the use of n+ to n+ FOXFET experimental and TCAD datasets as well as the new n+ to n-substrate FOXFET TCAD datasets as suitable representations of the on-chip parasitics.

Achievement of a fully calibrated n+ to n-substrate FOXFET now allows accurate simulation of electrical characteristics based on the proper description of charge buildup as a function of dose. By utilizing REM again for simulation, one is able to increase the radiation response resolution across the dose range of interest. Fig. 3.8 shows the reduction threshold voltage of the n+ to n-substrate FOXFET as simulated in ATLAS using REM. Threshold voltage shifts extracted from the experimental n+ to n+ FOXFET are also plotted in Fig. 3.8. The plot indicates excellent agreement between the radiation-enabled device simulations and experiments. Therefore it is seen that the ATLAS structures with REM simulation serve as a capable supplement to “fill in” the FOXFET dataset at additional total dose levels, not achieved in experiment. The calibrated structure is used to generate data suitable for compact modeling at 3 additional intermediate total dose stress step levels, which were not available via experimental irradiation datasets.

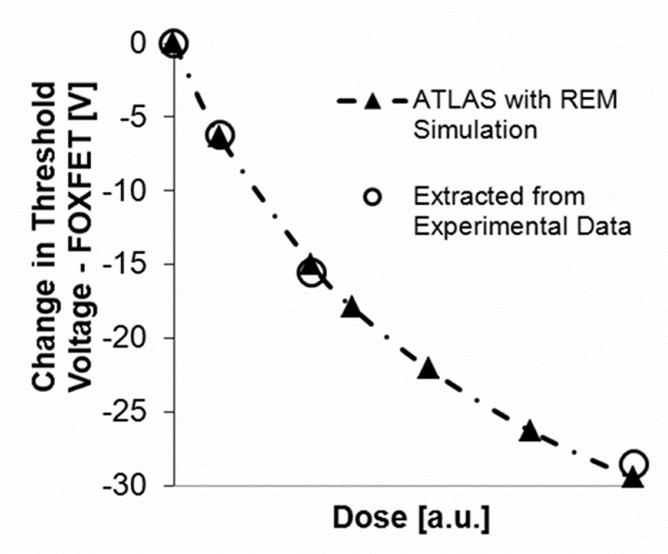


Fig. 3.8 Change in threshold voltage of the FOXFET versus applied total dose showing good agreement experimental irradiation and ATLAS simulation data.

Based on the results of Fig. 3.7 and Fig. 3.8, it is reasonable to assume that electrical characteristics taken from ATLAS simulations on the generated 2-D FOXFET structure will accurately represent the actual parasitic FOXFET structure found in circuit layout at the simulated dose. Using electrical characteristics from the 2-D TCAD simulation allows for creation of a comprehensive compact model library for the FOXFET structures as will be discussed in later.

The final BSIM3 compact models were created using data from the Silvaco REM simulations exclusively. The advantage being that compact models are more easily fit to the simulated data and a high level of agreement is obtained between simulation and the compact models. The disadvantage to this strategy is there is exhibited mismatch in the shape of the subthreshold slope between the Silvaco simulation and experimental data.

However, as mentioned previously, the non-linearity seen in the subthreshold slope is neglected.

Layout Investigation

FOXFET experimental and modeling data illustrates significant degradation of isolation oxides due to ionizing radiation. It is then necessary to verify if integrated circuit layout conditions exist which are conducive for inter-device leakage currents. For such parasitic currents to occur, it is necessary to have separate n-type regions of different biases, separated by p-type region. Additionally, polysilicon routed over isolation (LOCOS) oxide above the p-type region acts as a biased gate. This would serve to aide in inversion of the p-type region and increase radiation-induced damage in the oxide by providing a vertical electric field.

Review of the charge pump and non-overlapping clock generation circuit layouts reveals 51 possible parasitic FOXFET-like structures. The integrated circuit is designed in an n-type substrate/p-well technology, thus parasitic FOXFETs structures occur at the edges of p-wells in the design, as shown in Fig. 3.9. While the layout geometry does differ for many of the 51 parasitic FOXFETs, all have a basic common structure as shown in Fig. 3.10. The variation in parasitic FOXFET layout geometry is the subject of a later study, to be presented in the second half of this chapter.

In identified parasitic FOXFETs, the n- substrate, held at VDD, forms the drain while an n+ diffusion region forms the source. The n+ diffusion can be biased as low as –3×VDD, depending on circuit state. The p-well, which makes up the body of the parasitic, is biased at the most negative potential (i.e., –3×VDD). The gate of the

parasitic is a polysilicon interconnect line, biased as high as VDD, which runs over isolation field oxide at the p- well edge. The circuit bias conditions result in a 4×VDD (FOXFET polysilicon gate to p-well body) voltage across the field oxide, providing high electric field that enhances TID degradation. This combination of bias conditions as well as susceptibility to total dose degrading can lead to significant current conduction through the parasitic FOXFETs, essentially providing a short circuit current path from VDD to –3×VDD, as illustrated in Fig. 3.11.

This type of parasitic FET structure is found to occur 51 times within the charge pump and non-overlapping clock generation circuitry, thus it is reasonable to assume radiation-enabled activation of these parasitic, causing a significant number of parasitic current path and ultimately a collapse of the to –3×VDD output voltage at high doses. By simulating circuit operation with the addition of the parasitic FOXFETs back annotated into the schematic, this conclusion can be confirmed.

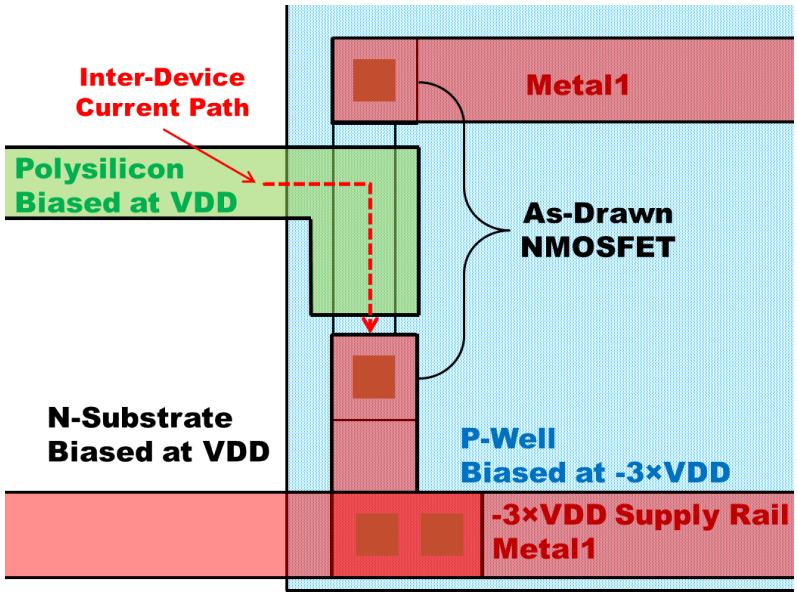


Fig. 3.9 Layout example of the parasitic FET structure with inter-device current path from the n-substrate to the n+ diffusion.

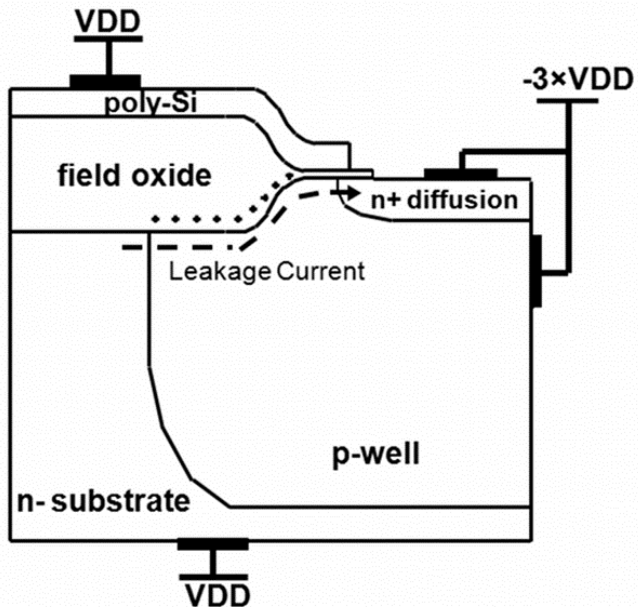


Fig. 3.10 Cross-section of the parasitic FOXFET structure occurring in the charge pump layout. Also indicated is the typical bias configuration for each region.

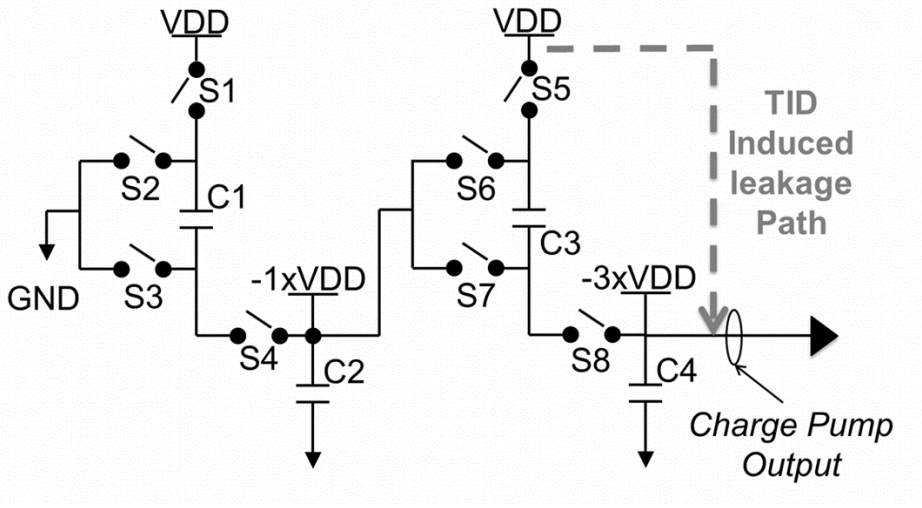


Fig. 3.11 Simplified charge pump schematic illustrating the radiation induced leakage path associated with the activation of parasitic FOXFET devices.

Compact Model Library

In order to implement the radiation-enabled simulation strategy outlined previously, it is necessary to generate a radiation-enabled compact model library. Since

the compact model selected for simulation is equivalent to selecting a dose level for our methodology, multiple compact models for the same device type must be generated. With the experimental and modeling results, it is determined that inter-device leakage currents cause the voltage collapse. To capture this in simulation, we can generate compact models of the parasitic FOXFET structures and add them into the schematic.

Compact models for the FOXFET parasitic device were generated in the BSIM3v3 compact modeling framework. Using the combined dataset from experimental testing and computer modeling, seven separate compact models were created representing all total dose stress step levels examined in experimentally and via TCAD. Creating compact models to represent the parasitic devices allows for full circuit simulation at each dose step.

Radiation Enabled Circuit Simulation

To recreate the voltage collapse failure mechanism seen in experiment, a test bench was developed to allow for radiation-enabled simulation. The test bench included the original charge pump and non-overlapping clock generation circuits as well as dummy capacitive and resistive loads to represent the rest of the integrated circuit for which the pumps supply. Also, the 51 parasitic FOXFETs had to be back annotated into schematic based the results of the layout investigation.

By successive transient simulations of the charge pump circuitry with back-annotated parasitic FOXFETs at all of the dose stress levels, we are now able to model the complete charge pump response with increasing dose. Fig. 3.12 illustrates the charge pump output voltage simulated with parasitic FOXFETs. As seen in the simulation

results, as we model increased total dose (interchange FOXFET compact models), the output voltage collapses in a similar fashion as that observed in experiment.

One notable consideration when comparing experiment to simulation in Fig. 3.12 is that the parasitic FOXFETs in the charge pump IC have irradiation biases controlled internally by the circuit state conditions during irradiation. This is important because, as we apply dose and begin to collapse the output voltage, the irradiation biases (specifically the p-well voltage of –3×VDD) of the FOXFETs are reduced. Thus the FOXFETs in the charge pump experimental data encounter a dynamic bias condition during irradiation. This decreasing bias leads to reduced damage in the FOXFET, somewhat slowing the collapse of the experimental output.

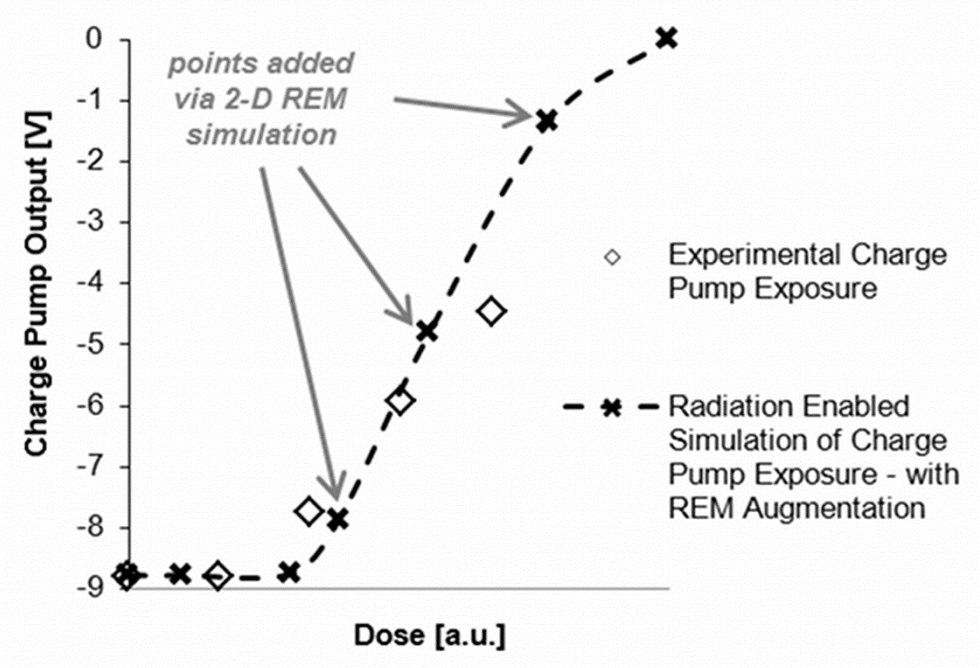


Fig. 3.12 Radiation-enabled circuit simulation of the charge pump output voltage (-3×VDD) compared against experimental test data.

The datasets obtained from individual FOXFET irradiations are extracted using a static bias during irradiation as specified in the experimental details section. In individual

device testing external supplies provide fixed bias conditions. Correlating this information with the known bias dependency of oxide trapped charge buildup, it is expected that the modeled/simulated damage would be greater than that of the full charge pump irradiation due to reduction in irradiation bias at upper dose levels of the experiment. This correlation is illustrated in the results of Fig. 3.12, as simulated collapse in the output voltage is more severe than that of the experiment at the higher total exposure levels.

The ability to accurately predict, or in the case of this analysis re-create, the radiation response of a given circuit is valuable as it supports front-end design mitigation of ionizing radiation effects. By analyzing the results of a radiation-enabled simulation, targeted and measured design changes can be implemented as part of a radiation hardening by design strategy within the context of other medical device design goals.

Analysis of Parasitic Field Oxide Transistors

The preceding case study found that leakage current through parasitic FOXFETs resulted in the collapse of charge pump output voltage. It was found that such parasitic FOXFETs are often of asymmetrical geometry. For a width/length scalable compact model of parasitic FOXFET structures to be fully realized, the geometric effects of the often irregularly shaped polysilicon layouts in a circuit must be quantified and effective width/length ratios must be determined. In this work we develop methods for effective width/length estimation, which may be applied to parasitic FOXFET layouts found in circuits fabricated in more advanced technologies.

By creating accurate radiation-enabled compact models for FOXFETs, the post-irradiation response can be simulated. This allows for impactful hardening-by-design approaches to be implemented prior to part fabrication [19, 21, 22, 62]. To accomplish the goal, an integrated test coupon containing various FOXFET test structures was designed and fabricated. Electrical measurements on these structures provide critical information that can be used in the development of width/length scalable models for parasitic transistors inherent in many IC designs. A photomicrograph of the test die is shown in Fig. 3.13. The die was manufactured in a 3 μm n-substrate CMOS technology used for precision high-voltage applications. The isolation oxides in this technology are LOCOS structures, with an average dielectric thickness of 1,000 nm.

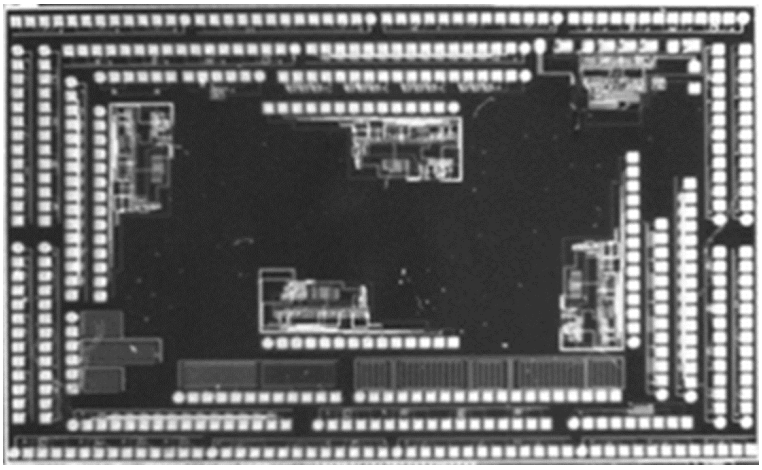


Fig. 3.13 Integrated test coupon developed specifically for radiation effects investigations containing various sub-circuits and test structures, including an array of FOXFETs.

Included on the test coupon are parasitic FOXFET structures found on a typical IC layout that, when degraded by ionizing radiation, may induce leakage paths that impact circuit operation [63]. A representative cross-section of the parasitic FOXFET of interest was illustrated previously in Fig. 3.10. All layouts are n-channel MOSFETs with

the polysilicon routing extending from the transistor gate across the p-well to the n-substrate boundary. The polysilicon routing creates a FOXFET structure between the n-substrate and the n+ diffusions of an as-drawn MOSFET.

Approach

As mentioned above, included on the test coupon IC are structures containing multiple variants of FOXFETs representative of parasitic devices that exist inherently on many IC designs. More specifically the test structure layouts were extracted from sub-circuits and standard library cells (e.g., inverters, NAND and NOR gates) developed for the technology investigated. The extracted layouts were reduced to include only the as-drawn NMOSFET and the resulting parasitic FOXFET generated between the source/drain diffusions and the n-substrate by the gate polysilicon interconnect. All nodes of the test structures (gate, drain, source, p-well/body, and n-substrate) were connected to independent wirebond pads for ease of packaging and characterization. Once fabricated and packaged, the electrical characteristics of the FOXFET devices were measured prior to and after exposure to ionizing radiation. Radiation exposure of the test coupon IC was performed in an x-ray irradiator (120 kV, 6 mA source with a 180 mm source to surface distance). Irradiations were completed using the step stress approach. The FOXFET structures were irradiated with a polysilicon gate bias of +12.8 V and all other terminals grounded. The irradiation bias was chosen to match the typical operational conditions used the technology and fix local electric fields that maximize TID damage in the LOCOS oxides [64]. Current-voltage measurements were performed before irradiation, and after four irradiation stress steps. One measurement completed at each of the steps is

a drain current vs. gate voltage sweep of the NMOSFET. For this measurement, the gate voltage was swept from 0 V to 35 V, the NMOSFET drain was fixed at 100 mV and the NMOSFET source, p-well and n- substrate were all fixed at 0 V. Measurement of drain, source, p-well and n-substrate currents allows determination of as-drawn and parasitic leakage currents prior to- and after irradiation. In the following section, the results of the FOXFET measurements are presented and analyzed.

In order to determine effective aspect ratios for non-rectangular polysilicon interconnect layouts, more complex FOXFETs were designed and characterized. By successfully estimating aspect ratios of non-rectangular layout it is then possible to build a parasitic FOXFET compact model that may be used in post-irradiation circuit simulations. Also included in the following section is a more in depth analysis of the effects of the NMOSFET gate dimensions on parasitic response. This analysis is necessary to establish if the as-drawn gate geometry affects the parasitic FOXFET response.

Parasitic FOXFET Analysis - Rectangular FOXFET Layout

To better understand the parasitic FOXFET, we first test and analyze the most simple test structure. Shown in Fig. 3.14 is the layout of a 4 μm/4 μm NMOSFET, with polysilicon interconnect routing creating a parasitic FOXFET, as indicated by the bent arrow. The simplicity of the interconnect shape, a simple rectangle, allows us to baseline the pre- and post-radiation performance of the FOXFET. This is valuable as we increase complexity of the FOXFET geometries.

The results of pre- and post-irradiation characterization are provided in Fig. 3.15. Fig. 3.15(a) illustrates the low threshold voltage (~0.7 V) and high drive current (~10 μA) of the as-drawn NMOSFET. In comparison, the parasitic FOXFET has a high threshold voltage (~30 V) and significantly lower drive current (~100 nA) as seen Fig. 3.15(b). Following radiation exposure the measured currents show a significant change in drain-to-substrate current, with drastically reduced threshold voltage and increased drive current, compared to only a minimal change in drain-to-source current.

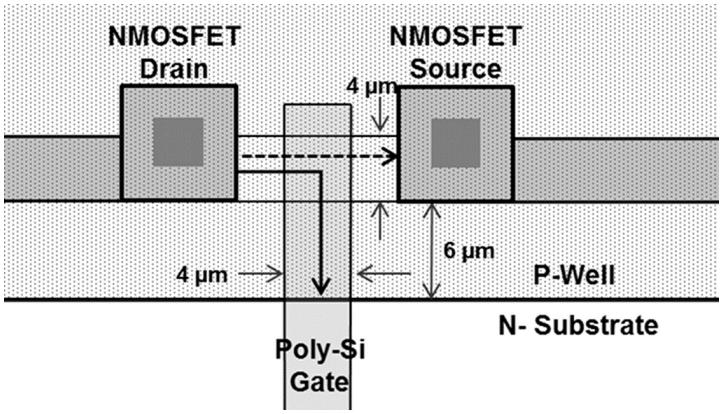
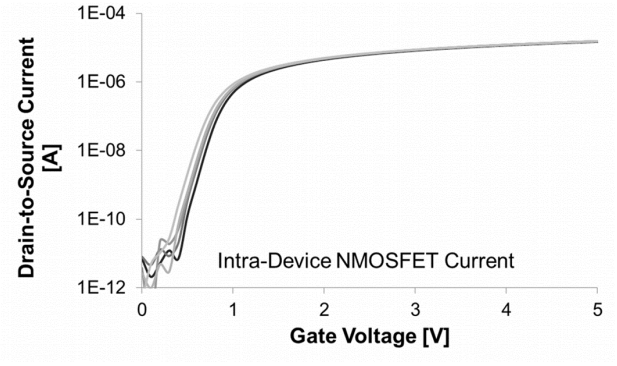


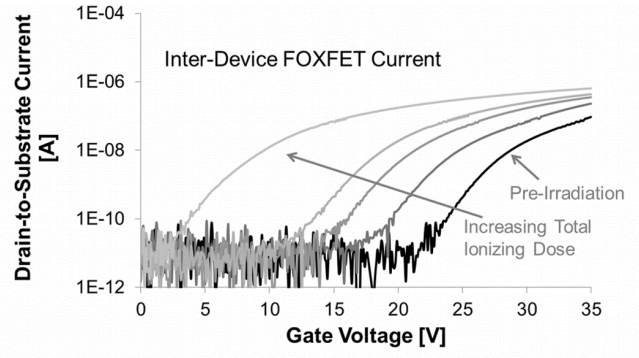
Fig. 3.14 Layout of 4 μm/4 μm NMOSFET. Arrows indicate designed MOSFET drain-to-source (dashed) and parasitic FOXFET drain-to-substrate (solid) current paths.

The substrate current measurements shown in Fig. 3.15(b) suggest a large buildup of positive oxide trapped charge (N_{ot}) in the base of the LOCOS resulting in parasitic leakage current from the as-drawn transistor to the n-substrate [65]. This large degradation in the substrate current must be modeled accurately in order to accurately simulate post-irradiation circuit behavior. Minimal shifting in the drain current characteristics in Fig. 3.15(a) indicates the thin gate oxide of the as-drawn NMOSFET is much less susceptible to N_{ot} buildup as compared to the much thicker LOCOS isolation oxide.

The rectangular FOXFET structure of Fig. 3.14 is useful for obtaining a baseline FOXFET current response that can be used for aspect ratio extraction of more complex FOXFET layouts. In order to demonstrate the general width/length scalability of these simple parasitic device designs, another similar test structure, shown on Fig. 3.16, was characterized. The as-drawn NMOSFETs of Fig. 3.14 and Fig. 3.16 are identical; however, the distance between the as-drawn transistor and the n-substrate boundary is increased from 6 µm to 20 µm. This change serves to increase the effective length of the FOXFET gate, giving Fig. 3.14 and Fig. 3.16 estimated FOXFET aspect ratios of 4 µm/6 µm and 4 µm/20 µm, respectively.



(a)



(b)

Fig. 3.15 Pre-and post-irradiation current-voltage response of the Fig. 3.14 test structure. Drain-to-source current vs. gate voltage response (a) shows minimal change post-irradiation. Drain-to-substrate current vs. gate voltage response (b) shows significant increase in inter-device current with increasing TID.

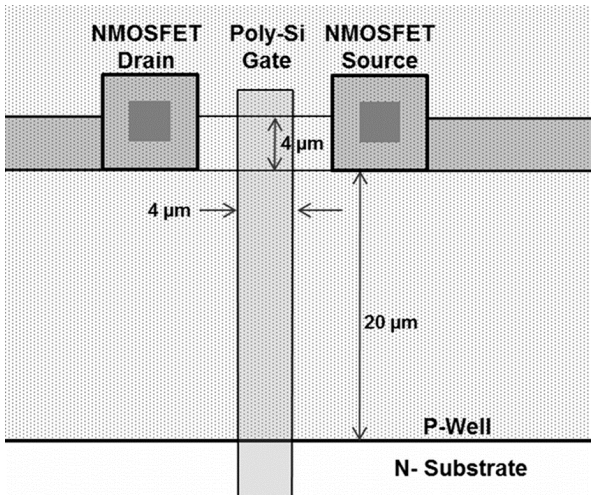


Fig. 3.16 Layout of 4 µm/4 µm NMOSFET similar to Fig. 3.14 with the distance from as-drawn transistor to n- substrate boundary increased.

Utilizing the pre-irradiation substrate current vs. gate voltage measurement data for these two rectangular parasitic FOXFETs supports the generation of a normalized (aspect ratio of 1 µm/1 µm) FOXFET current response. Substrate current normalization is accomplished by taking the substrate current data for both Fig. 3.14 and Fig. 3.16 layouts and dividing by the estimated FOXFET aspect ratios of 4 µm/6 µm and 4 µm/20 µm, respectively. Fig. 3.17 plots the current-voltage response for both layouts as well as the results of normalization of both datasets. The good correlation between both normalized substrate currents indicates that a) the estimated FOXFET aspect ratios are reasonable and b) the normalized dataset is suitable for use in our analysis and aspect ratio determination of more complex FOXFET layouts, as presented in the following subsection.

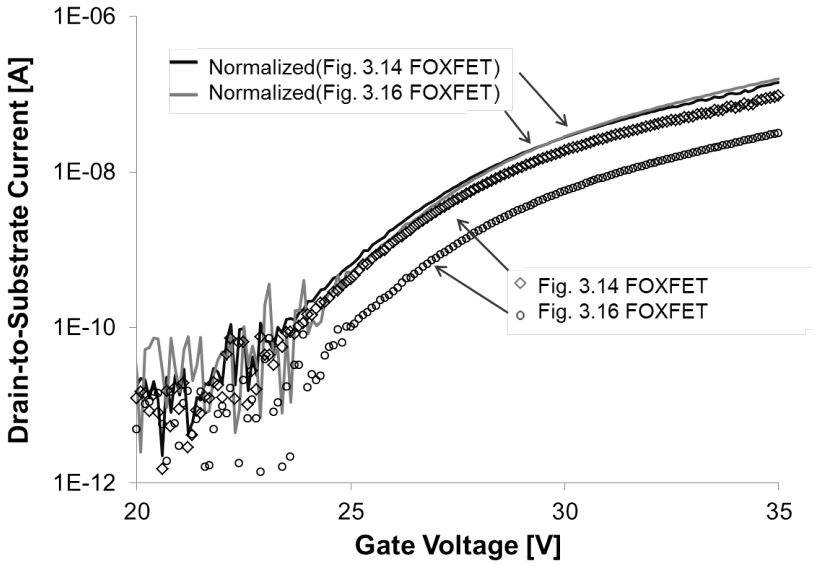


Fig. 3.17 Current-voltage response of the FOXFETs found in Fig. 3.14 and Fig. 3.16 (symbols). Normalization of the each of the FOXFET currents (solid lines) illustrates good agreement.

Parasitic FOXFET Analysis - Complex FOXFET Layouts

In the previous section it was established that the parasitic FOXFET structure would conduct significant inter-device current post-irradiation. Additionally a normalized FOXFET response was created to be representative of a scaled 1 μm/ 1 μm device. We now utilize the normalized parasitic response to estimate effective aspect ratios of more complex FOXFET layouts included on the test coupon IC. The layouts of additional structures included on the coupon are provided Fig. 3.18. However the effective aspect ratios of these structures are not as easily defined as the rectangular FOXFETs discussed above. Since polysilicon interconnects are commonly routed by the designer or via an automated layout tool to minimize the cell size, the layout can take many forms. However, to model the complex FOXFET structure in simulation it is necessary to determine an effective aspect ratio for any given shape of polysilicon gate.

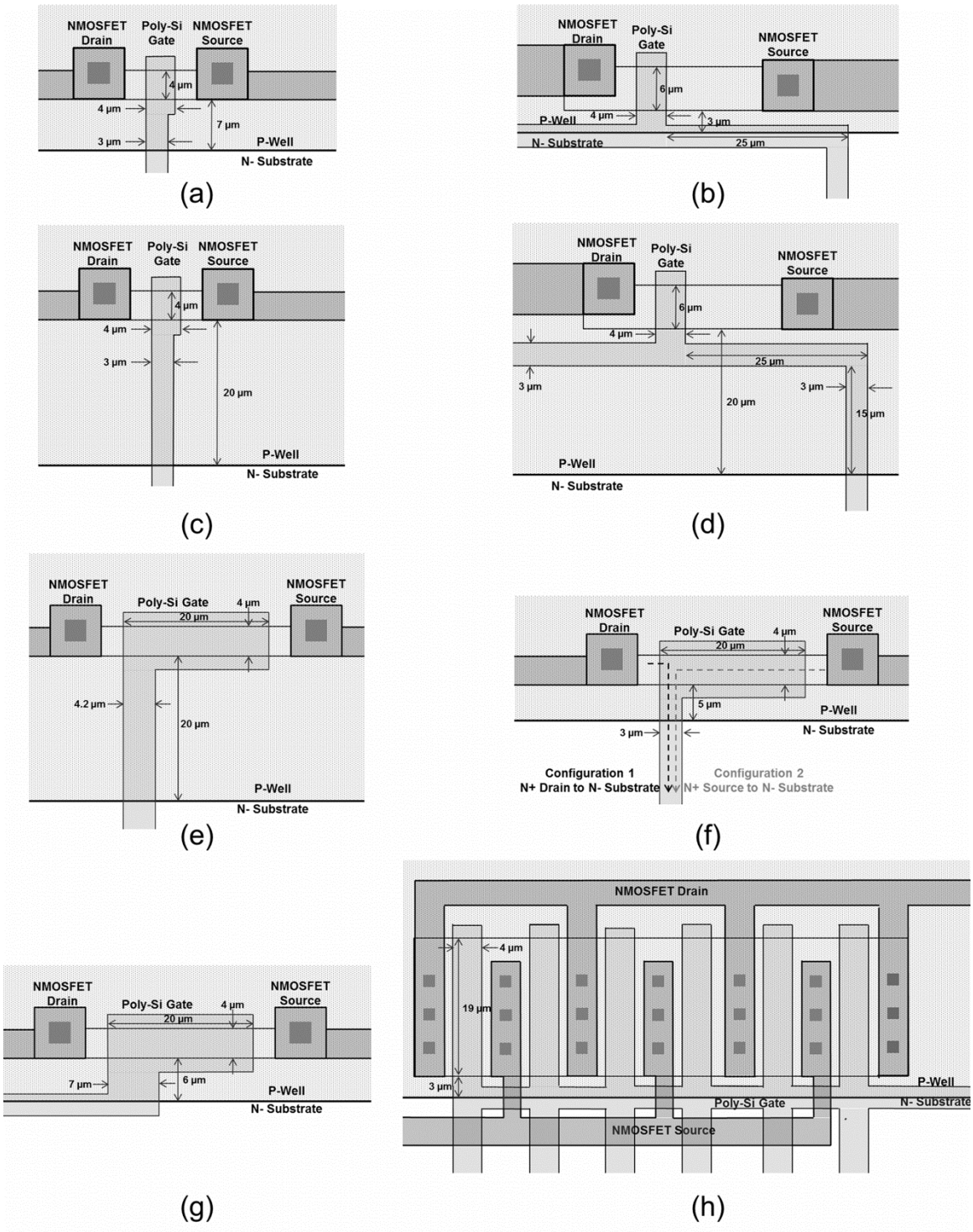


Fig. 3.18 NMOSFET transistor designs with aspect ratios of 4 µm/4 µm (a, c), 6 µm/4 µm (b, d), 4 µm/20 µm (e, f and g) and (h) 6×19 µm/4 µm respectively. Routing of the polysilicon gate interconnect forms a parasitic FOXFET structure in all layouts. Aspect ratios for the parasitic FOXFETs are estimated as 3 µm/7 µm (a), 4 µm/3 µm (b), 3 µm/20 µm (c), 3 µm/40 µm (d), 4.2 µm/20 µm (e), 3 µm/5 µm (f), 7 µm/6 µm (g) and 6×4 µm/3 µm (h) respectively

Again, current-voltage measurements were performed on these more complex designs, including the as-drawn drain-to-source current and parasitic n-substrate current vs. gate voltage. Once the n- substrate, or inter-device FOXFET, current is obtained we can compare against the previously calculated normalized substrate current to calculate an effective aspect ratio for the more complex structure. We chose to compare the pre-irradiation normalized substrate current to each complex FOXFETs pre-irradiation substrate current at a gate voltage of 35 V. Using the normalized substrate current of 0.14 μA at 35 V and applying Eq. 3.1 below allows for calculation of an effective aspect ratio for each FOXFET.

$$I_{Sub}(FOXFET) = (W/L) \times I_{Sub}(Normalized) \tag{3.1}$$

The resulting effective aspect ratios extracted from current-voltage data for the layouts shown in Fig. 3.18 can be found in Table 3.1. Two identical test coupon ICs were tested to record part-to-part variation in measured substrate current for a given FOXFET.

While extracting the aspect ratios for an individual FOXFET directly from the experimental data provides insight into the basic response of a specific parasitic device, this type of approach does little to support the identification of generalized scaling rules. Indeed, the ultimate goal is to be able to determine aspect ratios of any given parasitics in a circuit early in the design process. It is not feasible to experimentally test all parasitic FOXFETs for compact model creation, thus we must be able to estimate an effective aspect ratio based on the layout, regardless of its complexity.

Examining the layouts of Fig. 3.18 we perform a best estimation of width/length ratios for comparison against the previously calculated effective aspect ratios. Estimation is performed by determining the most direct rectangular polysilicon route from the as-drawn transistor to the

n-substrate boundary, ignoring all other polysilicon interconnect structures outside the direct path. For example, examining the layout of Fig. 3.18(g), presented again with additional markings in Fig. 3.19, we estimate the effective FOXFET gate area to be the 7 μm × 6 μm polysilicon rectangle between the as-drawn transistor and n-substrate boundary. This estimation discounts polysilicon interconnect area outside the rectangle, also denoted in Fig. 3.19. For this test device the estimated effective aspect ratio of 7 μm/6 μm (1.16) is found to be in excellent agreement with the calculated aspect ratio of 1.19.

Table 3.1 Effective FOXFET Aspect Ratios

Corresponding Fig. 3.23 FOXFET Layout	**Average Measured Substrate Current at V_G=35V**	**Effective Aspect Ratios Calculated from I-V data (W/L)**	**Effective Aspect Ratios Estimated from Geometry (W/L)**
(a)	83.3 ± 10.5nA	0.54	0.43 (3 μm/7 μm)
(b)	151.0 ± 24.7nA	1.00	1.33 (4 μm/3 μm)
(c)	33.2 ± 2.12nA	0.22	0.15 (3 μm/20 μm)
(d)	5.87 ± 0.86nA	0.04	0.08 (3 μm/40 μm)
(e)	56.1 ± 2.12nA	0.37	0.21 (4.2 μm/20 μm)
(f)	208.5 ± 23.3nA	1.28	0.60 (3 μm/5 μm)
(g)	182.0 ± 4.95nA	1.19	1.16 (7 μm/6 μm)
(h)	700.0 ± 5.59nA	4.62	8.00 (6×4 μm/3 μm)

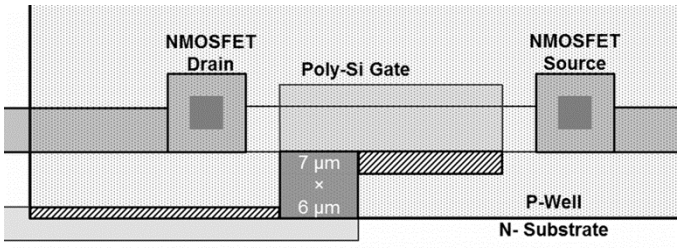


Fig. 3.19 Test structure layout previously shown in Fig. 3.18(g) with added marking to denote our estimated effective aspect ratio of 7 µm/6 µm. The polysilicon regions shown with striped shading are discounted in the aspect ratio estimate.

Similarly performed estimations on the other available layouts in Fig. 3.18 are included in Table 3.1 and compared in Fig. 3.20. While the agreement between estimated and calculated varies with each layout, overall the estimation technique offers very reasonable effective aspect ratios. Indeed the relative accuracy of this simple technique suggests that at least for larger geometry technologies, compact models for parasitic FOXFETs may be readily generated via post layout extraction routines, which calculate the effective W/L of a parasitic from the dimensions of the most direct rectangular polysilicon route.

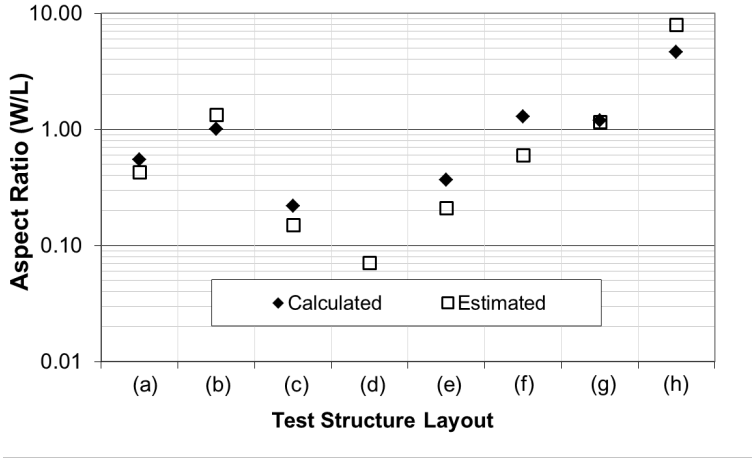


Fig. 3.20 Comparison of calculated versus estimated effective aspect ratios for test structure layouts corresponding with Fig. 3.18.

At present, it is not known how well this estimation approach would apply to more advanced CMOS technologies. The much smaller feature sizes of deep-submicron process would likely reduce estimation accuracy through the introduction non-ideal effects (e.g., short channel effects). However, the approach may serve as useful guideline for identifying general rules for modeling parasitic devices even in highly scaled technologies.

Consideration of As-Drawn Transistor Channel Geometry

When analyzing the parasitic FOXFET, it is also necessary to determine if the structure of the as-drawn transistor gate geometry impacts the current conduction of the parasitic inter-device structure. To determine the effect of the as-drawn NMOSFET design on FOXFET operation, we obtain experimental current-voltage characteristics for all devices using a modified measurement setup. Specifically, we measure the inter-device FOXFET configured such that only one of the two n+ diffusions acts as the FOXFET drain. Unlike, the previous measurements, the other diffusion is left floating during this test. To consider both possibilities, the current-voltage measurement was performed in two configurations on each test structure. However for the analysis we focus only on the layout and results of the layout shown in Fig. 3.18(f).

For measurement Configuration 1, we utilize the NMOSFET n+ drain diffusion as the FOXFET drain node, while floating the NMOSFET source, and Configuration 2 utilizes the NMOSFET n+ source diffusion as the FOXFET drain node, while floating the NMOSFET drain. Both Configurations 1 and 2 are denoted by overlaid arrows and labels on Fig. 3.18(f). In both measurement configurations the current-voltage response of the parasitic FOXFET was obtained in a diode-connected configuration to record the drain current vs. gate voltage response. The FOXFET gate (polysilicon interconnect) and “drain” (one or the other n+ diffusion) were swept

from 0 V to 35 V using 1 V steps and the FOXFET source (n- substrate) and body (p-well) were both held at ground.

The experimental results for the parasitic FOXFET in Fig. 3.18(f), measured in both Configurations 1 and 2, are shown in Fig. 3.21. The resulting current-voltage response shows very similar responses for both measurement configurations. This indicates that the impact of the increased path length underneath gate oxide (i.e., along the NMOSFET channel) has little measureable impact on the parasitic FOXFET's current response. The observed agreement between test configurations is consistent for all other devices tested. Note that the experimental FOXFET current data has been normalized to a 1 μm wide device by dividing by the FOXFET width of 3 μm, resulting in units of amps per micrometer. This is done to allow for comparison with two-dimensional simulation results.

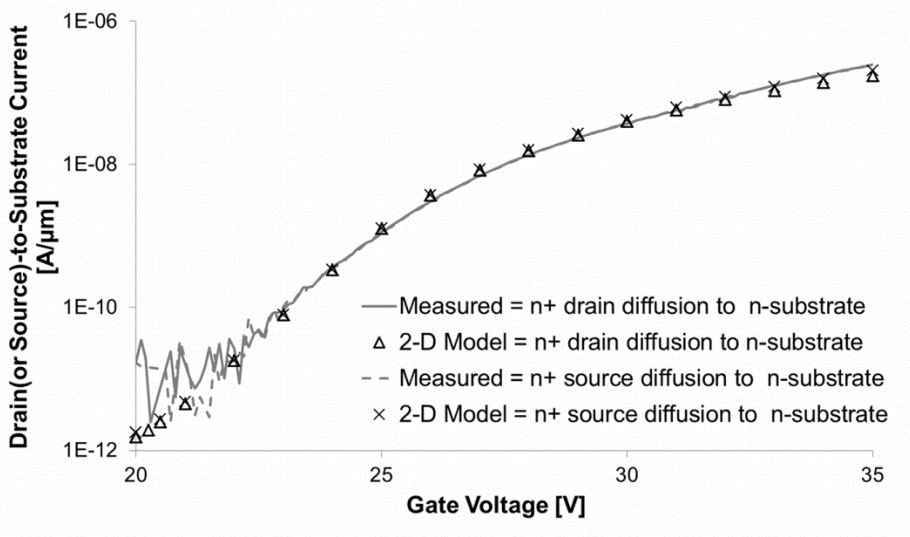


Fig. 3.21 Experimental measurements (lines) versus Silvaco TCAD model simulation (symbols) current-voltage results, completed in Configuration 1 and 2.

Technology computer-aided design (TCAD) simulations in the Silvaco ATLAS environment were employed to augment the experimental testing. By utilizing process information such as doping densities, gate thickness and field oxide thickness, two different 2-D structures representative of the inter-device paths of Configuration 1 and 2 were created. The Silvaco structures, representative of Configurations 1 and 2 are shown in Fig. 3.22 and Fig. 3.23, respectively. Both structures have identical doping profiles and oxide thicknesses. However the path length between the n+ diffusion and the field oxide "bird's beak" transition point is much longer in the structure of Fig. 3.23 compared to that of Fig. 3.22. Again, this longer path length replicates the geometric condition from n- substrate to n+ source diffusion seen in Fig. 3.18(f). Both structures are assumed to have a nominal width of 1 μm, the default value for 2-D structures in Silvaco.

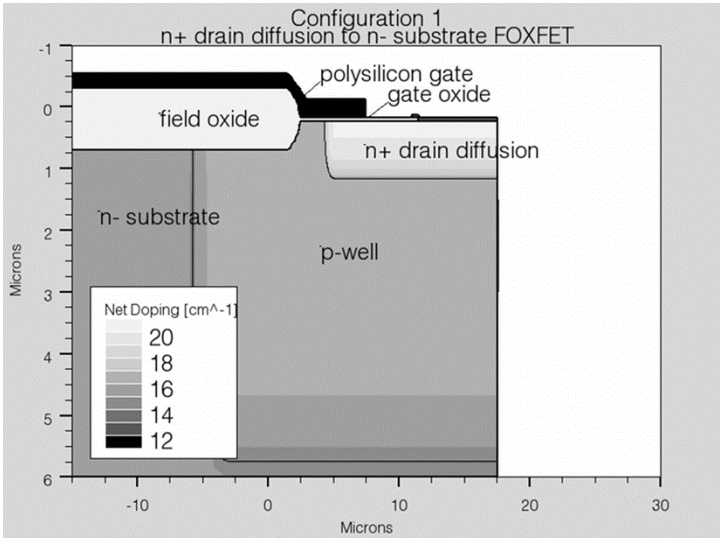


Fig. 3.22 2-D structure used to model configuration 1, the FOXFET between n+ drain diffusion and n- substrate.

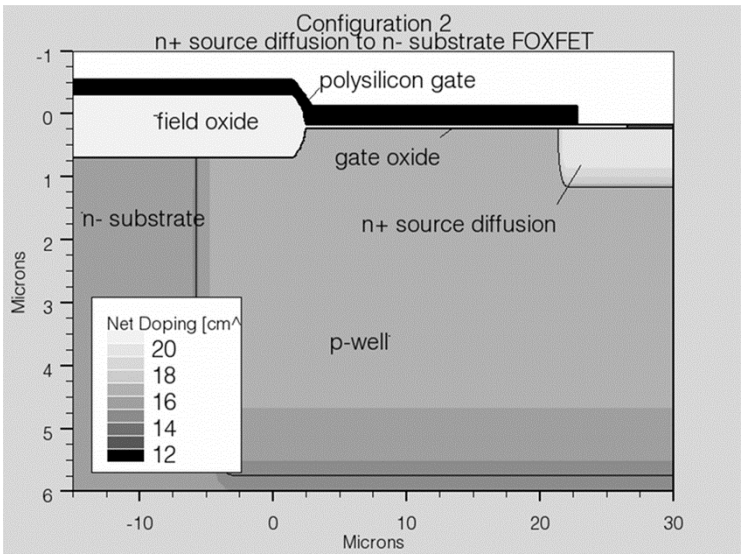


Fig. 3.23 2-D structure used to model configuration 2, the FOXFET between n+ source diffusion and n- substrate.

The simulation results for both 2-D TCAD configurations are shown in Fig. 3.21. The close match between simulations and measurements demonstrated that the increased path length underneath gate oxide (i.e., along the MOSFET channel) has little measureable impact on the parasitic FOXFET's drain current response. Rather, the FOXFET current conduction, which is a function of FOXFET aspect ratio, is almost solely determined by the polysilicon path dimensions over field oxide as it extends across the p-well to the n-substrate boundary. This leads us to conclude that the n+ diffusions do not define the active source/drain region of the parasitic FOXFET. Instead, it is the inverted channel under the thin-gate oxide along with the n-substrate that defines the drain and source of the FOXFET. Since the channel is created at a lower gate voltage than the region under field oxide, the as-drawn MOSFET channel is already well established as the FOXFET "channel" begins to invert and conduct current.

By discounting the effect of the as-drawn transistor gate geometry, the analysis presented above supports the FOXFET aspect ratio estimations presented in the previous section.

Hardening-By-Design Implications

In the previous sections, analysis was performed on parasitic FOXFETs of various layout configurations. From experimental measurements and 2-D modeling, generalized rules were developed to approximate effective width/length ratios for the parasitic FOXFETs laid out on the test coupon. Of course, designers will most likely not have a similar test coupon available in their technology. However a few simple, two-edge, FOXFET test structures will often be included in most process monitors in any given technology. By characterization of the pre- and post-radiation current-voltage response of their limited set of FOXFETs, a determination of the radiation tolerance of the isolation oxides for the technology can be made. The collected data can then be easily utilized for the creation of a compact model set, with one accurate compact model for the parasitic FOXFET at each collected total dose level. Compact models can thus be generated for the parasitic FOXFETs in a similar fashion as the as-drawn MOSFETs, scalable by width and length.

Once a compact model set is generated, a designer can then examine their circuit layout and locate all parasitic FOXFETs present on the IC. Application of the rules presented in this paper allows for the determination of width/length ratios of for any complex FOXFETs identified. The designer can then couple their FOXFET compact model set and effective aspect ratios for the identified FOXFETs into the original schematic. This is achieved by a) back-annotating all FOXFETs into schematic, b) assigning width/length ratios as determined from layout to the back-annotated devices, and c) pairing a single scalable FOXFET compact model to all FOXFETs. The choice of FOXFET compact model from the model set effectively chooses the total dose level for a radiation-enabled circuit simulation. This methodology for compact

modeling, back-annotation and circuit simulation was successfully demonstrated previously in the charge pump case study [63].

The ability to include the FOXFET in circuit simulation allows the designer to judge the impact of all parasitics on circuit operation at a given dose. The designer can then examine each FOXFET, weigh the potential degradation caused by each post-irradiated parasitic, and then apply published radiation hardening by design techniques to modify their circuit as they see fit, such as selectively eliminating parasitics to minimize inter-device leakage contributions while balancing other IC design goals] [21, 66]. Rapid feedback through simulation allows targeted RHBD modifications to be made while avoiding wholesale process or design rule changes.

Summary of inter-device leakage modeling

Inter-device parasitic current leakage due to total dose effects is a significant concern for any IC that could be exposed to radiation. Charge trapping in field isolation oxides leads to activation of parasitic FOXFETs, reducing circuit performance and potentially leading to operational failure. Radiation hardening strategies can be implemented to mitigate parasitics. Ideally, designers will be able to predict performance early in the design cycle. Simulation of circuitry with parasitic FOXFETs included allows for pre- and post-irradiation simulation of the circuit early in the design process supporting radiation-hardening-by-design activities, which improve radiation tolerance.

In the presented case study, total ionizing dose exposure data on the dual charge pump circuit shows a significant reduction of the internally generated –3×VDD supply rail with applied dose. To investigate the root cause of the reduction, PM devices were irradiated and electrically characterized. The PM test data indicate a significant buildup of N_{ot} in the LOCOS base of the

FOXFET structure in which leads to a significant reduction in FOXFET threshold voltage leading to inter-device leakage that loads the –3×VDD supply rail causing voltage collapse.

From the PM dataset additional 2-D ATLAS models were developed. Utilizing both experimental and simulated device data allowed for the creation of a comprehensive compact model library for the FOXFET. Back-annotating the FOXFET devices into the original schematic and re-simulating with each model of the library effectively sweeps total dose in simulation. Reproducing the voltage collapse in simulation validates the approach as well as allows for changes to be made to the IC layout and/or schematic to increase radiation hardness.

Further analysis of the FOXFET geometry effects was then presented. A test coupon IC, which includes structures designed for investigating total dose ionizing radiation effects, was designed and fabricated. Pre- and post-irradiation current-voltage response data shows that the parasitic FOXFET is an active device. To judge the impact of such inter-device currents in circuit simulation, width/length scalable compact models must be developed for the FOXFET. Additionally for accurate compact model development, the geometric effects of the parasitic FOXFETs must be quantified to accurately assign device aspect ratios. Experimental data on an array of test devices allowed for calculation of effective width/length ratios, which were compared to our own estimation techniques based on layout geometries. Additional investigations into the impact of the NMOSFETs geometric structure, which lies adjacent to the FOXFET, reveal that the FOXFET aspect ratio is determined only by the interconnect geometry and does not depend on the as-drawn transistor geometry.

Utilizing the presented rules to determine an effective width/length ratio for the parasitic FOXFET, the layout of a given circuit and a basic compact model set for the FOXFETs in a given technology allows for radiation-enabled circuit simulation. Such simulations allow for pre-

and post-irradiation modeling of the circuit early in the design process supporting targeted radiation-hardening-by-design.

CHAPTER 4

SIMULATION OF COMBINED INTRA-DEVICE EFFECTS

As outlined in Chapter 2, total dose exposure can lead to oxide trap buildup in both gate oxide trapped charge as well as oxide trapped charge buildup in isolation oxide sidewalls. In both NFETs and PFETs, oxide trapped charge in gate oxides causes a decrease in transistor threshold voltage. Additionally in an NFET, oxide trapped charge in isolation oxide sidewall can drastically increase off-state leakage, and is thought of as a parasitic NFET in parallel with the as-drawn transistor. Both effects within an NFET are illustrated in Fig. 4.1. In this case study, the total dose response of a ring oscillator is investigated. It is found that intra-device effects, specifically trapped charge buildup in gate and sidewall isolation oxides, are responsible for a change in oscillation frequency. Through modeling and simulation, the experimental results are recreated, illustrating a methodology that can be applied to other circuits.

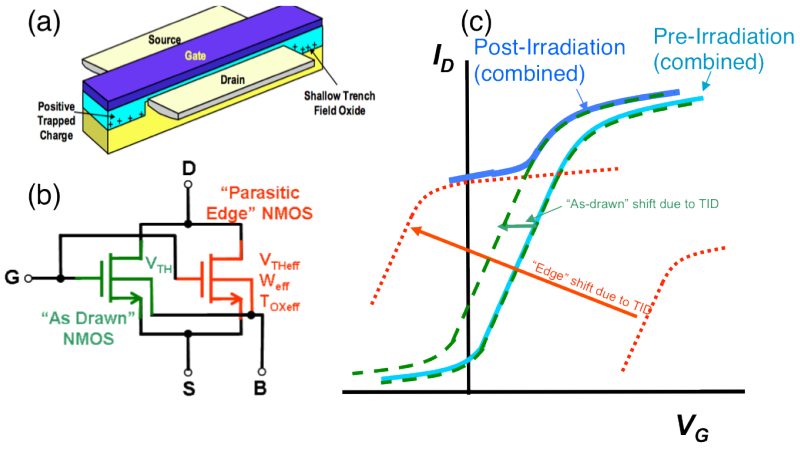


Fig. 4.1 (a) STI isolated transistor showing trapped-charge location corresponding with intra-device edge leakage current, (b) representative sub-circuit of the NFET with parasitic edge device and (c) current-voltage characteristics of gate-oxide and a parasitic "edge" transistor showing increase in off-state current post-irradiation due to the parasitic edge transistor [18, 39].

Case Study – the Ring Oscillator

Ring oscillators (ROs) are a widely used circuit topology, both as part of larger integrated circuits as well as implemented as monitors to gauge process variability and circuit aging. Phase-locked-loops often utilize ROs in their voltage controlled oscillator blocks in favor of LC oscillators as ring oscillators have a large tunable frequency range and improved manufacturability, since CMOS devices require significantly less die area than large passive elements. Process and reliability monitors are also common RO applications [67, 68]. Monitoring RO frequency response is advantageous since (a) test conditions reproduce many of the stress conditions of actual circuit applications, (b) variability in transistor operation is averaged over all devices in the RO, and (c) simple output frequency measurements can quickly quantify degradation. Along with process variability and degradation caused by circuit aging the effects of total ionizing dose (TID) on ROs must be fully considered if radiation exposure is a possibility. In this work we investigate TID effects on a RO manufactured in a high-reliability, high voltage (HV) 0.25 μm process via experiment and radiation-enabled simulation [69-71]. A circuit simulation of total dose effects is not a new concept [72-75]. However the work presented here builds on previous work, illustrating a new methodology for modeling radiation effects in CMOS [76]. Additionally the presented in-depth analysis of the HV RO response and resulting discussion motivates further use of ROs to model and monitor total dose degradation for TID-sensitive technologies.

The simplest RO designs are composed of an N number of delay stages, where N is an odd number. Often these delay stages are made up of simple CMOS inverter. The ring is completed by coupling together the output of the N^{th} stage to the input of the 1^{st} stage. In order to achieve oscillation the ring circuit must provide 360˚ of phase shift, with each stage providing

360˚/N of phase shift. Thinking of the ring in terms of each stage's digital input/output, if the 1st stage receives a digital "0" input it will supply a digital "1" to the 2nd stage, which will provide a digital "0" to the 3rd stage. This pattern continues as the last, odd numbered, Nth stage receiving a digital "0" input and feeding back a digital "1" back to 1st stage's "1" input. This autonomous change in digital state of 1st stage's input facilitates oscillation. This process then continues indefinitely and the circuit oscillates as long as the circuit remains powered. The oscillation frequency of the ring is a function of the delay through each stage (t_d). In order for the signal to go through the entire circuit once it would take $N \times t_d$, achieving a phase shift of 180˚. To complete one full period the signal must pass through the circuit once again, taking a total time of $2N \times t_d$. From the period the frequency can be expressed as

$$F = \frac{1}{2N \times t_d} \tag{5.1}$$

If a RO is implemented as part of a larger system, its oscillation frequency is its most important characteristic, thus understanding it's response over time or under any various stress conditions is of key importance. As described in the previous section, the deleterious effects of ionizing radiation will affect the operation of each inverter stage, skewing stage delay. Previous work in legacy technologies has reported experimental results on ROs following TID exposure and observed shifts in the operation frequency. Changes in frequency are attributed to shifts in N and PFET threshold voltages [70, 71]. More recent work at the 130 nm technology node again observed changes in operational frequency following irradiation, but at this node, shifts in as-drawn NFET and PFET threshold voltage are minimized due to ultra-thin gate oxides. Rather, RO frequency changes following total dose exposure are attributed to activation of the parasitic edge transistor, which is still a serious reliability concern even in advanced technologies [69].

Some high-reliability applications also require high voltages, such as implantable medical devices. These devices CMOS technologies still implement thick oxides as well as STI isolation, both of which are susceptible to total dose degradation. The results presented in this work are no exception. In this work we explore TID effects on a RO manufactured in a high-reliability, high voltage (HV) 0.25 μm process via experiment and radiation-enabled simulation of the ring oscillator. As will be shown, in this high reliability, high voltage process the effects of as-drawn (NFET and PFET) threshold shift as well as activation of the parasitic edge transistor must all be considered.

Experimental Setup

In this work, an integrated test coupon, manufactured in a high voltage 0.25 μm technology, containing various test circuits and individual transistors was utilized. Available within the coupon is a RO circuit, as well as the individual test transistors corresponding to devices within the oscillator. The RO consists of 1002 inverter stages as well as one tri-state inverter with a control input (Enable) to toggle the feedback loop on/off. The RO has individual pins for Input, Output, Enable and both V_{DD} and V_{SS} supply rails. Each stage consists of one 2.5 μm/1.2 μm HV PFET and one 2.5 μm/1.4 μm HV NFET, capable of supporting up to 20 V. Both N and PFETs have a nominal gate oxide thickness of 60 nm and utilize recessed shallow trench isolation (STI) with a nominal thickness of 350 nm. In addition to the oscillator circuit, individual N and PFETs with various aspect ratios were also characterized.

The electrical characteristics of two identical RO circuits were measured prior to exposure (0x) and after 6 total dose irradiation stress steps (1x, 2x, 4x, 6x, 10x, and 20x). For the RO characterization, the circuit was allowed to oscillate and the operational frequency and

supply current draw was measured. For this measurement, a V_{DD} of 1.5 V is utilized as it yields the greatest sensitivity to total dose, as will be explained in later sections. For the individual transistors, current-voltage measurements were performed seven times, once before irradiation, and after six irradiation stress steps. Radiation exposure was performed in an x-ray irradiator (120 kVp, 10 mA source with a 230 mm source to surface distance). All irradiations and electrical characterizations were performed at room temperature.

The ROs were biased during irradiation in two different configurations. Condition "C1" consisted of grounding all RO pins, so that all FET terminals were grounded. Condition "C2" consisted of biasing the RO Input and V_{DD} supply rail to 20 V while grounding V_{SS} and Enable. The C2 configuration forces the inverter chain into a static bias, disabling the feedback and preventing oscillation. In this condition each odd stage receives an input bias of 20 V while each even stage receives an input bias of 0 V. Configurations C1 and C2 capture the "best" and "worst" case irradiation bias conditions, respectively. To duplicate the circuit irradiation bias conditions the individual transistors were biased in 2 configurations. Configuration "T1" consisted of grounding all FET terminals (drain, gate, source, body) for all PFETs and NFETs tested. Configuration "T2" replicates worst case bias conditions; i.e., drain, source and body terminals are grounded for all NFETs and PFETs tested, and NFET gates were biased to +20 V while PFET gates were biased to -20 V. The bias conditions are summarized below in Table 4.1

Table 4.1 Summary of circuit and transistor irradiation bias conditions utilized. Best- and worst-case correspond to the least and most potential bias-dependent total-dose degradation, respectively.

	Circuit (Ring Oscillator) Bias Condition		**Transistor (NFET and PFET) Bias Condition**	
Bias Condition Label	C1	C2	T1	T2
Description	Best-Case Circuit Bias V_{DD}=IN=0V V_{SS}=EN=0V	Worst-Case Circuit Bias V_{DD}=IN=+20V V_{SS}=EN=GND	Best-Case Bias	Worst-Case Bias
NFET Bias	G=D=S=B=0V For all NFETs	G=+20V D=S=B=0V For 50% of NFETs G=S=B=0V D=+20V For 50% of NFETs	G=D=S=B=0V	G=+20V D=S=B=0V
PFET Bias	G=D=S=B=0V For All PFETs	G=D=B=S=+20V For 50% of PFETs G=D=0V S=B=+20V For 50% of PFETs	G=D=S=B=0V	G=−20V D=S=B=0V
Corresponds To	T1	T1 & T2		

Experimental Results - Ring Oscillator

Pre- and post-irradiation test results for the RO are shown in Fig. 4.2 and Fig. 4.3. It is seen that for both irradiation bias configurations the RO operation frequency changes non-linearly with increasing dose. For the "worst case" bias configuration (C2) the RO fails to operate past the 4th total dose stress step level (6x). The supply current of the RO shows a dramatic increase in supply current draw at this stress step level.

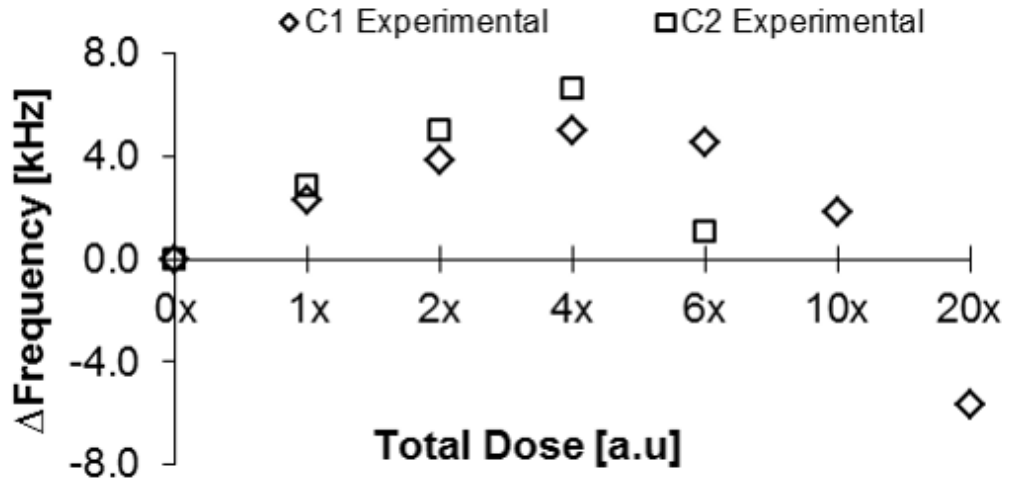


Fig. 4.2 Experimentally observed change in RO frequency vs. total dose. Shown are results for irradiation bias configurations C1 and C2. Pre-irradiation RO frequency is ~50 kHz at a supply voltage V_{DD} = 1.5 V.

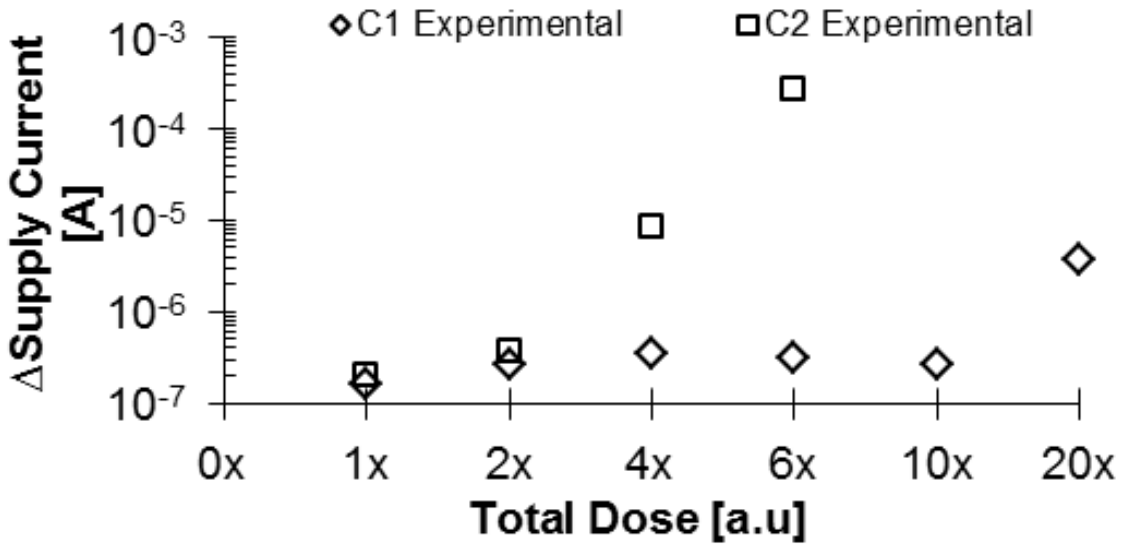


Fig. 4.3 Experimentally observed RO supply current vs. total dose. Shown are results for irradiation bias configurations C1 and C2. Pre-irradiation average supply current is ~4 μA, at a supply voltage of 1.5 V.

Experimental Results - Individual Test Transistors

Pre- and post-irradiation characterization of individual N and PFETs reveal decrease in both V_{Tn} and V_{Tp}, indicative of positive oxide trapped charge buildup (N_{ot}) in the gate oxide, as seen in Fig. 4.4. Additionally, for "worst case" irradiation bias configuration T2 (Fig. 4.5), the

NFETs exhibited significant increases in off-state current (I_{off} = I_D @ V_{GS}=0 V) indicative of N_{ot} buildup along the STI sidewall [34].

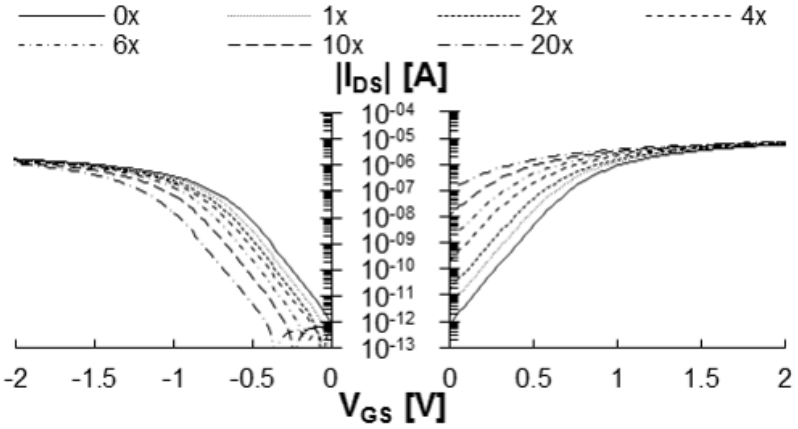


Fig. 4.4 $|I_D|$ vs. V_{GS} (V_{DS}=100 mV) characteristics of PFET (left) and NFETs (right) pre-irradiation and after 6 total dose irradiation step stress levels. Shown are experimental TID results utilizing irradiation bias configuration T1.

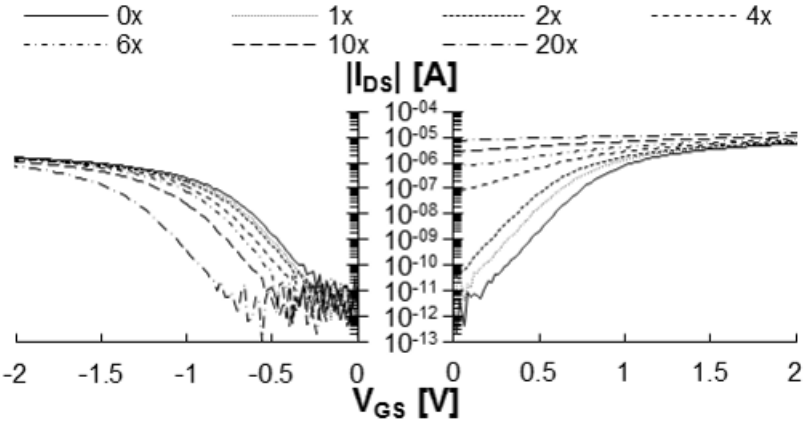


Fig. 4.5 $|I_D|$ vs. V_{GS} (V_{DS}=100mV) characteristics of PFET (left) and NFETs (right) pre-irradiation and after 6 total dose irradiation step stress levels. Shown are experimental TID results utilizing irradiation bias configuration T2.

Analysis

To understand the experimental results presented, analysis of the results is needed. RO oscillation frequency (*F*) can be expressed by Eq. 4.1, where *N* is the number of stages and t_d is

the average stage delay. The number of stages remains constant post-irradiation, thus a total-dose induced change in delay brings about the measured change in frequency. Average stage delay can be expressed by the average of propagation delays in the expression [77]

$$t_d = \frac{1}{2}\left(t_{pHL} + t_{pLH}\right), \tag{4.2}$$

where t_{pHL} is the high-to-low propagation delay and is defined as the time it takes the output drop to $V_{DD}/2$ when the inverter input is switched from low to high. Alternatively t_{pLH} is the low-to-high propagation delay of the inverter and is defined as the time it takes the output increase to $V_{DD}/2$ when the inverter input is switched from high to low. The high-to-low propagation delay is expressed as [77]

$$t_{pHL} = \frac{C}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n V_{DD}}\alpha_n, \tag{4.3}$$

where α_n is defined as [77]

$$\alpha_n = \frac{8V_{DD}^2}{7V_{DD}^2 - 12V_{DD}V_{Tn} + 4V_{Tn}^2} \tag{4.4}$$

Similarly the low-to-high propagation delay is expressed as [77]

$$t_{pLH} = \frac{C}{\mu_p C_{ox}\left(\frac{W}{L}\right)_p V_{DD}}\alpha_p \tag{4.5}$$

where α_p is defined as [77]

$$\alpha_p = \frac{8V_{DD}^2}{7V_{DD}^2 - 12V_{DD}\left|V_{Tp}\right| + 4\left|V_{Tp}\right|^2} \tag{4.6}$$

Equations (4.3) and (4.5) include parameters that do not change with increasing total dose: oxide capacitance (C_{ox}), device geometry (W, L), supply voltage (V_{DD}) and the lumped internal capacitance of the inverter (C). Although in general, TID can impact mobility (μ), the data show this not to be the case for the dose levels used in the experiment. Focusing on (4.4) and (4.6), it is evident that α_n and α_p will be affected by total dose due to changes in threshold voltage. From Fig. 4.4 and Fig. 4.5 it is seen that the NFET threshold voltage (V_{Tn}) is decreased while the magnitude of the PFET threshold voltage ($|V_{Tp}|$) is increased. However, the resulting effect on α_n and α_p are not immediately evident. Fig. 4.6 illustrates the change in these parameters with change in threshold voltage (or increased total dose) at selected V_{DD} voltages. RO frequency has a strong dependence on supply voltage, as illustrated in previous work [69]. However, it is seen that only at the lowest V_{DD} voltage (1.5 V) do changes in threshold voltage noticeably impact α_n and α_p (and furthermore, RO frequency). Sensitivity at a V_{DD} of 1.5 V makes it an excellent characterization condition to gauge the effect of total dose on RO operation.

The alpha parameters directly impact the propagation delay in (Eq. 4.3) and (Eq. 4.5). Therefore it is seen that the decrease in NFET threshold voltage will decrease t_{pHL} while the increase in magnitude of PFET threshold voltage will increase t_{pLH}. Both of these delays directly relate to average delay and oscillation frequency via (Eq. 4.2) and (Eq 4.1), respectively. To summarize, decrease in NFET threshold voltage will increase RO frequency, while increase in the magnitude of PFET threshold voltage will decrease RO frequency. Examining Fig. 4.6 in relation to the observed frequency response (Fig. 4.2), it can be deduced that at lower total dose levels, the NFET response dominates due to greater NFET threshold voltage shift, increasing RO frequency. But, as exposure continues it is evident in Fig. 4.6 that the effect of NFET threshold shift saturates with increasing TID. Conversely the effect of PFET threshold voltage shift

becomes more pronounced at higher total dose levels. This combination results the downturn in the RO frequency following the 4x total dose stress step level in Fig. 4.2.

The TID dependencies of the propagation delays are valid for both RO bias conditions presented. However configuration C2 adds an additional component to the observed total dose response. In this condition the parasitic edge transistor becomes an active circuit element due to NFET STI sidewall conduction, exhibited by increased NFET off-state current (Fig. 4.5). The parasitic edge transistor exists in parallel with the as-drawn NFET and affects the inverter stage in 2 ways: increased I_{DS} current in the NFET's on-state, further decreasing t_{pHL} and greatly reduced the NFET off-state resistance. The reduction in off-state resistance inhibits the PFET's ability to charge the inverter output, increasing t_{pLH}. If the edge transistor is conducting high enough current, the PFET may not be able to fully charge the output node. This means the inverter stage will not provide a "good digital 1" (i.e. inverter output ≈ V_{DD}) to the next stage in the chain. The propagation of "poor digital 1" will eventually prevent oscillation.

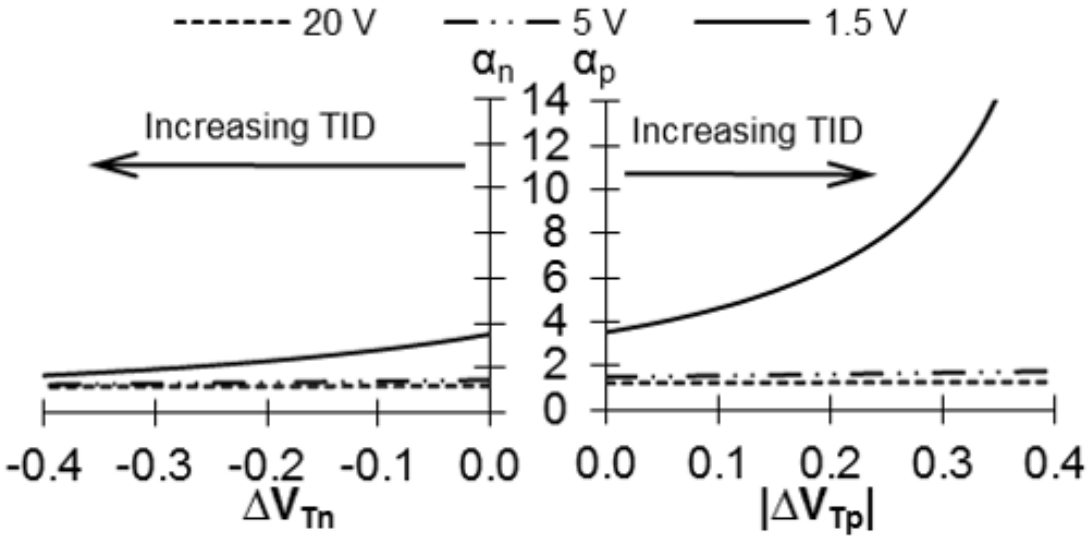


Fig. 4.6 α_n versus decrease in NFET threshold voltage (left) and α_p versus increase in magnitude of PFET threshold voltage (right) at V_{DD} voltages of 20 V, 5 V and 1.5 V.

Examining transistor bias configuration T1 (Fig. 4.4) it observed that NFET off-state current nears ~100 nA. At this stress step the off-state current is approximately one order of magnitude less than the on-state current. This manifests itself in the observed supply current spike at the 20x stress step level for bias configuration C1 in Fig. 4.3. Examining supply current response for bias configuration C2 in Fig. 4.3, it is seen that the supply current spikes at lower total dose, the 6x stress step level. Additionally it is noted that the oscillator fails to oscillate for bias configuration C2 at total doses greater than the 6x stress step level (Fig. 4.1). This current spike and failure to oscillate corresponds to significant NFET off-state leakage (i.e. > 100 nA) for bias configuration T2 as seen in Fig. 4.5. To capture all of these effects on RO operation concurrently it is necessary to implement the effects of total dose in circuit simulation.

Simulation Details

To model reduction in the NFET and PFET threshold voltages with increasing total dose, the linear extrapolation method is applied to every current-voltage curve illustrated in Fig. 4.4 [78]. This proves relatively simple for the first bias condition (i.e. T1) as the only effect contributing to shifts seen in is a reduction of the as-drawn threshold voltage. However, for the second radiation bias condition (i.e. T2 shown in Fig. 4.5) inclusion of the parasitic-edge transistor adds complexity to threshold voltage extraction. It proves difficult as contributions from as-drawn and parasitic edge are hard to differentiate in the narrow width (2.5 μm) I-V data. Here the parasitic edge and as-drawn transistors have similar aspect ratios, thus can conduct similar I_{DS} current, preventing linear extrapolation of V_{Tn}. However, utilizing wide width (20 μm) NFET total dose data (Fig. 4.7) current contributions are better differentiated and V_{Tn} can be obtained. For the purposes of the total dose simulation, the change in threshold voltage is of key

importance at each TID step. The results of threshold voltage extraction are shown in Fig. 4.8, for both irradiation bias conditions T1 and T2.

As described previously, the second radiation bias condition (i.e. T2) response of the parasitic edge transistor must also be quantified. For this condition, we cannot disregard the parasitic edge NFET and it must be included in the NFET model, along with the as-drawn NFET. To translate the effects of the as-drawn and parasitic edge NFETs into simulation, the change in as-drawn NFET operation is again modeled by reducing V_{Tn} (as shown in the previous section) while activation of the parasitic edge NFET is modeled by three total dose dependent parameters (W_{eff}, t_{OXeff} and V_{Teff}) [40].

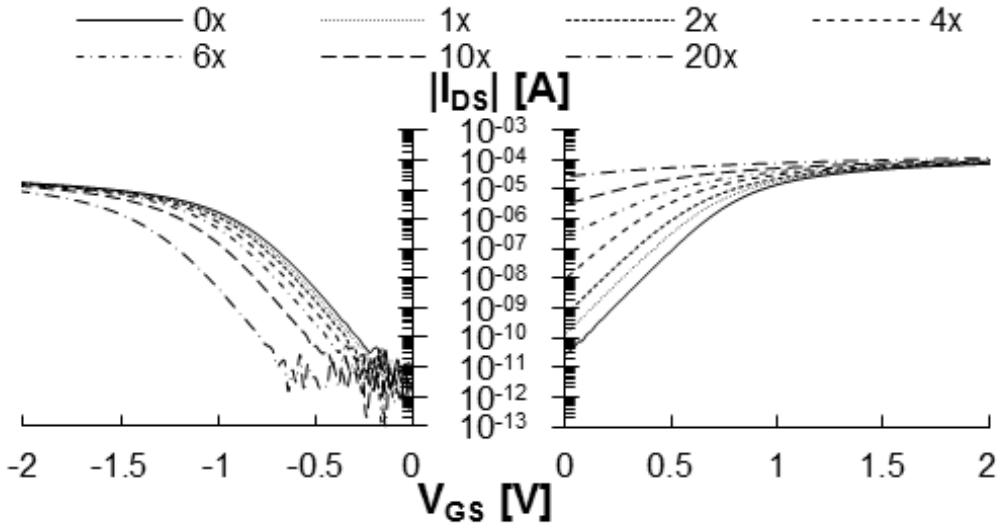


Fig. 4.7 $|I_D|$ vs. V_{GS} (V_{DS}=100mV) characteristics for W/L = 20 µm / 1.4 µm PFET (left) and NFET (right) pre-irradiation and after 6 total dose irradiation step stress levels. Shown are experimental TID results utilizing irradiation bias configuration T2.

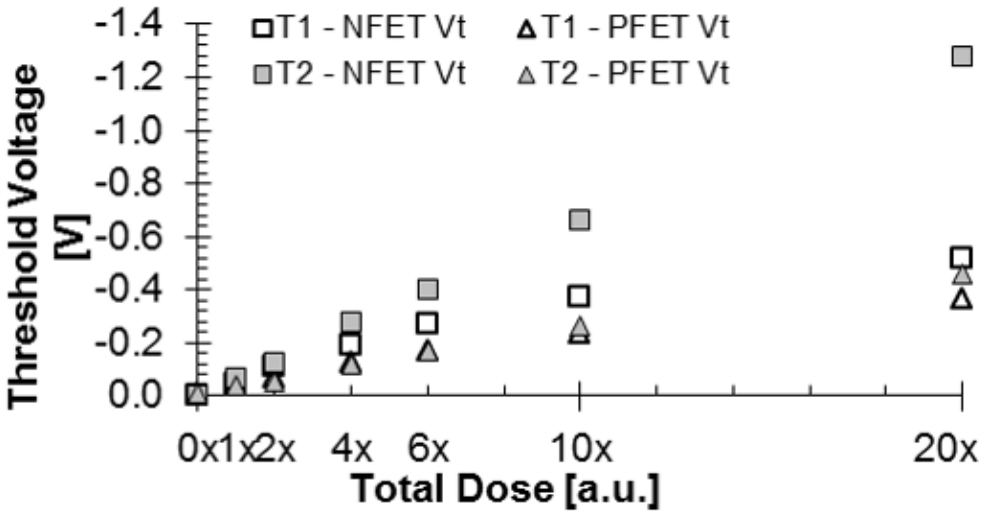


Fig. 4.8 Extracted NFET and PFET threshold voltages versus increasing total dose. Results shown are extracted from a W/L=2.5 µm /1.4 µm PFET experimental data for both bias conditions (T1 and T2). Alternatively W/L=2.5 µm /1.4 µm NFET data was used for bias condition T1 and W/L=20 µm /1.4 µm NFET for bias condition T2.

These three parameters can be determined by analytically fitting experimental off-state current ($I_{off} = I_{ds}$ @ V_{gs}=0 V) with increasing total dose (Fig. 4.9 and Fig. 4.10).

The following procedure was used to obtain the fits shown. First, I_{off} is extracted at each total dose (squares in Fig. 4.9 and Fig. 4.10) from individual NFET I-V characterization curves. Next, the subthreshold current equation [79]

$$I_{off} = I_{ds}\left(V_{gs} = 0\right) = \mu_{eff}\frac{\varepsilon_{ox}}{t_{ox}}\frac{W}{L}\left(m-1\right)\left(\frac{kT}{q}\right)^{2} e^{q\left(-V_{Tn}\right)/mkT}\left(1-e^{-qV_{ds}/kT}\right) \tag{5.1}$$

is applied to analytically calculate I_{off} for the as-drawn device. Here μ_{eff} is the electron mobility (~500 cm^2/V-s), ε_{ox} is the permittivity of SiO_2 (3.9ε_o), t_{ox} is the oxide thickness (~60 nm) and drain-to-source voltage (0.1 V). Variable m is expressed as

$$m = 1 + \frac{\sqrt{\left(\varepsilon_{Si} q N_A\right) \Big/ \left(4 \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)\right)}}{\varepsilon_{ox} \Big/ t_{ox}} \tag{5.2}$$

where ε_{Si} is the permittivity of Silicon ($11.7\varepsilon_o$), N_A is substrate doping (10^{17} cm^{-3}) and n_i is the intrinsic carrier concentration (10^{10} cm^{-3}). If threshold voltage (V_{Tn}) is less than 0 V then (7) becomes [79]

$$I_{off} = I_{ds}\left(V_{gs} = 0\right) = \mu_{eff} \frac{\varepsilon_{ox}}{t_{ox}} \frac{W}{L}\left(-V_{Tn} - \frac{V_{ds}}{2}\right)V_{ds} \tag{5.3}$$

Utilizing these equations and the extrapolated V_{Tn} from the wide (W=20 μm) NFET at each total dose (Fig. 4.7), the as-drawn I_{off} is calculated (dotted lines in Fig. 4.9 and Fig. 4.10). Then, using the same equation applied to the parasitic edge device, I_{off} of the parasitic edge is calculated (dashed lines in Fig. 4.9 and Fig. 4.10). In this calculation, the parasitic edge parameters W_{eff}, t_{OXeff} and V_{Teff} are used. By summing the as-drawn and parasitic edge I_{off}, the combined analytical off-state current (solid lines in Fig. 4.9 and Fig. 4.10) is achieved. With the analytical I_{off} fitting experimental I_{off} (square symbols in Fig. 4.9 and Fig. 4.10), the parasitic edge parameters (W_{eff}, t_{OXeff} and V_{Teff}) are obtained. The combined analytical I_{off} is deemed to have a good fit once it is within ±10% agreement with experimental I_{off} values at each of the total dose stress steps. The resulting extracted parameters can be seen in Fig. 4.11. It is important to emphasize that the same parasitic edge parameters (shown in Fig. 4.11) were used to achieve analytical fit illustrated in Fig. 4.9 and Fig. 4.10.

The parasitic edge transistor is not a "designed" device, thus it does not exist as part of the standard 0.25 μm HV technology libraries. A new BSIM3 compact model must be created.

This is accomplished by modifying the standard HV NFET compact model for the creation of a new NFET edge compact model. Similar to the modifications made to the as-drawn NFET compact model, the NFET edge VT0 parameter is initialized with a total dose dependent variable (V_{Teff}). Additionally, to model the edge device compact model parameter TOX is initialized to a total dose dependent variable (t_{OXedge}). These two parameters, along with a total-dose-dependent gate width (W_{eff}) allow for mapping of the previously extracted parasitic edge transistor parameters (W_{eff}, t_{OXeff} and V_{Teff}) into the Spectre tool.

To implement the newly created NFET edge compact model and the extracted parasitic edge transistor parameters as part of the RO simulation, a new circuit element must be generated. A new 4 terminal NFET symbol was created and added to the 0.25 μm HV technology library, representing the parasitic edge transistor. Then this new library device was placed in parallel to the original (as-drawn) NFET library device as part of a new NFET sub-cell schematic. The new NFET sub-cell containing two parallel NFETs (as-drawn and parasitic) is used by directly replacing all NFETs in every inverter stage of the RO.

Implementing the described simulation technique does create one complication. Bias-dependent total dose simulation variables have been introduced into the compact model, however every RO NFET (or PFET) in the 1003 stage does not necessarily have identical bias conditions. Specifically, if one NFET is to receive a high bias (T2) and another a low bias (T1), this must be modeled in simulation by a change in threshold voltage (ΔV_{Tn} in the compact model) to both NFETs. This case occurs in the RO set to a circuit irradiation bias condition C2 and must be addressed to allow for accurate simulation.

To solve the bias-dependency issue the two as-drawn variables (ΔV_{Tn} and ΔV_{Tp}) and the parasitic edge transistor variables (t_{OXeff} and V_{Teff}) are instantiated in the Component Description

Format (CDF) within the 0.25 µm device library. This action is analogous to many other standard component properties such as gate width or length. A given device library transistor can have one compact model but can be implemented numerous times on schematic with varying device geometries. The CDF was modified for the as-drawn N and PFETs and the new parasitic edge NFET to allow instantiation of all total dose variables.

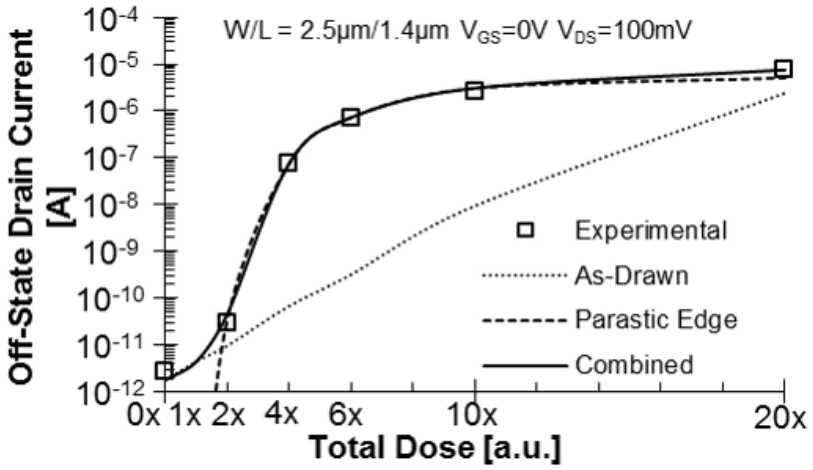


Fig. 4.9 Off-state drain current (i.e. I_D @ V_{GS}=0, V_{DS}=100mV) vs. total dose for a W/L = 2.5 µm / 1.4 µm NFET. Squares indicate experimental data while lines indicate analytical calculations.

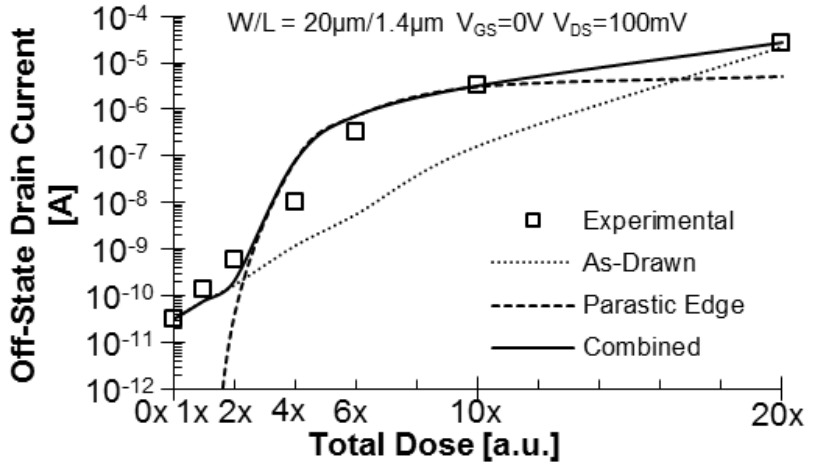


Fig. 4.10 Off-state drain current (i.e. I_D @ V_{GS}=0, V_{DS}=100mV) vs. total dose for a W/L = 20 µm / 1.4 µm NFET. Squares indicate experimental data while lines indicate analytical calculations.

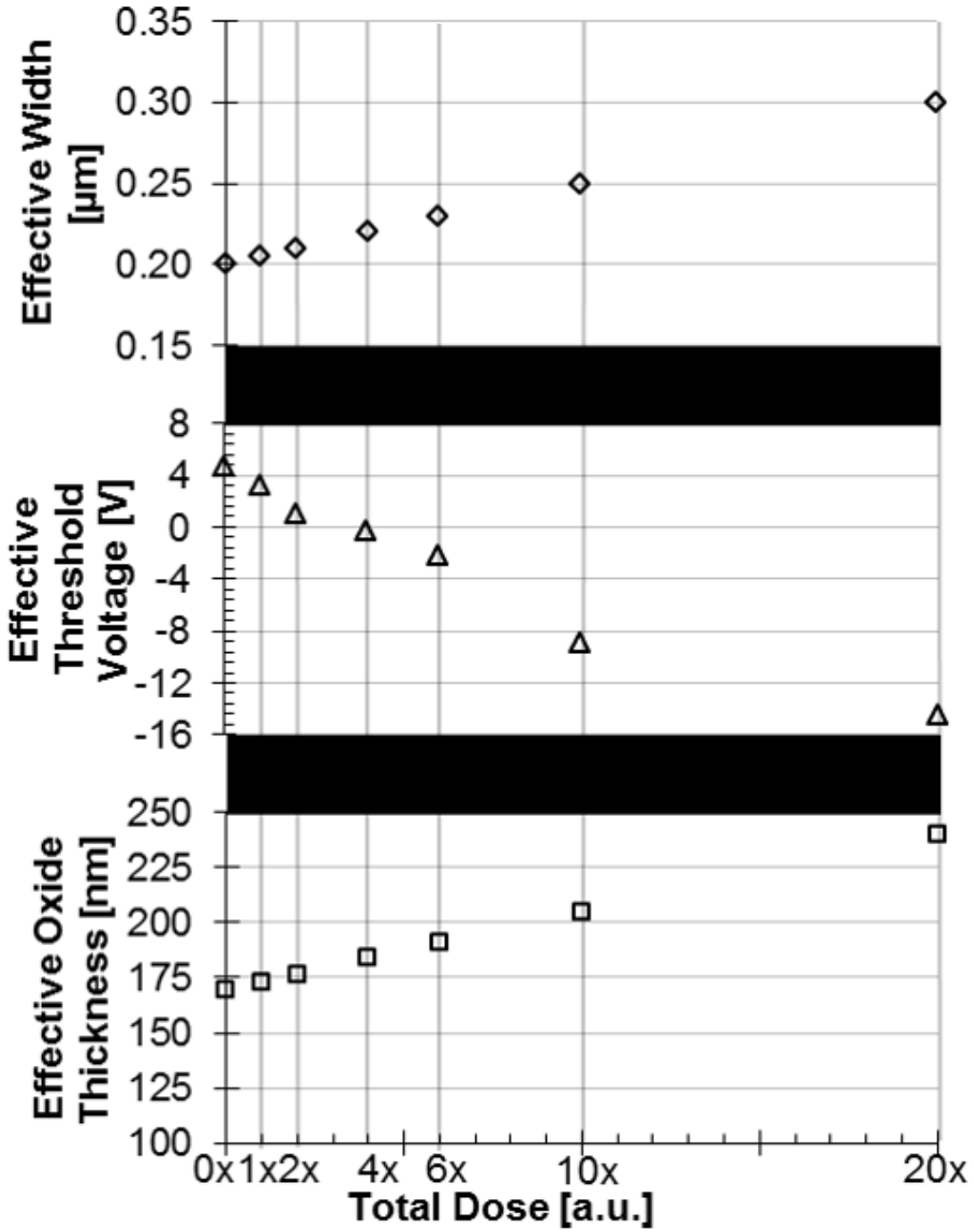


Fig. 4.11 Effective width (top), threshold voltage (middle) and oxide thickness (bottom) found for the parasitic edge transistor resulting from the fitting methodology illustrated in Fig. 4.9 and Fig. 4.10.

Simulation Results

Implementing the described methodology allows the total dose response of the N and PFET transistors to be simulated. This allows for comparison with the experimental data taken for both irradiation bias conditions, T1 and T2, as seen in Fig. 4.12 and Fig. 4.13, respectively. It is shown that total dose degradation of both the N and PFET is recreated in simulation, including the effects of parasitic NFET conduction as seen by the dramatic increase in off-state current above the 6x total dose step.

Based on the results of Fig. 4.12 and Fig. 4.13, it is expected that simulation of the RO circuit will also successfully recreate the total-dose response. Focusing first on circuit bias condition C1 (i.e. all terminals grounded) a transient simulation is performed utilizing the change in threshold voltage from transistor bias conditions T1. Simulation of average supply current and RO frequency shows good agreement with the measured total-dose response, as seen in Fig. 4.14 and Fig. 4.15.

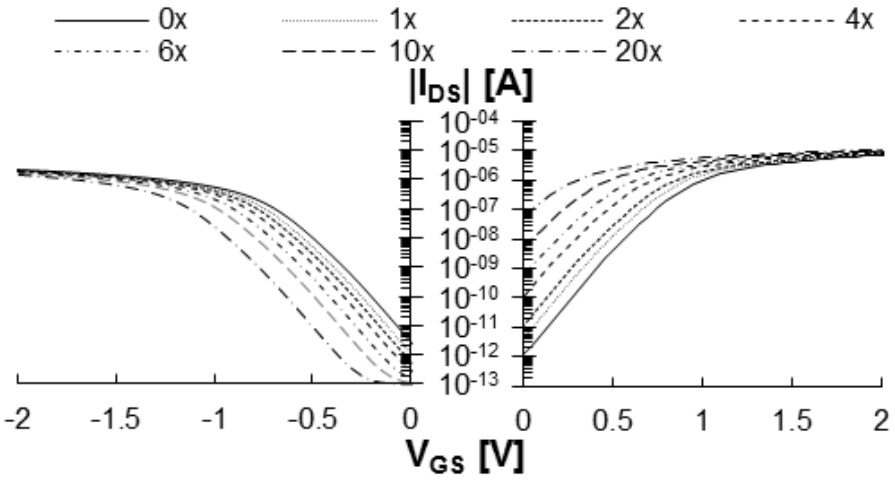


Fig. 4.12 Simulated $|I_D|$ vs. V_{GS} (V_{DS}=100 mV) characteristics of PFET (left) and NFETs (right) pre-irradiation and after 6 total dose irradiation step stress levels. Shown are TID results representative of irradiation bias configuration T1.

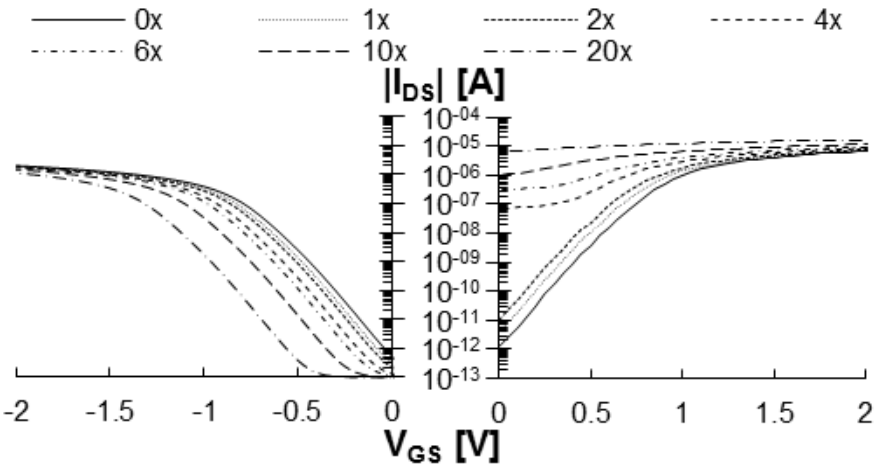


Fig. 4.13 Simulated $|I_D|$ vs. V_{GS} (V_{DS}=100 mV) characteristics of PFET (left) and NFETs (right) pre-irradiation and after 6 total dose irradiation step stress levels. Shown are TID results representative of irradiation bias configuration T2.

Next the circuit bias condition C2 is examined. In this case the simulation is slightly more complicated, as (a) the bias conditions for all NFETs and PFETs are not the same in the 1003 stage RO circuit and (b) the parasitic edge device is an active contributor for those NFETs biased "high" at transistor bias condition T1. When the RO is biased in configuration C2, half of the inverter stages receive a high input bias while the other half receives a low input bias. However, the previously described modifications made to the CDF allow simulation to address (a). The previously described analytical extraction method allowed quantification of the parasitic edge transistor response via its total-dose-dependent parameters (W_{eff}, t_{OXeff} and V_{Teff}). These parameters are implemented with a back-annotated parasitic edge NFET as part of the new NFET sub-cell, allowing for the simulation of the RO response as seen in configuration C2 in Fig. 4.1 and Fig. 4.2. Again, simulation correlates well with experiment, capturing the non-linear change in frequency, the spike in supply current and the subsequent failure to oscillate past the 6x total dose stress step.

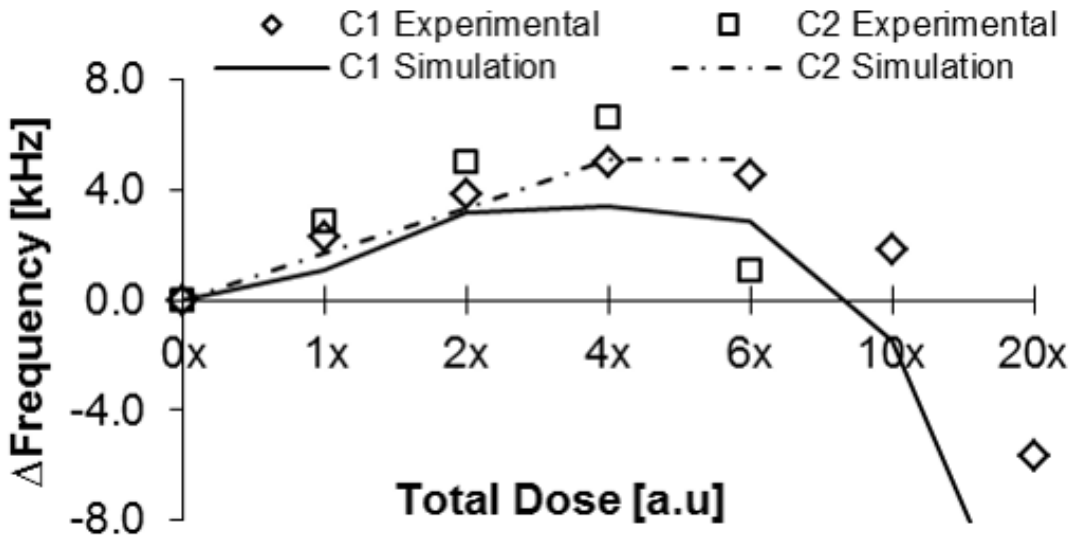


Fig. 4.14 Simulation of change in RO frequency vs. total dose. Shown are results representative of irradiation bias configurations C1 and C2 as defined in the text. Pre-irradiation RO frequency is ~50kHz at a supply voltage V_{DD}=1.5V.

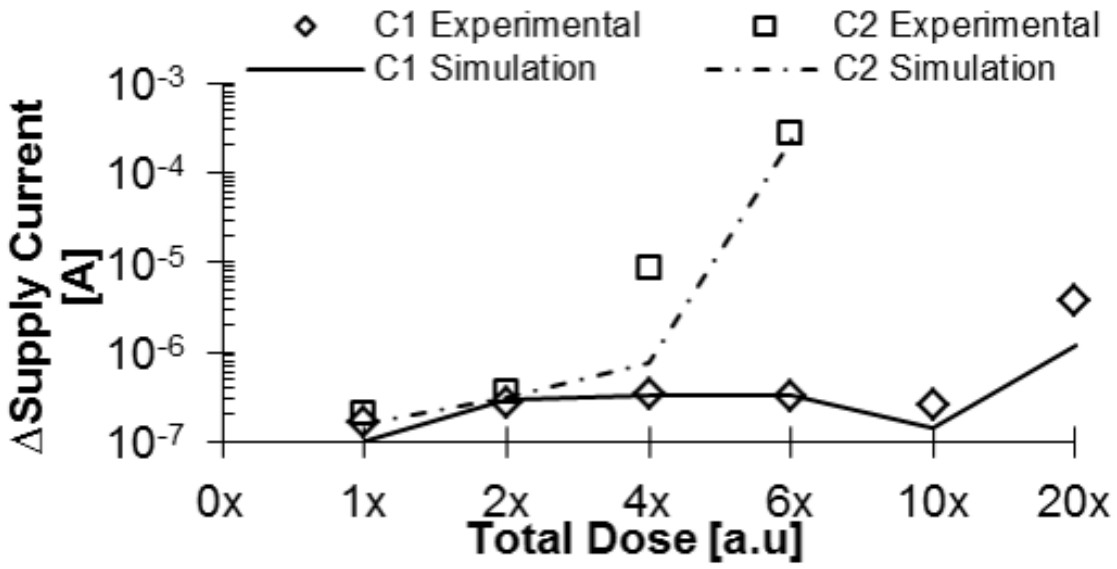


Fig. 4.15 Experimentally observed supply current vs. total dose. Shown are results representative of irradiation bias configurations C1 and C2 as defined in the text. Pre-irradiation average supply current is ~4μA at a supply voltage V_{DD}=1.5V.

Discussion

As discussed in the background section, a primary use of ring oscillators is for accurate voltage controlled oscillation. Using well-known methodologies for "edge-less" annular transistor layout, the effect of the NFET parasitic edge could be mitigated [62, 66]. However, the effect of total dose on the as-drawn NFETs and PFETs is difficult (or impossible) to mitigate since the high voltages required necessitate thick oxides. This requires an in-depth understanding of the technology's response to total dose. As such, the presented analysis and simulation methodology is applicable, as a given RO's response to total dose must be understood when utilized in a harsh environment setting. If the total dose response is well known, it is possible that operational corrections could be made to more accurately achieve desired operational frequency. Specifically, modification of the voltage-to-frequency mapping in a VCO post-irradiation would allow consistent control of operation frequency.

If a ring oscillator is used as an in-situ reliability monitor in a large circuit during application, again response to total dose in a harsh environment must be fully understood. In this paper irradiations were performed at high supply bias (i.e. 20 V corresponding to C2 and T2) for maximum total dose damage. However, characterization data was taken at a much lower supply bias (i.e. 1.5 V) as it provided the most meaningful total dose response results. As explained in the analysis, RO operational frequency is much more sensitive to changes in threshold voltage at low supply voltages.

For a reliability monitor it would be advantageous to bias the RO such that it best matches operation conditions in other critical sub-circuits on chip, possibly in a high voltage condition (i.e. $V_{DD} = 20$ V). However, assuming RO supply voltage is controllable in-situ, it could then be periodically and momentarily reduced (i.e. $V_{DD} = 1.5$ V) prior to RO frequency

sampling. As shown previously, the RO is significantly more sensitive to transistor TID degradation at this lower voltage. If well understood during design and simulation, the lower V_{DD} sample condition would give the greatest insight into radiation-induced shifts in the as-drawn threshold voltages as well as a radiation-induced activation of the parasitic edge NFET. With this information, radiation hardening by design (RHBD) decisions could be made, or even built into the design, based on the extracted degradation. For example it is possible reducing supply voltages and lowering operation frequencies in the crucial sub-circuits would extend circuit lifetime. This type of in-situ RHBD is only possible if designers have access to good predicative simulation techniques such as the methodology presented here.

CHAPTER 5

PREDICTIVE MODELING OF PARASITIC EDGE EFFECTS

Experimental characterization data is irreplaceable when trying to quantify the post-irradiated electrical response. However the process of gathering that data can be costly. Significant time and money is spent designing test die, developing fixtures such as PCBs and wiring as well use of lab time at a radiation source. Thus predictive modeling is attractive to reduce development cost.

In this chapter work is presented which was part of a greater effort to develop analog to digital converters (ADCs) for use in space. For this effort, test die and experimental irradiation data was not available. Thus a combination of TCAD device modeling, analytical parameter extraction and circuit simulation are used to estimate the radiation response of a 130 nm technology. By utilizing the approach, the circuit designer's simulation environment is enhanced to include predictive modeling of NFET intra-device leakage, allowing designers to make on-the-fly improvements to total dose hardness.

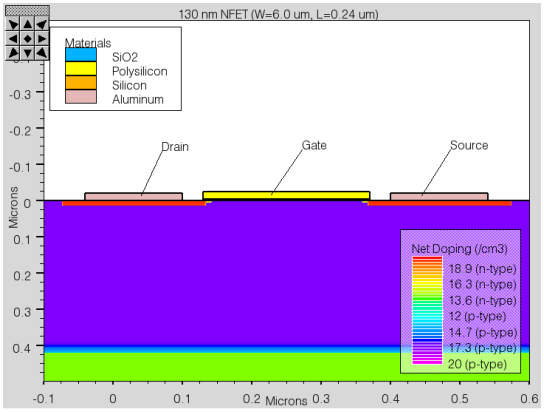
Approach

During development of an ADC, a designer would like to predict how their design would perform in the harsh environment of space; specifically how will the circuit perform after exposure to hundreds of krads of total dose. At early stages of circuit development, experimental irradiation test data is not available. The absence of post-irradiation current-voltage characteristics for transistors in the 130 nm technology consider here necessitates the use of a multi-step approach to analyze total dose effects. TCAD simulation with the Silvaco ATLAS REM model allows estimation of trapped charge build up due to ionizing radiation. Simulations

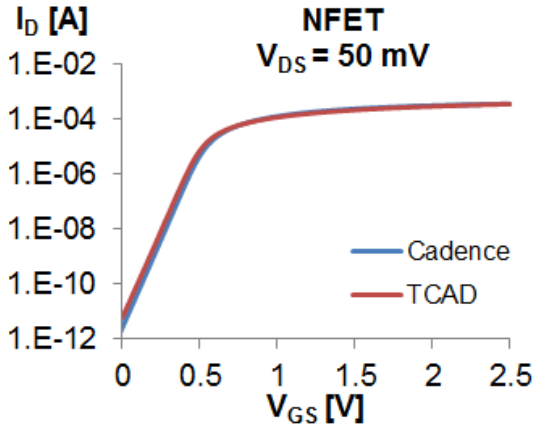
of 3 structures are performed: a standard NFET, a standard PFET and a structure representing the NFET isolation oxide sidewall. REM simulation reveals insignificant gate oxide charge trapping in both the NFET and PFET structures. Simulation of the NFET sidewall reveals significant oxide charge trapping in the NFET isolation oxide sidewall, which would cause a measureable increase in NFET intra-device leakage current. However, REM simulation is limited to 2-D TCAD structures, and to fully capture this intra-device leakage effect, a 3-D simulation would be required. To circumvent this issue and combination of analytical extraction is performed on the 2-D TCAD results and a circuit simulation technique is developed to capture the physically based TCAD response into total-dose-dependent compact models. The availability of compact models with total dose-dependent parameters allows designers to predictively simulate their circuit design's post-irradiated electrical response.

TCAD Device Modeling

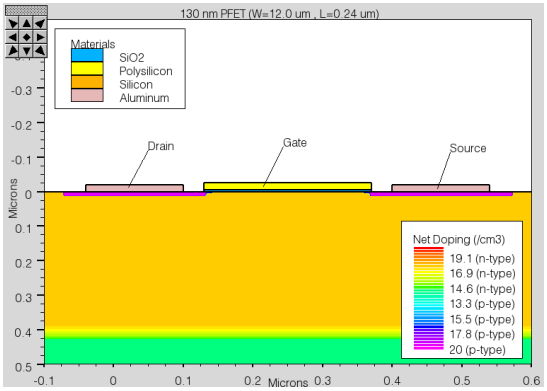
To represent the NFET and PFET from the 130 nm technology, three Silvaco TCAD structures were constructed. The first two 2-D structures, shown in Fig. 5.1, represent 2-D cross-sections of a standard NFET and PFET. TCAD modeling of the current-voltage characteristics for each device are calibrated against Cadence AMS simulation, using the foundry-supplied compact models. The resulting calibrated TCAD structures are then simulated in Silvaco ATLAS with the Radiation Effects Module (REM). REM is used in lieu of experimental irradiation data, as it allows an estimate of post-irradiation charge trapping in the N and PFET gate oxides. Simulation of NFET and PFET structures following REM simulated irradiation reveals no significant shift (~10 μV) in threshold voltage. This is expected, as device scaling has nearly-eliminated charge trapping in thin gate oxide [18, 39, 66, 80].



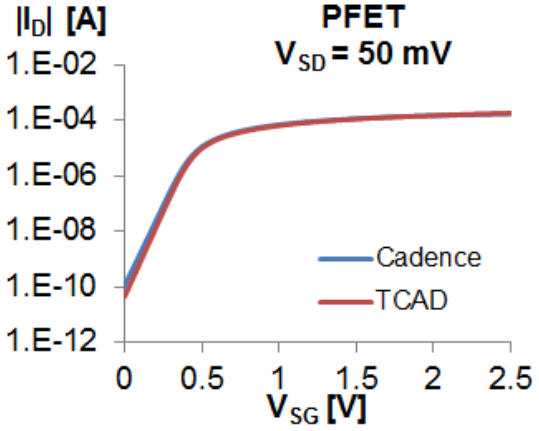
(a)



(b)



(c)



(d)

Fig. 5.1 2-D TCAD structures of the 130 nm (a) NFET and (c) PFET. TCAD modeled current-voltage characteristics of both (b) NFET and (d) PFET compare well against Cadence AMS simulation with the foundry-supplied compact models.

While gate oxide charge trapping is minimal, charge trapping along STI sidewalls is an on-going concern for n-channel transistors [18, 39, 56, 69]. Significant shallow trench isolation (STI) oxide sidewall charge trapping will result in activation of a “parasitic edge” transistor

leading to significant intra-device leakage in as-drawn NFETs. A 2-D TCAD structure was generated to represent the NFET sidewall, as shown in Fig. 5.2.

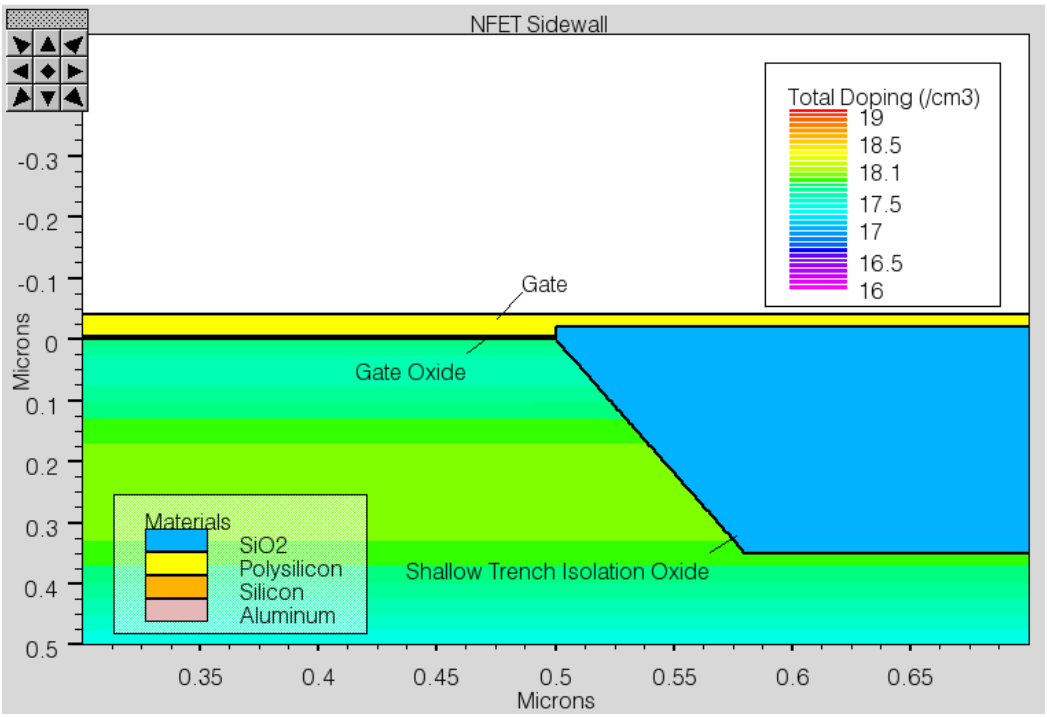


Fig. 5.2 2-D TCAD structure representative of an NFET sidewall. Drain-to-source current flow would be in the z-direction in this 2-D structure.

Subsequent Silvaco ATLAS with REM simulation allows for the calculation of charge trapping along the STI sidewall. The resulting oxide trapped charge profiles within the STI are shown in Fig. 5.3. The exhibited positive charge trapping will increase surface potential (ψ_s) at the Si/SiO_2 interface along the sidewall, which would be revealed as increased off-state leakage currents in the NFET. The increased off-state current is modeled as a "parasitic edge" transistor that conducts significant current in parallel with the "as drawn" NFET post-irradiation. Because the simulated NFET sidewall is a 2-D structure, the effect on NFET intra-device current cannot be captured. To circumvent this restriction, analytical and simulation methods are used to

correlate the results of oxide-trapped charge buildup in the STI to a corresponding intra-device current along the STI sidewall. This was accomplished by: 1) extracting structural electrical information from TCAD simulation structures 2) utilizing the information in analytical calculations resulting in 3) parameterization of the "parasitic edge" transistor for use in AMS simulation.

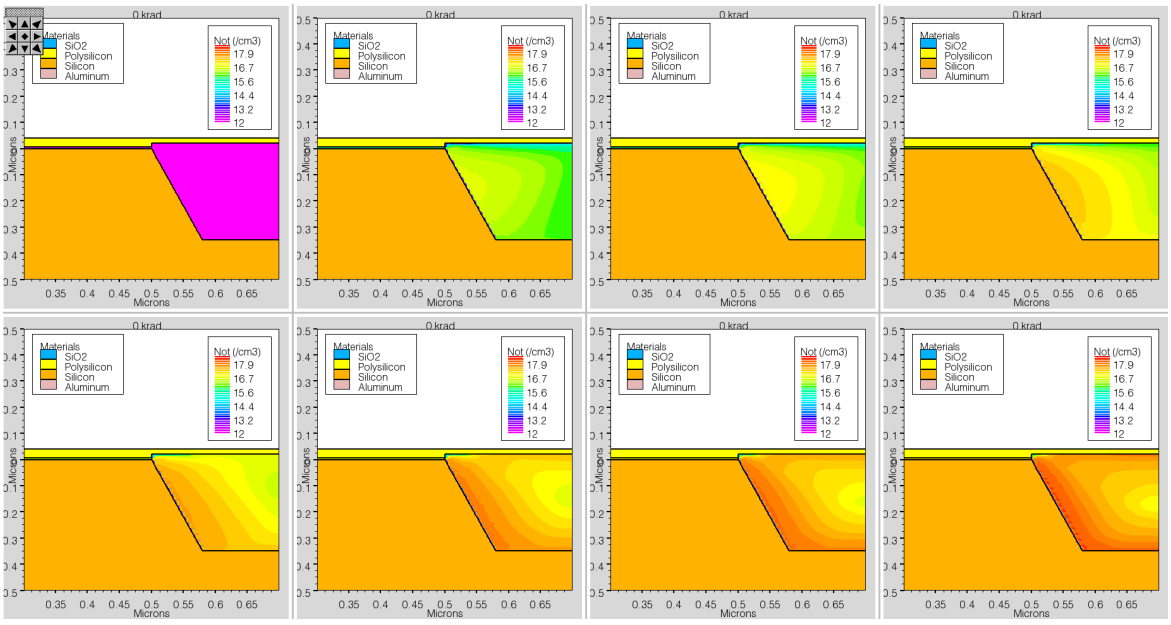


Fig. 5.3 Results of the ATLAS with REM simulation at increasing total dose levels illustrate the buildup of fixed oxide trapped charge (N_{ot}) along the STI sidewall. Total dose levels of 0k, 10k, 20k, 50k (top row, left to right) and 100k, 200k, 300k and 500 krad (bottom row, left to right) are shown.

Analytical Extraction of Parasitic NFET Parameters

To enable circuit simulation of the parasitic NFET, the simulated TCAD response shown must be quantified into a set of BSIM parameters. Within the BSIM4 compact model framework, threshold voltage (V_T), doping (N_A) and oxide thickness (t_{OX}) can be directly defined within a compact model. From the 2-D NFET sidewall structure (Fig. 5.3) the position-dependent doping

is extracted by taking a cutline along the STI sidewall (Fig. 5.4). To assign an effective oxide thickness along the depth of the STI sidewall, the arc-length formula is applied

$$t_{ox}(z) = 2\pi z \frac{\theta}{360} \tag{5.1}$$

Where z is position along the depth of the STI, and θ is the STI sidewall angle (θ=77˚).

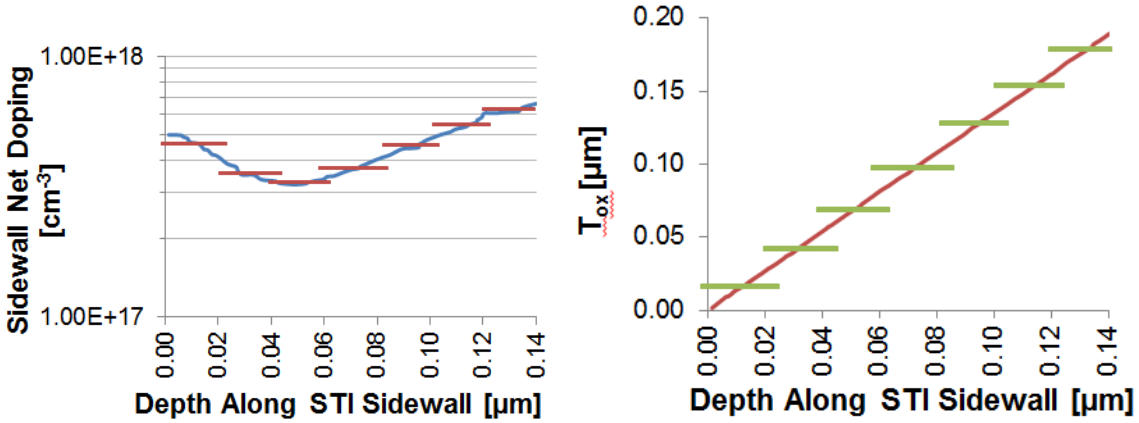


Fig. 5.4 Extracted Sidewall Doping vs. sidewall depth (left) and calculated effective oxide thickness vs. sidewall depth (right). Overlaid horizontal lines indicate the average value over a 20 nm depth increment.

ATLAS allows structure files to be saved during simulation, containing position-dependent electrical information, including potential within the Silicon. Structure files were saved prior to REM simulated irradiation and after each total dose stress step level (Fig. 5.3). From these structure files, a cut-line was obtained directly parallel to the STI sidewall, in the silicon, allowing extraction of the position-dependent surface potential at each total dose level. As total dose increases, positive charge trapped in the STI increases. This, in turn, increases the surface potential along the sidewall at each total dose stress, illustrated in Fig. 5.5.

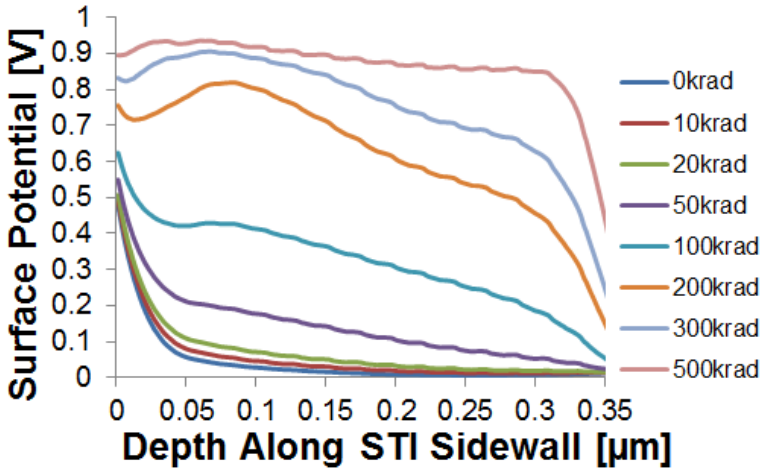


Fig. 5.5 Extracted surface potential along STI sidewall for each total dose stress step shown in Fig. 5.3.

At this point, position (z) dependent oxide thickness and doping have both been defined (Fig. 5.4). The third BSIM parameter needed is threshold voltage. Utilizing the position (z) and total dose (D) dependent surface potential (Fig. 5.5), threshold voltage can be calculated. Threshold voltage is defined as [81]:

$$V_T(D,z) = V_{FB}(D,z) + 2\phi_f(z) + \gamma(z)\sqrt{2\phi_f(z)} \tag{5.2}$$

where ϕ_t is the thermal voltage, $\phi_F(z)$ is the position-dependent Fermi potential, gamma is defined as:

$$\gamma(z) = \sqrt{2q\varepsilon_{Si}}\sqrt{N_A(z)}/C_{ox}(z) \tag{5.3}$$

and oxide capacitance can be written

$$C_{ox}(z) = \varepsilon_{ox}/t_{ox}(z) = \varepsilon_{ox}/2\pi z\frac{\theta}{360}. \tag{5.4}$$

Flatband voltage (V_{FB}) is defined as [81]:

$$V_{FB}(D,z) = \psi_s(D,z) + \gamma(z)\sqrt{\psi_s(D,z) + \phi_t e^{(\psi_s(D,z) - 2\phi_f(z))/\phi_t}} \tag{5.5}$$

Employing Eqs. 5.2-5.4 as well as the results presented in Fig. 5.4 and Fig. 5.5, the threshold voltage along the sidewall depth can be calculated, as shown in Fig. 5.6.

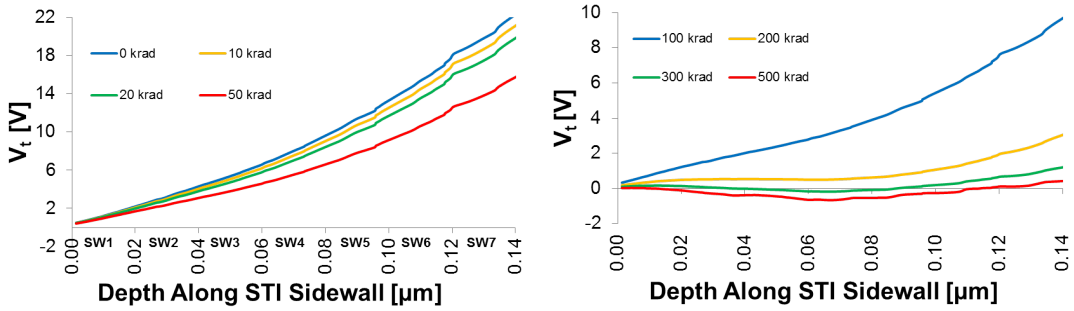


Fig. 5.6 Extracted threshold voltage along STI sidewall for each total dose stress step shown in Fig. 5.3. Divided in two charts for clarity.

As expected, pre-irradiation (0k rad) threshold voltage is large and increasing along the depth of the sidewall. It is evident that threshold voltage decreases dramatically with increasing total dose.

Implementation in Simulation

Within the BSIM4 compact transistor models, $V_{T,}$ N_A and t_{OX} can be directly defined within a new model for the parasitic transistor. However, all 3 parameters as previously extracted change continually along z, as shown in Fig. 5.4 and Fig. 5.6. For simulation a constant model value is needed for a given device instance is appropriate. Using a methodology modified from previously published technique, the parasitic edge transistor is divided into seven incremental parasitic edge transistors (labeled SW1-SW7) of nominal gate width W_i=20nm [39, 76], for which the extracted profiles for $V_{T,}$ N_A and t_{OX} are averaged over the 20 nm depth increment. This results in constant value for N_{Ai} , t_{OXi} and V_{Ti} for each of seven incremental transistor at

each total dose step, to be defined within the parasitic-edge transistor's compact model. This effectively steps the parasitic edge transistor's response, correlated to a chosen total dose level. Table 5.1and Table 5.2 summarize extracted values to be used in simulation.

Table 5.1 Incremental oxide thickness (T_{OXi}) and doping (N_{Ai}) for each of the seven parasitic edged transistors. Values extracted from Fig. 5.4 results.

Incremental Parasitic Edge Transistor	T_{OXi}	N_{Ai}
SW1	15.3 nm	4.62×10^{17} cm^{-3}
SW2	41.8 nm	3.58×10^{17} cm^{-3}
SW3	68.7 nm	3.29×10^{17} cm^{-3}
SW4	96.7 nm	3.74×10^{17} cm^{-3}
SW5	127.2 nm	4.56×10^{17} cm^{-3}
SW6	153.3 nm	5.50×10^{17} cm^{-3}
SW7	178.1 nm	6.28×10^{17} cm^{-3}

Implementation of the seven parasitic edge transistors into simulation is accomplished by creation of a new NFET sub-circuit (Fig. 5.7), used as a direct replacement for a single NFET device in simulation. The sub-circuit consists of 4 main sections: the "as drawn" NFET, a network of seven parasitic edge NFETs, four voltage-controlled voltage sources and one current controlled current source. The as-drawn NFET is a replication of the NFET the sub-cell is to replace. The parasitic edge NFET network represents the incremental parasitic edge transistors (SW1-SW7), as described previously.

Table 5.2 Incremental threshold voltage (V_{Ti}) for each of the seven parasitic edged transistors at each total dose stress step modeled in TCAD. Values extracted from Fig. 5.6 results.

	Total Dose Stress Step						
Incremental Parasitic Edge Transistor	**0 krad**	**10 krad**	**20 krad**	**50 krad**	**100 krad**	**200 krad**	**500 krad**
SW1	1.38 V	1.32 V	1.26 V	1.09 V	0.81 V	0.37 V	0.14 V
SW2	3.35 V	3.16 V	2.98 V	2.46 V	1.66 V	0.52 V	0.05 V
SW3	5.52 V	5.20 V	4.86 V	3.90 V	2.43 V	0.52 V	-0.09 V
SW4	8.33 V	7.84 V	7.36 V	5.75 V	3.42 V	0.55 V	-0.14 V
SW5	12.16 V	11.46 V	10.68 V	8.36 V	4.95 V	0.91 V	0.11 V
SW6	16.28 V	15.37 V	14.37 V	11.29 V	6.79 V	1.61 V	0.49 V
SW7	20.43 V	19.31 V	18.10 V	14.32 V	8.75 V	2.54 V	0.95 V

A voltage-controlled voltage source (VCVS) is then used to sample the as-drawn NFET nodal bias conditions (V_{DS}, $V_{GS,}$ V_{SS} and V_{BS}) and applies bias to the parasitic edge NFET network. The VCVS source mirrors bias conditions from the as-drawn NFET to the parasitic edge NFET network while decoupling the network's capacitance from the circuit. Finally a current-controlled current source (CCCS) is placed in parallel with the as-drawn NFET. The CCCS then samples the current through the parasitic edge NFET network, and replicates that current. CCCS inclusion is required due to VCVS inclusion, which decoupled the as-drawn and parasitic edge transistors. Additionally use of the CCCS to sample parasitic edge network currents is useful as we can avoid narrow channel effects within the parasitic edge models. If a 20 nm gate width are used for each of the 7 parasitic edge NFETs, short channel models would be active within the BSIM4 model. To avoid this, a 2 μm gate width is used, but then a $1/100^{th}$ multiplication factor is used in the CCCS to result in an current magnitudes equivalent to a 20

nm gate width case. This sub-circuit methodology results is a current flow in parallel to the as-drawn NFET equal to that of the parasitic edge transistor.

With the NFET sub-circuit substituted for an as-drawn NFET, successive Cadence AMS simulation while exchanging V_{Ti} values at a known total dose stress step effectively steps the total dose level for the NFET sub-cell.

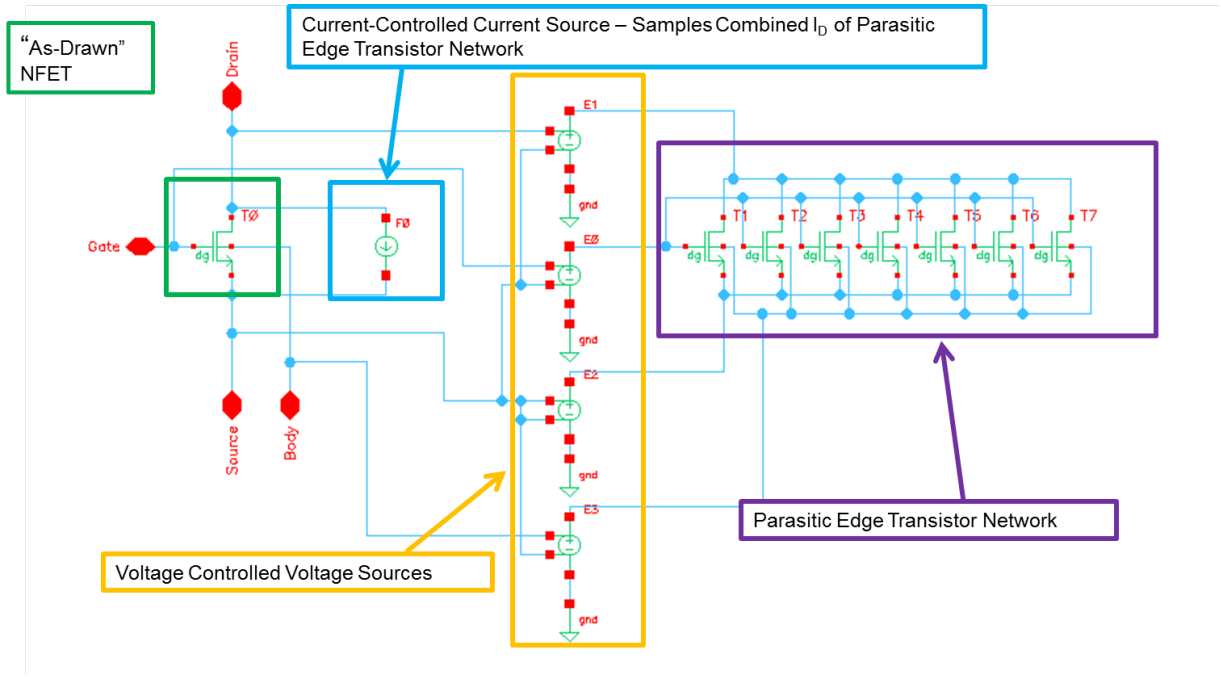


Fig. 5.7 NFET sub circuit used as a drop-in replacement for regular NFET's in a given design.

Simulation Results

Simulation of the NFET sub-circuit illustrates the predicted drain current response, as shown in Fig. 5.8, of an "irradiated" NFET at increasing total dose stress steps. From the simulated current voltage response, it is evident that at 50 krad, the parasitic edge NFET begins to contribute to the combined sub-circuit off-state (V_{GS} = 0 V) current, and at higher doses (i.e. 100 – 500 krad) the off-state current is significantly increased. From this simulation result the

off-state current as a function of simulated total dose can be determined, as shown in Fig. 5.9. If NFET devices, within any arbitrary circuit, exhibited this dramatic increase off state current, it would significantly degrade transistor performance, increase overall supply current and likely lead to complete circuit failure.

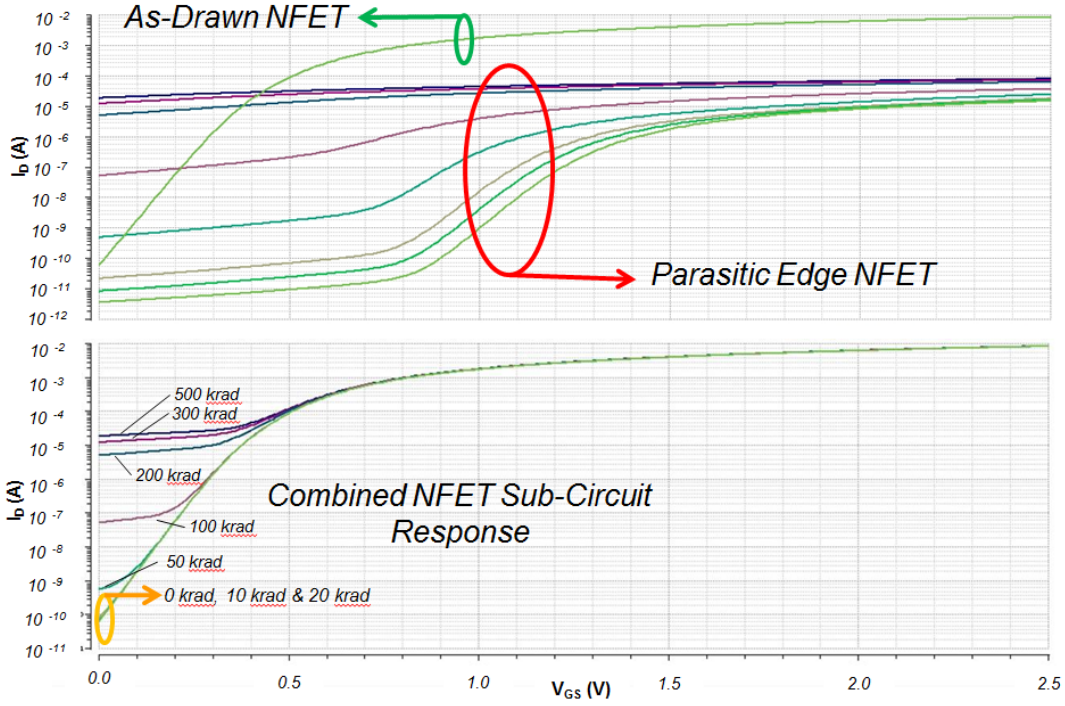


Fig. 5.8 Drain current vs. gate voltage response of the NFET sub-circuit at various simulated total dose stress steps. The top panel breaks the drain current into two components: that of the as-drawn NFET and the response of the parasitic NFET. The bottom panel illustrates the combined drain current response of the as-drawn and parasitic edge NFETs acting in parallel.

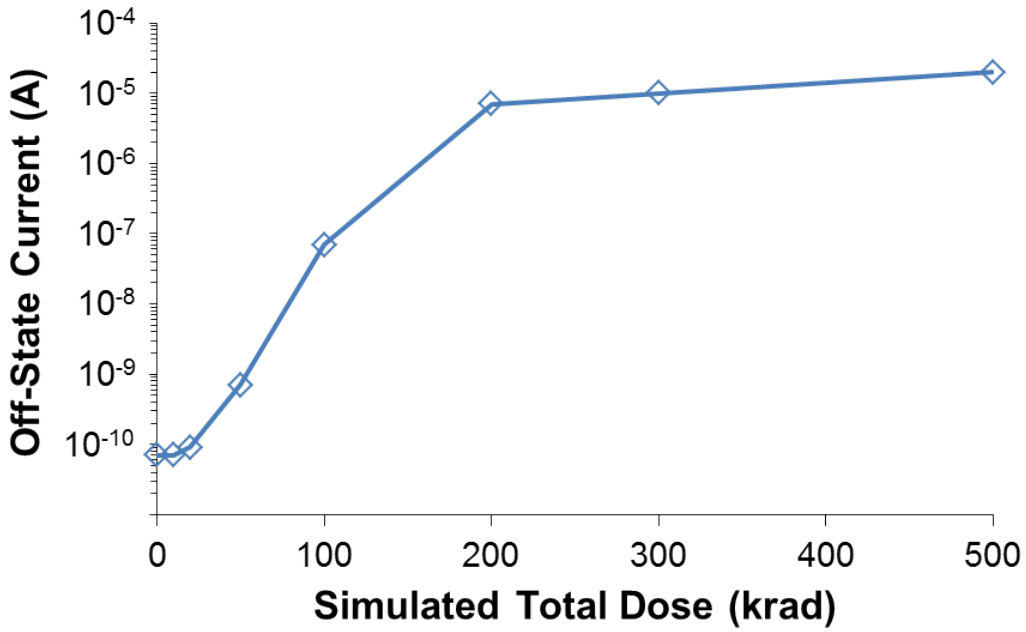


Fig. 5.9 Off-state (V_{GS} = 0 V) current vs. simulated total dose for the NFET sub-circuit.

Summary of Predictive Modeling

A methodology was presented for which predictive modeling and simulation is performed to anticipate degradation of an NFET following irradiation. Through 2-D TCAD simulation with total dose modeling capability, the buildup of trapped oxide charge is modeled. By way of analytical methods, the TCAD results are parameterized into constant values, suitable for substitution into a parasitic edge transistor compact model. A novel NFET sub-circuit is then implemented to allow simulation of the "post-irradiated" parasitic edge transistor in parallel with the "as-drawn" transistor. Simulation results reveal a significant increase in NFET off-state current, representative of parasitic intra-device current along the STI sidewall.

While experimental irradiation data is the best way to characterize the total dose response of a given transistor or circuit, predictive modeling presents a comparatively inexpensive and fast alternative. Access to modeling and simulation results like those presented would allow a

designer to predict the total dose response of their circuit during design, and make on-the-fly radiation hardening by design choices to improve post-irradiation performance.

CHAPTER 6

CONCLUSIONS

Summary and Contributions

The impact total dose irradiation has on reliability is a concern for any application for which radiation exposure is possible. However, this does not mean that the same total dose reliability hardness protocols should be applied in every case. Designers must understand early in the design cycle: 1) the radiation environment anticipated for their design, 2) the relative total dose susceptibility of devices manufactured in the chosen process technology and 3) the potential weak points in their circuit design. All 3 factors must work in concert with logistical concerns such as design cycle time and cost constraints to produce circuits that optimally perform over the required lifetime.

In deep space applications total dose effects are of chief concern. Doses can reach hundreds Mrads and failure of a single IC can lead to mission failure, spoiling years of effort and costing significant amounts of money. Thus great effort is taken in the design planning stages to meet and exceed hardness requirements. Process technologies are developed specifically for total-dose hardness; ultra-thin oxides limit charge trapping and hardening-by-design layout techniques are available as part of the standard hardening practice. Groups of engineers work specifically to predict the radiation environment as well as perform total dose characterization, mimicking in-situ conditions. All tasks are considered “mission critical” to the design thus are a necessity regardless of the cost and effort.

Alternatively other applications like implantable medical devices face a much different potential radiation environments and thus must prioritize their hardening efforts. Total dose levels will be much lower, often below a few krad, and exposure to radiation is not a certainty. This pushes total dose hardness down in prioritization in favor other concerns in an effort to

reduce cost and time to market. However, total dose cannot be ignored, as a single field failure of a circuit can have far reaching implications impacting the products perceived quality. Systemic failures would be even more deleterious, as products could be restricted from sale if there is a perceived danger to patients. Understanding the high potential risks is counterbalanced against cost, both in real dollars and effort.

While experimental irradiation and characterization of the final circuit design provides the ultimate measure of potential failure modes, this methodology can prove costly as it may be too late to implement necessary design to meet targeted total dose hardness levels. Designers must be empowered with understanding of the total dose response of their circuit as early as possible, ideally at each stage of design. This allows for targeted, iterative total dose hardening of only the most critical and susceptible circuit sub-cells. Techniques for simulating total dose effects, as presented here, offer the insight needed to achieve hardness, while not sacrificing other design goals and keeping hardening costs in check.

The dissertation is 6 chapters, focusing on techniques simulating total dose effects in high reliability electronic applications. The early chapters consist of background material detailing applications for which the presented simulation techniques are relevant, as well as details on the physical mechanisms of total dose effects and their impact on device operation. The rest of the dissertation focuses on two main effects, categorized as inter-device and intra-device effects.

Simulation of total dose induced inter-device leakage is demonstrated to analyze the loss of device isolation following irradiation. In the presented case study a charge pump, which is used to generate a battery-multiplied supply rail in an implantable pacemaker, is examined. Irradiation results reveal collapse of charge pump voltage with increasing total dose. Through analysis of circuit layout as well as irradiation of individual test structures, it is determined inter-

device leakage beneath LOCOS isolation oxides, through parasitic FOXFET structures, is responsible for the voltage collapse. The dataset is further enhanced via TCAD modeling of the inter-device leakage, and the combination of experimental and TCAD data is utilized to develop post-irradiation compact models for the parasitic FOXFET. Back-annotation of FOXFETs into the charge pump circuit schematic allows inclusion of total dose effects into simulation. Simulation results reveal collapse of the charge pump output voltage, confirming the post-irradiation inter-device leakage as the cause of experimentally observed response. Follow up work further investigated the nature of post-irradiation inter-device leakage paths. Test structures were specifically designed and characterized to analyze the "best fit" width to length aspect ratio of irregularly-shaped parasitic FOXFETs devices. Having accurate aspect ratios along with post-irradiation compact models increases credibility of circuit-level simulation of total dose effects.

Intra-device total dose effects can also lead to changes in circuit operation, and potentially circuit failure. Especially susceptible are commercial technologies that support higher voltages due to their thicker gate oxides and high electric fields. In the presented case study of a ring oscillator, it is revealed via experimental irradiation and characterization that both the ring oscillation frequency and supply current are both dramatically affected following exposure to x-rays. Through analysis it is found that combined effects of intra-device mechanisms, shifts in as-designed threshold voltages for both the NFET and PFET as well as a dramatic increase in off-state current for the NFET, are responsible for the observed change in circuit operation. These results are confirmed via a novel simulation methodology utilizing experimental data to extract parameters for total-dose enabled compact model parameters. Good agreement between experimental and simulated electrical response confirm the root cause of degradation. Not only does the work presented provide insight into the post-irradiation response of ring oscillators, it

also serves as basis for recommended future work: using ring oscillators as in-situ circuit health monitors for total dose effects.

In other cases, post-irradiated experimental data may not be available due to test time constraints, part availability or cost of testing. However, designers can gain insight into post-irradiated circuit response by way of TCAD modeling and predictive circuit simulation. In the work presented, TCAD simulation serves to predict the trapped charge buildup along the shallow trench isolation oxide sidewall. The 2D response is then correlated, through analytical methods, to compact model parameters used with the foundry-supplied process design kit. The result effectively estimates the expected contribution of parasitic edge leakage in NFETs, and gives the designer a useable measure to judge circuit level total dose response. While experimental results are nearly irreplaceable, the method presented can give the designer a rapid sense of radiation hardness, for a very low total cost.

Recommendations for Future Work

Continual advancement of total dose simulation techniques will continue to improve accuracy of simulation and reduce the time and cost for design-for-reliability programs, including minimizing the amount of experimental characterization needed. Some recommendations for future work include:

- Apply and refine methodologies presented in various other circuit designs and technologies to improve their robustness and accuracy.
- Implement total dose simulation techniques into front-end design flows to harden new circuit designs.

- Develop of “external” total dose models, such that foundry-provided compact models can remain un-edited but total dose circuit simulation can still be achieved.
- Create experimental testing and modeling studies to investigate the degradation of oxides under switched bias conditions. Currently models represent damage in test devices at static bias conditions, while integrated circuit field exposures occur during normal operation with dynamic electric field conditions.
- Implement of ring oscillators as in-situ circuit health monitors. Utilize the change in oscillation frequency as an indicator of total dose degradation as a circuit health monitor. Health monitor status could pass its status to other parts of custom ASICs, to where more critical sub-circuits could modify operation (de-rate voltages, slow clock cycles),extend system lifetime and reduce chance of complete failure.
- Refine 2D TCAD solutions and expand into 3D TCAD to include total dose simulation models to better predict total dose response. Both 2D and 3D TCAD modeling can greatly enhance an existing experimental dataset, or serve as a replacement when no experimental characterization has been performed.

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